Investigation of the Effects of Parasitic Components on Parallel and Series Connected Modular Motor Drives

Abstract: In this paper, DC link capacitor current and voltage ripple under the effect of parasitic inductances for a GaN based integrated modular motor drive (IMMD) are investigated. The variation in the interleaving scheme when inverter modules are connected in series or parallel are presented. The IMMD system used for the experiments has 4 inverter modules each having 270 V DC bus voltage and 2 kW output power.

1 Introduction

Integrated modular motor drives (IMMD) gained special interest in recent years thanks to their high power density and fault tolerance capability. Modular motor drives increase redundancy of the system which is desired in safety critical applications [1]. Moreover, power semiconductor devices with low voltage ratings such as Gallium Nitride (GaN) Field Effects Transistors (FETs) can be utilized, resulting in higher efficiency and higher power density [2]. There are several IMMD designs which have different types of modularity in terms of DC link connection, such as series connected [2] and parallel connected [1,3] topologies. In series connected drives, the main motivation is to utilize low voltage GaN devices in a higher DC link voltage. Parallel connection is used to distribute the heat dissipation surface and reduce the size of DC link capacitors by interleaving [4].

However, modular usage of voltage source inverters (VSI) brings its own challenges. Circulating currents and unbalanced voltages may occur and the parasitic components due to the physical connections between the modules may result in unbalanced stress on module capacitors. Therefore, careful layout design is required in order to minimize these effects, however too few studies in the literature give special attention to the parasitic components in modular drive topologies. In [5], two candidate DC bus architectures are compared in terms of DC bus current oscillations due to layout inductances.

In this paper, the effects of PCB parasitic inductances are investigated in a GaN based IMMD. The overshoots on GaN voltages due to power loop inductance are investigated. The actual DC link capacitor current stress and voltage ripples are analyzed considering commutation inductances between phases. Series and parallel connected inverter modules and the effect of connection inductances to their performance are analyzed.

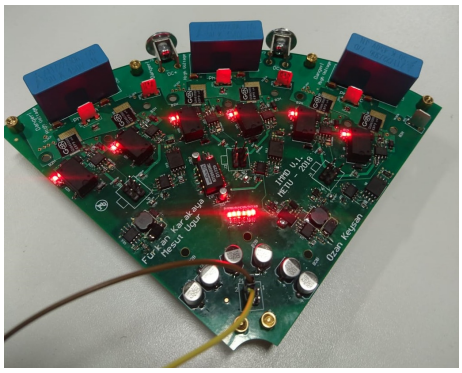


Fig. 1: 2 kW GaN based 3-phase inverter module

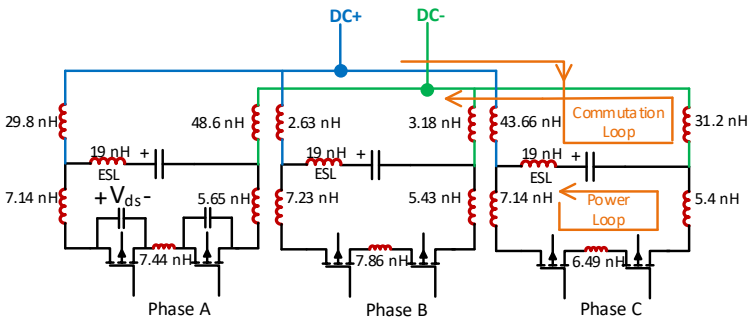
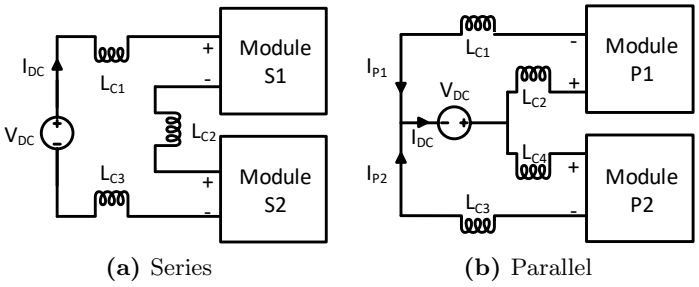


Fig. 2: Parasitic Inductance Map of a Single Module



(a) Series **(b)** Parallel

Fig. 3: Series and Parallel Connected Modules Configurations

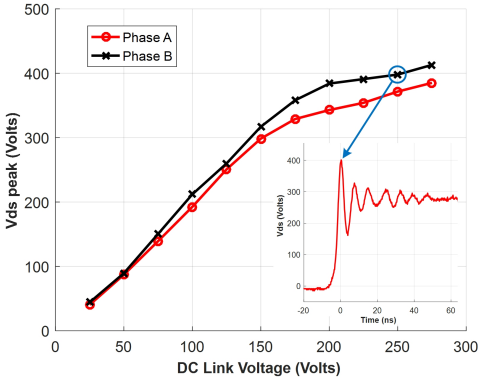


Fig. 4: Experimental voltage overshoot results

2 Description of the Modular Drive

The proposed IMMD is composed of 4 identical modules, one of which is shown in Fig. 1. The modules can be connected in series or parallel on the DC link. Single inverter module is rated at 2 kW at a DC link input of 270 V. Four modules drive a permanent magnet motor rated at 8 kW.

The module consists of half-bridge legs with GaN FETs having 650 V and 30 A ratings. Each leg has a 5 μF metal film capacitor, isolated gate driver dedicated to each GaN and a phase current measurement circuit. It is aimed to minimize the power loop and commutation loop inductances by placing DC link metal film and ceramic capacitors as close as possible.

For the inverter circuit given in Fig. 1, the power loop and commutation loop inductances are calculated using ANSYS/Q3D finite element analysis tool as given in Fig. 2. The power loop is effective when a switching occurs between top and bottom switches on a half-bridge, and the commutation loop is effective whenever current commutes from one phase to another.

As shown in Fig. 3, two modules can be connected either in series or in parallel. L_{C1} & L_{C3}, are total equivalent inductances of connectors and module to supply terminal connections and L_{C2} represents the total inductance of the connectors and the module to module connection.

3 Investigation of a Single Inverter Module

3.1 Power Device Stress

As shown in Fig. 2, the power loop includes two switches and single phase capacitor. When the phase current transfers from one switch to the other, the power loop parasitic inductances cause a voltage overshoot on the drain-source terminals of a switch as much as $L_p * di/dt$. Due to fast switching capability (i.e. high di/dt) of GaN FETs, the power loop inductance is the most important factor for device stress. Experimental results of device stress are presented in Fig. 4 for various DC link voltages. It can be seen that the peak stress on phase-B is higher since its power loop equivalent inductance is slightly larger than phase-A.

3.2 DC link Capacitor Stress

The DC link capacitors on each half-bridge are used to supply and sink the current ripple during switching periods. The power loop inductances are not effective on these capacitors' stress assuming ceramic capacitors are placed in much closer proximity. When the parasitic inductances are of considerable amount on the commutation loop, the stress of individual capacitors increase due to the longer path which the other capacitors have, as shown in Fig. 5. This results in higher capacitor RMS currents than analytically calculated values in [4] as shown in Fig. 6. This extra ripple current can increase the capacitor temperature and shorten its lifetime.

4 Investigation of Series and Parallel Connection

4.1 Series Connection

The DC bus voltage ripple of each module along with total DC bus are shown in Fig. 7. It has been shown that interleaving only reduces the ripple on total DC bus which has no positive effect on the modules since the module voltage ripples remain the same. Moreover, the capacitor ripple currents are not affected by interleaving since they simply have to conduct the same amount of current in series connection. Therefore, interleaving on series connection does not reduce the size of DC bus capacitors, although it is claimed so in the literature [2].

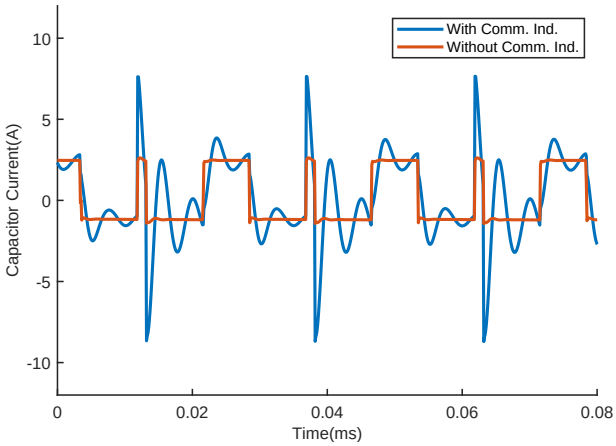


Fig. 5: DC bus capacitor current ripple with and without commutation loop inductances

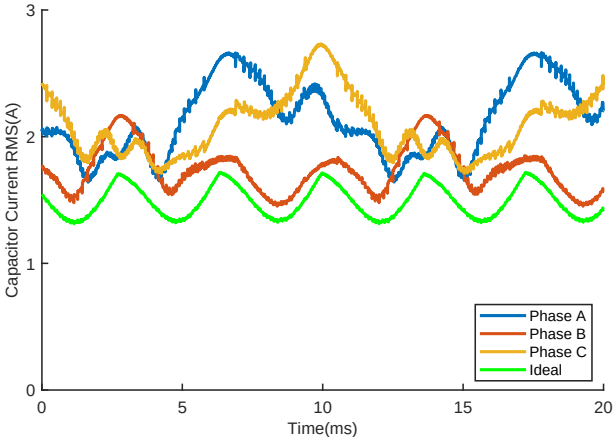


Fig. 6: Variation of RMS values of capacitor currents with and without commutation inductances

4.2 Parallel Connection

The parallel connection is usually favored to reduce the size of DC bus capacitors with interleaving. However, if the gate signals of two modules are phase shifted with proper angle, transition (circulating) currents between modules emerge, as shown in Fig. 8. The reduction on the capacitor current stress when interleaving is applied in parallel connected modules has been shown for different number of modules and phase shift angles in [4]. However, this analysis is only valid for ideal case where commutation and connection inductances are ignored. The RMS of capacitor currents with and without interleaving and parasitic inductances suggest that actual RMS current is larger as shown in Fig. 9. On the other hand, unlike series connection, interleaving can still be used in parallel connected modules to reduce the module voltage ripple, as shown in Fig. 10.

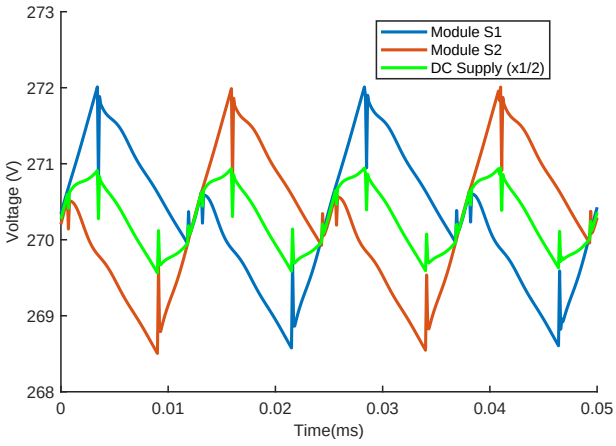


Fig. 7: DC bus voltage ripple in series connected modules

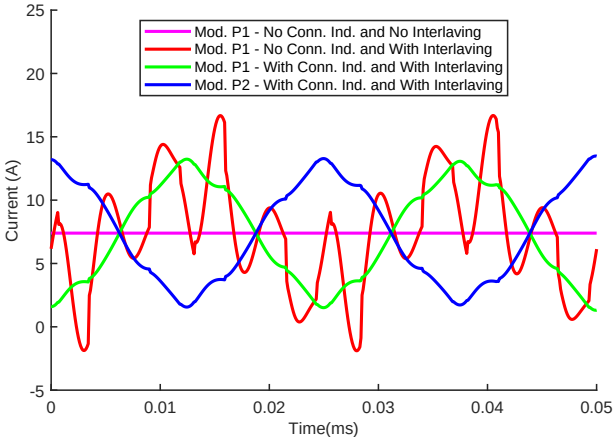


Fig. 8: Current transition occuring due to interleaving in parallel connected modules

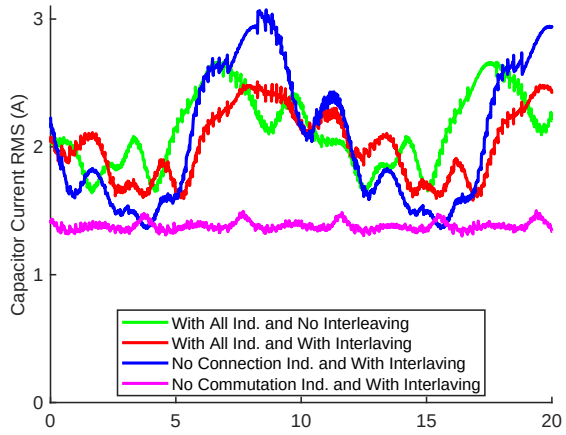


Fig. 9: Variation of DC bus capacitor current RMS in parallel connected modules

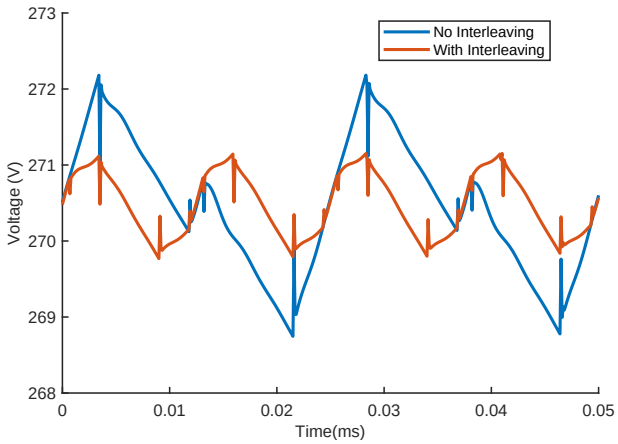


Fig. 10: Module DC bus voltage ripple with and without interleaving in parallel connected modules

5 Conclusion

In this paper, the effects of parasitic inductances on a modular motor drive are investigated. It is shown that device stress is only affected by the power loop inductances, whereas capacitor stress is caused by the commutation inductances. In series connected converters, interleaving has no useful effect on the capacitor stress and module voltage ripple. On the other hand, capacitor stress can be reduced by parallel connection with interleavig. However, the capacitor currents are not significantly reduced when parasitic inductances are taken into account. In the final paper, a complete analytical model will be introduced including parasitic inductances, number of modules and the interleaving effects. Inverter modules of the aforementioned IMMD prototype will be tested with series and parallel connection combinations and the experimental results will be presented.

References

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