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A DC Bus Capacitor Design Method for Various Inverter Applications

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***Abstract* - This paper involves the selection and sizing of the appropriate type of dc bus capacitor for various applications utilizing PWM operated three-phase voltage source inverters, such as battery operated systems, PV (photovoltaic) systems, UPSs, and motor drives. It classifies the power converter topologies based on dc bus ripple current frequency characteristics. A general approach for ripple current characterization is provided. Based on these characteristics, the two capacitor types suitable for this purpose, the electrolytic and film capacitors, used in inverter applications are reviewed. Capacitor power loss and voltage ripple calculation are provided for both types. Then, a thorough algorithm for dc bus capacitor design is provided. The application of the proposed design method is demonstrated through several design examples. Overall, the paper helps the power electronics development and design engineer in the design and performance evaluation procedure of dc bus capacitors for three-phase inverters. The method is simple but rigorous and accurate.**

I. INTRODUCTION

Three-phase power electronic conversion systems are widely utilized in motor drive, renewable energy, uninterruptible power supply (UPS), etc. systems for conditioning of the electric power. Many of these topologies, such as ac grid fed ac-dc-ac converters (motor drives, UPS systems, wind turbine generators, etc.) and dc source fed dc-ac converters [photovoltaic (PV) systems and battery fed applications, etc.] use three-phase voltage source inverters (VSIs). Very often, a boost converter also follows the PV or dc battery sources to increase the dc bus voltage before the inverter stage. The generic power conversion system structure is shown in Fig. 1 for all such systems. In all mentioned applications, the inverter sides of the circuits have very similar topologies and the circuits on the other side of the dc bus are the stages creating the variety among converter systems. The inverter is typically a three-phase, two-level VSI, while the other side may be of various structures such as diode/thyristor/transistor rectifiers, dc-dc converters, or just simple passive filters.

In all inverter applications, the dc bus faces high frequency ripple current due to high frequency pulse-width modulation (PWM) switching of the inverter. It also faces either low or high frequency ripple current from the source side converter depending on the source and converter type. The dc bus capacitor (C_{dc}) is utilized to both reduce the voltage ripple and bypass the current ripple. The topology of an application dictates the type and size of the appropriate capacitor, since it determines the ripple current frequency spectrum characteristics. Then, the current ripple determines the voltage ripple.

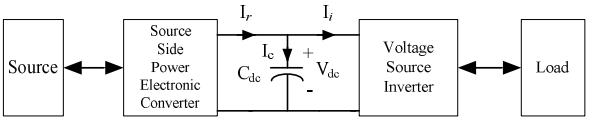

Figure 1. Generic power conversion system employing VSIs

Many studies have been conducted for design and optimization of C_{dc} for inverters [1]-[7]. One of the methods is conducting experiments to find the optimum capacitor size, which is too laborious and costly. Simulations may give insight and lead to a good design, but they are time consuming since each simulation is run for a specific operating condition involving large number of parameters. Instead, designing C_{dc} via an analytical approach involving a design algorithm reduces effort and cost and is intuitive. For C_{dc} size, ripple, and loss calculations, however, conventional approaches use very approximate (often empirical) formulas. Hence, either limited thermal reliability or conservative design; a rigorous approach is lacking. In addition, there is no broad classification and investigation of topologies based on the dc bus ripple current frequency characteristic. Thus, design rules have been considered application specific.

This paper provides a rigorous method for C_{dc} design for inverter applications, by primarily taking the current ripple characteristics (frequency spectrum) of both sides of the dc bus into account accurately. First, inverter applications are classified and characterized in terms of dc bus current ripple behavior. Second, the dc bus capacitor technologies are reviewed. Then, the ripple, loss, and size calculation methods are provided leading to the design algorithm. Then, full design examples follow. Motor drives with diode rectifier and regenerative front ends and transformerless UPS systems are considered.

II. TOPOLOGIES UTILIZING INVERTERS AND THEIR RIPPLE CURRENT CHARACTERISTICS

In all practical topologies in use, the inverter used in the dc-ac conversion stage injects high frequency current ripple to the dc bus. In the case of dc sources (battery or PV systems), if the sources are directly connected to the dc bus, no current ripple is injected to the dc bus from the input. If a boost converter takes place between the battery (or PV system) and the dc bus, the boost converter injects high frequency current ripple to the dc bus. At the input, if ac-dc conversion stage is used, again input current ripple is injected to the dc bus. Diode or thyristor rectifiers cause

low frequency current ripple, whereas PWM rectifiers impose high frequency current ripple to the dc bus. These topologies are tabulated in Table I according to the frequency characteristics of the dc bus current ripple.

The first topology considered, shown in Fig. 2, is the three-phase diode/thyristor rectifier cascaded with PWM inverter (widely used in motor drive applications). The diode rectifier generates 6-pulse voltage waveform at the dc bus. With the grid frequency being f_{re}, the dc bus voltage harmonics occur at $6f_{re}$ and its multiples, with the first being very dominant. With the PWM-VSI carrier frequency f_{ic} being much higher than $6f_{re}$, these harmonics are considered as low frequency (LF, under kHz) harmonics. As the dc bus impedance is high at low frequencies, large voltage and current ripple are generated in the dc bus due to the diode rectifier. This behavior is illustrated via the dc bus voltage and current waveforms in Fig. 3 and the corresponding dc bus current harmonic spectrum of Fig. 4 obtained from the simulation of a 29 kW induction motor drive (C_{dc}=5 mF, L_s= L_{dc}=620 µH) fed from 50 Hz, 220 V rms/phase grid. As the graphics illustrate, for 50 Hz grid, the dc bus current dominant harmonic is at 300 Hz and the magnitude of the spectrum decreases rapidly with the increasing frequency.

The inverter side of the drive injects PWM current ripple to the dc bus. This current ripple occurs at the carrier frequency, its multiples, and sidebands. The PWM current ripple characteristics are a function of the PWM method, operating modulation index (M_i), load current magnitude and load power factor (PF) [3],[6],[7]. In general, as f_{ic}>>f_{re}, the PWM harmonics are considered high frequency (HF, over kHz) harmonics. Fig. 5 illustrates the harmonic spectrum of the high frequency dc bus current ripple components for a 29 kW induction motor drive with f_{ic}=10 kHz space vector PWM (SVPWM) [6], M_i=0.78 and motor PF=0.86 (φ=30º).

TABLE I. DC BUS CURRENT RIPPLE FREQUENCY CHARACTERISTICS FOR VARIOUS POWER CONVERTER TOPOLOGIES

Topology		DC Bus Ripple Current	
Source Side	**Load Side**	**Source Side**	**Load Side**
Diode/Thyristor rectifier	PWM-VSI	Low frequency	High frequency
PV/battery			
PV/battery + Boost converter	PWM-VSI	High frequency	High frequency
PWM transistor rectifier			

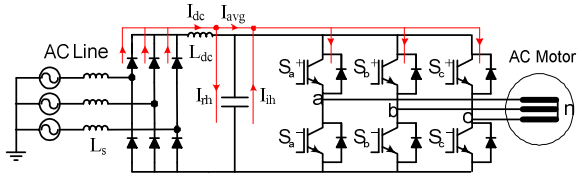

Figure 2. Diode/thyristor rectifier cascaded with PWM inverter

The dc bus capacitor C_{dc} receives harmonic current from both the rectifier (I_{rh}, LF) and inverter (I_{ih}, HF) sides. Therefore, the dc bus capacitor current ripple rms value is calculated as in (1).

$$I_c = \sqrt{I_{rh}^2 + I_{ih}^2} \qquad (1)$$

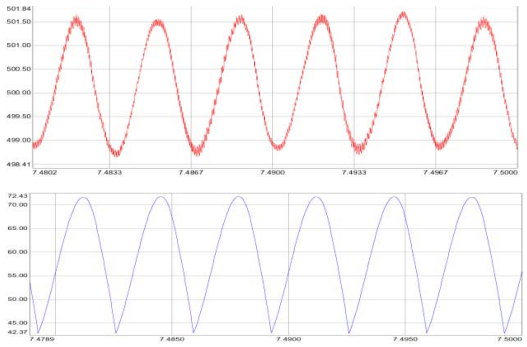

Figure 3. DC bus voltage (upper 0.5 V/div, 3.3 ms/div) and rectifier current (lower 5 A/div, 5 ms/div) waveforms

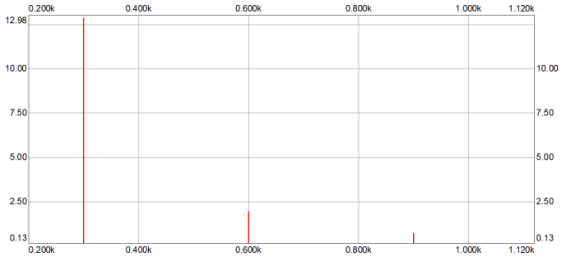

Figure 4. Rectifier side (low frequency) dc bus current harmonic spectrum (2.5 A/div, 200 Hz/div)

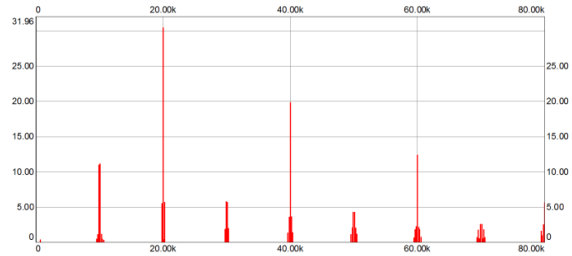

Figure 5. Inverter side (high frequency) dc bus current harmonic spectrum (5 A/div, 20 kHz/div)

In regenerative (involving bidirectional power flow) and/or high input power quality motor drive applications and UPS applications, shown in Fig. 6, the cascaded inverter-rectifier topology (also called back-to-back inverters) is commonly used. Both sides operate at high PWM frequencies, thus both sides inject high frequency current ripple to C_{dc}. If the PWM carrier frequency of each side is different, I_c contains all the frequency components of each side. If f_{rc}/f_{ic} (or the inverse) ratio is a large integer (indicating that the harmonic spectrum of I_c is wide), then the rms value of I_c can be correctly represented as in (1). Otherwise, it is less than the value calculated in (1), which represents the worst case ripple.

In the example of Fig. 7, the rectifier and the inverter have carriers of f_{rc}=10 kHz and f_{ic}=15 kHz, respectively. Near state PWM (NSPWM) [7] is employed for both sides. The grid is at f_{re}=50 Hz with V_s=220 V rms/phase. The load has 46.7 kW, f_{ie}=50 Hz, 70 A rms/phase ratings. The dc bus is V_{dc}=800V, and the operating conditions for both sides are M_i=0.6, φ=0°. As predicted, the I_c harmonic spectrum covers a wide range including components from both sides, with the carrier frequency components being dominant. There are no low frequency harmonics, major benefit of PWM operation on both sides.

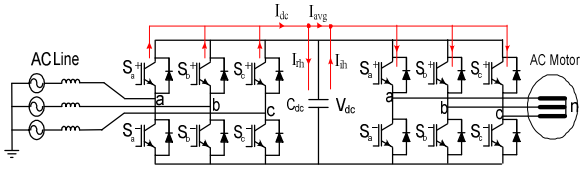

Figure 6. The back-to-back inverter and its dc bus current harmonics

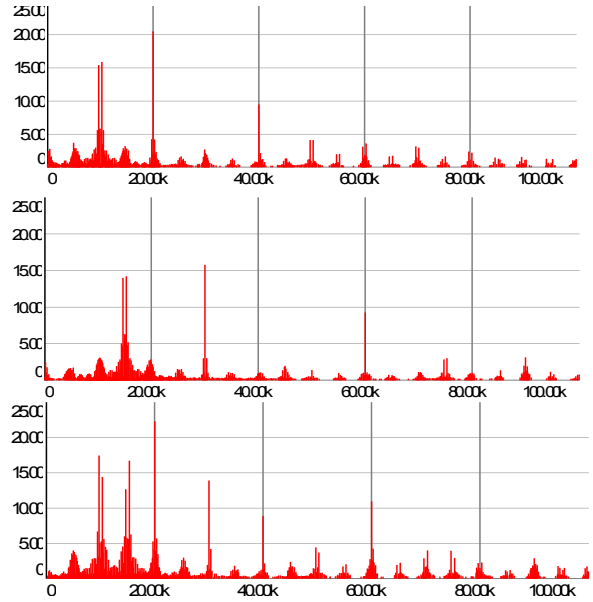

Figure 7. Harmonic spectrum of I_{rh} , I_{ih} and I_c from top to bottom, respectively. Operating conditions: on both sides NSPWM, M_i=0.6, φ=0° (PF=1), and f_{rc}=10 kHz, f_{ic}=15 kHz, (12.5 A/div, 20 kHz/div)

If the carrier frequency is the same on both sides (typical, $f_{rc}=f_{ic}$), the phase difference (φ_{ri}) between the two carriers becomes important. If the rectifier and inverter have the same carrier (φ_{ri}=0º), the ripple current pulses are centered with respect to the PWM cycle and the current polarities are opposite and there is at least partial cancellation (depending on M_i, PF, f_{re}, f_{ie}, and PWM method). If the carriers are of opposite polarity (φ_{ri}=180º), the pulses are centered but the currents are of the same polarity and they add. Thus, the dc bus ripple current becomes the largest. These two extreme cases are illustrated in Fig. 8, with all the parameters being the same as in the previous case, except that the carriers are at the same frequency (10 kHz) but in phase and 180º out of phase. In the figure, for the first few harmonics (dominant components) the cancellations or superpositions are clearly visible. In these simulations, both sides are operated at the same condition (M_i, PF, PWM method, etc. are all the same), thus the superposition and cancellation are nearly exact. Therefore, in such applications, it is important to synchronize the rectifier and inverter carrier and have φ_{ri}=0º to reduce the current ripple stress on the capacitor. In practice, the amount of cancellation depends on the operating conditions. For example, one converter can be completely disabled while the other is fully functioning (as in the UPS case with the grid off and the battery as the main energy source). In this case the design cannot rely on cancellation. In general, in a realistic design, (1) should involve selecting the worst case rms current of either side when operating alone.

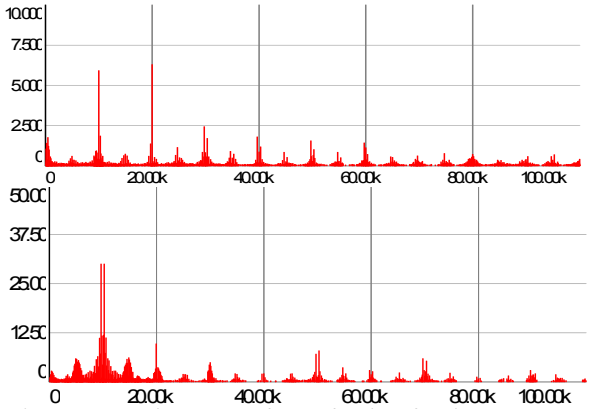

Figure 8. Harmonic spectrum of I_c as a function of carriers; top φ_{ri}=0º, (2.5 A/div), bottom φ_{ri}=180º (12.5 A/div). Operating conditions: on both sides NSPWM, M_i=0.6, φ=0°, $f_{rc}=f_{ic}$=10 kHz (20 kHz/div)

The topologies of Fig. 2 and Fig. 6 establish the basic two structures of Table I. The remaining application cases can be easily evaluated from the two basic studies conducted here. For example, battery to grid interface involves only one side inverter and one side dc, corresponding to the inverter part of the previously studied two cases. If a dc-dc converter is used between the battery and the dc bus of the inverter, then this case could be considered as a special case of back-to-back inverter as only one side is in inverter operating mode and the other side is in inverter operating as dc-dc converter (still injecting PWM current ripple, with more confined PWM spectra and meeting the properties discussed). Thus, the above studied cases are sufficient for establishing background before proceeding to advanced design issues.

III. Capacitors For Power Electronics

Generally electrolytic and film capacitors are used in the dc bus of an inverter. Aluminum electrolytic capacitors have high capacitance to volume ratio. This fact makes them ideal to decrease the dc bus voltage ripple (create a stiff dc bus voltage) and introduce high energy storage. Nevertheless, they have considerably high equivalent series resistance (ESR) and as a result, low ripple current rating, 20 mA/µF [8]. The ESR value of an electrolytic capacitor depends on the amplitude and frequency of the applied voltage, and the operating temperature (Fig. 9) [9]. The ESR increases with voltage, which limits the operating voltage (typically less than 500 V) [9]. Film capacitors, on the other hand, have very low ESR values and their rms current rating is higher, 1A/µF [8]. Fig. 10 illustrates the variation of the ESR of a film capacitor with frequency and temperature [10]. Film capacitors can operate under higher voltage levels. These facts make them very long-life devices compared to electrolytic type and they suit well in circuits with high ripple currents and voltages at the dc bus. However, their energy storage is significantly lower than the electrolytic ones. Both types have non-ideal electrical characteristics causing power dissipation. For electrolytics, ESR is the main cause of power loss [11]. The film capacitors' total power loss consists of ESR loss together with dielectric loss (caused by voltage ripple, increases with the frequency) [12]. Thus, for each capacitor type, different loss mechanisms must be considered in the design stage.

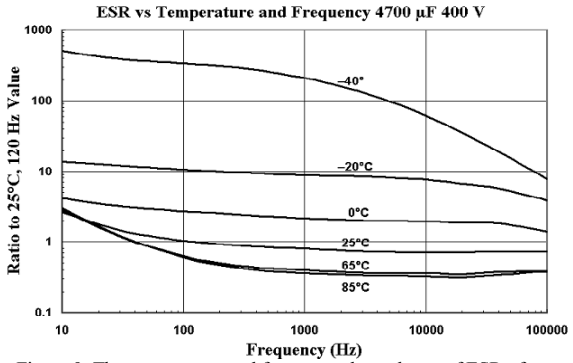

Figure 9. The temperature and frequency dependency of ESR of an aluminum electrolytic capacitor (with ESR:23 mΩ @ 120 Hz, 25ºC) [9]

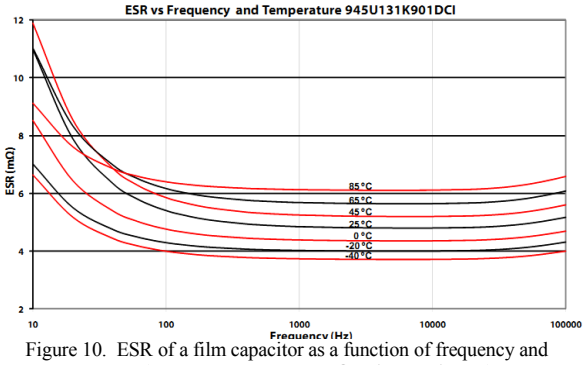

Figure 10. ESR of a film capacitor as a function of frequency and temperature (130µF, 900V, 41Arms @ 10kHz and 50ºC) [10]

The selection of the dc bus capacitor type depends on application requirements and circuit parameters. If the dc bus voltage ripple should be minimized, electrolytic capacitors are preferred due to high capacitance/volume ratio. Their voltage rating is generally low (500 V or less), such that high voltages are only obtained by establishing series banks which imply increased ESR. On the other hand, if high current ripple rating is required, film capacitors are chosen due to their low ESR (voltage rating is not an issue). This brings the cooling problem of the film capacitor into consideration. Generally electrolytic capacitors are low in cost compared to film capacitors. Film capacitors offer much longer life compared to electrolytic ones, so in many applications such as motor drives and PV systems, the designers try to use film capacitors in order to increase the life and reduce the size. In particular, in recent years the use of film capacitors in the electric vehicles (due to thermal reliability, small size, and long life), renewable energy (due to long life requirements on the power converters as the return on investment on such systems may be as long as 10-20 years), in fan/pump drives (cost and size reduction along with input power quality and long life enhancement requirements) has been increasingly dominating. As a result, both types find usage in industry for various reasons and design algorithms for both capacitor types become necessary.

In terms of matching between the power converter topologies (Table I) and capacitor type, the current ripple characteristics are the major determining factor. If the input side imposes low frequency current ripple (as in the diode/thyristor rectifier front-end) the voltage ripple may become large. As a result high dc bus capacitance is required and electrolytic type is suitable. In case of high frequency ripple current caused by the input and output (all other types), since the current ripple frequency is high, a large capacitance is not required for voltage ripple reduction ($Z_{dc\text{-}bus}=1/\omega C$). However, the large ripple current must be bypassed by the capacitor (without significant thermal stresses). This makes film capacitor ideal candidate for such applications. These requirements dictate the type selection and sizing of dc bus capacitors.

IV. Capacitor Loss and Size Calculation

Given a power conversion system circuit topology and having selected the capacitor type (and maybe the size also), it is important to estimate the capacitor losses for the purpose of design iteration and if the design is finalized, then the thermal performance. Both electrolytic and film capacitors have non-ideal mechanisms which cause losses and thus heating (temperature rise), which could be calculated based on datasheets or test parameters.

The conventional capacitor loss calculation approach uses the worst case (largest) total rms ripple current defined in (1) and the worst case (largest) ESR_{max} to find the total ESR power loss of a capacitor employing (2). Since the losses in this approach are overestimated, the approach yields an oversized capacitor. The more accurate approach should employ the detailed current harmonic spectrum information and take the frequency dependent ESR as in (3) into account, where $I_{\omega1}, I_{\omega2}, \ldots$ are the rms values of the dominant frequency ripple current components [3] and $ESR_{\omega1}$, $ESR_{\omega2}$, etc. are the corresponding frequency dependent ESR values obtained from the datasheet.

$$P_{loss-max} = I^2_{c-rms}.ESR_{max} \quad (2)$$

$$P_{loss} = (I^2_{\omega1}.ESR_{\omega1}) + (I^2_{\omega2}.ESR_{\omega2}) + \cdots \quad (3)$$

The ESR losses of an electrolytic capacitor and the ESR related loss part of a film capacitor can be calculated from (3). However, for the film capacitor the dielectric losses, which constitute a portion of the losses due to voltage ripple must be taken into account as in (4) separately for the high frequency harmonics (additional term effective high frequency, typically above several 10 kHz) [13]. However, in (4) the peak-to-peak voltage ripple V_{ripple} is required and it can be approximated by most dominant (mD) frequency voltage ripple. For this purpose, the capacitor current spectrum is required. In [3], the spectral content and the dominant frequency components (I_{mD}) are provided in detail as normalized quantities in a 3-D graphic, thus their use in (5) is straightforward. Then, for a given C_{dc} and peak to peak current ripple I_{mD}, the resulting V_{ripple} is calculated in (5).

$$P_{loss} = I^2_{rms\_f} \cdot R_{ESR\_f} + \frac{1}{2} \cdot C_{dc} \cdot V^2_{ripple} \cdot f_{mD}.tan\delta \quad (4)$$

$$V_{ripple} = \frac{1}{2\pi \cdot f_{md} \cdot C_{dc}} \cdot I_{mD} \quad (5)$$

The capacitor sizing process requires the topology information first. If diode/tyhristor rectifier front-end is involved, dominant low frequency ripple (at $6f_{re}$), if other topologies are involved, most dominant frequency ripple

must be considered. In the case of diode/thyristor rectifier, the capacitor size is approximated from the voltage ripple requirement as in (6), by assuming high performance rectifier (with 4% L_{dc} and 4% L_s) whose dc link current pulses are charging the capacitor with V_{ripple} at $6f_{re}$ frequency. In (6), P_{load} is the rated load power and $V_{s\text{-}rms}$ is the grid voltage rms value. In the case of film capacitor applications involving only high frequency ripple, as the current ripple is the input to the design, for a given voltage ripple criteria, the capacitor size can be obtained from (5) by rearranging the formula. Thus, the basic formulas for loss analysis, capacitor sizing, and V_{ripple} determination are simple and available for a detailed dc bus design algorithm of a power electronics system.

$$C_{dc} = P_{load}/[240 * V_{ripple} * V_{s-rms} * f_{re}] \qquad (6)$$

V. Capacitor Sizing Design Algorithm

The design algorithm involves the basic system design and narrows down to C_{dc} sizing. First the application type defines the power converter topology. Then based on the application type, proper PWM methods are selected [3], [13]. With these inputs, the design can progress as the current ripple spectrum and its dominant components become available (dominant harmonic current and its frequency for each side inverter are obtained by using the normalized quick 3-D look up graphics in [3]). In case of diode rectifier, the rectifier harmonics injected to the dc bus are estimated by assuming a dominant sixth harmonic, as will be discussed via the design example. Having the current ripple properties determined, the capacitor type is selected. Beyond this stage, the capacitor sizing algorithm progresses to an iterative stage. The current ripple injected from the input and output sides causes voltage ripple on and losses (thermal stresses) in the dc bus capacitor. Thus, a selected capacitor must satisfy the voltage ripple requirement of an application while its ripple current limit (thermal capacity) is not exceeded. Using the defined stress criteria (voltage ripple and temperature rise), the iterative optimization process continues until the design is completed and the algorithm outputs the final C_{dc} value. The algorithm is illustrated by a flowchart in Fig.11.

The iterative calculation procedures start after the current ripple information is input to the algorithm. First, the voltage ripple criteria is checked and if criteria is not met, the capacitance is increased iteratively selecting from the initially selected member of the product family or higher current rated family until the voltage ripple criteria is met. If the available capacitors cannot meet the criteria, then paralleling is applied. At the next step, power loss calculation is done with the parameters of the selected capacitor. Capacitor core temperature is calculated, and if the core temperature is below the threshold defined in the spec sheet, design is completed. Otherwise, the capacitor current rating is increased iteratively by selecting from the previously selected family or higher current rated family (or another capacitor is paralleled) until core temperature criteria is met and thermal reliability secured. As a result, the three criteria, first the current ripple, then the voltage ripple, and finally the thermal stress criteria are met in the finalized design. Further details on the algorithm are provided in [13]. If the initial design is conservative (oversized), the iteration can be applied as capacitor size reduction (not shown in the algorithm, for the sake of simplicity and brevity). Likewise, other criteria such as cost and size can be imposed in the algorithm as a part of product optimization. Next, design examples for various applications are considered.

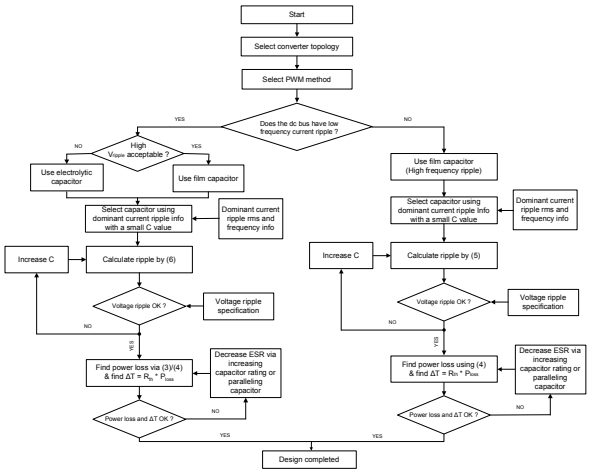

Figure 11. Flowchart for the capacitor selection and sizing algorithm

VI. Design Examples

In this section, the developed algorithm is utilized in C_{dc} design for various applications. A a transformerless UPS system, a regenerative motor drive with active front end, and an ac motor drive with diode rectifier front end with standard electrolytic and small film capacitors are considered. Other application examples, such as grid connected PV systems have similar attributes to the studied examples, therefore, the design stages discussed for the given applications can be easily extended to applications not included in the paper. The calculations in all examples are supported by simulations. Current and voltage ripple values, the harmonic spectra predicted, etc. are all matched with the simulation values.

Before proceeding with the design examples, it is beneficial to review the basic operating characteristics of typical loads interfaced with a PWM-VSI. As Fig. 12 shows, there are three basic operating conditions that an inverter might operate under. These operating conditions define the load PF and M_i level, thus along with the PWM method employed, they yield the information of current ripple injected to the dc bus by the inverter. If this information is considered apriori and the PWM method is selected such that the dc bus ripple current is less, the design yields better dc bus performance. Therefore, this approach will be favored in the design.

Assuming 70 A rms (100 A peak) sinusoidal load current, for the given operating points of Fig. 12, the dc bus current ripple rms value and its dominant harmonics for various PWM methods are summarized in Table II. The table illustrates the PWM method dependency of the rms current ripple and the dominant harmonics. It is apparent different operating conditions favor different PWM methods. Assuming the load current (100 A peak) as one per-unit, the results can be interpreted as percent values, such that they can be used as general results. The table establishes a guide for the PWM method selection for each application. While the table provides basic

information, wider range of operating conditions are evaluated in the 3-D graphic of ripple characteristics as a function of M_i and PF in [3] and these provide more rigorous results. Table II and the 3-D graphic in [3] will be utilized throughout the following design examples.

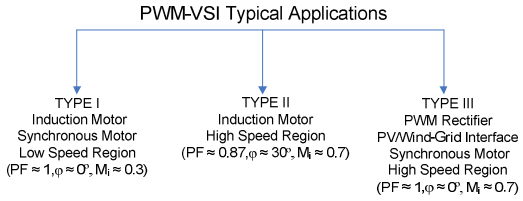

Figure 12. PWM-VSI applications and typical operating points

TABLE II. INVERTER DC BUS CURRENT RMS VALUE AND DOMINANT HARMONICS FOR VARIOUS PWM METHODS

PWM Method	M_i=0.3 φ=0° Irms=70 A		M_i=0.7 φ=30° Irms=70 A		M_i=0.7 φ=0° Irms=70 A	
	I_h(rms)	mD	I_h(rms)	mD	I_h(rms)	mD
SPWM	39.9	2	36.2	2	37.7	2
SVPWM	39.9	2	37.4	2	39	2
AZSPWM1	44.2	2	46.3	1/2	41.4	2
DPWM1	40.1	1	37.4	1	39.2	1
NSPWM	NA	NA	40.3	1	25.5	2

A. Transformerless UPS System

A UPS with 46.2 kVA (@ PF=1, 220 V/phase-rms, 50 Hz output ratings is considered. Back-to-back PWM-VSIs are employed. Since the UPS is transformerless and the load requires a neutral wire, the input and output neutral wires are common (through the dc bus midpoint connection), forming a 4-wire system. Thus, in addition to providing a stable neutral point, a return path is established for the unbalanced load currents. However, due to the midpoint connection, zero sequence signal injection is not allowed to the sinusoidal PWM signal, thus, the only applicable PWM strategy is SPWM for both the input and output sides. The rectifier operates across the low voltage grid and faces the rated voltage (high M_i) and PF=1 is preferred due to high power quality and low losses. According to Fig. 12, the application is Type II and based on Table II, $2f_c$ current harmonics are dominant (mD=2) at the dc bus. The load PF range is typically 0.8-1.0. Since the output is also operated at rated voltage, M_i is high, and for both the input and output M_i is 0.61. Based on Fig. 12, the load is Type II and III. According to Table II, the PF=0.8 condition results in less ripple current. Therefore, PF=1 at full load is the worst case design point for the inverter. As in the rectifier case, at the output also the dominant harmonic is at $2f_c$.The dc bus currents are tabulated in Table III for mentioned operating points. Since both rectifier and inverter side high frequency currents contribute to dc bus current harmonics and assuming that the carriers of input side and the output side are not synchronized, (1) is used to combine their effects as rms. Therefore, the overall dc bus high frequency current harmonics rms value is calculated as 59.4 A.

The dc bus voltage is selected as 800 V (±400 V). A film capacitor with the following specs is chosen; 220 µF, 600 V, 100 A rms, ESR=1 mΩ, R_{th}=8.4 °C/W (FFVE6K0227K) [12]. Two capacitors are connected in series (midpoint gives the neutral terminal), yielding 110 µF equivalent dc bus capacitor. The voltage ripple is calculated from (5), as V_{ripple}=3.6 $V_{peak\text{-}to\text{-}peak}$. This is lower than 1% and acceptable. The power loss is found from (4) as 3.52 W and assuming ambient temperature of T_A=50 °C, this causes a temperature rise of ΔT=29.5 °C. Since T_C=T_A+ΔT=79.5 °C << 120 °C, the design is completed.

Note that if the UPS load current is unbalanced (such as single phase loading) or includes low frequency harmonics (such as diode rectifier loading) and this current is not matched directly from the rectifier, the imbalance current may cause low frequency ripple on the dc bus capacitor. Similarly, with grid failure, under battery operating mode, if there is unbalanced load, the same condition occurs. In such cases, either an additional circuit has to supply these injected currents or a large capacitor has to be sized to suppress the voltage ripple and absorb the load harmonic current (implying the requirement for electrolytic capacitor).

TABLE III. TRANSFORMERLESS UPS SYSTEM DATA

Input (SPWM, f_{rc}=10 kHz)				Output (SPWM, f_{ic}=10 kHz)			
M_i	PF	I_{rh}(rms)	ImD_{rms}	M_i	PF	I_{ih}(rms)	ImD_{rms}
0.61	1	42	35.3 A	0.61	1	42 A	35.3 A

B. Regenerative Motor Drive with Active Front End

Regenerative motor drives are widely utilized in elevators, servo systems, etc. In such systems, the preferred topology is the back-to-back PWM-VSI. Unlike in the UPS systems, the neutral wire is not required and it is isolated. Thus, advanced PWM methods can be used on both sides to increase the dc bus voltage utilization and enhance the ripple and loss performance. The grid side VSI always operates at the same f_{ie}, M_i (high M_i), and PF (unity for low stress) conditions as in the UPS, while the motor side VSI operates at varying conditions, as a function of speed and load variation. If the motor is a PM-AC (servo) type (quite frequently), the machines is efficient and due to the magnet excitation, the load PF is also unity, in a wide operating range. Thus, the inverter has varying f_{ie}, M_i, and load current.

Let's consider a 46.2 kW servo motor drive operating against the standard low voltage grid. The input side has the same specs as in the UPS example; M_i=0.61, PF=1. Apparent from Table II (more accurately from the 3-D graph in [3]), NSPWM is the best PWM method for the rectifier side as it provides the lowest ripple. The motor rated current is 70 A rms (100 A peak). Since the motor must provide rated torque in the full range, at low M_i (Type I in Fig. 12) and high M_i (Type III in Fig. 12), the rated current capacity may be fully utilized throughout the M_i range. Let's consider two cases, M_i=0.61 at full power, and M_i=0.3 at half power. Both cases have PF=1 and rated current of 70 A rms. As Table II indicates, the M_i=0.3 condition results in more dc bus ripple current, thus it is the high thermal stress point for the dc bus capacitor. Therefore, this point is considered for design. For the inverter side, for M_i=0.3, according to Table II, SVPWM is the best approach. Not only it has low dc bus current ripple, but it also provides the lowest motor current PWM ripple, suitable for servo applications at low speed for low inertia loads. The ripple current, its dominant components

for both sides are listed in Table IV based on the 3-D graphics of [3] (also verified via simulations). In the table the operating parameters are also summarized.

TABLE IV. REGENERATIVE MOTOR DRIVE WITH ACTIVE FRONT END OPERATING PARAMETERS

Input (NSPWM, f_{ic}=15 kHz) mD = 2 (30 kHz)				Output (SVPWM, f_{rc}=10 kHz) mD = 2 (20 kHz)			
M_i	PF	I_{rh}(rms)	ImD_{rms}	M_i	PF	I_{ih}(rms)	ImD_{rms}
0.61	1	14 A	8.9 A	0.3	1	39.9 A	34.4 A

Since both rectifier and inverter side high frequency currents contribute to dc bus current harmonics and carrier frequencies are different (f_{ic}=10 kHz, f_{rc}=15 kHz), (1) is used to obtain the rms value of I_c as 42.3 A. Since the inverter side dominant current harmonic (34.4 A at 20kHz) is significantly higher than the rectifier side dominant harmonic (8.9 A at 30 kHz), the voltage ripple is determined by the inverter side. The dc bus voltage is selected as 800 V. A film capacitor with the following specs is chosen; 140 μF, 1000 V, 51 A rms, ESR = 2.5 mΩ, R_{th}=9.2 °C/W (FFVE6L00147K) [12]. The voltage ripple is calculated from (5), as V_{ripple}=2 $V_{p\text{-}p}$. This is lower than 1% and acceptable. The power loss is found from (4) as 4.5 W and assuming T_A=50 °C, this causes a temperature rise of ΔT=41.4 °C. Since T_C=T_A+ΔT=91.4 °C << 120 °C, the design is completed.

C. *PWM-VSI Fed Induction Motor Drive with Diode Rectifier Front End*

An induction motor drive with 29kW ratings is considered (Fig. 2). The rectifier for this drive is the same as was considered in section II, involving 50 Hz, 220 V rms/phase. After the selection of topology, to choose the PWM method, the characteristics of the load is considered. The induction motor drive design involves operating in a wide speed range covering both low and high M_i. Since this corresponds to Types I and II in Fig. 12, these operating conditions are represented in the first two columns of Table II. Based on the ripple characteristic observation of PWM methods in the table, for this application the choice of SVPWM is appropriate. At the next step, the capacitor type is chosen. As the rectifier injects low frequency harmonics to the capacitor, and dc bus voltage is less then 1000 V (about 500 V as shown in Fig. 3), electrolytic capacitor is suitable according to the flowchart. Then, as an initial estimation for C_{dc}, in order to provide 0.4% voltage ripple, using (6), C_{dc} is calculated as 5 mF (consistent with the simulations, see Fig. 3). Next, the power dissipation in the selected capacitor has to be calculated. This requires the knowledge of ripple current values imposed by diode rectifier and inverter. To calculate the PWM current ripple caused by the inverter, the 3-D graphic in [3] is used for the corresponding motor operating point. The diode rectifier harmonic current is dominantly the sixth harmonic, which is numerically estimated as $P_{load}/(10V_{s\text{-}rms})$. The sixth harmonic estimation also holds the base for the derivation of (6). Then the total rms ripple current is found by using (1). Table V includes current ripple information along with the motor drive operating point data.

TABLE V. 3-Φ DIODE RECTIFIER-PWM-VSI SYSTEM DATA

Input (diode rectifier)	Output (SVPWM, f_{ic}=10 kHz)	
I_{rhD}=9.2 A rms @ f_D=300 Hz	M_i	PF
	0.78	0.86
	mD = 2 (20kHz)	
	I_{ih} (rms)	I_{mD} (rms)
	32.3 A	20.2 A

Having obtained the current ripple information, the next step involves the C_{dc} sizing. Since V_{dc} is approximately 500 V, two aluminum electrolytic capacitors must be connected in series to form a capacitor bank. Each capacitor is rated as 300 V and this gives an overall rating of 600 V. In the circuit, 9.2 A rms low frequency current (dominant at 300 Hz) comes from the rectifier side and 32.3 A rms high frequency current comes from inverter side. Thus, the capacitor bank should be rated as $\sqrt{9.2^2 + 32.3^2} \approx 33.6$ A rms (each capacitor must carry 33.6 A rms at 20 kHz, because dominant current harmonic is at 20 kHz. Obtained from the catalog of a manufacturer (520C542T300CF2B, [15]), four capacitors with 5.4mF, 17A at 85ºC and 120Hz ratings (22.9 A at 20 kHz) and 20.7 mΩ ESR at 25ºC and 120 Hz are used to form a bank. Thus, the current capacity becomes 45.8A rms. At 85ºC, at 20 kHz and 300 Hz the ESR values are calculated as 8mΩ and 10mΩ. Thus, the power dissipation is calculated as: $P_{diss}=4.6^2 \cdot 0.01 + 16.15^2 \cdot 0.008 \approx 2.3$ W/capacitor. This causes ΔT=8.8 °C for a R_{th} of 3.8 ºC/W. With T_A=50 °C, the core temperature is found as T_C=T_A+ΔT=58.8 °C << 85 °C, thus, the design is completed.

D. *PWM-VSI Fed Induction Motor Drive with Diode Rectifier Front End with Small Film Capacitor*

Motor drives with diode rectifier front end employing small C_{dc} (using film capacitors) are becoming popular due to long life, compactness (as in integrated drives), and improved line current quality. Especially, variable torque type (fan, pump, etc.) loads benefit from the technology, as they allow stable operation of the dc bus with simple control algorithms [14]. In such systems, the design involves small or no inductor filters at the ac (L_s) and dc (L_{dc}) sides of the rectifier, for cost and size benefits, and the grid (distribution transformer leakage) inductance is involved in the filtering process. The rectifier dominant harmonics are at $6f_{re}$ and $12f_{re}$ (300/600 Hz for 50 Hz grid) and the small LC filter implies high resonance frequency, f_n, defined in (7). Unlike the conventional large electrolytic capacitor design (which is designed with f_n<<300 Hz), the small C_{dc} design involves a risk of resonant amplification. For this purpose, the small C_{dc} design requires selecting $12f_{re}$<<f_n<<f_{ic} criteria [14]. Therefore, small C_{dc} and small inductive filters meeting the high resonant frequency criteria indicates that large voltage ripple must be allowed in this design. Therefore, in this design, the current ripple criteria is the main criteria and the voltage ripple criteria is typically not considered.

$$f_n = \frac{1}{2\pi\sqrt{(2L_S+L_{dc})*C_{dc}}} \quad (7)$$

In the design example, a 30 kW motor drive (fan/pump application) with a small C_{dc} is considered. Assuming

f_{ic}=10 kHz, grid inductance L_s=15 µH, and inserting a dc link inductance of L_{dc}=112 µH, the design goal of placing f_n at 1.75 kHz (sufficiently distant to 600 Hz and 10 kHz) yields a small capacitor with C_{dc}=58 µF, by (7). The feasibility of this design is illustrated via the simulation waveforms of Fig. 13, Fig. 14, and Fig. 15. Due to small C_{dc}, the bus voltage and bus current have oscillations and the harmonic at 1200 Hz (7 A rms) is more dominant than 300 Hz component. The high frequency PWM current harmonics include the dominant $2f_{ic}$ and its multiples. Table VI includes system operating point data (VSI current ripple found via the 3-D graph in [3]). Next a 58 µF, 600 V film capacitor with 44 A rms, ESR=1 mΩ (not varying with frequency or temperature noticably), and R_{th}=6.4 °C/W (FFG86K0586K) is selected from a manufacturer website [12]. The power loss is found from (3) as 0.7 W and the temperature rise is 4.5 °C. Assuming ambient temperature of 50°C, the core temperature becomes, $T_C=T_A+\Delta T$=54.5 °C, lower than 105 °C, so the design is completed. Iterations in this and all other previous examples could be further conducted for reduced cost or size by considering lower rating capacitors (not attempted here for limited space and the sake of brevity).

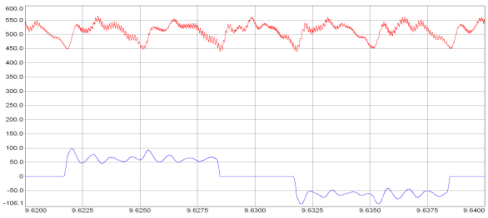

Figure 13. DC bus voltage (50 V/div, 2.5 ms/div) and line current waveform (50 A/div, 2.5 ms/div) of a small C_{dc} motor drive

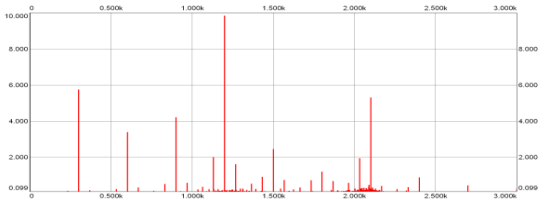

Figure 14. Low frequency (rectifier side) dc bus current spectrum of a small C_{dc} motor drive (2.5 A/div, 333 Hz/div)

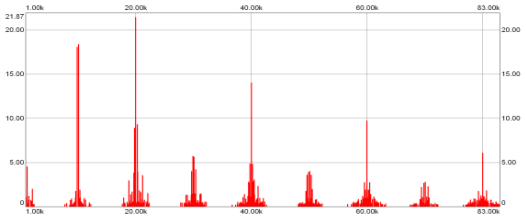

Figure 15. High frequency (inverter side) dc bus current spectrum of a small C_{dc} motor drive (5 A/div, 20 kHz/div)

TABLE VI. MOTOR DRIVE WITH SMALL C_{DC} SYSTEM DATA

Input (diode rectifier)	**Output (SVPWM, f_{ic}=10 kHz)**	
	M_i	**PF**
	0.79	0.75
I_{rhD}=7 A rms @ f_D=1200 Hz	**mD = 2 (20kHz)**	
	I_{ih} (rms)	**I_{mD} (rms)**
	28 A	18 A

VII. CONCLUSION

Dc bus capacitor design method for various power converter topologies involving two-level, three-phase inverters has been proposed. The design starts from selecting the power electronic converter topologies, progresses to the choice of efficient PWM methods, and finally iterates on the capacitor size. The method relies on the knowledge of the current ripple injected to the dc bus capacitor. The current ripple dominant components are estimated from a simple normalized 3-D graphic or calculated for all the discussed topologies involved in inverter applications (including diode rectifiers). Given the dominant current ripple, the voltage ripple is also calculated. The ripple components are compared with the set value to iterate the design algorithm, which also involves thermal reliability criteria. As a result, a capacitor meeting the voltage and current ripple requirements that also provides low thermal stress is selected. The method is illustrated via application examples, such as diode rectifier front end motor drives (with small and large C_{dc}), regenerative motor drives, and UPS systems. The paper also reviews the two capacitor technologies suitable for inverter applications. Overall, the paper helps the power electronics development and design engineer in the design and performance evaluation procedure of dc bus capacitors for three-phase inverters. The method is simple but rigorous and accurate.

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