Analysis of the Sideband Effect on the Stability of the Voltage-Mode-Controlled Boost Converter

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***Abstract*-- Although the small-signal model of the loop gain, which quantitatively include the sideband effect, have been proposed in the resent research, all results are for buck converters. When applying these results for the Voltage-Mode-Controlled(VMC) boost converter, the instability phenomenon, in some cases the converter with the leading-edge modulation is stable while with the trailing-edge modulation it becomes unstable, still couldn't be explained as the case that using average model. In order to indicate why these results aren't suitable for boost converter, it is firstly pointed out that the high-frequency characteristic of the duty ratio-to-output transfer function $G_{vd}(s)$, which the average model fails to describe, could affect the low-frequency performance of the loop gain and the modulator. Then, we give the theoretical prediction of $G_{vd}(s)$ by using the describe function method, which has excellent agreement with the measured results especially in the high-frequency region. By using the corresponding obtained loop gain, the aforementioned phenomenon would be explained. The work demonstrates significant importance of the research into the sideband effect on the stability for the DC/DC converter and the DC system.**

***Index Terms*--Boost converter, describe function method, high-frequency characteristic, sideband effect.**

I. Introduction

This work was initially motivated by a study of the sideband effect on the stability for the DC/DC converter and DC system, which is previously researched qualitatively in [1]. As the DC/DC converters become more widely used and corresponding application form become more various, more complex instability phenomenon caused by the sideband components have attracted researcher's attention. Hence, the related research begin to deepen, changing from qualitative research to quantitative research. For example, [2] proposed a multiple-frequency model by introducing the influence from one sideband component quantitatively for high-bandwidth Voltage-Mode-Controlled(VMC) buck converter, where the average model fails to describe the high-frequency performance of the loop gain, and the theoretical model has a good agreement with the measurement result; Also, the model proposed in [3], through the quantitative analysis of the sideband effect, succeed to predict the range of switching frequency of one buck converter, where the system become unstable for two cascade/parallel buck converters when the switching frequency of the other converter is constant.

The small signal models of the loop gain proposed in [2, 4-6] are all for buck converter, and can not explain the instability phenomenon that in some cases the boost converter with the leading-edge modulation is stable while with the trailing-edge modulation it becomes unstable as the case that using average model. Therefore, the question how to get the correct loop gain for the VMC Boost converter naturally arises. Look at the models in recent research carefully, we will find that the high-frequency characteristic of $G_{vd}(s)$, which the average model fails to describe, could affect the low-frequency performance of the loop gain and the modulator, and this has been neglected in [2, 4-6]. In addition, from the simulation results as will be shown in the section III, it will be found that the small-signal response of $G_{vd}(s)$ for trailing-edge or leading-edge modulated boost converter is not the same as each other in the high-frequency region, also both have badly agreement with the average model. So, it is reasonable to deduce that $G_{vd}(s)$ which is contained in the models proposed in [2, 4-6] should not be derived by using the average model. Our work is to revise these results by using the accurate prediction of $G_{vd}(s)$, which is obtained through the derivation which is similar to that proposed in [7].

This paper is organized as follows. Section II firstly summaries the models of the loop gain proposed in the existing literature and gives the expression of $G_{vd}(s)$. Simulation results for VMC Boost converter are provided in the section III to verify the proposed analysis. Finally, Section IV concludes this paper.

II. The Loop Gain Model For the VMC DC/DC Converter

By refining the derivation progress and the theoretical prediction proposed in [2, 4-6] for the loop gain of the PWM converter, the small-signal model of the PWM comparator can be derived and expressed as follows.

$$G_{PWM\_s}(s) = \frac{1}{V_m}\frac{1}{1+\sum_{\substack{k=-\infty \\ k\neq 0}}^{+\infty}\frac{1}{V_m}G_{vd}(s+k\omega_s j)\,\mathrm{H_v}\,G_c(s+k\omega_s j)} \quad (1)$$

where, V_m is the peak-to-peak value of the ramp, $G_{vd}(s)$ and $G_c(s)$ represents small-signal response of the duty ratio to output voltage and the controller, respectively. H_v is the sense gain of output voltage, ω_s is the angular switch

frequency. Correspondingly, we would obtain the loop gain for closed-form converter as

$$T_s(s)=\frac{1}{V_m}\frac{G_{vd}(s)\mathrm{H_v}\,G_c(s)}{1+\frac{1}{V_m}\sum_{\substack{k=-\infty\\k\neq 0}}^{+\infty}G_{vd}(s+k\omega_s j)\mathrm{H_v}\,G_c(s+k\omega_s j)} \tag{2}$$

Compared with the result represented in (2), the model proposed in [2, 4] only contains the influence of the sideband components around ω_s. In this paper, the model represented in (2) is called as sample-data model, because it is originally obtained in [6]. Also, 'sample-data model' imply that the result has a relationship with the sideband components, so it is more suitable for describing the characteristic of the model represented in (2) than 'describe function model' which is proposed in [8].

Look at (2) carefully, it can be found that the high-frequency characteristic of $G_{vd}(s)$ would affect the low-frequency response of the loop gain for PWM converter. Then, we derived $G_{vd}(s)$ by using the describe function method. The procedure is similar to that shown in [7], the difference is all the sideband components of the error signal are considered in this paper. In order to save pages, the detailed derivation will be introduced in the future paper and only the main idea of the derivation are included in this section.

First, let us select the time when the error signal v_c intersects the ramp waveform as the start point of each switching period T_s for the VMC DC/DC converter, and **x**, **u** and **y**(output voltage v) represent state vector, input vector and output vector, respectively. **x** and **y** contain two parts, respectively, and one is steady state vector **X** and **Y**, the other is perturbation vector $\hat{\mathbf{x}}$ and $\hat{\mathbf{y}}$. Also, let d denotes the duty ratio signal, and it also contains steady state part D and perturbation signal $\hat{d}$.

Second, assuming the error signal contains the components $\hat{v}_c(\omega_r+k\omega_s)$ of which the angular frequency are $\omega_r+k\omega_s$($k\in z$), where $n\omega_r=m\omega_s$($n, m\in z$), then according to the sampling principle the relationship between $\hat{d}(\omega_r+k\omega_s)$ and $\hat{v}_c(\omega_r+k\omega_s)$ would be built.

Third, we need to calculate the relationship between $\hat{\mathbf{x}}(\omega_r+k\omega_s)$, $\hat{\mathbf{y}}(\omega_r+k\omega_s)$ and $\hat{v}_c(\omega_r+k\omega_s)$. In every state, the equation (3) could be established. Then, from the solution of (3), the relationship between the value of $\hat{\mathbf{x}}(t)$, $\hat{\mathbf{y}}(t)$ in every switching period and the corresponding value $\hat{\mathbf{x}}(kT_s)$, $\hat{\mathbf{y}}(kT_s)$ would be arrived. Because of the periodic characteristics of $\hat{\mathbf{x}}$ and $\hat{\mathbf{y}}$, we could get the value $\hat{\mathbf{x}}(kT_s)$, $\hat{\mathbf{y}}(kT_s)$. Therefore, the relationship between the value of $\hat{\mathbf{x}}(t)$, $\hat{\mathbf{y}}(t)$ and $\hat{v}_c(\omega_r+k\omega_s)$ would be known. Next, using the describe function method, the relationship between $\hat{\mathbf{x}}(\omega_r+k\omega_s)$, $\hat{\mathbf{y}}(\omega_r+k\omega_s)$ and $\hat{v}_c(\omega_r+k\omega_s)$ would be established.

$$\begin{cases}\dot{\mathbf{x}}=\mathbf{A}_i\mathbf{x}+\mathbf{B}_i\mathbf{u}\\ \mathbf{y}=\mathbf{C}_i\mathbf{x}\end{cases}\quad(i=1,2) \tag{3}$$

Where, $\mathbf{A}_i$, $\mathbf{B}_i$ and $\mathbf{C}_i$(i=1,2) represent the system matrix. Therefore, $G_{vd}(s)$ could be obtained as

$$\mathbf{G}_{vd}(s)=(\mathbf{C}_1\boldsymbol{\alpha}_1(s)+\mathbf{C}_2\boldsymbol{\alpha}_2(s)\cdot e^{\mathbf{A}_1T_1}e^{-sT_1})\cdot(\mathbf{I}-e^{-sT_s}\boldsymbol{\Phi})^{-1}\Gamma_{xd}+\Gamma_{yd} \tag{4}$$

where,

$$\boldsymbol{\alpha}_i(s)=(\mathbf{A}_i-s\mathbf{I})^{-1}(e^{\mathbf{A}_iT_i}e^{-sT_i}-\mathbf{I})\ (i=1,2) \tag{4a}$$

$$\Gamma_{xd}=\left(\mathbf{A}_{on}-\mathbf{A}_{off}\right)\mathbf{X}(kT_s)+\left(\mathbf{B}_{on}-\mathbf{B}_{off}\right)\mathbf{u} \tag{4b}$$

$$\Gamma_{yd}=\left(\mathbf{C}_{on}-\mathbf{C}_{off}\right)\mathbf{X}(kT_s) \tag{4c}$$

where, $\mathbf{A}_{on}$, $\mathbf{B}_{on}$, $\mathbf{C}_{on}$ and $\mathbf{A}_{off}$, $\mathbf{B}_{off}$, $\mathbf{C}_{off}$ represent the system matrix which are the same as that defined in [9] when the switch transistor is in the on and off state, respectively, and $\mathbf{X}(k\mathrm{T_s})$ is the state vector value in the steady state. The relationship between $\mathbf{A}_{on}$, $\mathbf{B}_{on}$, $\mathbf{C}_{on}$, $\mathbf{A}_{off}$, $\mathbf{B}_{off}$, $\mathbf{C}_{off}$ and $\mathbf{A}_i$, $\mathbf{B}_i$ and $\mathbf{C}_i$(i=1,2) can be built easily for trailing-edge or leading-edge modulated DC/DC converter.

Next, let $G_{vd\_DF\_lag}(s)$ and $G_{vd\_DF\_lead}(s)$ represent the result when the trailing-edge modulation and the leading-edge modulation is used, respectively, and $G_{vd\_av}(s)$ represents the result derived by using the average model. Then we can get the corresponding the PWM model $G_{PWM\_s\_GvdDF\_trail}(s)$ and $G_{PWM\_s\_GvdDF\_lead}(s)$ and $G_{PWM\_s\_Gvdav}(s)$, and loop gain model $T_{s\_GvdDF\_trail}(s)$ and $T_{s\_GvdDF\_lead}(s)$ and $T_{s\_Gvdav}(s)$ by substituting $G_{vd\_DF\_lag}(s)$ and $G_{vd\_DF\_lead}(s)$ and $G_{vd\_av}(s)$ into (1) and (2), respectively, and let $T_{av}(s)$ represent the loop gain obtained by using the well-known average model. In next section, these theoretical prediction will be compared with the simulation results for the VMC Boost converter.

III. Simulation Results

To verify the validity of the analysis mentioned above, this section demonstrates the comparison between the theoretical prediction and measured results for the VMC boost converter with trailing-edge modulation and leading-edge modulation. The schematic diagram is shown in Fig.1 and the circuit parameters listed in Table I.

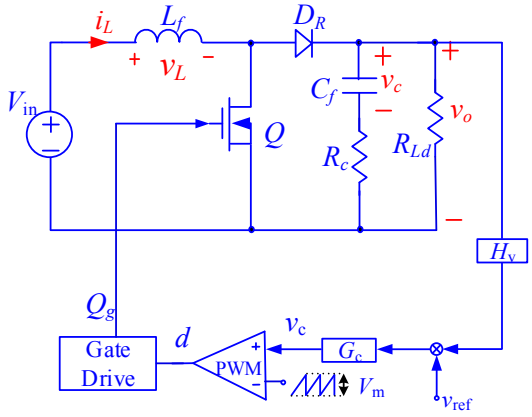


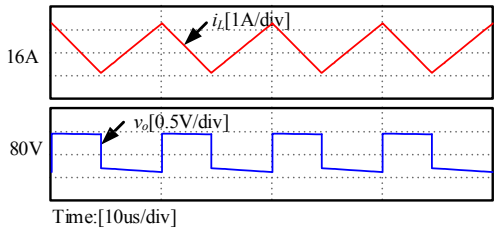
Fig. 1 The schematic diagram of the VMC Boost converter

TABLE I
CIRCUIT PARAMETERS OF THE VMC BOOST CONVERTER

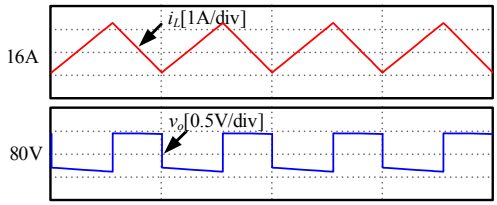
Circuit parameter	value	Circuit parameter	value
Input voltage V_{in} / V	36	inductor L_f /μH	95
Output voltage V_o / V	80	Capacitor C_f /μF	470
Output Power P_o / W	500	ESR/ mΩ	47
Switching frequency f_s / kHz	100	V_m /V	2.5
Voltage sense gain H_v	0.231	R_{Ld}/ (Ω)	12.8

Two compensators $G_{c1}(s)$ and $G_{c2}(s)$ were used, and corresponding expression are shown in (5). Fig.2 shows the waveforms of the inductor current and the output voltage when the two controllers are used with different modulation, respectively. When the controller $G_{c1}(s)$ is chosen, no matter which modulation is selected the converter will be stable. When the controller $G_{c2}(s)$ is used, it will be unstable when the trailing-edge modulation is selected.

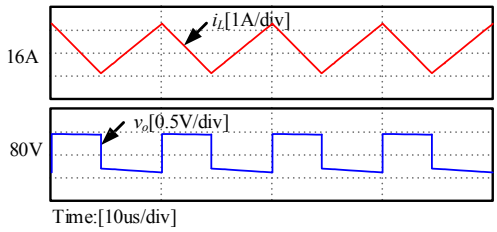
$$\begin{cases} G_{c1}(s) = \dfrac{4.77\times10^5(s+1.41\times10^3)(s+1.41\times10^3)}{s(s+8.91\times10^4)(s+2.22\times10^4)} \\ G_{c2}(s) = \dfrac{5.37\times10^6(s+2.83\times10^3)(s+1.89\times10^3)}{s(s+3.56\times10^4)(s+4.46\times10^4)} \end{cases} \quad (5)$$



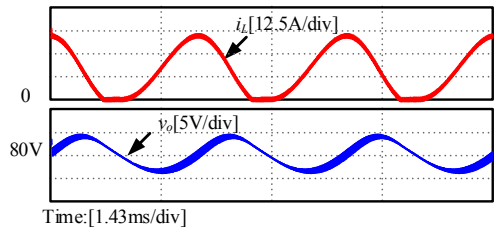
(a) the leading-edge modulation, G_{c1}



(b) the trailing-edge modulation, G_{c1}



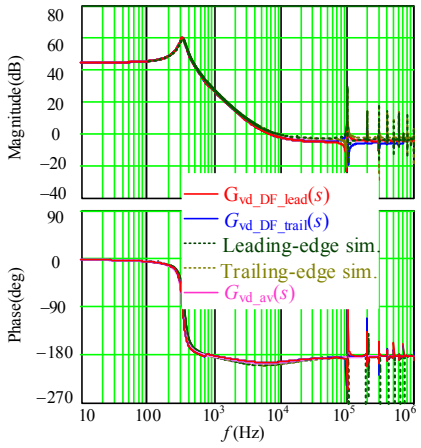
(c) the leading-edge modulation , G_{c2}



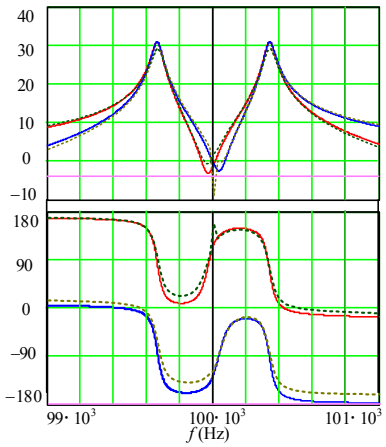
(d) the trailing-edge modulation, G_{c2}

Fig.2 Waveforms of the VMC Boost converter with different modulation and different controller

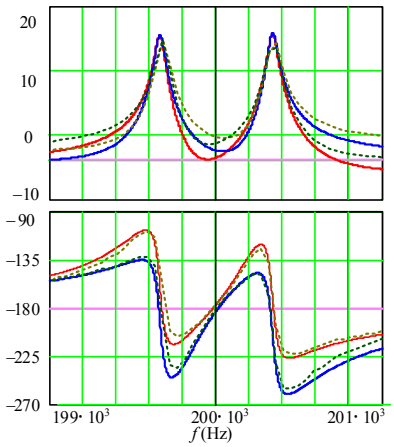
The comparison of $G_{vd}(s)$ when the different modulation is used are shown in Fig.3, and the switching frequency is 100kHz. As seen, in high-frequency region, there is a big difference between the response with different modulation, and the average model fails to describe the high-frequency characteristic of $G_{vd}(s)$. Also, Fig.3 shows the measurement results agree with the theoretical prediction of $G_{vd}(s)$, which was derived by using the describe function method as explained in Section II.



(a)



(b)



(c)

Fig. 3. (a)comparision of G_{vd}(s); (b) enlarge region of (a) around 100k; (c) enlarge region of (a) around 200k

Fig.4 and fig.5 show the comparison of loop gain and $G_{pwm}(s)$ when two compensators are used respectively. As seen, the theoretical prediction proposed in this paper and the measured results are in excellent agreement up to the switching frequency, and the average model have a big difference with the measured results in low frequency region which is apparent in fig.4(b) and fig.5(b).

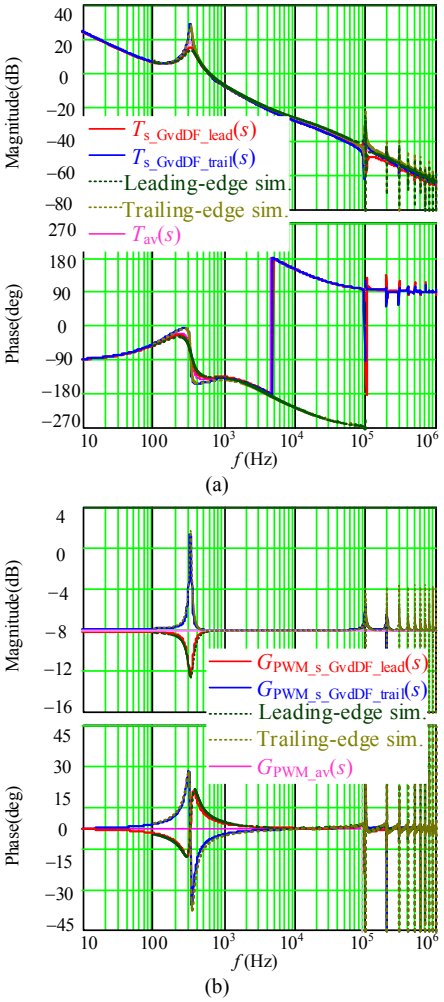


Fig. 4. (a) comparision of loop gain, (b) comparision of $G_{PWM}(s)$ between theoretical prediction and simulation results when $G_{c1}(s)$ is used

Although we have got the theoretical prediction which matches the simulation results, there still exists a question: How to deduce the instability case when the controller $G_{c2}(s)$ is used with the trailing-edge modulation, which the average model fails to explain. So, next we will use the approximate prediction, of which the detailed progress will be introduced in the future paper, to solve the problem. The approximate results of the expression in (1) and (2) could be concluded as expressed in (6) and (7), respectively, and the comparison with the simulation results are shown in Fig.6.

When $G_{c2}(s)$ is used, it would be found that $b_{\_lead}=5.5\times10^{-4}$ and $b_{\_trail}=-2.9\times10^{-4}$. Obviously, when the trailing-edge modulation is used with the controller $G_{c2}(s)$, the loop gain would contain two right-half plane poles. According to the Nyquist stability criterion, it could be found that the system will become unstable because the number of the counterclockwise encirclements of the (−1 + j0) point by the loop gain locus is not equal to the number of the RHP poles of the corresponding transfer function, which one can judge from Fig.6(a) and (7). Therefore, the aforementioned question could be explained, and the deduction is consistent with the actual unstable state.

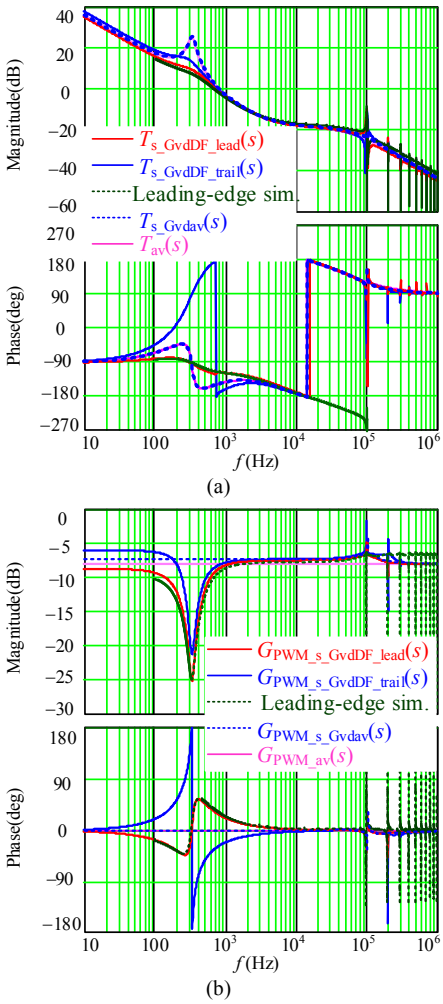


Fig. 5. (a) comparision of loop gain, (b) comparision of $G_{PWM}(s)$ between theoretical prediction and simulation results when $G_{c2}(s)$ is used.

To further illustrate the validity of the proposed model, the controller $G_{c3}(s)$ was chosen, the expression of which is as follows.

$$G_{c3}(s)=\frac{3.58\times10^{6}(s+2.83\times10^{3})(s+1.89\times10^{3})}{s(s+3.56\times10^{4})(s+2.23\times10^{4})} \tag{8}$$

When $G_{c3}(s)$ was used, the Boost converter would be stable with either modulation type. Fig.(7) shows the corresponding approximate prediction of the loop gain, and in this circumstance $b_{\_lead}=4\times10^{-4}$ and $b_{\_trail}=-1.7\times10^{-4}$. Then according to (7), one would find the loop gain with the controller $G_{c3}(s)$ and the trailing edge modulation also contain two right-half plane poles as the case when $G_{c2}(s)$ is used. In addition, fig.7 shows that the number of the counterclockwise encirclements of the (−1 + j0) point by the loop gain locus is equal to two. Therefore, one could infer that the Boost converter would be stable on the basis of the Nyquist stability criterion. The inference is consistent with the actual stable state.

$$\begin{cases} G_{PWM\_s\_GvdDF\_lead\_app}(s) = \dfrac{1}{V_m}\dfrac{L_eC_fs^2+(\dfrac{L_e}{R_{Ld}}+\dfrac{1}{D'}R_cC_f)s+1}{L_eC_fs^2+b_{lead}s+1} \\ G_{PWM\_s\_GvdDF\_trail\_app}(s) = \dfrac{1}{V_m}\dfrac{L_eC_fs^2+(\dfrac{L_e}{R_{Ld}}+\dfrac{1}{D'}R_cC_f)s+1}{L_eC_fs^2+b_{trail}s+1} \end{cases} \tag{6}$$

$$\begin{cases} T_{s\_GvdDF\_lead\_app}(s) = G_{vd\_av}(s)G_c(s)H_v\dfrac{1}{V_m}\dfrac{L_eC_fs^2+(\dfrac{L_e}{R_{Ld}}+\dfrac{1}{D'}R_cC_f)s+1}{L_eC_fs^2+b_{lead}s+1} \\ T_{s\_GvdDF\_trail\_app}(s) = G_{vd\_av}(s)G_c(s)H_v\dfrac{1}{V_m}\cdot\dfrac{L_eC_fs^2+(\dfrac{L_e}{R_{Ld}}+\dfrac{1}{D'}R_cC_f)s+1}{L_eC_fs^2+b_{trail}s+1} \end{cases} \tag{7}$$

Where,

$$\begin{cases} b_{lead} = \dfrac{L_e}{R_{Ld}}+\dfrac{1}{D'}R_cC_f+2\dfrac{V_o}{D'^2}\dfrac{1}{V_m}H_v2C_f\,\mathrm{Re}(G_c(j\omega_s)\dfrac{(e^{-j2\pi D}-1)}{2\pi j}) \\ b_{trail} = \dfrac{L_e}{R_{Ld}}+\dfrac{1}{D'}R_cC_f+2\dfrac{V_o}{D'^2}\dfrac{1}{V_m}H_v2C_f\,\mathrm{Re}(G_c(j\omega_s)\dfrac{(1-e^{-j2\pi D'})}{2\pi j}) \end{cases} \tag{7a}$$

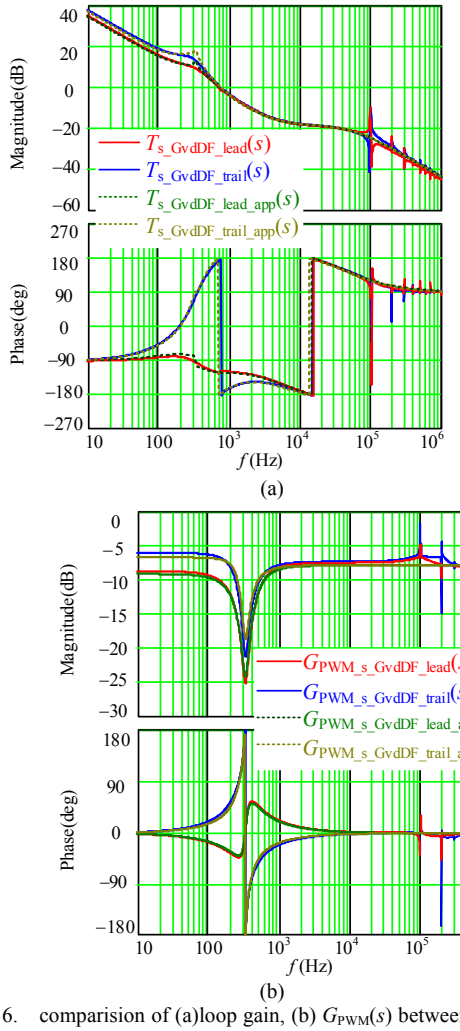


Fig. 6. comparision of (a)loop gain, (b) $G_{PWM}(s)$ between approximate theoretical prediction and simulation results when $G_{c2}(s)$ is used.

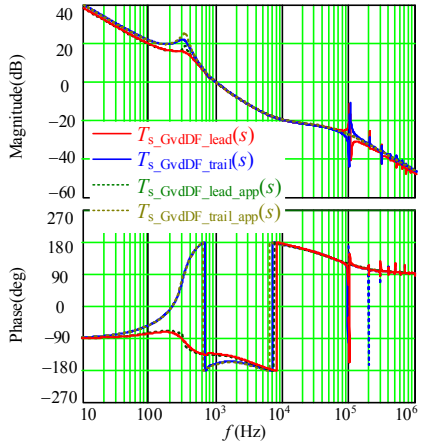


Fig. 7. comparision of loop gain between approximate theoretical prediction and simulation results when $G_{c3}(s)$ is used.

IV. Conclusions

In this paper, the sideband effect on the stability for the VMC boost converter by revising the existing loop gain model is analyzed. First, the small-signal transfer function of the PWM comparator is derived by selecting the time when the error signal intersects the ramp waveform as the start of each switching period by using the sample theory directly. The derivation can be regarded as an improvement of that in resent research. The result indicates that it is necessary to use the precisely duty ratio-to-output transfer function $G_{vd}(s)$ especially in the high-frequency region in order to arrive the low-frequency response of the loop gain for the VMC DC/DC converter, and this is ignored in previous research. Second, we give the theoretical prediction of $G_{vd}(s)$ by using the describe function method. The procedure is similar to that in [7],

while the time when the error signal intersects the ramp waveform is selected as the start of each switching period and all the sideband components of the error signal are included. Finally, it shows the excellent agreement between theoretical prediction and simulation results in the section III.

Perhaps the most important consequence of the sampled-data model(2), where $G_{vd}(s)$ is obtained by using the describe function method and can be expressed as (3), is that it bridges the gap between the existing loop gain model, which analyze the sideband effect quantitively, and the instability phenomenon mentioned above, thus allowing us to have a deeper understanding of the sideband effect on the stability for the closed-form DC/DC converter, and also paving a way for developing the modeling theory for DC/DC converter or the DC systems based on the averaging modeling strategic.

Although comparing to the averaging modeling, which is easy to understand and leads to the result with a simple form, the sample-data model is difficult to derive especially in the case when the high-frequency characteristic of the power stage transfer function need to obtain though the describe function, it has the distinct advantage in precisely predicting the loop gain model, thus helping us to explain more instability phenomenon which the average modeling fails to predict. Given that for a long time in the future the average modeling will be a popular and useful method for designing the regulators in the DC systems, the sample-data model could be regarded as a supplement in some certain cases. In other words, in the situation when the high-bandwidth DC system is required or the components around the switching frequency(or multiple switching frequency) couldn't be neglected, one could firstly use the averaging model to design the controller, then exploit the sample-data model to check the stability and deduce how to revise the controller in order to keep a balance between the improvement of the system performance and the stability.

The insights that have emerged from the work in this paper suggests that the loop gain model represented by (2) is yet to be conceived. This encourages a renewed research into the connection between the sample-data model and the instability phenomenon in the DC/DC converter and DC system, and promises to yield fruitful theoretical results. In this progress, it is the responsibility of the circuit designers to analysis the instability phenomenon carefully and conclude which type of the instability phenomenon is caused by the sideband effect. Obviously, the work in this paper is a small part of this progress, and the next work that develops sample-data model theory by combining the instability phenomenon will be continued.

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