Evaluation and Application of 600 V GaN HEMT in Cascode Structure

Xiucheng Huang, *Student Member, IEEE*, Zhengyang Liu, *Student Member, IEEE*, Qiang Li, *Member, IEEE*, and Fred C. Lee, *Life Fellow, IEEE*

***Abstract*—Gallium nitride high electron mobility transistor (GaN HEMT) has matured dramatically over the last few years. A progressively larger number of GaN devices have been manufactured for in field applications ranging from low power voltage regulators to high power infrastructure base-stations. Compared to the state-of-the-art silicon MOSFET, GaN HEMT has a much better figure of merit and shows potential for high-frequency applications. The first generation of 600 V GaN HEMT is intrinsically normally on device. To easily apply normally on GaN HEMT in circuit design, a low-voltage silicon MOSFET is in series to drive the GaN HEMT, which is well known as cascode structure. This paper studies the characteristics and operation principles of a 600 V cascode GaN HEMT. Evaluations of the cascode GaN HEMT performance based on buck converter at hard-switching and soft-switching conditions are presented in detail. Experimental results prove that the cascode GaN HEMT is superior to the silicon MOSFET, but it still needs soft-switching in high-frequency operation due to considerable package and layout parasitic inductors and capacitors. The cascode GaN HEMT is then applied to a 1 MHz 300 W 400 V/12 V LLC converter. A comparison of experimental results with a state-of-the-art silicon MOSFET is provided to validate the advantages of the GaN HEMT.**

***Index Terms*—Cascode structure, gallium nitride high electron mobility transistor (GaN HEMT), hard-switching, normally on, soft-switching.**

TABLE I
MATERIAL PROPERTIES OF GAN, SIC, AND SILICON

Properties	GaN	SiC	Si
Bandgap, E_G(eV)	3.4	3.2	1.12
Breakdown field, E_B(MV/cm)	3.3	3.5	0.3
Saturated drift velocity, Vs(10^7cm/s)	2.5	2.0	1.0
Electron mobility, μ(cm^2/Vs)	2000*	650	1500

*Electron mobility of GaN with 2DEG is 2000.

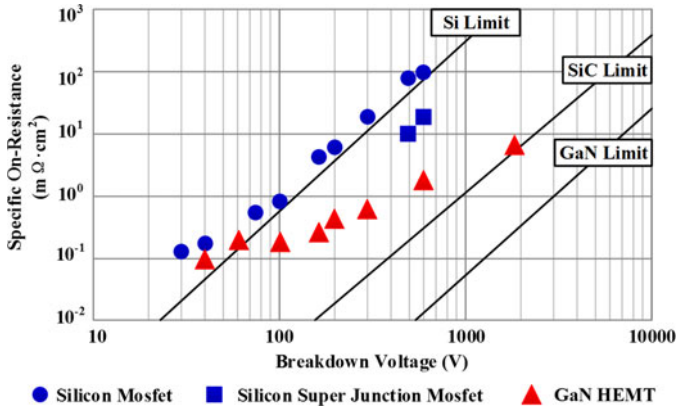

Fig. 1. Specific on-resistance versus breakdown voltage for GaN, SiC, and Si.

I. INTRODUCTION

THE future power converters not only must meet the characteristics demanded by the load but also have to achieve high power density with high ambient temperature, high efficiency, and high reliability. High power density is one of the key drivers and metrics for the advancement of power conversion technologies.

Generally speaking, a high-performance active device is the first force to push power density to meet the requirement of modern systems. Silicon has been a dominant material in power management since the late 1950s. However, due to continuous device optimizations and improvements in the production process, the material properties of silicon have increasingly become the limiting factor. Workarounds like the super junction stretch the limits but usually at substantial cost [1]–[3]. In recent years, gallium nitride high electron mobility transistor (GaN HEMT) has emerged as a promising device for high-frequency, high density power conversion [4]–[14]. The material properties of GaN as well as silicon and SiC are compared in Table I [1]. One way of translating these basic crystal parameters into a comparison of device performance is to calculate the best theoretical performance that could be achieved in each of these candidates. As shown in Fig. 1, the saturation limit of GaN is far beyond silicon and SiC [15]. The first generation of GaN HEMTs have proved that the GaN HEMT has a superior relationship between the on resistance and breakdown voltage than the silicon MOSFET due to a higher electrical field strength and enhanced mobility of electrons in the two-dimensional electron gas (2DEG). This translates into a GaN HEMT with a smaller die size for a given $R_{\mathrm{ds\_on}}$ and breakdown voltage, which directly increases power density.

Furthermore, GaN HEMT has a much smaller gate charge and junction capacitors when compared to the silicon MOSFET. A smaller gate charge achieves a faster turn-on/off speed for the devices, and a smaller junction capacitor stores less energy

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The authors are with the Bradley Department of Electrical and Computer Engineering, Center for Power Electronics Systems, Virginia Polytechnic Institute and State University Blacksburg, Blacksburg, VA 24061 USA (e-mail: xiucheng@vt.edu; lzy@vt.edu; lqvt@vt.edu; fclee@vt.edu).

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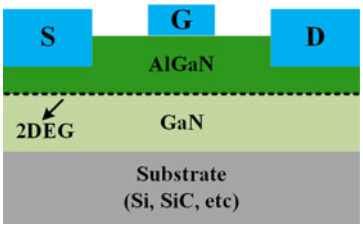

Fig. 2. Basic structure for GaN HEMT.

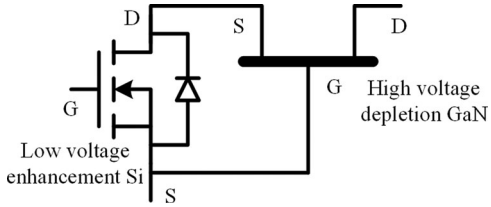

Fig. 3. Cascode configuration: a high voltage normally on GaN HEMT with a low-voltage normally off Si MOSFET.

during the turn-off period. Both of these characteristics are able to shorten the current and voltage transition interval and thus reduce switching loss. In general, the high performance of GaN HEMT provides the opportunity to achieve a higher frequency compared to the silicon MOSFET with the same efficiency. The switching frequency has been continuously pushed up to several megahertz to reduce the passive components size and increase power density [4], [5], [10], [11], [13], [14].

However, the switching loss of GaN HEMT is not only determined by the GaN die but is also related to the parasitic inductors of the device package and printed circuit board (PCB) layout [13]. These parasitic inductors will deteriorate the switch transition and increase the switching loss. Furthermore, the device junction capacitor still introduces a significant loss in hard-switching conditions, especially in bridge configuration. As far as we know, soft-switching technique is still beneficial for GaN HEMT to achieve high efficiency in high-frequency operation.

This paper aims to evaluate the static and dynamic performance of 600 V GaN HEMT. The characteristics of 600 V GaN HEMT are illustrated in Section II. Evaluation of the GaN HEMT performance based on hard-switching buck converter is shown in Section III. Comparisons between the GaN HEMT and the silicon MOSFET are presented. Section IV analyzes the switching loss of the GaN HEMT based on a buck converter under hard-switching and soft-switching conditions. Section V presents the application of the GaN HEMT in a 1 MHz 300 W 400 V/12 V LLC converter prototype. Experimental results compared with a silicon MOSFET are also provided to validate the advantages of the GaN HEMT.

II. Characteristics of 600 V GaN HEMT

Fig. 2 shows the typical 600 V GaN device structure including the 2DEG at the junction of the AlGaN–GaN boundary in which the electrons have extremely high mobility that produces the low on resistance of the GaN transistors [3]. It is also the reason these devices are called HEMTs rather than field effect transistors (FETs). It is clear then that the native nature of this device structure is a JFET with a high electron mobility channel and conducts in the absence of applied voltage (normally on).

Several techniques have been developed to provide a built-in modification of the 2DEG under the gated region, providing for normally off behavior [7], [10], [16]. However, one of the desirable features for normally off GaN HEMTs is gate overdrive protection [16]. When the switch is turned on, the Schottky gate of GaN HEMT is usually switched beyond the forward turn-on voltage to obtain the minimum on resistance. Due to the exponential current/voltage characteristic beyond the forward turn-on voltage, small increases in the forward bias could result in an excessive gate current that may lead to device failure.

Compared to the normally off GaN HEMT, the driving voltage for a normally on GaN HEMT can be extended to –30 to 2 V and –5 V is required to fully turn on, which has a sufficient safety driving margin. To easily apply a normally on GaN HEMT in circuit design, a low-voltage silicon MOSFET is used in series to drive the GaN HEMT, which is well known as cascode structure and is shown in Fig. 3.

The turn-on/off principles of the cascode GaN HEMT are briefly illustrated as follows. During the turn-on period, the silicon MOSFET gate–source capacitor C_{GS_Si} is charged until the threshold voltage is reached. Then, the MOSFET channel is conductive and displacement current flows through C_{GD_Si} and C_{DS_Si}. In parallel to C_{DS_Si}, the GaN HEMT gate–source capacitor C_{GS_GaN} is charged. When the rising gate voltage at the GaN HEMT exceeds the threshold value, the GaN HEMT channel is conductive and the drain–source voltage of the GaN HEMT is lowered. Eventually, the GaN HEMT gate–source voltage reaches nearly zero and it is fully turned on.

During the turn-off period, the gate of the silicon MOSFET is discharged through a driving circuit until it falls to the value where the MOSFET enters the saturation region. The load current charges the C_{DS_Si} and $_{GD\_Si}$ and forces the MOSFET drain–source voltage to rise. In parallel to C_{DS_Si}, the GaN HEMT C_{GS_GaN} is simultaneously discharged until it reaches the value where the GaN HEMT enters the saturation region. Then, the GaN HEMT drain–source voltage rises to the steady-state condition. Meanwhile, the load current transfers from the cascode GaN HEMT to the other switch.

In general, controlling the on/off state of the low-voltage silicon MOSFET to control the on/off state of the high-voltage GaN HEMT makes the cascode GaN HEMT behave as an enhancement device that is compatible with the commercial driver.

To further understand the steady operation of the cascode GaN HEMT, the $I-V$ curve is shown in Fig. 4, which is derived from the simulation model. The terminal behavior is just like a normally off MOSFET. There could be three conduction modes in real application during steady state. For each conduction mode, the drain to source voltage is calculated as follows:

$$v_{ds}=\begin{cases} i_{ds}\cdot\left(R_{\mathrm{DS\_GaN}}+R_{\mathrm{DS\_Si}}\right), v_{gs\_Si}=10\,\mathrm{V}, & i_{ds}>0 \\ -i_{sd}\cdot\left(R_{\mathrm{DS\_GaN}}+R_{\mathrm{DS\_Si}}\right), v_{gs\_Si}=10\,\mathrm{V}, & i_{sd}>0 \\ -\left(i_{sd}\cdot R_{\mathrm{DS\_GaN}}+v_{bd\_Si}\right), v_{gs\_Si}=0\,\mathrm{V}, & i_{sd}>0 \end{cases}. \quad (1)$$

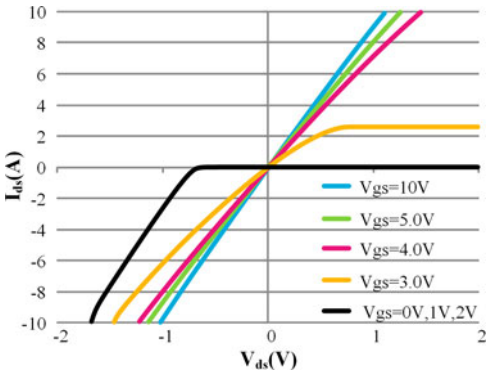

Fig. 4. $I-V$ characteristic of cascode GaN HEMT.

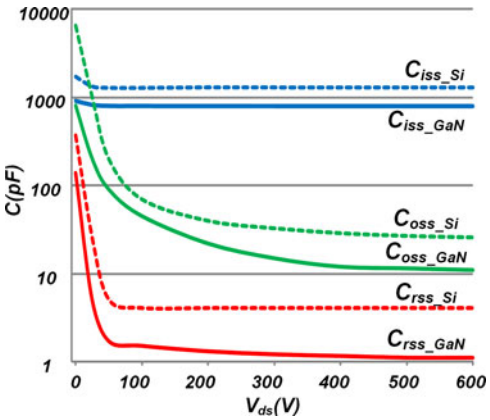

Fig. 5. $C-V$ characteristic of cascode GaN transistor.

In general, the on-resistance of the low-voltage silicon MOSFET is much smaller than the GaN HEMT. Therefore, the GaN HEMT dominates the conduction loss at steady state both in the first- and third-quadrant operation. It should be noted that in the third-quadrant operation, silicon body diode conducting introduces higher loss, which should be avoided.

Another important characteristic of the cascode GaN HEMT is the $C-V$ curve, which is shown in Fig. 5. As a comparison, the $C-V$ curve of a 600 V state-of-the-art super junction silicon MOSFET with the same $R_{\mathrm{ds\_on}}$ is also presented as the dash line. It is well known that recent GaN HEMTs all adopt a lateral structure and this makes them a very low capacitance device compared to the silicon MOSFET. In normal cases, a small capacitance enables fast switching speed and shortens voltage and current communication time. Furthermore, a small capacitance stores less energy during off state and, thus, dissipates less during turn-on transition.

III. Comparison of 600 V Cascode GaN HEMT and State-of-the-Art Silicon MOSFET Based on Hard-Switching Buck Converter

To make a clear comparison between the 600 V cascode GaN HEMT and the state-of-the-art silicon MOSFET, an open-loop 300–50 V synchronous buck converter is built, which is shown in Fig. 6. The switching frequency is 500 kHz. The converter

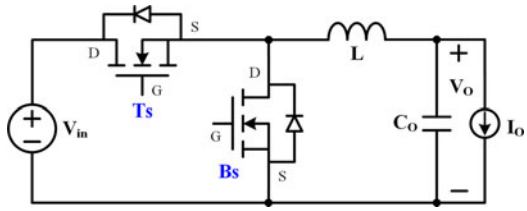

Fig. 6. Synchronous buck converter.

TABLE II
Parameters of TPH2002 (Cascode GaN HEMT) and State-of-the-Art Silicon MOSFET

Parameters	TPH2002*	FCP13N60N**
V_{ds_max}(V)	600	600
R_{ds_on}(Ω)	0.25	0.25
Q_g(nC)	6.2	40
Q_{rr}(nC)	13	3500
C_{oss_tr}(pF)/C_{oss_er}(pF)	45/25	150/60

*TPH2002 is from Transphorm Inc.
**FCP13N60N is super junction MOSFET from Fairchild Inc.

operates in continuous conduction mode (CCM) and the inductor current ripple is 1.5 A. The top switch and bottom switch represent either a cascode GaN HEMT or silicon MOSFET. Parameters are listed in Table II. It clearly shows that the gate charge Q_g of the cascode GaN HEMT is much smaller than the silicon MOSFET, which can directly save driving loss. The other two parameters are related to switching loss. The cascode GaN HEMT has a small amount of Q_{rr} due to the low-voltage silicon MOSFET, which is negligible, compared to the high-voltage silicon MOSFET. Another advantage of the cascode GaN HEMT is the smaller C_{oss} that stores less energy for dissipation at hard-switching conditions.

To differentiate the impact of Q_{rr} and C_{oss} on converter efficiency, two sets of experiments are implemented. The first one applies the silicon MOSFET as the top switch (T_s), and the silicon MOSFET or the cascode GaN HEMT as the bottom switch (B_s) in order to evaluate the Q_{rr} impact. The second set applies the cascode GaN HEMT as the bottom switch, and the silicon MOSFET or the cascode GaN HEMT as the top switch to evaluate the C_{oss} impact.

A. Q_{rr} Impact

It is well known that the reverse recovery charge of the bottom switch in buck converter will increase the turn-on loss of the top switch under CCM condition. The main reason is that during reverse recovery period, the bottom switch cannot block reverse voltage; the drain to source voltage of top switch is clamped at input voltage. While the top switch current increases very fast to support load current and bottom switch reverse recovery charge current. Therefore, the top switch turn-on switching energy that is integral of voltage and current across the device is quite large. Fig. 7 shows the comparison of the top switch turn-on transition waveforms. With the silicon MOSFET as the bottom switch, the transition time is about 30 ns. However, with the cascode GaN HEMT as the bottom switch, the time period is only 18 ns.

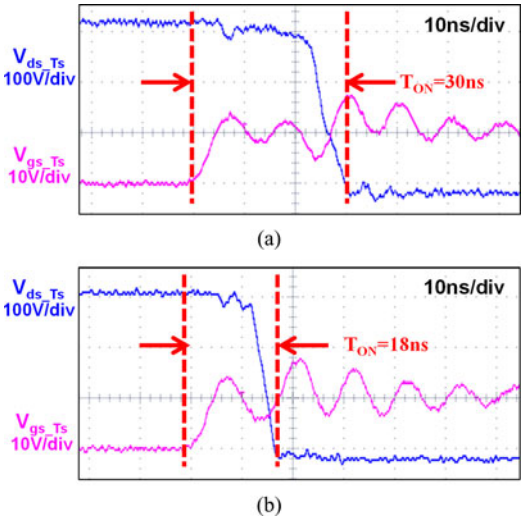

Fig. 7. Top switch turn-on transition waveforms: (a) silicon MOSFET as bottom switch and (b) cascode GaN HEMT as bottom switch.

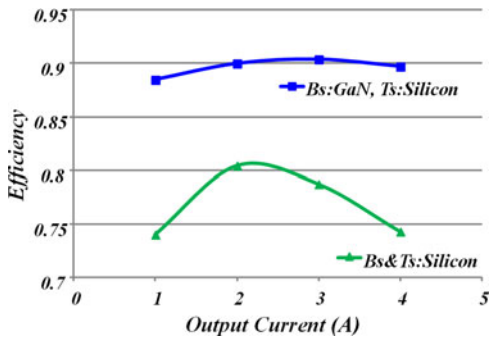

Fig. 8. Efficiency comparison (bottom switch: cascode GaN HEMT versus Si MOSFET; Top switch: Si MOSFET).

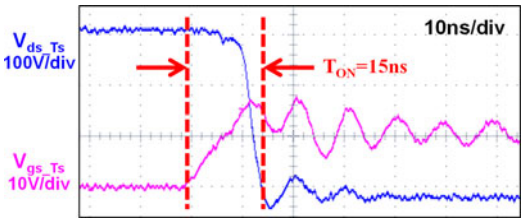

Fig. 9. Top switch turn-on transition waveforms (both top and bottom switches are cascode GaN HEMT).

Fig. 8 shows the test efficiency. Applying the cascode GaN HEMT as the bottom switch can improve efficiency over 15% under 4 A output condition, which saves more than 30 W on reverse recovery loss as expected.

B. C_{oss} Impact

The energy stored in C_{oss} of the top switch during the turn-off period is dissipated during the turn-on transition in buck converter under CCM condition. A smaller C_{oss} means a smaller switching loss. Fig. 9 shows the top switch turn-on transition waveform where both the top and bottom switches are cascode GaN HEMT. The turn-on transition time has shortened to 15 ns, which is critical for turn-on switching loss. Fig. 10 shows the

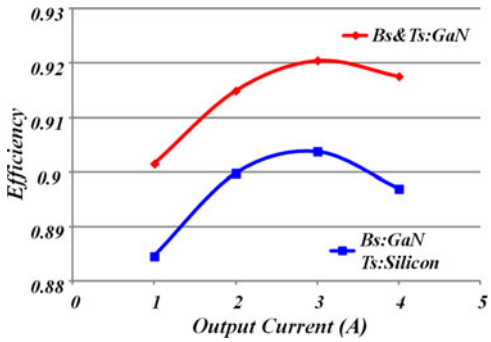

Fig. 10. Efficiency comparison (top switch: cascode GaN HEMT versus Si MOSFET; bottom switch: cascode GaN HEMT).

TABLE III
PARAMETERS OF BUCK CONVERTER

Parameters	Value	Parameters	Value
Input voltage	380V	Output voltage	200V
Switching frequency	500kHz	Maximum output current	6A
Inductor core material	3F35	Inductor current ripple	3A
Top switch	TPH2006*	Bottom switch	TPH2010*

*TPH2006 is from Transphorm Inc. V_{ds_max} = 600V, R_{ds_on} = 0.15Ω.
*TPH2010 is schottky diode from Transphorm Inc. V_{BR} = 600V, V_F = 1.3V@6A.

test efficiency. When the cascode GaN HEMT is used as the top switch, the efficiency is 2% higher than when the silicon MOSFET is used as the top switch.

At hard-switching condition, the cascode GaN HEMT is definitely better than the comparable silicon MOSFET. Applying the cascode GaN HEMT as the bottom switch can minimize the reverse recovery charge. Applying the cascode GaN HEMT as the top switch can further shorten the transition time, thus improving efficiency. However, the power loss of the converter with the cascode GaN HEMT is still quite high. The detailed loss analysis of the cascode GaN HEMT is presented in Section IV.

IV. Loss Analysis of 600 V Cascode GaN HEMT Based on Buck Converter

In this section, the detailed loss analysis is presented based on buck converter with experimental and simulation results. The most powerful tool to analyze the device loss is an accurate loss model. Simulation models for silicon MOSFET are commonly used to investigate the device performance. One of the advantages of the simulation model is that the voltage and current information of every node in the simulation can be easily derived. With great effort, the authors cooperate with Transphorm Inc. and develop a 600 V cascode GaN HEMT SPICE simulation model [17]. The accuracy of this model is validated by numerous experiments. The simulation waveforms match with the experimental results very well including the *dv*/*dt*, *di*/*dt*, magnitude, and frequency of voltage/current ringing during transition. Thus, this simulation model can be used to help analyze the transistor loss.

The key parameters for the hardware setup are listed in Table III. It is common sense that common source inductance, which is defined as the inductance shared by the power loop and

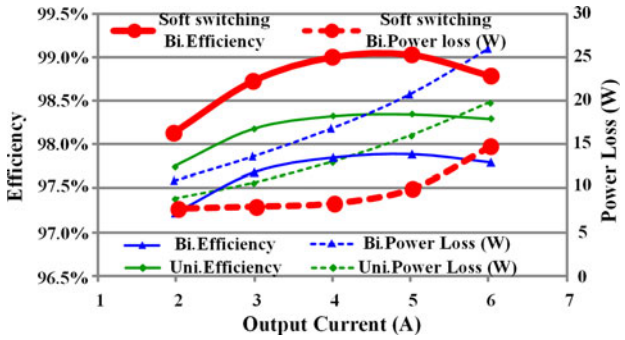

Fig. 11. Converter efficiency and power loss (Solid line: efficiency. From top to bottom: Soft-switching CRM bidirectional; CCM unidirectional; CCM bidirectional. Dash line: power loss. From top to bottom: CCM bidirectional; CCM unidirectional; Soft-switching CRM bidirectional).

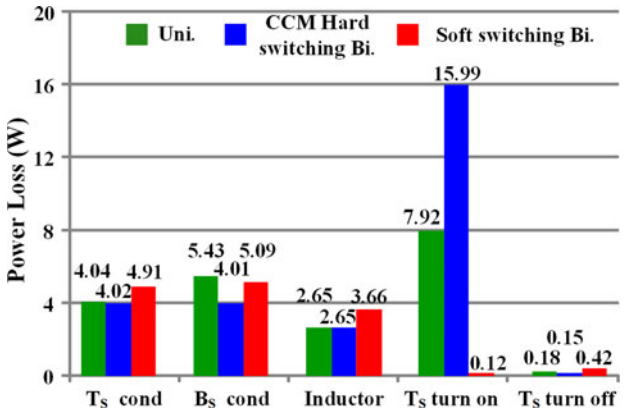

Fig. 12. Buck converter loss breakdown at 6A output current condition (Left bar: CCM unidirectional; middle bar: CCM bidirectional; right bar: soft-switching CRM bidirectional).

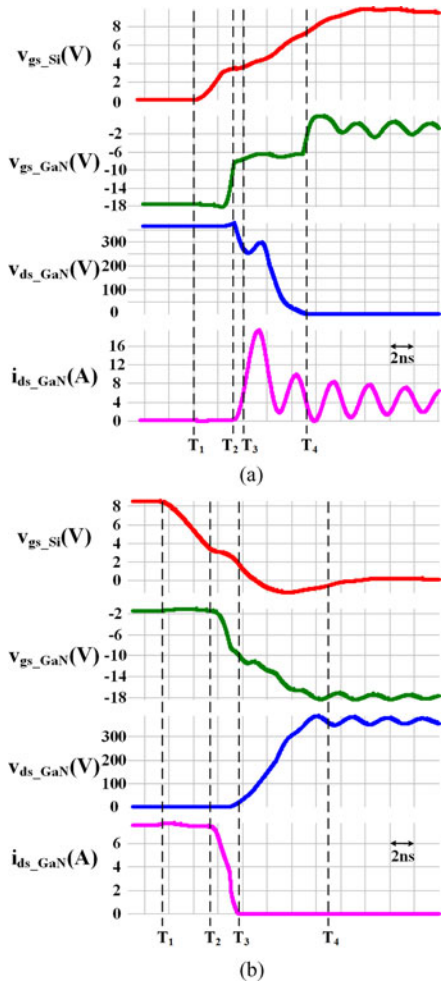

Fig. 13. Top switch turn-on/off transition waveforms with GaN Schottky diode as bottom switch: (a) turn on at 4.5 A and (b) turn off at 7.5 A.

driving loop impacts the switching loss significantly. In addition, the power loop inductance plays an important role on switching performance [18]–[20]. Therefore, the layout of the PCB is designed to eliminate the common source inductance (excluding package parasitic inductance) and minimize power loop inductance. The package for the cascode GaN HEMT also introduces nanohenry-level inductance switching performance [18]–[20]. Therefore, the layout of the PCB is designed to eliminate the common source inductance (excluding package parasitic inductance) and minimize power loop inductance. The package for the cascode GaN HEMT also introduces nanohenry-level parasitic inductance. The package and layout inductance is extracted from Ansoft Q3D FEA simulation, and it is then applied in SPICE simulation.

A. CCM Unidirectional Buck Converter

In the first setup, a Schottky diode is applied as the bottom switch to eliminate the reverse recovery impact. The middle solid line in Fig. 11 shows the converter efficiency and the middle dash line shows the total loss dissipation based on the experimental results. Then, the loss breakdown at 6 A output condition based on the device simulation model is shown as the left bar bar in Fig. 12. The inductor loss is measured by Mu's method [21]. Other loss terms are negligible compared to these five loss bars. The turn-on loss is 40 times larger than the turn-off loss under hard-switching conditions, which is quite different from the low-voltage condition [18]–[20].

For the top switch turn-on transition, the simulation waveforms are shown in Fig. 13(a). $v_{\mathrm{gs\_Si}}$ is the gate–source voltage of the low-voltage silicon MOSFET in the cascode structure. The other three waveforms are the gate–source voltage, drain–source voltage, and drain–source current of the GaN HEMT in the cascode structure. The switching loss of the low-voltage silicon MOSFET is negligible, which is true in this condition. At T_1 instant, the gate voltage is applied to the silicon MOSFET. Then, $v_{\mathrm{gs\_Si}}$ is charged up and the channel becomes conductive. The gate–source voltage of the GaN HEMT, which is in reverse parallel with the drain–source voltage of the silicon MOSFET, is charged toward the threshold voltage. At T_2 instant, the GaN HEMT is conductive and $i_{\mathrm{ds\_GaN}}$ starts to increase. At T_3 instant, the GaN HEMT current reaches the inductor current and then the GaN HEMT current supports both inductor current and bottom diode junction capacitor charging current during T_3 to T_4. During this period, the current overshoot is huge ($I_{\mathrm{pk}} =$ 18 A) and saturates the channel as the GaN HEMT is not yet

fully turned on in normal cases. Therefore, $v_{\mathrm{ds\_GaN}}$ increases instead of decreases in the first half of this stage. In fact, this phenomenon can also be observed with standalone switch under high-voltage test condition [22], [23]. Eventually the voltage across bottom diode is charged up with the overshoot current of the top switch, and this allows the $v_{\mathrm{ds\_GaN}}$ to be decrease to zero. The voltage and current transition time is about 6.1 ns and the energy dissipation is about 15.8 μJ which is 7.9 W loss at 500 kHz. Therefore, charging the output capacitor of the bottom switch increases the current overshoot and, thus, increases the turn-on switching loss.

For the top switch turn-off transition, the simulation waveforms are shown in Fig. 13(b). At T_1 instant, the gate driving signal is removed, and then the silicon MOSFET gradually enters the saturation region. The drain–source voltage of silicon MOSFET increases, which also means $v_{\mathrm{gs\_GaN}}$ decreases. At T_2 instant, the GaN HEMT enters the saturation region and the channel current starts to decrease and $v_{\mathrm{ds\_GaN}}$ starts to increase. Because of the internal current source turn-off mechanism, which is unique to cascode structure, $v_{\mathrm{gs\_GaN}}$ shortly drops below the pinch off value at T_3 [24]. Then, the rest of the terminal current charges the C_{oss} of the top switch and, consequently, $v_{\mathrm{ds\_GaN}}$ rises to the steady-state value. The inductor current transfers from the top switch to the bottom switch. It clearly shows that the voltage and current transition time is short and the energy dissipation is about 0.2 μJ. This value is extremely small compared to the same level silicon MOSFET, which is typically larger than 5 μJ. During the turn-off transition, the low-voltage silicon MOSFET dissipates about 0.2 μJ energy.

B. CCM Bidirectional Buck Converter

The bidirectional buck converter is widely used in industrial applications. Compared to the aforementioned unidirectional buck converter, a cascode GaN HEMT is applied as bottom switch. The dead time is fine tuned to optimize the converter efficiency over all load range. The bottom solid line in Fig. 11 shows the converter efficiency and the top dash line shows the power loss. It clearly shows that the bidirectional buck converter efficiency is lower that the unidirectional one. Then, the middle bar in Fig. 12 shows the loss breakdown at 6 A output condition based on the simulation model. The turn-on loss increases to 16 W, twice larger than the unidirectional case. The other loss bars do not change much.

Fig. 14 shows the top switch turn-on transition waveforms of the bidirectional case. The analysis of the transition period is similar to the unidirectional case. The main difference is that the reverse recovery charge of the bottom switch increases the current overshoot ($I_{\mathrm{pk}} = 23$ A) and transition time ($T_{\mathrm{tr}} = 8.3$ ns). The area of $I_{\mathrm{ds\_GaN}}$ larger than I_L means the reverse recovery charge as well as junction capacitor charge. The energy dissipation is 32 μJ, which is 16 W at 500 kHz. At hard-switching condition, applying any active switch with reverse recovery charge as the bottom switch will deteriorate the top switch turn-on transition, thus increasing the turn-on loss dramatically.

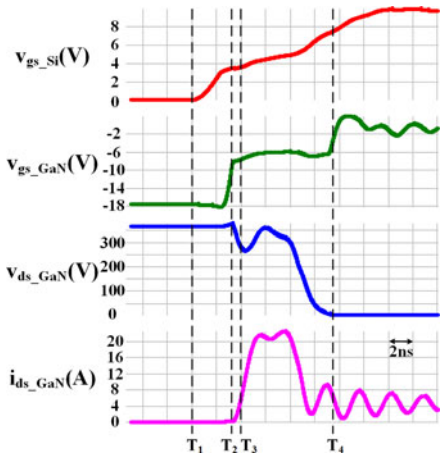

Fig. 14. Top switch turn-on transition with cascode GaN HEMT as bottom switch at hard-switching condition.

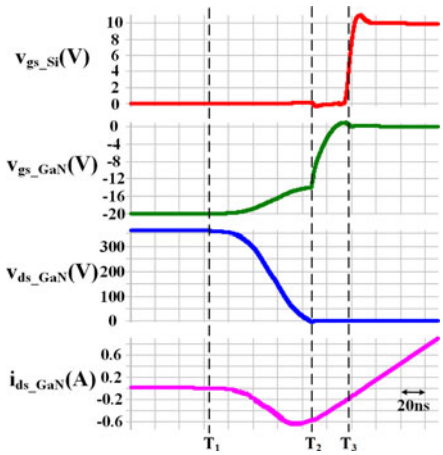

Fig. 15. Top switch turn-on transition with cascode GaN HEMT as bottom switch at CRM.

C. Critical Conduction Mode (CRM) Bidirectional Buck Converter

Operating the buck converter at CRM, the bottom switch is turned off with zero current, thus eliminating the reverse recovery effect. Based on the input–output condition, the top switch can achieve zero-voltage turn on, which further removes the junction capacitor charge effect. Fig. 15 shows key waveforms of top switch turn-on transition waveforms in CRM buck converter. The turn-off transition is similar with CCM hard-switching condition. At T_1 instant, the buck inductor resonates with junction capacitors of top and bottom switches. $v_{\mathrm{ds\_GaN}}$ naturally decreases to zero at T_2. The remaining negative inductor current continues to discharge the drain–source voltage of silicon MOSFET in the cascode structure, as well as gate–source voltage of the GaN HEMT. At T_3 instant, gate signal is applied. zero-voltage switching (ZVS) operation is achieved as long as the inductor current is still negative at T_3.

The top solid line in Fig. 11 shows the converter efficiency with soft-switching and the bottom dash line shows the power loss. The right bar in Fig. 12 shows the loss breakdown at 6 A output condition and it clearly shows that the turn-on loss is

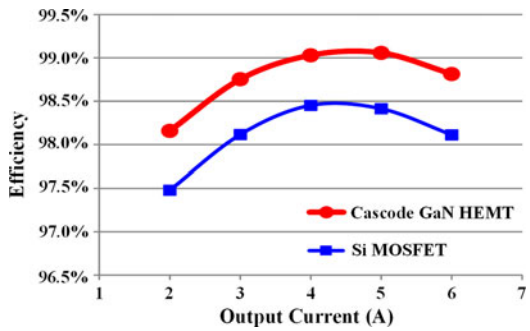

Fig. 16. CRM buck converter efficiency comparison (Top line: cascode GaN HEMT; Bottom line: Si MOSFET).

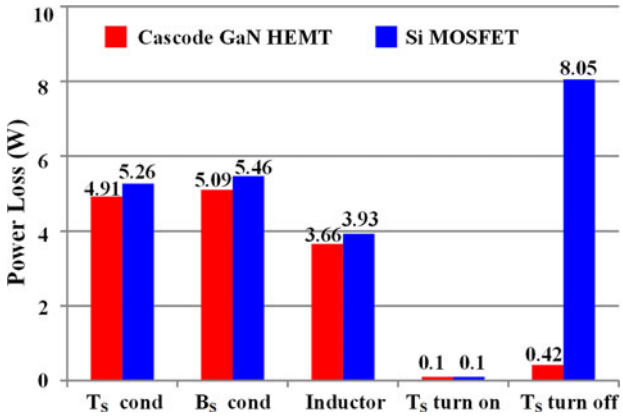

Fig. 17. CRM buck converter loss breakdown at 6A output condition (left bar: cascode GaN HEMT; right bar: Si MOSFET).

minimized and only introduces a little more conduction loss with CRM operation. The increase of conduction loss at CRM is due to the increase of root mean square (rms) value of inductor and switch current. The rms value of triangular waveform (CRM) is definitely larger than square waveform (CCM) with same average value.

In a word, in high-voltage low current buck converter with cascode GaN HEMT, usually below 10 A, turn-on loss dominates in hard-switching conditions, and turn-off loss is very small due to the intrinsic current source driving mechanism. Actually, this is also true in other topologies, such as boost, buck–boost, etc. Applying a Schottky diode as the bottom switch at CCM hard-switching operation is more efficient due to a small reverse recover charge. While with soft-switching operations, turn-on loss is minimized and introduces a little more conduction loss. It should be noticed that the turn-off loss remains low even the turn-off current doubles. This characteristic makes the cascode GaN HEMT very suitable for high-frequency operation as long as zero-voltage turn on is achieved.

Section III has demonstrated that the cascode GaN HEMT is superior to the state-of-the-art silicon MOSFET at CCM hard-switching condition. Fig. 16 shows efficiency comparison between the cascode GaN HEMT and the silicon MOSFET at CRM soft-switching condition. It clearly shows that the cascode GaN HEMT gains 0.7%–0.8% efficiency improvements at CRM soft-switching condition. Fig. 17 shows the loss breakdown at 6 A output condition. The cascode GaN HEMT has

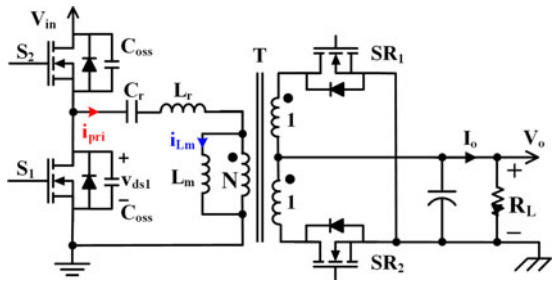

Fig. 18. LLC resonant converter.

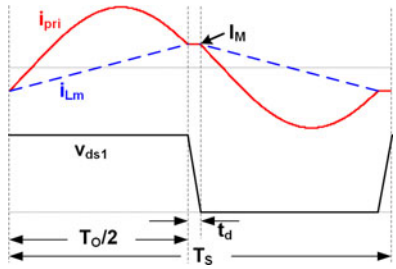

Fig. 19. Relationship of dead time and magnetizing current.

much smaller turn-off loss due to current source turn-off mechanism, which is unique to the cascode structure. Also the cascode GaN HEMT has smaller conduction loss because smaller junction capacitor requires smaller circulating energy to achieve ZVS operation.

V. Application of 600 V Cascode GaN HEMT in 1 MHz LLC Converter

Resonant converters can achieve ZVS and enable power supplies to operate at high switching frequencies with high efficiency. In particular, the LLC resonant converter operating at resonant frequency can achieve ZVS for primary side switches and zero-current switching (ZCS) for secondary-side rectifiers, which is shown in Fig. 18. Therefore, the LLC resonant converter has very low switching loss and is suitable for high-frequency high density power supply applications. The operation principle and design procedure of LLC converter can refer to [25]–[27].

One limitation of conventional design with silicon MOSFET is the tradeoff between dead time and magnetizing current, which is shown in Fig. 19. I_M is the peak value of magnetizing current; T_O is the resonant period formed by resonant inductor and capacitor; T_S is the switching period. Dead time and magnetizing current serve to discharge $C_{\rm oss}$ and thus achieve ZVS. This relation can be described as follows:

$$C_{\rm OSS} \approx \frac{I_m \cdot t_{\rm d}}{2V_{\rm in}}. \tag{2}$$

Silicon MOSFET has a large junction capacitor that requires either longer dead time or larger magnetizing current to achieve ZVS. Both of these approaches deteriorate the converter efficiency significantly in high-frequency operation.

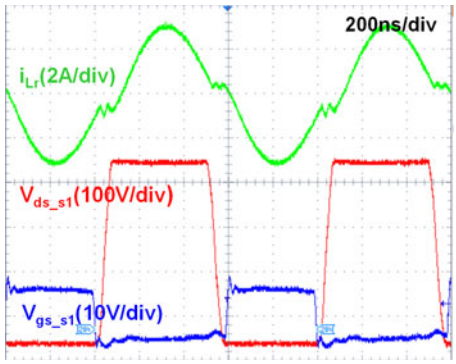

Fig. 20. Key waveforms with cascode GaN HEMT.

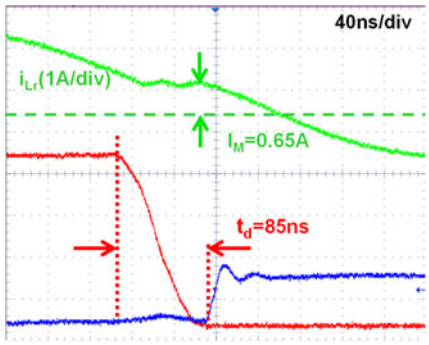

Fig. 21. Zoom in waveforms with cascode GaN HEMT.

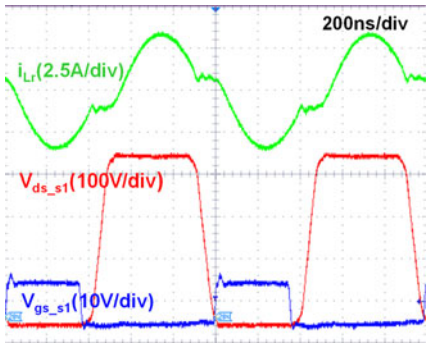

Fig. 22. Key waveforms of with silicon MOSFET.

However, the limitation is a minor issue with cascode GaN HEMT due to very small $C_{\rm oss}$, which has already been mentioned in Section II. To highlight the better characteristics of the cascode GaN HEMT, a state-of-the-art silicon MOSFET is also adopted as the primary switch for comparison. The parameters are shown in Table II.

The experimental waveforms of 1 MHz 300 W 400 V/12 V LLC prototype with cascode GaN HEMT and silicon MOSFET are shown in Figs. 20–23, respectively. It clearly shows that for the GaN prototype, the dead time is 85 ns and the magnitude of magnetizing current is 0.65 A. While for the silicon MOSFET prototype, it takes 105 ns dead time and 1.2 A magnetizing current to achieve ZVS. A shorter dead time and a smaller magnetizing current mean a smaller rms current on the primary and secondary side. Furthermore, the cascode GaN HEMT has a much smaller Q_g, which saves a lot on driving loss and further increases converter efficiency. The efficiency shown in Fig. 24

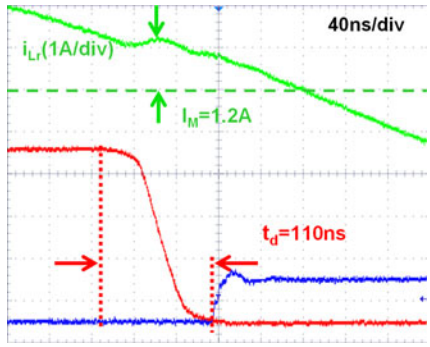

Fig. 23. Zoom in waveforms with silicon MOSFET.

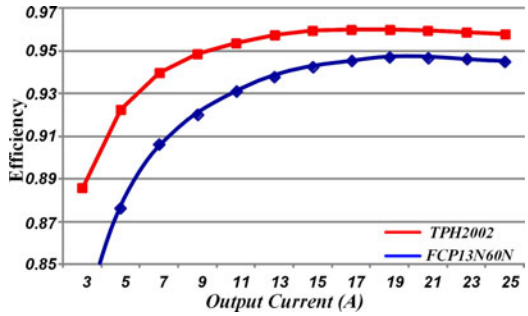

Fig. 24. Efficiency comparison between cascode GaN HEMT and state-of-the-art silicon MOSFET in 1 MHz LLC converter.

clearly validates the advantages of GaN HEMT. At full-load condition, the cascode GaN HEMT prototype efficiency is 1% better than the silicon MOSFET version. At light load, the efficiency difference becomes even larger.

VI. Conclusion

This paper introduces the characteristic and basic operation principle of 600 V cascode GaN HEMT. The device performance is compared and evaluated with the state-of-the-art silicon MOSFET. The loss analyses of the cascode GaN HEMT based on buck converter are presented. At hard-switching conditions, the turn-on loss dominates due to the reverse recovery charge and junction capacitor charge impact. However, the turn-off loss is negligible due to the intrinsic current source driving mechanism. This characteristic makes the cascode GaN HEMT very suitable for high-frequency operation as long as ZVS turn on is achieved. A 1 MHz 300 W 400 V/12 V LLC converter validates the advantages of the cascode GaN HEMT over the silicon MOSFET.

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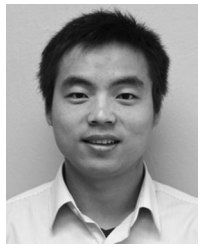

Xiucheng Huang (S'12) was born in Zhejiang, China, in 1986. He received the B.S. and M.S. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 2008 and 2011, respectively. He is currently working toward the Ph.D. degree at the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA.

His current research interests include high-frequency high power density power conversion, soft-switching technique and power architecture.

Zhengyang Liu (S'12) received the B.S. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2011. He is currently working toward the M.S. degree at the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA.

His current research interests include high-frequency power conversion techniques and wide bandgap power semiconductor devices.

Qiang Li (M'11) received the B.S. and M.S. degrees in power electronics from Zhejiang University, Hangzhou, China, in 2003 and 2006, respectively, and the Ph.D. degree from Virginia Tech, Blacksburg, VA, USA, in 2011.

He is currently an Assistant Professor at the Center for Power Electronics Systems, Virginia Tech. His current research interests include high-density electronics packaging and integration, high-frequency magnetic components, and high-frequency power conversion.

Fred C. Lee (S'72–M'74–SM'87–F'90–LF'12) received the B.S. degree in electrical engineering from the National Cheng Kung University, Tainan, Taiwan, in 1968, and the M.S. and Ph.D. degrees in electrical engineering from Duke University, Durham, NC, USA, in 1972 and 1974, respectively.

He is currently a University Distinguished Professor at Virginia Tech, Blacksburg, VA, USA, and the Director of the Center for Power Electronics Systems (CPES), a National Science Foundation Engineering Research Center (NSF ERC) established in 1998, with four university partners—University of Wisconsin-Madison, Rensselaer Polytechnic Institute, North Carolina A&T State University, and University of Puerto Rico-Mayagüez—and more than 80 industry members. The center's vision is "to provide leadership through global collaboration to create electric power processing systems of the highest value to society." Over the ten-year NSF ERC Program, CPES has been cited as a model ERC for its industrial collaboration and technology transfer, as well as education and outreach programs. His current research interests include high-frequency power conversion, distributed power systems, renewable energy, power quality, high-density electronics packaging and integration, and modeling and control. He holds 69 U.S. patents and has authored and coauthored 238 journal articles and more than 596 refereed technical papers. During his tenure at Virginia Tech, he has supervised to completion 71 Ph.D. and 80 Master's students.

Dr. Lee received the William E. Newell Power Electronics Award in 1989, the Arthur E. Fury Award for Leadership and Innovation in Advancing Power Electronic Systems Technology in 1998, and the Ernst-Blickle Award for achievement in the field of power electronics in 2005. He has served as the President of the IEEE Power Electronics Society (1993–1994). He was named to the National Academy of Engineering in 2011.