

A GaN Pulse Width Modulation Integrated Circuit for GaN Power Converters

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Abstract—We report the first gallium nitride (GaN)-based pulse width modulation (PWM) integrated circuit (IC) featuring monolithically integrated enhancement- and depletion-mode high electron mobility transistors and lateral field-effect rectifiers on the GaN smart power technology platform. The PWM IC is able to generate 1-MHz PWM signal with its duty cycle modulated effectively by a reference voltage (V_c) over a wide range with good linearity. It features a 5 V supply voltage and is composed of a sawtooth generator and a comparator, both of which can be operated at 1 MHz and exhibit proper functionality over a wide temperature range (from 25 °C to 250 °C). This circuit demonstration further proves the feasibility of an all-GaN solution that features monolithically integrated peripheral gate control circuits and power switches for GaN power converters. An all-GaN solution would lead to a compact system with improved efficiency and enhanced reliability.

Index Terms—All-gallium nitride (GaN) solution, GaN, gate driver, integrated circuit (IC), pulse width modulation (PWM).

I. INTRODUCTION

OWING to their capability for high-power, high-frequency, and high-temperature operations [1], [2], gallium nitride (GaN)-based power switches and rectifiers have emerged as promising candidates for next-generation power electronic applications that demand highly efficient and compact power converters. GaN power switches have been shown to offer a more efficient and compact solution for power conversion systems compared with their Si-based counterparts [3]–[7]. However, all the reported demonstrations use Si-based gate drive integrated circuits (ICs) to control discrete GaN power switches, due to the lack of GaN-based mixed-signal control circuits. Such hybrid gate drive schemes are larger in size than on-chip gate drive scheme and the requirements placed on packaging the gate driver chip and the power chip could be stringent due to high sensitivity of parasitics when GaN power devices are switched at high frequencies [8]. In contrast, an integrated GaN-based gate

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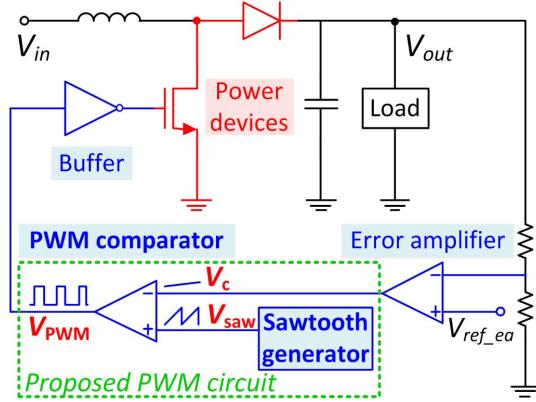


Fig. 1. Block diagram of a typical voltage-mode PWM boost converter. The proposed GaN-based PWM circuit is outlined in green dash.

driver could deliver better system performance with suppressed parasitics, faster operation speed, as well as high-temperature operation capabilities. Therefore, an all-GaN solution featuring monolithically integrated power devices and peripheral control circuits is highly desirable to fully exploit the superior performance offered by GaN devices.

Widely adopted in power converter (e.g., switched-mode power supplies) gate drivers, pulse width modulation (PWM) circuit is of particular importance to the gate control ICs given their essential role of controlling the power switch duty cycles and regulating the converter output voltages. Fig. 1 shows the block diagram of a typical voltage-mode PWM boost converter. The PWM signal (V_{PWM}) is generated by comparing the reference voltage (V_c) sampled from the converter output against a fixed sawtooth signal (V_{saw}). Then, the PWM signal goes through a buffer stage [9], which provides the driving capability as well as proper output voltage levels to turn the power switch ON and OFF.

In this paper, we demonstrate the first GaN-based PWM circuit using monolithically integrated enhancement- and depletion-mode (E/D-mode) high electron mobility transistors (HEMTs) and lateral field-effect rectifiers (L-FERs) [10]. The circuit is able to generate 1-MHz PWM signal with its duty cycle modulated linearly over a wide range. This paper augments and refines the work first presented in [11] from both the theoretical analysis and measurement results of the GaN-based PWM IC. It is organized as follows. The fabrication process and device characteristics are provided in Section II. Design and characterization of the PWM IC is presented and discussed in Sections III and IV. In Section V, we conclude this paper.

II. DEVICE FABRICATION AND CHARACTERISTICS

With a 2-D electron gas (2DEG) channel of high electron density and mobility, the *lateral* AlGaN/GaN heterojunctions grown on low cost and highly scalable silicon substrates provide a technology platform that is particularly suitable for monolithic integration of low-voltage-rated peripheral control circuits and high-voltage-rated power components [12]. On this platform, various GaN-based sensing/control/protection functional blocks [13]–[15] have been developed to address various application-related issues for enhanced device reliability and improved circuit functionalities.

In this paper, we focus on developing GaN-based PWM circuit that can be monolithically integrated with GaN power switching devices. Such a monolithic integration scheme is expected to lead to significantly reduced parasitics and lower packaging costs compared with the hybrid gate drive solutions using traditional Si-based gate drive ICs.

A. Fabrication Process

The GaN circuits were fabricated on a commercially available GaN-on-Si (111) HEMT sample featuring a 1.8- μm GaN buffer and 20-nm barrier layer (including 1-nm AlN, 17-nm AlGaN, and 2-nm GaN cap). The fabrication process started with source/drain ohmic contact formation using electron-beam evaporated Ti/Al/Ni/Au metal stack with subsequent rapid thermal annealing at 850 °C for 30 s. Then, 50-nm SiN_x was deposited as the passivation layer by plasma enhanced chemical vapor deposition. After that, planar isolation using multienergy F ion implantation [16] was conducted. Then, the fluorine plasma ion implantation technique [17], [18] was used to convert D-mode channels into E-mode ones for realizing E-mode HEMTs and L-FERs. Subsequently, gate metallization was carried out by E-beam evaporation of Ni/Au.

B. Device Characteristics

The dc output and transfer characteristics of the monitoring devices fabricated on the same chip with the GaN ICs are shown in Fig. 2. The threshold voltage is -1.8 V for D-mode HEMT and $+1.0$ V for E-mode HEMT at room temperature, using linear extraction method (at $V_{DS} = 10$ V). The maximum current density is 340 mA/mm (at $V_{GS} = 3$ V) in the E-mode HEMT and 325 mA/mm (at $V_{GS} = 0$ V) in the D-mode HEMT. The L-FER, which is essentially a HEMT-compatible diode [10], shows a forward conduction current I_D of 300 mA/mm at a forward voltage of 3 V at room temperature [Fig. 2(c)].

III. GaN PWM IC DESIGN

The GaN-based pulse width modulator incorporates two functional blocks, i.e., a sawtooth generator and a comparator, as shown in Fig. 3. The sawtooth generator produces a sawtooth signal (V_{saw}) and the comparator (referred to as the PWM comparator) produces the PWM signal (V_{PWM}) by comparing the reference voltage (V_r) sampled from

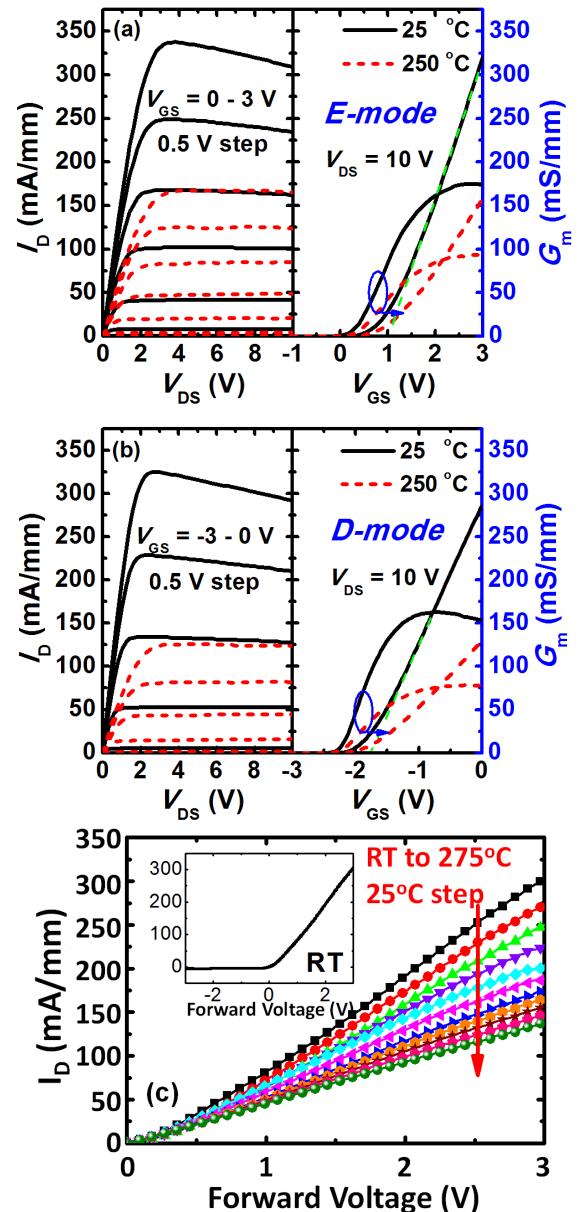


Fig. 2. Output ($I_D - V_{DS}$) and transfer ($I_D - V_{GS}$) characteristics of (a) E-mode HEMT, (b) D-mode HEMT, and (c) L-FER.

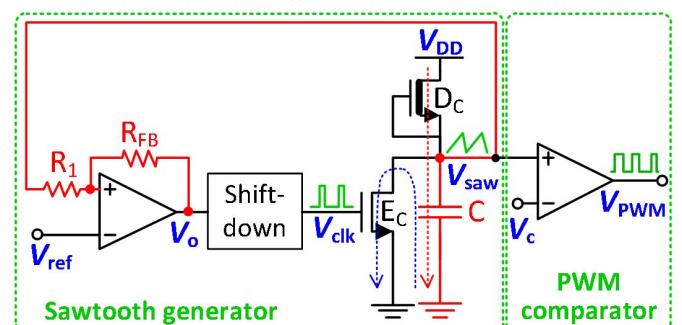


Fig. 3. Block diagram of the GaN-based PWM IC. Three off-chip passive components are used (marked in red line) for the sawtooth generator. V_c is the reference voltage sampled from the converter output.

the converter output against the sawtooth signal (V_{saw}). The pulse width of V_{PWM} is modulated by V_c , and its frequency is determined by that of V_{saw} .

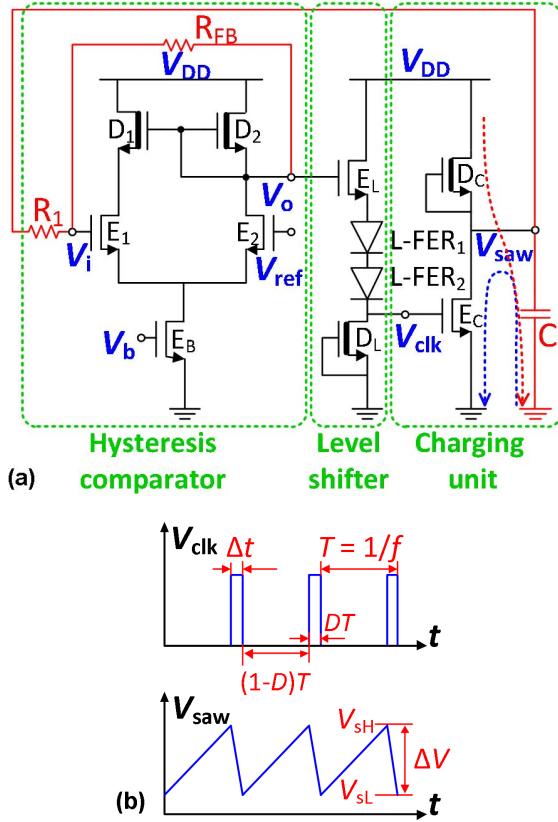


Fig. 4. (a) Circuit schematic and (b) theoretical output waveforms of the GaN sawtooth generator. The red dashed arrow shows the charging path for capacitor C and the blue dashed arrow indicates the discharging path.

A. Sawtooth Generator

As shown in Fig. 4, the sawtooth generator is a three-stage functional block composed of a hysteresis comparator, a step-down level shifter and a charging unit. The sawtooth signal is generated by charging and discharging the off-chip capacitor (C), whereas the control signal of this periodically repetitive process is essentially provided by the hysteresis comparator. The level shifter in the second stage is inserted to shift the first-stage output to lower levels that can be accommodated at the third-stage input, because of the limited gate voltage swing of the E-mode Schottky-gate HEMT.

One complete cycle of V_{saw} consists of two stages, i.e., the ramp-up stage and the ramp-down stage [Fig. 4(b)]. During the ramp-up, the reset switch E_C is OFF and the capacitor C is charged by a charging current (I_{ch}) sourced by the D-mode current source D_C until V_{saw} reaches the high switching threshold (V_{TH}) of the hysteresis comparator, at which point the comparator toggles to logic high output state (V_{OH}) and turns ON E_C . In consequence, V_{saw} starts to drop as C discharges through E_C with a discharging current I_{dis} . The ramp-down stage ends when V_{saw} reaches the low switching threshold (V_{TL}) of the hysteresis comparator. Then, the comparator toggles again (to V_{OL}) and turns OFF E_C as a result. Accordingly, the capacitor starts to charge again, marking the beginning of another cycle. At steady state, the circuit oscillates at frequency f and generates a sawtooth signal with amplitude of ΔV .

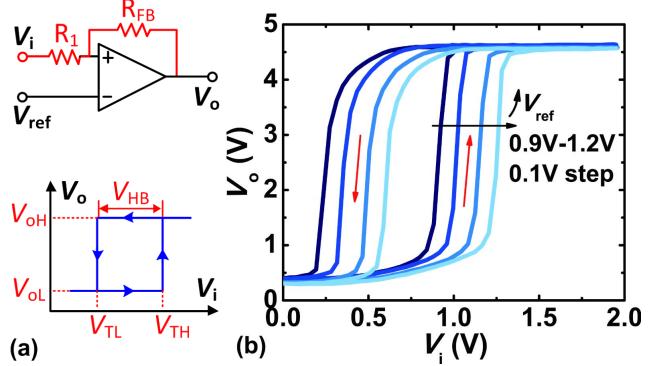


Fig. 5. (a) Circuit configuration and parameter definition of the hysteresis comparator. (b) VTC measured with $R_1/R_{FB} = 10/47 \text{ k}\Omega$. The switching thresholds can be shifted by tuning V_{ref} .

1) *Hysteresis Comparator and ΔV* : The two switching thresholds (i.e., V_{TL} and V_{TH}) of the hysteresis comparator can be derived with

$$\begin{aligned} V_{TH} &= (1 + R_1/R_{FB})V_{ref} - (R_1/R_{FB})V_{oL} \\ V_{TL} &= (1 + R_1/R_{FB})V_{ref} - (R_1/R_{FB})V_{oH} \\ V_{HB} &= V_{TH} - V_{TL} = (R_1/R_{FB})(V_{oH} - V_{oL}). \end{aligned} \quad (1)$$

The window between V_{TH} and V_{TL} represents the amount of hysteresis, and is denoted as the hysteresis band V_{HB} [Fig. 5(a)]. The switching thresholds depend on both the resistance ratio R_1/R_{FB} and the reference voltage V_{ref} , whereas the hysteresis band is determined merely by R_1/R_{FB} ratio for a given comparator output swing (i.e., $V_{oH} - V_{oL}$). The voltage transfer characteristics (VTC) of the hysteresis comparator [Fig. 5(b)] shows that V_{TH} and V_{TL} can be shifted toward the same direction by changing V_{ref} , whereas V_{HB} is independent of it.

The amplitude (ΔV) of the sawtooth signal can be expressed as

$$\Delta V = V_{sH} - V_{sL} = V_{TH} - V_{TL} = V_{HB} \quad (2)$$

where ΔV is the same as the hysteresis band of the comparator, which is mainly controlled by R_1/R_{FB} ratio. It should be noted that ΔV is under the influence of the comparator output swing as well, which may vary with different loadings and supply voltages.

The lower (V_{sL}) and upper (V_{sH}) limit of V_{saw} are set by the comparator switching thresholds (V_{TL} and V_{TH} , respectively). The sawtooth signal can be shifted up and down by tuning V_{ref} .

2) *Charging Unit and f* : The frequency (f) of V_{saw} can be linearly approximated from $I_C = C\Delta V/\Delta t$, where I_C is the average charging or discharging current and Δt is the corresponding time duration. From above relationship, f can be expressed as

$$f = (I_{dis}D)/(C\Delta V) = [I_{ch}(1 - D)]/(C\Delta V) \quad (3)$$

$$\begin{aligned} I_{dis}DT &= I_{ch}(1 - D)T \\ D &= I_{ch}/(I_{ch} + I_{dis}). \end{aligned} \quad (4)$$

From (3), smaller capacitance (C) is preferred to achieve larger f for given amplitude ΔV (Fig. 6). In addition, larger

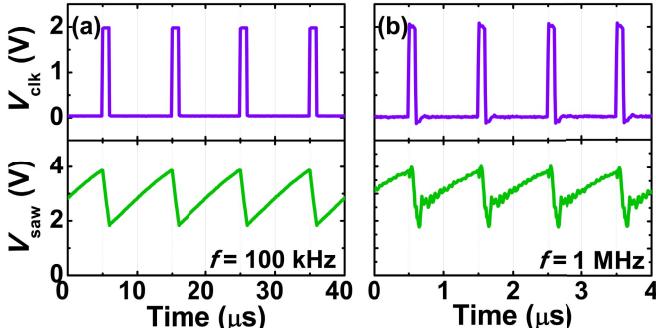


Fig. 6. Input (V_{clk}) and output (V_{saw}) waveforms of the charging unit. The input signals (0–2 V square wave) are generated by the function generator. The frequency of the sawtooth signal can be increased using smaller capacitor. (a) $f = 100$ kHz and $C = 4.6$ nF. (b) $f = 1$ MHz and $C = 460$ pF.

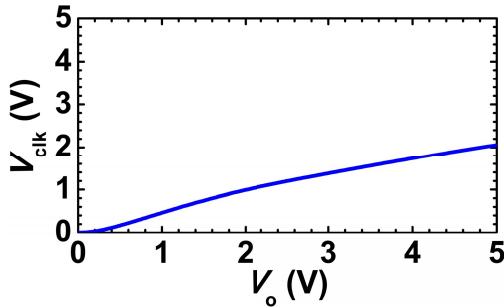


Fig. 7. VTC (input— V_o and output— V_{clk}) of the level shifter (second stage). Voltage as high as 5 V (output of the first stage) can be down shifted to around 2 V, which is safe enough for the E-mode HEMT E_C in the third stage.

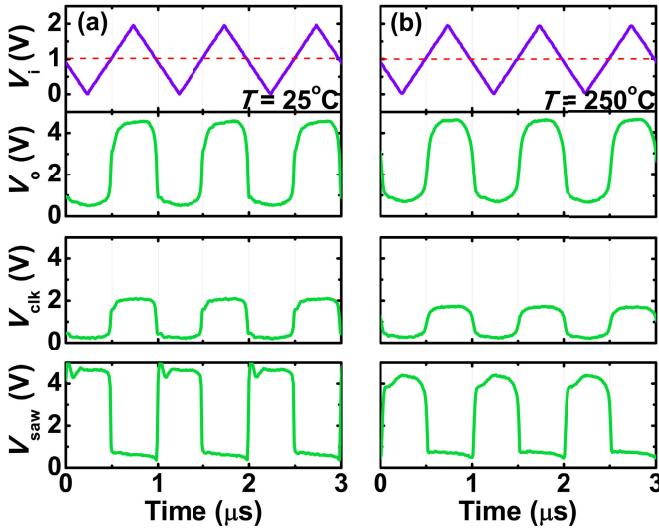


Fig. 8. Open-loop ac performance of the GaN sawtooth generator at $f = 1$ MHz. $V_{\text{DD}} = 5$ V and $V_{\text{ref}} = 1$ V (red dashed line). V_i is the input signal, V_o , V_{clk} , and V_{saw} are the output signals of the three stages, respectively. (a) $T =$ room temperature. (b) $T = 250^\circ\text{C}$. The third stage is essentially a direct coupled FEL logic inverter without the off-chip capacitor.

charging (and discharging) current would help speed up the ramp-up (and -down) process of V_{saw} , leading to larger f . Meanwhile, V_{saw} would exhibit good linearity if the charging (and discharging) current is constant.

The duty cycle (D) of the sawtooth signal is defined as the percentage over one period when reset switch E_C is ON. According to (4), D is governed by current ratio $I_{\text{ch}}/I_{\text{dis}}$. Specific duty cycle of the sawtooth signal can be achieved by

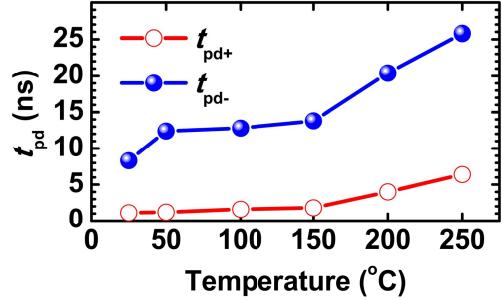


Fig. 9. Open-loop circuit propagation delay of the three-stage sawtooth generator (from input V_i to third-stage output V_{saw}) up to 250 °C.

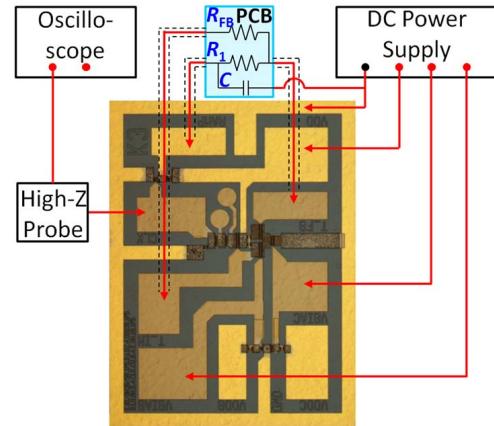


Fig. 10. Closed-loop measurement setup of the GaN sawtooth generator. SMD resistors and capacitor are soldered onto a PCB and connected to the chip with ac probes. High-impedance probe is used to monitor the output waveforms.

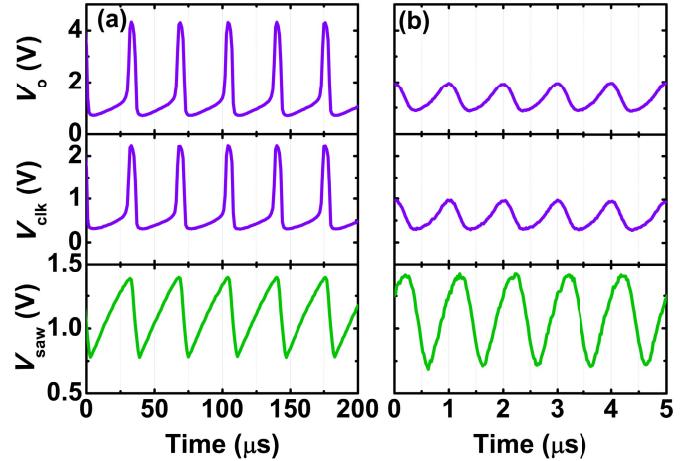


Fig. 11. Closed-loop waveforms of the sawtooth generator, $V_{\text{DD}} = 5$ V. (a) $f = 28$ kHz, $R_1/R_{\text{FB}} = 10/47$ kΩ, and $C = 46$ nF. (b) $f = 1$ MHz, $R_1/R_{\text{FB}} = 1/4.7$ kΩ, and $C = 460$ pF.

designing the device dimensions [width/length (W/L) ratio] of E_C and D_C . It should be noted that D can also be affected by the voltage level of comparator output because that the gate voltage applied on E_C during its ON-state can also modulate I_{dis} .

3) *Level Shifter*: The output voltage of the hysteresis comparator can be as high as close to the 5 V supply voltage, which could cause undesirable device degradation [19] if

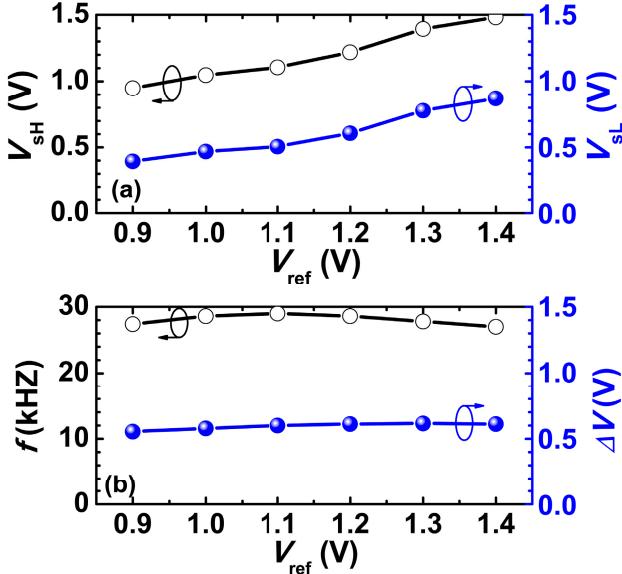


Fig. 12. Shifting V_{saw} up and down by tuning V_{ref} . $f = 28$ kHz and $V_{DD} = 5$ V. (a) Top (V_{sh}) and bottom (V_{sl}) limit of V_{saw} versus V_{ref} . (b) Amplitude and frequency of V_{saw} versus V_{ref} .

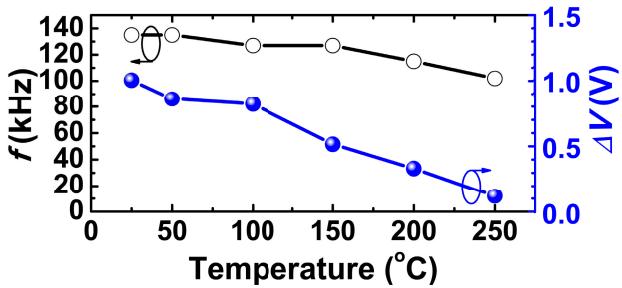


Fig. 13. High-temperature performance of GaN sawtooth generator. $R_1/R_{FB} = 10/47$ k Ω , $C = 4.7$ nF, and $f = 135$ kHz at RT.

directly fed to the Schottky-gate E-mode HEMT (E_C) in the third stage. The level shifter, configured in the form of the source follower with two additional L-FERs (to further reduce the output voltage levels), acts as the interface between the hysteresis comparator and the charging unit by shifting the comparator output voltage into lower levels that is safe enough for E_C (Fig. 7).

B. PWM Comparator

The PWM comparator is a bootstrapped comparator [14]. With the generated sawtooth signal (V_{saw}) and the reference voltage (V_c) sampled from the converter output connected to its two input terminals, the PWM comparator is able to produce a PWM signal (V_{PWM}) at its output (Fig. 3).

IV. MEASUREMENT RESULTS AND DISCUSSION

A. Sawtooth Generator

1) Open-Loop Circuit Performance: With all off-chip passive components disconnected to the circuit, the on-wafer test of the open loop GaN sawtooth generator was conducted first to characterize its inherent circuit performance.

Fig. 8 shows the open-loop ac performance of the sawtooth generator. The input signal (V_i) is generated from a function

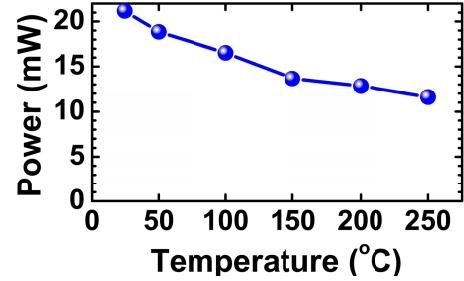


Fig. 14. Power consumption of the sawtooth generator versus temperature.

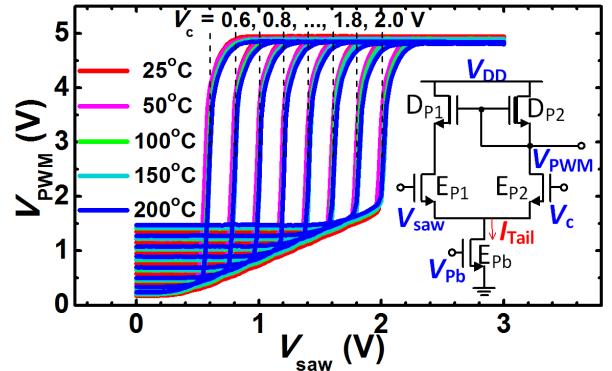


Fig. 15. VTC of PWM comparator configured in noninverting mode. Inset: circuit schematic of the PWM comparator.

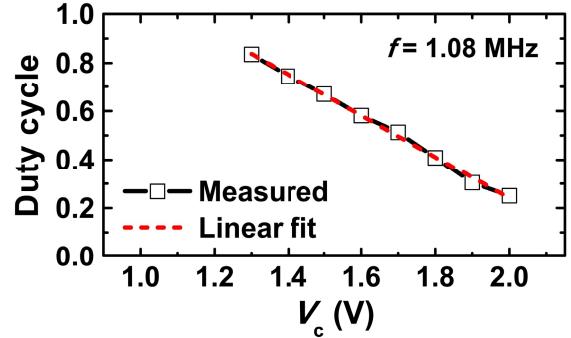


Fig. 16. Duty cycle modulation of the PWM circuit operated at ~ 1.08 MHz.

generator, and the output signals are measured with a high-impedance active probe with 0.1-pF input capacitance and 10-M Ω input resistance. The supply voltage (V_{DD}) is 5 V and the reference voltage (V_{ref}) is set to be 1 V. All the three stages (i.e., V_o , V_{clk} , and V_{saw}) exhibit good operations at 1 MHz from room temperature to 250 °C. The sharp rising and falling edges of the output signals indicate that the circuit can be operated well above 1 MHz.

The three-stage sawtooth generator features a propagation delay of 1.1 and 8.3 ns at rising and falling edge (Fig. 9), respectively, at room temperature, indicating an intrinsic speed limit far beyond 1 MHz. This propagation delay is smaller than most of the Si-based comparators, even including some of the ones specially designed for high-speed applications [20]–[22].

The larger delay at high temperatures is attributed to the decreased drain current in GaN HEMTs due to 2DEG mobility

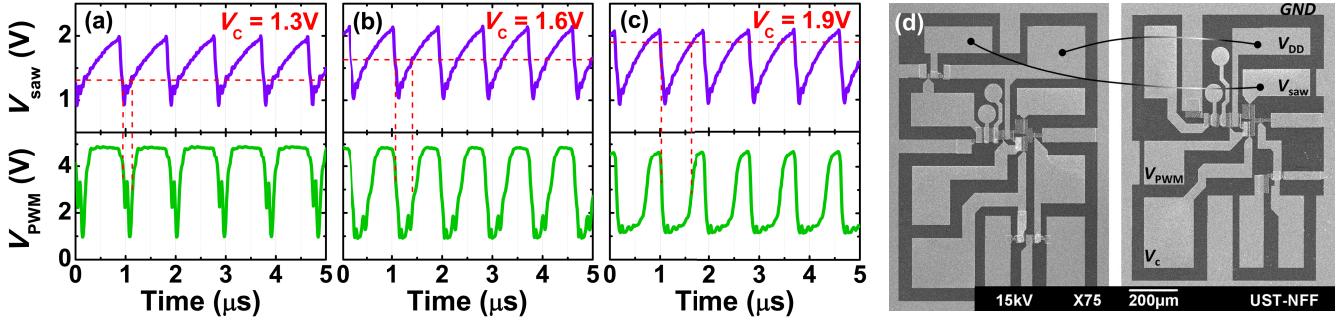


Fig. 17. Waveforms of GaN PWM circuit, $V_{DD} = 5$ V and $I_{DD} \sim 5$ mA. V_c (red dashed line) cuts V_{saw} ($f \sim 1.08$ MHz and $V_{saw} \sim 0.89$ V–2.18 V) and determines the duty cycle of V_{PWM} . (a) $V_c = 1.3$ V, (b) $V_c = 1.6$ V, (c) $V_c = 1.9$ V, and (d) scanning electron microscope picture of the adjacent dies (left—sawtooth generator and right—PWM comparator). The GaN-on-Si chip is wire-bonded and mounted onto a PCB which also houses three off-chip passive components.

degradation [23]. Nevertheless, the propagation delay is small enough for 1-MHz operations even at 250 °C.

The unsymmetrical delay time at rising (t_{pd+}) and falling (t_{pd-}) edges is the result of the different device dimensions of the two HEMTs D_C (W/L = 8/5 μ m) and E_C (W/L = 40/1.5) in the third stage, which leads to various charging and discharging speed for the same capacitive load.

2) Closed-Loop Circuit Characteristic: Closed-loop measurements are conducted with three off-chip passive components connected to the GaN chip, as shown in Fig. 10. The generated sawtooth waveforms under 5 V V_{DD} and 1.3 V V_{ref} are shown in Fig. 11. With an R_1/R_{FB} ratio of 10/47 k Ω and C of 46 nF, the circuit is able to oscillate at 28 kHz and generates a sawtooth signal with amplitude of ~0.62 V. According to (1) and (2), ΔV is calculated to be 0.7 V (from 0.7 to 1.4 V). A good agreement has been obtained between experiment and calculation.

With a smaller capacitance of 460 pF, the oscillating frequency is increased to 1 MHz. It should be noted that the resistors are also scaled to 1 /4.7 k Ω since larger resistances in the loop could prolong the propagation delay significantly and limit the oscillation frequency to less than 1 MHz. The smaller swing of the comparator output (V_o) at 1 MHz is caused by the larger loading effect as the penalty of adopting smaller feedback resistors, as well as the noticeably reduced slew rate (SR) due to large input capacitance of the passive ac probes. Nevertheless, it is still large enough to switch E_C ON and OFF, and consequently, the sawtooth signal can be generated.

The sawtooth signal can be shifted up and down by tuning V_{ref} [Fig. 12(a)], whereas its amplitude and frequency are hardly affected by V_{ref} [Fig. 12(b)]. Fig. 13 shows the high-temperature characteristics of the sawtooth generator. Both the frequency and amplitude of V_{saw} are smaller at elevated temperatures. This is because of the reduced ON-state current in E/D-mode HEMTs at high temperatures. This current degradation slows down the charging (and discharging) process of capacitor C and worsens the loading effect, leading to lower frequency, and smaller amplitude. The power consumption of the sawtooth generator is about 20 mW at room temperature, and becomes lower as the temperature increases (Fig. 14).

B. PWM Comparator Characteristics

The PWM comparator configured in noninverting mode exhibits dc transfer characteristics shown in Fig. 15. Proper ac operations have been obtained at frequencies well above 1 MHz from room temperature to 250 °C [14].

C. Pulse Width Modulator Performance

To test the GaN PWM circuit, adjacent GaN sawtooth generator and PWM comparator in the same die were wire-bonded on-chip. The GaN chip is mounted onto a printed circuit board (PCB) and connected to the off-chip resistors and capacitor.

Circuit performances up to 1 MHz are investigated with a 5 V supply voltage. The generated sawtooth signal (V_{saw}) is injected into the PWM comparator and compared against V_c , yielding a PWM signal with its duty cycle modulated by V_c . Fig. 17 shows the PWM waveforms when the circuit is operated at ~1.08 MHz. The pulse width of the PWM signal can be modulated over a wide range (by varying V_c from 1.3 to 2.0 V with V_{saw} oscillating between 0.89 and 2.18 V), as shown in Fig. 16. It should be pointed out that present duty cycle range of the PWM circuit (0.25–0.85 at 1 MHz) is limited by the maximum SR of the PWM signal, which is proportional to the sinking current (i.e., I_{Tail} , current of E_{Pb}) (inset of Fig. 15) [24] of the PWM comparator. An even wider duty cycle range of the PWM signal can be achieved by optimizing the device dimensions of the PWM comparator (e.g., increase the W/L ratio of the E-mode current tail to provide a larger I_{Tail} , and therefore a higher SR) in future design. In addition, the linearity of sawtooth signals [Fig. 17(a)–(c)] could be further improved by optimizing device dimensions and circuit topologies of the sawtooth generator (e.g., increase the W/L ratio of devices in the hysteresis comparator and replace the D-mode HEMT in the charging unit with a more precise current source, so that I_{ch} and I_{dis} would be more close to constant) in the future. It should be noted that the testing frequency (1 MHz) is limited not by the GaN circuits, but by the input capacitance (1 pF) of the oscilloscope probes used in the measurement. The PCB implementation of the PWM circuit has limited the test at room temperature at present.

It is worth noticing that for practical applications of driving a typical GaN-based power switch, a buffer stage ought to

be further implemented (as shown in Fig. 1) on the GaN-based platform [9] to provide proper driving capability that well matches the requirements of the power device.

V. CONCLUSION

The first GaN-based PWM circuit featuring monolithically integrated E/D-mode HEMTs and rectifiers has been successfully demonstrated. Composed of a sawtooth generator and a PWM comparator, the circuit is able to generate 1-MHz PWM signal with its duty cycle modulated over a wide range. Both the sawtooth generator and the PWM comparator can operate properly at temperatures up to 250 °C. The frequency and amplitude of the generated sawtooth signal can be tuned flexibly by changing the off-chip capacitor and resistors. This PWM circuit could be monolithically integrated with GaN power switches with highly compatible fabrication processes to realize GaN power converters with compact size, reduced parasitics, and improved reliability.

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