Interleaved Parallel Inverter with Rectifier and DC supply

enes.ayaz.1996

October 2019

1 Introduction

IMMD structure gives a flexibility to connect modular inverter as series or parallel. Series inverter led us to use switching elements in lower voltage ratings. Parallel connection can be used in order to decrease DC Link capacitor stress by interleaving.
Carrier signals of parallel connected inverters are phase shifted with respect to each other.Thus, circulating currents is created and if the phase shift is 180 degree in ideal case (no parasitic and connection inductance and resistance) input current ripple decreases.The ripple of the input current is drawn by DC Bus Capacitor (in ideal case) and the DC Bus capacitor stresses decreases.
However, in our experimental data, we observed that DC Bus capacitor voltage ripple increases although input current ripples decreases. The results are not explained by using our simulation results. Only different thing is that 3-phase uncontrolled rectifier is used for DC Supply. This is a nonlinear elements and it gives some harmonics to inverter. Also, the ripple current can be drawn from rectifier not only DC Bus capacitor in the situation.

2 Analytical Solution of DC link Currents

Input current can be calculated by phases current and switching functions.

$$I_{dc} = S_A I_A + S_B I_B + S_C I_C$$

Also, switching functions can be analyzed by using Fourier expansion. Our signal are real and our switching functions can be shown by *cosine* expansion.
'Pulse Width Modulation for Power Converters: Principles and Practice' by Lipo explain the Fourier expansion for sinusoidal PWM. There are 2 requirements. One is carrier is triangular signal not saw tooth and the reference frequency is integer ratio of carrier frequency.
In addition, the switching function have some variables such as M modulation index, θ_o output phase, θ_c carrier phase, w_c carrier frequency and w_o output frequency.

$$
\begin{aligned}
&1 + M\cos(w_o + \theta_o) \\
&+(\tfrac{4}{pi})\textstyle\sum_{m=1}^{inf} J_o(\tfrac{mM\pi}{2}))sin(\tfrac{m\pi}{2})cos(m(w_c + \theta_c)) \\
&+(\tfrac{4}{pi})\textstyle\sum_{m=1}^{inf}\sum_{n=-inf}^{inf}(\tfrac{1}{m})J_n(\tfrac{mM\pi}{2}))sin(\tfrac{(m+n)\pi}{2})\ cos(m(w_c + \theta_c) + n(\theta_o + w_o))
\end{aligned}
$$

Can be seen as above, switching function is comprised of DC, fundamental, carrier and carrier harmonics and side band components.
"A General Analytical Method for Calculating Inverter DC-Link Current Harmonics' (journal) show that phase currents can be calculated by using load impedance and switching functions.

$$
\begin{bmatrix} I_A(w) \\ I_B(w) \\ I_C(w) \end{bmatrix} = \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \times \begin{bmatrix} S_A(w) \\ S_B(w) \\ S_C(w) \end{bmatrix}
$$

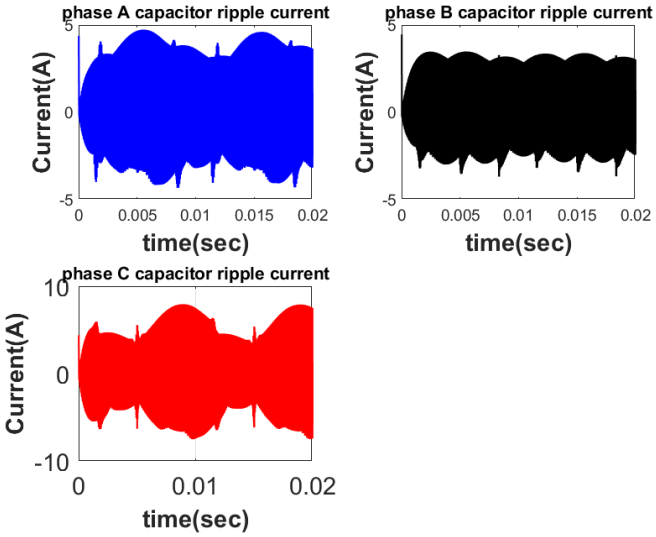
Thus, we can convolve the switching functions and phase currents in frequency domain in place of multiplying in time domain.
In addition, above current formula from switching functions shows that if the impedance is dominated by inductive load, the phase currents can be taken as only fundamental harmonics. Thus, phase current can be written as modulation index and load angle.

$$
\begin{bmatrix} I_A(w) \\ I_B(w) \\ I_C(w) \end{bmatrix} = \begin{bmatrix} \frac{V_{dc}}{|Z(w_f|}cos(w_f - \Theta_o - \Theta_load) \\ \frac{V_{dc}}{|Z(w_f|}cos(w_f - \Theta_o - \Theta_load - \frac{2\pi}{3}) \\ \frac{V_{dc}}{|Z(w_f|}cos(w_f - \Theta_o - \Theta_load + \frac{2\pi}{3}) \end{bmatrix}
$$

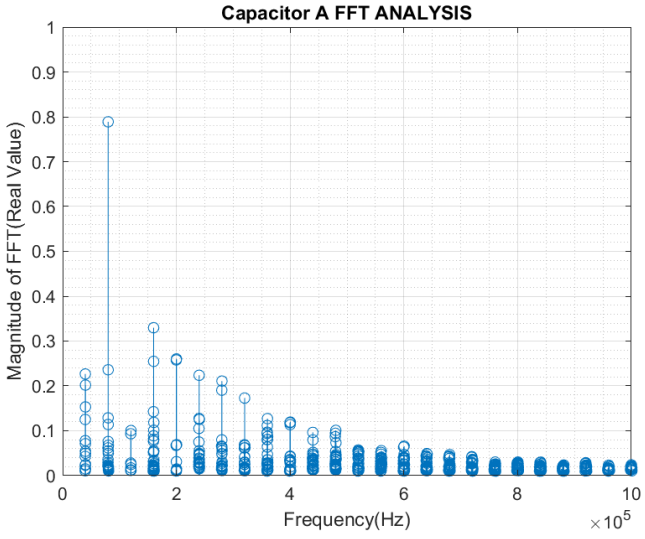
'Analysis and Calculation of DC-Link Current and Voltage Ripples for Three-Phase Inverter With Unbalanced Load' journal argue that ignoring and considering output high frequency current components by calculated the input current.

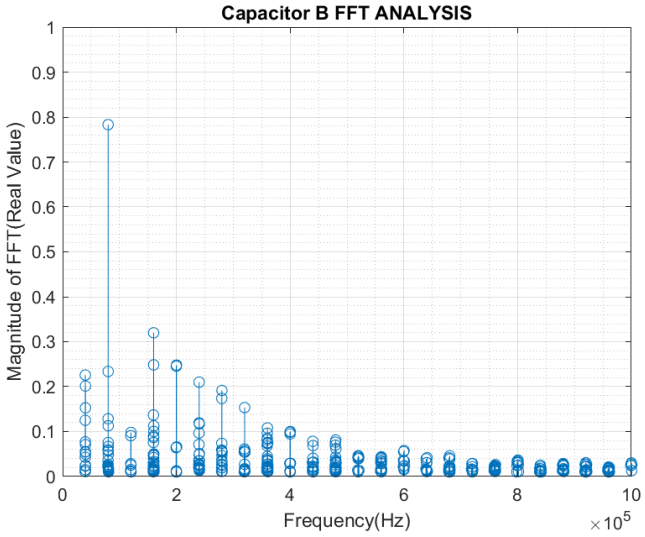
3 Simulink Simulation results for single module

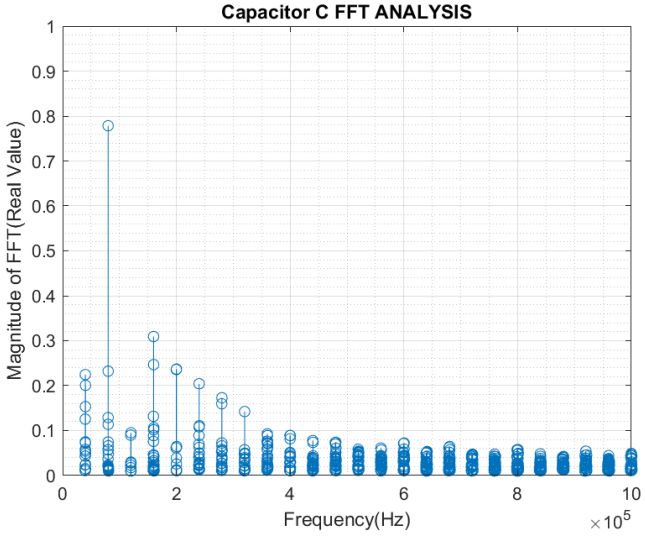
Model of 3-phase inverter with parasitic impedance is run and capacitor currents in time domain was loaded.



FFT of the capacitor currents were calculated.

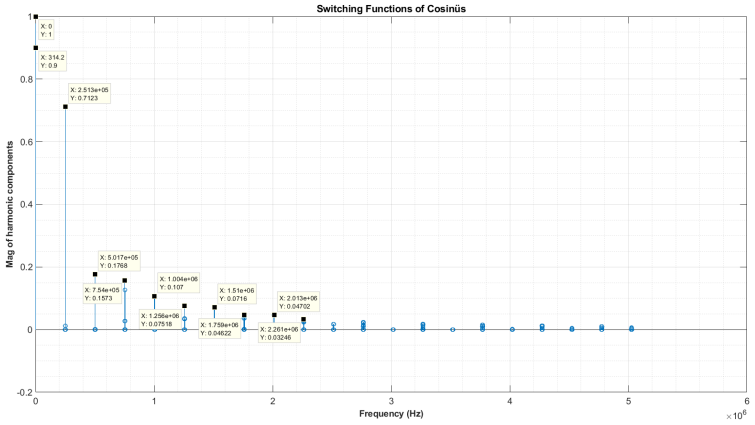


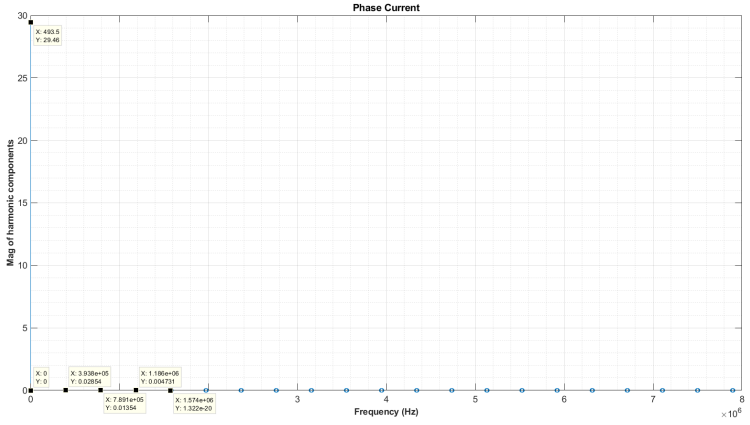

Capacitor B FFT ANALYSIS
Magnitude of FFT(Real Value)
Frequency(Hz)
×10^5

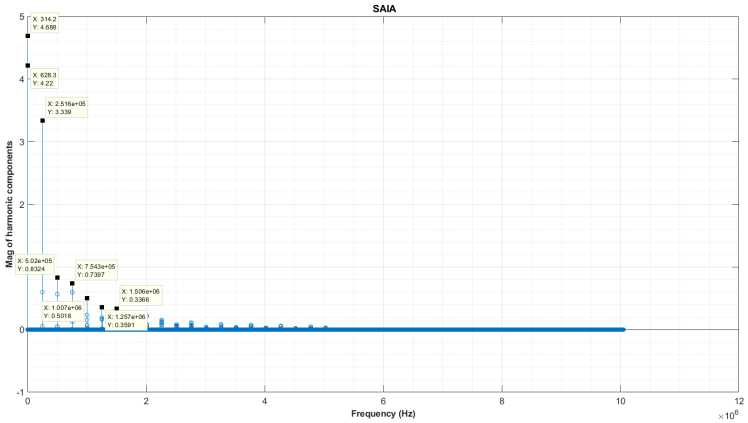

Capacitor C FFT ANALYSIS
Magnitude of FFT(Real Value)
Frequency(Hz)
×10^5

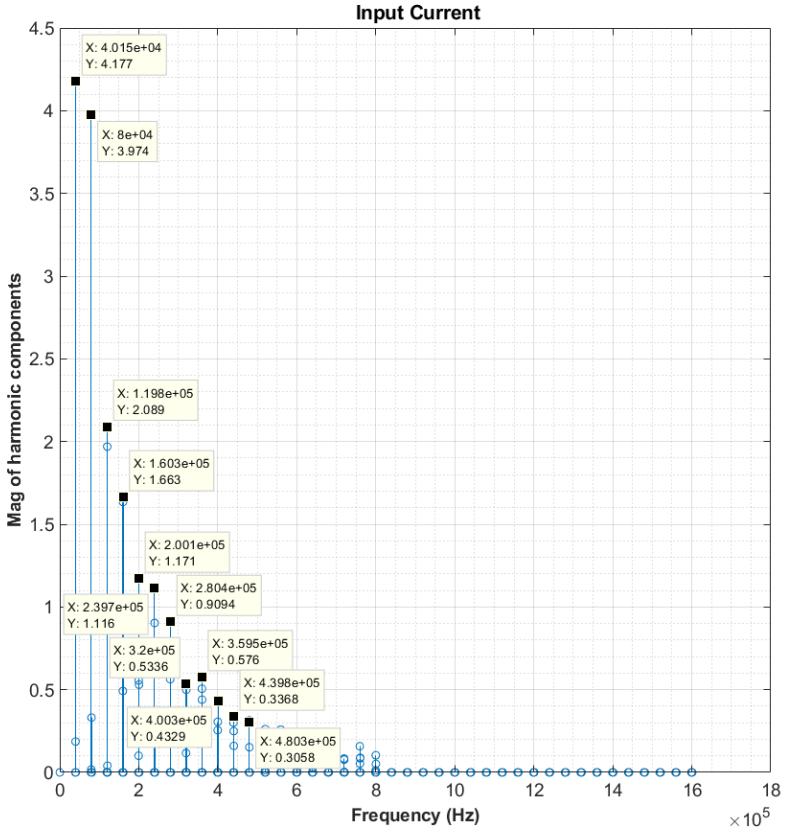
4 Analytical Solution for single module

Single module analytical module can be modeled by using switching functions. Switching functions can be expended in cosines signals. Then, phase currents is calculated by using them. After that point input current of each phase and total input current is calculated by using convolution.



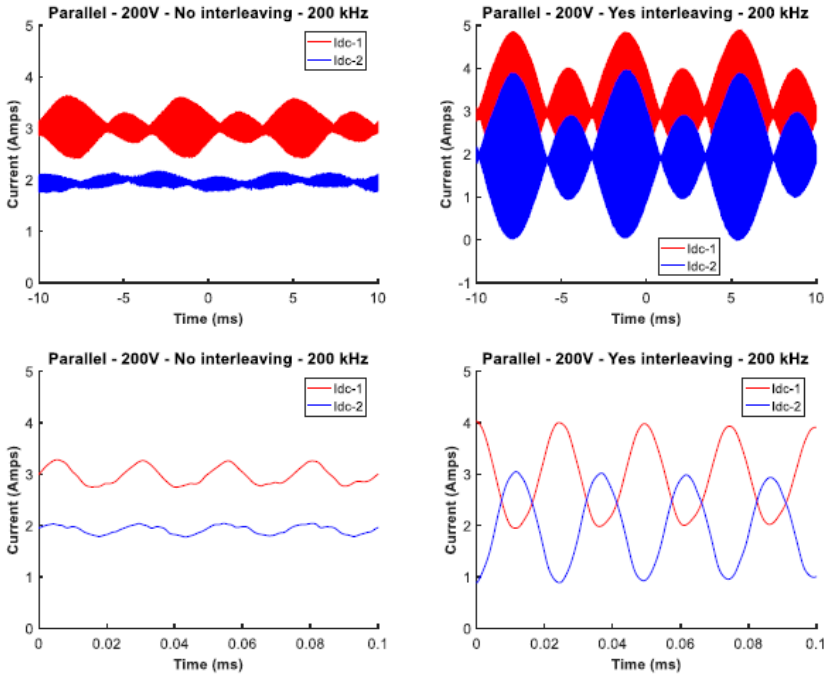



SAIA
Mag of harmonic components
Frequency (Hz)
×10^6

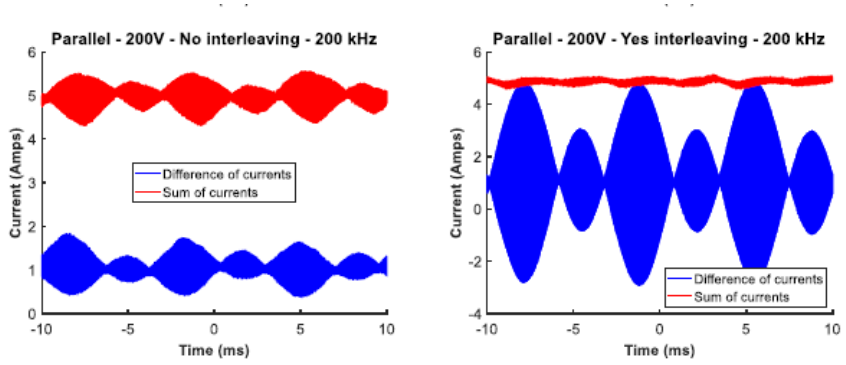

Input Current
Mag of harmonic components
Frequency (Hz)
×10^5
X: 4.015e+04
Y: 4.177
X: 8e+04
Y: 3.974
X: 1.198e+05
Y: 2.089
X: 1.603e+05
Y: 1.663
X: 2.001e+05
Y: 1.171
X: 2.804e+05
Y: 0.9094
X: 2.397e+05
Y: 1.116
X: 3.2e+05
Y: 0.5336
X: 3.595e+05
Y: 0.576
X: 4.398e+05
Y: 0.3368
X: 4.003e+05
Y: 0.4329
X: 4.803e+05
Y: 0.3058

5 Experimental Result

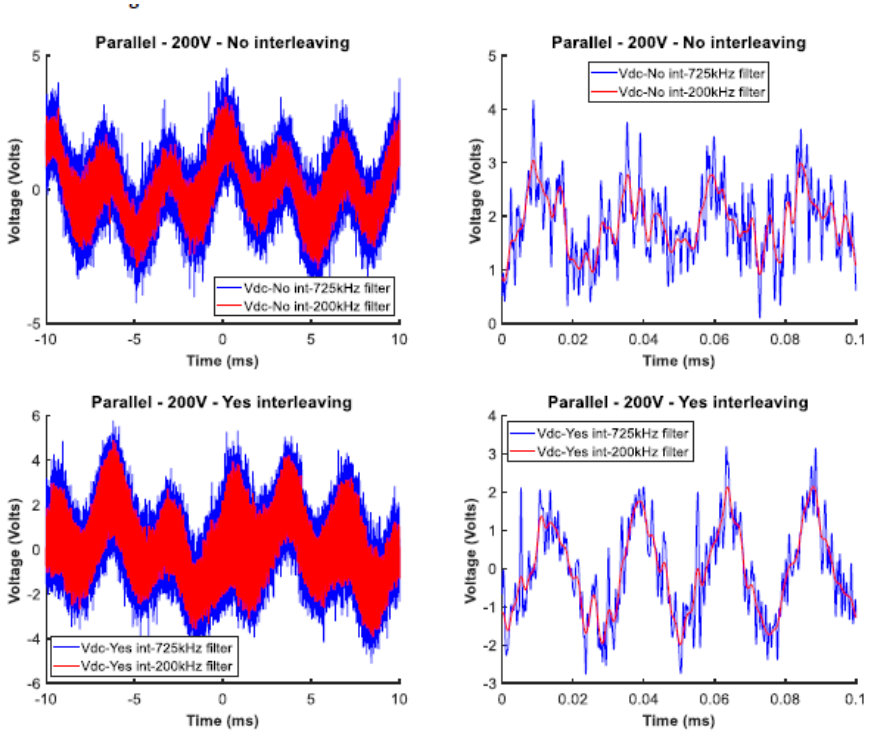
Two module paralleled inverters were tested. The module currents, input current with current probe and with shunt resistance, input voltage were measured. It is expected that interleaving does not improve the current ripples of the modules. It improves only the input current. It creates a circulating current in modules. Thus, the current of two modules can be divided in two part as sum and difference of the currents. Sum of the current must be improved in a manner of ripple and it decreases the DC-Bus stress. Also, we can think that all current ripple is drawn from capacitor and voltage of capacitor should be improved in a manner of ripple at ideal case. In addition, interleaving increases the difference of currents (or circulating current).



Module currents are shown.



Sum and difference of the module currents represent input and circulating current.



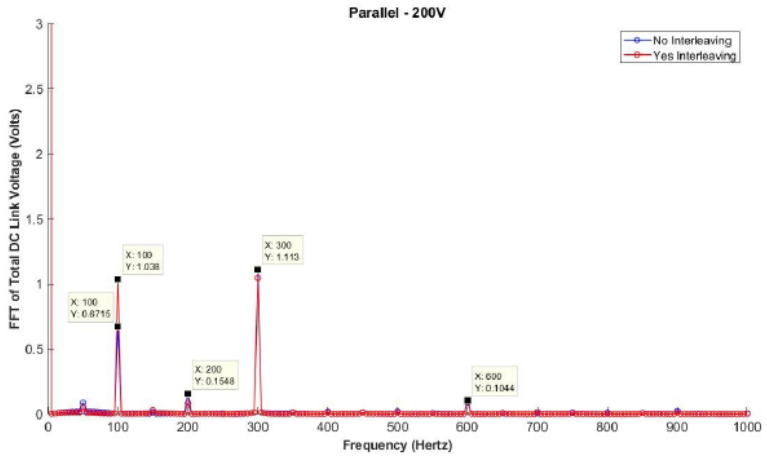
Voltage of DC-Bus capacitor.

5.1 Warning:

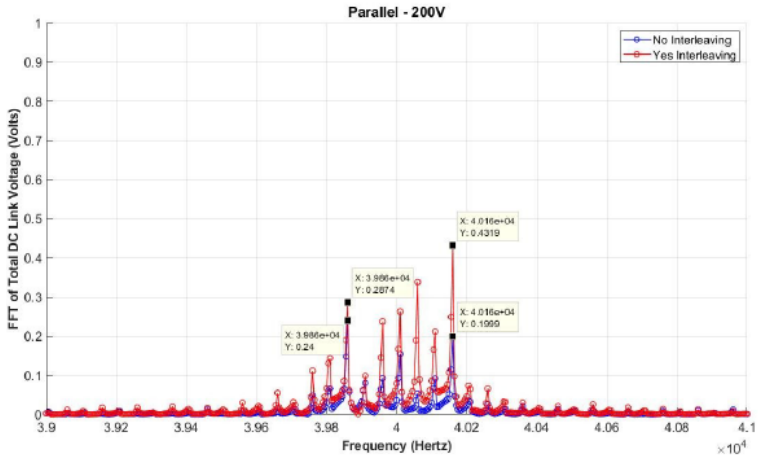
Input current or sum of the module currents decreases but voltage of DC-Bus increases. Why?? Interleaving gives a benefit or not? Do we decreases the stress of DC-Bus capacitor??

6 FFT results of Experiment

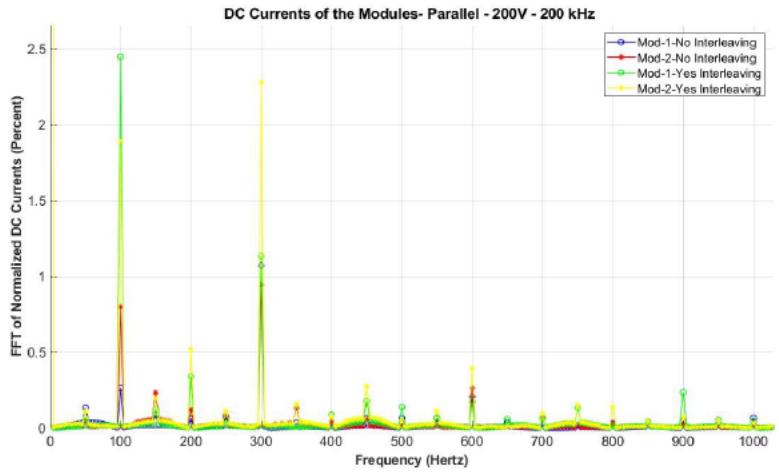
FFT analysis of experimental data show that interleaving makes 100Hz and 300 Hz and multiplies harmonics worse. Although 100 Hz is related to unbalanced situation, source of 300Hz and multiplies are not known.



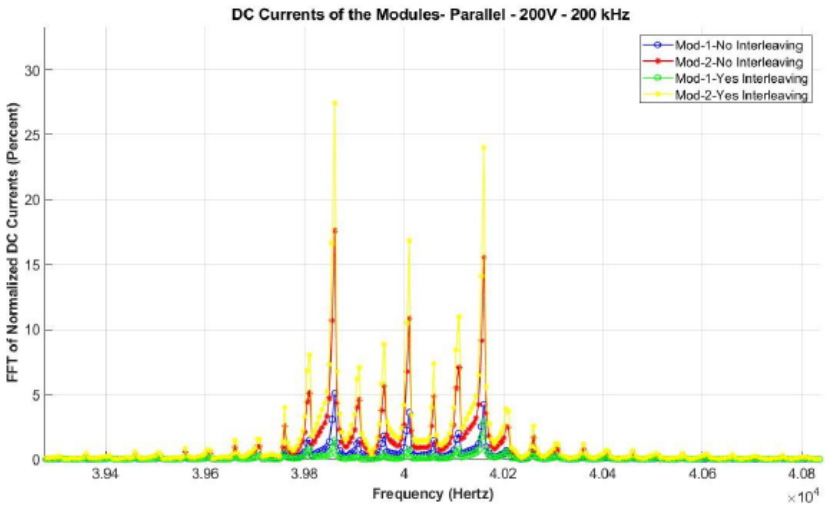
DC Voltage FFT analysis (Zoom in below 1 kHz)



DC Voltage FFT analysis (Zoom in range of 40kHz)



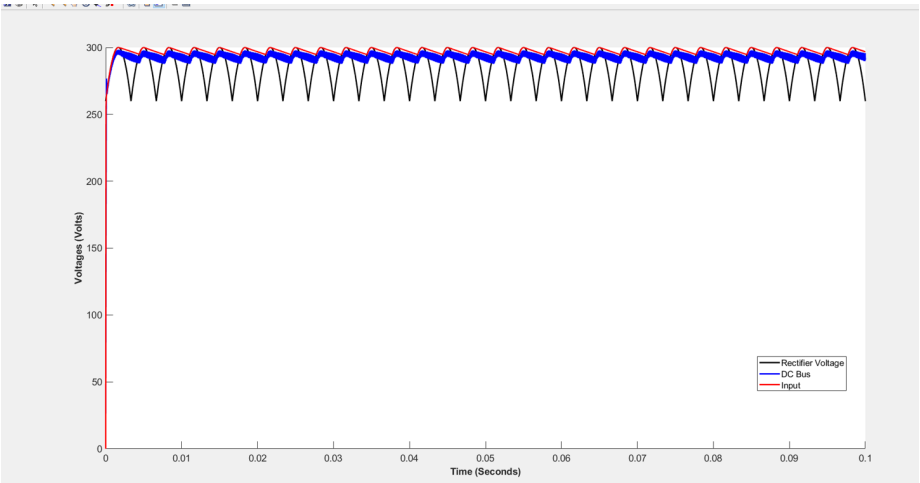
Modules current FFT analysis (Zoom in below 1 kHz)



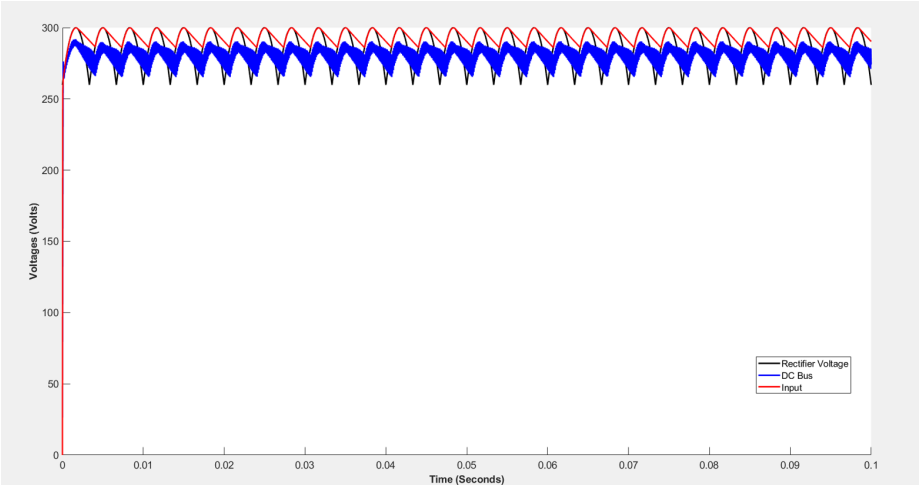
Modules current FFT analysis (Zoom in range of 40kHz)

7 Effect of 3-phase rectifier by using State Space Model.

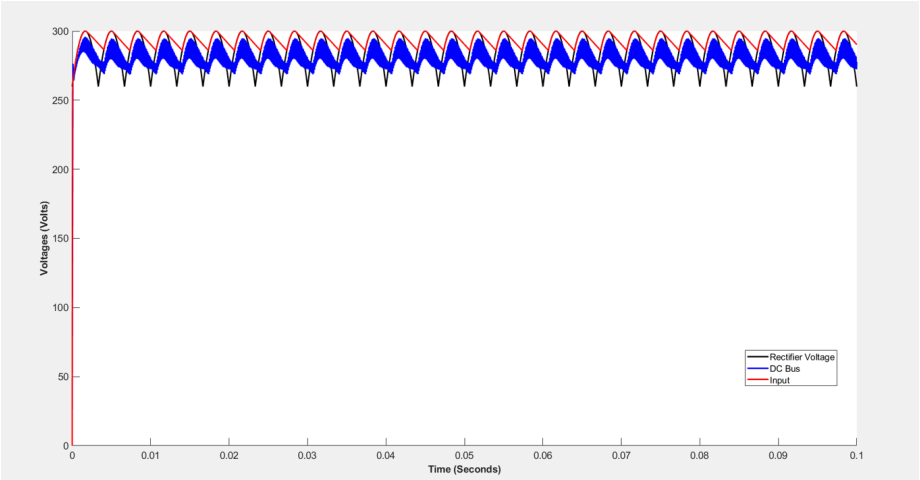
We can think that rectifier model is split in two part. One of them is 3 phase(six pulse) supply voltages and it supply current for inverter and capacitors of rectifier.
If rectifier capacitors exceed the voltage of six pulse, six pulses behaves like open circuit and the current of inverter is supplied by rectifier capacitor until the rectifier capacitor voltages become lower than rectifier voltages.



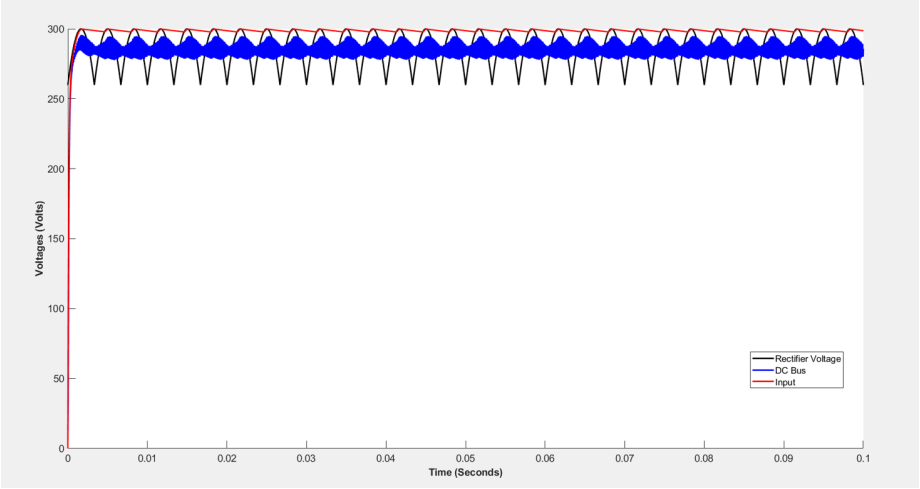
$R_{rec} = 1e-2$ (It determines the time constant of capacitor charging)
$M = 0.5$ (it determines the current supplied by capacitor at discharging mode)
$\delta = \pi/2$ (phase of reference voltages)
$C_{drec} = 1.1mF$(realistic value)



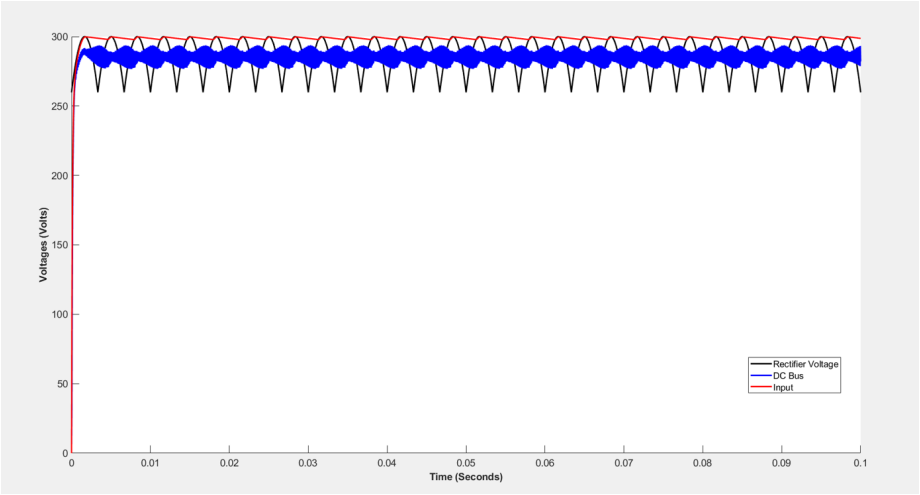
$R_{rec} = 1e-2$ (It determines the time constant of capacitor charging)
$M = 0.9$ (it determines the current supplied by capacitor at discharging mode)
$\delta = \pi/2$ (phase of reference voltages)
$C_{drec} = 1.1mF$ (realistic value)



$R_{rec} = 1e-2$(It determines the time constant of capacitor charging)
$M = 0.9$ (it determines the current supplied by capacitor at discharging mode)
$\delta = 0$(phase of reference voltages)
$C_{drec} = 1.1mF$ (realistic value)



$R_{rec} = 1e-2$ (It determines the time constant of capacitor charging)
$M = 0.9$ (it determines the current supplied by capacitor at discharging mode)
$\delta = 0$(phase of reference voltages)
$C_{drec} = 10mF$ (unrealistic value)



$R_{rec} = 1e-2$(It determines the time constant of capacitor charging)
$M = 0.9$ (it determines the current supplied by capacitor at discharging mode)
$\delta = \pi/2$(phase of reference voltages)
$C_{drec} = 10mF$ (unrealistic value)

Actually, the dc bus has third harmonic injected by 3 phase (non linear, we do not know other other injection).
It is actually low frequency part and we can observe this at fft analysis and eyes.
Also, dc bus has a envelope(six step) . Envelope is not low frequency part, it is actually modulation of high frequency and low frequency part. We can observe because of side band.
Reference voltages phases changes the envelope phase.

$$V_{dcbus} = V_{dc} + V_{3rd} * sin(2\pi 300t + \phi_1) + V_{envelope} sin(2\pi f_S t + \phi_{20}) sin(2\pi 150t + \phi_3 + \delta)$$

8 Summary

Experimental data includes harmonic components such as 100 Hz, 300Hz(multiplies) and switching frequency(with side bands).
We can explain 100 Hz harmonic by unbalanced load. If required, it can be calculated analytically or modelled by matlab-simulink. Also, switching frequency can be calculated analytically by using frequency domain and convolution. However, rectifier is nonlinear components. It is hard to calculate harmonic distribution of rectifier by analytically.

8.1 The moral of a Story

In order to explain 300 Hz and multiplies components, we establish test setup which has two different DC source. One of them 3-phase rectifier and other is high frequency DC-DC converter. Thus, we can test two situation and we observe the 300Hz components to explain the connection of 300 Hz an rectifier.