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Analytic Calculation of the DC-Link Capacitor Current for Pulsed Single-Phase H-Bridge Inverters*

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Keywords: Uninterruptible power supplies (UPS), Converter circuits, High frequency power converter, Power transmission, Harmonics, Measurements

Abstract

For pulsed single-phase H-bridge inverters the capacitor current in the dc-link circuit is analytically calculated. These calculations can be applied for a constant dc-voltage as well as for a sinusoidal modulated voltage and sinusoidal current at the output. The additional load of the dc-link capacitor caused by harmonic currents of the filter circuit or by switching transitions of semiconductors is examined, too. At last, the calculations are confirmed by practical measurements.

Introduction

The dc-link capacitor contributes substantially to the volume, the weight and the costs of a pulsed inverter. For this reason the necessary amount of capacitors has to be determined exactly to prohibit over design [1]. With most applications the capacitor design is crucially determined by the current load. In this paper the capacitor current is mathematically calculated for a pulsed single-phase H-bridge inverter. For this purpose the power stage of the pulse inverter is presented in the Fig. 1. It consists out of an inverter bridge, an input filter circuit with dc-link capacitors and a filter circuit on the alternating voltage side.

First for the calculation an ideal sinusoidal modulated voltage u_P and a sinusoidal current i_P with any phase angle at the inverter output is supposed. The influence of the harmonic current by the output filter circuit of the inverter is calculated later. The load of the dc-link capacitors by switching transitions in the H-bridge is examined. The valid inverter control schemes for the calculation are introduced hereunder. The calculation results are proven by practical measurements.

Control schemes of single phase inverters

Two pulsed control schemes are presented in Fig. 2. The output voltage of the inverter bridges are controlled by three voltage levels. With the first control scheme in the figure on the left both inverter-legs are only pulsed with the half output pulse frequency of the inverter. Besides one inverter-leg is pulsed with a long pulse, while the other bridge-leg is pulsed with a short pulse. The difference of the two bridge-legs pulses results in two new pulses at the phase output. After each half fundamental period the pulse lengths of the two bridge-legs are exchanged, so that the polarity of the output voltage u_P changes. In the middle of the figure the sinusoidal fundamental portion of the output voltage u_{P1} is presented. Besides the voltage a sinusoidal output current i_{P1} with phase shift angle is drawn in. Below the output current distribution in the switching elements of the inverter bridge is shown. In the figure the current in the transistors i_T and diodes i_D of the switching element S is depicted.

With the pulse control scheme in the figure on the right, one bridgeleg is pulsed for a half fundamental period alternating with a sine-modulated or with a complementary sine-modulated signal, while the other bridge-leg changes the voltage at the output each half fundamental period. If the high frequency pulsed half-bridge creates a sine-modulated signal, the output of the other half-bridge is negative. With complementary sine-modulated signal of the bridge-leg the other one creates a positive signal. The difference of the two output voltages results in a sine-modulated signal with three voltage levels.

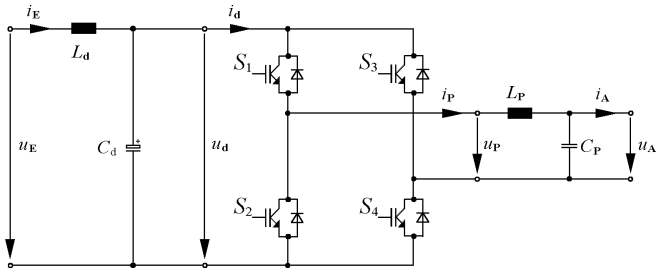

Fig. 1: Power stage of the pulsed H-bridge inverter with input and output filter circuit

Calculation of the dc-link capacitor current

Now for the pulsed control schemes the current in the dc-link circuit will be calculated. Beside a sinusoidal duty cycle shape that means a sinusoidal modulated voltage u_P and a sinusoidal current i_P at the output of the inverter bridge is assumed. Moreover, the voltage u_d in the dc-link circuit is presumed as constant. The input current of the inverter can be split in a dc-component, in an ac-component with double fundamental frequency and in a higher-frequent component given that the dc-link voltage U_d is constant, at sinusoidal modulated voltage u_P and sinusoidal output current i_P [2, 3, 4, 5]. In Fig. 3 the input current of the inverter as well as its split into individual components for ohmic - and inductive load are presented.

The middle part of the figure shows that the current flow in the inverter input recurs after a half fundamental period. Therefore for the calculation, only the range $0° \leq \omega_1 t \leq 180°$ is considered.

*: This paper has been designated as outstanding paper of EPE 2003

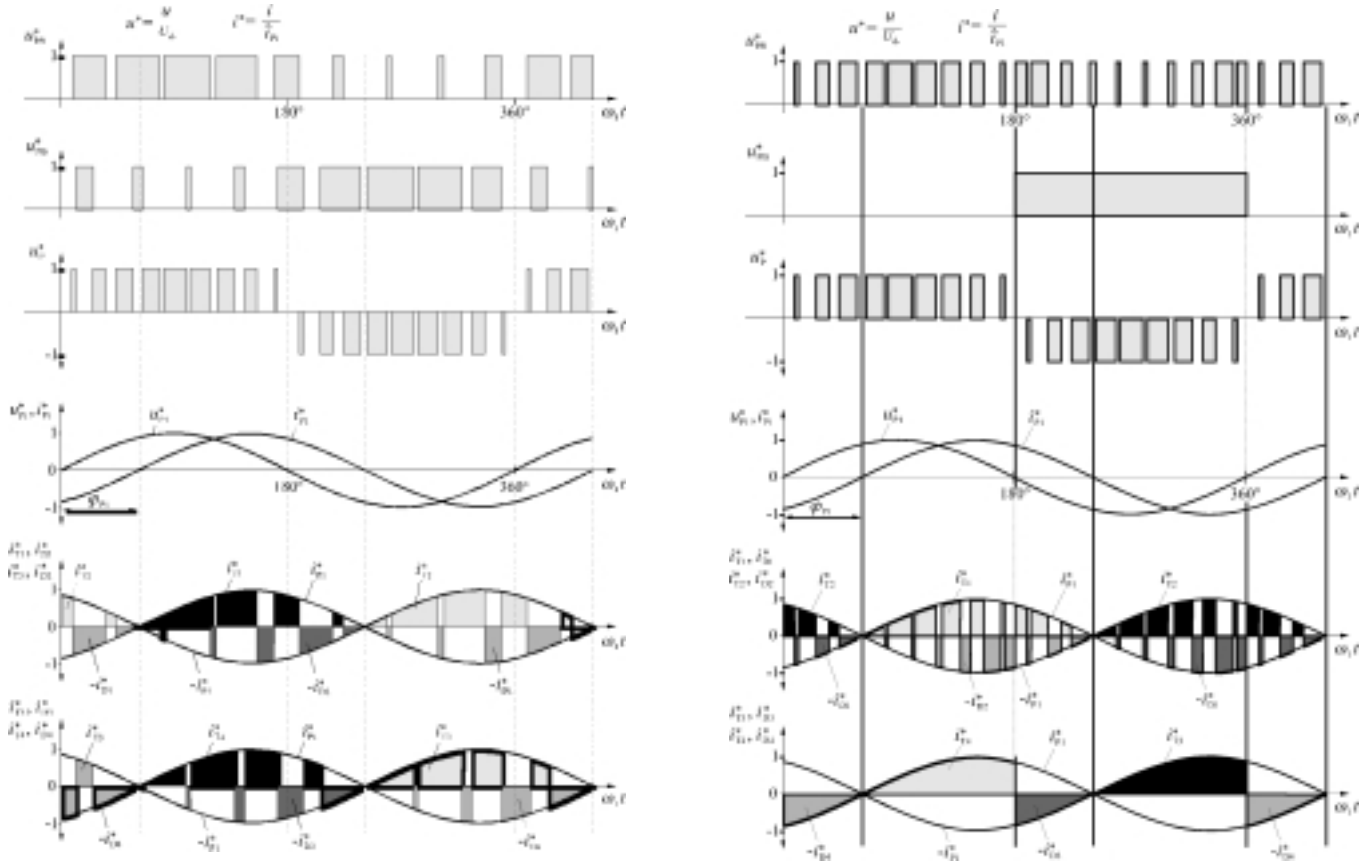

Fig. 2: Voltage- and current waveforms in the single phase inverter for two sine-modulated pulse control schemes with three voltage levels [2]

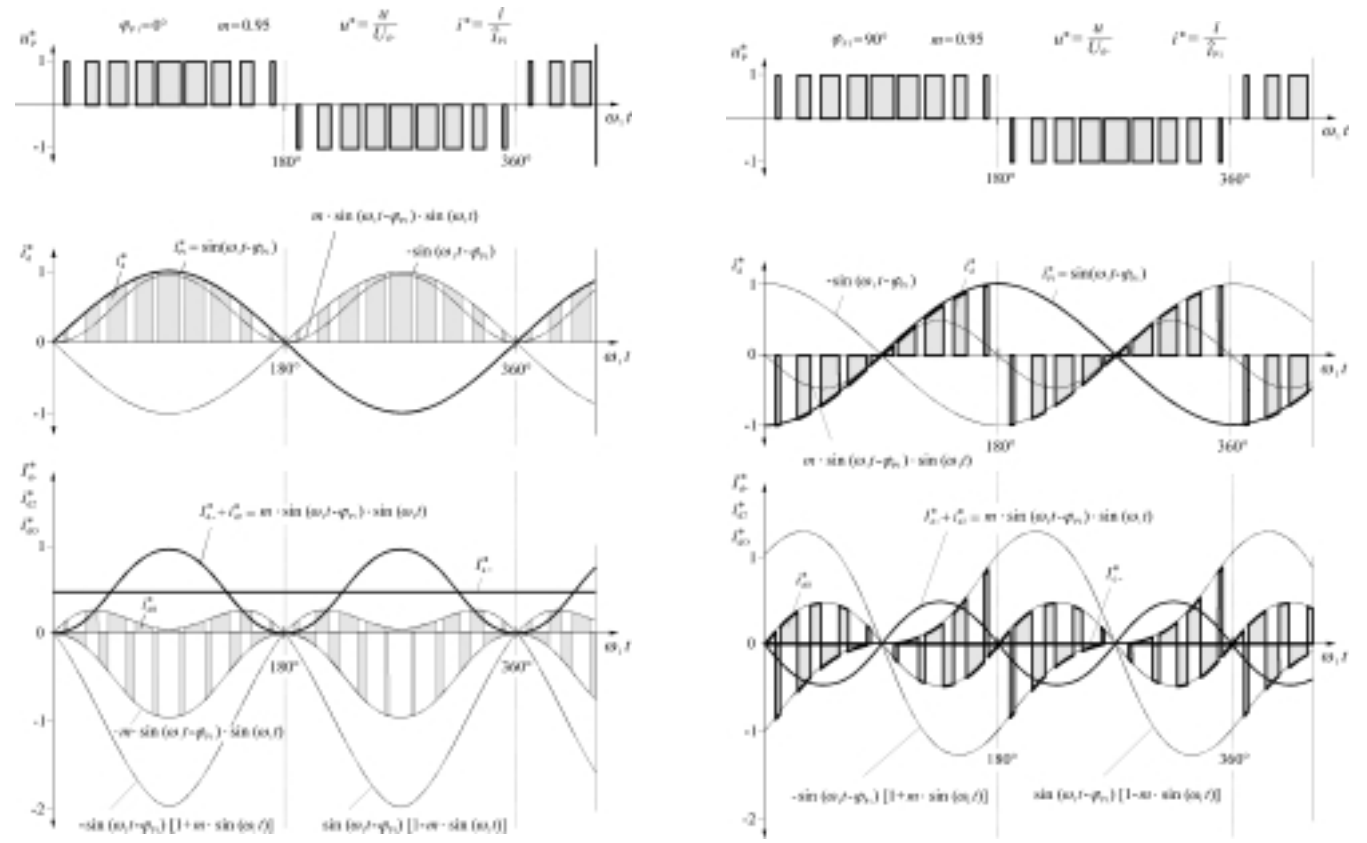

Fig. 3: Input current i_d of a single phase inverter and its split into the individual components with a phase shift angle of $\varphi_{P1} = 0°$ (left) and $\varphi_{P1} = 90°$ (right) [2]

Within this range the fundamental current in the filter circuit inductor forms an envelope for the current pulses at the input of the inverter. The instantaneous value of the current is dependent to the phase shift angle φ_{P1} of the inductor current and the actual duty cycle of the modulation factor *m*. In the following formulas the waveform of the current and the related duty cycles in the switch-on states – that means connection to the positive terminal of the dc-link capacitor – are shown.

Current – and duty cycle waveforms in the switch-on state:

$$i_{de}(t) = \hat{i}_{P1} \cdot \sin(\omega_1 t - \varphi_{P1}), \tag{1}$$

$$\frac{t_e(t)}{T_P(t)} = m \cdot \sin(\omega_1 t), \tag{2}$$

for $0 \le m \le 1$ and $-90° \le \varphi_{P1} \le 90°$.

The average-values of the current pulses in all individual pulse periods results in a dc-current which is superimposed by an alternating current with double fundamental frequency [I_{d-} + $i_{d2}(t)$]. This current is determined by multiplication of current and duty cycle waveforms.

$$I_{d-} + i_{d2}(t) = i_{de}(t) \cdot \frac{t_e(t)}{T_P(t)}, \tag{3}$$

$$I_{d-} + i_{d2}(t) = m \cdot \hat{i}_{P1} \cdot \sin(\omega_1 t - \varphi_{P1}) \cdot \sin(\omega_1 t). \tag{4}$$

The constant dc-component I_{d-} and the double fundamental frequency component $i_{d2}(t)$ results to:

$$I_{d-} = \frac{m \cdot \hat{i}_{P1}}{2} \cdot \cos(\varphi_{P1}), \tag{5}$$

$$I_{d2} = \frac{m \cdot \hat{i}_{P1}}{2 \cdot \sqrt{2}}. \tag{6}$$

The two formulas shows: the dc-component depends on the phase shift angle φ_{P1} and on the modulation factor *m*. The rms-value of the double fundamental frequency portion however has same value at all phase shift angles φ_{P1} and changes only with the modulation factor *m*.

Now with the low-frequency current waveform of equation (4) the envelopes of the pulses of the higher-frequency current portion are determined. This is done by subtracting of the determined low-frequency current portion (equation 4) from envelope of the output current and zero line (inverting). The associated duty cycles are shown for the current pulses in the switch-on and -off condition.

Current – and duty cycle waveform in the switch-on state:

$$i_{dO\,e}(t) = \hat{i}_{P1} \cdot \sin(\omega_1 t - \varphi_{P1}) \cdot \left[1 - m \cdot \sin(\omega_1 t)\right], \tag{7}$$

$$\frac{t_e(t)}{T_P(t)} = m \cdot \sin(\omega_1 t). \tag{8}$$

Current – and duty cycle waveform in the switch-off state:

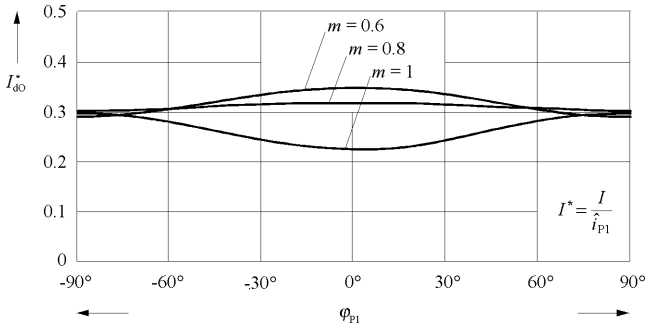

Fig. 4: Higher-frequency current portion in the dc-link capacitors (rms-value)

$$i_{dO\,a}(t) = -\hat{i}_{P1} \cdot m \cdot \sin(\omega_1 t - \varphi_{P1}) \cdot \sin(\omega_1 t), \tag{9}$$

$$\frac{t_a(t)}{T_P(t)} = 1 - m \cdot \sin(\omega_1 t). \tag{10}$$

The rms-value of the higher-frequency current portion is determined by the current waveforms and the appropriate duty cycles within half fundamental period. For this the integral is set up in switched on- and switched off-state and then the arithmetic sum of the two partial results is calculated.

$$I_{dO}^2 = \frac{1}{\pi} \cdot \int_0^{180°} \left[i_{dO\,e}^2(t) \cdot \frac{t_e(t)}{T_P(t)} + i_{dO\,a}^2(t) \cdot \frac{t_a(t)}{T_P(t)} \right] d\omega_1 t, \tag{11}$$

$$I_{dO}^2 = \frac{m \cdot \hat{i}_{P1}^2}{\pi} \cdot \int_{0°}^{180°} \left[\sin(\omega_1 t - \varphi_{P1})\right]^2 \cdot \left[\sin(\omega_1 t) - m \cdot \sin^2(\omega_1 t)\right] \cdot d\omega_1 t, \tag{12}$$

$$I_{dO} = \hat{i}_{P1} \cdot \sqrt{\frac{m}{24 \cdot \pi} \cdot \left[24 - 6 \cdot \pi \cdot m + (8 - 3 \cdot \pi \cdot m) \cdot \cos(2\varphi_{P1})\right]}. \tag{13}$$

In Fig. 4 the rms-value of the higher-frequency current in the dc-link capacitors is presented for different modulation factors *m* as a function of the phase shift angle φ_{P1}. This result refers to the control of the inverter bridge with three voltage levels.

The result shows: the higher-frequency rms-current depends on the modulation factor *m* of the inverter and on the fundamental phase shift angle φ_{P1}. As the parasitic inductance from the half-bridge to the dc-link circuit usually is very much lower than to the dc-voltage supply (factor > 100) approximately the entire higher-frequency current – presented in the figure – flows through the dc-link circuit capacitor. The maximum value of the current is indicated in the following formula:

$$I_{dO\,max} \approx 0.35 \cdot \hat{i}_{P1}, \tag{14}$$

for $\varphi_{P1} = 0°$ and $m \approx 0.566$.

Beside this current, still another portion of the current with double frequency (equation 6) flows in the dc-link capacitors. This portion depends considerably on inductance L_d in the dc-input of the inverter and can easily be determined from the parallel connection of L_d and C_d. By arithmetic addition of the higher-frequency current

portion and the current with double frequency the total value of current in the dc-link circuit capacitors can be determined [2].

Current harmonics of the filter circuit and the switching transitions

The accomplished capacitor current calculations are referring to an ideal sinusoidal output current at the inverter bridge. Now current harmonics of the dc-link capacitor, caused by the output filter circuit of the inverter or by switching transitions in the inverter bridge has to be determined.

Current harmonics of the output filter circuit

In the filter circuit a triangle waveform current is generated by the pulse frequency of the inverter which is superimposed by the fundamental current. The influence of this harmonic current in the filter circuit has to be calculated. In Fig. 5 the principle shape of the triangle harmonic current (middle) and the sinusoidal output current which is superimposed by a harmonic current (below) for pulse width modulation are presented.

The amplitude of the current ripple $\Delta I_{PO}(t)$ in the filter inductor is dependent by the voltage-time area in the pulse period and the inductance value. The shape of the voltage-time areas within the fundamental period changes and can be calculated from the product of the inductor voltage in the switch-on state and the associated switch-on duration. It is assumed that the voltage at the output of the filter circuit is constant during the switching-on status. With the following formula the current ripple is calculated within one fundamental period [2].

$$\Delta i_{PO}(t) = \frac{u_{LP}(t) \cdot t_e(t)}{L_P}. \qquad (15)$$

Now the voltage waveform at the inductor in the switch-on state and the related duty cycles for the fundamental period are calculated for control of the three voltage level inverter. Furthermore the pulse width modulation with constant pulse frequency is assumed. Voltage – and duty cycle waveform in the switch-on state:

$$u_{LP}(t) = U_{d-} \cdot \left[1 - m \cdot \sin(\omega_1 t)\right], \qquad 16)$$

$$\frac{t_e(t)}{T_P} = m \cdot \sin(\omega_1 t), \qquad (17)$$

for $0 \le m \le 1$ in the range of $0° \le \omega_1 t \le 180°$

With these relations the waveform of the current ripple $\Delta I_{PO}(t)$ in the inductor within one fundamental period is determined [6]. Afterwards the maximum of the current ripple can be calculated by derivations of the equation. As design criteria for the output filter inductance this maximum current ripple usually set to values between 0.1 and 0.3 of the peak-value of nominal output current.

$$\Delta i_{PO}(t) = \frac{U_{d-} \cdot T_P}{L_P} \cdot \left[1 - m \cdot \sin(\omega_1 t)\right] \cdot m \cdot \sin(\omega_1 t), \qquad (18)$$

with $\Delta i_{PO\ max} = \dfrac{U_{d-} \cdot T_P}{4 \cdot L_P}$ at $m \cdot \sin(\omega_1 t) = \dfrac{1}{2}$.

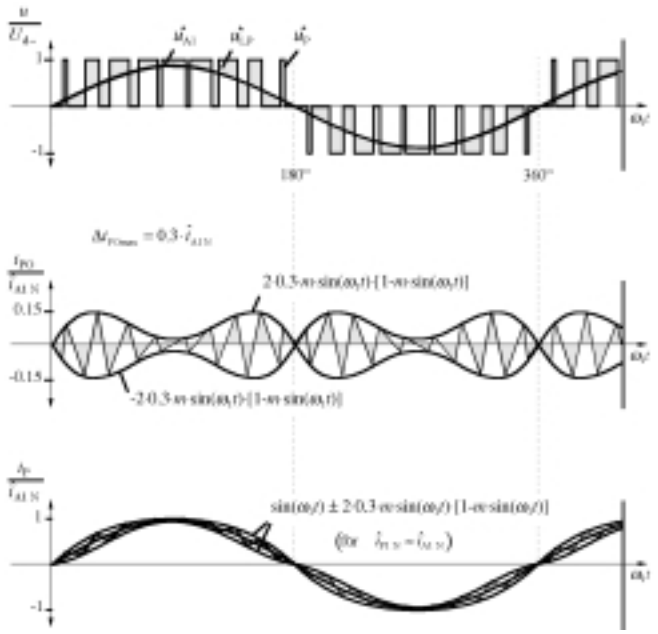

Fig. 5: Superimposition of the output - and triangle waveform current in the output filter circuit

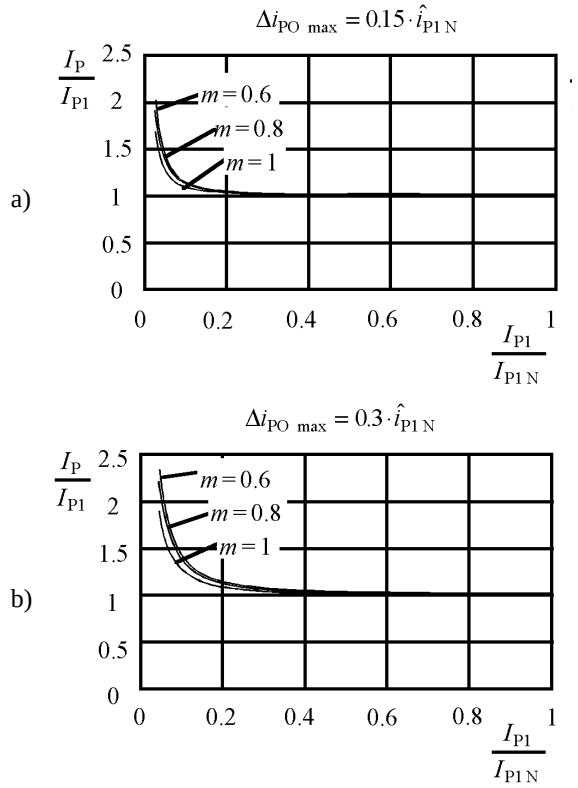

Fig. 6: Influence of the triangle harmonic current to the total rms-current in the filter inductance at pulse width modulation with three voltage levels

With the determined relation the current ripple waveform $\Delta I_{PO}(t)$ can be indicated as a function of the maximum current ripple ΔI_{POmax} and the modulation factor m.

$$\Delta i_{PO}(t) = 4 \cdot \Delta i_{PO\ max} \cdot \left[1 - m \cdot \sin(\omega_1 t)\right] \cdot m \cdot \sin(\omega_1 t). \qquad (19)$$

In Fig. 5 the shape of the triangle waveform current is presented during one fundamental period. Below in the figure, one can recognize the fundamental current at ohmic load is superimposed with the triangle waveform harmonic current.

For the calculation from the rms-value of a triangle waveform current harmonics first the rms-current within one pulse period must by calculated. If the result is transferred to each pulse period, an "rms-current waveform" for the fundamental period is received.

$$I_{\mathrm{PO}\,T_\mathrm{p}}(t) = \frac{4\cdot\Delta i_{\mathrm{PO\,max}}}{2\cdot\sqrt{3}}\cdot\left[1-m\cdot\sin(\omega_1 t)\right]\cdot m\cdot\sin(\omega_1 t). \tag{20}$$

The integration of the rms-values in the individual time-interval results in the total rms-value of the harmonic triangle waveform current within one fundamental period.

$$I_{\mathrm{PO}} = \sqrt{\frac{1}{T_1}\cdot\int_0^{T_1}\left[I_{\mathrm{PO}\,T_\mathrm{p}}(t)\right]^2\cdot\mathrm{d}t}, \tag{21}$$

$$I_{\mathrm{PO}} = \sqrt{\frac{1}{\pi}\cdot\int_0^{\pi}\left[\frac{4\cdot\Delta i_{\mathrm{PO\,max}}}{2\cdot\sqrt{3}}\cdot\left[1-m\cdot\sin(\omega_1 t)\right]\cdot m\cdot\sin(\omega_1 t)\right]^2\mathrm{d}\,\omega_1 t}, \tag{22}$$

$$I_{PO} = \Delta i_{PO\,\max}\cdot\sqrt{\frac{12\cdot\pi\cdot m^2-64\cdot m^3+9\cdot\pi\cdot m^4}{18\cdot\pi}}. \tag{23}$$

The complete rms-value of the current in the inductor can be calculated with geometrical addition of the fundamental – and the triangle waveform current harmonics.

$$I_\mathrm{P} = \sqrt{I_{\mathrm{P1}}^2 + I_{\mathrm{PO}}^2}, \tag{24}$$

$$I_\mathrm{P} = \sqrt{\frac{\hat{i}_{\mathrm{P1}}^2}{2} + \frac{\Delta i_{\mathrm{PO\,max}}^2\left(12\cdot\pi\cdot m^2-64\cdot m^3+9\cdot\pi\cdot m^4\right)}{18\cdot\pi}}, \tag{25}$$

for $\Delta i_{\mathrm{PO\,max}} = (0.1-0.3)\cdot\hat{i}_{\mathrm{A1\,N}}$,
$0\le m\le 1$.

Fig. 6 shows the influence of the triangle waveform harmonic current to the total rms-value dependent on the output power for two different maximum current ripples. The maximum current ripple in the filter circuit is referred to the peak value of the fundamental current in the filter circuit inductor with nominal power output $\hat{i}_{\mathrm{P1N}}$. This peak value is at nominal power nearly equal to the peak value of output current ($\hat{i}_{\mathrm{P1N}} = \hat{i}_{\mathrm{A1N}}$).

The result of the calculation shows that the triangle harmonic current has a neglectable contribution to the total rms-value at larger output power. Only if output power is smaller than 20 % of

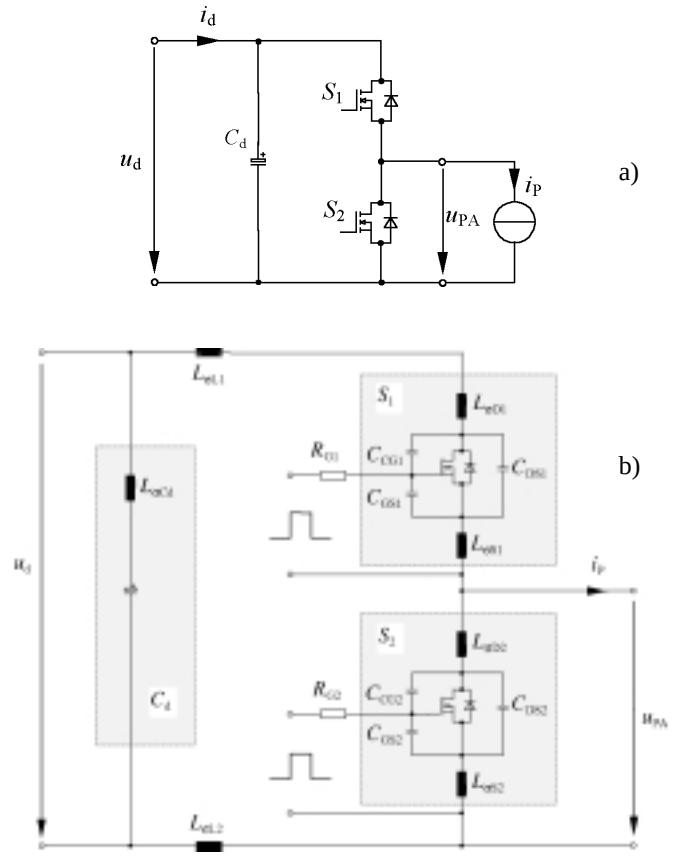

Fig. 7: Phase-leg of a hard switched MOSFET-Inverter (a) with parasitic elements (b)

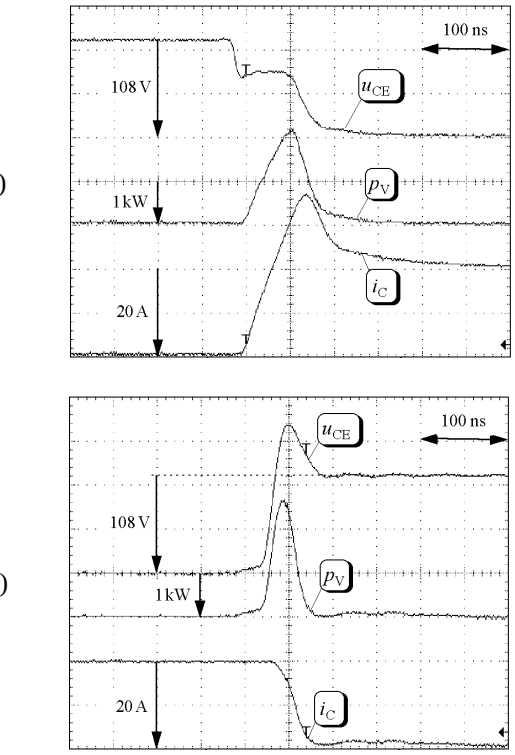

Fig. 8: Hard switch-on (a) and switch-off transition (b) of a transistor in a bridge-leg with inductive load

the nominal power a deviation from ideal line is recognized. If the maximum current ripple of the inductor is designed to smaller value (Fig. 6a), than the influence of the triangle harmonic current to the total rms-value becomes still smaller.

As the harmonic current in the output filter circuit with large output power has only a negligible contribution to the total rms-value, it will also hardly affect the load of the dc-link capacitors. Only with small output power an additional heating by harmonic currents in the dc-link capacitors has to be expected. The influence of the triangle waveform current ripple to the load of the dc-link capacitor is calculated for a dc/dc-converter in [7]. Even with a current ripple of 0.6 of the maximum output current the additional load by the triangle waveform current with nominal output power is small.

Current harmonics of the switching transitions

In inverters the transistors are generally hard switched, that means the transistors operate without snubbers. For this kind of switching transitions in the inverter bridge the additional current load of the dc-link capacitors is to be examined. For the analysis of the hard switching transition the relevant electric circuit of one phase-leg is presented in Fig. 7a. Parasitic inductances from the dc-link capacitor, the copper track on the PCB and the semiconductors are included to the current path. Besides capacitive coupling between the leds of the MOSFET have to be considered [8, 9].

Fig. 8 shows the switch-on - (a) and the switch-off transition (b) of a transistor in the half-bridge. During switch-on the current i_C in the semiconductor rises as the voltage at the transistor at first stays almost constant. Only if the current in the opposite diode of the half-bridge reaches the value of the reverse current peak, the voltage u_{CE} at the switching element decreases. The switch-on element is loaded thereby with the output current and the reverse current from the diode.

At switch-off first the voltage at the transistor rises to the value of the dc-link circuit voltage before the current begin to decrease in the switching element. During the current decreases the voltage at the transistor shows an over-shoot. In the middle of the figures the shape of the instantaneous power dissipation in the transistor is shown in each case.

During the switched-off transitions of the transistors in the inverter additional load in the dc-link capacitor will not occur. During the switch-on transition a reverse diode current through the diode flows into the dc-link capacitor. This additional current into the dc-link circuit can have a substantially contribution to the heating of the inverter capacitors with small output power. But at higher power generally the calculated capacitor current caused by output current dominates. However no statement for all semiconductor types can be made here. Beyond this the additional current depends considerably by the pulse frequency of the inverter.

Comparison of the calculations with practical measurements

Now the calculated capacitor current in the dc-link circuit will be compared with practical measurements of on an IGBT inverter. The inverter presented in Fig. 1 has a nominal output power of P_{AN} = 1200 W and a dc-link voltage of U_{d-} = 108 V. The modulation scheme of the inverter is presented in Fig. 2 on the right. For all switch elements in the bridge two IGBTs with internal diodes are connected parallel. The low-frequency pulsed half-bridge (50 Hz) consists out of IGBTs of the type IXYS IXGH38N60U1 in the other half-bridge (33 kHz) IGBTs of the type IXYS IXGH32N60AU1 are used. The output filter consists of an induc-

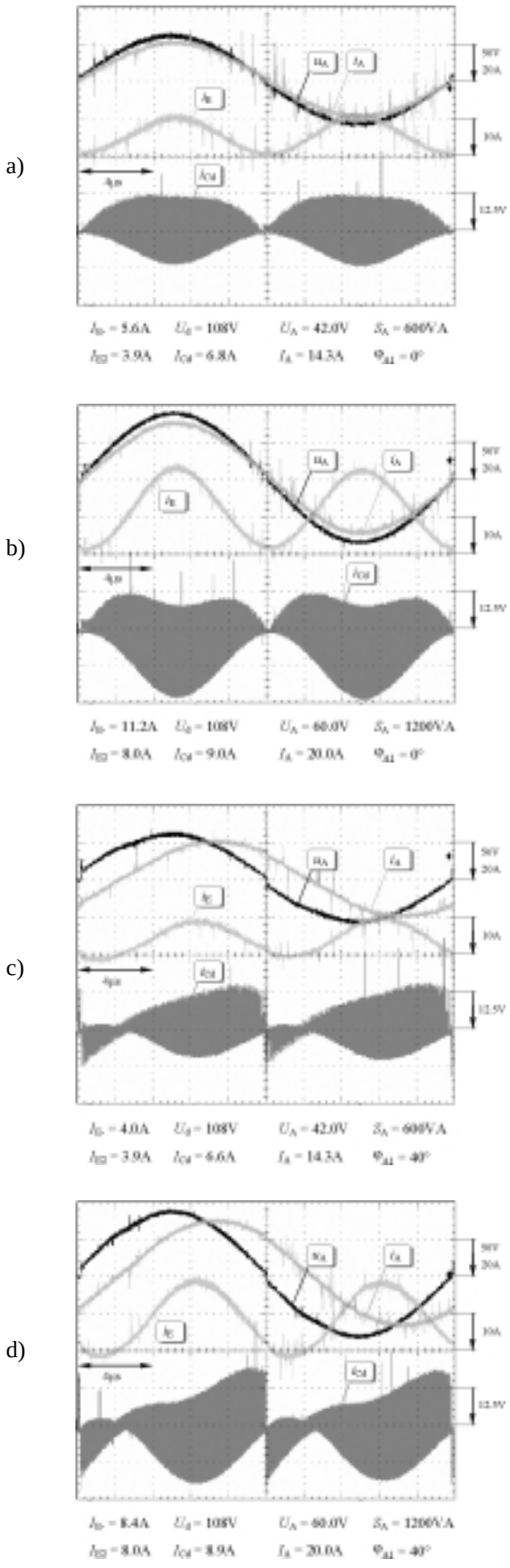

Fig. 9: Current in the dc-link capacitors as well as the input - and output values of a single-phase inverter (practical measurements)

tor (L_P = 125 µH, Epcos E-70 N27 core) and of three parallel connected capacitors of the type Wima MKP 10 (4.7 µF, 160 V-/ 100 V~). The wiring between dc-input and power supply has a parasitic inductance. The dc-link circuit of the inverter is build out of six capacitors of the type Epcos B41507-B9228-M (two in series and three parallel).

In Fig. 9 the sinusoidal output values u_A and i_A as well as the input current i_E of the inverter are presented for ohmic (a, b) and ohmic/inductive loads (c, d). The inverter operates in each case at half nominal load (Fig. a, c) and at nominal load (Fig. b, d). The dc-link voltage of 108 V is approximately constant in all cases (not presented). The current in the dc-link capacitors i_{Cd} is shown below in the diagrams. The scales of the electrical values are presented right in each case, whereby the tip of each arrow marks the zero-line. All designations of the electrical values are given in Fig. 1.

The results show that the inverter input current i_E consists out of a dc-component i_{E-} and a portion with double fundamental frequency i_{E2}. With increasing output power the amplitude of the double fundamental frequency becomes larger, so that the dc-portion and rms-value of the low frequency part in the H-bridge input changes. Besides the dc-current i_{E-} vary with the phase shift angle at the inverter output. Due to the high switching frequency of the inverter the envelope curve of the capacitor current i_{Cd} is well visible. The envelope waveform repeats after a half fundamental period. A small asymmetry to the "90° mirror-axis" in the current curve at ohmic load can be seen above in the figure. It is caused by a small portion of the double fundamental current in the dc-link capacitors and by a very small shift of the phase angle by the output filter circuit.

All waveforms in principle correspond very well with the mathematical derivations. The results from the measurements, what is written below each plot show also a very good correspondence to the calculated values.

Conclusion

Today pulse inverters are used world-wide in many areas for the ac-power supply. The dc-link capacitors in the pulse-controlled power stages contribute thereby substantially to the volume, to the weight and to the costs of an inverter. For this reason the necessary size of capacitors has to be determined exactly to avoid over design. Usually the dc-link capacitor size is determined by the current load.

For a single-phase inverter bridge the dc-link capacitor current in this publication was calculated analytically. A constant input dc-voltage as well as a sinusoidal current at the output of the inverter H-bridge is assumed. The results show, that the capacitor current can be split in a portion having double fundamental frequency and a higher-frequency component. The low-frequency current into the H-bridge is split differently into capacitor current and input current according to the design of the input filter circuit. The higher-frequency current portion flows nearly completely through the dc-link capacitors. The maximum value is 0.35 of the output current peak-value.

The influence of harmonics, which result from the output filter circuit and from the switching transistions in the inverter bridge, is examined. It is shown, that at small output power significant capacitor load is caused by these harmonics. But at high output power the calculated capacitor current caused by output current dominates again, so that no considerable additional load will occur. At the end the calculations are compared with practical measurements of an IGBT inverter. A good correspondence between the calculated and measured values is shown.

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