Challenges of Junction Temperature Sensing in SiC Power MOSFETs

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***Abstract*-- Junction temperature sensing is an integral part of both on-line and off-line condition monitoring where direct access the bare die surface is not available. Given a defined power input, the junction temperature enables the estimation of the junction-to-case thermal resistance, which is a key indicator of packaging failure mechanisms like solder voiding and cracks. The use of temperature sensitive electrical parameters (TSEPs) has widely been proposed as a means of junction temperature sensing however, in SiC power devices there are certain challenges regarding the use of TSEPs. Bias Temperature Instability (BTI) from charge trapping in the gate dielectric causes threshold voltage drift, which in SiC affects some of the key TSEPs including ON-state resistance, body diode forward voltage as well as the turn-ON current commutation rate. This paper reviews the challenges of junction temperature sensing in SiC power devices, the impact of BTI on TSEPs and how different researchers have approached the issue of power cycling SiC power devices and modules.**

***Index Terms*— SiC MOSFETs, Junction Temperature, BTI, Power Cycling**

I. Introduction

Condition monitoring based on junction temperature sensing by means of Temperature Sensitive Electrical Parameters (TSEPs) appears as a suitable method for increasing the reliability of power electronic systems [1, 2]. TSEPs are also fundamental for power cycling, as they enable the control of the junction temperature excursion during power cycling, which is fundamental for obtaining lifetime estimation [3]. The ability to determine the junction temperature during power cycling is also fundamental for monitoring the degradation of the thermal impedance of the device/module due to degradation of the packaging elements, namely solder and wirebonds.

TSEPs have been widely used for silicon devices, however there are several challenges regarding the use of TSEPs in SiC power devices. SiC power MOSFETs, by virtue of the wider bandgap compared to silicon, are not as temperature sensitive as silicon devices [4]. This is sometimes presented as an advantage, especially since the switching and conduction losses do not increase rapidly with temperature [5, 6].

From the point of view of condition monitoring, the reduced temperature sensitivity of SiC makes the use of TSEPs for junction temperature sensing more difficult. Moreover, the drift of the threshold voltage caused by Bias Temperature Instability (BTI) in SiC MOSFETs [7-9] adds more complexity to the process of junction temperature measurement, making it a challenge compared to Si devices. This paper is organized as follows: section II presents a review of some of TSEPs in SiC MOSFETs, section III evaluates how the threshold voltage shift caused by BTI affects the measurement of the junction temperature using TSEPs and section IV reviews the proposed methodologies for power cycling SiC MOSFETs and section V concludes the paper.

II. TSEPs In SiC MOSFETs Overview

The temperature sensitivity of some of the most common TSEPs for SiC MOSFETs is presented in this section. The evaluated TSEPs are the threshold voltage V_{TH}, ON-state resistance $R_{DS\text{-}ON}$, gate voltage plateau V_{GP}, the body diode voltage V_{SD} and the switching rate of the drain current dI_D/dt. There are other TSEPs like the internal gate resistance or peak gate current [10-11] which are not covered in this paper.

A. Threshold voltage

The threshold voltage V_{TH} is a well-known TSEP for MOS gate devices [12, 13]. The threshold voltage can be defined as the gate voltage required to invert the channel i.e. to raise the MOSFET surface potential to twice the bulk potential [13]. An expression of V_{TH} is given by (1) [13].

$$V_{TH} = \frac{\sqrt{4\varepsilon_S kTN_A ln(N_A/n_i)}}{C_{ox}} + \frac{2kT}{q} ln\left(\frac{N_A}{n_i}\right) - \frac{Q_{ox}}{C_{ox}} \quad (1)$$

V_{TH} reduces with temperature due to the increasing intrinsic carrier concentration n_i. A detailed expression of the temperature sensitivity of V_{TH} is given in [14].

B. ON-state resistance

The ON-state resistance $R_{DS\text{-}ON}$ of a MOSFET is the resistance between the drain and source terminals when the device is ON. It is comprised of different parasitic resistances which contribute to the total ON-state resistance, as defined in [15]. In the case of a SiC planar MOSFET, the total $R_{DS\text{-}ON}$ can be expressed using (2) [15, 16]. R_{CH} is the channel resistance, R_{JFET} is the resistance of the JFET region and R_{DRIFT} is the resistance of the drift layer. In a SiC trench MOSFET, there is no JFET resistance, so R_{JFET} is eliminated from (2).

$$R_{DS\text{-}ON} \sim R_{CH} + R_{JFET} + R_{DRIFT} \quad (2)$$

This work was supported by the UK Engineering and Physical Science Research Council through the grant EP/R004366/1

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In SiC MOSFETs, as a result of the high critical electric field, a thinner drift layer is required for blocking high voltages, thereby the contribution of R_{DRIFT} to the total ON-state resistance is reduced compared with Si MOSFETs. This means that the contribution of the R_{CH} to the total R_{DS-ON} is high especially for low voltage devices.

The channel resistance R_{CH} is given by (3) [8]. V_G the gate driving voltage, μ_n the electron effective mobility, C_{OX} the gate oxide capacitance density, L_{CH} is the length of the channel and W the channel width.

$$R_{CH} = \frac{L_{CH}}{W\mu_n C_{OX}(V_G - V_{TH})} \quad (3)$$

The temperature coefficient (TC) of R_{DRIFT} and R_{JFET} is positive (PTC), as both increase with temperature, whereas the channel resistance decreases with temperature meaning it has a negative temperature coefficient (NTC) [16]. As the contribution of the channel resistance is higher in SiC MOSFETs, the temperature sensitivity of R_{DS-ON} is not as pronounced as in Si MOSFET.

This is shown in Fig. 1, where the normalized R_{DS-ON} is plotted as a function of temperature for a series of different 1200 V MOSFETs. It is clearly observed how R_{DS-ON} more than doubles its value in the case of silicon MOSFETs, whereas in the case of the evaluated SiC MOSFETs the temperature sensitivity is lower. Comparing the first and second generation devices, the higher temperature sensitivity of the second generation is due to the improved channel resistance [16]. This results on a well-defined PTC, which is required for paralleling devices safely.

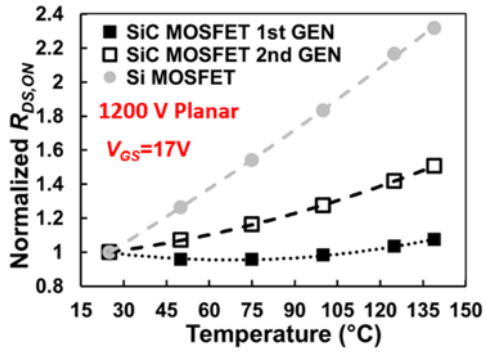

Fig. 1 Normalized ON-State resistance as a function of temperature for different 1200 V Si and SiC MOSFETs

From (3) it is observed how the channel resistance is affected by the gate voltage used to turn-ON the MOSFET as well as temperature (mobility and threshold voltage). Driving the device with lower gate voltage will increase the partial contribution of the R_{CH} to the total R_{DS-ON}, resulting in different temperature coefficients as a function of the gate voltage [17].

This is shown in Fig. 2(a) for a 1st generation SiC MOSFET, where a clear PTC is observed for gate voltage values greater than 16 V and a NTC is observed for lower V_G values. Depending on the SiC MOSFET generation and the improved channel resistance, the impact of the gate voltage will be different. Fig. 2(b) shows the R_{DS-ON} as function of V_{GS} for a 2nd generation device which has PTC for the whole range of driving gate voltage values, with an increased temperature sensitivity as V_{GS} increases.

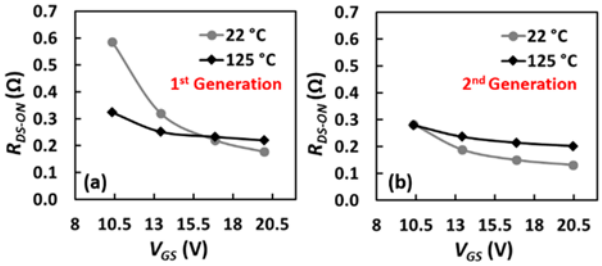

Fig. 2 ON-state resistance as a function of the gate voltage at 22 °C and 125 °C for a SiC MOSFET. (a) First Generation, (b) Second generation

C. Switching rate of the drain current

The switching rate of the drain current dI_{DS}/dt is a TSEP for SiC MOSFET which is analyzed in detail in [17, 18], where it is shown that dI_{DS}/dt increases with temperature. Its temperature sensitivity can be analyzed using (4) [18].

$$\frac{d^2 I_{DS}}{dtdT} = \frac{dV_{GS}}{dt}\left(\beta\left|\frac{dV_{TH}}{dT}\right| - (V_{GS} - V_{TH})\left|\frac{d\beta}{dT}\right|\right) \quad (4)$$

From (4), the elements contributing to the temperature sensitivity of the current commutation rate are dV_{TH}/dT and $d\beta/dT$. In the case of SiC, dV_{TH}/dT dominates the change of $d\beta/dT$, thereby, the turn-ON current switching rate increases with temperature.

Fig. 3 shows the drain current transients during turn-ON of a 650 V SiC trench MOSFET at different temperatures, which were measured using a conventional double pulse test setup. The gate voltage V_{GS} and gate resistance R_G used for characterization were selected to maximize the temperature sensitivity of dI_{DS}/dt, as described in [17]. Fig. 3 clearly shows how the switching rate increases with temperature

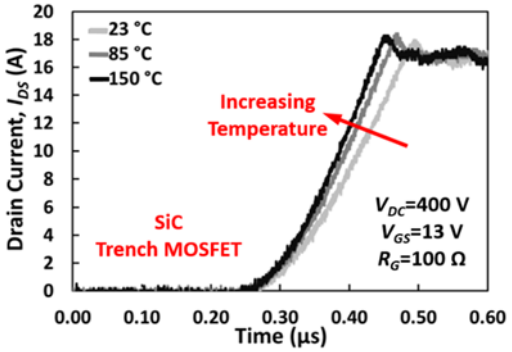

Fig. 3 Drain current transients during turn-ON of a SiC trench MOSFET at different temperatures

D. Gate voltage plateau during turn-ON

As a result of the temperature sensitivity of V_{TH} and dI_{DS}/dt the gate voltage plateau has also a well-defined temperature sensitivity in SiC MOSFETs [18]. The gate voltage plateau is the gate-source voltage value when the drain current reaches the load current during turn-ON. Its value is given by (5) and it is also affected by the value of the load current I_{LOAD} [13].

$$V_{GP} = V_{TH} + \sqrt{\frac{I_{LOAD} L_{CH}}{\mu_n C_{OX} W}} \quad (5)$$

Fig. 4 shows the gate voltage transient during turn-ON of a SiC trench MOSFET at different temperatures, where

it is clearly observed how the gate plateau voltage decreases with temperature.

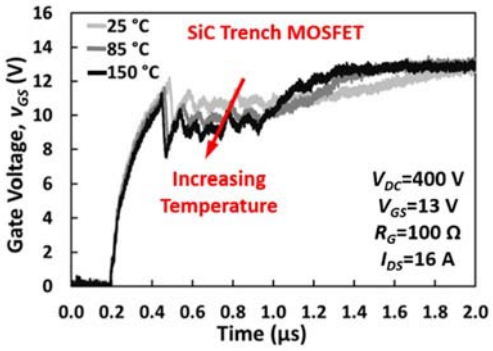

Fig 4 Gate voltage transients during turn-ON of a SiC trench MOSFET at different temperatures

The gate current plateau has the opposed temperature sensitivity to the gate voltage plateau, increasing with temperature [18].

E. Body diode voltage.

The voltage of a PN junction is a well-known TSEP for silicon and silicon carbide devices. It is widely used for determining the junction temperature during power cycling [19] and can be used for diodes and the parasitic body diode of a MOSFET. The forward voltage V_F of PiN diode in the ON-state is given by the sum of the junction voltages, $V_j(p^+n)$ and $V_j(nn^+)$, and the drift layer voltage V_{drift}, as given in (6) [20].

$$V_F = V_j(p^+n) + V_{drift} + V_j(nn^+) \qquad (6)$$

The temperature dependency of the ON-state voltage of PiN diode is determined by the temperature coefficients of the different elements comprising the total voltage. V_F is used as a temperature sensor at low currents and in this situation, the forward voltage V_F of a PiN diode is mainly determined by the junction voltages, defined in (7) [20].

$$V_j(p^+n) + V_j(nn^+) = \frac{kT}{q} ln \frac{p_L n_R}{n_i^2} \qquad (7)$$

The total junction voltage defined in (7) decreases with temperature as its temperature dependency is inversely proportional to the intrinsic carrier concentration n_i, which increases with temperature [20].

Due to the wide bandgap properties, V_F is higher for SiC PiN diodes [20] and one of the peculiarities of the body diode of SiC MOSFETs is that it requires a negative voltage to fully close the channel, resulting on 3rd quadrant characteristics which are V_{GS} dependent [12, 19-21]. Fig. 5 shows the forward voltage V_{SD} of the body diode of a 1200 V SiC planar MOSFET as a function of temperature for a current of 50 mA. The voltage was measured using V_{GS}=0 (partial channel conduction) and V_{GS}=-10 V (no channel conduction) and the impact on V_{SD} and its temperature sensitivity is clearly observed [21].

Some challenges regarding instrumentation and real time measurement of junction temperature in SiC MOSFETs were evaluated in [22], however the objective of this paper is to evaluate how BTI will affect the performance and accuracy of TSEPs for determining the junction temperature of SiC MOSFETs. This will be presented in section III.

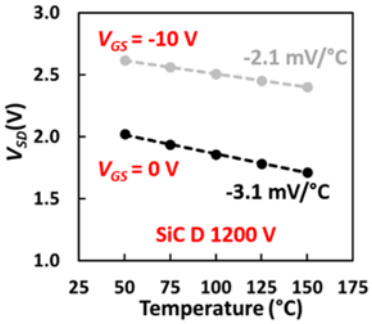

Fig. 5 Forward voltage V_{SD} of the body diode of a 1200 V SiC planar MOSFET as a function of temperature for different gate voltages. I_{SD}=50 mA

III. Bias Temperature Instability in SiC And Impact On TSEPs

Bias temperature instability simply refers to the process where traps in the gate dielectric are charged during MOS gate accumulation or inversion thereby resulting in a shift in the threshold voltage due to increase oxide, interface and near-interface traps, together with the wide bandgap of 3.3 eV of SiC, the narrow band offsets to the dielectric [8].

One of the main challenges affecting the adoption of SiC MOSFETs as the power semiconductor of choice in power applications is the reliability of the gate oxide [23]. Despite the improvements of the latest SiC power MOSFETs [24], threshold voltage shift caused by BTI and dielectric breakdown appear as reliability concerns for SiC power devices compared with Si power devices. A thorough comparison of different power devices under accelerated gate bias stress tests was presented in [25], were it was shown that the voltages required to damage the gate oxide are considerably higher for Si devices. In addition to the breakdown of the oxide, the shift of V_{TH} is a reliability concern which has implications on the application [7, 8]. These may be increased power losses due the increased ON-state resistance [8] or uneven current sharing during switching transients if the threshold voltage shift is different for devices connected in parallel [26, 27].

The application of a positive bias on the MOS gate results in an accumulation of electrons in the semiconductor adjacent to the gate dielectric thereby causing the trapping of negative charges and a concomitant increase in the threshold voltage since a greater positive voltage is required to overcome the negative charges. This is called positive bias temperature instability (PBTI). Likewise, the application of a negative bias on the MOS gate results in an accumulation of holes and a resultant decrease in the threshold voltage resulting from trapped positive charges in the oxide. This is called negative bias temperature instability (NBTI).

This phenomenon is well understood on silicon devices and improved oxidation, surface treatment and anneal processes have reduced the occurrence. However, in SiC power MOSFETs, as a result of the presence of carbon atoms during the oxidation of the semiconductor, the

increased oxide, interface and near-interface traps make NBTI and PBTI more active.

The threshold voltage shift recovers when the gate bias is removed and this recovery is accelerated if the gate is biased with the opposed polarity to the stress. The impact of stress time, temperature and recovery time are analyzed in [7-9, 28, 29]. To show the difference between SiC and Si devices, accelerated high temperature gate bias stresses have been performed on commercially available devices. The stress and relaxation schematic circuits are shown in Fig. 6. The objective of this recovery is to characterize only the non-recoverable shift of threshold voltage caused by the accelerated stress test and use the stressed device to evaluate the impact of V_{TH} shift on the TSEPs.

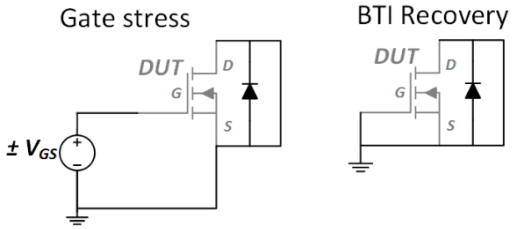

Fig. 6 Stress and recovery circuits for gate bias stress tests

For studying the impact of BTI the stresses applied were +40 V during 1 hour at 150 °C for the evaluation of PBTI and -40 V during 1 hour at 150 °C for the evaluation of NBTI. The voltage stresses are higher than the recommended values but are deemed suitable for show the differences between Si and SiC devices. The transfer characteristics of the devices were obtained using a curve tracer model 371B from Tektronix at ambient temperature before stress and after a relaxation period of 16 hours with the gate and source terminals shorted (V_{GS}=0). The measured transfer characteristics are shown in Fig .7(a) for SiC MOSFETs and Fig. 7(b) for Si IGBTs.

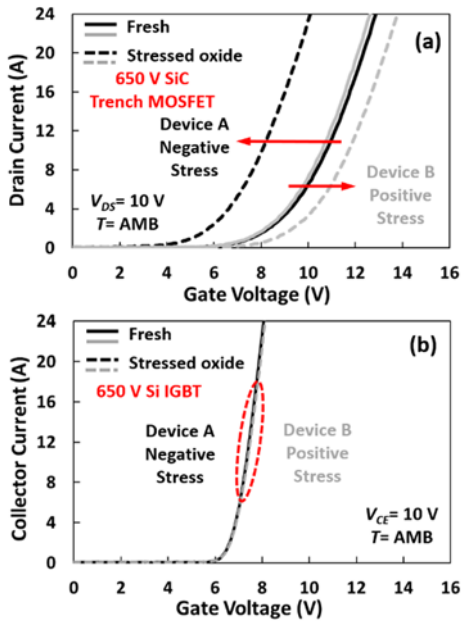

Fig. 7 BTI impact on transfer characteristics. (a) SiC MOSFET (b) Si IGBT

Comparing both figures it is clearly observed how in the case of Si IGBTs there is no shift of the transfer characteristics, whereas in the case of SiC MOSFETs a positive shift is observed for PBTI and a negative shift is observed for NBTI. In the TSEPs presented in section II, the threshold voltage plays a fundamental role, thereby the threshold voltage shift caused by gate biasing stress would have an impact on them, starting with the threshold voltage itself, as the transfer characteristics in Fig. 7(a) show.

It is important to make two remarks before evaluating the impact of BTI on TSEPs. First, capturing the real shift after nominal stress is difficult, as V_{TH} recovers after stress removal [7-9] and it is also affected by the measurement technique [8]. Second, the real shift of V_{TH} after stress can be higher than the V_{TH} shift measured some seconds after stress removal. In real time operation, with no time allowed to recover and characterization in the range of microseconds it may have a considerable impact as shown in [19], for the measurement of V_{TH} after a power pulse.

A. BTI and ON-state resistance

As described in section II, in SiC power MOSFETs the channel resistance has an important contribution to the total $R_{DS\text{-}ON}$. As R_{CH} is affected by the value of V_{TH}, it is expected that BTI has an impact on the output characteristics of SiC power MOSFETs. Fig. 8 shows the measured pre-stress and post-stress output characteristics of the SiC trench MOSFET subjected to PBTI stresses of +40 V at 150 °C during one hour. The output characteristics were measured at ambient temperature using a curve tracer Tektronix 371B. Fig. 8 shows a shift of the output characteristics, indicating an increase of the ON-state resistance, which is more apparent for V_{GS} = 12 V, as the contribution of the channel resistance is higher. From the output characteristics the calculated ON-state resistance is shown in Fig. 9. Similar measurements are shown in Fig. 10 and Fig. 11 for the NBTI stress of the SiC trench MOSFET (one hour biased at V_{GS}=-40 V and 150 °C).

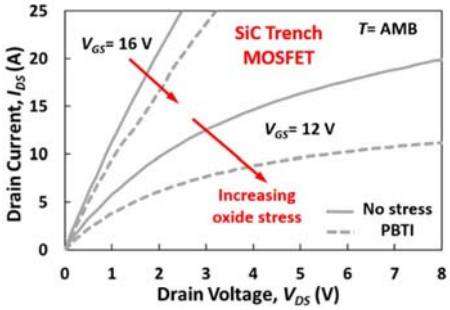

Fig. 8 Output characteristics of a SiC trench MOSFETs pre- and post- PBTI stress (+ 40 V at 150 °C during 1 hour)

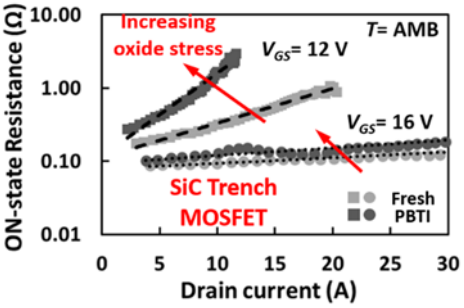

Fig. 9 $R_{DS\text{-}ON}$ as a function of current for a SiC trench MOSFET. PBTI stress (+ 40 V at 150 °C during 1 hour)

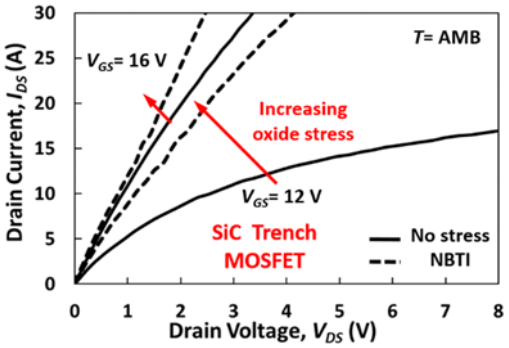

Fig. 10 Output characteristics of a SiC trench MOSFETs pre- and post- NBTI stress (-40 V at 150 °C during 1 hour)

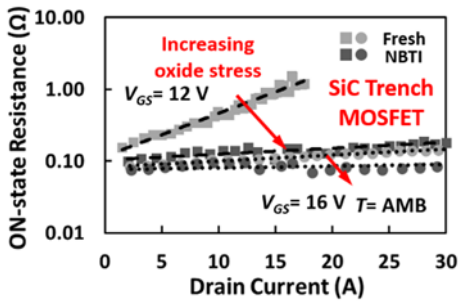

Fig. 11 $R_{DS\text{-}ON}$ as a function of current for a SiC trench MOSFET. NBTI stress (-40 V at 150 °C during 1 hour)

The results presented in Fig. 9 and Fig. 11 show how the ON-state resistance is affected by BTI, especially when the MOSFETs are driven at low gate voltages. As the ON-state resistance is a parameter that is usually monitored to indicate damage of the packaging during power cycling tests, this change of resistance may have a considerable impact on the evaluation of the measured results. This has been considered by different researchers for developing suitable methods for monitoring ON-state resistance during power cycling and decoupling the packaging degradation and the changes of electrical resistance of the chip [30].

In some cases, for monitoring the degradation of the packaging elements it can be considered to operate in the Zero Temperature Coefficient (ZTC), which is the point where the characteristics will not be affected by temperature. The change of the partial contribution of the channel resistance due to BTI in SiC MOSFETs will affect the ZTC point of the ON-state resistance as function of V_{GS}, as shown in Fig. 12, for a 900 V planar SiC MOSFET.

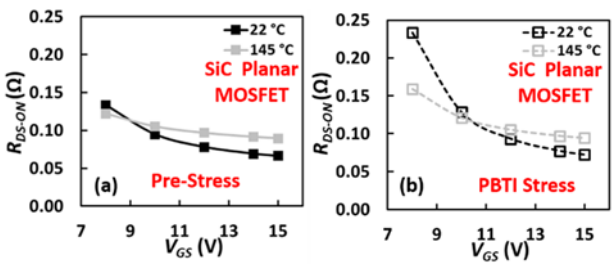

Fig. 12 $R_{DS\text{-}ON}$ as function of V_{GS} at 22 °C and 145 °C. (a) Before stress, (b) After PBTI stress

For this planar device, the PBTI stress was 35 V at 150°C and the characterization measurements were performed after 16 hours relaxation at V_{GS}=0, like in the case of the SiC Trench MOSFET. Fig. 12(a) shows the pre-stress ON-state resistance as function of V_{GS} for a SiC planar MOSFET, whereas Fig. 12(b) shows the same characteristics post-PBTI stress, which in both cases were characterized for a current of 50 mA, thereby in the ohmic region.

What is interesting to evaluate is how BTI would affect the accuracy of $R_{DS\text{-}ON}$ as temperature indicator. This is shown for NBTI and PBTI stress and a 650 V SiC trench and a 900 V SiC planar MOSFET in Fig. 13(a) and Fig 13(b) respectively, which shows the measured $R_{DS\text{-}ON}$ at a temperature of 145°C for different gate voltages.

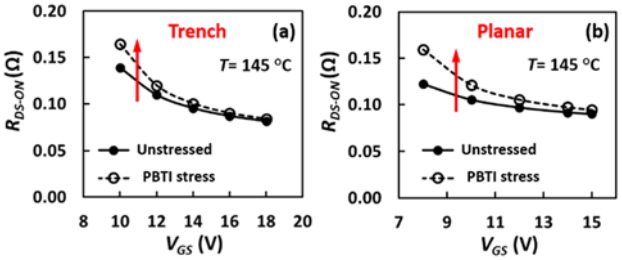

Fig. 13 Impact of PBTI on the ON-state resistance as function of the gate voltage (a) SiC Trench MOSFET, (b) SiC Planar MOSFET

The resistances were measured in the ohmic region using a low current and in both cases it is clearly observed how for high gate voltages the impact of BTI is minimized due to the lower contribution of R_{CH} to the total ON-state resistance. Increasing the partial contribution of R_{CH} makes the impact of BTI on $R_{DS\text{-}ON}$ more apparent, resulting in lower accuracy of $R_{DS\text{-}ON}$ as temperature indicator at low V_{GS} values. This is more apparent for the planar MOSFET, indicating a higher impact of BTI.

From the results in Fig. 9 and Fig 11, it is also observed how the value of the drain current may have an impact on the measured ON-state resistance, which is minimized if the devices are driven with high V_{GS} values. In addition to the impact of BTI on $R_{DS\text{-}ON}$ as temperature indicator, this change of $R_{DS\text{-}ON}$ may have a considerable impact on power cycling, as it can affect the losses and the junction temperature excursion during the experiments.

B. BTI and switching rate of the drain current

The shift of the transfer characteristics due to BTI shown in section II indicates a clear impact on the dynamic/transient characteristics of SiC MOSFETs, thereby it is important to assess its impact on dynamic TSEPs like the switching rate of the drain current. To that end, the turn-ON transients were measured as a function of temperature pre- and post-stress using a conventional double pulse test setup.

The gate stresses were +40 V during one hour at 150 °C for PBTI and -40 V during one hour at 150 °C for NBTI, characterizing the transients after 16 hours relaxation time at V_{GS}=0. Fig. 14(a) shows the measured turn-ON transients before and after PBTI stress, whereas Fig. 14(b) shows the measured transients for NBTI stress. In both cases the transients were measured at a temperature of 23 °C. As shown in Fig. 14(a), a rightwards shift caused by PBTI is observed together with a reduction of the switching rate. In the case of NBTI, shown in Fig. 14(b), a

leftwards shift is observed in the turn-ON transient together with a clear increase of the switching rate. Comparing both figures, the impact of NBTI is more apparent.

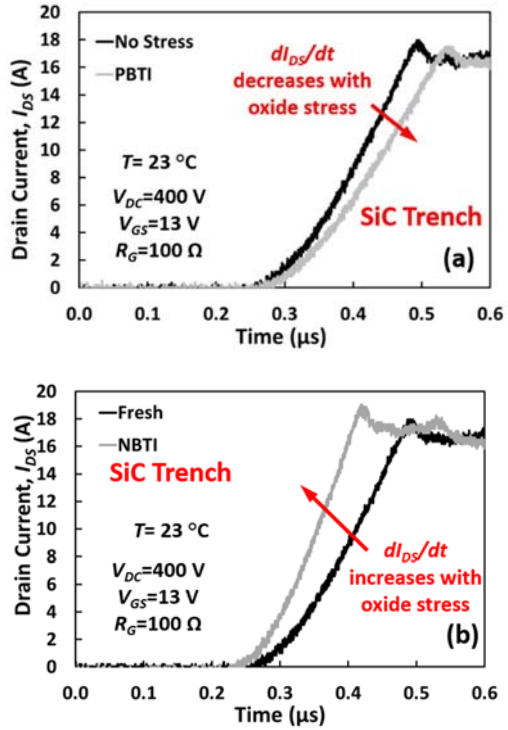

Fig. 14 SiC Trench MOSFET – (a) Impact of PBTI on the drain current turn-on transient (b) Impact of NBTI on the drain current turn-on transient

An interesting observation is that due to this shift, the measured transient can be the same for two different temperatures, as shown in Fig. 15. The temperature was defined using a small heater attached to the discrete device, waiting enough time to reach a steady state and assume thermal equilibrium.

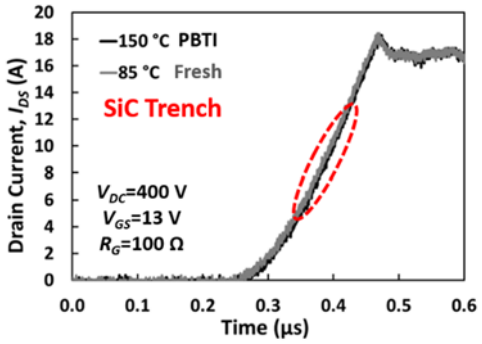

Fig. 15 SiC Trench MOSFET – Overlapping turn-ON current transients at different temperatures caused by PBTI

The results in Fig. 14 indicate that the accuracy of the TSEP will be affected by BTI, as the switching rate will be affected by the threshold voltage shift. The differences on the measured dI_{DS}/dt (measured using a gate resistance R_G=100 Ω and a gate voltage V_{GS}=13 V) are summarized in Table I. The accelerated stress tests shows a considerable impact of BTI on the switching transients, especially in the case of NBTI.

Table I SiC Trench – Impact of BTI stresss on the measured dI_{DS}/dt during turn-ON (I_{DS}=16 A, T= 23 °C)

	Switching Rate Unstressed (A/µs)	Switching Rate Stressed (A/µs)	Difference (%)
PBTI	83.9	73.4	-12.6
NBTI	84.9	115.4	+35.9

C. BTI and gate voltage plateau

Similar to the switching rate of the drain current during turn-ON, the gate voltage plateau V_{GP} is also affected by BTI. Fig. 16 shows the gate voltage transients measured at a temperature of 85 °C for the unstressed and PBTI-stressed SiC trench MOSFET, where it is clearly observed that V_{GP} increases after PBTI stress due to the higher V_{TH}.

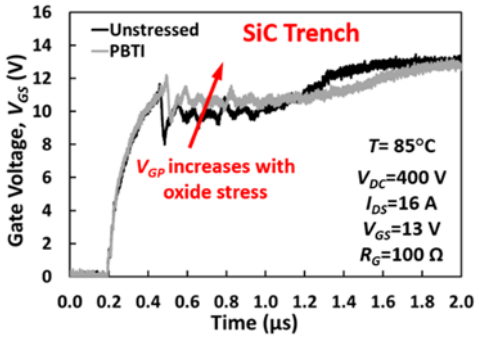

Fig. 16 Impact of PBTI on the gate voltage turn-ON transient. SiC Trench MOSFET

The use of parameters accessible from the gate driver (like V_{GP}) are interesting from the point of view of condition monitoring, as the measuring circuits will be easy to implement [11]. However, from the results shown in Fig. 16 (where two different V_{GP} values are observed for the same temperature) and Fig. 17 (where the same V_{GP} is obtained for different temperatures) the use of TSEPs depending on V_{TH} will be challenging for SiC MOSFETs. The measured gate voltage transients in Fig. 17 correspond to the drain current transients in Fig. 15.

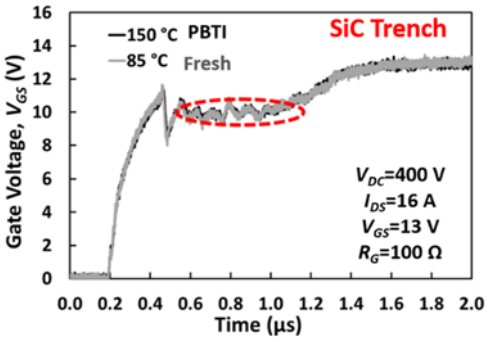

Fig. 17 Overlapping gate voltage turn-ON transients at different temperatures caused by PBTI

D. BTI and body diode voltage

As mentioned in section II, to completely remove the dependency of V_{SD} on V_{GS}, it is necessary to bias with a high magnitude negative V_{GS} to ensure that the channel is closed and no coupling exists between the body diode and the MOSFET channel. In SiC MOSFETs, the body effect is more evident because of the high V_{SD} compared to

silicon (due to the wide bandgap) [21]. This means that the V_{SD} depends on the V_{TH} hence, using V_{SD} as a TSEP requires careful consideration since a change in V_{TH} through BTI will affect the calibrated temperature sensitivity of V_{SD}.

To evaluate this, SiC trench MOSFETs were subjected to cumulative PBTI and NBTI stresses. Device A (PBTI) was subjected to two stages of +35 V at 150 °C for 30 minutes whereas device B (NBTI) was subjected to two stages of -35 V at 150 °C for 30 minutes. Each stress phase was followed by a 16 hour recovery at V_{GS}=0, characterizing V_{SD} as TSEP afterwards. The current used was 50 mA and the results are shown in Fig. 18(a) for PBTI and Fig. 18(b) for NBTI.

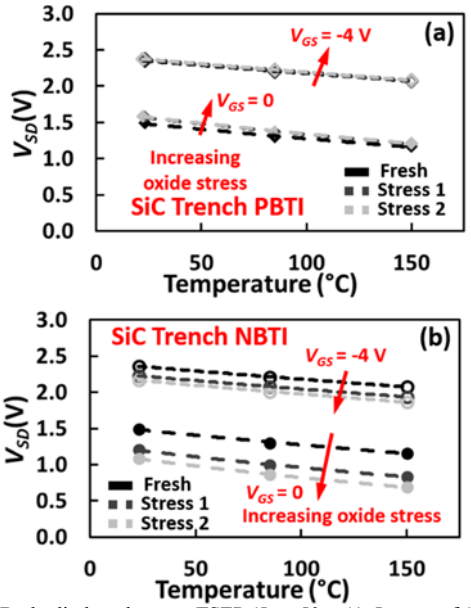

Fig. 18 Body diode voltage as TSEP (I_{SD}= 50 mA). Impact of (a) PBTI (b) NBTI

As it was already demonstrated in [19], and shown in Fig .18(a), biasing the device with a negative gate voltage minimizes the impact of PBTI on the accuracy of V_{SD} as TSEP. In the case of NBTI, in Fig. 18(b), a higher negative voltage would be required to fully close the channel, as the rated gate voltage does not eliminate the impact of NBTI.

IV. Review of Power Cycling Strategies for SiC

Power cycling is a useful tool for obtaining lifetime estimation of power modules and understand the failure mechanisms and weaknesses of the packaging system. Researchers have proposed different strategies and topologies for power [31, 32].

The first challenge of power cycling SiC devices arises from its different thermomechanical properties, resulting in higher stresses on the packaging materials and a reduced lifetime if the packaging system is not improved, as traditional packaging methods were designed for silicon devices [33, 34]. In addition to this, the shift of V_{TH} due to BTI can have serious consequences in power cycling tests, including the junction temperature measurement using TSEPs and variation of power losses, as the ON-state resistance is affected by BTI.

The area of power cycling of SiC power devices has recently been very active, starting with the proposal of the body diode as TSEP using a negative gate voltage and the use of $R_{DS\text{-}ON}$ at high positive voltages for heating up the device [19]. The impact of the negative bias during junction temperature measurement has been evaluated in [35], where a methodology for compensation has been proposed. Monitoring both the degradation of the wire-bonds and the impact of PBTI on $R_{DS\text{-}ON}$ during power cycling has been subject of different analysis and circuits have been proposed for monitoring both resistances during the accelerated lifetime tests [30, 36, 37]. The presence of Schottky diodes in SiC power modules, requires eliminating the additional external diode from the current path [37] or the use of optical temperature sensors [37, 38], which also eliminates the drift of TSEPs caused by BTI.

V. Conclusions

In this paper the use of TSEPs in SiC has been reviewed. It has been show how the V_{TH} shift caused by BTI affects the accuracy of $R_{DS\text{-}ON}$, the drain current and gate voltage transients during turn-ON and the body diode voltage as TSEPs. It has been shown that if the contribution of R_{CH} to the total ON-state resistance is minimized driving the devices at high V_{GS} values, the impact of BTI is minimized, however it cannot be neglected in the whole range of gate voltages. In the case of the switching transients, it is possible to obtain the same transient at different temperatures. Currently there is plenty of research activity in the area of power cycling for SiC MOSFETs, with the aim of addressing the impact of BTI on junction temperature measurement and power losses during power cycling. An example is the use of the well-stablished body diode voltage as TSEP, which requires a negative gate voltage for eliminating the impact of PBTI.

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