

# A Wideband Power Amplifier MMIC Utilizing GaN on SiC HEMT Technology

Charles Campbell, *Senior Member, IEEE*, Cathy Lee, Victoria Williams, Ming-Yih Kao, *Senior Member, IEEE*, Hua-Quen Tserng, *Life Fellow, IEEE*, Paul Saunier, *Senior Member, IEEE*, and Tony Balisteri

**Abstract**—The design and performance of a wideband power amplifier MMIC suitable for electronic warfare (EW) systems and other wide bandwidth applications is presented. The amplifier utilizes dual field plate 0.25- $\mu\text{m}$  GaN on SiC device technology integrated into the three metal interconnect (3 MI) process flow. Experimental results for the MMIC at 30 V power supply operation demonstrate greater than 10 dB of small signal gain, 9 W to 15 W saturated output power and 20% to 38% peak power-added efficiency over a 1.5 GHz to 17 GHz bandwidth.

**Index Terms**—Distributed amplifier, gallium nitride (GaN), MMIC, power amplifier.

## I. INTRODUCTION

MODERN electronic warfare systems specify amplifiers with high power, wide bandwidth and high efficiency. Until recently, solid-state monolithic amplifier solutions have been capable of addressing this need for only modest output power levels. System designers have had to rely on TWT based power amplifiers to achieve order of magnitude increases in output power over available solid-state devices. Wideband power amplifiers MMICs are also in demand for the test equipment market as well as general use.

To better serve these requirements researchers have developed power amplifier MMICs utilizing the nonuniform distributed power amplifier (NDPA) approach [1]–[5]. Impressive results have been published in both GaAs and GaN based semiconductor technologies. The achievable output power with the NDPA approach is proportional to  $V_d^2/R_L$  where  $V_d$  is the power supply voltage and  $R_L$  is the load impedance that the amplifier is driving. The output power of the amplifier may be increased by designing it to operate with a higher power supply voltage or to drive a lower load impedance.

If the power supply voltage is limited by the transistor technology being used then designing the NDPA for a lower load impedance is a viable option. Of course if the amplifier is ultimately to be operated in a 50  $\Omega$  system, impedance transforming networks will be required which may reduce the overall gain, bandwidth and output power of the circuit. A recent example of this approach was reported by Meharry *et al.* [1]. The two-stage power amplifier MMIC combines four NDPA sections designed

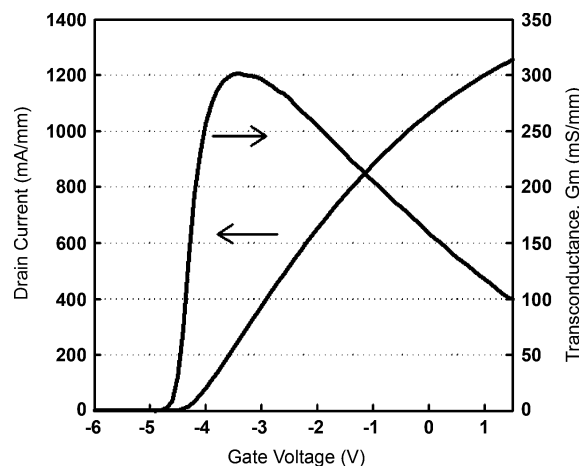


Fig. 1. DC transfer characteristics of GaN HEMT.

to drive a 3  $\Omega$  load impedance with a wideband impedance transforming network that brings the output impedance back to 50  $\Omega$ . Measured results under pulsed power conditions for the MMIC demonstrate 4 W output power and 20% to 30% power-added efficiency (PAE) over a 4–18 GHz bandwidth using a GaAs PHEMT process operated at 5 V.

The other option for increasing output power is to use a high voltage transistor technology and a correspondingly higher power supply voltage. Modern GaN transistors are well suited for this application allowing a near order of magnitude increase in power supply voltage while delivering similar gain and efficiency performance as GaAs PHEMT devices [6]. Recently, results for a wideband GaN NDPA MMIC were published by Gassmann *et al.* [2]. Measured continuous wave (CW) data for this MMIC demonstrate 5 W to 7 W output power and 19% to 32% PAE over a 2–15 GHz bandwidth for 20 V power supply operation. In this paper the design and measured CW performance of a GaN on SiC NDPA MMIC covering a 1.5 to 17 GHz frequency range are presented.

## II. DEVICE TECHNOLOGY

The AlGaIn/GaN MMIC was fabricated entirely with the TriQuint Semiconductor baseline process on the 3-inch GaN on SiC manufacturing line. The epitaxial structure has a Si GaN buffer with advanced Fe-doping for improved isolation. An AlN spacer was inserted between the buffer and the AlGaIn schottky barrier layer. The surface was terminated by a GaN cap layer for better leakage performance.

The active device epitaxial layers were isolated by performing mesa etch down to the GaN buffer. The ohmic

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The authors are with TriQuint Semiconductor, Richardson, TX 75080 USA (e-mail: ccampbell@tqs.com).

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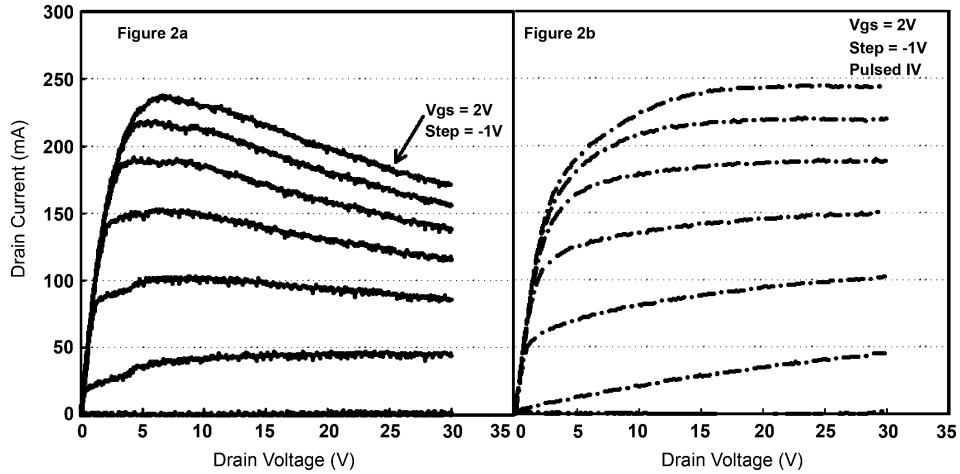


Fig. 2. DC and pulsed IV characteristics of GaN HEMT.

source-drain spacing was  $4 \mu\text{m}$  with nominal contact resistance of  $0.5 \Omega \text{ mm}$ . The contacts were formed by alloying a Ti/Al/Mo/Ti/Au metal stack at  $850^\circ\text{C}$ . The gate-length was defined by patterning and etching a  $0.25 \mu\text{m}$  opening in the  $\text{SiN}_x$ . A second patterning and subsequent metallization over the etched  $\text{SiN}_x$  opening completes the gate metal and forms an integrated field-plate. In addition, a source-connected second field-plate (2FP) was implemented to reduce the high-field related device degradation. The distance from the source to the 2FP was selected to improve the PAE and gain at high voltage. For backside via, the SiC wafers were ground and polished to  $100 \mu\text{m}$ , and the GaN/SiC vias were etched in an ICP-RIE process. Finally, the backside ground plane was plated with  $> 4 \mu\text{m}$  of Au.

The DC transfer characteristics are measured at  $V_{DS} = 10 \text{ V}$  and  $V_{GS} = -7 \text{ V}$  to  $1.5 \text{ V}$ . Median threshold voltage was  $-4.2 \text{ V}$  with standard deviation of  $0.35 \text{ V}$  across four wafers. The maximum dc transconductance was  $300 \text{ mS/mm}$ . Maximum drain current at  $V_{GS} = 1.5 \text{ V}$  was  $1.2 \text{ A/mm}$ . A typical transfer curve is shown in Fig. 1. The Schottky forward turn-on voltage was  $1.3 \text{ V}$  at  $1 \text{ mA/mm}$  and reverse two-terminal breakdown voltage was greater than  $80 \text{ V}$  for  $I_{GD} = 5 \text{ mA/mm}$ . Typical three-terminal  $V_{BVDs}$  is  $60 \text{ V}$  for  $I_{DS} = 5 \text{ mA/mm}$ .

The DC IV characteristics of a  $200 \mu\text{m}$  FET are plotted in Fig. 2(a). The peak drain current was measured at  $V_{GS} = 2 \text{ V}$  and the device is completely pinched off at  $V_{GS} = -4 \text{ V}$  and  $V_{DS} = 30 \text{ V}$ . The thermal-related droop starts to impact the device when the gate is biased at  $-1 \text{ V}$  or higher as shown the figure. The pulsed IV performance is routinely monitored as part of the statistical process control. Fig. 2(b) shows a representative pulsed IV plot measured with a DIVA system. Each measurement is pulsed from a quiescent bias condition of  $V_{GS} = -5 \text{ V}$  and  $V_{DS} = 30 \text{ V}$ . The data shows that pulsing from a completely pinched off state to a fully-on state, results in minimal current collapse and  $I_{DS}$  of  $1.2 \text{ A/mm}$  is achieved.

The peak  $f_T$  measured at  $V_{DS} = 20 \text{ V}$  is  $25 \text{ GHz}$  and  $10 \text{ GHz}$  load pull data at  $40 \text{ V}$  drain bias for  $4 \times 100 \mu\text{m}$  FET cells consistently shows  $7.5 \text{ W/mm}$ ,  $65\%$  PAE, and  $14 \text{ dB}$  of associated power gain. For a typical amplifier bias condition of  $30 \text{ V}$ – $200 \text{ mA/mm}$ ,  $f_T$  and  $f_{max}$  are nominally  $25 \text{ GHz}$  and

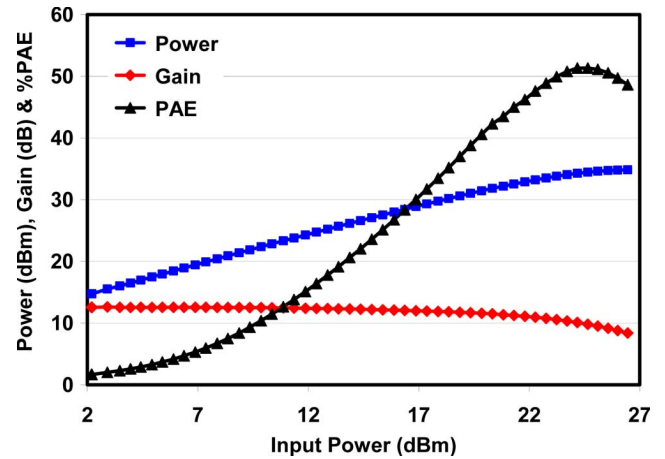


Fig. 3. 18 GHz load pull results at  $40 \text{ V}$  bias.

$105 \text{ GHz}$ , respectively. Load pull data under continuous wave conditions at  $18 \text{ GHz}$  is plotted in Fig. 3 for a  $4 \times 100 \mu\text{m}$  FET with a  $40 \text{ V}$  drain bias and  $100 \text{ mA/mm}$  quiescent current. The results demonstrate greater than  $50\%$  PAE with an associated  $6.2 \text{ W/mm}$  output power and  $10 \text{ dB}$  power gain.

### III. CIRCUIT DESIGN

As discussed in Section I, the NDPA topology was selected for this design. Theoretical details regarding this architecture are well described in the literature and will not be repeated here [3], [4]. A simplified schematic diagram for the basic NDPA circuit is shown in Fig. 4. The approach is to taper the drain line characteristic impedances,  $Z_{o,n}$  to better maintain a near optimum load for all of the FET cells. Under the following simplifying assumptions an approximate analysis of the circuit shown in Fig. 4 can be performed to provide an initial estimate for the drain transmission line impedances. First, the transmission line lengths can be adjusted such that the transistor currents add in-phase, and second, the FET output capacitance  $C_p$  can be absorbed into the transmission lines. Given the simplifying assumptions the output of the  $n$ th transistor in the amplifier can be

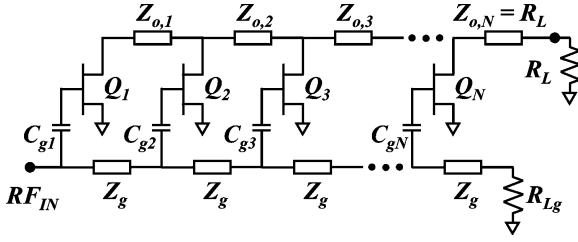


Fig. 4. Basic NDPA topology.

modeled as shown in Fig. 5. Summing the currents at the drain node and solving for the load impedance presented to the FET

$$R_{p,n} = \frac{V}{-I_{Qn}} = Z_{o,n} \left( 1 + \frac{\sum_{i=1}^{n-1} I_{Qi}}{I_{Qn}} \right) = Z_{o,n} \left( \frac{\sum_{i=1}^n W_{Qi}}{W_{Qn}} \right). \quad (1)$$

Note that in (1) transistor current has been replaced by device periphery. This is a valid substitution if all transistors are biased the same and driven equally. Normalizing the load impedances in (1)

$$R_p(\Omega \cdot \text{mm}) = R_{p,n} W_{Qn} = Z_{o,n} \sum_{i=1}^n W_{Qi}. \quad (2)$$

Presumably the normalized optimum load resistance is a known quantity for the process and is extracted from load pull data. Solving (2) for the unknown characteristic impedances results in the following:

$$Z_{o,n} = \frac{R_p(\Omega \cdot \text{mm})}{\sum_{i=1}^n W_{Qi}}. \quad (3)$$

For transistor closest to the output ( $n = N$ ),  $Z_{o,N} = R_L$  and (3) reduces to the following:

$$\frac{R_p(\Omega \cdot \text{mm})}{R_L} = \sum_{i=1}^N W_{Qi}. \quad (4)$$

This is the expected result. At low frequency the individual FET optimum load resistances,  $R_{p,n}$  will combine in parallel and this parallel combination should be equal to the load impedance  $R_L$  to maximize the output power of the amplifier. In other words, given the normalized optimum load resistance the total FET periphery will be constrained by (4) for an optimally matched design. This constraint on the total transistor periphery is also a constraint on the output power of the amplifier. Transforming the load impedance to a lower value allows for increased periphery and a corresponding increase in output power.

Consider the 10 cell example shown in Table I where two different cases have been analyzed. The first case utilizes equal periphery FET cells and illustrates a fundamental problem. Due to the high voltage operation of GaN devices, FET cells typical

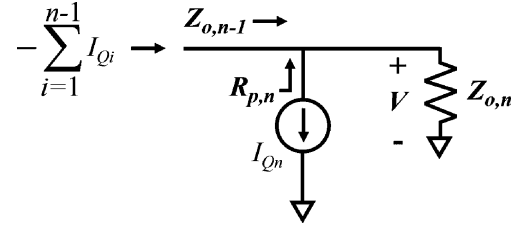


Fig. 5. Simplified FET output model.

of the frequency range of interest can easily have normalized  $R_p$  exceeding 100  $\Omega$ . Unfortunately, it is difficult to realize microstrip transmission lines with characteristic impedances much greater than about 120  $\Omega$  with the existing GaN on SiC process. The first transmission line for the equal cell size case is completely unrealizable. This transistor will be poorly loaded and will operate at reduced output power and efficiency. The situation can be improved by making the first FET cell larger than those that follow, effectively limiting the maximum transmission line impedance in the circuit [4]. One can far better approximate the characteristic impedance of the first transmission line for the unequal FET size case. The estimated output power shown in Table I is calculated assuming a sine wave output as  $V_d^2/2R_L$ .

Typically NDPA designs utilize capacitors in series with the gate of each FET cell to increase the cut-off frequency of the composite gate transmission line at the expense of gain. The series capacitor values should also be tapered to equalize the RF drive voltage present at the gate of each transistor. A high value resistor will have to be placed in parallel with each gate capacitor to provide a gate bias path for the FETs.

A design goal for this MMIC was to achieve a 10:1 bandwidth including X-band and as much of Ku-band as possible. It was determined that a 10 cell design optimized the small signal gain over this frequency range [3]. Utilizing (3), an approximate analysis for the case of a 35  $\Omega$  load impedance is shown in Table II. The first cell is sized at 520  $\mu\text{m}$  with the remaining 9 cells sized at 320  $\mu\text{m}$  each for a total periphery of 3.4 mm. The strategy is to use a quarter wave transmission line, centered near the upper band edge, to transform the 50  $\Omega$  load to 35  $\Omega$ . This approach will peak up the output power and efficiency at the upper band edge while sacrificing some performance at lower frequencies. This trade-off is reasonable because the transistor technology has better performance and the matching network exhibits lower loss at low frequency. Using the data shown in Table II as a starting point the circuit was optimized with AWR Microwave Office utilizing nonlinear EEHEMT models fit to pulsed IV, small signal s-parameter and load pull data. The matching networks and drain bias circuits were then finalized by extensive EM simulation with the Sonnet EM software package.

Circuits were fabricated with the TriQuint Semiconductor three-metal interconnect (3MI) process which features high density capacitors (1200 pF/mm<sup>2</sup>), thick plated lines (6.77  $\mu\text{m}$ ) and capacitors constructed directly over substrate vias. A photograph of the completed MMIC is shown in Fig. 6; the circuit dimensions are 5.54 mm  $\times$  2.77 mm. A schematic diagram of the circuit is shown in Fig. 7.

TABLE I  
TEN CELL NONUNIFORM DISTRIBUTED PA EXAMPLE

NDPA Example	FET	Equal FET Sizes		Unequal FET Sizes	
	Number	WQ(mm)	Zo (Ohm)	WQ(mm)	Zo (Ohm)
FET Rp (Ohm-mm) = 120	1	0.24	500	0.60	200
RL (Ohm) = 50	2	0.24	250	0.20	150
Total FET Width (mm) = 2.4	3	0.24	167	0.20	120
Number of Cells = 10	4	0.24	125	0.20	100
Supply Voltage (V) = 30	5	0.24	100	0.20	86
Max RF Power (W) = 9.0	6	0.24	83	0.20	75
	7	0.24	71	0.20	67
	8	0.24	63	0.20	60
	9	0.24	56	0.20	55
	10	0.24	50	0.20	50

TABLE II  
TEN CELL NONUNIFORM DISTRIBUTED PA DESIGN

GaN NDPA Design	FET	WQ(mm)	Rp (Ohm)	Zo (Ohm)
FET Rp (Ohm-mm) = 120	1	0.52	231	231
RL (Ohm) = 35	2	0.32	374	139
Total FET Width (mm) = 3.4	3	0.32	374	102
Number of Cells = 10	4	0.32	374	80
Supply Voltage (V) = 30	5	0.32	374	66
Max RF Power (W) = 12.9	6	0.32	374	56
	7	0.32	374	49
	8	0.32	374	43
	9	0.32	374	39
	10	0.32	374	35

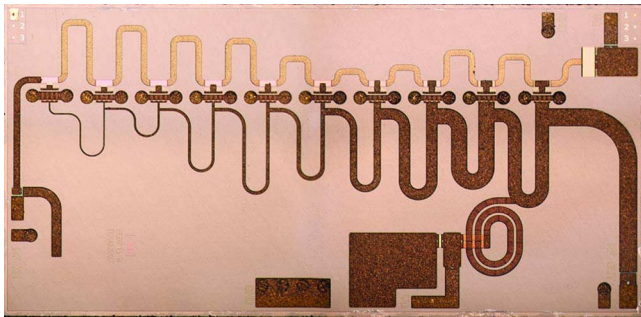


Fig. 6. Photograph of the NDPA MMIC.

#### IV. MEASURED RESULTS

Completed wafers were 100% DC and RF tested at TriQuint Semiconductor's on-wafer test facility. The RF tests performed on-wafer are small signal *s*-parameters and pulsed power, both at a quiescent condition of 30 V–500 mA. On-wafer *s*-parameter data for 294 amplifier MMICs are shown in Fig. 8. The on-wafer *s*-parameter results indicate 10 dB to 14 dB typical small signal gain over a 2–18 GHz frequency range. Pulsed power and efficiency data collected on-wafer is plotted in Fig. 9 for 231 devices. The power data was collected at a constant +30 dBm input power level which is the maximum presently available for the on-wafer test system over a 2–18 GHz instantaneous bandwidth. The drain bias voltage is pulsed from 0 V to 30 V with a 10  $\mu$ s pulse width running at 10% duty cycle. Due to test time considerations the on-wafer pulsed power data was collected from 2 GHz to 18 GHz in 4 GHz steps, therefore it is difficult to

assess the characteristics of the band edges between 2–6 GHz and 14–18 GHz. The PAE is greater than 21% from 2–14 GHz and the output power is typically 9 W to 10 W from 6–14 GHz.

A particularly sensitive circuit element in the design was the drain bias choke. The inductance of the choke sets the low frequency cutoff for the amplifier, however, if the choke is physically too large then high frequency performance is compromised. The low frequency impedance of the bias choke is the cause of the gain roll-off and increase in output return loss at the low end of the band evident in Fig. 8. Furthermore, the choke has to be able to reliably support over 1000 mA of bias current. Therefore, particular attention was given to design and EM simulation of the bias spiral inductor. To improve the quality factor of the choke a rounded design was selected. The spiral is constructed with air bridge metal suspended about 2  $\mu$ m above the substrate to increase the self resonant frequency of the inductor. A 3-D rendering of the bias choke layout is shown in Fig. 10. Measured versus modeled data for a fabricated bias choke test circuit is plotted in Fig. 11 and shows very good agreement between experiment and simulation.

To facilitate a more accurate comparison to the measured results, the AWR AXIEM EM tool was used to simultaneously EM simulate a large portion of the MMIC. A rendering of what this simulation encompasses is shown in Fig. 12. Models for the FETs, bias choke and RF interconnect structures are connected to the 32-port EM simulation at the appropriate locations. All comparisons between experiment and simulation that follow utilize the AXIEM EM simulation model.

Singulated, DC and RF good MMICs were soldered to 40-mil-thick Cu-Moly carriers which were screwed down to

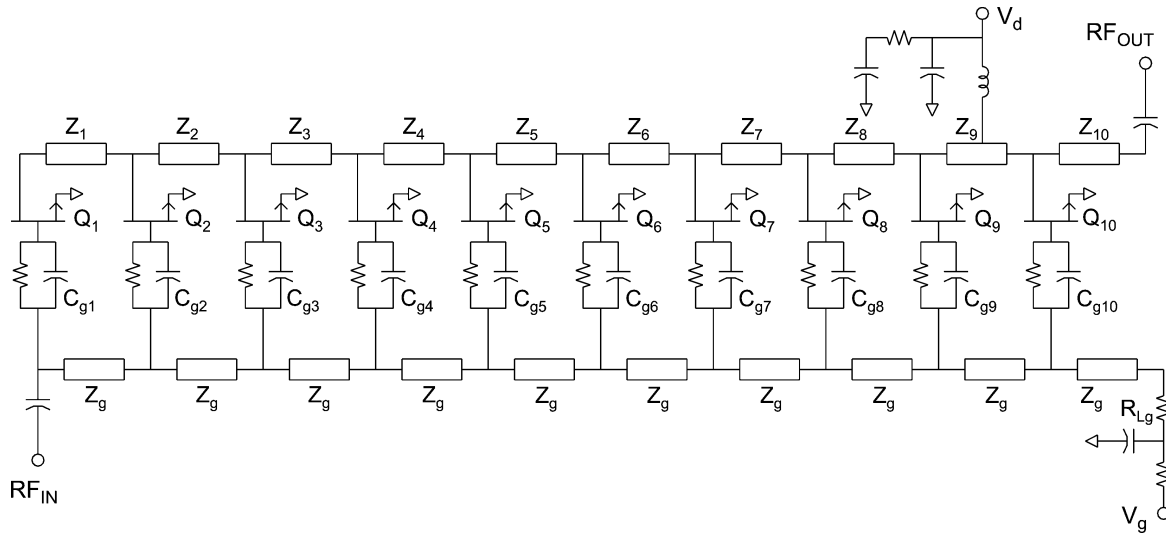


Fig. 7. Schematic diagram of the NDPA MMIC.

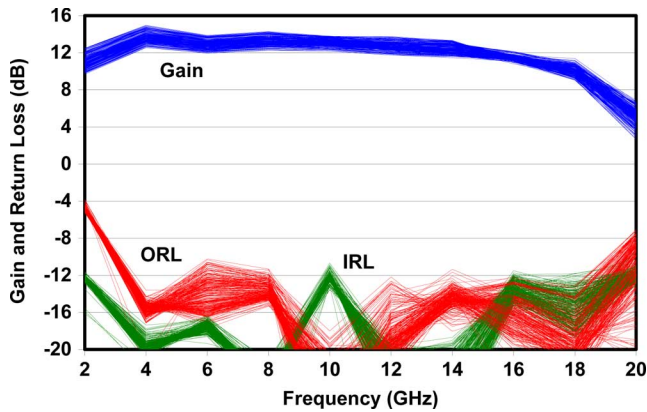


Fig. 8. On-wafer s-parameters.

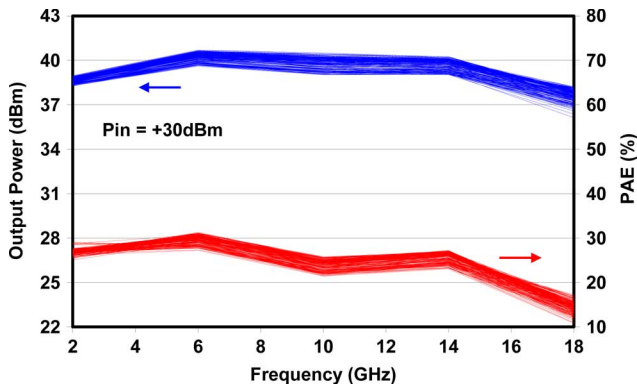


Fig. 9. On-wafer pulsed power.

an Aluminum test fixture with an intervening layer of Indium foil. Alumina  $50\ \Omega$  de-embedding lines 470-mil-long were connected to the RF ports of the MMIC with two 25-mil-long bondwires. The far ends of the de-embedding lines were contacted with 2.9 mm connectors which can be calibrated out of the measurements. A photograph of the test fixture is shown in Fig. 13. The entire test fixture was mounted to an Aluminum heat sink with thermal grease. Temperature measurements of the carrier plate surface indicated that this arrangement maintained about a  $+30^\circ\text{C}$  base plate temperature for the MMIC.

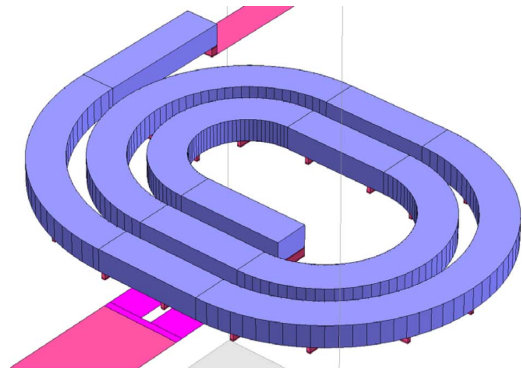


Fig. 10. Layout of drain bias choke circuit.

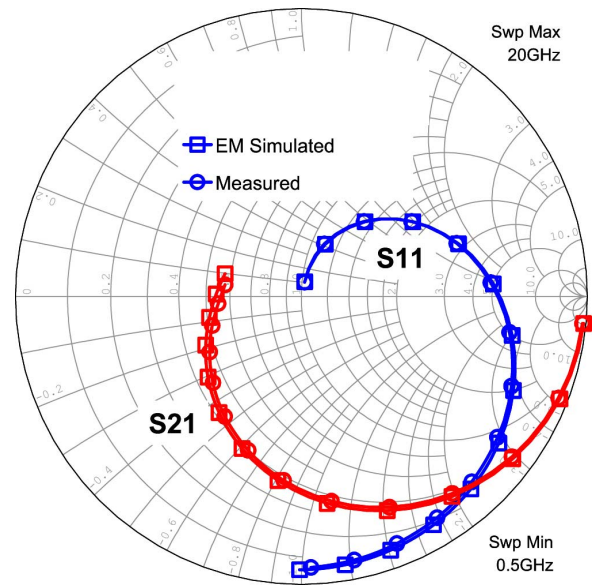


Fig. 11. Measured versus modeled results for the drain bias choke.

The amplifier MMICs are nominally biased at 30 V and 500 mA. Measured results for the small signal gain and return loss are shown in Fig. 14 for a sample of eight amplifiers. The simulated small signal gain is shown as the broken line and is in good agreement with the measured results. The measured



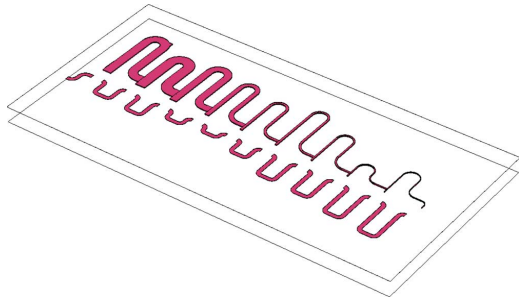


Fig. 12. 32-port AXIEM EM simulation.

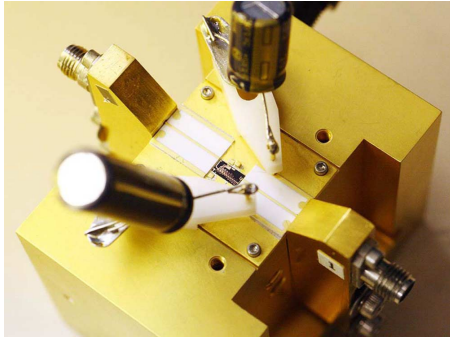


Fig. 13. Test fixture assembly.

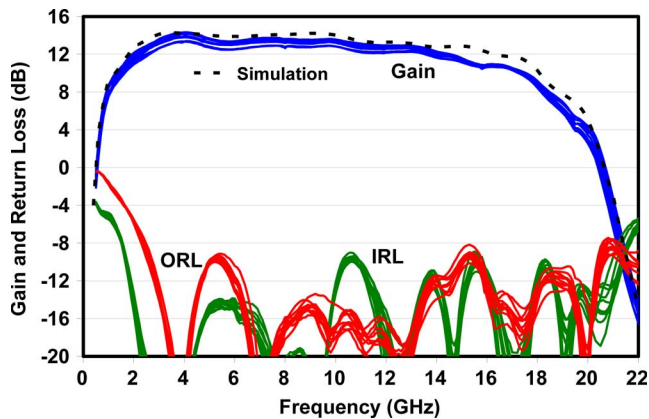


Fig. 14. 30 V small signal gain and return loss.

small signal gain is typically greater than 10 dB from 1.5 GHz to 17 GHz.

Measured results for output power and efficiency with +32 dBm CW input power are shown in Fig. 15 for a sample of six amplifiers. The simulated results are shown as broken lines and are in reasonably good agreement with experiment. Possible causes for the observed measured versus modeled discrepancies are many including inaccuracies in the nonlinear model, harmonic terminations and coupling between the RF structures not accounted for in the EM simulations. The output power is typically greater than 8 W over a 1.5 GHz to 17 GHz frequency range with a peak value of 13 W occurring at about 5 GHz. The associated power added efficiency is typically greater than 20% with a maximum value of 38%. The power gain at 32 dBm input power varies between about 7 dB and 9 dB. Power and efficiency data versus input power for one of the amplifiers is plotted in Fig. 16 over a subset of frequencies.

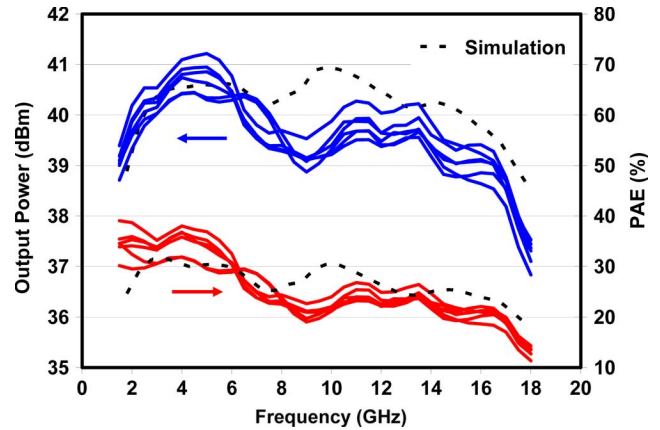


Fig. 15. +30 V CW power data at 32 dBm input power.

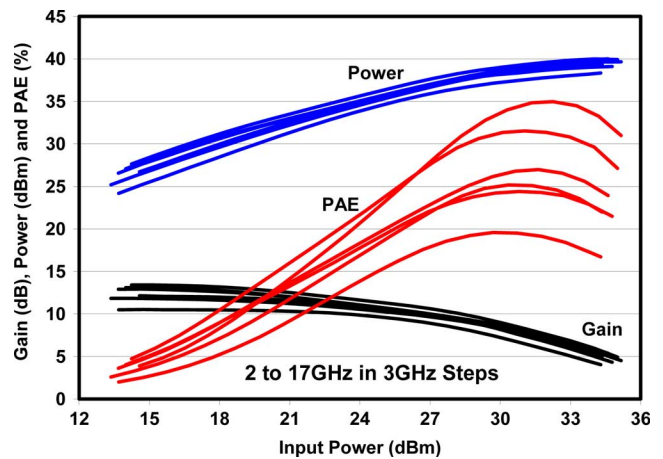


Fig. 16. +30 V CW power data versus input power.

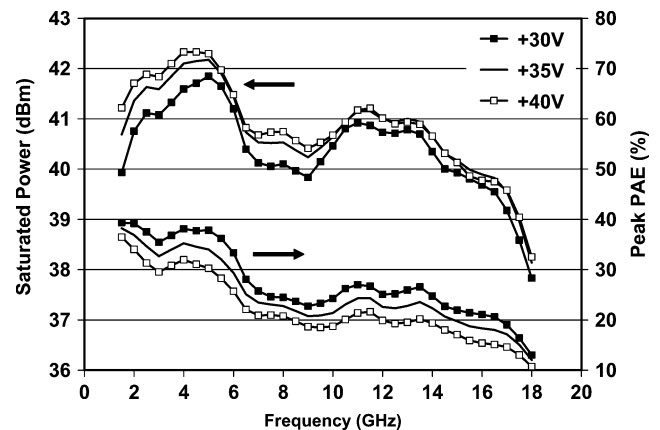


Fig. 17. CW power data versus supply voltage.

The observed compression curves are well behaved with no evidence of kink, odd-mode or driven oscillations. Saturated CW output power and peak power added efficiency for 30 V, 35 V and 40 V power supply voltages are shown in Fig. 17. In general, increasing the supply voltage from 30 V to 35 V produces an increase in output power of 0.3 dB to 0.5 dB with a corresponding 2% point penalty in efficiency. Further increasing the supply voltage to 40 V does little good and actually results in a reduction of output power at the upper end of the frequency band.

## V. CONCLUSION

The design and performance of a 1.5–17 GHz nonuniform distributed power amplifier MMIC has been presented. The device utilizes 0.25  $\mu\text{m}$  dual field plate GaN on SiC transistor technology and was processed with the baseline TriQuint Semiconductor three-metal interconnect flow. For the 1.5–17 GHz band, experimental results demonstrate 9 W to 15 W saturated output power with an associated PAE typically above 20%. To the authors' knowledge, these results are among the highest reported for a monolithic solid-state power amplifier covering this frequency range.

## ACKNOWLEDGMENT

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**Charles Campbell** (S'85–M'87–SM'06) was born in Evanston, IL, in 1965. He received the B.S.E.E., M.S.E.E., and Ph.D. degrees from Iowa State University, Ames, IA, in 1988, 1991, and 1993, respectively.

From 1993 to 1998, he was with Texas Instruments, Dallas, TX, involved with microwave module design and MMIC development. Since 1998, he has been with the Texas division of TriQuint Semiconductor where he has held positions of Design Team Leader, Design Engineering Director, and most recently, Design Engineering Fellow. His interests

are compact, high-power MMIC design techniques and device modeling.

**Cathy Lee** received the B.S.E.E. and M.S.E.E. degrees from the University of Illinois at Urbana-Champaign in 1997 and 2000, respectively.

She joined the R&D group at TriQuint Semiconductor, Richardson, TX, in 2000 as the lead process development engineer for GaN HEMT devices. She was a key contributor on the TriQuint team of the Phase II of the DARPA WBG-RF program and is the program manager for Phase III of the program.

**Victoria Williams** received the B.S. degree from Rutgers University, New Brunswick, NJ, and the Ph.D. degree from Cornell University, Ithaca, NY.

Since 2001, she has been with the Texas division of TriQuint Semiconductor, where she has held positions in process engineering and R&D, most recently, as Member of the Technical Staff in R&D. She has been involved in the development of MOCVD, ion-implant, and wet chemical processes and, currently, works on materials and process development for GaN-based devices.



**Ming-Yih Kao** (M'85–SM'02) received the B.S. degree in physics from the National Tsing-Hua University, Taiwan, the Masters degree in electrical engineering from the University of Massachusetts at Amherst, and the Ph.D. degree in electrical engineering from the University of Texas at Dallas.

He has been with TriQuint Semiconductor since January 1998 as a Senior Member of Technical Staff in the Engineering group. Before he came to the United States from Taiwan for graduate study, he was first a process engineer, then a process engineering manager in charge of silicon power device development for three years. From 1987 to 1995, he worked at GE's Electronics Laboratory where he was engaged in the development of state-of-the-art GaAs pseudomorphic HEMTs, InP-based devices and MMIC process technology. He continued his research in the compound semiconductor device development at TI's Central Research Laboratories from 1995 to 1997. Presently, he is working on Gallium Nitride and Gallium Arsenide devices and process development. He was the principle engineer behind several major HEMT process and technology developments as well as production transfer at TriQuint. He has more than 60 technical publications in refereed journals and conferences.



**Hua-Quen Tserng** (M'70–SM'83–F'92–LF'05) received the M.S. and Ph.D. degrees in electrical engineering from Rice University, Houston, TX, in 1966 and 1968, respectively.

He has been with TriQuint Texas since January 1998. Presently, he is a Senior Fellow in TriQuint Military Business Unit. From 1968 to 1998, he was with Texas Instruments where he had been involved in the development of advanced heterostructure transistors and power and low-noise MMICs for military and commercial applications. He had managed a number of technology programs including: V-band power amplifiers for SDI, Ka-band InP HBT power amplifiers for seeker, Ka-band amplifiers and phase shifters for phased array jammers, and X-band pHEMT power amplifiers for high power phased array radar. In 1985, he was one of the first to demonstrate microwave power applications of AlGaAs/GaAs HBTs. He has published more than 100 papers in the area of solid-state microwave/millimeter-wave devices and circuits and holds 16 U.S. patents.

Dr. Tserng was elected an IEEE Fellow in 1992 for his technical contribution to monolithic microwave integrated circuits and devices. He has achieved the status of IEEE Life Fellow in 2005. He has presented numerous invited papers at international conferences and served as session chairman or co-chairman in various microwave conferences.

**Paul Saunier** (M'79–SM'87) received the M.S. and Ph.D. degrees from Carnegie Mellon University, Pittsburgh, PA, after graduating from Ecole Centrale de Lyon, France.

He is a Senior Fellow at TriQuint Semiconductor. He is responsible for the development of advanced GaN and GaAs devices. He has been the Principal Investigator for the DARPA contract for wide-bandgap semiconductors for RF applications. Prior to joining TriQuint in 1999, he was a Texas Instruments Fellow managing the FET Group of TI Central Research Laboratories. He has over 100 publications.



**Tony Balistreri** received the B.S.E.E. degree from Marquette University, Milwaukee, WI, and the Masters degree in electrical engineering from Rice University, Houston, TX, majoring in computer hardware.

He is the manager of Research and Development at TriQuint Semiconductor Texas. He joined Texas Instruments' MOS Memory Design Group in Houston in 1982 as a design engineer working on Dynamic RAMs and Video RAMs. During this time he was active in JEDEC working towards developing DRAM, VRAM and Synchronous DRAM standards. He was named Member, Group Technical Staff in 1991 and Senior Member, Technical Staff in 1993. Taking

advantage of the customer and application knowledge gained while developing memory standards, he was later named New Product Development Manager for High Speed and Graphics DRAMs. In 1998, he joined Micron Technology as part of their acquisition of Texas Instruments' Memory business where he worked as Product Engineering Manager for Synchronous DRAMs. In 1999 he joined TriQuint Semiconductor as Program Manager for Research and Development where he led several large government contracts, including NIST, ONR, NRL, ARL, and DARPA, as well as various commercially funded programs. In 2005, he was named Director of Research and Development. He has several patents in the fields of DRAM design and computer graphics.

Mr. Balistreri is a member of Sigma Phi Delta engineering fraternity and is active in the Project Management Institute.