Analytical calculation of the RMS current stress on the DC-link capacitor of voltage-PWM converter systems

J.W. Kolar and S.D. Round

Abstract: A simple analytical expression for the current stress on the DC-link capacitor caused by the load-side inverter of a voltage DC-link-converter system is derived. The DC-link capacitor-current RMS value is determined from the modulation depth and by the amplitude and the phase angle of the inverter output current assuming a sinusoidal inverter output current and a constant DC-link voltage. Despite neglecting the output-current ripple, the results of the analytical calculation are within 8% of measurements made from digital simulation and an experimental system, even if the output-current ripple is relatively high as in the case of low-frequency IGBT inverter systems. The simple analytical expression provides significant advantages over simulation methods for designing the DC-link capacitor of PWM converter systems.

1 Introduction

Voltage DC-link inverters are frequently fed via uncontrolled rectifier bridges from the single-phase or the three-phase mains, as shown in Fig. 1. There, in the DC link, aluminium electrolytic capacitors (connected in series and/or in parallel) are usually used:

(*a*) to compensate the difference between the power requirement of the inverter (whose mean value is constant in steady-state operation) and the output power of the input-rectifier bridge varying with two or six times the mains frequency;

(*b*) to supply the input current of the inverter with pulse frequency;

(*c*) to reduce the spread of current harmonics with pulse frequency into the mains;

(*d*) to take in the demagnetisation energy of the drive (e.g. induction machine) in case of an emergency shutdown of all converter transistors;

(*e*) to supply transient-power peaks; and

(*f*) to protect the inverter from transient peaks of the mains voltage.

As explained, for example, in [1], the operating voltage and especially the working temperature have a significant influence on the working life of electrolytic capacitors. If, for example, an aluminium electrolytic capacitor is operated at 0.9 × rated voltage, the failure rate is reduced to 60% compared with operation at rated voltage (c.f. Fig. 7 in [1]). If the working temperature is reduced, the typical working life doubles for every 10°C below the rated temperature (Arrhenius Law, c.f. p. 6 in [2]), since, at the lower temperature, the diffusion of the gaseous parts of the electrolyte through the end seal is reduced and thus the drying out of the capacitor is delayed. Therefore, to meet a demanded mean time between failure of the inverter, in addition to selecting an appropriate rated voltage of the capacitor, the correct thermal design is of major importance.

The temperature that is important for the working life is the can temperature T_c (c.f. Fig. 8 in [3]). T_c is determined from the ambient temperature T_a and the power dissipation in the capacitor, as caused by the capacitor RMS current $I_{C,rms}$:

$$T_c = T_a + I_{C,rms}^2 R_{ESR} R_{th,c-a} \tag{1}$$

where R_{ESR} denotes the equivalent series resistance of the capacitor, which represents the sum of the frequency-sensitive resistance of the oxide dielectric, the temperature-sensitive resistance of the electrolyte and the relatively constant small contributions of the foil, the tabs and the terminals [3, 4]; and $R_{th,c-a}$ that denotes the thermal resistance between the capacitor can and the ambient.

Therefore, for a correct thermal design of the capacitor the RMS value $I_{C,rms}$ of the DC-link-capacitor current is of

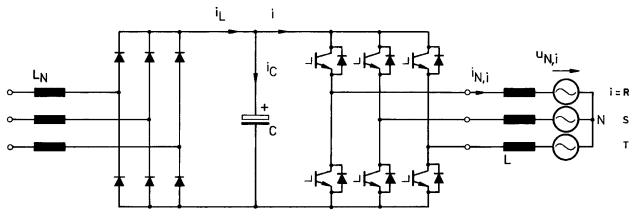

Fig. 1 *Basic power circuit of a voltage DC-link converter*
The AC machine, fed by the inverter, is considered by a simple equivalent circuit formed by leakage inductances L and back EMF $u_{N,i}$. The inductors L_N at the input limit the peak values of the input currents and/or the effects on the mains, and the current stress on the DC-link capacitor C [12]

IEE Proceedings online no. 20050458

doi:10.1049/ip-epa:20050458

Paper first received 1st November 2005 and in final revised form 17th January 2006

The authors are with the ETH Zurich, Power Electronic Systems Laboratory, Physikstrasse 3, Zürich CH-8092, Switzerland

E-mail: round@lem.ee.ethz.ch

paramount importance. The methods for calculating $I_{C,rms}$ as proposed in the literature are based on a spectral analysis of the phase quantities (c.f. [5], Fig. 4*h* in [6], [7–11]) and/or rely on digital simulations. Besides the considerable amount of time required to establish a simulation model, one drawback of these methods is the inability to determine the influence of the inverter's operating point, which is characterised by the modulation depth and by the amplitude and phase displacement of the inverter-output current and voltage fundamentals, on the capacitor-current stress as the simulation is valid only for a single set of operating parameters.

However, as shown in this paper, it is also possible to calculate the RMS current of the DC-link capacitor in an analytically closed form in the time domain with sufficient accuracy. Therefore, the effort necessary for designing the capacitor regarding the current stress thus is reduced to the evaluation of a simple mathematical expression. In addition, the knowledge of the influence of the operating parameters on the capacitor-current RMS value can easily be used to determine the worst-case current stress.

2 Basic considerations

For preparing the analytical calculation of the capacitor-current stress, a brief review of the fundamentals of the inverter control and of the formation of the inverter input current i is presented. Owing to the symmetries of an ideal three-phase voltage system and the phase-symmetric structure of the converter power circuit, the analysis can be limited to a $\frac{\pi}{3}$-wide interval of the inverter-output-voltage fundamental period.

2.1 Space-vector modulation

For stationary operation, the reference value of the inverter output voltage can be represented by a space vector

$$\boldsymbol{u}_{U,(1)} = \hat{U}_U \exp(j\phi_U) \qquad \phi_U = \omega_N t \tag{2}$$

of constant magnitude $\hat{U}_U$ and constant angular speed $\omega_N = 2\pi f_N$ (f_N denotes the inverter output frequency). $\boldsymbol{u}_{U,(1)}$ is approximated within each pulse half period $t_\mu \in [0, T_P)$ by switching between the immediately neighbouring inverter output-voltage space vectors. For the angle interval $\phi_U \in (\frac{\pi}{3}, \frac{2\pi}{3})$ (c.f. Fig. 2) which is considered in the following, the switching state sequence is

$$\begin{aligned} &\ldots|_{t_\mu=0}(0\,0\,0) - (0\,1\,0) - (1\,1\,0) - (1\,1\,1)|_{t_\mu=\frac{1}{2}T_P} \\ &(1\,1\,1) - (1\,1\,0) - (0\,1\,0) - (0\,0\,0)|_{t_\mu=T_P}\ldots \end{aligned} \tag{3}$$

where each inverter switching state is characterised by the triple (s_R, s_S, s_T) of the associated phase switching functions s_i, where $i = R, S, T$. We define $s_i = 1$ if the output voltage of phase i referred to the fictitious centre point of the DC link is positive, $u_{U,i} = +\frac{1}{2}U_O$, and $s_i = 0$ if the output voltage of phase i is negative, $u_{U,i} = -\frac{1}{2}U_O$.

The relative on times of the switching states (0 1 0) and (1 1 0),

$$\begin{aligned} \delta_{(0\,1\,0)} &= \frac{\sqrt{3}M}{2}\sin\left(\phi_U - \frac{\pi}{3}\right) \\ \delta_{(1\,1\,0)} &= \frac{\sqrt{3}M}{2}\sin\left(\phi_U + \frac{\pi}{3}\right) \end{aligned} \tag{4}$$

can be determined by simple geometrical considerations (c.f. Fig. 2) and are defined by the location ϕ_U of the respective pulse half period within the fundamental period of the inverter output voltage and by the relative amplitude

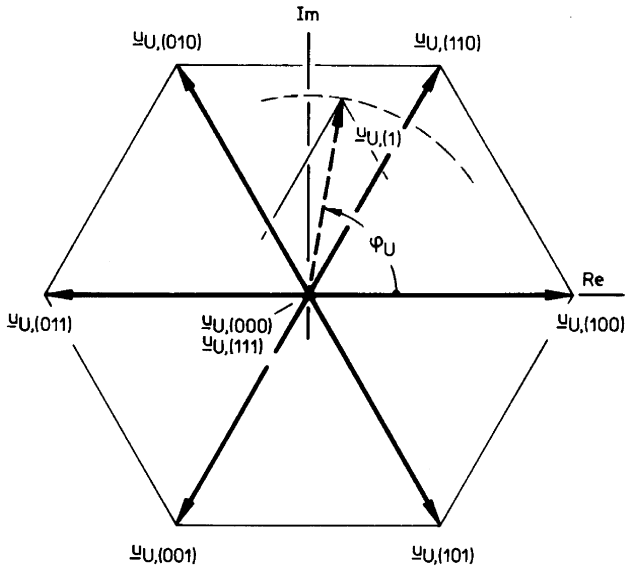

Fig. 2 *Space vectors of the inverter output voltage assigned to the active inverter-switching states and to the nonvoltage-forming switching states (0 0 0) and (1 1 1)*
Inverter output voltage reference value $\boldsymbol{u}_{U,(1)}$ which is formed from the average over a pulse half period of position ϕ_U; $\boldsymbol{u}_{U,(1)}$ is associated with the fundamental of the pulse-width-modulated inverter-output phase voltages $u_{U,i}$, $i = R, S, T$

of the inverter-output-voltage fundamental and/or the modulation index

$$M = \frac{\hat{U}_U}{\frac{1}{2}U_O} \qquad M \in \left[0, \frac{2}{\sqrt{3}}\right] \tag{5}$$

where the DC-link voltage is assumed to be constant. In contrast, the distribution of the total on time of the nonvoltage-forming (free-wheeling) switching states (0 0 0) and (1 1 1)

$$\delta_{(0\,0\,0)} + \delta_{(1\,1\,1)} = 1 - (\delta_{(0\,1\,0)} + \delta_{(1\,1\,0)}) \tag{6}$$

between the beginning and the end of each pulse half period can be chosen freely without influencing the fundamental output-voltage phasor $\boldsymbol{u}_{U,(1)}$. This degree of freedom

$$\delta_{(1\,1\,1),\mathrm{r}} = \frac{\delta_{(1\,1\,1)}}{\delta_{(1\,1\,1)} + \delta_{(0\,0\,0)}} \qquad \delta_{(1\,1\,1),\mathrm{r}} \in [0, 1] \tag{7}$$

can be used to minimise the RMS value of the inverter-output-current ripple with switching frequency [13]. Alternatively, one could also use a suboptimal even distribution $\delta_{(0\,0\,0)} = \delta_{(1\,1\,1)}$ and/or $\delta_{(1\,1\,1),\mathrm{r}} = 0.5$ to obtain a low realisation effort of the inverter control [14].

2.2 Inverter-input-current formation

As becomes immediately clear by considering the inverter bridge legs as two-pole switches between the positive and negative DC-link bus ($s_i = 1$ and/or 0), the input current i of the inverter is determined by

$$i = s_R i_{N,R} + s_S i_{N,S} + s_T i_{N,T} \tag{8}$$

In this paper the dead-time interval, which has to be considered for the gating of the transistors of a bridge leg in practice, and the reverse recovery current of the free-wheeling diodes, which have a minor influence on the shape of i [15, 16], are neglected. The input inverter current i is formed by segments of the inverter output phase currents $i_{N,i}$ and is dependent on the inverter switching state. For the switching state (0 1 0), the output terminal of phase S is

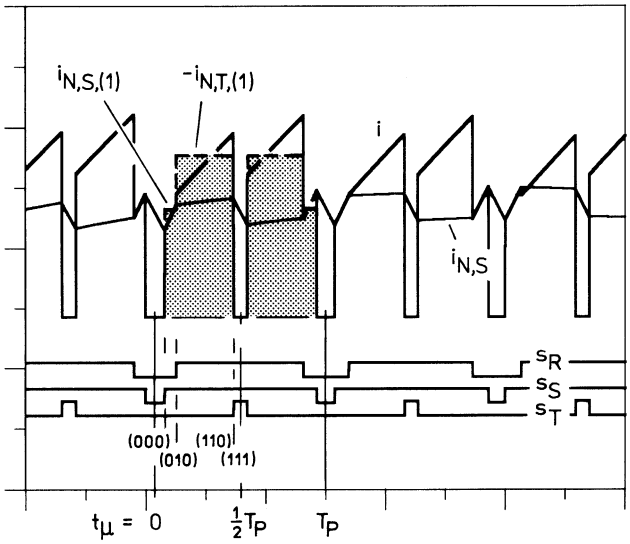

Fig. 3 *Formation of the inverter input current i with dependency on the inverter switching state (s_R, s_S, s_T)*
Local time behaviour of the inverter input current i, of the inverter output phase current $i_{N,S}$ and of the phase-switching functions s_R, s_S and s_T
Simplified shape of the inverter input current resulting from neglecting the phase-current ripple and/or exclusive consideration of the phase-current fundamentals (shown as broken lines highlighted by the tinted area)

connected to the positive DC bus and phases R and T are switched to the negative DC-link rail; therefore, i and $i_{N,S}$ show identical time behaviour (c.f. Fig. 3). For switching state (1 1 0) the current is $i = -i_{N,T}$, since

$$i_{N,R} + i_{N,S} + i_{N,T} \equiv 0 \tag{9}$$

has to be considered. Only during the free-wheeling states (0 0 0) and (1 1 1) will no current appear at the converter input. The distribution $\delta_{(1\,1\,1),r}$ of the free-wheeling states between the beginning and the end of a pulse half period therefore, to a first approximation, only has an influence on the position of the current-conduction intervals $i = i_{N,S}$ and $i = -i_{N,T}$ within a pulse half period, but does not influence the shape of i in principle.

3 Calculation of average and RMS value of the inverter input current

A purely sinusoidal shape of the inverter output currents

$$\left.\begin{aligned} i_{N,R,(1)} &= \hat{I}_N \cos(\phi_U - \phi) \\ i_{N,S,(1)} &= \hat{I}_N \cos\left(\phi_U - \frac{2\pi}{3} - \phi\right) \\ i_{N,T,(1)} &= \hat{I}_N \cos\left(\phi_U + \frac{2\pi}{3} - \phi\right) \end{aligned}\right\} \tag{10}$$

corresponding to a space vector

$$\boldsymbol{i}_{N,(1)} = \hat{I}_N \exp\{j(\phi_U - \phi)\} \tag{11}$$

is assumed where ϕ denotes the phase displacement of the fundamentals of the inverter output voltage $\boldsymbol{u}_{U,(1)}$ and the inverter output current $\boldsymbol{i}_{N,(1)}$. This is equivalent to only considering the fundamental of the phase currents, which to a first approximation show a constant value within a pulse half period. The error caused by neglecting the output-current ripple is calculated in Section 5 and remains small even if the ripple amplitude reaches relatively high values compared with the amplitude of the phase-current fundamental.

3.1 Mean value of the inverter input current

Based on the considerations in Section 2.2, the 'local' mean value of the inverter input current (related to a pulse half period) is

$$i_{avg} = \frac{2}{T_P} \int_0^{\frac{1}{2}T_P} i \, dt_\mu \tag{12}$$

Equation (12) can be expressed as

$$i_{avg} = \delta_{(0\,1\,0)} i_{N,S} - \delta_{(1\,1\,0)} i_{N,T} \tag{13}$$

With this, and (4) and (10), we obtain

$$i_{avg} = I_{avg} = \frac{3}{4} \hat{I}_N M \cos\phi \tag{14}$$

Corresponding to the constant power supplied by a symmetrical and sinusoidal three-phase voltage/current system, the inverter input current shows a constant local average value $i_{avg} = I_{avg}$, i.e. the local and 'global' (related to the fundamental of the output voltage) mean values are identical. For $\cos\phi = 0$ the inverter generates only fundamental reactive power and/or no power is supplied from the DC link (harmonic power components are neglected). Accordingly, we have $I_{avg} = 0$, and the inverter input current i is defined by segments out of the vicinity of the zero crossings of the output phase currents $i_{N,i}$ with alternating signs (c.f. Fig. 4*a*).

On the contrary, for $\cos\phi = 1$ we have purely active-power operation and/or maximum current is supplied by the DC link. There, i is formed by segments of identical signs near the vicinity of the maxima of the phase currents $i_{N,i}$ (c.f. Fig. 4*b*). For a given value of the fundamental displacement factor $\cos\phi$ of the output-current/voltage system I_{avg}, will rise linearly with increasing modulation index M. This can be explained by considering the linear increase of the width of the current pulses [see (4)] appearing at the inverter input for increasing modulation index M or by the increase of the inverter output power owing to the proportional increase of the fundamental output voltage as a consequence of the higher modulation index M [see (5)].

Note that, besides the (global) mean value, i ideally does not contain any low-frequency harmonics but only harmonics of the switching frequency.

3.2 RMS value of the inverter input current

For the local RMS value of the inverter input current

$$i_{rms}^2 = \frac{2}{T_P} \int_0^{\frac{1}{2}T_P} i^2 \, dt_\mu \tag{15}$$

we have in analogy to (14):

$$i_{rms}^2 = \delta_{(0\,1\,0)} i_{N,S}^2 + \delta_{(1\,1\,0)} i_{N,T}^2 \tag{16}$$

Therefore, with

$$I_{rms}^2 = \frac{3}{\pi} \int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} i_{rms}^2 \, d\phi_U \tag{17}$$

and (4) results in the global RMS value I_{rms} of i being

$$I_{rms} = I_{N,rms} \sqrt{\left\{ \frac{2\sqrt{3}}{\pi} M \left(\frac{1}{4} + \cos^2\phi \right) \right\}} \tag{18}$$

In connection with (18) note that the RMS value of the inverter input current i, to a first approximation (as calculated by considering only the output phase current fundamentals), is independent of the inverter control scheme. As the fundamentals of the output phase currents $i_{N,S,(1)}$ and $-i_{N,T,(1)}$ are assumed to be approximately constant within $t_\mu \in [0, \frac{1}{2}T_P)$, there is therefore no influence

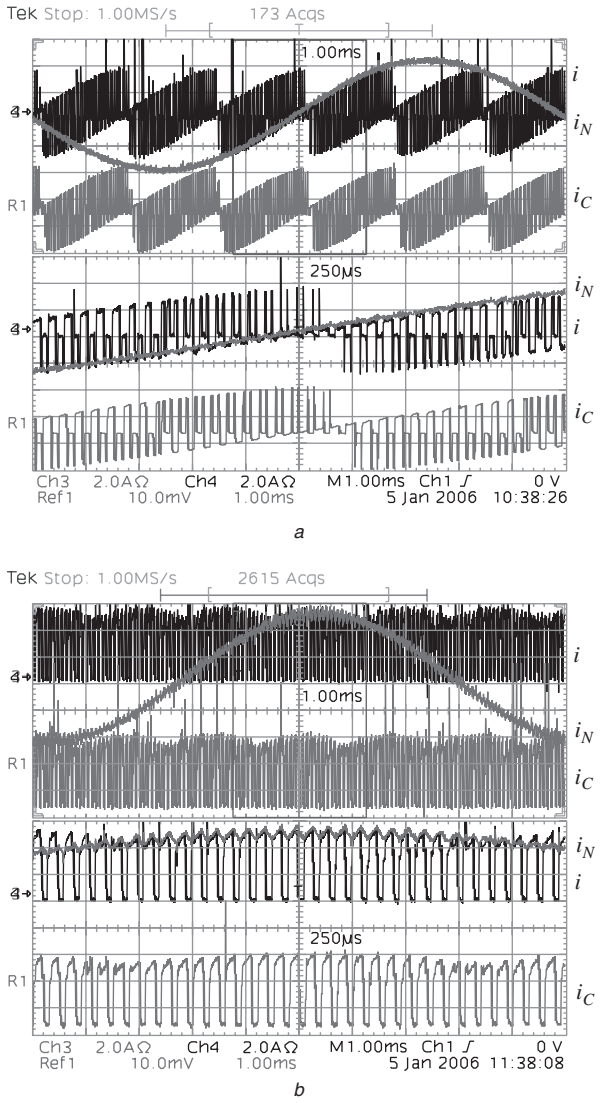

Fig. 4 *Experimental measured time behaviour of the inverter input current i, the output phase current $i_{N,R}$ and the capacitor current i_C for a fundamental period and 60° of the converter output voltage*
a $\cos\phi = 0$
b $\cos\phi = 1$

of the actual position of the switching state intervals $\delta_{(0\,1\,0)}$ and $\delta_{(1\,1\,0)}$ on the value of i_{rms}. The only (minor) influence of $\delta_{(1\,1\,1),\mathrm{r}}$ on i_{rms} and I_{rms} is by the ripple component of $i_{N,S}$ and $-i_{N,T}$, which has been neglected for the derivation of (18).

4 DC-link capacitor-current RMS value

The DC-link capacitor current is defined by the difference

$$i_C = i_L - i \tag{19}$$

of the inverter input current i and the output current i_L of the converter input stage (see Fig. 1), which in most cases is realised as an uncontrolled three-phase rectifier bridge.

By splitting up i and i_L into DC and AC components (designated by subscript 'ac'),

$$\begin{aligned} i &= I_{avg} + i_{ac} \\ i_L &= I_{L,avg} + i_{L,ac} \end{aligned} \tag{20}$$

one now can replace (19) by

$$i_C = i_{L,ac} - i_{ac} \tag{21}$$

As is immediately obvious, the load on the DC-link capacitor is defined solely by the AC components of i and i_L, as the DC component I_{avg} of i can be considered to be supplied directly by the input-rectifier bridge.

With (20) and

$$I_{C,rms}^2 = \frac{3}{\pi}\int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} i_C^2\, d\phi_U \tag{22}$$

one obtains for the global RMS value of the DC-link capacitor current

$$I_{C,rms}^2 = I_{ac,rms}^2 + \frac{6}{\pi}\int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} i_{ac} i_{L,ac} d\phi_U + I_{L,ac,rms}^2 \tag{23}$$

The problem with a mathematical evaluation of this equation is calculation of the integral that is dependent on i_{ac} and $i_{L,ac}$. If, however, as in the case at hand, the currents i_L and i do not contain harmonics in the same frequency range [harmonics of higher amplitudes are usually only present for ordinal numbers $n < 50$ in the output current of uncontrolled rectifier bridges (see, for example, Fig. 13 in [17]) the frequency range being occupied by harmonics of i is defined by the inverter switching frequency and typically shows a lower bound of $n \simeq 200 \ldots 500$ for a realisation using IGBTs], the integral is

$$\frac{6}{\pi}\int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} i_{ac} i_{L,ac} d\phi_U = 0 \tag{24}$$

and the current stress on the DC-link capacitor is determined by

$$I_{C,rms}^2 = I_{ac,rms}^2 + I_{L,ac,rms}^2 \tag{25}$$

Therefore, the RMS value of the DC-link-capacitor current can clearly be divided into a contribution being determined by the mains-commutated input rectifier and a contribution caused by the PWM inverter (see Fig. 7 in [4]). For brevity, only the calculation of the capacitor-ripple contribution due to the inverter, $I_{C,rms,1} = I_{ac,rms}$, is discussed in detail. For discussion of the calculation of ripple contribution due to the uncontrolled rectifier, see, for example, [18].

If the DC link is fed instead via a self-commutated rectifier, e.g. a three-phase PWM rectifier system with high pulse frequency (see, for example, p. 201 in [19]), the DC-link-capacitor current is a superposition of harmonics of the DC-link input and output currents. The current stress on the DC-link capacitor is therefore dependent the amplitudes and the phase relationships of the harmonics of equal ordinal number, resulting in a higher or lower amplitude of the respective harmonics in the DC-link-capacitor current. Therefore, $I_{C,rms}$ can be minimised by an appropriate coupling and/or synchronisation of the rectifier and inverter controls (see Section 3 in [20] and [21]).

The maximum current stress on the DC-link-capacitor current, which occurs for the worst-case correlated operation, is

$$I_{C,rms,max} = I_{ac,rms} + I_{L,ac,rms} \tag{26}$$

and is derived in the Appendix (Section 10), as well as given in [22] (see eqn. (50) in [22]). For a more accurate determination of $I_{C,rms}$, one would have to undertake a digital simulation.

For the RMS value $I_{C,rms,1}$ of the AC component i_{ac} of i, we have in general

$$I_{C,rms,1}^2 = I_{rms}^2 - I_{avg}^2 \tag{27}$$

and with (14) and (18) (see also [24])

$$I_{C,rms,1} = I_{N,rms}\sqrt{\left[2M\left\{\frac{\sqrt{3}}{4\pi} + \cos^2\phi\left(\frac{\sqrt{3}}{\pi} - \frac{9}{16}M\right)\right\}\right]} \tag{28}$$

Equation (28) represents the required functional dependency of the capacitor-current stress on the inverter operating parameters (see Fig. 5). The proportional relationship of $I_{C,rms,1}$ and $I_{N,rms}$ and/or $\sqrt{M}$ can be explained clearly by considering the fact that i is formed by segments of the phase currents. The widths of the segments are dependent on the modulation index M [see (8)] and the $\sqrt{M}$ term is produced from the RMS calculation. For $M = 0$, the inverter remains in the free-wheeling state within the entire pulse half period; therefore, we then have $i = 0$ or $i_{C,rms,1} = 0$, respectively.

If $\cos\phi \simeq 1$ is assumed, in addition to I_{rms}, also the DC component I_{avg} increases with increasing M, according to (14) and (18). Therefore, according to (27) a maximum of the DC-link-capacitor-current RMS value $I_{C,rms}$ occurs about in the middle of the modulation range:

$$M_{I^2_{C,rms,1}\rightarrow max} = \frac{8\sqrt{3}}{9\pi}\left(1 + \frac{1}{4\cos^2\phi}\right) \tag{29}$$

This can be explained clearly by considering the RMS value of the AC component of a unipolar square-wave signal with variable duty ratio α which reaches a maximum for $\alpha = 0.5$. For operation of the inverter at maximum modulation depth M_{max}, the shape of i still shows intervals with zero current (of relative width $\delta_{(000)} + \delta_{(111)}$, [see (4) and (6)]). Accordingly, the inverter input current in any case shows a AC component i_{ac} and/or $I_{C,rms,1}$ that does not reach 0 for values of M close to M_{max}.

If $\cos\phi \simeq 0$, again, a sequence of phase-current segments showing increasing widths for increasing M is switched into the DC link. However, there is no reduction of $I_{C,rms,1}$ compared with I_{rms} owing to the missing DC component I_{avg} of i. Therefore, $I_{C,rms}$ coincides with I_{rms} [c.f. (18)] and the maximum of $I_{C,rms}$ occurs for maximum modulation depth $M_{max} = 2/\sqrt{3}$ and/or turns into a boundary maximum. This is true in general for

$$\cos\phi \leq \sqrt{\frac{1}{4\left(\frac{3\pi}{4} - 1\right)}} = 0.43 \tag{30}$$

In this connection, note that, for

$$M' = \frac{16\sqrt{3}}{9\pi} = 0.98 \tag{31}$$

the resulting current stress $I_{C,rms,1}$ is independent of the value of $\cos\phi$.

According to Fig. 5, the current stress on the DC-link capacitor is dependent of the fundamental displacement factor $\cos\phi$. For the case where the inverter controls a permanent-magnet AC machine (with near unity power factor), then the worst-case current-stress estimation, used as a basis for the capacitor dimensioning, is given by

$$I_{C,rms,1} \simeq \frac{1}{\sqrt{2}} I_{N,rms} \tag{32}$$

For asynchronous-motor and PWM-rectifier applications, where a reduced power factor and/or a high modulation index are used, the capacitor-current stress can be estimated

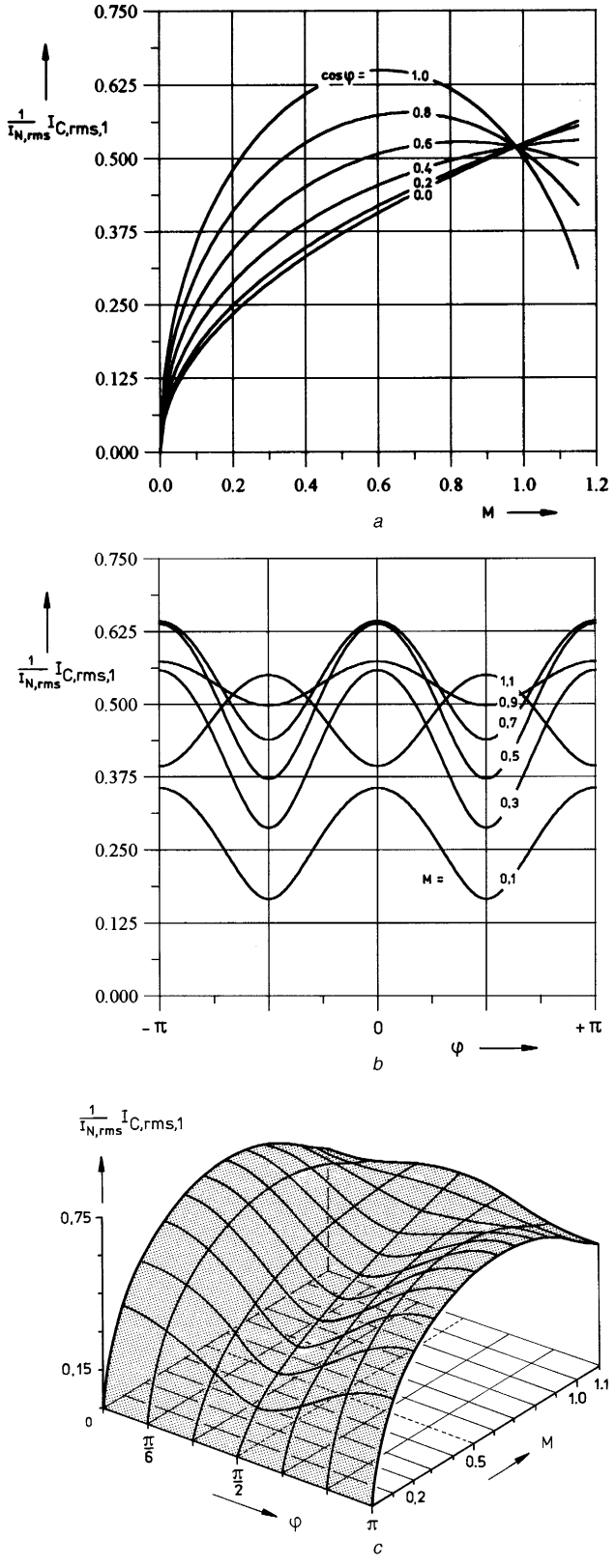

Fig. 5 *Dependency of the inverter-side contribution $I_{C,rms,1}$ (28) to the global DC-link-capacitor current RMS value $I_{C,rms}$ on the inverter modulation index M and on the phase displacement ϕ of the fundamental of the inverter output phase voltages $u_{U,i}$ and the associated output phase currents $i_{N,i}$*
a M
b ϕ
c Three-dimensional representation

using the simple expression

$$I_{C,rms,1} \simeq \frac{1}{2} I_{N,rms} \tag{33}$$

5 Accuracy estimation and experimental verification

To be able to derive a simple expression for the inverter-side current stress $I_{C,rms,1}$ on C and to be independent of details of the inverter control scheme, the ripple of the inverter output currents $i_{N,i}$ has been neglected and/or only the fundamentals $i_{N,i,(1)}$ of the phase currents $i_{N,i}$ have been considered so far. Thus, a very clear approximation, being independent of the absolute values of the DC-link voltage U_O, the pulse frequency f_P and the stray inductance L of the AC machine (c.f. Fig. 1) has been derived. Now the error, which is caused by the neglecting the phase-current ripple, compared with an exact calculation by digital simulation, is determined and/or the limit of the applicability of (28) for the design of the DC-link capacitor is determined.

To characterise the ripple of the phase currents, a parameter

$$\kappa = \frac{1}{\hat{I}_N} \frac{U_O T_P}{8L} \tag{34}$$

is defined. Thus all operating parameters which influence the formation of the output-current ripple are combined and related to the amplitude of the output-current fundamental ($U_O T_P/8L$ represents the ripple amplitude resulting from application of a symmetrical square-wave voltage of frequency f_P, duty cycle $\alpha = 0.5$ and amplitude $\frac{1}{2}U_O$ to L). Furthermore, a symmetrical distribution $\delta_{(1\,1\,1),r} = 0.5$ of the free-wheeling switching state (see Section 2.1) is assumed, which is frequently applied in practice owing to the low calculation effort required to determinate the inverter switching instants [23].

For feeding the DC link via an uncontrolled rectifier bridge, the value of the DC-link voltage is determined directly by the mains voltage and usually shows a very low ripple. Therefore, for the following reasons a constant DC-link voltage of $U_O = 540\,\text{V}$ is assumed corresponding to the voltage value resulting from operation of the converter system on the European low-voltage three-phase mains (line-to-line voltage: $400\,\text{V}_{rms}$) and ideal capacitive smoothing. For the switching frequency we define $f_P = 1/T_P = 10\,\text{kHz}$. Thus, by considering output-inductance values in the range $L = 0.3375$–$1.35\,\text{mH}$ in connection with an amplitude of the output phase currents being set to $\hat{I}_N = 20\,\text{A}$, a range of $\kappa = 0.25$–1.0 is inspected, where the output-current shape changes from being approximately sinusoidal ($\kappa = 0.25$) to having a relatively high ripple component ($\kappa = 1$, see Fig. 6). Furthermore, the conditions for $\cos\phi = 1$ and $\cos\phi = 0$ are investigated as, in these cases, qualitatively different shapes of i and/or i_{ac} occur (c.f. Fig. 4).

The dependency of the relative error

$$\text{f} = \frac{1}{I_{C,rms,1,sim}} \left(I_{C,rms,1,(28)} - L_{C,rms,1,sim}\right) \tag{35}$$

of the analytical calculation of $I_{C,rms,1}$ based on (28), $I_{C,rms,1,sim}$ denotes the inverter-side current stress on C as determined by digital simulation on κ and M is shown in Fig. 7. For values of M close to 0, the phase currents show a very low ripple (see Fig. 16 of [24]). Therefore, the error caused by assuming a purely sinusoidal output-current shape remains very small. For increasing modulation depth M, a higher relative error of the analytical approximation occurs due to the increasing output-current-ripple amplitude.

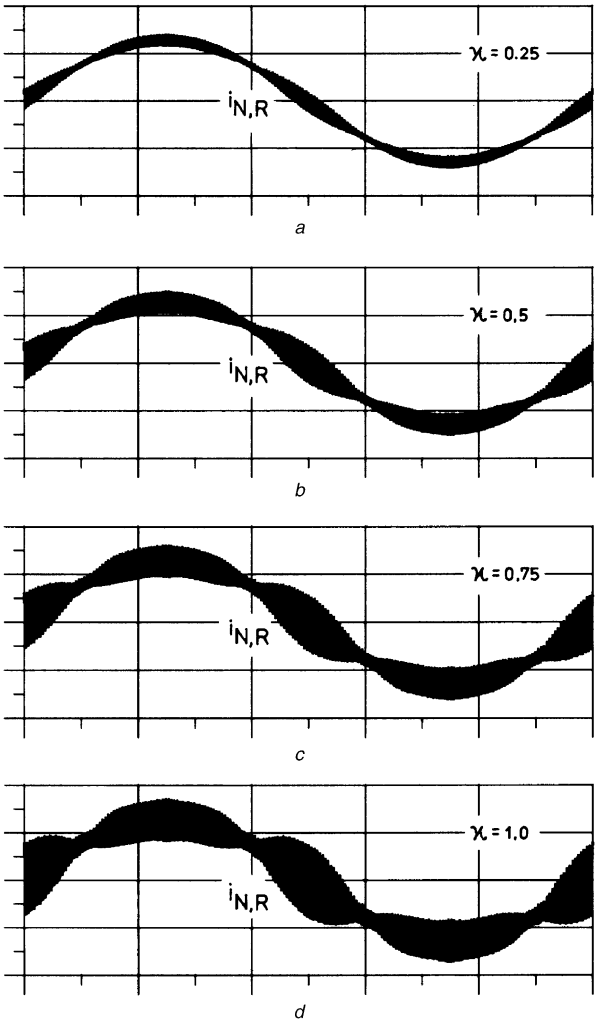

Fig. 6 *Time behaviour of an inverter-output-phase current for different values of the parameter κ, which characterises the relative amplitude of the output current ripple*
$\kappa = 0.25$, 0.5, 0.75 and 1.0
$\cos\phi = 1$
$M = 1.0$
a $\kappa = 0.25$
b $\kappa = 0.5$
c $\kappa = 0.75$
d $\kappa = 1.0$

In $\cos\phi = 0$, in general there is lower accuracy than for $\cos\phi = 1$. This can be explained clearly by the fact that, for $\cos\phi = 0$, the inverter input current [and correspondingly also i_{ac}, (21)] is formed by segments near the vicinity of the zero crossings of the output-phase currents; thus a current ripple of given amplitude κ has a relatively greater influence on the shape of i compared with forming i from segments near the vicinity of the maxima of the phase currents and/or for $\cos\phi = 1$ (c.f. Fig. 4).

Where a minimum degree of accuracy, such as $|\text{f}| <$ 5–10%, is required for the dimensioning, then the application range of (28) is limited to $\kappa \simeq 0.75$. This, however, certainly includes the conditions typically present in practice for operating an IGBT inverter at rated power. Therefore, the dimensioning can be based on (28) and/or a time-consuming calculation of $I_{C,rms,1}$ by digital simulation can be omitted.

5.1 Experimental verification

A three-phase inverter, switching at 20 kHz, connected to a *RL* load and supplied by a 540 V DC power supply is used

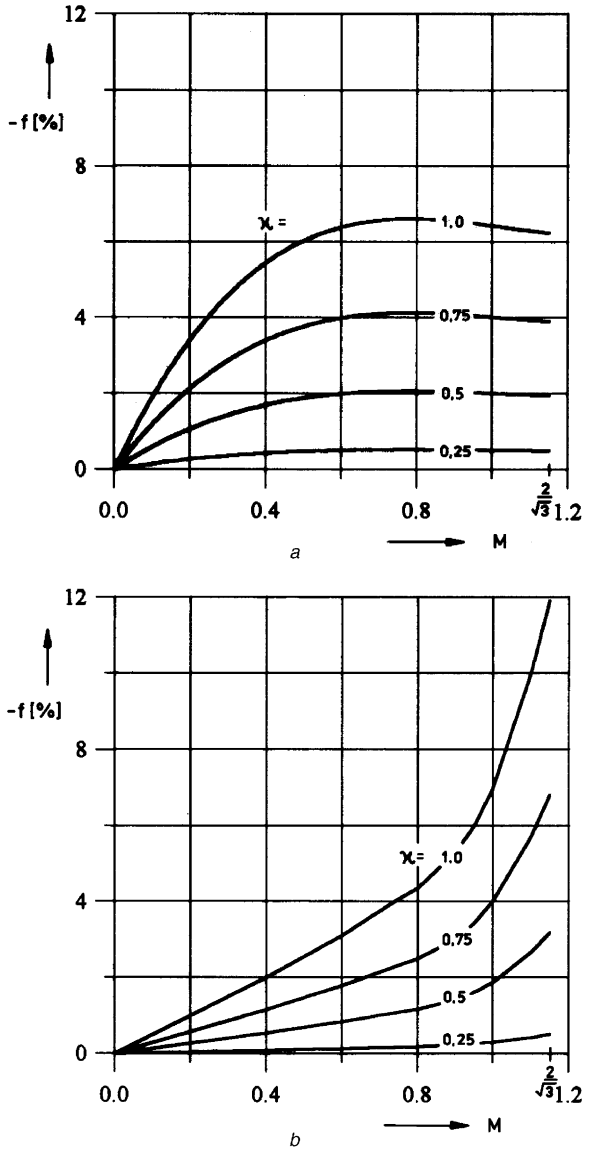

Fig. 7 *Relative error f of the analytical calculation of the capacitor-current stress $I_{C,rms,1}$ as caused by the PWM inverter (28) from the results of a digital simulation with dependency on the modulation index M and the relative amplitude κ of the inverter output current ripple*
a $\cos\phi = 1$
b $\cos\phi = 0$

to verify experimentally the analytical expression given in (28). The inverter system is operated with two load power factors of $\cos\phi = 1$ and $\cos\phi = 0$. For $\cos\phi = 1$, the load resistance is adjusted for varying modulation values to maintain a current of approximately 3.5 A RMS through the load. For a modulation index of $2/\sqrt{3}$, this corresponds to an output power of 2.4 kW. To generate results with two different levels of current ripple, the inverter output inductance is changed from 1 mH to 8 mH to produce $\kappa = 0.1$ and $\kappa = 0.8$, respectively. For $\cos\phi = 0$, a large inductance of 25 mH is used solely as the load and produces a low level of current ripple. In this case, the DC voltage is varied between 60 and 540 V to maintain approximately 3 A RMS of load current over the range of modulation indices.

The current flowing into the inverter and the inverter load current are measured using two Tektronix A6312 100 MHz current probes, and a LeCroy LT584L oscilloscope is used to calculate the respective RMS

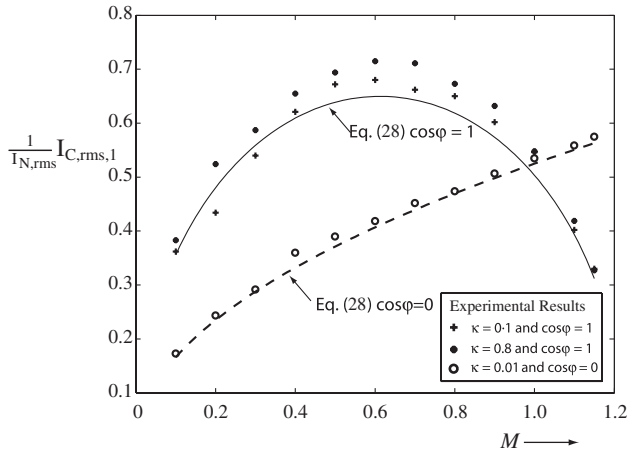

Fig. 8 *Experimental results compared with analytical calculation of the capacitor-current stress $I_{C,rms,1}$ as caused by the PWM inverter (28)*
Comparison is for various discrete modulation indices *M*, and two output phase angles $\cos\phi = 1$, with small ($\kappa = 0.1$) and large ($\kappa = 0.8$) current ripple, and $\cos\phi = 0$

values. The ratio of the capacitor RMS current, due to the inverter, to the inverter-output RMS current is plotted in Fig. 8 together with (28) for both values of load power factor. From Fig. 8, it can be seen that, for $\cos\phi = 0$ the average error between the measured result and that calculated from (28) is 3%. When $\cos\phi = 1$ and there is a small ripple ($\kappa = 0.1$), the average error between the calculated and measured values is 5%, rising to 8% for a high ripple ($\kappa = 0.8$). As is shown in Fig. 7, the analytical expression under estimates the level of ripple current and this is also shown in the experimental results, where the measured RMS currents for $\cos\phi = 1$ are 5–10% higher than the calculated values. The greatest variation occurs for the mid-range modulation values, which is the range where the current ripple is the greatest. Overall, (28) is experimentally verified to be quite accurate in determining the capacitor RMS current due to the inverter.

6 Dimensioning of the DC-link capacitor

For the dimensioning of *C* for current stress, the data sheet specifies a maximum permissible current stress $I_{C,rms,dim}$ for a required working life of the aluminium electrolytic capacitor with dependency on the ambient temperature T_a. $I_{C,rms,dim}$ represents a fictitious current RMS value (c.f. p. 9 in [25]) which considers the decrease of R_{ESR} of an aluminium electrolytic capacitor with increasing frequency. In most cases, the value of this resistance is given for a frequency of $f = 100$ Hz ($R_{ESR,100\,Hz}$). Therefore, we have, for the losses occurring in the capacitor,

$$P_C = R_{ESR,100\,Hz} I^2_{C,rms,dim} \tag{36}$$

with

$$I^2_{C,rms,dim} = \sum_{f_i} k_{f_i} I^2_{C,(f_i),rms} \tag{37}$$

and

$$k_{f_i} = \frac{R_{ESR,f_i}}{R_{ESR,100\,Hz}} \tag{38}$$

where $I_{C,(f_i),rms}$ denotes the RMS value of the spectral component of i_C with frequency f_i; and R_{ESR,f_i} defines the value of the equivalent series resistance being given for this frequency.

According to the data sheets of aluminium electrolytic capacitors, about a constant value of $k_{f_i>10\,\mathrm{kHz}} \simeq 0.45$ is given for frequencies $f > 10$ kHz (see, for example, p. 35 in [26])). For a realisation of the inverter with IGBTs (as assumed in this paper) the switching frequency is typically set to $f_P > 10$ kHz. Therefore, the effective current stress on the DC-link capacitor caused by the inverter can be calculated simply via

$$I^2_{C,rms,1,dim} \simeq 0.45\, I^2_{C,rms,1} \tag{39}$$

There, $I_{C,rms,1}$ denotes the capacitor-current RMS value resulting for the maximum amplitude of the inverter output current. For the low-frequency components of the capacitor current that are caused by the uncontrolled rectifier bridge at the system input, a different weighting of the harmonics has to be performed according to the capacitor data sheet (see, for example, Fig. 3 in [4] or p. 37 in [26]) and/or calculated by a digital simulation.

By comparing the admissible current stress of a capacitor with the actually occurring total current stress the number of capacitors to be connected in parallel can be determined and/or a capacitor having a sufficiently high capacitance and, therefore, a relatively high maximum current rating can be chosen. Because of the larger surface of capacitors of higher capacitance (and/or higher volume), the heat-transmission resistance $R_{th,c-a}$ shows a lower value. Therefore, for a given can temperature T_c, a higher power loss $I^2_{C,rms,dim}R_{ESR}$ of the capacitor can be tolerated [see (1)]. In connection with this, note that the capacitance in the DC-link capacitor of practical systems is usually determined by the effective capacitor current stress and not, for example, by a given maximum admissible value of the amplitude of the DC-link voltage ripple. This confirms the assumption of a constant DC-link voltage made in Section 2.1.

7 Conclusions

In this paper, a simple analytical expression for the current stress on the DC-link capacitor of a three-phase PWM-converter system, as caused by the inverter stage, is derived. The DC-link capacitor-current RMS value is determined from the modulation depth and from the amplitude and the phase angle of the inverter output current assuming a sinusoidal inverter output current and a constant value of the DC-link voltage. The validity of the analytical expression is verified by digital simulation and experimentally. Even with a large current ripple in the output current, the average error between the analytical result and the simulated and experimental results is less than 8% for the full range of modulation indices. Therefore the analytical expression meets the accuracy requirements for designing the DC-link capacitor for practical IGBT inverter systems.

8 Acknowledgment

The authors thank Thomas Wolbank and Manfred Schrödl of the Department of Electrical Drives and Machines, Technical University of Vienna, for their participation in discussions on this topic.

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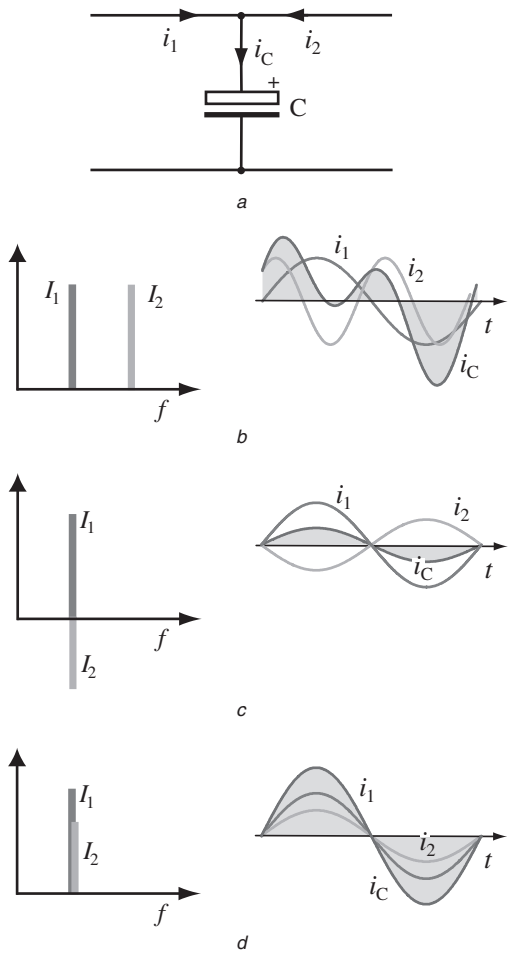

Fig. 9 *Capacitor RMS-current determination for uncorrelated and correlated input and output currents*
a Simplified circuit
b Uncorrelated input and output currents $I_{C,rms} = \sqrt{(I_{1,rms}^2 + I_{2,rms}^2)}$
c Out-of-phase but same frequency currents $I_{C,rms} = I_{1,rms} - I_{2,rms}$
d In-phase currents $I_{C,rms} = I_{1,rms} + I_{2,rms}$, which produces the worst-case capacitor-RMS-current value

10 Appendix: Calculation of worst-case RMS current stress on DC-link capacitor

Using Fig. 9*a* the capacitor current is defined as

$$i_C = i_1 + i_2 \tag{40}$$

The direction of the current is defined differently from that in Fig. 1 to simplify understanding, and it has no influence on the result.

The RMS capacitor current is calculated as

$$\begin{aligned} I_{C,rms}^2 &= \frac{1}{T_N}\left(\int_{T_N} i_1^2 dt + 2\int_{T_N} i_1 i_2 dt + \int_{T_N} i_2^2 dt\right) \\ &= I_{1,rms}^2 + 2\int_{T_N} i_1 i_2 dt + I_{2,rms}^2 \end{aligned} \tag{41}$$

The upper limit of the integral of the product of i_1 and i_2 is determined from the Cauy–Schwarz inequality:

$$\left|\int f \cdot g\, dx\right|^2 \leq \left(\int f^2 dx\right)\left(\int g^2 dx\right) \tag{42}$$

Therefore,

$$\left(\int i_1 i_2 dt\right)^2 \leq \left(\int i_1^2 dt\right)\left(\int i_2^2 dt\right) = I_{1,rms}^2 I_{2,rms}^2 \tag{43}$$

and

$$\begin{aligned} I_{C,rms}^2 &\leq I_{1,rms}^2 + 2I_{1,rms}I_{2,rms} + I_{2,rms}^2 \\ &= (I_{1,rms} + I_{2,rms})^2 \end{aligned} \tag{44}$$

or finally

$$I_{C,rms} \leq I_{1,rms} + I_{2,rms} \tag{45}$$

This is graphically shown in Fig. 9*d* by the capacitor current being formed from the sum of the individual in-phase (correlated) currents. For uncorrelated (different fundamental frequencies) currents (Fig. 9*b*) the capacitor RMS current is $I_{C,rms} = \sqrt{(I_{1,rms}^2 + I_{2,rms}^2)}$.