# Parallel Interleaved Inverters for Reactive Power and Harmonic Compensation

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***Abstract* – This article investigates the concept of paralleling power inverters for reactive power and harmonic compensation. The investigation focuses on a topology that shares the dc-bus capacitor between two parallel interleaved inverters. The advantages of the proposed approach are: i) decreased current ripple or use of lower switching frequency due to the interleaving, ii) reduced stress in dc-link capacitor due to the shared connection, iii) efficient implementation for high power applications because of paralleling. Different comparisons between the selected topology and regular power converters are discussed. Practical tests, on a three-phase 5 kVA, 400 V prototype, are presented to validate the analysis.**

***Keywords – interconnected power systems; pulse width modulated inverters; reactive power; power system harmonic; active filters.***

## I. INTRODUCTION

The demand of high power in power electronics is usually limited by the available semiconductor technology, due to the maximum allowed current, voltage, losses and switching frequency. One solution to cope with the required power is to build the power converter from multiple lower power units connected in parallel, either connecting multiple power switches or multiple inverters in parallel [1]–[3].

This paper discusses the connection in parallel of multiple inverters. Some arguments to support the paralleling concept are briefly described such as it is easier to extend the total rated power of the application by simply adding a new inverter. The design, production, installation and maintenance of each inverter become much simpler and flexible. Furthermore, parallel inverters may be physically implemented as independent controlled modules, which give the entire power unit an intrinsic redundancy feature, providing ride-through functions when a module fails (Fig. 1).

There are many parallel topologies described in the literature, for different fields especially where a high power density integration is required, such as power sources, traction systems, uninterruptible power supplies [4], power factor correction circuits and active power filters (APF) [5], [6].

Regarding the compensation of the reactive power, different considerations [7], [8] are currently discussed, proposing that the users supplying reactive power should be paid since they provide voltage regulation and reduction of the power losses.

This movement creates a potential market for high power reactive compensation devices, motivating the production of efficient reactive power units. Thereby, the research may be leaned in finding new topologies with cheaper passive components, higher power integration, higher redundancy and lower EMI [9].

The present work analyzes the application of parallel-interleaved inverters for reactive and harmonic current compensation. The topology consists of a parallel connection of (two) identical three-phase interleaved PWM inverters, sharing the same dc-capacitor as depicted in Fig. 1.

Several issues are presented and discussed in the paper; like reduction of the switching current ripple, the use of smaller passive components and the implementation of different modulation strategies to reduce the EMI. The design of the selected topology is discussed by comparing it to regular power inverters.

The results obtained show that for the proposed topology the line inductors are reduced almost to 60% comparing to a typical there-phase PWM inverter. Furthermore, if the topology is to be used for reactive power compensation then the dc-capacitor is reduced to 25%, due to the decrease of dc-current ripple.

As the present technology in IGBT's allows for switching frequencies typically of 10 kHz – 20 kHz, it opens the possibility of a reactive power compensator mainly composed of semiconductors with very small passive components. Hence, the usage of smaller passive components and the possibility of building it as a modular device makes this topology very attractive for high power industrial applications.

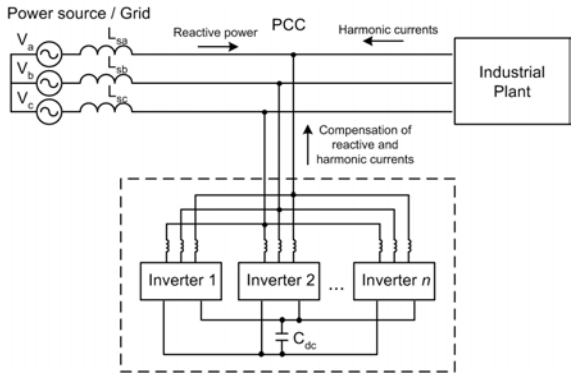



Fig. 1. Principle diagram of paralleling *n* multiple power inverters. All inverters share the same capacitor $C_{dc}$.

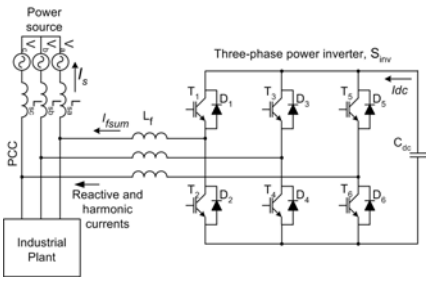



Fig. 2. Typical active front-end inverter topology (Case-A).

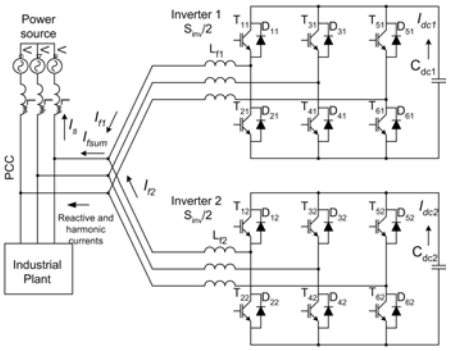



Fig. 3. Diagram of 2 separated parallel inverters with split dc-capacitors (Case-B).

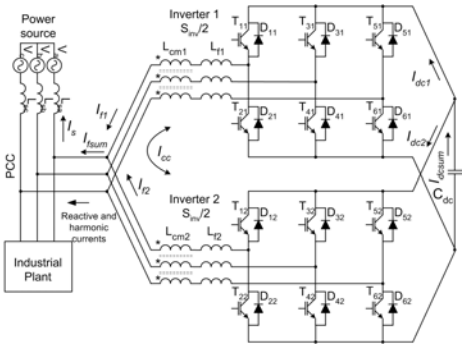



Fig. 4. Diagram of the analyzed topology with 2 parallel interleaved inverters sharing the same dc-capacitor (Case-C).

## II. Analysis and Design

This section gives the design of the selected topology. The main focus is put on the line inductance and the dc-capacitor, which are designed based on some initial considerations. The assumptions are that the design is carried out initially for sinusoidal output current and then after the obtained design is extended for active power filters, where the inverters control non-sinusoidal currents. Both parallel inverters are running with the same switching frequency, and the inverters have the same power rating, thus the total output power is equally divided between them. Three cases are studied:

- Case-A – single unit inverter (typical three-phase inverter as shown in Fig. 2),
- Case-B – parallel connection of 2 interleaved inverters with split dc-capacitors (as in Fig. 3),
- Case-C – parallel connection of 2 inverters, both sharing the same dc-capacitor (as in Fig. 4).

Several criteria are imposed, for having the same base of comparison between the selected topologies (see Fig. 5 and Table I): line-to line voltage $V_{LL}$ is set to 1 per unit (pu), total output power $S_{inv}$ of 1 pu (consequently the total current delivered to the source $I_{inv}$ of 1 pu), line current ripple is limited to $\Delta i_{max}$, voltage ripple across the dc-capacitor is limited to $\Delta v_{max}$.

The design is carried on along with different practical tests on a laboratory setup described in §V. The values of the line inductors are 5 % (i.e. 5 mH) for Case-A and 3 % (i.e. 3 mH) for Case-B and -C. The total line current $I_{inv}$ is 6 $A_{peak}$.

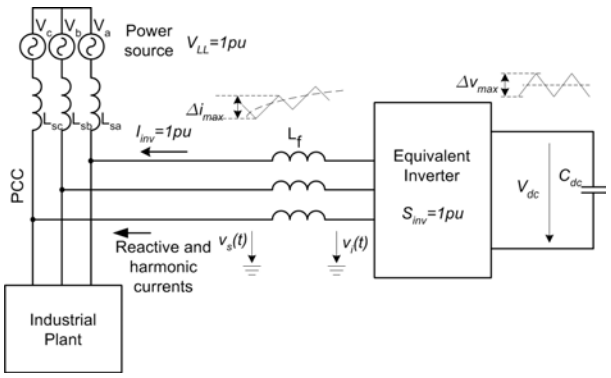



Fig. 5. Imposed criteria used for designing the power inverter.

TABLE I. Input parameters used in design and testing (see Fig. 5).

| Parameter | Symbol | Normalized value | Test values |
|---|---|---|---|
| Inverter power | $S_{inv}$ | 1 pu | 4.8 [kVA] |
| Line voltage | $V_{LL}$ | 1 pu | 400 [V] |
| Line current (peak) | $I_{inv\ (pk)}$ | 1.42 pu | 10 [$A_{peak}$] |
| Line current (RMS) | $I_{inv}$ | 1 pu | 7 [$A_{RMS}$] |
| Current ripple (peak) | $\Delta i_{max}$ | 20 %$I_{inv\ (pk)}$ | 2 [$A_{pk\text{-}pk}$] |
| Ratio of current ripple | $K_{If} = \Delta i_{max}/I_{inv}$ | 0.28 pu | 0.28 pu |
| Base impedance | $Z_b = V_{LL}/\sqrt{3}\ I_{inv}$ | 1 pu | 33 [Ω] |
| Ratio of line inductors | $K_{Lf} = 2\pi f_1 L_f/Z_b$ | - | - |
| Ratio of common mode coils | $K_{Lcm} = 2\pi f_1 L_{cm}/Z_b$ | - | - |
| DC-voltage | $V_{dc}$ | 1.8 pu | 700 [V] |
| Ratio of dc-voltage | $K_{Vdc} = V_{dc}/V_{LL}$ | 1.8 pu | 1.8 pu |
| DC-voltage ripple | $\Delta v_{max}$ | 1-2 % · $V_{dc}$ | 10 [V] |
| Line frequency | $f_1$ | 1 | 50 [Hz] |
| Switching frequency | $f_{sw}$ | 204 | 10.2 [kHz] |
| Ratio of switching freq. | $K_{fsw} = f_1/f_{sw}$ | 204 | 204 |
| Duration of zero vector | $t_0$ | - | - |
| Ratio of zero vector | $K_{t0} = t_0/T_{sw}$ | - | - |

### A. Line Inductor

The design of the inductor is based on the imposed line current ripple, which depends on the existing dc-voltage, modulation strategy and switching frequency as used in (1). There are different methods to calculate the value of the switching current ripple as a function of the modulation strategy and the desired line inductor [12]. A previous study [13] investigates a simplified method for calculation of the line inductor, based on the equivalent model of the inverter in each commutation states. The value of the line inductor $X_f$ for Case-A is finally obtained as in (3).

$$v_s(t) = L_f \frac{di_f(t)}{dt} + v_i(t) \tag{1}$$

$$\Delta i_{\max} = 2\frac{V_{dc}\cdot\Delta t}{3L_f} = 2\frac{K_{Vdc}V_{LL}\cdot\Delta t}{3L_f} \tag{2}$$

$$X_f^{(CASE-A)} = \omega_1 L_f = \frac{4\pi K_{Vdc}}{\sqrt{3}K_{If}}\cdot\underbrace{\frac{V_{LL}}{\sqrt{3}I_{inv}}}_{Z_b}\cdot\underbrace{\frac{f_1}{f_{sw}}}_{1/K_{fsw}} = \frac{4\pi K_{Vdc}}{\sqrt{3}K_{If}}\cdot\frac{Z_b}{K_{fsw}} \tag{3}$$

For Case-B and Case–C, the inductor is designed using the same equation as in (1) separately applied for each inverter. The total line current is the summation the individual inverter currents.

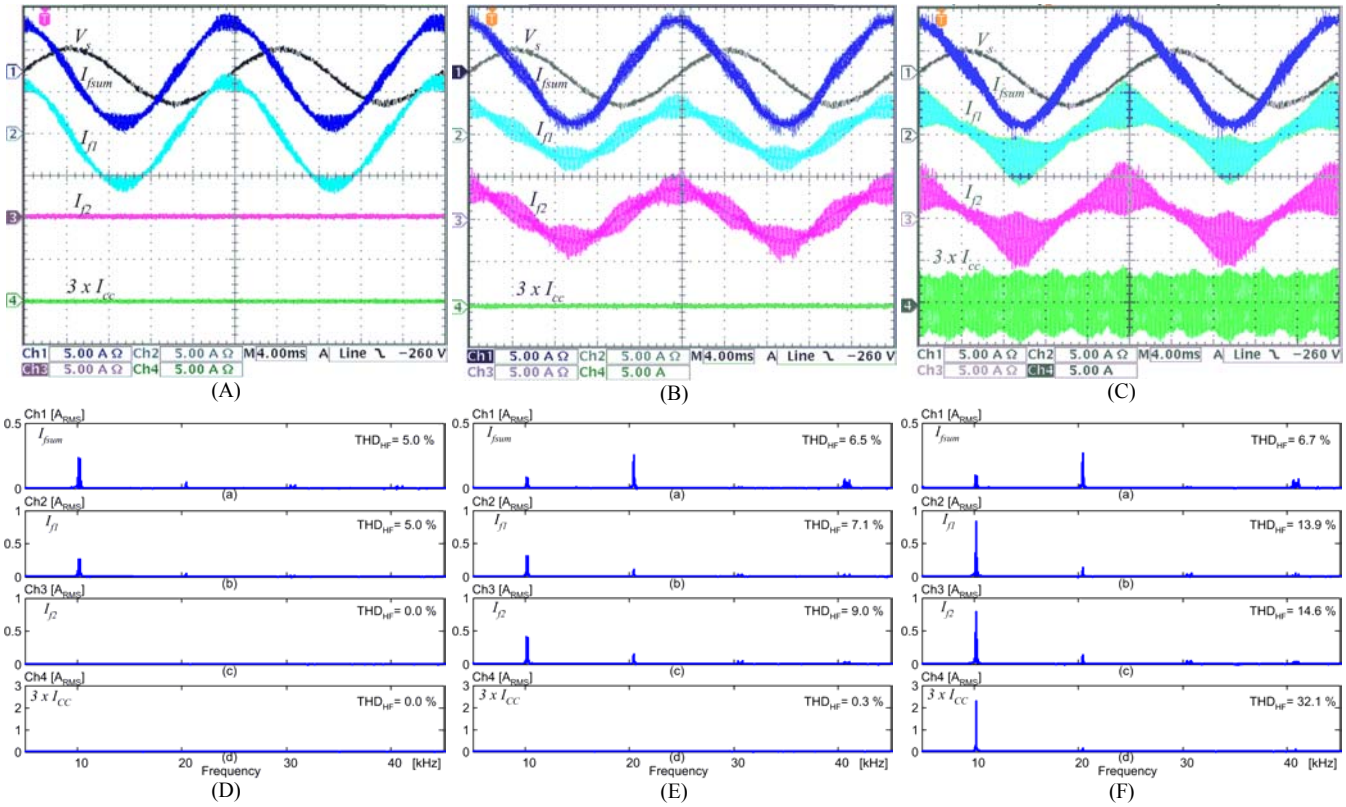



Fig. 6. Measured line currents for a reference current of 6 $A_{peak}$ reactive current and sinusoidal PWM modulation: A) Case-A, B) Case-B, C) Case-C; D), E), F) harmonic current spectrum for each measured current focused at the switching frequencies.

It is proven in [13] that the total line current ripple ($I_{fsum}$ in Fig. 3) is reduced due to the interleaving, to a fraction of 0.6 times individual inverter's ripple. Or vice versa, if the line current ripple is maintained as imposed in Table I, then the inductors can be reduced by the same amount, as given in (4).

$$X_f^{(Case-C)} = X_f^{(Case-B)} = 0.6 \cdot X_f^{(Case-A)} \tag{4}$$

When connecting the inverters in parallel, cross-currents circulate from one inverter to the other, depending on the inverters' switching states. If the power source is stiff, (i.e. low short-circuit impedance), then the cross-currents in Case-B are negligible, because the current ripple generated by each inverter sinks into the grid.

However, for Case-C, because there is no galvanic isolation between inverters and they share the dc-capacitor $C_{dc}$, there is a circulation current (referred to as cross-current $I_{cc}$ in Fig. 6C) that occurs due to the opposite zero vectors $v_7$ and $v_0$ [13]. The cross-current $I_{cc}$ is the natural consequence of interleaving the carriers by 180°.

There are 2 important effects of the cross-current. The first effect is the increase of the current peak value in each inverter as it will described next. The second effect is the risk that may appear in the case of a small unbalance between inverters (e.g. different line inductances, different duty cycles), which determines a lower frequency current circulating between inverters as a zero-sequence current [14]. Since the zero-sequence current is of a low frequency, a proper controller designed for the zero-axes can remove it. However, a current controller cannot mitigate the first effect, since its frequency is given by the switching frequency. The amplitude of the cross-currents can be calculated as in (5).

Fig. 6 shows the time- respective the frequency domain waveforms of the measured currents for all three cases. The line current ripple in Case-B and -C is near the same as the ripple in Case-A, even though the line inductors are decreased to 60 % in Case-B and -C. The cross-current $I_{cc}$ can also be seen in Case-C.

Different solutions can be found to reduce or eliminate the cross-currents as like: galvanic isolation transformer [6], separate dc-capacitors [15], inter-phase coils on the dc-bus, higher switching frequency PWM strategies [16].
Most of these solutions have different drawbacks, for instance the galvanic isolation transformer must be designed for higher frequency and rated at the total nominal current; the inter-phase coils must carry a dc-current which is difficult to design in respect the core saturation limits; the increase in the switching frequency may also be limited in practice.

The solution applied here is the use of common mode coils ($L_{cm}$ in Fig. 4) to provide a high impedance path for circulating cross-currents.

$$V_{dc} = \left(L_{f1} + L_{f2} + L_{cm1} + L_{cm2}\right)\frac{\Delta i_{cc}(t)}{t_0(t)} \tag{5}$$

where: $V_{dc}$ is the voltage on the dc-capacitor, the $L_{f1}$, and $L_{f2}$ are the values of the line inductors, $\Delta i_{cc}$ is the amplitude of the cross-current developed during the interval $t_0$ which depends on the duration of the zero vectors.

$$I_{cc} = \frac{2\sqrt{3}\pi K_{Vdc} K_{t0}}{2(K_{Lf} + K_{Lcm})} \underbrace{\frac{V_{LL}}{\sqrt{3}Z_b}}_{I_{inv}} \underbrace{\frac{f_1}{f_{sw}}}_{1/K_{fsw}} = \frac{\sqrt{3}\pi K_{Vdc} K_{t0}}{(K_{Lf} + K_{Lcm}) K_{fsw}} I_{inv} \tag{6}$$

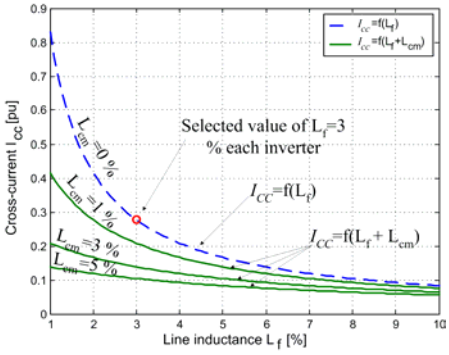



Fig. 7. Cross-current $I_{cc}$ as a function of both inductances: inverter inductance $L_f$ respective common mode inductance $L_{cm}$.

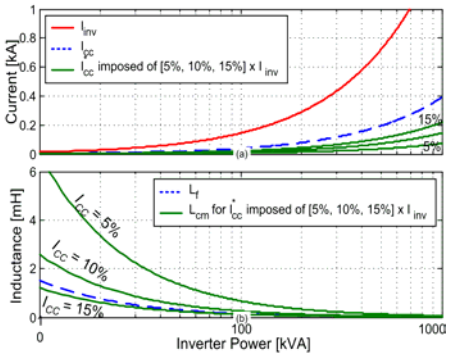



Fig. 8. Currents and inductances in Case-C as functions of the inverter power a) Line current and cross-current. b) Line inductance (3 %) and common mode inductance.

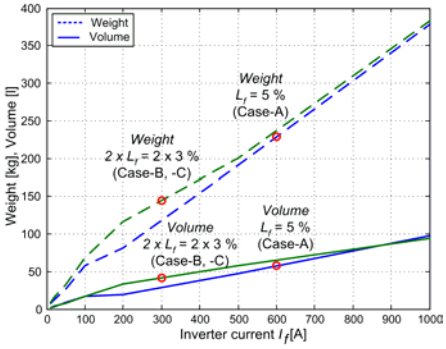



Fig. 9. Evaluation of the weight and volume of 2 inductors of 3 % (Case-C) and an inductor of 5 % (Case-A) for different values of the inverter current $I_f$.

As indicated in (6), the cross-current depends on the size of both, line inductor ($L_f$) and the installed common-mode inductor ($L_{cm}$). Fig. 7 presents how the cross-current develops along with the line inductance. It can be seen that a larger common-mode inductor can effectively reduce the cross-current. For instance, for a value of 3 % line inductance alone, the cross current is about 0.3 pu, while installing an additional common-mode inductance of 3 % reduces the cross-current to near 0.1 pu.

Another calculation example of the common-mode inductor is given in Fig. 8. Here the size of the common-mode inductor is selected based on the desired value of the cross-current. For a cross-current $I_{cc}$ of 15 % out of the total inverter current, the common mode inductor has almost the same absolute value as the line inductor. If one designs the application for lower cross-current, then the value of the common-mode inductor should be highly increased. For an allowed cross-current value of only 5 %, the common-mode inductor is almost 3 times higher.

As previously calculated, the line inductors are reduced to 60 % by interleaving the carriers, in order to keep the same amplitude for the line current ripple. However, as Case-A uses a single three-phase inductor, while Case-B and -C use two pairs, the design demands more analysis if this is economically feasible. In practice, the weight, size, and cost of the inductors are of a major concern. They all depend on many parameters, like the magnetic core, type of windings, manufacturing technology, desired tolerance and required operating conditions. These are difficult to analyze from a simple approach, but it is assumed that the relation between inductors maintains the same.

An evaluation is given in Fig. 9 for two types of inductors, one of 5 % (as in Case-A) and the other of 3 % (as in Case-B or -C). The inductors are calculated as in [17] using laminated iron core, sinusoidal line current and an operating temperature of 25 °C. The calculations did not consider the required increase of the inductor size in order to cope with the heat caused by the power losses in core and windings, thus the inductor size increases almost linear with the current [17].

Fig. 9 shows that the weight of a 5 % inductor rated for 600 Amps is higher than the weight of 2 inductors of 3 % rated for 300 Amps each. Their volume is also in the same ratio. However, as Case-C has supplementary common mode inductors, their weight and volume must also be considered. It is expected that the common-mode inductors may not be very large since their core must be designed mainly for common-mode signals and not the nominal inverter current. On the other hand the use of common-mode coils is a common practice in industry for protecting the inverters against common mode noise signals from the grid, thus such inductors are used anyway.

### *B. DC-link Capacitor*

When the inverter provides only reactive current the capacitor may be sized based on the dc-voltage ripple caused by the switching frequency. As a general approach the minimum required dc-capacitor is determined as:

$$C_{dc,\min} = \frac{\int_{t1}^{t2} i_{dc}(t)\,dt}{\Delta v_{\max}(t)}, \; i_{dc}(t) = s_a(t)\cdot i_a(t) + s_b(t)\cdot i_b(t) + s_c(t)\cdot i_c(t), \tag{7}$$

where $i_{dc}(t)$ and $v_{max}(t)$ are the capacitor current and voltage ripple; $s_a$, $s_b$, $s_c$ are the switching functions, and $i_a(t)$, $i_b(t)$, $i_c(t)$ are the line currents.

If some simplified assumptions are considered such that the integration time interval ($t_1$, $t_2$) is half of the switching period $T_{sw}$ and the dc-current ($I_{dc}$) is half of the peak value of the nominal line current [12], then the minimum required dc-capacitor for Case-A is:

$$C_{dc,\min}^{(Case-A)} = \left(\frac{1}{2}\frac{\sqrt{2}I_{inv}}{\Delta v_{\max}}\right)\cdot\frac{T_{sw}}{2} = \frac{1}{2\sqrt{6}f_1 K_{dc\max} K_{Vdc} K_{fsw}}\frac{1}{Z_b} \tag{8}$$

For Case-B, the dc-current in each capacitor is half of the total line current, because of the power sharing, which makes the ripple of the dc-voltage half as calculated in Case-A. Or vice-versa, if the dc-voltage ripple is kept constant, then the capacitor can be reduced to half.

In Case-C, since the capacitor is shared between two interleaved inverters, the instantaneous dc-current is half of Case-A and its frequency is doubled. This makes the capacitor 4 times lower than in Case-A.

$$C_{dc,\min}^{(Case-B)} = \frac{C_{dc,\min}^{(Case-A)}}{2}, \text{ and } C_{dc,\min}^{(Case-C)} = \frac{C_{dc,\min}^{(Case-A)}}{4} \tag{9}$$

If the application is an active filter, then the capacitor value should be calculated to cope with a certain value of dc-voltage drop caused by the load variation.

$$C_{dc}^{(Case-A)} = \frac{V_{LL}\Delta I_{inv}}{2\sqrt{3}\left(V_{dc,drop}^2 - V_{dc}^2\right)f_1} \tag{10}$$

where $\Delta I_{inv}$ is the step increase in the real fundamental line current; $V_{dc,drop}$ is the maximum allowed variation of the dc-voltage.

This means that the required capacitance is much larger than the value in (8) [18]. For Case-B, the dc-capacitor is still half of Case-A because the inverter power is half. However, for Case-C the dc-capacitor is the same as in Case-A, because the same amount of power is required to be stored in dc-link in order to cope with the load variation.

Another important issue when designing the capacitor is the current stress. Different methods are proposed in literature, either spectral analysis or simulations [12]. The dc-current determines specific power losses in the capacitor as in (11) and consequently an increase of the capacitor temperature as in (12), thus decreasing its lifetime.

$$P_{Cdc} = \sum_h \left(P_{ESR}(h)\right) = \sum_h \left(R_{ESR}(h)\cdot I_{C,RMS}^2(h)\right) \tag{11}$$

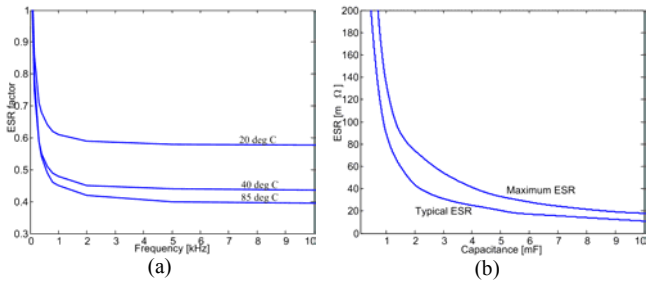
$$T_{Cdc} = T_a + P_{Cdc}\cdot R_{th} \tag{12}$$

where $T_{Cdc}$ and $T_a$ are the capacitor respective ambient temperatures, $R_{ESR}(h)$ and $I_{C,RMS}(h)$ are the equivalent series resistance respective the RMS current of the capacitor at different harmonic orders $h$.

The equivalent series resistance ($R_{ESR}$) decreases whenever one of the following increases: ambient temperature $T_a$, ripple current, current frequency, capacitor can size, and capacitance (for the same can size) [19]. Variation of $R_{ESR}$ with the frequency is only of a small amount, and practically it can be considered constant for any frequency higher than 2-3 kHz. Its value is averaged to 0.45 times the $R_{ESR}$ value for 100 Hz at 20°C (see Fig. 10a). On the other hand, the variation of $R_{ESR}$ with the capacitance is much larger, reaching a difference of almost 2 times, if one compares the $R_{ESR}$ of a given capacitor to its double value (see Fig. 10b).

If one splits the power losses from (11) into low order harmonics ($P_{Cdc}^{LF}$ caused mainly by the control) and high order harmonics ($P_{Cdc}^{HF}$ caused by the switching frequency), and takes into account that the ESR is almost constant for higher frequencies, then it can be proven that high frequency power losses are directly dependent on the total harmonic distortion ($THD_{HF}$) calculated as in (13).

$$P_{Cdc}^{HF} = 0.45\cdot R_{ESR(100Hz)}\cdot I_{C,RMS}^2 \underbrace{\sum_{h>50}\left(\left(\frac{I_{C,RMS}(h)}{I_{C,RMS}}\right)^2\right)}_{THD_{HF,h>50}^2} \tag{13}$$




(a) (b)

Fig. 10. Excerpt from capacitor datasheets showing the dependence of ESR with the frequency and capacitance [19].

Thus, the comparison between Case-A, -B, -C, resumes to the calculation of the $THD_{HF}$ caused by the switching frequency. The spectrum of the measured dc-current is calculated for all three cases in Fig. 11.

For Case-A the $THD_{HF}$ is double compared to Case-B, but only one of the capacitors is measured in Case-B, Since the capacitor is of a lower capacitance, the equivalent $R_{ESR}$ is almost double, and thus the total power losses for both capacitors together in Case-B is near the same as the value calculated in Case-A. In order to reduce the losses the capacitor, its capacitance must be increased but this is not economically viable.

For Case-C the $THD_{HF}$ is half and there is only one dc-capacitor. This indicates that the total current stress in Case-C is reduced to 25 % compared to Case-A. However, if the capacitor is 4 times lower (i.e. $R_{ESR}$ 4 times higher), the total power losses would be the same. Therefore, the capacitor may be selected for example only 2 times lower instead of 4 times, which is sufficient enough to reduce the losses to half.

### C. Inverter rating

The rating of the inverter is determined by calculating the IGBT currents. The cross-current changes the shape of the IGBT current with a possible increase of the switching and conduction power losses. However, simulation of the inverter for different common mode inductors shows that the RMS value of the IGBT current has insignificant changes, but only the peak value increases (see Table IV and Fig. 12), [13].

## III. Control Structure

The control algorithm may be developed in different ways, either in stationary or synchronous frames. Here the last was selected for implementation [13]. A typical control diagram for Case-A is given in Fig. 13a, which has a current controller (*Reg* $I_{dq}$) in the inner loop and a voltage controller (*Reg* $V_{dc}$) in the outer loop.

For active harmonic filtering applications the load current is also measured and the harmonic currents are isolated and imposed as current reference ($I_{HRef}$) by the harmonic detection block. For Case-B, since there are 2 independent inverters, the control of each is self-regulating, which means that the overall implementation of the control is twice as in Fig. 13a.

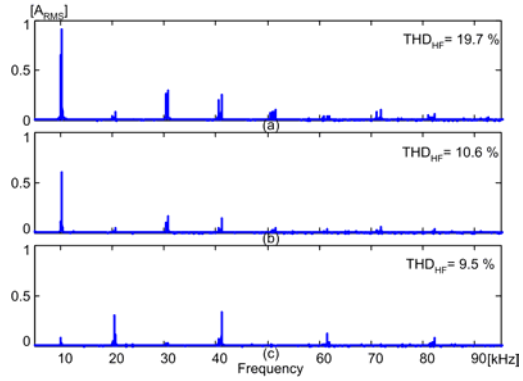



Fig. 11. Measured harmonic spectrum of the dc-currents for a) Case-A, b) Case-B at only one of the inverter, c) Case-C.

The control diagram for Case-C is particular because of the shared dc-capacitor. Thus, there are two additional issues, the zero sequence current and the common dc-voltage regulation.

In a typical three-phase three-wire stand-alone inverter the zero-sequence current generated by the zero vectors does not flow, but in the existing topology with parallel inverters there is a circulating cross-current as explained in §II. Even if the average of the cross-current theoretically is zero during one fundamental period, any small difference between the inverters determines a lower frequency current circulating between them. The zero-sequence current is removed by a current controller placed on zero-axis (*Reg* $I_z$), which keeps a null average of the zero sequence current [14].

As both inverters use the same dc-capacitor there is one single voltage control loop. The output of the voltage controller is equally divided to be the reference for both inner current controllers. This creates a balance in the power losses dissipation for both inverters and also assures closer symmetry in the voltage references for each inverter, which is needed in order to have a good cancellation in the current ripple. For the same reason the harmonic current reference is equally divided for each inverter.

## V. Experimental Results

All three cases are evaluated on an existing laboratory stand used for compensation of both reactive power and harmonic current distortion. The setup consists of 2 paralleled inverters of a total power of 5 kVA, working at 10.2 kHz switching frequency. The line inductors are set as $L_f$=5 mH for Case-A and $L_f$=$L_{f1}$=$L_{f2}$=3 mH for Case-B and -C.

The common mode inductors in Case-C are set to $L_{cm1}$= $L_{cm2}$=2 mH. Some of the measurements are already presented in §II regarding the generation of the reactive power (Fig. 6).

Initially the design of the inverter in §II was done for a sinusoidal modulation strategy (SPWM). Other types of modulations are also practically tested as it can be seen in Fig. 14A: space vector modulation (SVM), discontinuous modulation with different types of switch clamping (DPWM1 and DPWM3) [12].

Fig. 14B and Fig. 14C show the simulated line current ripple as power factor correction (PFC) for Case-A with a line inductor of 5 mH respective for Case-B with a line inductor of 3 mH each inverter. As it can be seen, the maximum value of the line current ripple is near the same for SPWM (and also DPWM3), which validates the design. For the SVM and DPWM1 the ripple increases. For Case-C the line current ripple is similar for SPWM and SVM. However, discontinuous modulations cannot be implemented [16] because cross-currents cannot be regulated, as there are no alternative zero vectors $v_0$ and $v_7$ during one switching period.

Table II indicates the losses measured of the total inverter in each case for all four modulation strategies. Case-C has always higher losses because of there are 2 inverters (thus, involving switching and conduction losses) but also because of the circulation of the cross-current that increases the losses in the line inductors.

Fig. 15 shows the mitigation of the harmonic currents and the spectrum of the line current $I_s$ (see also Fig. 4), which indicates that the switching frequency is reduced for Case-B and -C. Different other results are collected in Table III.

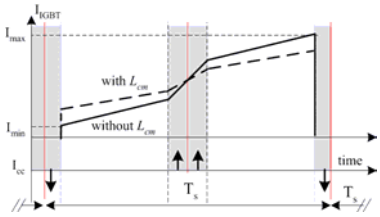
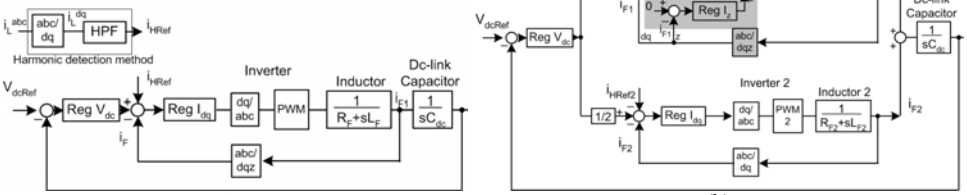
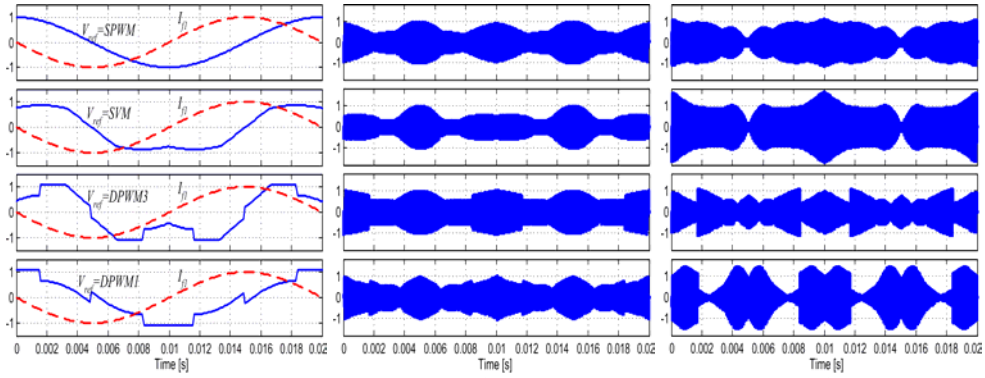



Fig. 12. Representation of the IGBT current during one commutation period.




(a) (b)

Fig. 13. Diagram of the control in dq-reference frame for a) Case-A, b) Case-C.



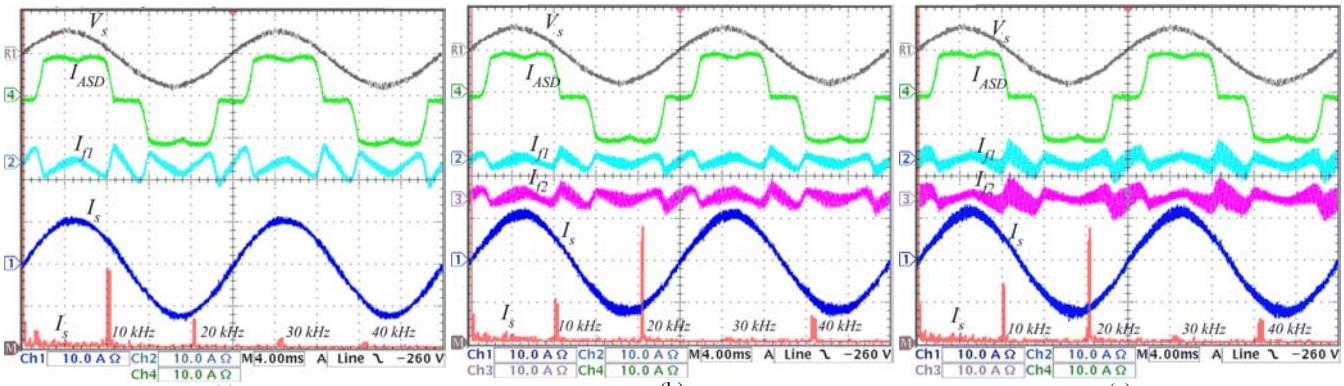

(A) (B) (C)

Fig. 14. Simulated line current ripple for different PWM strategies. a) sin-PWM b) space vector modulation SVM, c) and d) discontinuous PWM (DPWM1,3). A) voltage reference, B) line current ripple in Case-A for $L_f$ of 5 %, B) line current ripple in Case-B for $L_{f1}$, $L_{f2}$ of 3 %.

TABLE II. Measured power losses of the total inverter for different modulation strategies tested on the existing setup.

| Losses [%] vs. modulation | | Case-A | Case-B | Case-C |
|---|---|---|---|---|
| Reactive power | SPWM | 3.8 | 5.1 | 6.5 |
| | SVM | 4.8 | 3.7 | 5.8 |
| | DPWM1 | 3.4 | 5.3 | 8.2* |
| | DPWM3 | 3.2 | 3.5 | 6.2* |
| Harmonic filtering | SPWM | 2.8 | 3.4 | 7.1 |
| | SVM | 2.6 | 3.1 | 6.6 |
| | DPWM1 | 2.4 | 3.0 | 8.0* |
| | DPWM3 | 2.2 | 2.9 | 6.7* |

* practically not viable because of the strong cross-current [16].




(a) (b) (c)

Fig. 15. Measured waveforms for mitigation of harmonic currents generated by an Adjustable Speed Drive of 2.5 kVA a) Case-A, b) Case-B, c) Case-C.

TABLE III. Comparison of the selected topologies for an inverter power $S_{inv}$=3 kVA and a switching frequency of 10.2 kHz.

| Parameter | Case-A | Case-B | Case-C* |
|---|---|---|---|
| Front line inductor value ($L_f$) | 0.05 pu | 0.03 pu | 0.03 pu |
| DC-link capacitor value ($C_{dc}$) | 0.62 pu | 0.31 pu | 0.15 pu |
| Total power flow in each inverter ($S_{inv}$) | 1.00 pu | 0.50 pu | 0.50 pu |
| Total line current distortion ($THD_i$) | 6.5 % | 8.4 % | 8.9 % |
| 1st switching frequency harmonic of $I_{fsum}$ | 5.6 % | 2.0 % | 2.1 % |
| 1st switching frequency harmonic of $I_{f1}$ | 5.6 % | 7.2 % | 18.2 % |
| Current rating for one IGBT [$A_{rms}$] | 0.53 pu | 0.28 pu | 0.29 pu |
| Maximum current for one IGBT [$A_{pk}$] | 1.15 pu | 0.75 pu | 0.90 pu |

* tested for a common mode inductor $L_{cm}$ of 2 mH.

## VI. Conclusion

This paper discusses a parallel topology of 2 three-phase power inverters connected in parallel and sharing the same dc-capacitor. A comparison of the selected topology with a regular three-phase inverter for application is presented for reactive power and harmonic compensation. The paper gives different design specifications, which prove that for the selected topology the passive components are significantly reduced. Simulation and experimental results for a 400V/5kVA unit validates the presented analysis.

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