Very High Frequency PWM Buck Converters Using Monolithic GaN Half-Bridge Power Stages With Integrated Gate Drivers

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***Abstract*—Integration is a key step in utilizing advances in GaN technologies and enabling efficient switched-mode power conversion at very high frequencies (VHF). This paper addresses design and implementation of monolithic GaN half-bridge power stages with integrated gate drivers optimized for pulsewidth-modulated (PWM) dc–dc converters operating at 100 MHz switching frequency. Three gate-driver circuit topologies are considered for integration with half-bridge power stages in a 0.15-μm depletion-mode GaN-on-SiC process: an active pull-up driver, a bootstrapped driver, and a novel modified active pull-up driver. An analytical loss model is developed and used to optimize the monolithic GaN chips, which are then used to construct 20 V, 5 W, 100 MHz synchronous buck converter prototypes. With the bootstrapped and the modified pull-up gate-driver circuits, power stage efficiencies above 91% and total efficiencies close to 88% are demonstrated. The modified active pull-up driver, which offers 80% reduction in the driver area, is found to be the best-performing approach in the depletion-mode GaN process. These results demonstrate feasibility of high-efficiency VHF PWM dc–dc converters based on high levels of integration in GaN processes.**

***Index Terms*—Circuit optimization, gallium nitride power devices, GaN integrated circuits, modeling, monolithic power converters, switched-mode power converters, VHF amplifiers.**

I. Introduction

RECENT advances in dc–dc converters operating at radio frequencies (RF) have been enabled by advances in device technologies, circuit configurations, and circuit design techniques. In particular, wide bandgap (GaN, SiC) devices and technologies are opening possibilities to efficiently operate switched-mode power converters at very high frequencies (VHF). These opportunities depend on advances in power-stage circuits, gate-drive design techniques, as well as integration and packaging steps. Some dc–dc converters, such as boost, SEPIC, Ćuk, class-E^2, etc., use a source-grounded transistor, which simplifies applications of RF-based circuit design techniques [1]–[11]. Half-bridge power stages, however, are found in many important power converter configurations, including synchronous buck converters and many other half-bridge and full-bridge-based topologies. In the half-bridge stage, realization of the high-side driver capable of supporting very high switching frequencies is particularly challenging. Using discrete GaN devices and discrete gate-drive circuit design techniques, high efficiency operation has been demonstrated at switching frequencies in the 10–40 MHz range [12]. To support even higher switching frequencies, it is necessary to consider power stage and gate driver integration techniques, in order to mitigate effects of parasitic capacitances and inductances, and losses associate with level-shifting of the high-side control signal. A 200 MHz converter with integrated bootstrap driver using 0.25-μm GaN high electron mobility transistors (HEMTs) has been shown to have 73% overall efficiency in an envelope-tracking application [13]. An integrated driver using resistive pull-up technique in a 0.7-μm GaN process has been described in [14], leading to 64% overall efficiency when the converter is used as an envelope-tracking amplifier. Higher levels of integration are also pursued by industry, such as monolithic half-bridge stages [15] and devices with co-packaged gate drivers [16].

The objectives of this paper are to introduce and compare several options for monolithic integration of gate drivers and half-bridge power stages, and to present a loss-model-based design optimization approach for such monolithic GaN chips in a 0.15-μm depletion-mode (normally on) GaN-on-SiC process (Qorvo TQGaN15 [17]). The gate-drive options considered include an active pull-up driver, a bootstrapped driver, and a modified active pull-up driver [18], [19]. The modified active pull-up driver is shown to offer efficiency and area advantages over the active pull-up and the bootstrapped designs, respectively. Furthermore, an analytical loss model is presented, allowing design optimization of monolithic half-bridge stages with integrated gate drivers. The monolithic GaN chips and the design optimization approach are verified by experiments on 20 V, 5 W synchronous buck converters operating at 100 MHz switching frequency. Fig. 1 shows the converter diagram used for demonstration and experimental verification. The design using the integrated modified active pull-up driver is shown to have greater than 91% peak power-stage efficiency.

This paper is organized as follows: Section II briefly summarizes the GaN process and the device characteristics, and introduces the operating principles of the active pull-up, bootstrapped, and modified active pull-up driver circuits. Section III presents the analytical loss model and the efficiency optimization approach, with application details given for the monolithic

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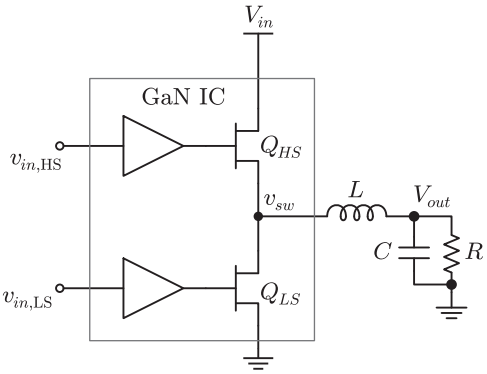


Fig. 1. Synchronous buck converter based on the monolithic GaN half-bridge chip with integrated gate drivers.

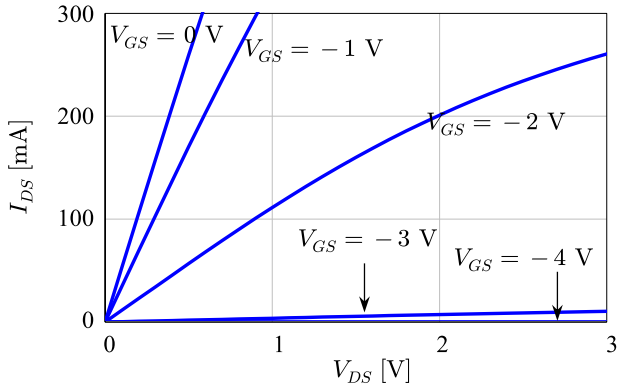


Fig. 2. Simulated I–V curve for a 12×100-μm device.

GaN power stage with the modified active pull-up drivers. Experimental results are provided in Section IV, while Section V concludes this paper.

II. Monolithic GaN Half-Bridge Power Stage With Integrated Gate Drivers

The monolithic half-bridge chip shown in Fig. 1 includes two power switch devices Q_{HS} and Q_{LS} in the half-bridge configuration, and the corresponding high-side and low-side gate drivers, providing required gate-to-source voltages given the two ground-referenced switch control input signals $v_{\mathrm{in,HS}}$, $v_{\mathrm{in,LS}}$, respectively. Since the switch-node voltage v_{sw} is swinging between zero and the input dc voltage V_{in}, the high-side driver must provide effective level shifting between the control input $v_{\mathrm{in,HS}}$ and the gate-to-source voltage $v_{\mathrm{gs,HS}}$ of the high-side switch Q_{HS}. This section describes several approaches to achieving the required integrated gate-drive functions targeting operation at very high switching frequencies. The process available for integration is a 0.15-μm GaN-on-SiC process, with transistor transition frequencies in excess of 80 GHz. The process has been developed for power amplifiers and other RF monolithic microwave integrated circuit applications [20], [21]. The SiC substrate provides high thermal conductivity and high power operation capability. Only n-type depletion mode (D-mode) lateral transistors are available in the process, with a threshold voltage V_{th} of approximately $V_{\mathrm{th}} \approx -3.5$ V. The size of the device with multiple unit cells is usually defined in terms of the gate periphery $W = NW_g$, where N is the number of fingers, and W_g is the cell gate width. As an example, a simulated I–V curve for a $W = 12 \times 100\,\mu\mathrm{m} = 1.2$-mm device is given in Fig. 2. When operated as a switch, the gate-drive voltages are 0 V for the switch ON-state and -5 V for the switch OFF-state. Gate-to-source voltages as low as -10 V are within the capabilities of the process. In general, the process-dependent maximum gate-to-source voltage limitations must be taken into account in the gate-driver circuit designs. While the process breakdown voltage is 50 V, operating voltages up to 20 V are considered in the designs described in this paper. For switch applications, the process parameters of interest include the specific on resistance $R_{\mathrm{on},s}$, specific input and output capacitances $C_{\mathrm{iss},s}$ and $C_{\mathrm{oss},s}$, respectively, and the specific gate charge $Q_{g,s}$. These process parameters are listed in Table I.

TABLE I
Device Specific Parameters

	$R^1_{\mathrm{on},s}$	$C^2_{\mathrm{oss},s}$	$C^3_{\mathrm{iss},s}$	$Q^4_{g,s}$
Simulated	2.1 Ω·mm	0.4 pF/mm	1.5 pF/mm	8.8 pC/mm
Measured	1.6 Ω·mm	–	–	–

[1] $I_{\mathrm{DS}} = 100$ mA
[2] $C_{\mathrm{oss},s} = C_{\mathrm{gd},s} + C_{\mathrm{ds},s}$, at $V_{\mathrm{DS}} = 20$ V
[3] $C_{\mathrm{iss},s} = C_{\mathrm{gd},s} + C_{\mathrm{gs},s}$, at $V_{\mathrm{DS}} = 0$ V
[4] $V_{\mathrm{DS}} = 20$ V

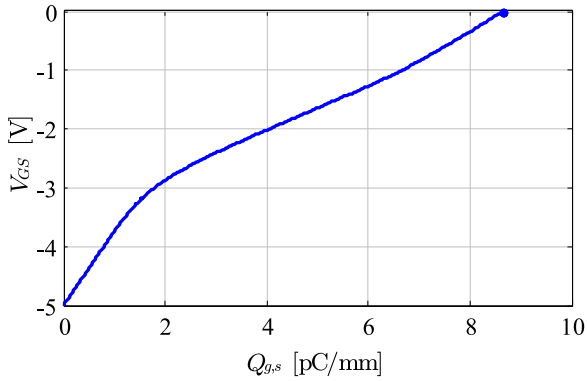


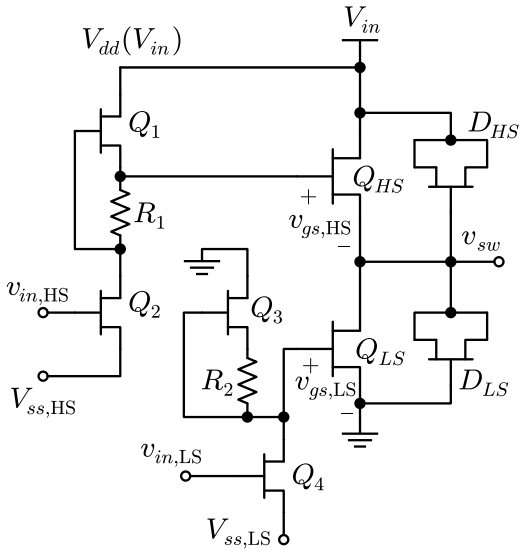
Fig. 3. Simulated gate-to-source voltage V_{GS} as a function of the specific gate charge $Q_{g,s}$ (gate charge in Coulombs per millimeter of gate periphery).

The simulated normalized $Q_{g,s}$ versus V_{GS} curve is given in Fig. 3. Based on the values shown in Table I, the device figure of merit is FOM $= R_{\mathrm{on},s}Q_{g,s} = 18.5$ pVs, which is at least an order of magnitude smaller compared to state-of-the-art silicon MOSFETs with similar voltage rating, and about three times smaller than some of the comparable GaN-on-Si devices, such as EPC8008 (FOM $= 56$ pVs) [22].

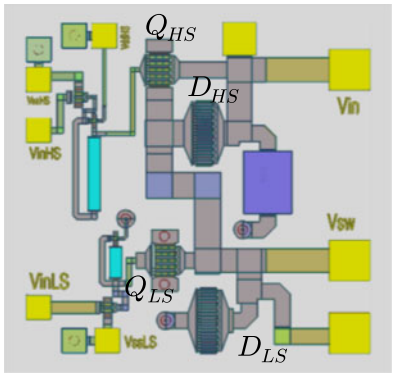
This section presents and compares three gate-drive circuit configurations: the active pull-up driver in Section II-A, the bootstrapped driver in Section II-B, and the modified active pull-up driver in Section II-C. A comparison is given in Section II-D, which shows that the modified active pull-up driver offers several advantages over the other circuits.

A. Active Pull-Up Driver

Fig. 4(a) shows the schematic of the monolithic GaN power stage with the active pull-up drivers. This simplest gate-driver



(a)



(b)

Fig. 4. Active pull-up driver with half-bridge power stage: (a) schematic; and (b) chip layout, 2.4 × 2.3 mm.

configuration considered is used to introduce circuit design techniques common to all GaN chip designs described in this paper. The half-bridge power stage consists of the high-side switch Q_{HS} and the low-side switch Q_{LS}. The chip layout is given in Fig. 4(b). The pull-up voltage V_{dd} for the high-side driver is the same as the converter input voltage, $V_{dd} = V_{\mathrm{in}} = 20$ V. One significant difference between GaN lateral devices and standard vertical silicon MOSFETs is that the lateral GaN device does not include an antiparallel body diode. Consider the synchronous rectifier (device Q_{LS}) in the half-bridge power stage. When the device is OFF, with the gate-to-source voltage at approximately $V_{ss,\mathrm{LS}} = -5$ V, reverse conduction can still occur, but the drain voltage must drop to a relatively large negative value of at least $V_{ss,\mathrm{LS}} - V_{\mathrm{th}} \approx -1.5$ V. With current flowing from source to drain of the synchronous rectifier, the drain voltage is around -2 to -3 V. This reverse conduction may occur during dead times in commutations between Q_{HS} and Q_{LS}. To reduce the corresponding reverse conduction losses, Schottky diodes D_{HS} and D_{LS} are integrated across the half-bridge power switch transistors Q_{HS} and Q_{LS}, respectively, as shown in Fig. 4(a). A Schottky diode can be obtained by shorting drain and source of

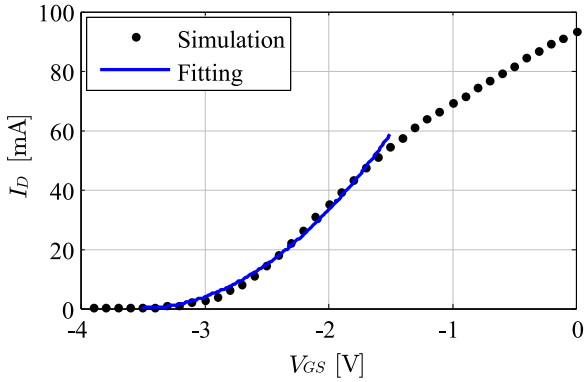


Fig. 5. Simulated I_D–V_{GS} curve for a 4×25-μm device, with quadratic equation curve fitting (-3.5 V$\leq V_{\mathrm{GS}} \leq -1.5$ V) over imposed. $V_{\mathrm{DS}} = 20$ V.

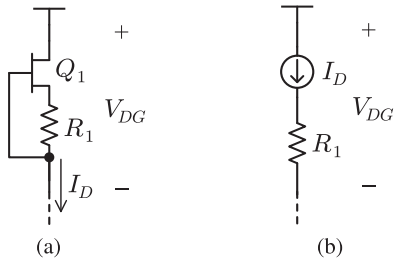


Fig. 6. (a) Transistor with source degeneration resistor; and (b) equivalent circuit.

a transistor, and by using the exponential I–V characteristic of the gate-to-source and the gate-to-drain Schottky junctions, or by other process-specific means.

Given the process characteristics, the device parameters depend on the device size $W = NW_g$, which determines the on resistance $R_{\mathrm{on}} = R_{\mathrm{on},s}/W$, input capacitance $C_i = WC_{\mathrm{iss},s}$, output capacitance $C_o = WC_{\mathrm{oss},s}$, and gate charge $Q_g = WQ_{g,s}$. For a power switch device, the gate periphery W is a parameter that affects the tradeoff between conduction losses and switching losses. The use of this parameter in the design optimization process is described further in Section III.

Consider the high-side driver consisting of the input transistor Q_2 loaded by an active pull-up circuit comprising Q_1 and R_1, as shown in Fig. 4(a). A simplified analysis is presented first for this basic active pull-up structure. The same active pull-up circuit design techniques are used in all integrated drivers reported in this paper. The active pull-up circuit shown in Fig. 6(a), takes advantage of the depletion-mode transistor characteristics. When V_{DG} is large enough so that Q_1 is in saturation region, it behaves as a current source, as shown in Fig. 6(b). For a given value of R_1

$$V_{\mathrm{GS}} = -R_1 \cdot I_D \tag{1}$$

where V_{GS} then determines the drain current based on the device $I_D(V_{\mathrm{GS}})$ characteristic in saturation, which can be found approximately as follows. For a GaN transistor with gate periphery $W = 4 \times 25\ \mu\mathrm{m} = 0.1$ mm, the simulated drain current I_D versus gate-to-source voltage V_{GS} curve is given in Fig. 5. The portion of the curve where -3.5 V $\leq V_{\mathrm{GS}} \leq -1.5$ V is fitted to the quadratic equation similar to the basic characteristic of a

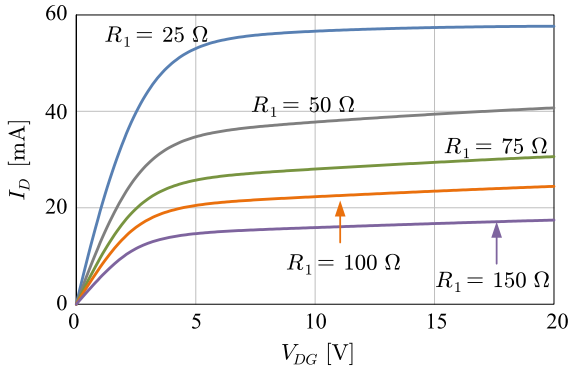


Fig. 7. Simulated I_D–$V_{\rm DG}$ curve for a 4 × 25-μm device, with different values of R_1.

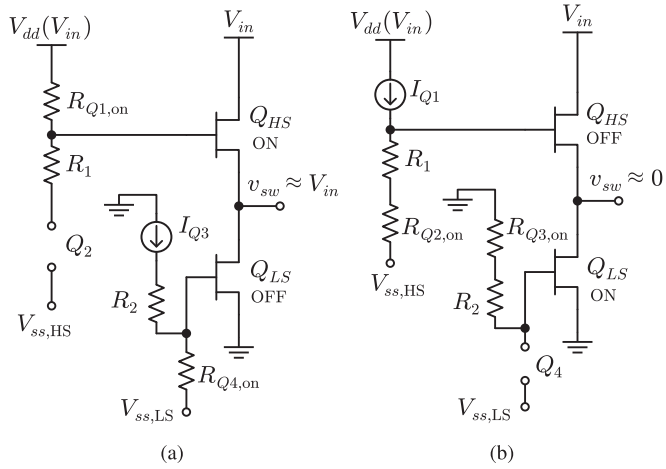


Fig. 8. Simplified diagram for the operation of active pull-up driver: (a) $Q_{\rm HS}$ on, $Q_{\rm LS}$ OFF; and (b) $Q_{\rm HS}$ OFF, $Q_{\rm LS}$ ON. $D_{\rm HS}$ and $D_{\rm LS}$ are removed for simplicity.

silicon MOSFET in saturation

$$I_D \approx K\left(V_{\rm GS} - V_{\rm th}\right)^2 \tag{2}$$

with $K = 14.6$ mA/V^2 and $V_{\rm th} = -3.5$ V. For $V_{\rm GS} > -1.5$ V, the curve does not follow (2) very well, as a result of a self-heating effect, which degrades the electrons saturation velocity, and therefore, reduces the current [23]. Nevertheless, for $-3.5\ {\rm V} \le V_{\rm GS} \le -1.5$ V, which is most relevant for the pull-up circuit design, the approximation (2) is adequate.

Combining (1) and (2) yields

$$I_D \approx K\left(-R_1 I_D - V_{\rm th}\right)^2 \tag{3}$$

which can be solved for I_D

$$I_D = \frac{1 - 2KR_1V_{\rm th} - \sqrt{1 - 4KR_1V_{\rm th}}}{2KR_1^2}. \tag{4}$$

The source degeneration resistance R_1 can be selected to set the current limit for the active pull-up circuit, relatively independently from variations in the device threshold voltage. For instance, when R_1 is 100 Ω, I_D is 22.6 mA; when R_1 is 75 Ω, I_D is 28.1 mA. Using detailed device models, the circuit in Fig. 6(a) is simulated in AWR Microwave Office, for different values of R_1, as shown in Fig. 7. The curves for 75 Ω and 100 Ω in saturation region match the values obtained from (3).

Given the current source equivalent of the active pull-up structure shown in Fig. 6(b), the operation of the active pull-up driver in Fig. 4 can be analyzed in more detail. In order to turn the high-side switch $Q_{\rm HS}$ ON, Q_2 is turned OFF, and Q_1 turns ON, pulling the gate of $Q_{\rm HS}$ up to $V_{dd} = V_{\rm in}$. During $Q_{\rm HS}$ turn-ON transition, $v_{\rm sw}$ ramps up to $V_{\rm in}$. As a result, $v_{\rm gs}$ of $Q_{\rm HS}$ is maintained at approximately 0 V. Recall that all devices are depletion-mode n-type devices with approximately -3.5 V threshold voltage. At $v_{\rm gs,HS} = 0$ V, the high-side power switch $Q_{\rm HS}$ is fully ON. A simplified circuit diagram corresponding to the case when $Q_{\rm HS}$ is in the ON-state is shown in Fig. 8(a), with $R_{Q1,\rm on}$ being the ON-state resistance of Q_1. While the high-side switch is ON, the low-side switch is OFF. This is accomplished by turning the low-side gate-drive transistor Q_4 ON, bringing the gate of $Q_{\rm LS}$ to $V_{ss,\rm LS} + I_{Q3}R_{Q4,\rm on} = -5$ V.

To commutate the half-bridge switches, turning Q_2 on starts a turn-OFF transition of $Q_{\rm HS}$. The gate of $Q_{\rm HS}$ is pulled down to $V_{ss,\rm HS} < 0$, plus a voltage drop across Q_2 ($I_{Q1}R_{Q2,\rm on}$) and $I_{Q1}R_1$

$$v_{g,\rm HS} = V_{ss,\rm HS} + (R_1 + R_{Q2,\rm on}) \cdot I_{Q1} \tag{5}$$

which is set to produce $v_{\rm gs} \approx -5$ V by the choice of component parameters and the bias voltage $V_{ss,\rm HS}$. When Q_2 is ON, the active pull-up transistor Q_1 together with the source-degeneration resistor R_1 act approximately as a constant current source I_{Q1}. As shown in (4), the value of I_{Q1} can be adjusted by changing the size of Q_1 or the value of R_1. A simplified circuit diagram for these states of the switches is shown in Fig. 8(b). Once $Q_{\rm HS}$ is turned OFF, the switch-node voltage $v_{\rm sw}$ is pulled down by the buck filter inductor current (not shown) toward approximately 0 V, allowing zero-voltage switching (ZVS) turn-ON of $Q_{\rm LS}$ [24]. The $Q_{\rm LS}$ turn-ON transition is initiated by turning the low-side gate-drive transistor Q_4 OFF.

Fig. 8 can be used to make an approximate analysis of driver losses. The values of the current sources I_{Q3} and I_{Q1} are determined by the device sizes and R_2 and R_1, respectively. In the optimized design, $I_{Q3} = 13.2$ mA and $I_{Q1} = 8.5$ mA. For a given duty cycle D, the static driver conduction loss is

$$\begin{aligned} P_{d,\rm cond} &= P_{d,\rm cond\_HS} + P_{d,\rm cond\_LS} \\ &= (V_{\rm in} - V_{ss,\rm HS})\, I_{Q1}\,(1 - D) + (-V_{ss,\rm LS})\, I_{Q3} D. \end{aligned} \tag{6}$$

Numerical values for the driver losses based on the simple static model are calculated and given in Table III for three duty cycles: 0.25, 0.5, and 0.75. In practice, there are additional switching losses, dominated by losses due to current spikes during switching transients and by losses due to charging and discharging of gate and other node capacitances, as discussed further in Section III-A.

Dynamic performance of the gate drivers in terms of turn-ON and turn-OFF times is determined by two options available to connect the driver to the gate of the power device: at the top or at the bottom of the source degeneration resistor. The connection for the low-side driver is chosen at the bottom of R_2, to speed up the turn-OFF time of the synchronous rectifier

TABLE II
SUMMARY OF DEVICE SIZES AND COMPONENT VALUES

	$Q_{\rm HS}, Q_{\rm LS}$	$D_{\rm HS}, D_{\rm LS}$	W_{Q1}	W_{Q2}	W_{Q3}	W_{Q4}	R_1	R_2	D_1	C_1
Active	$10 \times 125\ \mu$m	$10 \times 120\ \mu$m	$2 \times 25\ \mu$m	$4 \times 50\ \mu$m	$2 \times 25\ \mu$m	$4 \times 50\ \mu$m	300 Ω	125 Ω	–	–
Bootstrapped	$20 \times 200\ \mu$m	$20 \times 100\ \mu$m	$4 \times 25\ \mu$m	$4 \times 25\ \mu$m	–	–	175 Ω	–	$2 \times 25\ \mu$m	126 pF
Modified	$20 \times 200\ \mu$m	$20 \times 100\ \mu$m	$4 \times 25\ \mu$m	$4 \times 50\ \mu$m	$4 \times 25\ \mu$m	$4 \times 50\ \mu$m	100 Ω	75 Ω	–	–

TABLE III
COMPARISON OF ESTIMATED CONDUCTION LOSSES IN INTEGRATED GATE DRIVERS AND POWER STAGE DEVICE SIZE

	Estimated $P_{d,\rm cond}$ [mW]			
D	0.25	0.5	0.75	W [mm]
Active	195	152	109	1.25
Bootstrapped[1]	123	125	126	4
Modified	171	157	143	4

[1]Assuming the same low-side driver as the modified active pull-up.

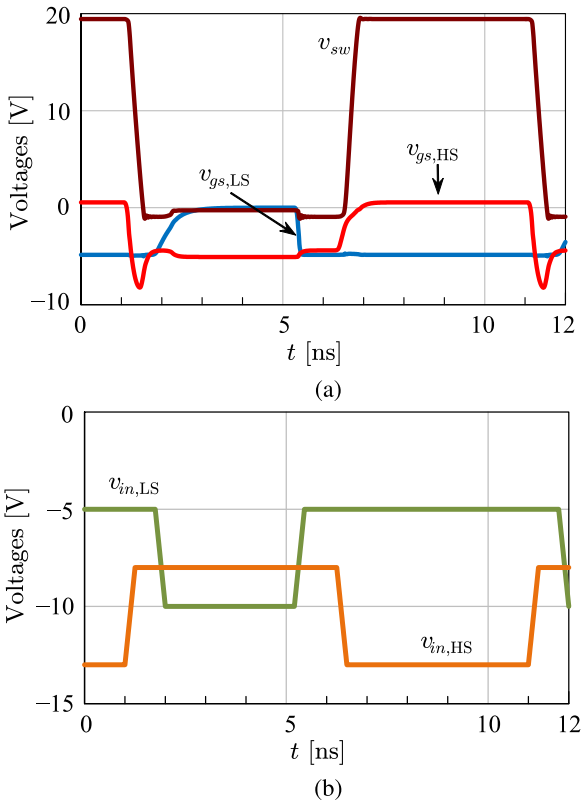


Fig. 9. Simulated waveforms of the active pull-up driver: $D = 0.5$, $I_o = 250$ mA, $f_s = 100$ MHz.

$Q_{\rm LS}$ and improve the ZVS low-to-high transition. In this case, fast turn-OFF of $Q_{\rm LS}$ helps the resonant transition that consists of charging of the switch-node capacitance from 0 V to $V_{\rm in}$. If the gate of $Q_{\rm LS}$ were connected to the top of R_2, the slower turn-OFF of the negative current through $Q_{\rm LS}$ would increase switching losses and reduce the energy available to complete the resonant transition. With the connection shown, the turn-ON transition of $Q_{\rm LS}$ is slower. This is acceptable because $Q_{\rm LS}$ is turned on at zero voltage during the brief time interval when the freewheeling diode $D_{\rm LS}$ is conducting.

The high-side driver connection is to the top of R_1, which in this case ensures both fast turn-ON and fast (but not fastest possible) turn-OFF. During the turn-on transition of $Q_{\rm HS}$, current flows through Q_1 only, instead of Q_1 and R_1, providing the fastest possible turn-ON of $Q_{\rm HS}$. During the turn-OFF transition of $Q_{\rm HS}$, current flows through R_1 and Q_2. Given the external voltage source $V_{ss,\rm HS}$ and the initial voltage of the gate of $Q_{\rm HS}$ ($V_{g,\rm HS} = V_{\rm in}$), the large initial voltage across R_1 provides a large negative gate current and fast turn-OFF even though R_1 is in the current path. If the gate of $Q_{\rm HS}$ were connected to the bottom of R_1, the turn-OFF would be even faster but at the expense of increased gate-drive losses and risks associated with temporarily exposing gate-to-source of $Q_{\rm HS}$ to exceedingly high negative voltage.

Compared to a simple resistive pull-up driver [14], an advantage of the active pull-up driver is that in the OFF-state of the high-side switch $Q_{\rm HS}$, the high-side driver current is limited to the current source value I_{Q1}, while Q_1 still provides a low impedance gate-to-source circuit when the high-side switch is in the ON-state. A disadvantage of the active pull-up driver is that I_{Q1} flows from $V_{dd} = V_{\rm in}$, which increases the conduction losses during the OFF-state of the high-side switch $Q_{\rm HS}$, and the switching losses during transitions.

The gate-drive circuit design amounts to a tradeoff between power consumption and speed. For instance, making R_1 smaller results in a faster falling edge in the driving signal of $Q_{\rm HS}$, at the expense of larger I_{Q1}, and larger power dissipated on Q_1 and R_1. Conversely, a larger R_1 results in reduced power losses in the gate driver, but longer fall and rise times in the gate voltage for the high-side power transistor $Q_{\rm HS}$. Driving signals with longer rise/fall times result in higher switching losses in the power stage. Table II gives the parameters found to minimize the total power loss. With the device sizes and component values shown in Table II, the circuit in Fig. 4(a) is simulated in AWR Microwave Office using detailed device models, with a current sink $I_o = 250$ mA connected to $v_{\rm sw}$, which resembles a synchronous buck converter with a large filter inductor. The gate driver bias voltages $V_{ss,\rm HS}$ and $V_{ss,\rm LS}$ are set to -8 and -5 V, respectively. They are provided by external very low-power voltage sources. The simulated waveforms are shown in Fig. 9, including driver input voltages $v_{\rm in,HS}$ and $v_{\rm in,LS}$, switch node voltage $v_{\rm sw}$ and the gate-to-source voltages of the power stage transistors operating at 100 MHz switching frequency. Note that the rise and fall times of $v_{\rm gs}$ waveforms as well as the switch-node voltage $v_{\rm sw}$ are all within 1 ns.

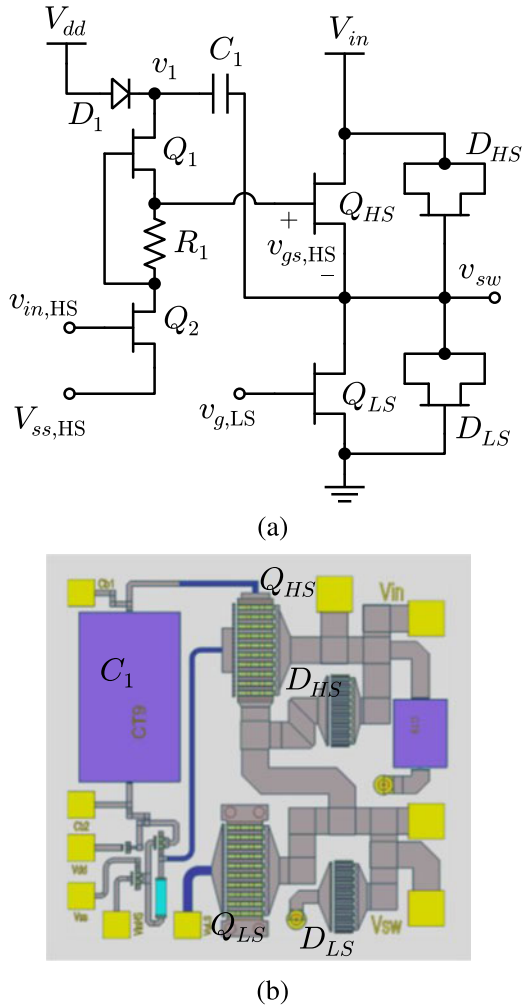


Fig. 10. Bootstrapped driver with half-bridge power stage: (a) schematic; and (b) chip layout, 2.4 × 2.3 mm.

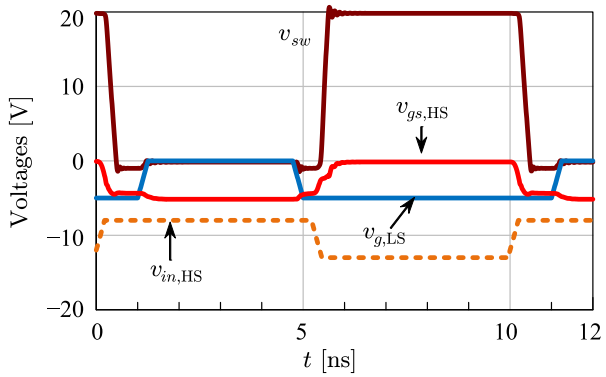


Fig. 11. Simulated waveforms of the bootstrapped driver: $D = 0.5$, $I_o = 500$ mA, $f_s = 100$ MHz.

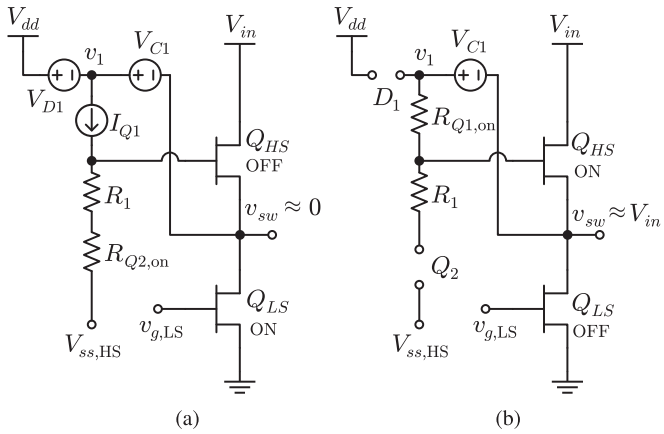


Fig. 12. Simplified circuit diagrams illustrating operation of bootstrapped driver in two states of the switches: (a) Q_{HS} OFF, Q_{LS} ON, and (b) Q_{HS} ON, Q_{LS} OFF. The antiparallel diodes D_{HS} and D_{LS} are not shown, for simplicity.

B. Bootstrapped Driver

As discussed in Section II-A, the active pull-up driver for the high-side switch is supplied from the input voltage, $V_{dd} = V_{\mathrm{in}}$. To avoid the power dissipation associated with the need to supply the driver from the input voltage, a bootstrap scheme is considered in this section. The schematic and the chip layout of the bootstrapped driver integrated along with the half-bridge power stage are shown in Fig. 10. Diode D_1 and bootstrap capacitor C_1, which are integrated on the same chip, allow a significant reduction in the required gate-driver supply voltage V_{dd}.

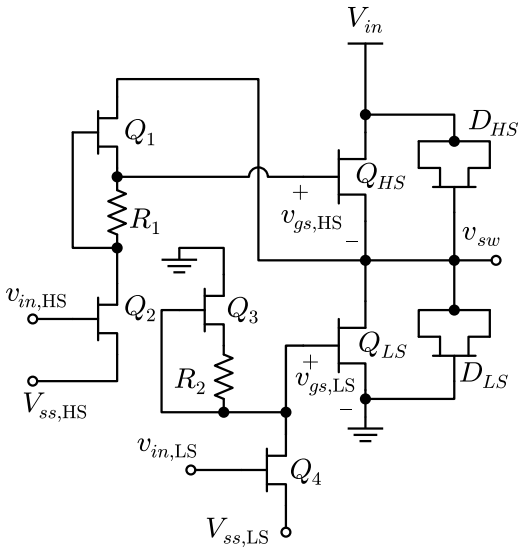
As in the active pull-up driver, the high-side switch Q_{HS} ON/OFF-state is decided by the state of the driver transistor Q_2. When Q_2 is ON, Q_{HS} is OFF and vice versa. Simplified circuit diagrams corresponding to the two states of the switches are shown in Fig. 12. Consider the case when Q_2 is ON, Q_{HS} is OFF, and Q_{LS} is ON so that $v_{\mathrm{sw}} \approx 0$. As described in Section II-A, Q_1, together with the source degeneration resistor R_1, behaves as a current source I_{Q1}, and $V_{dd} \approx 1$ V is selected such that the bootstrap capacitor voltage $V_{C1} \approx 0$ V, as shown in Fig. 12(a).

Consider next a transition to the state when Q_{LS} is OFF and Q_{HS} is ON. After the low-side switch Q_{LS} is turned OFF, Q_2 can be turned OFF to initiate turn-ON of the high-side switch Q_{HS}. Assuming hard switching operation, with Q_2 OFF, I_{Q1} charges the gate capacitance of Q_{HS}, which turns ON and, as a result, the switch node voltage v_{sw} increases. As the voltage across Q_1 drops, and current through Q_1 drops, Q_1 becomes fully ON, with small on-resistance $R_{Q1,\mathrm{on}}$ connecting $V_{C1} \approx 0$ across the gate-to-source terminals of Q_{HS}, thus completing the turn-ON transition of the high-side switch. In ZVS operation, the timing of the events is different, as v_{sw} increases to V_{in} before Q_2 is turned OFF, but the gate driver operation is otherwise very similar. With $v_{\mathrm{sw}} \approx V_{\mathrm{in}}$, diode D_1 is reverse biased, preventing discharge of C_1.

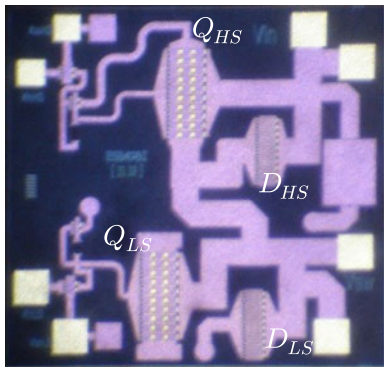
The static conduction power loss for the bootstrapped driver can be found as

$$\begin{aligned} P_{d,\mathrm{cond}} &= P_{d,\mathrm{cond\_HS}} + P_{d,\mathrm{cond\_LS}} \\ &= (V_{dd} - V_{ss,\mathrm{HS}})\, I_{Q1}\,(1-D) + (-V_{ss,\mathrm{LS}})\, I_{Q3} D \end{aligned} \quad (7)$$

assuming the same low-side driver as in Fig. 13(a) is also implemented, for a fair comparison. Since V_{dd} is much lower, the best design utilizes a larger I_{Q1} current to produce faster transitions and to reduce switching losses in the power stage. In this case,



(a)



(b)

Fig. 13. Modified active pull-up driver with half-bridge power stage: (a) schematic; and (b) chip microphotograph, 2.4 × 2.3 mm.

I_{Q1} is 13.5 mA, compared to 8.5 mA in the active pull-up driver. Device sizes and component values for the bootstrapped driver are given in Table II. Numerical values for the static losses, for different duty cycles, are given in Table III. The increased driving speed enables the use of larger power stage devices (Q_{HS} and Q_{LS}) and allows higher output power, compared to the case with the active pull-up driver. This circuit is simulated using the same configuration described before for $I_o = 500$ mA, with waveforms presented in Fig. 11. The gate driver bias voltages $V_{ss,\mathrm{HS}}$ of -8 V is provided by an external voltage source.

A clear advantage of the bootstrapped driver is that it operates from reduced V_{dd}, which implies reduced static power losses compared to the active pull-up driver. This, in turn, allows a design with a larger bias current targeting faster transitions, and allowing use of larger power-stage devices. As a result, the overall efficiency and output power capability can be improved. Another advantage of the bootstrapped driver is that it allows positive gate-to-source voltages for the high-side switch. This provides additional design flexibility, and the ability to use the driver with enhancement-mode devices. A disadvantage of the bootstrapped driver is the need for a relatively large capacitor

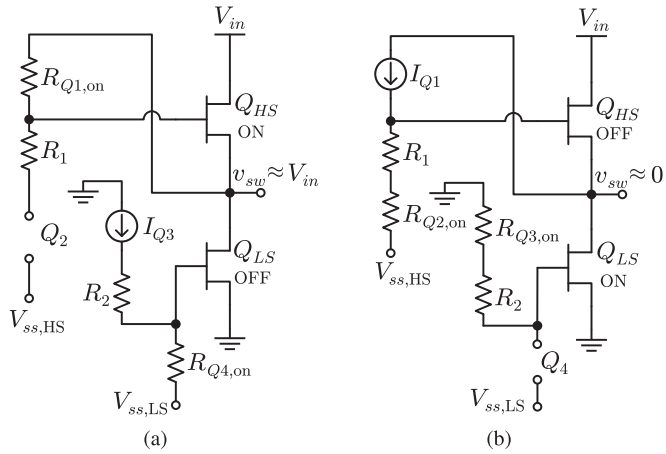


Fig. 14. Simplified diagram for the operation of modified active pull-up driver: (a) Q_{HS} ON, Q_{LS} OFF; and (b) Q_{HS} OFF, Q_{LS} ON. D_{HS} and D_{LS} are removed for simplicity.

C_1, which must hold the required voltage during the time when Q_{HS} is ON. An on-chip capacitor is implemented for minimal parasitic inductance. However, an external bootstrap capacitor may still be required, especially when switching at lower frequencies. Because of the area taken by C_1, and because of a chip-size limitation, the circuit design in Fig. 10 does not include a low-side driver.

C. Modified Active Pull-Up Driver

To address disadvantages of the active pull-up and the bootstrapped drivers, a novel modified active pull-up driver circuit has been constructed, as shown in Fig. 13. Instead of using an external voltage source V_{dd}, the high-side driver (drain of Q_1) is simply connected to the switching node v_{sw}. This configuration significantly reduces the driver power consumption by taking advantage of the fact that the switching node voltage v_{sw} becomes approximately zero when Q_{HS} is OFF and Q_{LS} is ON.

Fig. 14 shows simplified circuit diagrams illustrating operation of the modified active pull-up driver in the two switch states. The operating principle for the high-side driver is as follows: the gate-to-source voltage $v_{\mathrm{gs,HS}}$ of Q_{HS} is equal to the source-to-drain voltage of Q_1. In order to turn the high-side switch Q_{HS} on, Q_2 is OFF, and Q_1 is ON, which is represented by small on-resistance $R_{Q1,\mathrm{on}}$ in Fig. 14(a), and $v_{\mathrm{gs,HS}}$ is approximately 0 V. As a result, the depletion-mode high-side switch Q_{HS} is fully ON. When Q_2 is turned ON, the gate of Q_{HS} is pulled down to $V_{ss,\mathrm{HS}} < 0$ V, plus voltage drops across Q_2 ($I_{Q1}R_{Q2,\mathrm{on}}$) and $I_{Q1}R_1$

$$v_{g,\mathrm{HS}} = V_{ss,\mathrm{HS}} + (R_1 + R_{Q2,\mathrm{on}}) \cdot I_{Q1} \tag{8}$$

which is designed to be -5 V by the choice of I_{Q1}, R_1, and $R_{Q2,\mathrm{on}}$, as shown in Fig. 14(b). Once Q_{HS} is turned OFF, the switch-node voltage v_{sw} is pulled down by the buck filter inductor current (not shown) toward approximately 0 V, allowing zero-voltage switching (ZVS) turn-ON of Q_{LS} after a brief dead time. The Q_{LS} turn-ON transition is initiated by turning the low-side gate-drive transistor Q_4 OFF. The dead time is selected to minimize the time diode D_{LS} is conducting.

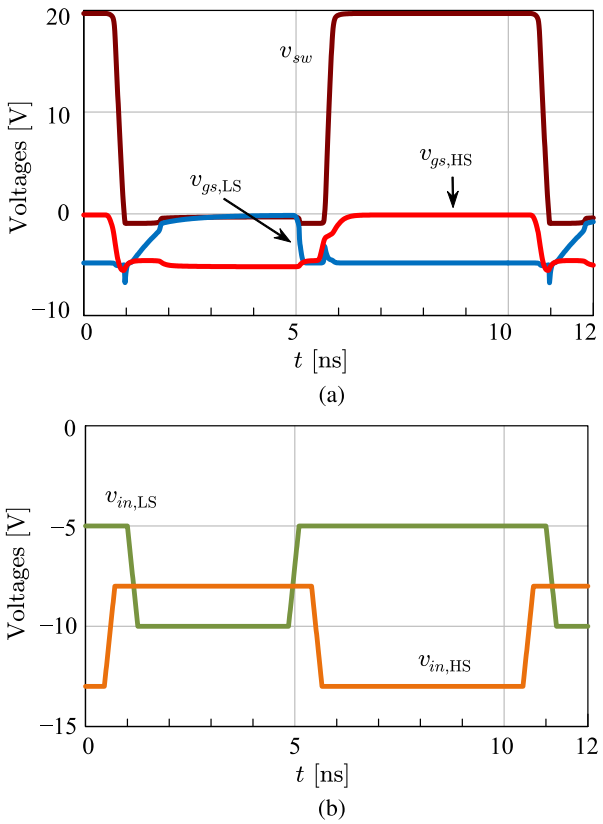


Fig. 15. Simulation of the modified active pull-up driver: $D = 0.5$, $I_o = 500$ mA, $f_s = 100$ MHz.

In this case, current I_{Q1} is supplied from the switching node, which is around 0 V, much lower compared to $V_{dd} = V_{\mathrm{in}}$ in the active pull-up driver. As in the case of the bootstrapped circuit, reduced driver losses allow overall improved efficiency and higher output power capabilities. Table II gives the sizes of transistors used in this circuit. The static conduction power loss in the modified active pull-up driver is

$$\begin{aligned} P_{d,\mathrm{cond}} &= P_{d,\mathrm{cond\_HS}} + P_{d,\mathrm{cond\_LS}} \\ &= \left(-V_{ss,\mathrm{HS}}\right) I_{Q1} \left(1 - D\right) + \left(-V_{ss,\mathrm{LS}}\right) I_{Q3} D. \end{aligned} \quad (9)$$

For this driver, I_{Q1} is 23.3 mA and I_{Q3} is 25.6 mA. The estimated static driver conduction losses, for different duty cycles are included in Table III. Simulated waveforms illustrating operation of the modified active pull-up driver are shown in Fig. 15. Similar to the active pull-up driver, external voltage sources provide the gate driver bias voltages $V_{ss,\mathrm{HS}}$ and $V_{ss,\mathrm{LS}}$ of -8 V and -5 V, respectively.

D. Comparison of Integrated Gate Drivers

Table II summarizes the device sizes and component values used in the three presented designs of monolithic GaN power stages chips with integrated gate drivers. All chip sizes are constrained to be the same (2.4 mm × 2.3 mm). Based on the design optimization approach described in detail in the next section, the device sizes and the parameter values are selected to minimize the total power loss, including gate-driver losses, for a given set of operating conditions: $V_{\mathrm{in}} = 20$ V, $f_s = 100$ MHz, $D = 0.5$, output power $P_{\mathrm{out}} = 5$ W for the chip with bootstrapped driver and modified active pull-up driver, and $P_{\mathrm{out}} = 2.5$ W for the chip with active pull-up driver. Because of the increased gate-driver power consumption, the active pull-up driver uses the smallest bias currents, i.e., the largest R_1 and R_2. As a result, the active pull-up driver sourcing capabilities and the resulting switching speeds are the lowest. To achieve the best compromise between switching and conduction losses, the power devices in the chip with the active pull-up drivers are the smallest in size, i.e., have the smallest gate periphery W. The bootstrapped driver employs a relatively large bootstrap capacitor, which is why no space was available on the chip to include the low-side driver.

Based on (6), (7), and (9), Table III compares the estimated conduction losses in the three integrated gate drivers. Note that the power-stage device size W is the smallest on the chip with the active pull-up drivers. Although the active pull-up driver is designed to have the lowest bias current, it still has the largest driver loss at $D = 0.25$. The modified active pull-up driver estimated conduction losses are slightly higher than in the bootstrapped driver because the modified active pull-up drivers allow the largest bias currents, and therefore, the fastest switching speeds. Compared to the bootstrapped driver, additional advantages of the modified active pull-up driver are that there are no needs for the additional auxiliary supply voltage V_{dd} and a large bootstrap capacitor. As a result, the chip area for the high-side driver is reduced by 80%. Therefore, the modified active pull-up driver design is simpler, requires a smaller footprint, and allows operation over wide range of frequencies without the need for an external bootstrap capacitor.

III. Loss Modeling and Design Optimization

As noted in Section II, the device sizes and the parameters in monolithic GaN power stages with integrated gate drivers can be selected to minimize total losses for given operating conditions. This section presents details of the loss modeling and optimization process, which extends the approach presented in [12] by inclusion of gate-driver losses, and more detailed power-stage loss models. The optimum design makes the best trade-off between switching and conduction losses, which depends on the selected gate-driver configuration. Details are presented for the monolithic GaN chip design using the modified active pull-up driver. Similar loss models and the design optimization approach apply to the chips with the other integrated gate-driver configurations presented in Section II.

A. Loss Model

The loss mechanisms taken into account in the loss model are as follows:

1) power stage conduction loss P_c:
   a) conduction loss due to ON-resistance: $P_{c,\mathrm{Ron}}$;
   b) reverse conduction loss $P_{c,\mathrm{rev}}$.
2) power stage switching loss P_s:
   a) turn-ON loss $P_{s,\mathrm{on}}$, in cases of hard switching or partial ZVS;

b) turn-OFF loss $P_{s,\text{off}}$, taking into account non-zero current at turn-OFF;

total power stage devices loss $P_{\text{pwr}} = P_c + P_s$.

3) inductor loss P_L, including dc and ac loss, $P_{L,\text{dc}}$ and $P_{L,\text{ac}}$, respectively.

4) integrated gate driver loss P_d:

a) static conduction loss $P_{d,\text{cond}}$;

b) switching loss $P_{d,\text{sw}}$.

The total loss is then given by

$$P_t = P_c + P_s + P_L + P_d. \tag{10}$$

The loss model details are presented next.

1) Power Stage Conduction Losses: Conduction loss due to ON-resistance can be found as

$$P_{c,\text{Ron}} = \left(I_o^2 + \frac{1}{3}\Delta i_L^2\right) R_{\text{on,d}} \tag{11}$$

where $R_{\text{on,d}}$ is the effective dynamic ON-resistance [25], I_o is the average output current, and Δi_L is the inductor current ripple.

The reverse conduction loss can be expressed as

$$P_{c,\text{rev}} = \frac{1}{2} V_F I_p \Delta t_d f_s + \frac{1}{2} V_F |I_v| \Delta t_d f_s + V_F I_p t_{\text{on,ls}} f_s \tag{12}$$

where V_F is the reverse voltage drop (Schottky diode forward voltage drop); I_p and I_v are the inductor peak and valley current, respectively, f_s is the switching frequency, and $t_{\text{on,ls}}$ is the rise time of the v_{gs} waveform produced by the low-side driver. The first two terms are related to the limited dead-time resolution Δt_d, which necessitates a minimum reverse conduction time. On average, the dead-time quantization error is $1/2 \cdot \Delta t_d$. The last term is associated with the turn-ON speed of the low-side power device Q_{LS}, assuming the rise time of the low side driver is $t_{\text{on,ls}}$.

2) Power Stage Switching Losses: The turn-ON switching loss is considered to be determined solely by charging or discharging of the equivalent switching node capacitance C_{sw}, which is the sum of the two output capacitances C_{ds} of the transistors, the diode capacitances and the additional capacitance introduced by the chip package and the printed circuit board (PCB) traces [12]. Since the switch-node voltage high-to-low transition is always a ZVS transition, only the low-to-high transition is considered, including three cases.

1) Complete ZVS transition

$$P_{s,\text{on}} = 0 \tag{13}$$

which is subject to the following three ZVS conditions:

$$J_v \leq 0 \tag{14}$$

$$\sqrt{J_v^2 + D^2} > 1 - D \tag{15}$$

$$t_{LH} = \frac{\alpha_{LH}}{\omega_0} \leq t_{d,\max} \tag{16}$$

with $t_{d,\max}$ being the maximum allowed dead time, set to 10% of the switching period, and where J_v is the normalized inductor valley current at the start of the resonant transition, $J_v = I_v \sqrt{L/C_{\text{sw}}}/V_{\text{in}}$. $\omega_0 = 1/\sqrt{LC_{\text{sw}}}$ is the resonant frequency in radians.

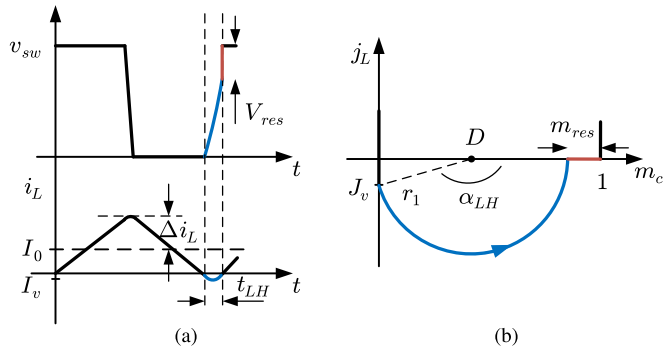


Fig. 16. (a) Example waveform for partial ZVS; and (b) its state plane representation.

2) Hard switching

$$P_{s,\text{on}} = \frac{1}{2} C_{\text{sw}} V_{\text{in}}^2 f_s \tag{17}$$

where C_{sw} is the total equivalent switching node capacitance.

3) Partial ZVS

$$P_{s,\text{on}} = \frac{1}{2} C_{\text{sw}} (V_{\text{in}} m_{\text{res}})^2 f_s \tag{18}$$

m_{res} being the fraction of voltage remaining in C_{sw} when the resonant transition ends.

An example waveform and the state-plane diagram corresponding to a partial ZVS transition are shown in Fig. 16. In this case, the ZVS condition (15) is not satisfied, and m_{res} can be written as

$$m_{\text{res}} = 1 - D - \sqrt{J_v^2 + D^2} \tag{19}$$

for $D < 0.5$. When the ZVS condition (16) is not satisfied, m_{res} becomes

$$m_{\text{res}} = 1 - D - \sqrt{J_v^2 + D^2} \cdot \cos\left[\pi - \cos^{-1}\left(\frac{D}{\sqrt{J_v^2 + D^2}}\right) - \frac{t_{d,\max}}{\sqrt{LC_{\text{sw}}}}\right]. \tag{20}$$

The turn-OFF loss, due to finite switching speed and nonzero power switch current at turn-OFF can be estimated as

$$P_{s,\text{off}} = \frac{I_{p,\text{HS}}^2 t_{0H}^2 f_s}{24 C_{\text{sw}}} + \frac{I_v^2 t_{0L}^2 f_s}{24 C_{\text{sw}}} + \frac{1}{2} L_p I_p^2 f_s \tag{21}$$

where t_{0H} and t_{0L} are the current turn-OFF times for the high-side Q_{HS} and the low-side Q_{LS} switches, respectively, and L_p is the total parasitic inductance in series with the half-bridge switches due to chip package and PCB traces. Compared to [26], where more accurate and more complex models are presented to address parasitic inductances, a relatively simple model that accounts for energy stored in the parasitic inductances is employed here. As gate-driver integration greatly mitigates the effects of parasitic inductances, the simple model is found to be sufficiently accurate and suitable for design optimization. Expression (21) assumes that the device channel current transitions to zero as a linear function of time during t_{0H} (or t_{0L}), while the total device current remains constant and equal to $I_{p,\text{HS}}$ (or I_v).

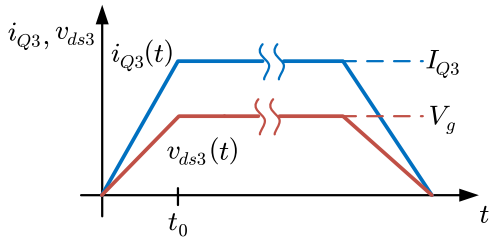


Fig. 17. Assumed voltage and current waveforms of Q_3 for low-side driver switching loss estimation.

In particular, in the modified active pull-up driver, during turn-OFF transition, the peak driver current $I_{d,\mathrm{pk}}$ also flows through the power stage high-side device. As a result, the peak current in the power stage high-side device is given by

$$I_{p,\mathrm{HS}} = I_p + I_{d,\mathrm{pk}}. \tag{22}$$

3) Inductor Losses: The average power loss in the inductor is found using Fourier series expansion:

$$P_L = I_o^2 R_{L,\mathrm{dc}} + \sum_{n=1}^{\infty} \frac{1}{2}\left(\frac{V_{\mathrm{in}}}{f_s L}\frac{\sin(n\pi D)}{n^2\pi^2}\right)^2 R_n \tag{23}$$

where R_n is the effective resistance at frequency f_n, calculated based on the inductor Q-factor versus frequency plot provided by the inductor manufacturer, and D is the duty cycle. Considering the Q-factor versus frequency curves of high-Q air-core inductors [27], [28], it is sufficient to include the first five harmonics in (23). Given the empirical nature of the equivalent resistance R_n, (23) accounts for all ac losses, including skin and proximity effects.

4) Driver Losses: The static conduction loss for the modified active pull-up driver is given by (9) in Section II-C. Consider first switching losses $P_{d,\mathrm{sw\_LS}}$ in the low side driver. The power loss for charging and discharging the gate of the power stage device Q_{LS} can be expressed as

$$P_{d,\mathrm{QLS}} = C_{\mathrm{gs,LS}} V_g^2 f_s \tag{24}$$

where $C_{\mathrm{gs,LS}}$ is the charge-equivalent gate-to-source capacitance of Q_{LS}, and V_g is the gate-drive voltage swing (5 V). It can be seen from Fig. 13(a) that the driver transistor Q_4 is hard switching, and the loss associated with its equivalent output capacitor is

$$P_{d,\mathrm{Q4}} = C_{\mathrm{ds},4}(-V_{ss,\mathrm{LS}})^2 f_s. \tag{25}$$

Referring to Fig. 13(a), the low-side driver transistor Q_3 is operating in either saturation or linear region, and the switching loss associated with Q_3 switching is given by

$$P_{d,\mathrm{Q3}} = \underbrace{C_{\mathrm{gs},3}(I_{Q3}R_2)^2 f_s}_{C\,\mathrm{gs\ loss}} + \underbrace{C_{\mathrm{ds},3} V_g^2 f_s}_{C\,\mathrm{ds\ loss}} + \underbrace{2\cdot\frac{1}{3} I_{Q3} V_g t_0 f_s}_{\mathrm{transition\ loss}} \tag{26}$$

where the last portion of the loss is calculated based on the waveforms shown in Fig. 17.

Finally, the total low-side driver loss is

$$P_{d,\mathrm{LS}} = P_{d,\mathrm{cond\_LS}} + P_{d,\mathrm{QLS}} + P_{d,\mathrm{Q4}} + P_{d,\mathrm{Q3}}. \tag{27}$$

The high-side driver loss can be found following similar reasoning. The loss due to the high-side power device Q_{HS} gate charge is

$$P_{d,\mathrm{QHS}} = C_{\mathrm{gs,HS}} V_g^2 f_s. \tag{28}$$

where $C_{\mathrm{gs,HS}}$ is the charge equivalent gate-to-source capacitance of Q_{HS}. The switching losses of Q_2 and Q_1 can be written as

$$P_{d,\mathrm{Q2}} = C_{\mathrm{ds},2}(V_{dd} - V_{ss,\mathrm{HS}})^2 f_s \tag{29}$$

$$P_{d,\mathrm{Q1}} = \underbrace{C_{\mathrm{gs},1}(I_{Q1}R_1)^2 f_s}_{C\,\mathrm{gs\ loss}} + \underbrace{C_{\mathrm{ds},1} V_g^2 f_s}_{C\,\mathrm{ds\ loss}} + \underbrace{\frac{1}{3} I_{Q1} V_g t_0 f_s}_{\mathrm{transition\ loss}}. \tag{30}$$

Referring to Fig. 13(a), note that Q_1 goes into complete OFF-state when Q_2 is turned ON, due to the current spike of discharging the gate of Q_{HS}. Therefore, the transition loss in (30) is one half of the corresponding loss component in (26).

The total loss for the high-side driver is

$$P_{d,\mathrm{HS}} = P_{d,\mathrm{cond\_HS}} + P_{d,\mathrm{QHS}} + P_{d,\mathrm{Q2}} + P_{d,\mathrm{Q1}}. \tag{31}$$

B. Efficiency Optimization

The design optimization problem is to find the design parameters expressed in vector form as

$$\mathbf{X} = [W_{Q1} \quad W_{Q2} \quad W_{Q3} \quad W_{Q4} \quad R_1 \quad R_2 W] \tag{32}$$

so that the total loss P_t is minimized for a given set of operating conditions. W_{Q1} through W_{Q4} are gate peripheries for transistors Q_1 through Q_4, respectively, and W is the gate periphery for both the high-side and the low-side power stage devices.

The driver loss is directly a function of $\mathbf{X}$

$$P_d = P_d(\mathbf{X}). \tag{33}$$

However, the power stage loss P_{pwr} is a function of timing parameters and $I_{d,\mathrm{pk}}$, lumped together into vector $\mathbf{Y}$

$$\mathbf{Y} = [t_{\mathrm{on,LS}} \quad t_{0L} \quad t_{0H} \quad I_{d,\mathrm{pk}}]. \tag{34}$$

In order to setup the optimization problem, a relation between $\mathbf{X}$ and $\mathbf{Y}$ needs to be established, i.e., it is necessary to find $\mathbf{Y} = f(\mathbf{X})$ so that the total loss can be found in terms of the design parameters

$$P_t = P_d(\mathbf{X}) + P_{\mathrm{pwr}}(f(\mathbf{X})) = P_t(\mathbf{X}). \tag{35}$$

The function $f(\mathbf{X})$ is approximated using RC time constants

$$t_{\mathrm{on,LS}} = 2(R_2 + R_{Q3,\mathrm{on}})(C_{\mathrm{gs,LS}} + C_{\mathrm{ds},Q4}) \tag{36}$$

$$t_{0L} = 2R_{Q4,\mathrm{on}}(C_{\mathrm{gs,LS}} + C_{\mathrm{ds},Q4}) \tag{37}$$

$$t_{0H} = (R_1 + R_{Q2,\mathrm{on}})(C_{\mathrm{gs,HS}} + C_{\mathrm{ds},Q1}) \tag{38}$$

$$I_{d,\mathrm{pk}} = \frac{2Q_{\mathrm{off,HS}}}{t_{0H}} = \frac{2(C_{\mathrm{gs,HS}} + C_{\mathrm{ds},Q1})V_g}{t_{0H}} = \frac{2V_g}{R_1}. \tag{39}$$

The factor of 2 approximates the rise time (10–90%) in an RC circuit as $t_r \approx 2.2\tau$ for the low-side driver timing $t_{\mathrm{on,LS}}$ and t_{0L}. For the high-side driver t_{0H}, however, $1\cdot\tau$ is used because the initial voltage across the high-side driver before Q_{HS} turns OFF is much higher $(V_{\mathrm{in}} - V_{ss,\mathrm{HS}})$, as shown in Fig. 13(a).

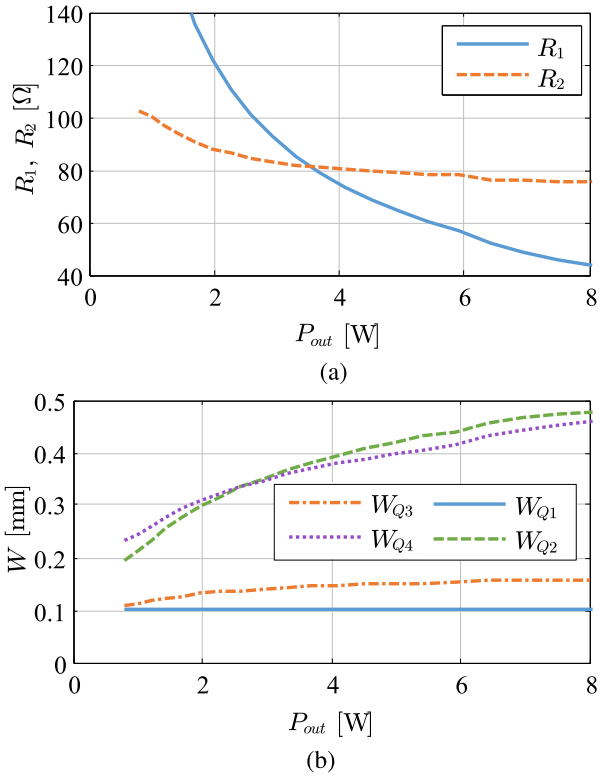


Fig. 18. Optimum driver parameters for maximum total efficiency with $V_{\text{in}} = 20$ V, $R = 20\ \Omega$, and $L = 47$ nH: (a) R_1 and R_2; and (b) W_{Q1}, W_{Q2}, W_{Q3}, and W_{Q4}.

As one of the main benefits of on-chip integration, the parasitic inductances between the gate drivers and the power devices are negligibly small. The lengths of on-chip interconnects, which can be viewed as microstrip transmission lines, are very small, between 0.1 and 1 mm. The resulting parasitic inductances are in the order of 0.1–0.3 nH from 100 MHz to 1 GHz. Simulations of circuit performance with parasitic inductances included in the gate drive path verify that the effects can be safely neglected even in the VHF range of operation.

The design optimization problem can now be solved numerically using a nonlinear constrained optimization method. A constraint for the minimum transistor gate periphery is $W_{\min} = 0.1$ mm. The operating points considered assume input voltage $V_{\text{in}} = 20$ V, switching frequency $f_s = 100$ MHz, and a fixed load resistance $R = 20\ \Omega$ in Fig. 1. A 47-nH inductor is selected such that the low-to-high ZVS transition takes 7.5% of the switching period when $D = 0.5$ and $P_{\text{out}} = 2.5$ W. The nonlinear constrained optimization problem is solved over a range of duty cycles D resulting in a range of P_{out}.

Fig. 18 shows how the optimum driver parameters vary over the considered range of output power. The optimum driver parameter values for three duty cycles 0.25, 0.5, and 0.75 (corresponding to P_{out} of approximately 1.2, 5, and 11 W, respectively) are given in Table IV.

In order to gain more insight into the significance of each design parameter, another set of plots are obtained by varying only one parameter at a time, while keeping the other parameters at the optimum values obtained for $D = 0.5$. The resulting driver

TABLE IV
OPTIMUM AND ACTUAL USED DEVICE SIZES AND COMPONENT VALUES

	R_1 [Ω]	R_2 [Ω]	W_{Q1} [mm]	W_{Q2} [mm]	W_{Q3} [mm]	W_{Q4} [mm]	W [mm]
$D = 0.25$	174	98	0.10	0.23	0.11	0.25	2.0
$D = 0.5$	65	80	0.10	0.42	0.14	0.39	3.6
$D = 0.75$	32	75	0.10	0.49	0.15	0.52	5.3
Actual	100	75	0.1	0.2	0.1	0.2	4

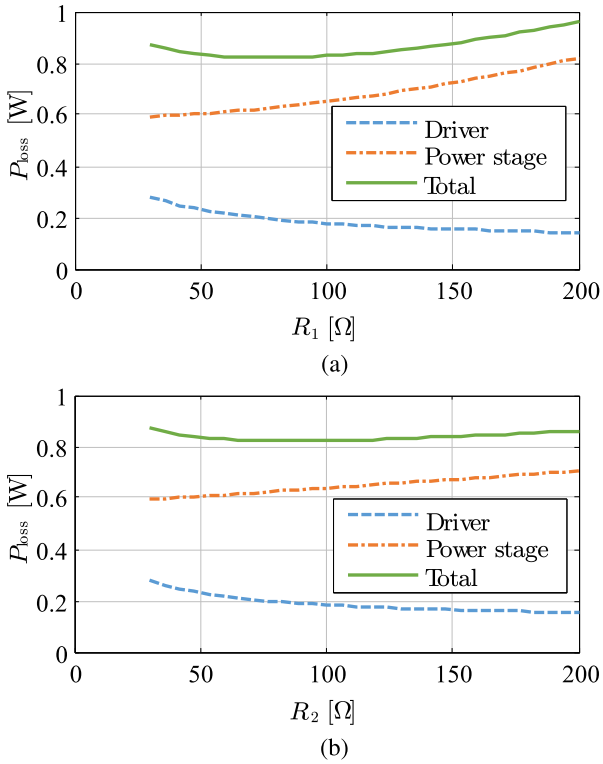


Fig. 19. Driver loss, power stage loss, and total loss when varying one parameter at a time and keeping other parameters the same as the optimum values at $D = 0.5$: (a) R_1 and (b) R_2.

loss, power stage loss, and total loss are given in Figs. 19 and 20. The fact that the loss curves are relatively flat implies that the optimum design is not very sensitive with respect to individual parameter values or, equivalently, uncertainties in loss models. For example, from Fig. 19, it can be seen that the total loss does not change much for any R_1 and R_2 in the range of 50–100 Ω. From Fig. 20(a), it follows that the minimum size for Q_1 is preferred to minimize the total loss. In addition, the acceptable sizes for Q_2 and Q_4 are any values greater than approximately 0.2 mm. The optimum power stage device size W is in the range of 2.5–4 mm, as shown in Fig. 20(e). These conclusions are consistent with understanding of how various parameters affect operation of the driver. Fig. 19 shows that larger R_1 and R_2 result in lower driver static current, and therefore, lower driver power consumption; however, the power stage loss increases due to increased switching losses associated with longer rise/fall times. From the driver schematic in Fig. 13(a), it is clear that larger W_{Q1}, W_{Q2}, W_{Q3}, and W_{Q4} provide lower ON-resistances

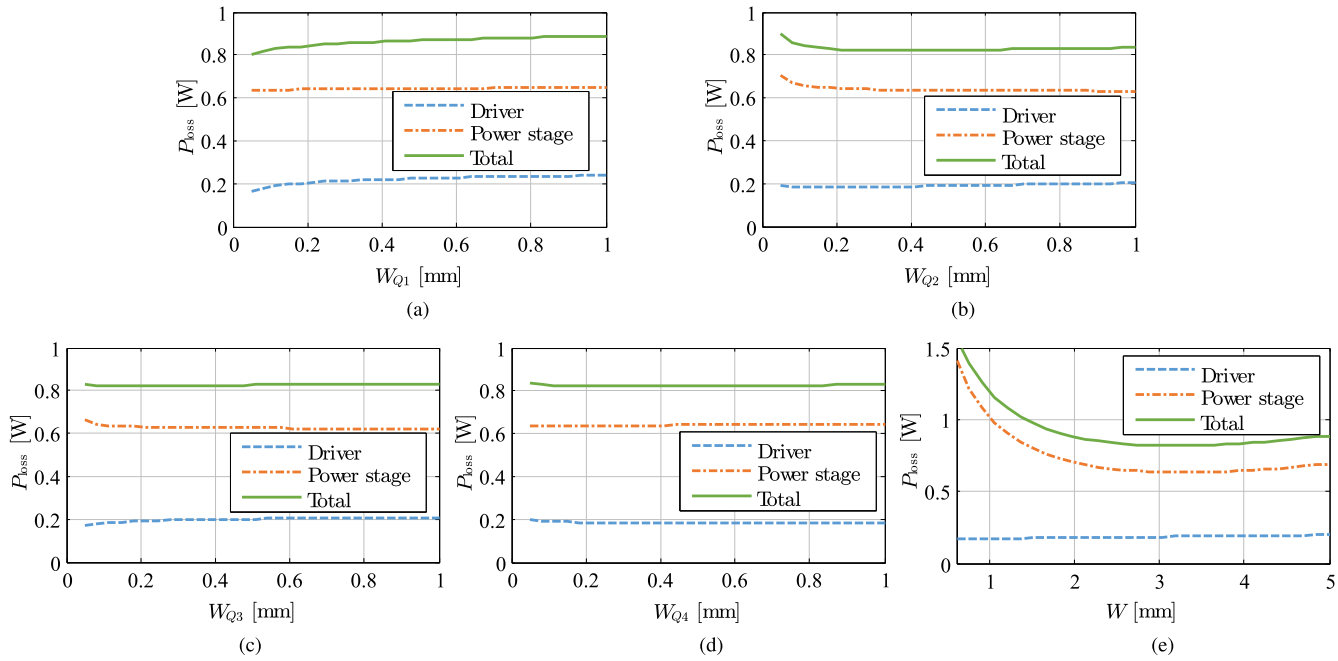


Fig. 20. Driver loss, power stage loss, and total loss when varying one parameter at a time and keeping other parameters the same as the optimum values at $D = 0.5$: (a) W_{Q1}; (b) W_{Q2}; (c) W_{Q3}; (d) W_{Q4}; and (e) W.

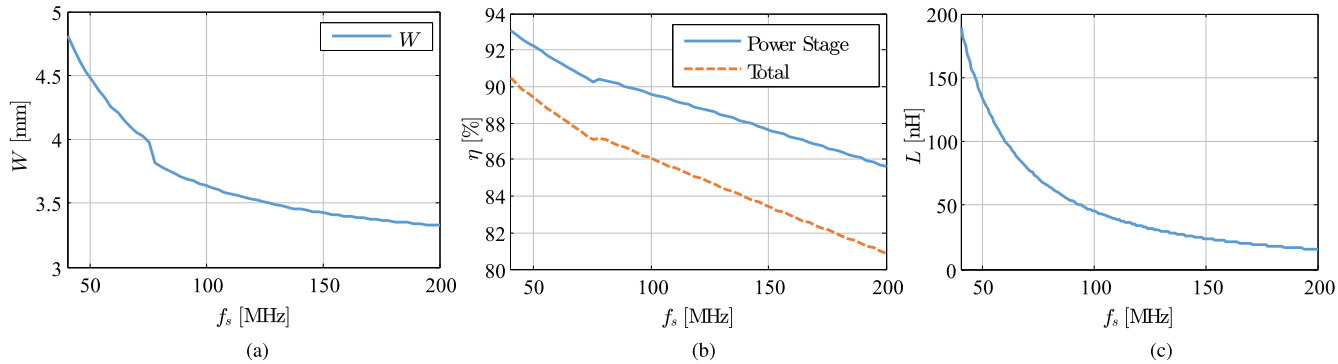


Fig. 21. (a) Optimum power stage device size; (b) maximum power stage, and total efficiency including integrated driver loss; and (c) selected inductor value for each switching frequency.

TABLE V
LOSS MODEL PARAMETERS

$R_{on,d}$	V_F	C_{sw}	$t_{on,LS}$	t_{0L}	t_{0H}	t_0
0.8 Ω	0.9 V	11.6 pF	1 ns	300 ps	500 ps	200 ps

and faster transitions, but result in larger device capacitance and higher driver switching losses.

The actual values used in the final chip design using the modified active pull-up driver are given in Table IV based on the optimum parameter values found for $D = 0.5$, with further adjustments made based on the aforementioned considerations to simplify layout and to fit the layout into the available chip area. The corresponding loss model parameters are summarized in Table V.

C. Efficiency Performance as a Function of Switching Frequency

The design optimization approach has further been applied to examine the achievable efficiency as a function of switching frequency. Fig. 21 shows the optimum power device size and the corresponding peak total efficiency of the converter with the modified active pull-up driver, for $D = 0.5$ and $P_{out} = 5$ W over the frequency range of 40–200 MHz. For each frequency, the chip parameters are optimized, and the inductor is selected such that the low-to-high ZVS transition is 7.5% of the switching period at $P_{out} = 2.5$ W. The inductance as a function of frequency is shown in Fig. 21(c). In the results shown, inductor losses are excluded. A dip in the curves can be seen around 75 MHz, which is due to partial ZVS operation at frequencies greater than 75 MHz.

At 40 MHz switching frequency, the model predicts 93% power-stage efficiency and 90% total efficiency at 5 W output

Fig. 22. Synchronous buck converter prototype with the GaN chip using the modified active pull-up driver.

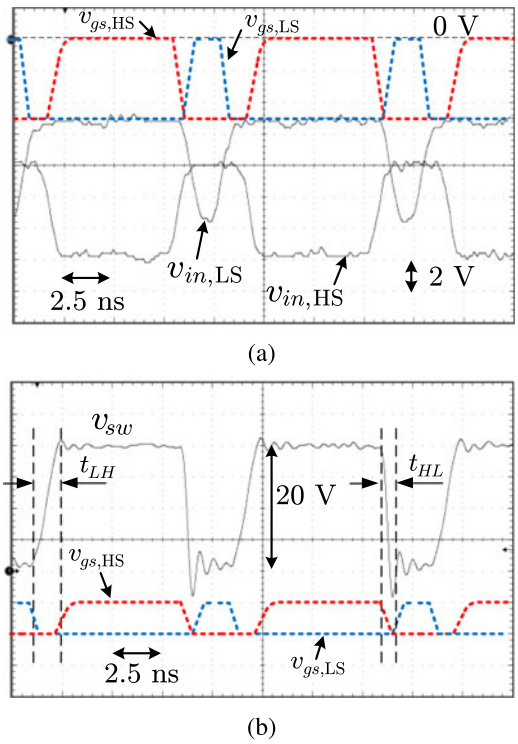


Fig. 23. (a) Measured control signals at the input stage: $v_{\mathrm{in,HS}}$ and $v_{\mathrm{in,LS}}$ at $v_{\mathrm{in}} = 0$ V, $f_{\mathrm{sw}} = 100$ MHz, and the sketched gate-to-source voltages $v_{\mathrm{gs,HS}}$ and $v_{\mathrm{gs,LS}}$; and (b) switching node voltage with ZVS, v_{sw}, at $v_{\mathrm{in}} = 20$ V, $v_{\mathrm{out}} = 14$ V, $P_{\mathrm{out}} = 2.2$ W, $f_{\mathrm{sw}} = 100$ MHz, with the same sketched gate-to-source voltages $v_{\mathrm{gs,HS}}$ and $v_{\mathrm{gs,LS}}$.

power. At 100 MHz, the predicted power-stage efficiency is 89% and the total efficiency is 86%. At 200 MHz, the efficiencies drop to 85% and 81% for the power-stage and the total, respectively.

IV. Experimental Results

The converter chips, fabricated and packaged using 20-pin 4×4 mm QFN packages, are used to build three 20 V, 5 W synchronous buck converters operating at 100 MHz switching frequency. Pulsewidth-modulated (PWM) control signals with 125 ps duty-cycle resolution are generated using an Altera Stratix IV FPGA. The control signals are transmitted through level shifter matching networks to obtain the desired voltage swings for the integrated converter chips. Filter components capable of operating at high frequencies are selected: low-ESR decoupling and output filtering capacitors (American Technical

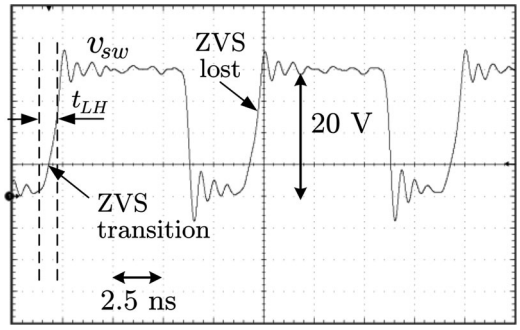


Fig. 24. Switching node voltage with partial ZVS, v_{sw}, at $v_{\mathrm{in}} = 20$ V, $v_{\mathrm{out}} = 14$ V, $P_{\mathrm{out}} = 2.7$ W, $f_{\mathrm{sw}} = 100$ MHz.

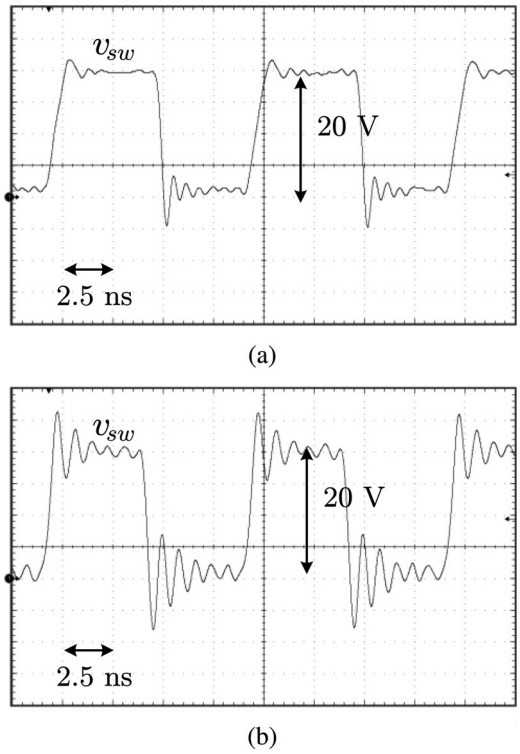


Fig. 25. (a) Switching node voltage with ZVS, v_{sw}, at $v_{\mathrm{in}} = 20$ V, $v_{\mathrm{out}} = 10$ V, $P_{\mathrm{out}} = 2$ W, $f_{\mathrm{sw}} = 100$ MHz; and (b) switching node voltage with hard-switching (no ZVS), v_{sw}, at $v_{\mathrm{in}} = 20$ V, $v_{\mathrm{out}} = 10$ V, $P_{\mathrm{out}} = 3.8$ W, $f_{\mathrm{sw}} = 100$ MHz.

Ceramics), and high-Q air-core inductors (1812SM series from Coilcraft).

Four-layer PCBs are designed to minimize the switching node parasitic capacitance and trace inductances, similar to the designs described in [12]. Fig. 22 shows a prototype with the modified active pull-up driver. The other two prototypes are similar.

Fig. 23 shows the control pulses $v_{\mathrm{in,HS}}$, $v_{\mathrm{in,LS}}$ and the switching node voltage v_{sw} at $D = 0.75$, 2.2 W output power and 100 MHz switching frequency, where the gate-to-source waveforms $v_{\mathrm{gs,HS}}$ and $v_{\mathrm{gs,LS}}$ are sketched to help verify ZVS operation according to the timing obtained by simulations. The waveforms are well-behaved with noticeable ZVS transitions observed in Fig. 23(b). At 2.7 W output power, partial ZVS

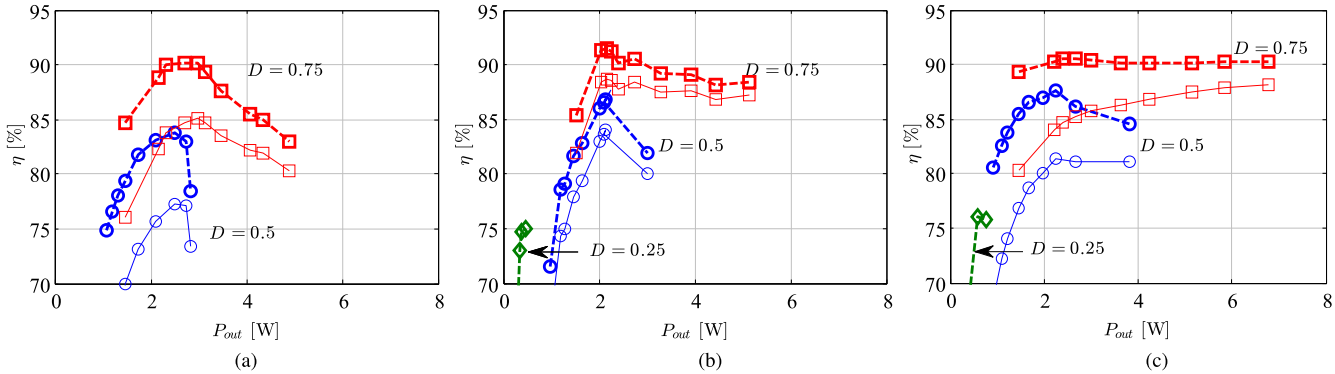


Fig. 26. Power stage efficiencies (dotted lines) and total efficiencies (solid lines): (a) active pull-up driver; (b) bootstrapped driver; and (c) modified active pull-up driver.

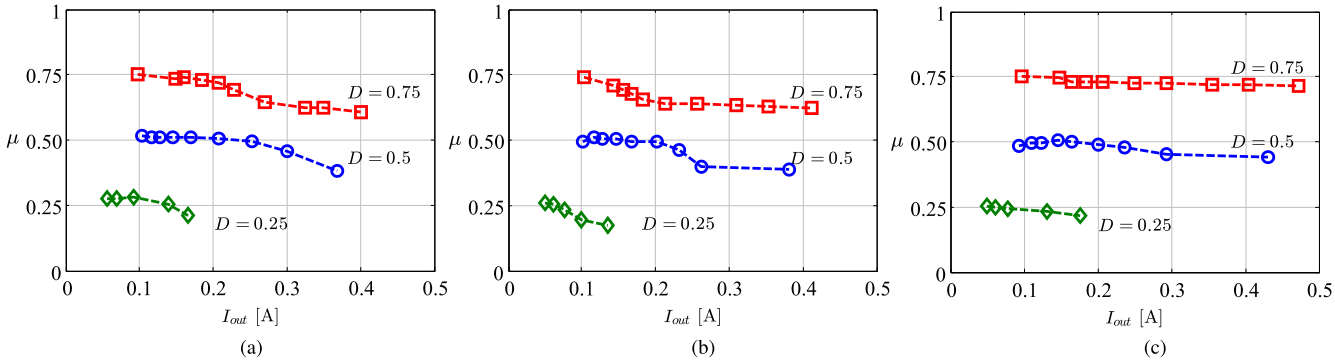


Fig. 27. Voltage conversion ratio (μ): (a) active pull-up driver; (b) bootstrapped driver; and (c) modified active pull-up driver.

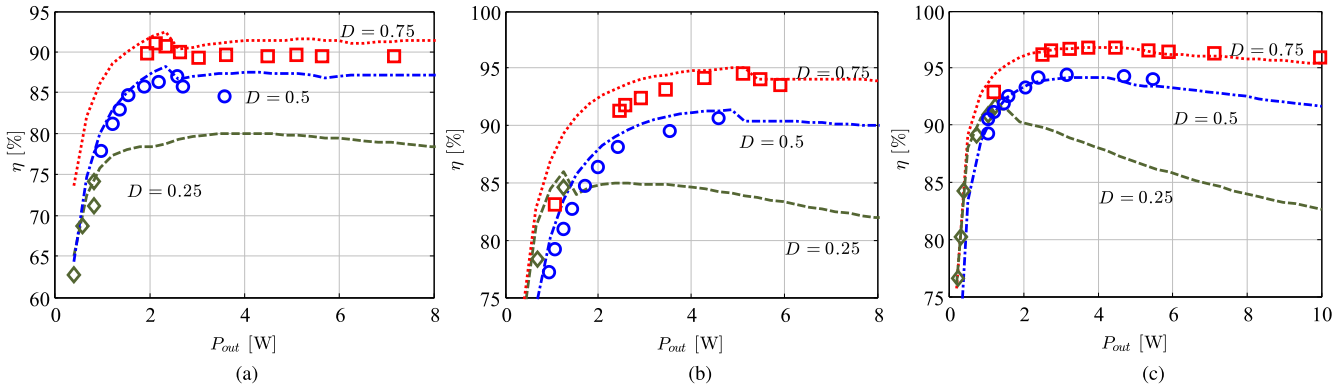


Fig. 28. Buck converter measured versus calculated power stage efficiency at 20 V: (a) $f_s = 100$ MHz, 47-nH inductor; (b) $f_s = 40$ MHz, 90-nH inductor; and (c) $f_s = 10$ MHz, 538-nH inductor.

occurs, as shown by the switching node voltage waveform in Fig. 24. At the beginning of the rising edge, a resonant transition with lower slope is observed first, followed by a hard-switching transition and larger ringing. Fig. 25 shows additional switching node voltage waveforms at $D = 0.5$. A resonant ZVS transition can be observed at the rising edge in Fig. 25(a). When soft-switching is completely lost, larger ringing can be observed in the switching node voltage, as shown in Fig. 25(b). This ringing is due to a resonance between bonding wire inductances and on-chip and off-chip capacitances at the switching node and the supply node. On the chip die, however, the ringing amplitude is limited by the integrated antiparallel Schottky diodes and likely smaller in amplitude compared to the ringing observed externally using a scope probe. No adverse effects have been observed in the operation of the gate driver circuitry due to hard switching.

Efficiency is measured at 100 MHz switching frequency, and 20 V input voltage, at several duty cycles (0.25, 0.5, 0.75), and output power levels, up to 7 W. The output filter includes a 47 nH inductor, which allows ZVS within a range of operating conditions (up to about 3 W at $D = 0.75$), when proper dead times are applied in the control signals. Fig. 26 shows the measured efficiencies for the three prototypes. Power-stage efficiencies are shown as bold dotted lines; total efficiencies,

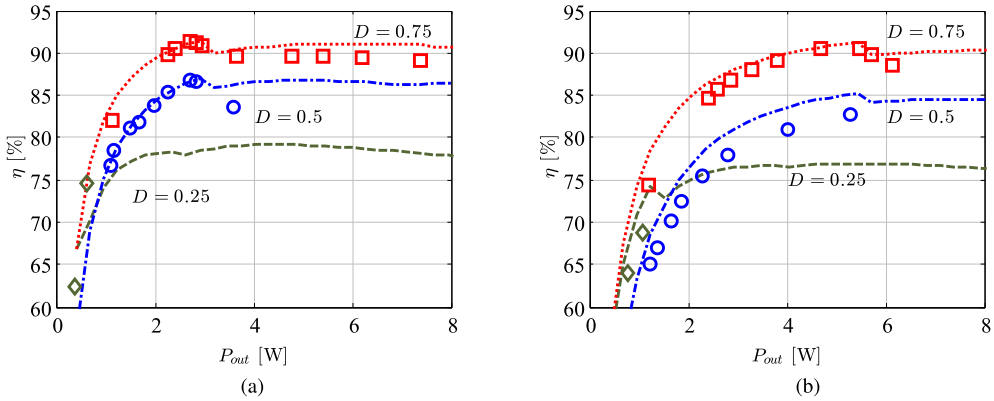


Fig. 29. Buck converter measured versus calculated power stage efficiency at 20 V and $f_s = 100$ MHz, with: (a) 39-nH inductor and (b) 27-nH inductor.

including on-chip gate driver losses, are shown using thinner solid lines. For all three power stages, efficiencies peak above 90%. The active pull-up driver has the lowest power-stage efficiency, as shown in Fig. 26(a), due to the higher on-resistance of the smaller power-stage devices, selected as a compromise against the driver power losses. The converter with the modified active pull-up driver has the highest power-stage efficiency over a wide range, as shown in Fig. 26(c). In terms of total efficiency, including gate driver losses, the bootstrapped driver performs the best, as shown in Fig. 26(b), but this is because this chip does not include the low-side gate driver.

Voltage conversion ratio plots are given in Fig. 27, where duty cycle D corresponds to the FPGA command value. As a result of losses, ZVS, and other timing imperfections, the actual conversion ratio $\mu = V_{\text{out}}/V_{\text{in}}$ tends to drop when the load current is increased. The prototype with the modified active pull-up driver exhibits the most favorable characteristics: flat conversion ratio curves with $\mu \approx D$ over the widest range of currents. This simplifies control and signal predistortion, especially in envelope tracking applications [12], [19].

In order to verify the power stage loss model, the converter performance is measured at three different switching frequencies (100, 40, and 10 MHz), and at several duty cycles (0.25, 0.5, and 0.75) over a range of output power levels. The output filter includes a 47 nH (or 90 nH, or 538 nH) inductor for 100 MHz (or 40 MHz, or 10 MHz), respectively. In addition, the converter is measured at 100 MHz switching frequency with two other inductors: 39 nH and 27 nH, for further verification. In Figs. 28 and 29, the measured power stage efficiencies are shown as markers, whereas lines represent the loss model predicted efficiencies. A good agreement can be observed between the experiments and the analytical model.

A loss budget for the converter operating at 100 MHz switching frequency, 0.75 duty cycle with 47-nH inductor is shown in Fig. 30, for two output power levels in order to compare ZVS and hard-switching operation. The loss model attempts to include all major loss mechanisms but is still simple enough to allow design optimization. Up to about 11% of loss is not accounted for by the loss model. Discrepancies between the model and the measured results can be ascribed to (a) approximations employed and modeling errors, and (b) second-order loss mechanisms.

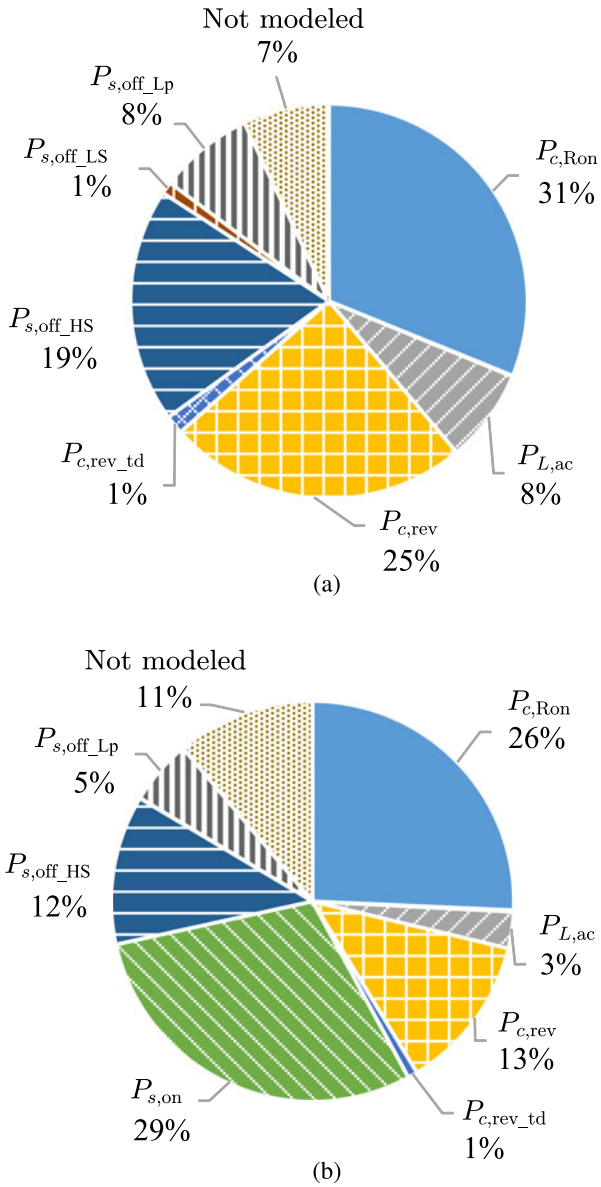


Fig. 30. Power stage loss break-down at 20 V, $D = 0.75$ and $f_s = 100$ MHz with 47 nH inductor: (a) $P_{\text{out}} = 2.3$ W, ZVS; and (b) $P_{\text{out}} = 5$ W, hard switching. Values below 1% are not shown.

TABLE VI
PREDICTED VERSUS MEASURED DRIVER LOSS FOR MODIFIED ACTIVE PULL-UP DRIVER

D	0.25	0.5	0.75
Estimated P_d [mW]	204	194	184
Measured P_d [mW]	206	192	180

The unmodeled effects include the temperature dependence of on-resistance and losses associated with capacitor ESRs. For the ZVS case, conduction loss, including reverse conduction, dominates, as shown in Fig. 30(a). For the hard switching case, both conduction loss and switching loss are significant, as shown in Fig. 30(b). Finally, good agreement between the estimated total driver loss (including switching loss) and the measured data can be observed in Table VI.

V. CONCLUSION

Integration is a key step in utilizing advances in GaN technologies and enabling efficient switched-mode power conversion at VHF. This paper addresses integration of gate driver circuits with half-bridge power stages in a depletion-mode GaN-on-SiC process, targeting VHF PWM dc–dc converters. Three gate driver circuit topologies are considered and compared: an active pull-up driver, a bootstrapped driver, and a novel modified active pull-up driver. Circuit operation and design tradeoffs are described for the three gate drivers. An analytical loss model is developed and used to optimize the monolithic GaN chips, which are then used to construct 20 V, 5 W, 100 MHz synchronous buck converter prototypes. The converter prototypes are tested at various duty cycles and output power levels. The loss model and the design optimization results are verified by experimental results. Power stage efficiencies peak around 91% for the chips with the bootstrapped and the modified active pull-up integrated drivers. The modified active pull-up driver is found to be the best suited for the depletion-mode process. It requires the smallest area (80% reduced gate-driver area compared to the bootstrapped driver), and results in the power-stage efficiency above 90% over a wide range of operating points. The monolithic GaN chip with the modified active pull-up driver shows the best performance in terms of voltage conversion ratio, total efficiency, and overall simplicity.

The results presented in this paper demonstrate feasibility of high-efficiency VHF PWM dc–dc converters based on high levels of integration in a GaN process, and the use of air-core inductors. Directions open for future work include scaling to higher power and voltage levels, as well as design and implementation of controller chips to support PWM switching at VHF.

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