Understanding the Effect of PCB Layout on Circuit Performance in a High-Frequency Gallium-Nitride-Based Point of Load Converter

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***Abstract*—The introduction of enhancement-mode gallium-nitride-based power devices such as the eGaN FET offers the potential to achieve higher efficiencies and higher switching frequencies than possible with silicon MOSFETs. With the improvements in switching performance and low parasitic packaging provided by eGaN FETs, the printed circuit board (PCB) layout becomes critical to converter performance. This paper will study the effect of PCB layout parasitic inductance on efficiency and peak device voltage stress for an eGaN FET-based point of load (POL) converter operating at a switching frequency of 1 MHz, an input voltage range of 12–28 V, an output voltage of 1.2 V, and an output current up to 20 A. This paper will also compare the parasitic inductances of conventional PCB layouts and propose an improved PCB design, providing a 40% decrease in parasitic inductance over the best conventional PCB design.**

***Index Terms*—DC–DC power conversion, packaging, power semiconductors.**

I. Introduction

NONISOLATED point of load (POL) converters are found in computers, telecommunication systems, handheld electronics, and many other applications. With the ever increasing power demands of modern technologies, combined with the desire for smaller size and lower power consumption, the pursuit of POL converters achieving higher power density and efficiency is a necessity to meet system demands. The majority of POLs are nonisolated step down buck converters, often having a large step down ratio from as high as 28 V input to 1.2 V output. The most straightforward way to improve power density in a traditional buck converter is to increase switching frequency, enabling a volume reduction in the output inductor and capacitors [1]. The practical issue with increasing switching frequency is a decrease in efficiency as a result of higher losses, limiting current silicon (Si) based solutions to the range of a couple hundred kilohertz to a megahertz.

To improve the high-frequency performance of silicon-based POL converters, there have been many efforts to improve device characteristics and packaging. For improved device performance, the switching-related parameters, gate to drain charge (Q_{GD}), gate to source switching charge (Q_{GS2}), and gate charge (Q_G) for the top switch have decreased and body diode reverse recovery (Q_{RR}) and body diode forward voltage (V_{DF}) for the synchronous rectifiers have been improved with the addition of an internal Schottky diode. Advanced packaging techniques have also improved performance by providing reduced parasitic inductances [2]–[4]. For silicon power devices, the gains in device performance have slowed as the technology reaches its theoretical limit [5] and the package improvements have been limited by the inherent trench structure at higher voltages.

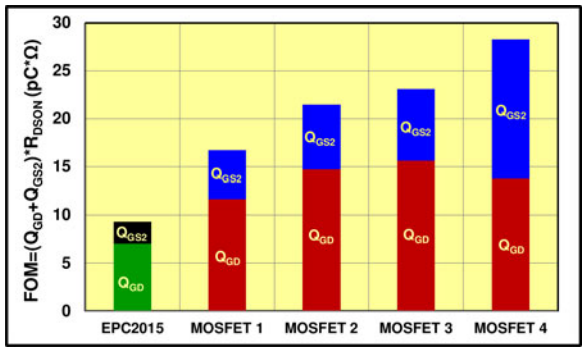

Fig. 1. Figure of merit comparison for 40 V devices.

Gallium nitride (GaN) transistors have emerged as a possible replacement for silicon devices in various power conversion applications. GaN transistors are a high electron mobility transistor (HEMT) with a higher band gap, electron mobility, and electron velocity than silicon and silicon carbide devices [6]. These material characteristics make the GaN device more suitable for higher frequencies and higher voltage operation.

The first commercially available enhancement mode GaN devices have a lateral structure with voltages ranging from 40 to 200 V. These devices operate similarly to the traditional Si MOSFETs and can provide improved switching and packaging performance [7]. The comparison of switching figure of merit (FOM) for 40 V devices is shown in Fig. 1, the eGaN FET has a 45% lower FOM than the best state-of-the-art Si device.

With higher switching speeds and lower package parasitic inductance, the PCB layout becomes a limiting factor in converter performance. To demonstrate the impact of PCB layout on performance, this study will compare three different PCB designs' efficiency and peak voltage stress for a 1 MHz eGaN FET-based POL. The three designs will comprise two conventional PCB layouts and a proposed improved layout. The parasitic

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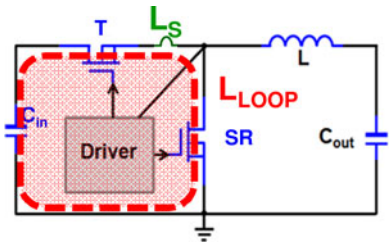

Fig. 2. Synchronous buck converter with parasitic inductances.

inductances of the designs will be compared for different board thicknesses and builds. The final demonstration is an optimal layout with a switching frequency of 1 MHz, an input voltage range of 12–28 V, an output voltage of 1.2 V, and an output current up to 20 A demonstrating the superior capability of eGaN FETs.

II. Evaluating Impact of Parasitic Inductance on Switching Performance in an eGaN FET Synchronous Buck Converter

In a practical buck converter, there are two major parasitic inductances that have a significant impact on converter performance, as shown in Fig. 2. The common source inductance L_s is the inductance shared by the drain to source power current path and gate driver loop. The high-frequency power loop L_{Loop} is the power commutation loop and comprised of the parasitic inductance from the positive terminal of the input capacitance, through the top device (T), synchronous rectifier (SR), ground loop, and input capacitor (C_{in}).

The common source inductance L_s has been shown to be critical to performance because it directly impacts the driving speed of the devices [8]–[10]. The available gate drive current at turn on is given by

$$I_G = \frac{V_{\mathrm{Driver}} - V_{\mathrm{GS}} - V_{\mathrm{LS}}}{R_G} = \frac{V_{\mathrm{Driver}} - V_{\mathrm{GS}} - L_S \cdot (di_D/dt)}{R_G} \tag{1}$$

where I_G is the gate drive current, V_{Driver} is the gate drive voltage, V_{GS} is the gate to source voltage across the device, V_{LS} is the effective voltage across the common source inductance, which is equal to $L_S \cdot di_D/dt$ during device commutation, and R_G is the gate resistance of the driver and the eGaN FET.

The common source inductance is mainly controlled by the package inductance of the device. There has been significant effort to reduce the common source inductance to minimize switching loss [2]. In [7], the impact of the eGaN FET land grid array (LGA) package and the reduction of package parasitic inductance and resistance over the best available trench devices are quantified.

The high-frequency loop inductance L_{Loop} impacts the switching speed and the peak drain to source voltage spike of the devices. The high-frequency loop inductance is mainly controlled by the circuit layout and package inductance. There have been research efforts to reduce the loop inductance in modules to minimize switching loss and voltage overshoot [11]–[15]. During the switching transition, a voltage is induced across the high-frequency loop inductance equal to

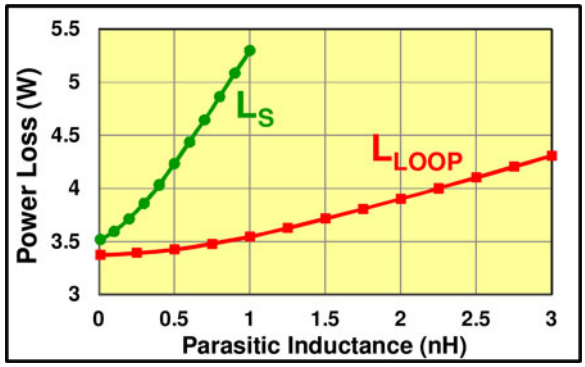

Fig. 3. Parasitic inductance impact on power loss ($V_{\mathrm{IN}} = 12$ V, $V_{\mathrm{OUT}} = 1.2$ V, $I_{\mathrm{OUT}} = 20$ A, Fs = 1 MHz, $L = 150$ nH, T: EPC2015 SR: EPC2015).

$$V_{L_{\mathrm{Loop}}} = L_{\mathrm{Loop}} \cdot \frac{di_D}{dt}. \tag{2}$$

During the turn-on transition of a device, the drain current is rising and the positive di_D/dt across the loop inductance reduces the effective voltage across the device, reducing switching loss and resulting in a negative voltage spike. During the turn-off transition, the drain current is falling and the negative di_D/dt across the loop inductance increases the effective voltage across the device, inducing a positive voltage spike and increasing switching loss.

The impact of parasitic inductance on total power loss for an eGaN buck converter is calculated and shown in Fig. 3 [15]. It can be seen that by introducing common source and high-frequency loop inductance, the loss increases. By adding as little as 1 nH of common source inductance, losses can increase 50% over an ideal case. This is due to common source inductance's negative impact on both turn-on and turn-off switching transitions. Adding 3 nH of loop inductance increases loss by 30% over the ideal case. The smaller relative increase in loss is a result of the partial loss savings at turn on from high-frequency loop inductance.

Understanding the impact of parasitic inductance on performance, the designers of the eGaN FET made the reduction of package parasitics a high priority. For the eGaN FET, a device with a higher voltage lateral structure, all of the connections are contained on the same side of the die. This allows for the die to be mounted directly to the PCB, minimizing the total parasitics to the internal bussing and external solder bumps. To further decrease parasitics, the drain and source connections are arranged in an interleaved LGA, providing multiple parallel connections to the PCB from the die. The result is a device package inductance in the range of a couple hundred picohenry [7].

With the significant reduction in package-related inductance provided by the eGaN FET, the package inductance is minimized and no longer the major parasitic loss contributor. The high-frequency loop inductance, controlled by PCB layout now becomes a major contributor to loss, making layout of the eGaN FETs critical to high-frequency performance. To verify this, different layouts with similar common source inductance and different loop inductances were compared. From the efficiency

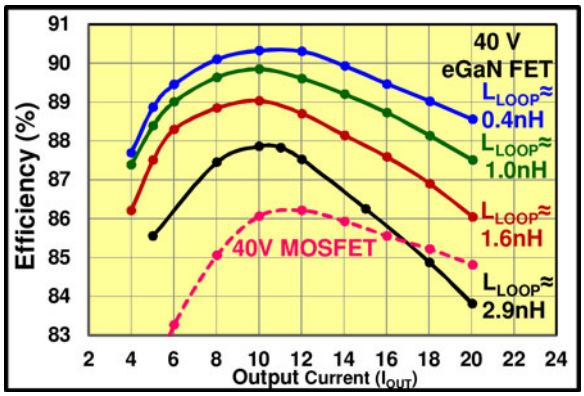

Fig. 4. Impact of high-frequency loop inductance on efficiency for designs with similar common source inductance ($V_{\rm IN}$ = 12 V, $V_{\rm OUT}$ = 1.2 V, Fs = 1 MHz, L = 150 nH, eGaN FETs: T: EPC2015 SR: EPC2015, MOSFETs: T: BSZ097N04LSG SR: BSZ040N04LSG).

curves obtained from various experimental prototypes, shown in Fig. 4, the impact of layout on efficiency can be seen for the eGaN FET at 1 MHz. An increase in the high-frequency loop inductance from around 0.4 to 2.9 nH results in additional loss, decreasing efficiency by over 4%.

The accuracy of the high-frequency parasitic loop inductances were verified experimentally by measuring the resonant frequency of the ringing voltage after the top switch turns on. When the top switch turns on, the high-frequency loop inductance and output capacitance of the synchronous rectifier ring at the resonant frequency, yielding

$$L_{\rm LOOP} = \frac{T_{\rm Ring}^2}{4 \cdot \pi^2 \cdot C_{\rm OSS}} \tag{3}$$

where $L_{\rm LOOP}$ is the high-frequency loop inductance, $T_{\rm Ring}$ is the ringing period, and $C_{\rm OSS}$ is the output capacitance of the synchronous rectifier.

As eGaN FETs significantly increase switching speeds by providing reduced FOM and package parasitics, even small values of high-frequency loop inductance cause an increase in voltage overshoot when compared with slower, higher parasitic Si MOSFET devices. Decreasing the high-frequency loop inductance results in lower voltage overshoot, increased input voltage capability, and reduced EMI. Fig. 5 shows the drain to source voltage waveforms of the synchronous rectifier for eGaN FET designs with a high-frequency loop inductance of 1.6 nH and 0.4 nH; the voltage overshoot is reduced from 100% of the input voltage to 25%, respectively.

III. Comparison of Conventional PCB Layouts

For eGaN FETs with faster switching speeds and lower packaging parasitic inductances, the layout can significantly degrade efficiency and cause voltage overshoot on the devices, as demonstrated in the previous section. In this section, the parasitic inductance of conventional PCB layouts will be compared for eGaN FET-based designs.

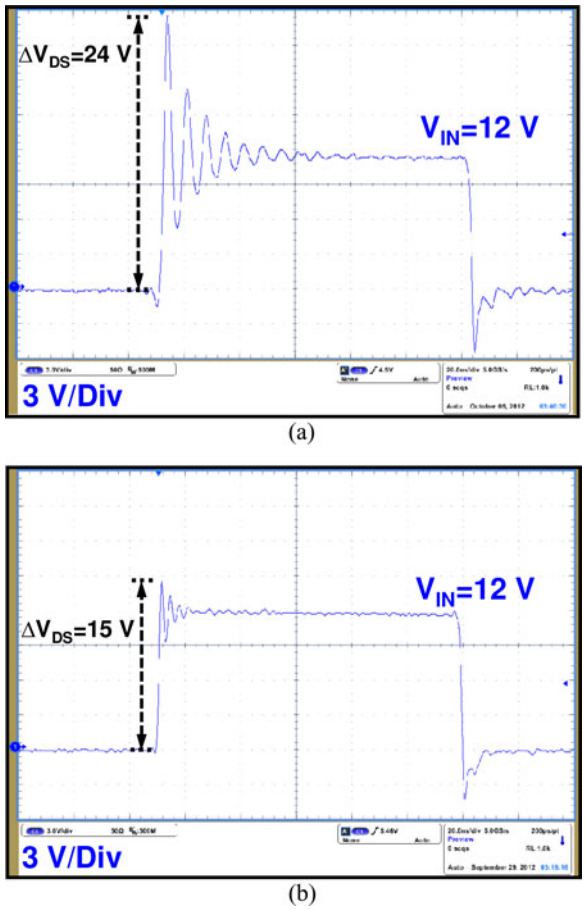

Fig. 5. Synchronous rectifier switching waveforms of designs with (a) $L_{\rm LOOP} \approx$ 1.6 nH and (b) $L_{\rm LOOP} \approx$ 0.4 nH ($V_{\rm IN}$ = 12 V, $V_{\rm OUT}$ = 1.2 V, $I_{\rm OUT}$ = 20 A, Fs = 1 MHz, L = 150 nH, eGaN FETs: T: EPC2015 SR: EPC2015).

A. Lateral High-Frequency Power Loop

The first conventional layout places the input capacitors and devices on the same side of the PCB in close proximity to minimize the size of the high-frequency loop [16]. The high-frequency loop for this design is contained on the same side of the PCB and is considered a lateral power loop as a result of the power loop flowing parallel to the board plane on a single layer. An eGaN FET design arranged in a lateral power loop was created and the part placement and high-frequency power loop are shown in Fig. 6 with the high-frequency loop highlighted in yellow. For this design, the inductor connection is made through internal layers using vias in between the top switch and synchronous rectifier. The driver layout is the same for all of the designs in this work, it is located in close proximity to the eGaN FETs to minimize common source and gate inductance and keep the common source and gate inductance constant between designs. This allows a comparison of only the influence of loop inductance.

While minimizing the physical size of the loop is important to reduce parasitic inductance, the design of the inner layers is also critical. For the lateral power loop design, the first inner layer serves as a "shield layer." This layer has a critical role to shield

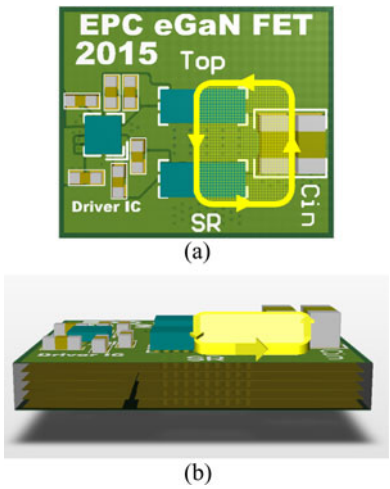

Fig. 6. Conventional lateral power loop with eGaN FETs. (a) Top view. (b) Side view.

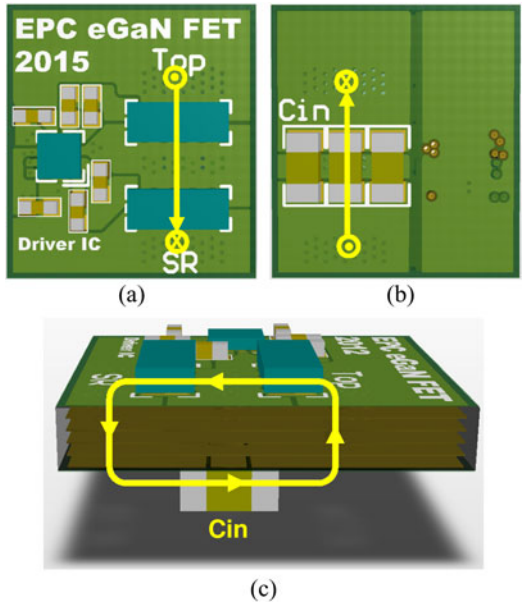

Fig. 7. Conventional vertical power loop with eGaN FETs. (a) Top view. (b) Bottom view. (c) Side view.

the circuit from the fields generated by the high-frequency power loop. The power loop generates a magnetic field that induces a current, opposite in direction to the power loop, inside the shield layer. The current in the shield layer generates a magnetic field to counteract the original power loop's magnetic field. The end result is a cancellation of magnetic fields that translates into a reduction in parasitic inductance. Having a complete shield plane in close proximity to the power loop provides the best performance.

For the lateral power loop design, the high-frequency loop inductance should show little dependence on board thickness as the power loop is contained on the top layer. The lateral design should be very dependent on the distance from the power loop to the shield layer which is contained on the first inner layer.

B. Vertical High-Frequency Power Loop

The second conventional layout places the input capacitors and devices on opposite sides of the PCB, with the capacitors generally being located directly underneath the devices to minimize the physical loop size (see Fig. 7). This layout is considered a vertical power loop because the power loop travels perpendicular to the board plane with vias connecting the power loop vertically through the board. An eGaN FET design arranged in a vertical power loop was created and the part placement and high-frequency power loop are shown in Fig. 7 with the high-frequency loop highlighted in yellow. Again, space is left between the devices to allow the inductor connection.

For the vertical power loop design, there is no shield layer due to the vertical structure of the power loop. As opposed to the use of a shield plane, the vertical power loop uses a field self-cancellation method to reduce inductance. For the PCB layout, the board thickness is generally much thinner than the horizontal length of the traces on the top and bottom side of the board. As the thickness of the board decreases, the area of the loop shrinks significantly when compared to the lateral power loop, and the current flowing in opposing directions on the top and bottom layers begins to provide field self-cancellation, further reducing parasitic inductance. For a vertical power loop to be effective, the board thickness must be minimized.

For the vertical power loop design, the loop inductance is heavily dependent on the board thickness as the power loop is contained on the top and bottom layers of the PCB. Without the requirement of a shield layer, the distance between the first inner layer and top layer has little impact on the inductance.

IV. Proposed Optimal Layout for Reduced High-Frequency Parasitic Inductance and Resistance

To provide the benefits of reduced loop size, field self-cancellation, consistent inductance independent of board thickness, a single-sided PCB design, and high efficiency for a multilayer structure, an improved optimal layout is proposed in this study, shown in Fig. 8. The design utilizes the first inner layer, shown in Fig. 8(b), as a power loop return path. This return path is located directly underneath the top layer's power loop, Fig. 8(a), allowing for the smallest physical loop size combined with field self-cancellation. The side view [see Fig. 8(c)] illustrates the concept of creating a low profile self-cancelling loop in a multilayer PCB structure. The characteristics of the conventional and proposed optimal designs are compared in Table I.

The improved layout places the input capacitors in close proximity to the top device, with the positive input voltage terminals located next to the drain connections of the top eGaN FET. The eGaN FETs are located in the same arrangement as the lateral and vertical power loop cases. Located between the two eGaN FETs is a series of interleaved inductor node and ground vias arranged to match the LGA fingers of the SR eGaN FET. The interleaved inductor node and ground vias are duplicated on the bottom side of the synchronous rectifier. These interleaved vias provide the following three advantages:

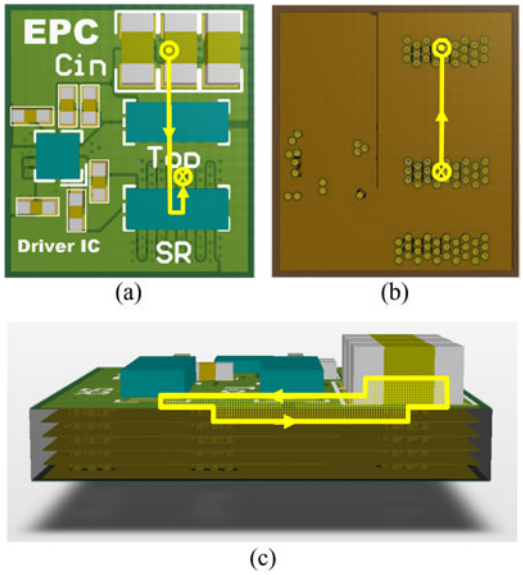

Fig. 8. Proposed optimal power loop with eGaN FETs. (a) Top view. (b) Top view of inner layer 1. (c) Side view.

TABLE I
CHARACTERISTICS OF CONVENTIONAL AND OPTIMAL POWER LOOP DESIGNS

	Lateral Loop	Vertical Loop	Optimal Loop
Single Sided PCB Capability	Yes	No	Yes
Field Self Cancellation	No	Yes	Yes
Inductance Independent of Board Thickness	Yes	No	Yes
Shield Layer Required	Yes	No	No

1) The via set located in between the two eGaN FETs provides a reduced length high-frequency loop inductance path leading to lower parasitic inductance.
2) The via set located beneath the SR eGaN FET provides additional vias for reduced resistance during the SR eGaN FET freewheeling period, reducing conduction losses.
3) The interleaving of the via sets with current flowing in opposing direction allows for reduced eddy and proximity effects, reducing ac conduction losses.

V. EXPERIMENTAL RESULTS

To compare the performance of the proposed optimal power loop with conventional lateral and vertical designs for a wide range of applications, four separate board builds were created. The designs varied the overall thickness of the board and the distance between the top layer and the first inner layer in the board (inner layer distance). These parameters are illustrated in Fig. 9. The specifications for the test boards are contained in Table II. The part layouts remained unchanged (see Figs. 6–8), and all the designs comprised four layers with two ounce copper thickness.

The values of the high-frequency loop inductance for varying board thicknesses and inner layer distance were simulated and the results are presented in Fig. 10. From the data, it can be seen that for the lateral power loop the board thickness has little impact on the high-frequency loop inductance, while the inner layer distance (the distance from the power loop to the shield layer) significantly impacts the inductance. For the vertical power loop, the inner layer distance has very little impact on the inductance of the design, while the board thickness significantly impacts the inductance by as much as 80% when the board thickness is doubled from 31 to 62 mil.

For the proposed layout, the design shares the traits of the lateral power loop by showing little dependence on board thickness and a strong dependence on inner layer distance. This design provides a significant reduction in loop inductance from the removal of the shield layer and reduced physical size of the power loop; traits similar to the vertical power loop design. Combining the strengths of both conventional designs, and limiting the weaknesses, the proposed design can provide a significant reduction in inductance compared to the best conventional lateral and vertical power loops.

The power loss for the four experimental designs is shown in Fig. 11 for the three different loop layouts. From these data, it can be seen that for similar parasitic inductances the power loss

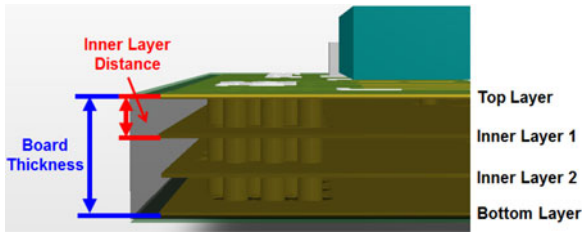

Fig. 9. PCB cross-section drawing of board thickness and inner layer distance for experimental designs.

TABLE II
BOARD SPECIFICATIONS FOR LAYOUT COMPARISON

	Board Thickness (mils)	Inner Layer Distance (mils)
Design 1	31	4
Design 2	31	12
Design 3	62	4
Design 4	62	26

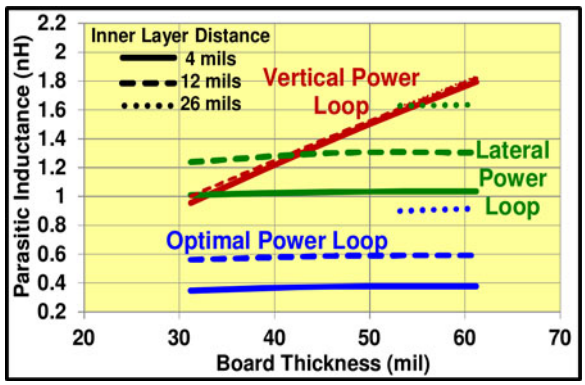

Fig. 10. Simulated high-frequency loop inductance values for lateral, vertical, and optimal power loops with different board thickness and inner layer distance.

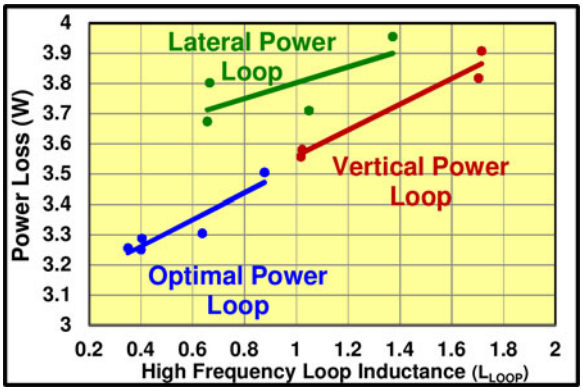

Fig. 11. Experimental power loss plot for lateral, vertical, and optimal power loop designs ($V_{\rm IN}$ = 12 V, $V_{\rm OUT}$ = 1.2 V, $I_{\rm OUT}$ = 20 A, Fs = 1 MHz, L = 300 nH, T: EPC2015 SR: EPC2015).

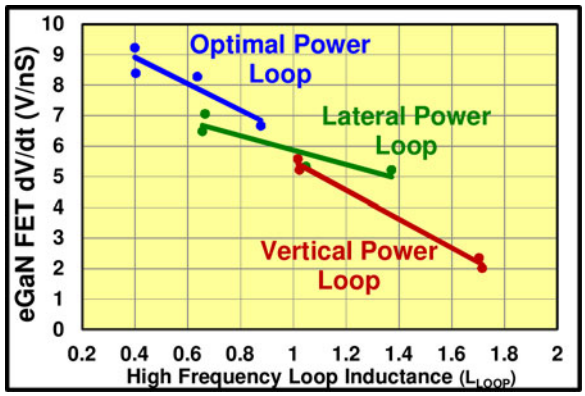

Fig. 13. Measured device switching speed versus loop inductance ($V_{\rm IN}$ = 12 V, $V_{\rm OUT}$ = 1.2 V, $I_{\rm OUT}$ = 20 A, Fs = 1 MHz, L = 300 nH, T: EPC2015 SR: EPC2015).

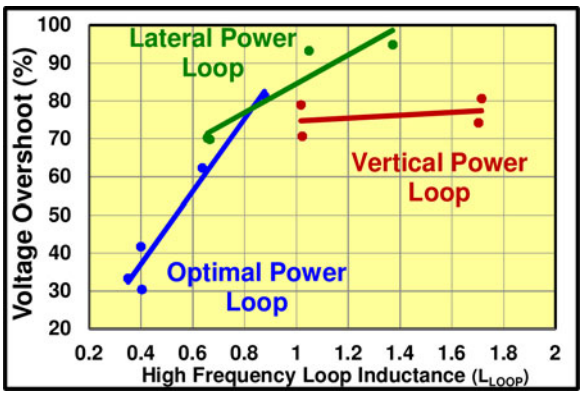

Fig. 12. Measured voltage overshoot versus loop inductance ($V_{\rm IN}$ = 12 V, $V_{\rm OUT}$ = 1.2 V, $I_{\rm OUT}$ = 20 A, Fs = 1 MHz, L = 300 nH, T: EPC2015 SR: EPC2015).

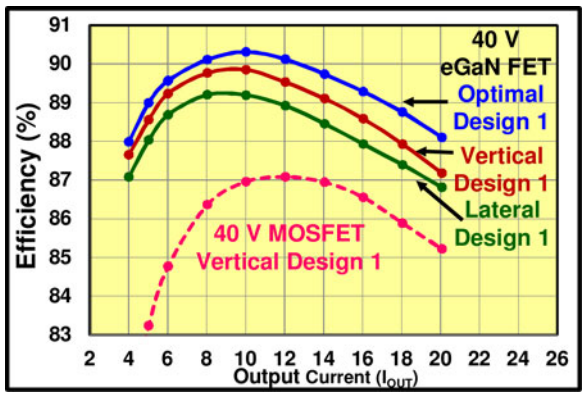

Fig. 14. Efficiency comparisons for design 1 ($V_{\rm IN}$ = 12 V, $V_{\rm OUT}$ = 1.2 V, Fs = 1 MHz, L = 300 nH, eGaN FETs: T: EPC2015 SR: EPC2015, MOSFETs: T: BSZ097N04LSG SR: BSZ040N04LSG).

of the lateral loop is higher than the vertical loop. The cause of the increased loss in the lateral power loop can be attributed to the additional loss in the shield layer, which is not required in the vertical or proposed power loop. The experimental hardware verifies the predicted trend of increased loop inductance and higher power loss.

The voltage overshoot for the different designs is shown in Fig. 12. As loop inductance increases up to 1.4 nH, so does the voltage overshoot. When the loop inductance is over 1.4 nH, the voltage overshoot does not significantly increase further. This can be explained by Fig. 13 that shows the measured switching speed of the different designs. As the loop inductance increases, the *dV/dt* of the device decreases significantly. This results in higher power loss, but helps limit voltage overshoot. For the two vertical loop designs with the highest loop inductance, the switching speed is reduced over 60% when compared to all the other designs.

Shown in Fig. 14 are the efficiency results of design 1 for the three proposed designs compared to a silicon implementation utilizing a vertical power loop with the smallest commercial package, a 3 $\times$3 mm TSDSON-8, to minimize the power loop. For the Si MOSFET design, the high-frequency loop inductance was measured to be around 2 nH, compared to 1 nH for a similar power loop using eGaN FETs. This is due to the large packaging inductance of the Si MOSFET dominating the loop design. As a result of the superior FOM and packaging of the eGaN FETs, all of the power loop structures outperform the Si MOSFET benchmark design. With the optimal power loop, the efficiency can be improved for the eGaN FETs. An almost 3% full load and a 3.5% peak efficiency improvement is achieved when compared to the Si MOSFET.

For the different eGaN designs, the optimal power loop provides a 0.8% and 1% full load efficiency improvement over the vertical and lateral power loops, respectively. For all of the design tests outlined in Table II, the optimal layout provides the highest efficiency and lowest device voltage overshoot.

The switching waveforms for the eGaN FET vertical and optimal layouts and Si MOSFET vertical layout benchmark are shown in Fig. 15. Both eGaN FET designs offer significant switching speed gains when compared to the Si MOSFET benchmark. For the eGaN FET with the conventional vertical layout, the high switching speed combined with a traditional PCB layouts loop inductance experiences a large voltage spike. The optimal layout eGaN FET design offering minimized loop

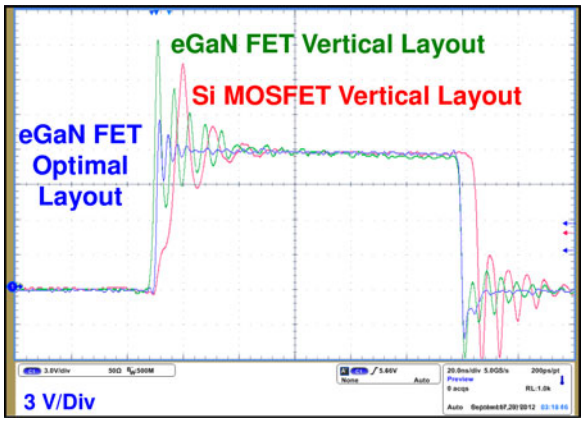

Fig. 15. Synchronous rectifier switching waveforms of optimal eGaN FET, vertical eGaN FET, and vertical MOSFET design 1 ($V_{\mathrm{IN}} = 12$ V, $V_{\mathrm{OUT}} = 1.2$ V, $I_{\mathrm{OUT}} = 20$ A, Fs = 1 MHz, $L = 300$ nH, eGaN FETS: T: EPC2015 SR: EPC2015, MOSFETs: T: BSZ097N04LSG SR: BSZ040N04LS G).

Fig. 16. Experimental prototype for optimal design 1 (eGaN FETS: T: EPC2015 SR: EPC2015 Driver: LM5113).

inductance offers a 500% increase in switching speed and a 40% reduction in voltage overshoot when compared to the 40 V Si MOSFET benchmark. For the eGaN FET with low package parasitic inductance, the layout is critical to switching at high speeds, limiting device overshoot, and improving efficiency (see Fig. 16).

With the reduced voltage overshoot and high efficiency achievable with the optimal eGaN FET layout, the converter has the ability to handle much higher input voltages with low voltage rated devices. The converter was operated at input voltages of 12, 19, 24, and 28 V, and the efficiency curves are shown in Fig. 17. As the input voltage increases, the switching losses in the converter also increase, leading to lower efficiency. With the reduction in switching losses and reduced voltage overshoot provided by the optimal layout, the efficiency can be improved for higher input voltage designs.

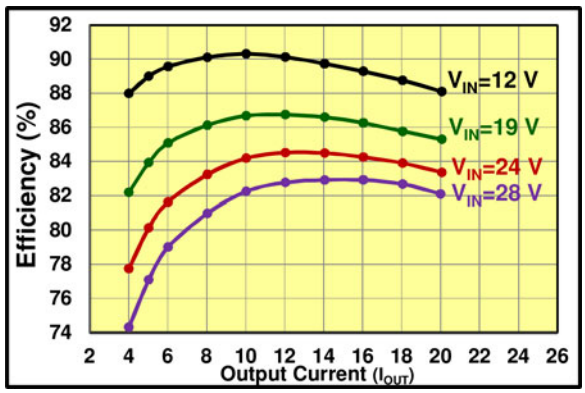

Fig. 17. Efficiency of optimal layout design 1 at varying input voltages ($V_{\mathrm{OUT}} = 1.2$ V, Fs = 1 MHz, $L = 300$ nH, eGaN FETs: T: EPC2015 SR: EPC2015).

VI. Conclusion

The introduction of high-performance GaN FETs offers the potential to switch at higher frequencies and efficiency than possible with traditional Si MOSFET technology. Combined with improved figures of merit and low parasitic packaging, GaN FETs require a low parasitic PCB layout to fully utilize the device's capability. The impact of PCB layout parasitics on circuit efficiency has been assessed, and there has been significant effort to reduce these parasitics. To evaluate the impact of high-frequency loop inductance on performance, multiple designs of conventional lateral and vertical power loops with the same minimal common source inductance were created and compared.

To overcome the limitations of the conventional PCB layouts, an optimal layout is proposed to achieve the best performance with eGaN FETs. This layout achieved the following:

1) A 40% reduction in high-frequency loop inductance compared to conventional PCB designs.
2) A 35% reduction in voltage overshoot compared to conventional PCB designs.
3) A 10% decrease in total power loss compared to conventional PCB designs.
4) A compact single sided design with high-frequency loop inductance independent of board thickness

With all of the PCB designs studied in this paper, eGaN FETs significantly outperformed the best equivalent silicon devices on the market today. Through the use of an optimal layout, the benefits of eGaN FET technology are further enhanced, providing additional efficiency gains and higher voltage operation capability.

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