Date: 23.06.2019

Attendees: Enes Ayaz, Mesut Uğur

Location: Electrical Machines Laboratory

Target: V1.3 Gate Driver Board (#1)

Test type: Single, Series and Parallel Connected Inverter tests with RL load

Aims before the test:

1. To observe the voltage of each DC bus capacitor to obtain its current.

2. To the module voltages of series connected modules with and without interleaving

Conditions: 22 Ohm Ron, 2 Ohm Roff. 300V VDC. RL Load. 40kHz fsw. 0.9 power factor. Sinusoidal PWM with 0.9 modulation index.

Steps:

1. Single inverter is tested with maximum load and 100V DC bus using Agilent power supply. Voltage of each capacitor and DC link current are recorded.
2. Single inverter is tested with maximum load and 300V DC bus using Semicron power supply. Voltage of each capacitor and DC link current are recorded.
3. Modules are connected in series and tested with partially balanced load with 100V DC bus using Agilent power supply. Voltage of each modules and total voltage are recorded using conventional PWM.
4. Step 3 is repeated with interleaving.

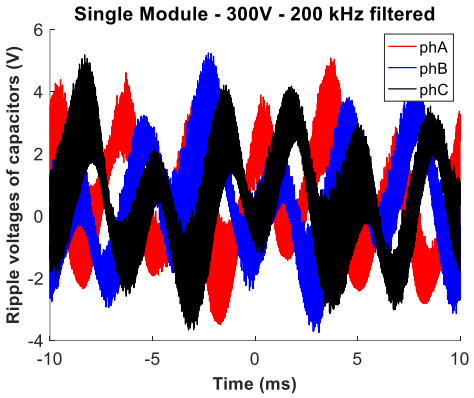
Next time: Series connection test will be repeated with higher voltage. Parallel connected modules will be tested with and without interleaving.

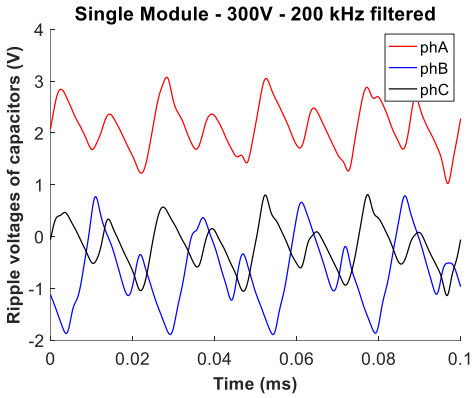
Results:

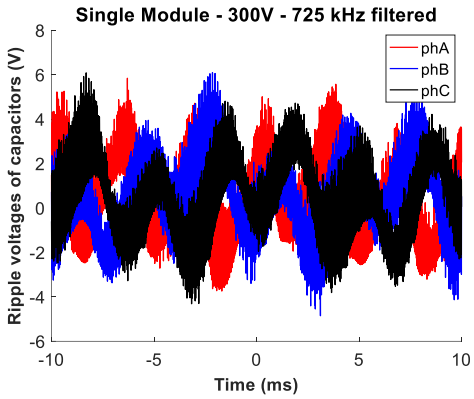
1. Single module – 100V

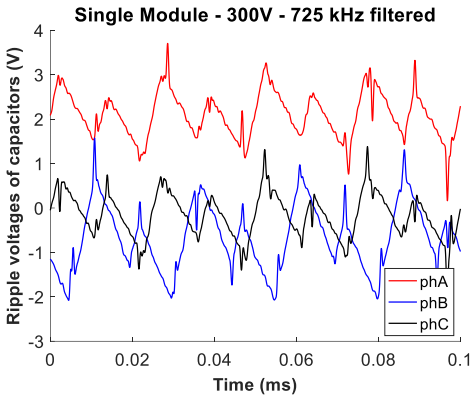
Data is not included since the tests are performed with 300V later.

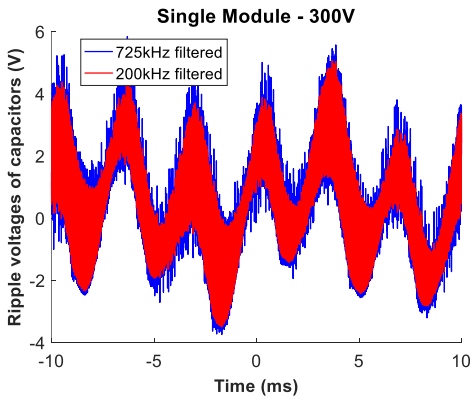
2. Single module – 300V

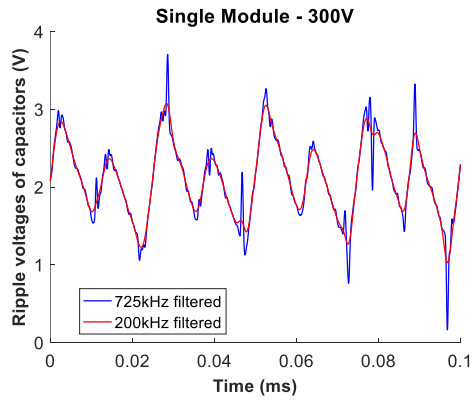


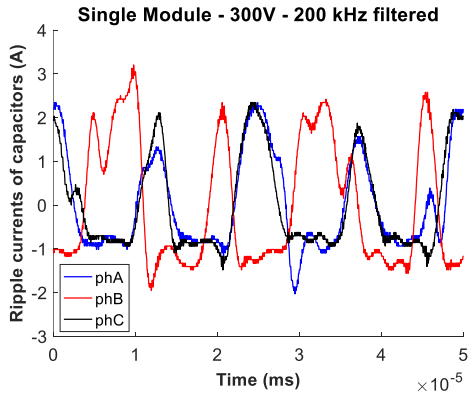


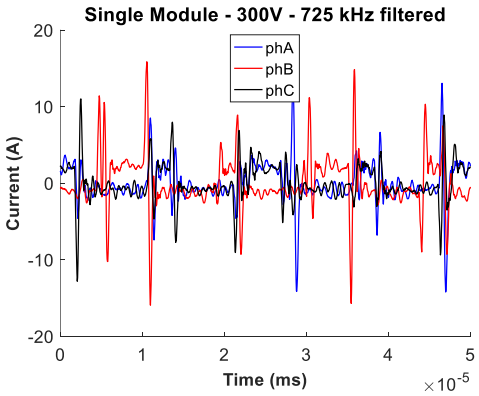


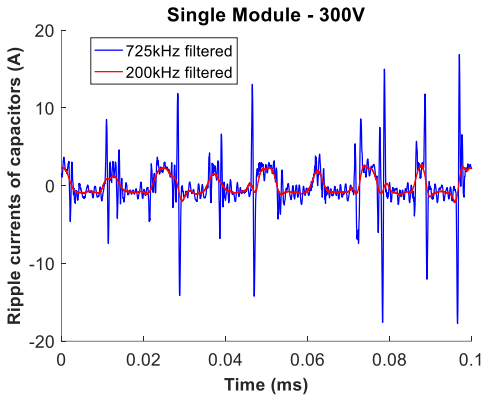


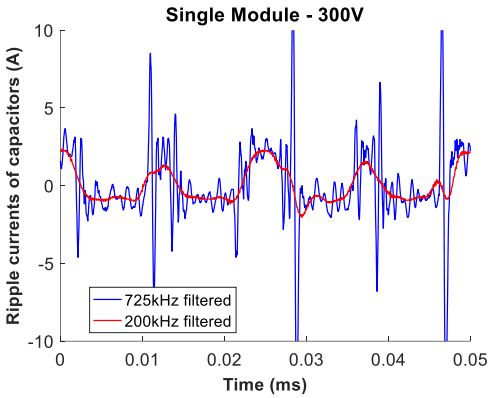


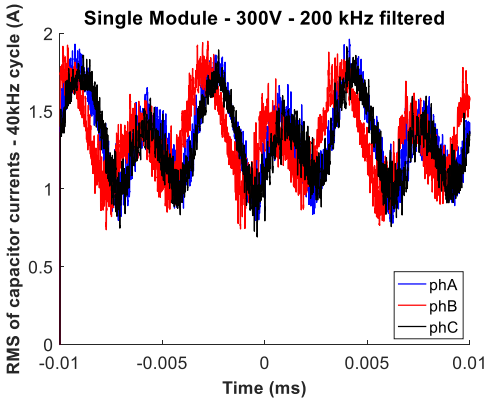


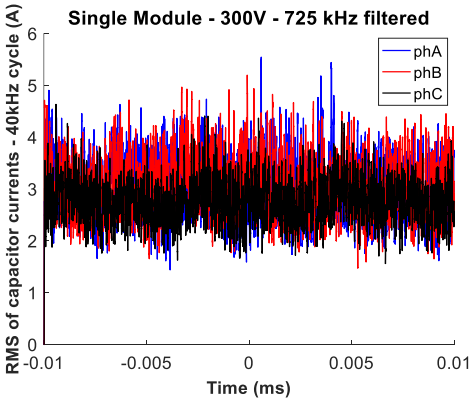

Single Module - 300V - 200 kHz filtered
Ripple currents of capacitors (A)
Time (ms)
×10^-5
phA
phB
phC

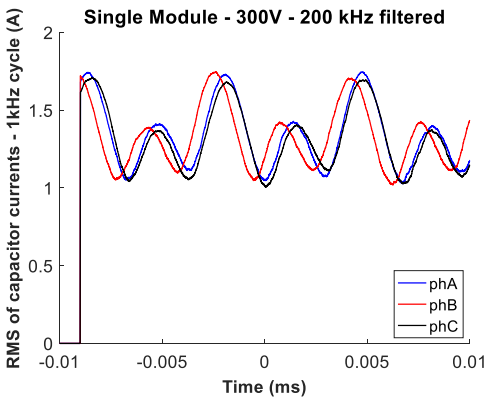

Single Module - 300V - 725 kHz filtered
Current (A)
Time (ms)
×10^-5
phA
phB
phC

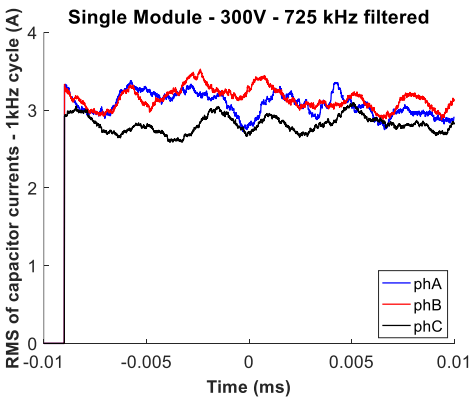

Single Module - 300V
Ripple currents of capacitors (A)
Time (ms)
725kHz filtered
200kHz filtered

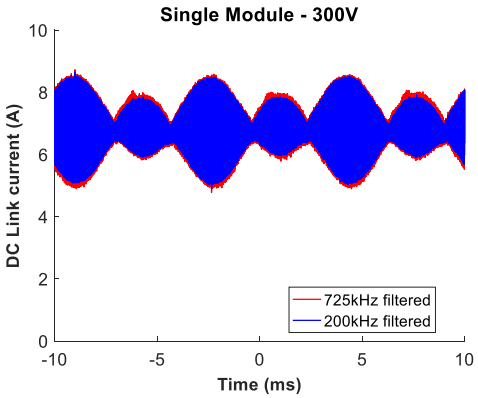

Single Module - 300V
Ripple currents of capacitors (A)
Time (ms)
725kHz filtered
200kHz filtered

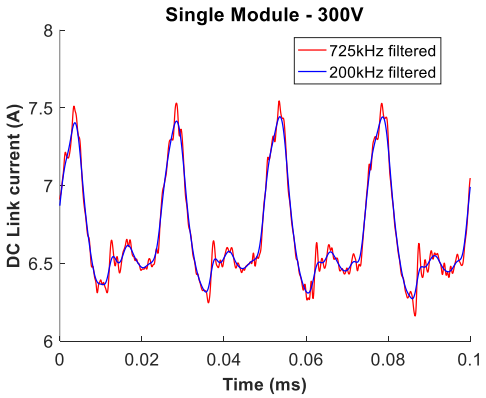

Single Module - 300V - 200 kHz filtered
RMS of capacitor currents - 40kHz cycle (A)
Time (ms)
phA
phB
phC


Single Module - 300V - 725 kHz filtered
RMS of capacitor currents - 40kHz cycle (A)
Time (ms)
phA
phB
phC


Single Module - 300V - 200 kHz filtered
RMS of capacitor currents - 1kHz cycle (A)
Time (ms)
phA
phB
phC

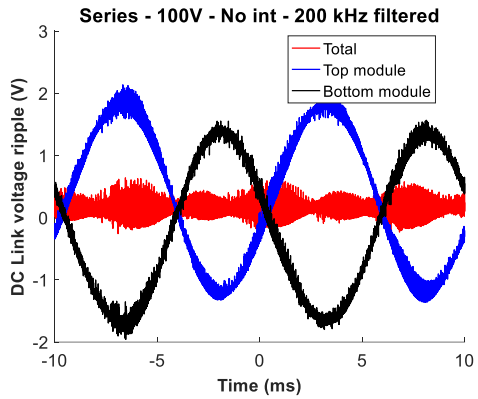

Single Module - 300V - 725 kHz filtered
RMS of capacitor currents - 1kHz cycle (A)
Time (ms)
phA
phB
phC

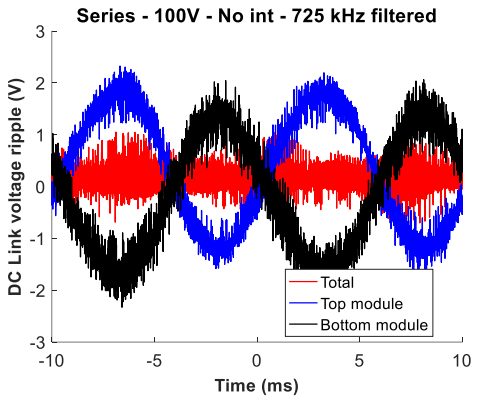

Single Module - 300V
DC Link current (A)
Time (ms)
725kHz filtered
200kHz filtered
10
8
6
4
2
0
-10
-5
0
5
10

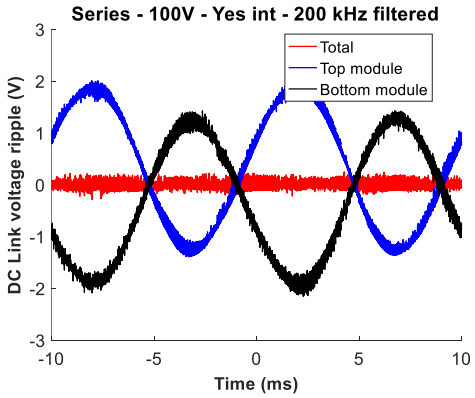

Single Module - 300V
DC Link current (A)
Time (ms)
725kHz filtered
200kHz filtered
8
7.5
7
6.5
6
0
0.02
0.04
0.06
0.08
0.1

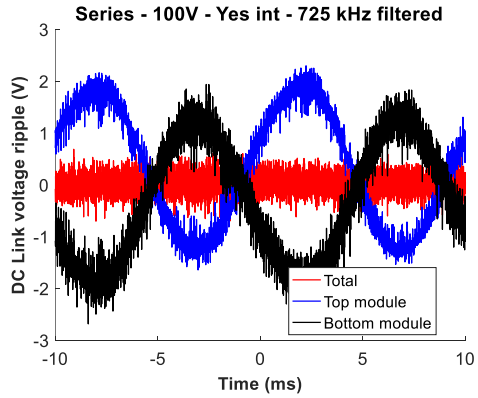
3. Series connected

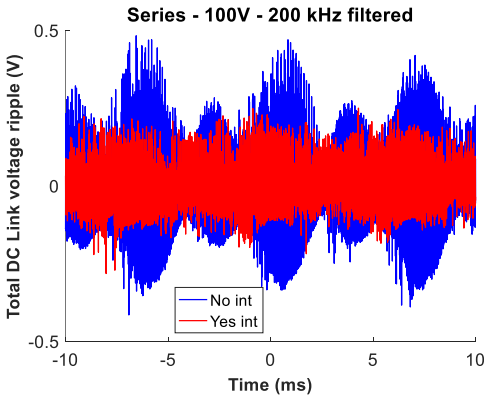
DC voltages are shared as 40V and 60V with 100V input voltage due to load unbalance.

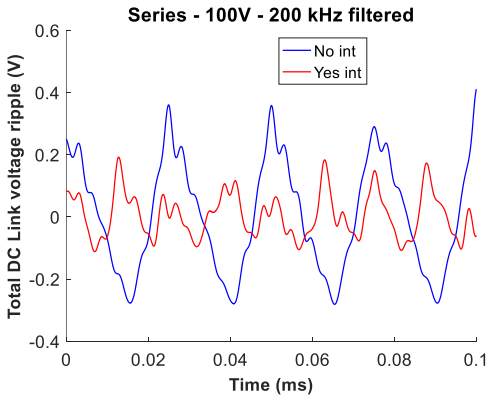


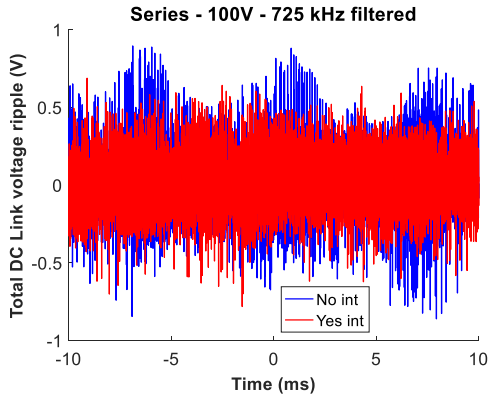


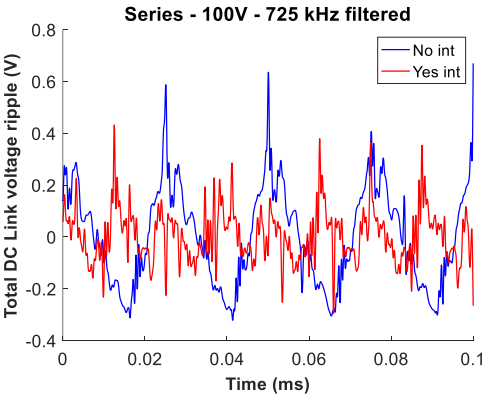












Although interleaving results are promising, there is an unexpected behaviour regardsless of interleaving such that, the module voltages have low frequency ripple which cancel out in total voltage. This was not observed in simulation. The reason may be due to rectifier.

For now, a 4 cycle (of 40 kHz) based avering is applied to observe the module voltage waveforms. The results are below: