AlGaN/GaN Metal-Insulator-Semiconductor (MIS)-HFETs Based DC-DC Boost Converters with Integrated Gate Drivers

Miao Cui[1,2], Qinglei Bu[1,2], Yutao Cai[1,2], Ruize Sun[3], Wen Liu[2], Huiqing Wen[2], Sang Lam[2], Yung. C. Liang[3], Ivona Z. Mitrovic[1], Stephen Taylor[1], Paul R. Chalker[4] and Cezhou Zhao[2*]

[1] Department of Electrical Engineering and Electronics, University of Liverpool, Liverpool, UK.
[2] Department of Electrical and Electronic Engineering, Xi'an Jiaotong-Liverpool University, Suzhou, China.
[3] Department of Electrical and Computer Engineering, National University of Singapore, Singapore.
[4] School of Engineering, Centre for Material and Structures, University of Liverpool, Liverpool, UK.
*E-mail : Cezhou.Zhao@xjtlu.edu.cn

***Abstract*-- This study proposed a 100 kHz, 5V/11V boost converter with an integrated gate driver for a power switching device using recessed E-mode MIS-HFETs. The integrated gate driver consisting of multi-stages DCFL (Direct-Coupled FET Logic) inverters and a buffer stage, has large input swing (up to 10 V) and wide noise margin with gate dielectric, which benefits applications requiring large gate swing without any additional drivers or level shifters. The impact of transistor size on rise times and fall times have been studied. Either buffer stage or larger width of DCFL inverter can reduce rise times from 2.4 μs to less than 0.5 μs at 100 kHz, so the output voltage of boost converter is increased by 10 % at a duty cycle of 0.7. However, large buffer width can result in high gate overshoot and oscillation, indicating careful design to balance switching speed and oscillation.**

***Index Terms*—AlGaN/GaN MIS-HFETs, integrated gate driver, DC-DC converters.**

I. Introduction

AlGaN/GaN heterojunction based power transistors have enabled a new generation of compact and highly efficient power electronics in many applications.[1] The monolithic integration of separate devices on a single chip is highly required to avoid parasitic inductances and capacitances, and to reduce the physical size of the circuit. For GaN based DC-DC converters, recent studies have been reported to monolithically integrate drivers with power transistors. A compact DC-DC buck converter (12-1.8 V) with integrated gate drivers was published in [2, 3], using p-AlGaN based normally-off gate injection transistors (GITs). Zhang. *et. al* [4] optimized integrated gate driver circuits for depletion mode GaN HEMTs on SiC substrate, and the DC-DC buck converter has an efficiency of over 90 % at 100 MHz. A quasi-normally-off push pull gate driver was integrated to drive a depletion GaN power transistor on Si substrate.[5] A gate current booster with a mesa resistor based inverter was applied to improve both fall times and rise times of a recessed enhancement mode (E-mode) MOS-HFET switching device.[6]

However, seldom reports show systematic studies of the impact of the integrated drivers on the performance of the DC-DC converters. In this work, we monolithically integrated gate driver using direct-coupled FET logic (DCFL) inverters [7-11]and a buffer stage [2, 12], with an E-mode MIS-HFET switching device for DC-DC boost converter. The E-mode switching device was formed by digital gate etching [13, 14], and 20 nm atomic layer deposition (ALD) Al_2O_3 gate insulator was used to enlarge gate swing with forward gate tolerance up to 10 V. The impact of device width on the driving capability of gate drivers have been carefully studied. Finally, a 100 kHz 5/11V boost converter with an optimized integrated gate driver was achieved at room temperature.

II. Experiments and Discussion

In this section, the monolithic fabrication process of E-mode MIS-HFETs and D-mode HEMTs is introduced in Part A, the electrical performance of discrete devices and the DCFL inverter are shown in Part B. Part C introduces four types of gate drivers, and results of boost converters with integrated drivers are summarized in Part D.

A. Fabrication Process

The AlGaN/GaN epitaxy used in this work consists of a 4.2 μm GaN buffer on a Si substrate, a 21 nm $Al_{0.25}Ga_{0.75}N$ barrier and 1 nm GaN cap layer. The Au-free source and drain ohmic contacts were formed by e-beam evaporation of Ti/Al/Ni/TiN (25/125/45/55 nm) metal stacks. Annealing at 800 °C for 45 s in N_2 ambient was then performed by rapid thermal anneal (RTA). Both D-mode MIS-HEMTs and E-mode MIS-HFETs were fabricated on the same substrate, with the structure shown in Fig. 1 (a). 150 nm plasma enhanced vapor deposition (PECVD) SiN_x was deposited as an etching hard mask for the E-mode gate etching. Digital etching using O_2 plasma treatment at the GaN surface for 3 minutes at 60 °C with a RF (radio frequency) power of 100 W was performed. Afterwards, the oxidation layer was removed by wet etching in 1:10 hydrochloric acid for 1 minute. After 40 cycles of digital etching, the full recess depth of around 22 nm was verified by atomic force microscopy (AFM) with a slow etch rate of about 0.6 nm per cycle, shown in Fig. 1 (b) and Fig. 1 (c). A 20 nm ALD Al_2O_3 gate dielectric for E/D-mode devices was deposited and Ni/TiN were finally evaporated as the gate metal.

For integrated drivers, additional PECVD SiN_x passivation and metal Al were deposited to connect

separate devices in GaN integrated circuits (ICs). All drivers, power transistor and separate E/D-mode devices (for I-V measurement) were fabricated on the same chip.

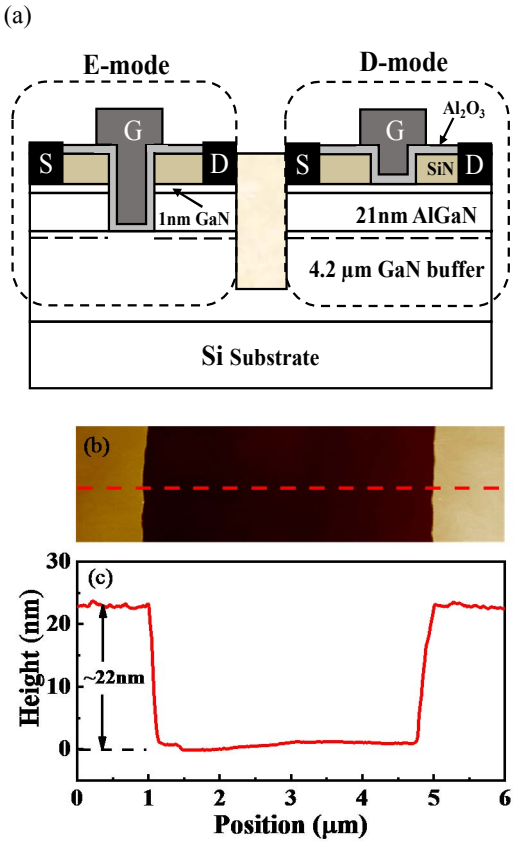
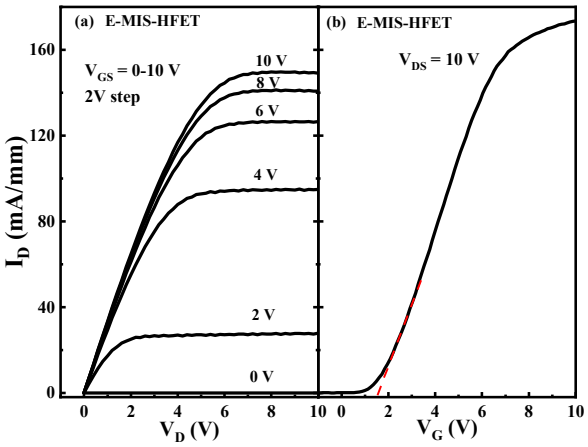


Fig.1 (a) Schematic diagram of E-mode MIS-HFETs and D-mode MIS-HEMTs. (b) Top view and (c) Cross section profile of gate trench in E-mode MIS-HFETs.

B. Device and Inverter Characteristics

The output and transfer characteristics of separate devices fabricated on the same chip with GaN gate drivers are shown in Fig. 2. The threshold voltage is + 1.5 V for E-mode devices and -8.5 V for D-mode devices as determined by extrapolation in the linear region. The gate voltage tolerance for E-mode MIS-HFETs is up to + 10 V, indicating large gate swing, and the large gate swing can benefit driver design without additional drivers or level shifters.



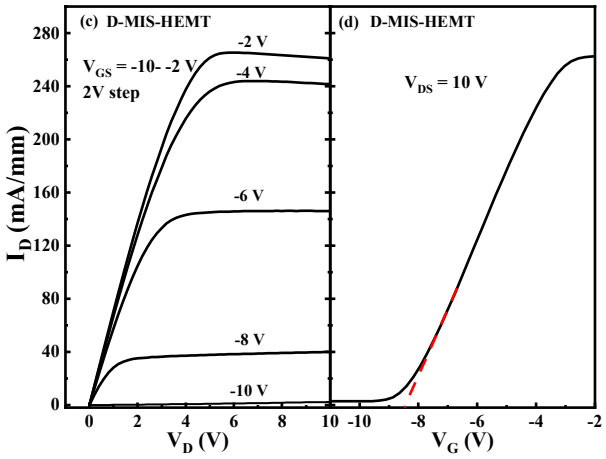
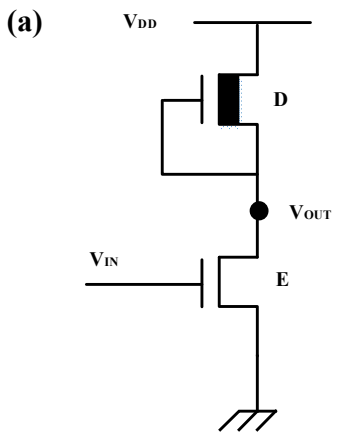


Fig. 2 Output and transfer characteristics of E-mode devices (a) and (b), D-mode devices (c) and (d), respectively. (Device dimension: $L_{GS}/W_G/L_G/L_{GD}$=5/100/3/10 μm).

Fig. 3 (a) shows the schematic circuit of a DCFL inverter, which is consisted of a D-mode MIS-HEMT (L_{GS} /W_G /L_G /L_{GD}=5/50/3/10 μm) and an E-mode MIS-HFET (L_{GS} /W_G /L_G/L_{GD}=5/2000/3/10μm). The static voltage transfer curve (VTC) is shown in Fig. 3 (b), the inverter exhibits a V_{th} of 4 V with a large input swing up to 10 V, which benefits applications requiring large gate swing without any additional drivers or level shifters. The output high (V_{OH}) and low (V_{OL}) of the DCFL inverter are 10 and 0.11 V, respectively, with an output swing of 9.89 V. The V_{IL} and V_{IH} are 3.33 and 4.61 V, and the noise margin NM_L and NM_H are 3.22 and 5.39 V, respectively, indicating a large noise margin. The dynamic performance of the DCFL inverter is shown in Fig. 3 (c) with a frequency of 100 kHz. Although the DCFL inverter can work with an input voltage up to 10 V, the integrated gate drivers can have large overshoot up to 15 V, which will increase leakage current of the inverter. In this work, the maximum gate voltage applied on the integrated gate drivers is chosen as 5 V in order to minimize the impact of leakage current on the performance of integrated drivers and converters.



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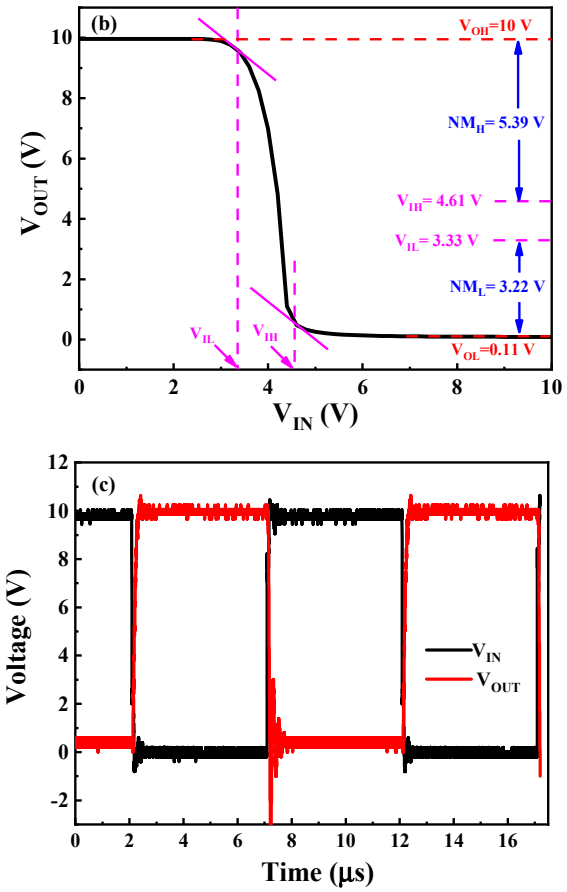

Fig. 3 (a) The circuit schematic of the DCFL inverter, (b) static voltage transfer curve, (c) dynamic waveform at 100 kHz. The applied voltage V_{DD}=10 V. (D-mode device: $L_{GS}/W_G/L_G/L_{GD}$=5/50/3/10µm, E-mode device: $L_{GS}/W_G/L_G/L_{GD}$=5/2000/3/10 µm).

C. *Integrated Gate Driver*

Table I shows four types of drivers fabricated on the same chip. They share the same gate length L_G=3 µm, gate to source distance L_{GS}=5 µm and gate to drain distance L_{GD}=10 µm, but have different numbers of stages, width of DCFL inverters and buffer stage.

TABLE I
A LIST OF FOUR TYPES OF INTEGRATED GATE DRIVERS

Type	No. 1	No. 2	No. 3	No. 4
D/E-mode width (DCFL inverter)	10/200 µm	50/2000 µm	10/200 µm	50/2000 µm
Number of inverter	2	2	3	3
Buffer width (E_{B1} and E_{B2})	No	No	500 µm	2000 µm

Fig. 4 (a) shows the circuit diagram of the gate driver, and Fig. 4 (b) shows the photograph of a typical driver No. 3. A DCFL inverter consists of a D-mode active resistor with source-drain connected and an E-mode device. The buffer stage consists of two E-mode devices E_{B1} and E_{B2}. The results of different drivers are shown in Fig. 4 (c), all drivers have comparable driving capability in terms of rise and off times (< 0.5 µs) at 100 kHz, except driver No. 1, which has a large rise time of 2.4 µs and a relatively small fall time (< 0.5 µs). The large rise time of No. 1 may be attributed to the small D-mode width of 10 µm, this is because according to Fig 4. (d), the rise times of single-stage inverters with the same D-mode width as No. 1 are almost unchanged for different E-mode widths ranged from 100 µm to 500 µm, this indicates the rise time of DCFL inverter is independent on the width of E-mode device and only related to the width of D-mode device. The increase of the top D-mode width of DCFL inverter will cause a decrease in the rise time. This could also be confirmed by driver No. 2 (width= 50 µm), which shows a reduced rise time compared with driver No. 1. Additionally, the fall time is independent on the gate width for all drivers as shown in Fig. 4 (a) regardless of big width differences among all drivers.

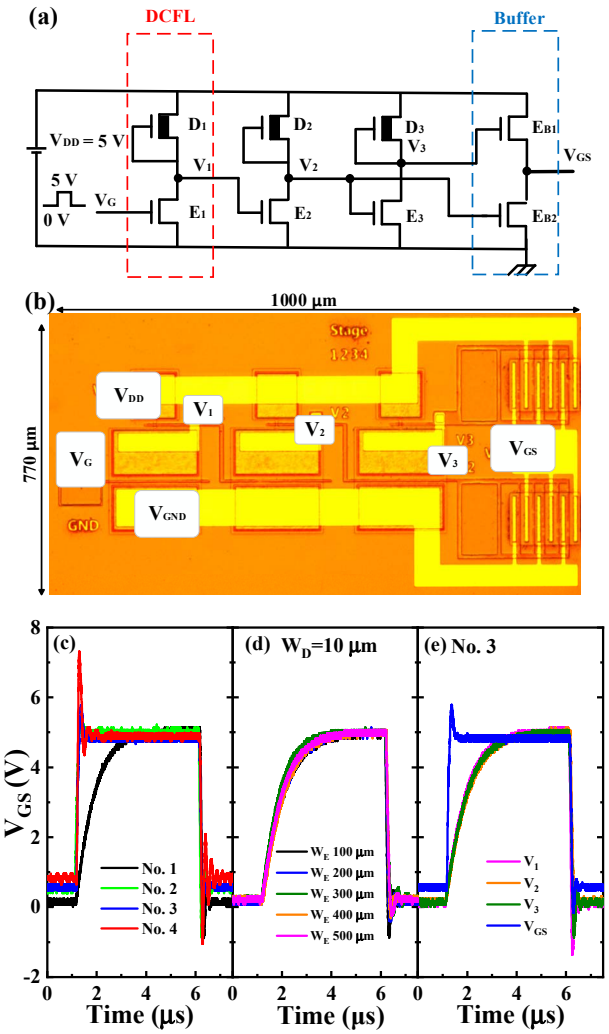

Fig. 4 (a) Circuit diagram of gate driver and (b) a photograph of gate driver No. 3. (c) Dynamic V_{GS} waveforms of four drivers. (d) Output waveforms with different E-mode width of discrete single-stage inverters fabricated on the same chip (width of D-mode: W_D=10 µm). (e) Voltage waveform at each stage of driver No. 3. V_{DD}=$V_{G,\,max}$=5 V, 100 kHz.

The rise time of driver No. 3 (same D-mode width as No. 1) can also be greatly reduced from 2.4 μs (V_1, V_2 and V_3) to < 0.5 μs (V_4) with a buffer stage (width = 500 μm), shown in Fig. 4 (e). In the meantime, No. 3 exhibits low gate overshoot. A larger buffer width of driver No. 4 (width = 2000 μm) have large gate charging current, and this could consequently decrease the rise time. However, a very large gate voltage overshoot (peak voltage +7.4 V) and an obviously increased oscillation during turn-on and turn-off transition are observed in Fig. 4 (c) (red line). Unfortunately, the gate voltage overshoot will seriously damage or breakdown the power transistor, especially for low gate voltage tolerance transistors, such as HEMTs or P-GaN HEMTs, whose $V_{G,\,max}$ are usually less than 7 V.[15] GaN based MIS-HFETs are capable to increase the gate overshoot tolerance due to the insertion of gate dielectric, which can increase gate swing. Hence, the balance between switching speed and oscillation requires careful consideration during the design process of the driver.

Fig. 5 (a) shows the circuit diagram of soft switching test, using No. 3 to driver a 2000 μm E-mode device E, which was connected in series with a load resistor R_D. The dynamic waveforms with different load resistors are shown in Fig. 5 (b) at 400 kHz. The driver can work normally at 400 kHz, indicating good driving capability with a buffer stage at high frequency. Moreover, the rise times of the output are increasing with increasing load resistance, due to the reduced charging current with a large load resistance. This coincides with the large rise time of No. 1 (small width or large resistance of D-mode active resistor) in Fig. 4 (c).

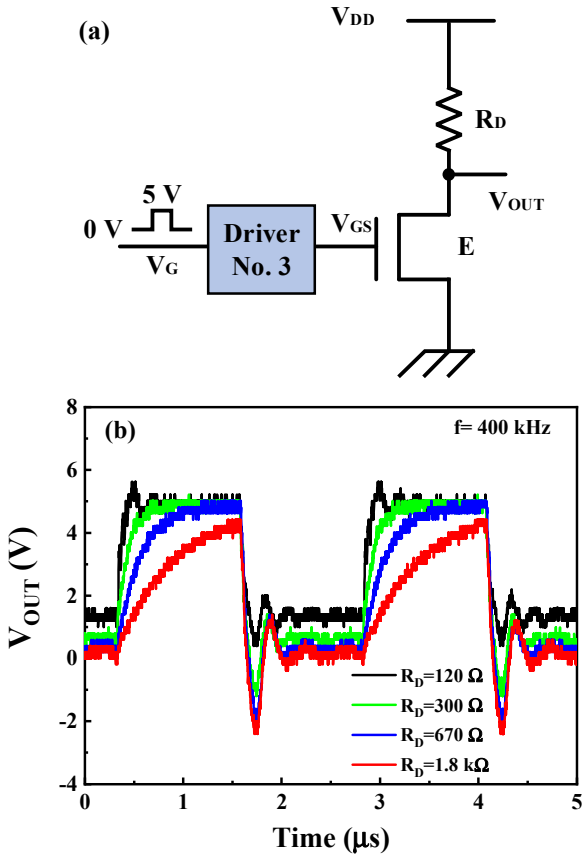

Fig. 5 (a) Circuit diagram of the switching test using No. 3 to drive a 2000 μm E-mode device E with a resistor load R_D. (b) Dynamic output waveforms with different load resistors of 120, 300, 670 Ω and 1.8 kΩ at 400 kHz.

D. Boost Converter Results

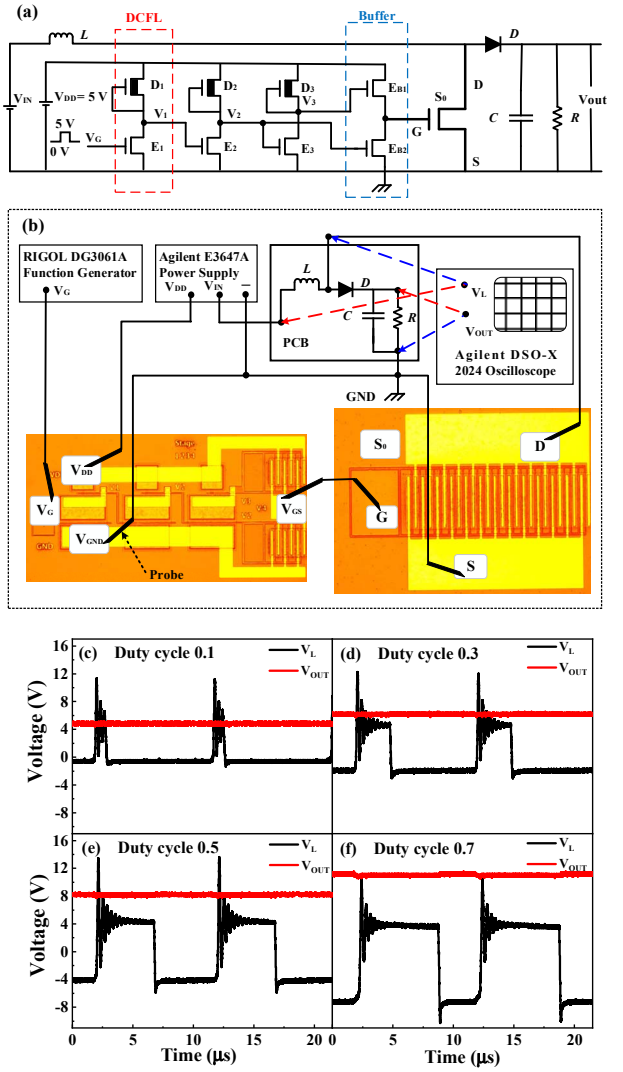

Fig. 6 (a) Circuit diagram of the boost converter. (b) The experiment set up of the boost converter with integrated gate driver No. 3 and a switching transistor S_0. (L=1 mH, the threshold voltage for discrete diode D is + 0.7 V, C=10 μF, R=500 Ω, V_{IN}=V_{DD}=5V, f=100 kHz). Waveforms of the boost converter with integrated gate driver No. 3 at various duty cycles (c) 0.1, (d) 0.3, (e) 0.5 and (f) 0.7. (V_L is the voltage drop of the inductance L).

Fig. 6 (a) shows the circuit diagram of the boost converter, with an integrated power transistor S_0 and the gate driver No. 3. The gate driver and transistor S_0 were fabricated on the same chip, but here we separates them in the circuit in order to distinguish two parts. The transistor S_0 is an E-mode MIS-HFET with a width of 5 mm. Fig. 6 (b) shows the experiment set up for the boost converter, the inductor L, discrete diode D, capacitor C and load resistor R were externally integrated on a PCB board, the gate driver and transistor S_0 were externally connected

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with other components using probes, and the negative electrodes of power supply should be connected to the common ground GND. Differential voltage probes were used to detect the dynamic inductance and output voltages shown in an oscilloscope. The output converter and inductance voltages of driver No. 3 are shown in Fig. 6 (c)-(f), with duty cycles of 0.1, 0.3, 0.5 and 0.7, respectively. The output voltage V_{OUT} is increasing with increasing duty cycles as expected.

The boost converter results (with four different gate drivers) are shown in Fig. 7. The calculated values are also plotted in the figure for comparison. Driver No. 1 shows overall lowest output voltages among all the drivers due to reduced duty cycles caused by large rise time in Fig. 4 (c). For other three drivers, experimental results are comparable with calculated values at lower duty cycles (D= 0.1 and 0.3), but smaller than calculated values at higher duty cycles (D= 0.5 and 0.7), and the discrepancies between them increase with increasing duty cycles, which might be caused by dynamic R_{on} (on-state resistance) or current collapse at large current. The boost converter of driver No. 3, with a low rise/fall time and small gate overshoot/oscillation, features a 5 V/11 V conversion at 100 kHz, the converter output at duty cycle 0.7 is increased by 10% compared with driver No. 1.

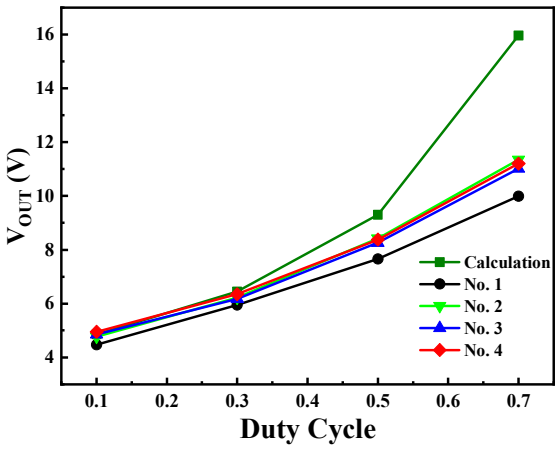

Fig. 7 Output voltages of four drivers and calculated values at various duty cycles.

III. Conclusions

An Integrated gate driver with an E-mode MIS-HFET based power device is proposed and investigated in GaN based DC-DC boost converters. The proposed gates driver with DCFL inverters and a buffer amplifier has large gate swing without any additional drivers or level shifters. The impact of inverter size and buffer stage width on driving capability are studied. A large D-mode width of the DCFL inverter or a buffer amplifier can improve reduce rise times or switching-on times. However, a large buffer width can result in high gate overshoot and oscillation, indicating careful gate driver design should be made to balance switching speed and oscillation.

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