Evaluation of Possible Traction Inverter Topologies for Heavy-Duty Electric Vehicles

ABSTRACT

This paper evaluates traction inverters for heavy-duty electric vehicles, focusing on key criteria such as raised power ratings with improved efficiency and power densities. Boosted voltage and current levels are required to achieve higher power levels and provide megawatt charging system solutions, which results in the need to utilize new semiconductors and topologies. In this study, 3-Level neutral point clamped (3L-NPC) and 2-Level 6-phase (2L-6Ph) voltage source inverters (VSIs) are evaluated and compared to conventional 2-Level 3-phase (2L-3Ph). The comparison uses figure-of-merit parameters and a virtual prototyping method based on several performance indices, such as efficiency, power density, output harmonic quality, and reliability. Then, efficiency maps are acquired to find out the sweet operating points, minimizing losses. Results show that the 3L-NPC VSI system provides a higher switching frequency, which also shrinks the size of the passive elements and cooling system. Although the 3L-NPC inverter requires additional power switches and isolated gate drivers, its estimated performance outweighs such reliability and cost-dependent issues. Therefore, this study concludes that multi-level inverter topologies hold promise for high-voltage, high-power traction drives.

INTRODUCTION

The interest in electrifying heavy-duty vehicles is continuously increasing due to the growing need for sustainable transportation to mitigate environmental issues [**1**]. One critical part of achieving this sustainable transportation is to improve the traction inverter, which transfers energy from the battery to the electric machine [**2**]. Until recently, the traction inverters have mainly utilized a 2-level, 3-phase voltage source inverter (2L-3Ph-VSI) with Si-based insulated-gate-bipolar transistors (Si-IGBTs) due to their cost-effectiveness, technology maturity, and ease of control [**3**]. However, new trends for various topologies with distinct power semiconductors have emerged since heavy-duty vehicles require new key features, such as increased power ratings, improved efficiencies, and enhanced power densities [**4**].

With the recent advancements in technology, there is a growing trend towards increasing the DC-link voltages to 1000 V and beyond. The motivation behind this shift is primarily driven by the desire to enhance the power density of propulsion systems [**5**]. Also, higher DC-link voltages enable megawatt charging, which, in turn, reduces charging time and cable weights [**6**]. Furthermore, assuming keeping the inverter power rating constant, higher DC-link voltages lead to lower current ratings, reducing the inverter's conduction losses. Additionally, to increase the power ratings of traction systems to several hundred kilowatts, it is imperative to consider augmenting the current rating of the traction inverter. Further, passing to wide bandgap semiconductors such as SiC MOSFETs instead of Si-IGBTs enhances efficiency since SiC MOSFETs have superior properties,

including wider bandgap width that permits operation at high voltages, higher saturation velocity that enables high-frequency switching, and higher thermal conductivity that facilitates high-temperature operation [**7**]. Thereby, alternative topologies that utilize SiC MOSFETs hold a huge potential to replace the existing topologies. Numerous topologies have been proposed in the literature to enhance the performance of traction inverters. For instance, a 4-leg/2-level inverter has been studied to reduce the common mode voltage (CMV) and prevent bearing failure. However, such topologies are raising system losses and costs due to the additional power switches [**2**]. Accordingly, focusing on multi-level and multi-phase inverters to achieve high-power and efficient inverters for heavy-duty vehicles seems more fruitful.

Multi-level inverters (MLIs) such as the 3-level neutral point clamped (3L-NPC) have gained significant attention due to their numerous benefits. They can utilize higher DC-link voltage by implementing compatible power devices with lower voltage ratings, thereby reducing the overall cost of the inverter system [**5**]. These power devices with lower voltage ratings deliver lower on-state resistance and higher switching frequencies, shrinking the system's losses and passive components. In addition, they provide better harmonic quality at the differential output, which reduces the additional harmonic losses of the motor. Moreover, the DC-link capacitance requirement is diminished while increasing the level of the inverters, lessening the total volume of the inverter.

Multi-phase inverters (MPIs), such as 2-level 6-phase (2L-6Ph) VSIs, have been gaining popularity due to their capability to enhance the total power handling capability [**8**]. Increasing the phase number reduces the need for DC-link capacitance, thereby minimizing the volume and cost of the system [**9**]. Additionally, using MPIs provides a modular system, which provides fault tolerance and so improves reliability [**10**].

The rest of the article is organized as follows ... (to be continued in the final version)

System Specifications and Requirements

Table I shows system specifications for heavy-duty vehicles at the present application. Selecting an appropriate DC-link voltage is critical to ensure efficient and reliable megawatt charging; hence, a voltage of 1250 V has been chosen. The system's power rating is determined by the vehicle dynamics, which encompasses the load of heavy-duty vehicles and has been calculated as 300 kW. Regarding traction machines, two options are available: 3-phase and 6-phase. Both options use the same phase voltages; however, the phase current for the 6-phase traction system is halved to maintain the same power rating.

TABLE I: System Specifications and Requirements

Parameter	Value	**KPIs**
Power Rating	$300\ kW$	Efficiency
Input Voltage $\mathrm{V_{in}}$	$1250\ V$	Power density
Input Current $\mathrm{I_{in}}$	$240\ A$	Output harmonics
Phase Voltage $\mathrm{V_{pn}}$	$625\ V$	Reliability
Power Factor $\mathrm{p_f}$	0.9	
Phase Current $\mathrm{I_p}$	$356\ A$ and $178\ A$	
Switching Frequency $\mathrm{f_s}$	$10-25\ kHz$	

In order to compare the evaluated topologies, there are several key performance indices (KPIs) listed in Table I. The circuit diagrams of these topologies are illustrated in Fig. 1.

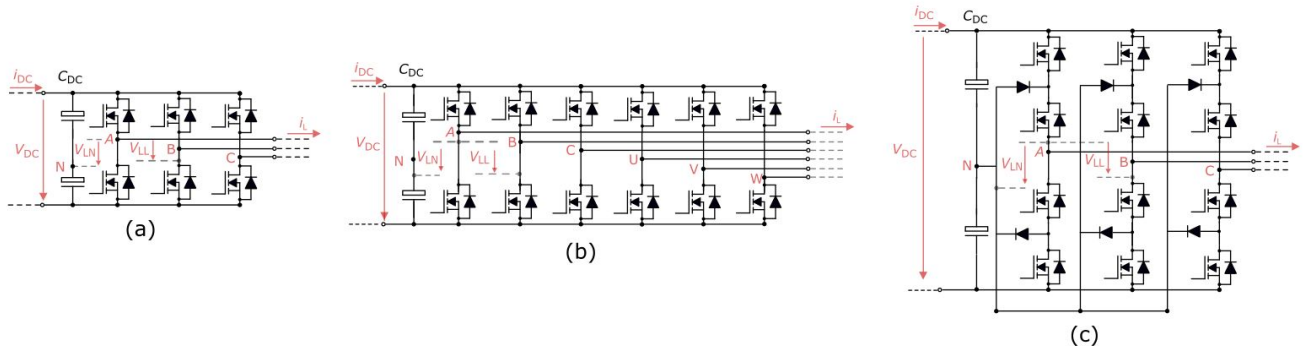


Fig. 1: The evaluated inverter topologies. a) 2L-3Ph-VSI. b) 3L-NPC-VSI. c)2L-6Ph-VSI.

The Virtual Prototyping Method

This section presents a system modeling methodology utilizing Figure-of-Merit (FOM) parameters. The modeling includes semiconductor loss calculation, cooling system size estimation, DC-link capacitance requirement estimation, and output harmonic calculation. This approach offers a comprehensive and accurate system-level understanding of the performance characteristics of high-power traction inverters.

A. Semiconductor Loss Modelling with Figure-of-Merits

The semiconductor losses are divided into two main parts: conduction and switching losses. The conduction loss for a single switch can be calculated as given by

$$P_c = \frac{1}{2\pi} \int_{\theta_{C1}}^{\theta_{C2}} r_{ds} \cdot i_{ds}(\theta)^2 \cdot D(\theta)\, d\theta \tag{1}$$

where duty cycles ($D(\theta)$), switch current ($i_{ds}(\theta)$), conduction angles (θ_{C1} to θ_{C2}), and on-state resistance (r_{ds}) are required. The on-state resistance depends on the voltage rating (U_B) and die area (A_{die}) that can be roughly calculated as given by

$$r_{ds} = \frac{k_R \cdot U_B^{\alpha_r}}{A_{die}} \tag{2}$$

where k_r and α_r are technology dependent coefficients. While calculating conduction losses, the effect of the body diode can be ignored in the reverse conduction of MOSFETs and during dead times. Ignoring the body diode leads to overestimating the loss during the reverse conduction and underestimating the loss during the dead times [**11**]. Therefore, these assumptions partly compensate for each other.

The switching loss comprises two main components: zero current switching loss and overlapping loss [**12**]. The zero current switching energy is reliant on the output capacitance ($C_{oss,Q}$) and switching voltage (U_{dc}); however, the overlapping energy is proportionate to $\frac{dV}{dt}$ and $\frac{di}{dt}$. Firstly, the zero current switching energy can be estimated using the FOM of SiC devices as given by

$$E_{sw-ZCS} = C_{oss,Q}(U_{dc}) \cdot U_{dc}^{\alpha_c} = k_c \cdot U_b^{\alpha_c} A_{die} \cdot U_{dc}^2 \tag{3}$$

Secondly, the overlapping switching energy can be calculated as given by

$$E_{sw-overlapping} = (\frac{V_{dc} \cdot I_{sw}^2}{2 \cdot \frac{di}{dt_{on}}} + \frac{V_{dc}^2 \cdot I_{sw}}{2 \cdot \frac{dv}{dt_{on}}}) + (\frac{V_{dc} \cdot I_{sw}^2}{2 \cdot \frac{di}{dt_{off}}} + \frac{V_{dc}^2 \cdot I_{sw}}{2 \cdot \frac{dv}{dt_{off}}}) \tag{4}$$

where $\frac{dV}{dt}$ and $\frac{di}{dt}$ should be selected regarding layout parasitics, gate driver and isolation requirements of the motor. Finally, the total switching losses can be calculated by using

$$P_{sw} = \frac{f_{sw}}{2\pi} \int_{\theta_{SW1}}^{\theta_{SW2}} (E_{sw-overlapping}(\theta) + E_{sw-ZCS}(\theta))\, d\theta \tag{5}$$

during a switching angle (θ_{SW1} to θ_{SW2}). It will continue in the final paper.

B. The Selection of Switch Ratings

Selecting the voltage rating of a switch has a noteworthy impact on the design stage of the traction inverter. It is often selected higher than the blocking voltage with a safety factor to account for voltage overshoots caused by high switching speeds and layout parasitics and the effect of cosmic rays on reliability [**13**]. In our system, the safety factor of 1.36 is selected, leading to the switches' voltage ratings of 1700 V for 2-level topologies and 850 V for 3-level topologies. Furthermore, the optimal die area or current rating of the switch plays a critical role in the efficiency performance of the inverter. The appropriate die area depends on the switching frequency and the voltage change rate ($\frac{dv}{dt}$), as illustrated in Fig. 2. The die area will be chosen in the next section by comparing the switching frequency and $\frac{dv}{dt}$.

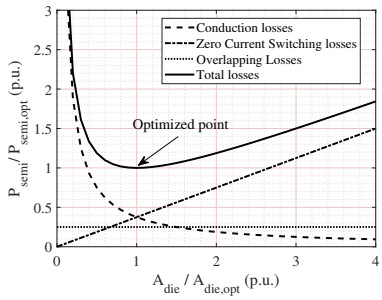


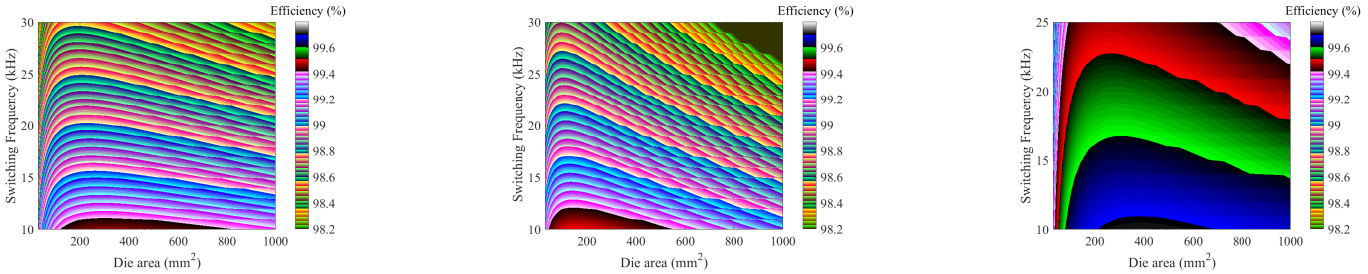
Fig. 2: Total switch losses for varying die area at a specific switching frequency and $\frac{dV}{dt}$.

C. Other Subsections

Implementation of the Loss Modelling Algorithm in Different Topologies. Cooling System Size Estimation, DC-link Capacitance Requirements, and Output Harmonics will be added in the final version.

Results of the Virtual Prototyping Method

The efficiency assessment of various topologies has been carried out through a comprehensive sweep of die area and switching frequency to identify an optimal operation point that minimizes inverter losses. As illustrated in Fig. 3, this process has resulted in a set of efficiencies and an operation point is selected for all topologies at 99.4 percent efficiency. Other results and comparisons will be added in the full paper.



(a) 2-Level 3-Phase VSI. (b) 2-Level 6-Phase VSI. (c) 3-Level NPC VSI.

Fig. 3: The efficiency over varying die area and switching frequency (The conduction losses are scaled by 1.5 to consider the junction temperature at 100 ^oC.).

CONCLUSIONS AND FUTURE WORK

To be added in the final version.

References

[1] C. H. T. Lee, W. Hua, T. Long, C. Jiang and L. V. Iyer, "A Critical Review of Emerging Technologies for Electric and Hybrid Vehicles," in IEEE Open Journal of Vehicular Technology, vol. 2, pp. 471-485, 2021, doi: 10.1109/OJVT.2021.3138894.

[2] J. Reimers, L. Dorn-Gomba, C. Mak and A. Emadi, "Automotive Traction Inverters: Current Status and Future Trends," in IEEE Transactions on Vehicular Technology, vol. 68, no. 4, pp. 3337-3350, April 2019, doi: 10.1109/TVT.2019.2897899.

[3] I. Husain et al., "Electric Drive Technology Trends, Challenges, and Opportunities for Future Electric Vehicles," in Proceedings of the IEEE, vol. 109, no. 6, pp. 1039-1059, June 2021, doi: 10.1109/JPROC.2020.3046112.

[4] B. Fahimi et al., "Automotive Electric Propulsion Systems: A Technology Outlook," in IEEE Transactions on Transportation Electrification, doi: 10.1109/TTE.2023.3321707.

[5] Mohammad M. Qasim, David M. Otten, Zoltán S. Spakovszky, Jeffrey H. Lang, James L. Kirtley and David J. Perreault. "Design and Optimization of an Inverter for a One-Megawatt Ultra-Light Motor Drive," AIAA 2023-4161. AIAA AVIATION 2023 Forum. June 2023.

[6] A. Poorfakhraei, M. Narimani and A. Emadi, "A Review of Multilevel Inverter Topologies in Electric Vehicles: Current Status and Future Trends," in IEEE Open Journal of Power Electronics, vol. 2, pp. 155-170, 2021, doi: 10.1109/OJPEL.2021.3063550.

[7] Fatahilah, Muhammad Fahlesa et al. "3D GaN nanoarchitecture for field-effect transistors." Micro and Nano Engineering (2019): n. pag.

[8] W. Taha, P. Azer, A. D. Callegaro and A. Emadi, "Multiphase Traction Inverters: State-of-the-Art Review and Future Trends," in IEEE Access, vol. 10, pp. 4580-4599, 2022, doi: 10.1109/ACCESS.2022.3141542.

[9] L. Jin, S. Norrga, O. Wallmark and N. Apostolopoulos, "Modulation and Power Losses of a Stacked Polyphase Bridge Converter," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 1, pp. 409-418, March 2017, doi: 10.1109/JESTPE.2016.2621349.

[10] M. Ugur and O. Keysan, "Design of a GaN Based Integrated Modular Motor Drive," 2018 XIII International Conference on Electrical Machines (ICEM), Alexandroupoli, Greece, 2018, pp. 1471-1477, doi: 10.1109/ICELMACH.2018.8506862.

[11] J. Ebersberger, M. Hagedorn, M. Lorenz and A. Mertens, "Potentials and Comparison of Inverter Topologies for Future All-Electric Aircraft Propulsion," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 10, no. 5, pp. 5264-5279, Oct. 2022, doi: 10.1109/JESTPE.2022.3164804.

[12] J. Azurza Anderson, G. Zulauf, J. W. Kolar and G. Deboy, "New Figure-of-Merit Combining Semiconductor and Multi-Level Converter Properties," in IEEE Open Journal of Power Electronics, vol. 1, pp. 322-338, 2020, doi: 10.1109/OJPEL.2020.3018220.

[13] Z. Gao, J. Zhang, Y. Huang, R. Guan and Y. Zhou, "A Closed-Loop Active Gate Driver of SiC MOSFET for Voltage Spike Suppression," in IEEE Open Journal of Power Electronics, vol. 3, pp. 723-730, 2022, doi: 10.1109/OJPEL.2022.3209334.

[14] Z. Wang, Y. Wu, M. H. Mahmud, Z. Zhao, Y. Zhao and H. A. Mantooth, "Design and Validation of A 250-kW All-Silicon Carbide High-Density Three-Level T-Type Inverter," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 578-588, March 2020, doi: 10.1109/JESTPE.2019.2951625.

[15] H. Zhang et al., "Design and Evaluation of a 1200-V/200-A SiC Three-Level NPC Power Module," in IEEE Transactions on Industry Applications, vol. 59, no. 5, pp. 6412-6426, Sept.-Oct. 2023, doi: 10.1109/TIA.2023.3288500.