Evaluation of Possible Traction Inverter Topologies for Heavy-Duty Electric Vehicles

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***Abstract*—This paper evaluates traction inverters for heavy-duty electric vehicles, focusing on key criteria such as raised power ratings with improved efficiency and power densities. Boosted voltage and current levels are required to achieve higher power levels and provide megawatt charging system solutions, which results in the need to utilize new semiconductors and topologies. In this study, 3-Level neutral point clamped (3L-NPC) and 2-Level 6-phase (2L-6Ph) voltage source inverters (VSIs) are evaluated and compared with conventional 2-Level 3-phase VSIs' (2L-3Ph-VSIs) topology. The comparison uses figure-of-merit parameters and a virtual prototyping method based on several performance indices, such as efficiency, power density, output harmonic quality, and reliability. Then, efficiency maps are acquired to find out the sweet operating points, minimizing losses. Results show that the 3L-NPC VSI system provides a higher switching frequency, which also shrinks the size of the passive elements and cooling system. Although 3L-NPC requires additional power switches and isolated gate drivers, its promised performance outweighs such reliability and cost-dependent issues. Therefore, this study concludes that multi-level inverter topologies hold promise for high-voltage, high-power traction drives.**

***Index Terms*—traction inverter, switching losses, conduction losses, 3 level neutral point clamped inverter**

I. Introduction

The interest in electrifying heavy-duty vehicles is continuously increasing due to the growing need for sustainable transportation to mitigate environmental issues [1]. One critical part of achieving this sustainable transportation is to improve the traction inverter, which transfers energy from the battery to the electric machine [2]. Until recently, the traction inverters have mainly utilized a 2-level, 3-phase voltage source inverter (2L-3Ph-VSI) with Si-based insulated-gate-bipolar transistors (Si-IGBTs) due to their cost-effectiveness, technology maturity, and ease of control [3]. However, new trends for various topologies with distinct power semiconductors have emerged since heavy-duty vehicles require new key criteria, such as increased power ratings, improved efficiencies, and enhanced power densities [4].

With the recent advancements in technology, there is a growing trend towards increasing the DC-link voltages to 1000 V and beyond. The motivation behind this shift is primarily driven by the desire to enhance the power density of propulsion systems [5]. Also, higher DC-link voltages enable megawatt charging, which, in turn, reduces charging time and cable weights [6]. Furthermore, assuming keeping the inverter power rating constant, higher DC-link voltages lead to lower current ratings, reducing the inverter's conduction losses. Parallelly, regarding increasing the power ratings of traction systems to several hundred kilowatts, it is imperative to consider augmenting the current rating of the traction inverter. Further, passing to wide bandgap semiconductors such as SiC MOSFETs instead of Si-IGBTs enhances efficiency since SiC MOSFETs have superior properties, including wider bandgap width that permits operation at high voltages, higher saturation velocity that enables high-frequency switching, and higher thermal conductivity that facilitates high-temperature operation [7]. Thereby, alternative topologies that utilize SiC MOSFETs hold a huge potential to replace the existing topologies. Numerous topologies have been proposed in the literature to enhance the performance of traction inverters. For instance, a 4-leg/2-level inverter has been studied to reduce the common mode voltage (CMV) and prevent bearing failure. However, such topologies are raising system losses and costs due to the additional power switches [2]. Accordingly, focusing on multi-level and multi-phase inverters to achieve high-power and efficient inverters for heavy-duty vehicles seems more reasonable.

Multi-level inverters (MLIs) such as the 3-level neutral point clamped (3L-NPC) have gained significant attention due to their numerous benefits. They can utilize higher DC-link voltage by implementing compatible power devices with lower voltage ratings, thereby reducing the overall cost of the inverter system [5]. These power devices with lower voltage ratings deliver higher switching frequencies and thus shrink the

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system's passive components. In addition, they provide better harmonic quality at the differential output, which reduces the additional harmonic losses of the motor. Moreover, the DC-link capacitance requirement is diminished while increasing the level of the inverters, lessening the total volume of the inverter.

Multi-phase inverters (MPIs), such as 2-level 6-phase (2L-6Ph) VSIs, have been gaining popularity due to their capability to enhance the total power handling capability [8]. Expanding the phase number reduces the need for DC-link capacitance, thereby minimizing the volume and cost of the system [9]. Additionally, using MPIs provides a modular system, which provides fault tolerance and so improves reliability [10].

The rest of the article is organized as follows. Section II presents the system specification and explains the requirements that must be fulfilled. Section III proposed a virtual prototyping method to evaluate the semiconductor losses, estimate the DC-link capacitance, and size the cooling system. Section IV reveals the analytical results of the evaluated topologies and presents a comparative analysis of the findings. Section VII draws a conclusion by demonstrating the inverter's trend in achieving high voltage and power.

II. System Specifications and Requirements

Table I shows system specifications for heavy-duty vehicles at the present application. Selecting an appropriate DC-link voltage is critical to ensure efficient and reliable megawatt charging; hence, a voltage of 1250 V has been chosen. The system's power rating is determined by the vehicle dynamics, which encompasses the load of heavy-duty vehicles and has been calculated as 300 kW. Regarding traction machines, two options are available: 3-phase and 6-phase. Both options use the same phase voltages; however, the phase current for the 6-phase traction system is halved to maintain the same power rating.

TABLE I: System Specifications and Requirements

Parameter	Value
Power Rating	300 kW
Input Voltage $\mathrm{V_{in}}$	1250 V
Input Current $\mathrm{I_{in}}$	240 A
Phase Voltage $\mathrm{V_{pn}}$	625 V
Power Factor $\mathrm{p_f}$	0.9
Phase Current $\mathrm{I_p}$	356 A and 178 A
Switching Frequency $\mathrm{f_s}$	$10-25$ kHz

KPIs
Efficiency
Power density
Output harmonics
Reliability

On the side of these specifications, several key performance indices (KPIs), as shown in Table I, exist to compare the evaluated topologies, the circuit diagrams of which are illustrated in Fig. 1.

III. The Virtual Prototyping Method

This section presents a system modeling methodology utilizing Figure-of-Merit (FOM) parameters. The modeling includes

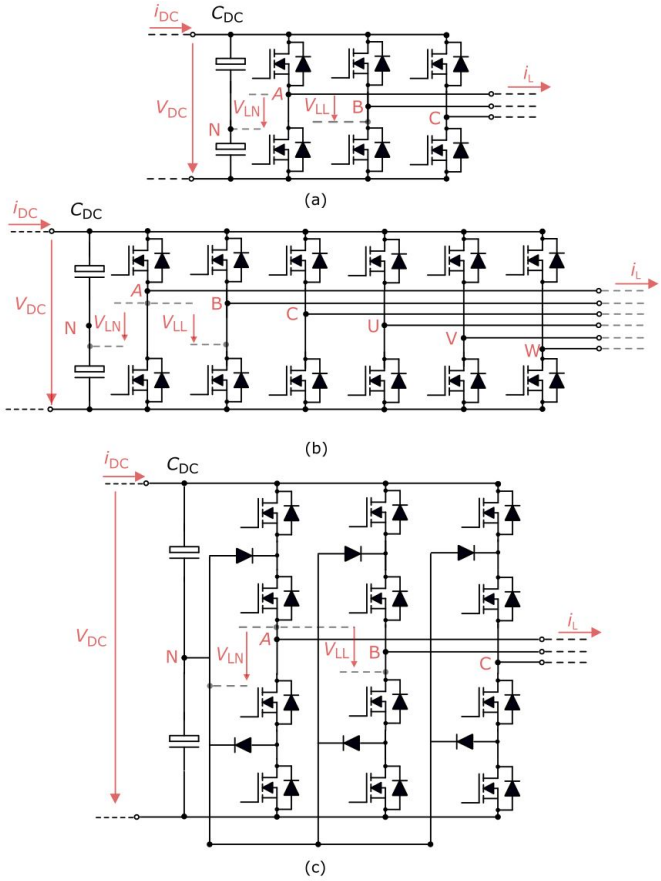


Fig. 1: The evaluated inverter topologies. a) 2L-3Ph-VSI. b) 3L-NPC-VSI. c)2L-6Ph-VSI.

semiconductor loss calculation, cooling system size estimation, DC-link capacitance requirement estimation, and output harmonic calculation. This approach offers a comprehensive and accurate system-level understanding of the performance characteristics of high-power traction inverters.

A. Semiconductor Loss Modelling with Figure-of-Merits

The semiconductor losses are divided into two main parts: conduction and switching losses. The conduction loss for a single switch can be calculated as given in (1) where duty cycles ($D(\theta)$), switch current ($i_{ds}(\theta)$), conduction angles (θ_{C1} to θ_{C2}), and on-state resistance (r_{ds}) are required.

$$P_c = \frac{1}{2\pi}\int_{\theta_{C1}}^{\theta_{C2}} r_{ds}\cdot i_{ds}(\theta)^2\cdot D(\theta)\,d\theta \tag{1}$$

On-state resistance depends on the voltage rating (U_B) and die area (A_{die}) that can be roughly calculated as given in (2) where k_r and α_r are technology dependent coefficients.

$$r_{ds} = \frac{k_R\cdot U_B^{\alpha_r}}{A_{die}} \tag{2}$$

While calculating conduction losses, the effect of the body diode can be ignored in the reverse conduction of MOSFETs and during dead times. Ignoring the body diode leads to

overestimating the loss during the reverse conduction and underestimating the loss during the dead times [11]. Therefore, these assumptions compensate for each other.

The switching loss comprises two main components: zero current switching loss and overlapping loss [12]. The zero current switching energy is reliant on the output capacitance ($C_{oss,Q}$) and switching voltage (U_{dc}); however, the overlapping energy is proportionate to $\frac{dV}{dt}$ and $\frac{di}{dt}$. Firstly, the zero current switching energy can be estimated using the FOM of SiC devices as given in (3).

$$\begin{aligned} E_{sw-ZCS} &= C_{oss,Q}(U_{dc}) \cdot U_{dc}^{\alpha_c} \\ &= k_c \cdot U_b^{\alpha_c} A_{die} \cdot U_{dc}^2 \end{aligned} \tag{3}$$

Secondly, the overlapping switching energy can be calculated as given in (4) where $\frac{dV}{dt}$ and $\frac{di}{dt}$ should be selected regarding layout parasitics, gate driver and isolation requirements of motor.

$$\begin{aligned} E_{sw-overlapping} = &(\frac{V_{dc} \cdot I_{sw}^2}{2 \cdot \frac{di}{dt_{on}}} + \frac{V_{dc}^2 \cdot I_{sw}}{2 \cdot \frac{dv}{dt_{on}}}) \\ &+ (\frac{V_{dc} \cdot I_{sw}^2}{2 \cdot \frac{di}{dt_{off}}} + \frac{V_{dc}^2 \cdot I_{sw}}{2 \cdot \frac{dv}{dt_{off}}}) \end{aligned} \tag{4}$$

Lastly, the total switching losses can be calculated by using (5) during a switching angle (θ_{SW1} to θ_{SW2}).

$$P_{sw} = \frac{f_{sw}}{2\pi} \int_{\theta_{SW1}}^{\theta_{SW2}} (E_{sw-overlapping}(\theta) + E_{sw-ZCS}(\theta))\, d\theta \tag{5}$$

Furthermore, multi-level topologies include additional diodes. The switching losses of these diodes might be ignored when SiC Schottky diodes are utilized. Thus, the diode losses can be calculated by using (6) where diode conduction angle (θ_{D1} to θ_{D2}), diode on-state voltage drop (V_{on}) and diode current ($i_{ds}(\theta)$) are needed.

$$P_d = \frac{1}{2\pi} \int_{\theta_{D1}}^{\theta_{D2}} V_{on} \cdot i_{ds}(\theta) \cdot D(\theta)\, d\theta \tag{6}$$

Unlike MOSFETs, the diode has an additional voltage drop (u_o), and on-state voltage drop (V_{on}) can be calculated as presented (7) by using FOM parameters.

$$\begin{aligned} V_{on} &= r_d \cdot I_d + u_o \\ &= (\alpha_d \cdot U_d^{2.5} + b_d) \cdot I_d + u_o \end{aligned} \tag{7}$$

The FOM parameters for SiC MOSFETs and diodes are given in Table II, retrieved from [11], [12].

B. The Selection of Switch Ratings

Selecting a switch's rated voltage has a noteworthy impact on the design stage of the traction inverter. It is often selected higher than the blocking voltage with a safety factor to account for voltage overshoots caused by high switching speeds and layout parasitics [13]. In our system, the safety factor of 1.36 is selected, leading to the switches' voltage ratings of 1700 V for 2-level topologies and 850 V for 3-level topologies. Furthermore, the optimal die area or current rating of the switch plays a critical role in the efficiency performance of the inverter. The appropriate die area depends on the switching frequency and the voltage change rate ($\frac{dv}{dt}$), as illustrated in Fig. 2. The die area selection will happen in the next section by comparing the switching frequency and $\frac{dv}{dt}$.

TABLE II: Figure of Merit Parameters for SiC MOSFETs and SiC Schottky Diodes [11], [12].

Parameter	Value	Unit
k_r	$7.2 \cdot 10^{-3}$	$m\Omega \cdot mm^2 \cdot V^{-1.6}$
α_r	1.6	unitless
k_c	$1.6 \cdot 10^4$	$pFmm^{-2} \cdot V$
α_c	-1	unitless
α_d	$649.6 \cdot 10^{-6}$	$\Omega \cdot mm^2 \cdot V^{-2.5}$
β_d	$202.2 \cdot 10^{-3}$	$\Omega \cdot mm^2 \cdot$
u_o	0.8127	V

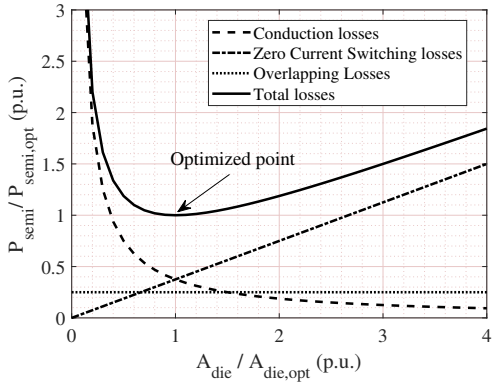


Fig. 2: Total switch losses for varying die area at a specific switching frequency and $\frac{dV}{dt}$.

C. Implementation of the Loss Modelling Algorithm in Different Topologies

The conduction and switching angles for switches and diodes are employed in calculating semiconductor losses using (1), (5), and (6). However, these angles vary based on different topologies [11], [14], [15]. As presented in Table III and Table IV, the angles for each switch and diode in a single leg during a positive half-cycle of the line current can be provided. It is also necessary to recognize that the switching voltage equals the DC-link voltage for 2-level topologies, whereas, for 3-level topologies, the switching voltage is half of the DC-link voltage.

TABLE III: Conduction and Switching Angles for 2L-3Ph and 2L-6Ph VSIs [11].

Switch	Conduction Angle	Duty ratio	Switching Angle
Upper	ϕ to $\pi + \phi$	$\frac{1+m_a \cdot sin(\theta)}{2}$	ϕ to $\pi + \phi$
Lower*	ϕ to $\pi + \phi$	$\frac{1-m_a \cdot sin(\theta)}{2}$	-

* means that the switch is in reverse conduction.

TABLE IV: Conduction and Switching Angles for 3L-NPC VSI [11].

Switch	Conduction Angle	Duty Ratio	Switching Angle
Upper-Top	ϕ to π	$m_a \cdot sin(\theta)$	ϕ to π
Upper-Middle	ϕ to π π to $\pi+\phi$	1 $1+m_a \cdot sin(\theta)$	π to $\pi+\phi$
Lower-Middle*	π to $\pi+\phi$	$-m_a \cdot sin(\theta)$	-
Lower-Bottom*	π to $\pi+\phi$	$-m_a \cdot sin(\theta)$	-
Upper-Diode	ϕ to π π to $\pi+\phi$	$1-m_a \cdot sin(\theta)$ $1+m_a \cdot sin(\theta)$	-
Lower-Diode	-	-	-

* means that the switch is in reverse conduction.

D. Cooling System Size Estimation

Fig. 3 illustrates a basic thermal model for the inverter, where two switches are integrated within the same package.

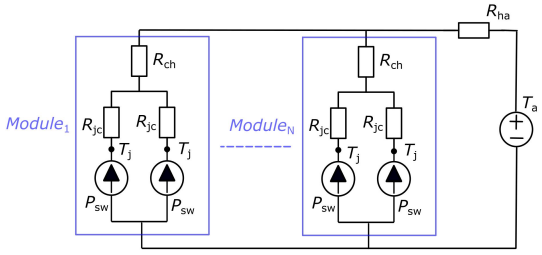


Fig. 3: An example of thermal circuit for inverter where R_{jc} is junction-to-case thermal resistance, R_{ch} is case-to-heatsink thermal resistance, R_{ha} is heatsink-to-ambient thermal resistance, T_j is junction temperature, and T_a is ambient temperature.

The thermal resistance from the junction-to-case decreases as the chip area increases, as shown in (8).

$$R_{jc} = \frac{r_{th-die}}{A_{die}} \tag{8}$$

Even if the total losses are the same for different topologies, the loss distribution and total die area lead to different heatsink sizes while keeping the junction temperature constant. For a simplified calculation, the thermal resistance for the heatsink can be determined as given in (9).

$$R_{ha} = \frac{T_j - T_a}{P_{loss}} - (R_{jc-eq} + R_{ch-eq}) \tag{9}$$

Then, the heatsink volume can be estimated by utilizing the cooling system performance index (CSPI) as shown in (10) [16].

$$V_h[liter] = \frac{1}{R_{ha}[\frac{^oC}{W}] \cdot CSPI[\frac{W}{^oC \cdot liter}]} \tag{10}$$

E. DC-link Capacitance Requirements

The selection of DC link capacitance relies on various factors such as switching frequency, voltage ripple requirements, line current, modulation technique, etc. This section aims to calculate the DC link capacitance to roughly compare its size for different topologies. Certain assumptions have been made to accomplish this goal. Firstly, the modulation technique chosen is carrier-based sinusoidal pulse width modulation (PWM). Secondly, the line current is considered pure sinusoidal. Lastly, all harmonics are considered to be provided by the DC-link capacitors, whereas DC current comes from the battery.

As an initial step, the capacitor current in the time domain ($I_C(t)$) can be calculated as given in (11) where $S_n(t)$ is the switching function of the top switches of the n^{th} phase and $I_n(t)$ is the current of the n^{th} phase [17].

$$I_C(t) = \sum_{n=1}^{\#Ph} = S_n(t) \cdot I_n(t) \tag{11}$$

The switching functions ($S_n(t)$) are different in 2-level and 3-level inverters, and they can be calculated by using double Fourier series as given in (12), the coefficient of which can be found in [18].

$$\begin{aligned} S(t) = &\frac{A_{00}}{2} + \\ &\sum_{}^{\infty} \left[A_{0n}\cos\left(n\left[\omega_o t + \theta_o\right]\right) + B_{0n}\sin\left(n\left[\omega_o t + \theta_o\right]\right)\right] + \\ &\sum_{m=1}^{\infty} \left[A_{m0}\cos\left(m\left[\omega_c t + \theta_c\right]\right) + B_{m0}\sin\left(m\left[\omega_c t + \theta_c\right]\right)\right] + \\ &\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \left[\begin{array}{c} A_{mn}\cos\left(m\left[\omega_c t + \theta_c\right] + n\left[\omega_o t + \theta_o\right]\right) \\ +B_{mn}\sin\left(m\left[\omega_c t + \theta_c\right] + n\left[\omega_o t + \theta_o\right]\right) \end{array}\right] \\ &(n \neq 0) \end{aligned} \tag{12}$$

Given the switching functions, the capacitance requirement is numerically calculated as presented in (13) for a specific peak-to-peak voltage ripple (ΔV^{pp}).

$$C_{bus} \geq \frac{max\left(\int_0^{Ts}(I_C(t) - I_{dc})dt\right) - min\left(\int_0^{Ts}(I_C(t) - I_{dc})dt\right)}{\Delta_V^{pp}} \tag{13}$$

F. Output Harmonics

The switching functions of (12) are used to calculate the differential output harmonics as presented in (14).

$$V_{out}(t) = V_{DC} \cdot (S_{AN}(t) - S_{BN}(t)) \tag{14}$$

Since the inverter's load is inductive, the harmonic component's impact decreases while increasing the harmonic numbers. Therefore, weighted total harmonic distortion, as given in (15), can be used as an indicator for the harmonic quality of the output [18].

$$WTHD = \frac{1}{V_{out-1}} \sum_{h=2}^{\infty} \frac{V_{out-h}^2}{h} \tag{15}$$

IV. Results of the Virtual Prototyping Method

The efficiency assessment of various topologies has been carried out through a comprehensive sweep of die area and switching frequency to identify an optimal operation point that minimizes inverter losses. As illustrated in Fig. 4, this process has resulted in a set of efficiencies and an operation point

is selected for all topologies at 99.4 percent efficiency. Each topology's switching frequency and die area information for these operation points are given in Table V.

TABLE V: Switching Frequencies and Die Areas of the Selected Designs.

Topology	Switching Frequency (kHz)	Die Area (mm^2)	Efficiency (%)
2L-3Ph	11	300	99.4
2L-6Ph	12	120	99.4
3L-NPC	25	90	99.4

Firstly, considering the die areas, the equivalent thermal resistance of junction-to-case and case-to-heatsink can be calculated by taking r_{th-die} as $2.5[\frac{^oC}{W \cdot mm^2}]$ and R_{ch} per module as $0.025[\frac{^oC}{W}]$. The topologies' thermal parameters and the required heatsink's thermal resistance are shown in Table VI where CSPI is taken as 10 for a water-cooling system, ignoring the heat-exchanger volume.

TABLE VI: Thermal Parameters and Heatsink-to-Ambient Resistance

Topology	T_j (^oC)	T_a (^oC)	R_{jc-eq} ($\frac{^oC}{W}$)	R_{ch-eq} ($\frac{^oC}{W}$)	R_{ha} ($\frac{^oC}{W}$)	CSPI ($\frac{W}{^oC \cdot liter}$)	Volume ($liter$)
2L-3Ph	100	25	0.0014	0.0084	0.0317	10	3.15
2L-6Ph	100	25	0.0017	0.0042	0.0355	10	2.8
3L-NPC	100	25	0.0015	0.0028	0.0371	10	2.7

Secondly, this study primarily focuses on the inverter losses while acknowledging the significance of harmonic losses on the traction motor. The weighted total harmonic distortion (WTHD) is a useful metric to account for motor harmonic losses without exact calculation. WTHDs of three topologies with given switching frequencies are illustrated in 5. The output harmonic quality of 3L-NPC VSI surpasses other topologies, as expected since it enables higher switching frequency and a 5-step voltage level at the output.

Lastly, The capacitance requirements are computed and laid out in the form of Table VII. The volume estimation is carried out with the aid of [19]. It is observed that the lowest capacitance demand is in 2L-6Ph, even though the applied switching frequency is lower than that of 3L-NPC.

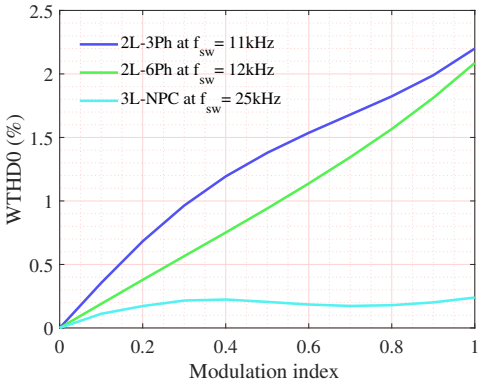


Fig. 5: Output harmonic quality of the evaluated topologies.

TABLE VII: The capacitance requirements of the evaluated topologies.

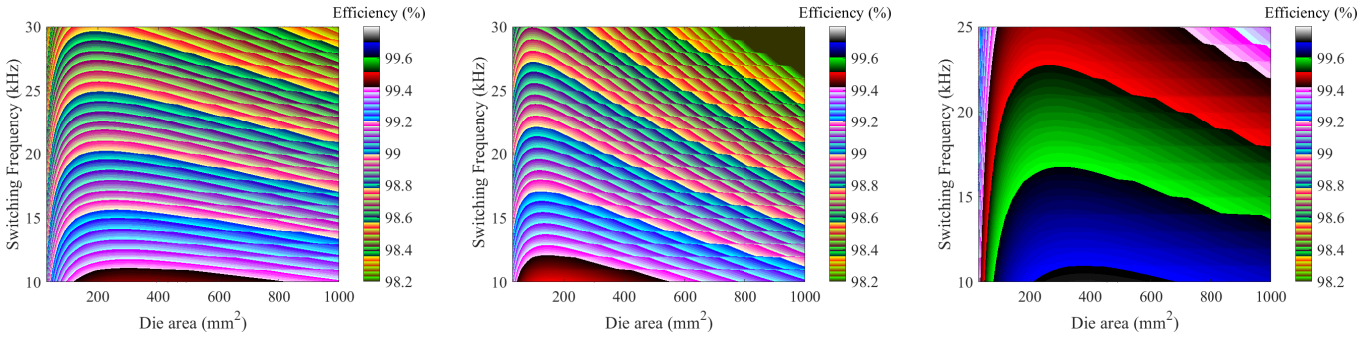
Topology	Switching Frequency (kHz)	Capacitance (μF)	Size ($Litre$)
2L-3Ph	11	525	3.5
2L-6Ph	12	300	2
3L-NPC	25	2x 200	2.66

V. Reliability Discussion

Upon initial investigation, 2L-3Ph VSIs would offer higher reliability than other topologies due to fewer switch and gate drive failure points. However, the switches in these inverters pose higher thermal stress resulting from higher semiconductor losses, which can lead to fatigue failures. Unlike 2L-3Ph VSIs, 2L-6Ph VSIs possess built-in redundancy that can operate in 3 phases, allowing them to function with reduced power in case of a failure and enhancing system reliability. Furthermore, DC-link capacitors are often the root cause of failures in traction inverters. Accordingly, 3L-NPC VSIs pose less stress on the DC-link capacitors, improving reliability.

VI. Conclusion

After conducting an extensive analysis of possible topologies in heavy-duty electric vehicles to keep pace with the



(a) 2-Level 3-Phase VSI. (b) 2-Level 6-Phase VSI. (c) 3-Level NPC VSI.

Fig. 4: The efficiency over varying die area and switching frequency (The conduction losses are scaled by 1.5 to consider the junction temperature at 100 ^oC.).

raised DC-link voltages and boosted power ratings, it can be concluded that 3L-NPC VSIs outperform 2L-3Ph and 2L-6Ph VSIs regarding several key performance indices. Through the utilization of a virtual prototyping method to calculate these performance indices, the use of figure-of-merit parameters ensured a fair comparison within the technology barrier. The adoption of 3L-NPC VSIs, which use lower voltage-rated MOSFETs, has resulted in a reduction of switching losses, allowing for an increase in switching frequency. This increase in frequency, coupled with the additional voltage level on output, has improved the output harmonic quality and has led to a reduction in the need for passive elements. These factors have resulted in a smaller volume, which ultimately reduces the total cost. Thus, the findings of this study suggest that the implementation of 3L-NPC VSIs could be a viable solution for heavy-duty electric vehicles to cope with the desired specifications.

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