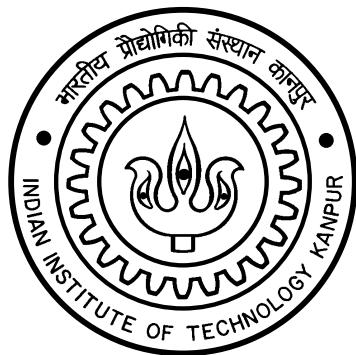


Modeling and Analysis of GaN HEMTs for Power-Electronics and RF Applications

by

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**Department of Electrical Engineering
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Modeling and Analysis of GaN HEMTs for Power-Electronics and RF Applications

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Sheikh Aamir Ahsan

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CERTIFICATE

It is certified that the work contained in the thesis titled **Modeling and Analysis of GaN HEMTs for Power-Electronics and RF Applications**, by **Sheikh Aamir Ahsan**, has been carried out under my supervision and that this work has not been submitted elsewhere for a degree.

Prof. Yogesh Singh Chauhan
Department of Electrical Engineering
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August, 2017

To My Best Buddies –

Ahsan,

My Awesome Father

and

Yüsuf,

My Adorable Son

Synopsis

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Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) and their associated power-electronics and RF applications have been a topic of academic and industrial research over the past couple of decades. This is due to the commendable level of performance promised by the GaN material system and the hetero-junction that it forms with AlGaN, leading to features such as high breakdown voltage, high mobility, high saturation velocity, high sheet carrier density, the ability to withstand high operating temperatures etc. In order to take full advantage of these properties and to translate them into viable circuit applications, a robust and accurate GaN HEMT compact model is urgently needed.

The existing literature encompasses a huge variety of models that are primarily empirical, table-based, artificial neural-network based or X-parameter based models. Such models obscure the device-circuit interactions as they are not based on the physics governing the various behavioural nuances and device dynamics.

High fidelity physics-based compact models for GaN HEMTs, particularly surface-potential-based, are desirable and the industry is looking for them for multiple reasons. First, GaN technology is still not fully matured and a physics-based model would help a great deal in the device design and therefore in the evolution of the GaN technology itself. Second, a physics-based model offers a relatively smaller set of parameters whose flow of extraction is simple and can be related to the intrinsic device physics, leading to a more meaningful model card. Finally, physics-based models are inherently scalable with regard to bias, temperature or geometry, which is of great significance to circuit designers as they can explore a wider design space.

GaN HEMTs exhibit certain nonidealities in their behaviour, such as current collapse, knee walk-out etc., which are manifestation of trapping effects within the device. A good compact model is supposed to capture this behaviour very well as this non-linearity severely reflects in the large-signal harmonic balance and load pull characteristics. Moreover, state-of-the-art models are also expected to accurately model the device characteristics for multiple bias, temperature and geometry conditions, without compromising on the computational efficiency and robustness at the same time. A desirable feature of the model is simple and well defined parameter extraction flow. Small-signal model parameter extraction for microwave transistors forms a key ingredient of their overall modeling process since it is a prerequisite to the subsequent large-signal and noise modeling.

In view of the above, the main objectives behind the research work carried out in this thesis are as follows:

- To develop a physics-based capacitance model for multiple field-plated GaN devices for accurate switching behaviour; to perform numerical and mixed-mode simulation to study the impact of field-plates on circuit switching transients; validation against commercial power GaN device.
- To present an RF GaN HEMT compact model for small-signal and large signal RF simulations; develop a comprehensive parameter extraction methodology; validation of the model and extraction procedure against broadband measured S-parameters, harmonic-balance and load-pull data; carry out statistical sim-

ulation study using proposed model.

- To study large gate-periphery GaN devices for novel parameter extraction methodologies; to mathematically understand the stability behaviour of GaN devices, particularly the impact of via-inductances on Rollett's stability factor.
- To analyze and model kink-effects observed in high frequency characteristics such as h_{21} and S_{22} of GaN HEMTs.

This thesis has been organized in seven chapters. To begin with, **Chapter 1** briefly presents the overview of the GaN device physics, polarization and the formation of the two dimensional electron gas (2DEG) in GaN HEMTs and the state-of-the-art in GaN technology for power-electronics and RF applications.

In **Chapter 2**, a discussion on contemporary GaN HEMT compact models available in the industry is made. A background of the Advanced SPICE Model for GaN HEMTs (ASM-GaN-HEMT) is given around which most of the work in this thesis is carried out. The status of the GaN HEMT standardization activity at the Compact Model Coalition (CMC) is also briefly touched.

In **Chapter 3**, a physics-based compact model is presented for field-plates, which have made their way into commercial GaN HEMTs for power-electronic applications due to their ability to enhance the device breakdown voltage. The incorporation of field-plates however comes at the cost of increased capacitances and therefore need to be accounted for in a switching circuit application. The significance of having field-plate capacitance model is illustrated through numerical and mixed mode transient simulations. Useful insight, obtained from numerical simulations about cross-coupling and substrate capacitances, is used to model these effects and successfully validate it against measured data of state-of-the-art power GaN devices for multiple bias and temperature conditions.

In **Chapter 4**, an end to end GaN HEMT based RF modeling solution, all the way from DC parameter extraction to simulating large-signal drive-up simulations, using a physics-based model, is reported. A step-by-step small-signal model extraction procedure is demonstrated which is extensively validated over broad-band

S-parameters of commercial RF GaN devices. The RF extraction procedure proposed in this portion of the thesis is distinct from the existing models and very useful from a model user's point of view since it involves the tuning or adjustment of only a handful of parameters, which is primarily facilitated by the strong physical background of the model. Self-heating model and a working trap-model, extracted from pulsed-IV measurements, are included in order to realize a more realistic model. Load-pull and harmonic balance simulations are performed to benchmark the model performance at large-signal RF excitation against corresponding measured data for a state-of-the-art RF GaN device. In addition, statistical simulations are also performed to identify possible causes of variability in a batch of 10 GaN devices.

In **Chapter 5** we exploit certain interesting features that are exhibited by large gate-periphery GaN devices to perform the RF parameter extraction which markedly differs from the existing methodologies in literature. The primary objective of this methodology is to extract the model using a single set of measured S-parameters (which could be converted to Z-parameters), without needing to de-embed the contribution of extrinsic bus-inductances. A study on the stability performance and its modeling is also carried out in this portion of the thesis. It is mathematically shown that high via-inductances lead to certain dips in stability as a result of their coupling with the intrinsic drain to source capacitance.

Chapter 6 is addressed towards analyzing and modeling the two major kink-effects reported in microwave devices - for h_{21} & S_{22} . h_{21} is an important figure of merit since it determines the unity current gain frequency (f_T) of a microwave device whereas S_{22} is crucial in determining the output matching network. Kink effects in both of these quantities therefore need to be considered which could be of importance to RF designers, both in the device and circuit domain. Here, both these effects are studied using mathematical expressions, which are further used to understand the impact of various model elements on the location and severity of these kink-effects.

Finally, **Chapter 7** summarizes the main findings of the work carried out in this thesis and suggests the directions for possible extensions.

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Abbreviations

GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
RF	Radio Frequency
2DEG	Two Dimensional Electron Gas
ASM	Advanced SPICE Model
CMC	Compact Model Coalition
Si	Silicon
BJT	Bipolar Junction Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
LDMOS	Laterally Diffused MOSFET
IGBT	Insulated Gate Bipolar Transistors
SiC	Silicon Carbide
GaAs	Gallium Arsenide
InP	Indium Phosphide
HBT	Heterojunction Bipolar Transistors
SiGe	Silicon Germanium
AlGaN	Aluminum Gallium Nitride
InN	Indium Nitride
MOVPE	Metal-Organic Vapor Phase Epitaxy
MOCVD	Metal-Organic Chemical Vapor Deposition
MBE	Molecular Beam Epitaxy

UID	Unintentionally Doped
CTE	Coefficient of Thermal Expansion
Ga	Gallium
N	Nitrogen
FP	Field Plate
PAE	Power Added Efficiency
PA	Power Amplifier
DIBL	Drain Induced Barrier Lowering
2D	Two Dimensional
3D	Three Dimensional
EDA	Electronic Design Automation
MVSG	MIT Virtual-source GaN HEMT
BFOM	Baliga Figure of Merit
GFP	Gate-connected Field Plate
SFP	Source-connected Field Plate
TCAD	Technology Computer Aided Design
SP	Surface Potential
DUT	Device Under Test
CLM	Channel Length Modulation
AR	Access Region
SHE	Self Heating Effect
SS-EC	Small Signal Equivalent Circuit
GMF	Gate Manifold
DMF	Drain Manifold
SMF	Source Manifold
PDK	Process Design Kit
TRL	Thru Reflect Load
KE	Kink-Effect

LUT	Look Up Table
PEL	Parameter Extraction Language
HDL	Hardware Description Language
ADS	Advanced Design System

xl

List of Symbols

f_T	Unity Current Gain Frequency
R_{on}	ON Resistance
Cu ₃ N	Copper Nitride
Al ₂ O ₃	Sapphire
P _{SP}	Spontaneous Polarization Vector
P _{PZ}	Piezoelectric Polarization Vector
E_F	Quasi Fermi Level
E_D	Occupied Donor Level
E_0	Zeroth Sub-band Energy Level in the triangular quantum well
E_1	First Sub-band Energy Level in the triangular quantum well
I_{ds}	Drain Current
g_{ds}	Output Conductance
g_m	Transconductance
v_{ds}	Drain to Source Voltage
v_{gs}	Gate to Source Voltage
I_{dsat}	Drain Saturation Current

V_{off}	Cutoff Voltage
V_{br}	Breakdown Voltage
Q_g	Gate Charge
Q_{rr}	Reverse Recovery Charge
R_g	Gate Resistance
$R_{g,i}$	Intrinsic Gate Resistance
$R_{g,f}$	Gate Finger Resistance
L_g	Gate Length
$C_{p,T}$	Fringing T-gate Capacitance
L_{sd}	Source to Drain Distance
t_{bar}	Barrier Thickness
C_{gs}	Gate to Source Capacitance
C_{gd}	Gate to Drain Capacitance
C_{ds}	Drain to Source Capacitance
v_x	Carrier Injection Velocity
V_{go}	Gate Overdrive Voltage
V_{th}	Thermal Voltage
C_{iss}	Input Capacitance
C_{rss}	Reverse Capacitance
C_{oss}	Output Capacitance
W	Gate Width
C_{subd}	Substrate to Drain Capacitance

ψ	Surface Potential
ψ_d	Drain-side Surface Potential
ψ_s	Source-side Surface Potential
Q_d	Drain Charge
Q_s	Source Charge
Q_{ch}	Channel Charge
C_g	Gate Capacitance per Unit Area
L_{GFP}	Gate Field Plate Length
L_{SFP}	Source Field Plate Length
α_{cc}	Cross Coupling Scaling Factor
C_{accd}	Drain Access Region Capacitance
ΔE_c	AlGaN/GaN Conduction Band Discontinuity
σ_{pz}	Polarization Induced Charge Density
E_g	Band Gap
V_{bi}	Built-in Voltage
C_{J0}	Bias-independent Depletion Capacitance
T	Temperature
$TNOM$	Nominal Temperature
d	Insulator Thickness
k	Index for different FP transistors
I_{gg}	Gate Drive Current
P_{out}	Delivered RF Output Power

P_{in}	Input RF Power
N_f	Number of Gate Fingers
U_0	Carrier Mobility
R_{TH0}	Thermal Resistance
C_{TH0}	Thermal Capacitance
Δ_T	Rise in Temperature
$V_{sat,A}$	Access Region Carrier Saturation Velocity
$U_{0,A}$	Access Region Carrier Mobility
$N_{s0,A}$	Access Region Sheet Carrier Density
I_{pp}	Peak to Peak Current Swing
v_{pp}	Peak to Peak Voltage Swing
R_{ds}	Access Region Resistance
η_0	DIBL Parameter
C_{DSCD}	Subthreshold Slope Degradation Parameter
V_{dQ}	Quiescent Drain Bias Voltage
V_{gQ}	Quiescent Gate Bias Voltage
ω	Angular Frequency
$C_{gs,i}$	Gate Source Intrinsic Capacitance
$C_{gd,i}$	Gate Drain Intrinsic Capacitance
$C_{ds,i}$	Drain Source Intrinsic Capacitance
$C_{gs,p}$	Gate Source Parasitic Capacitance
$C_{gd,p}$	Gate Drain Parasitic Capacitance

$C_{ds,p}$	Drain Source Parasitic Capacitance
S_{xy}	Scattering Parameter
Γ	Reflection Coefficient
V_{trap}	Trap Voltage
μ	Mean
$\sigma\%$	Standard Deviation Percent
$[Z]$	Z-Parameter Matrix
$[Y]$	Y-Parameter Matrix
L_g	Gate Bus-Inductance
L_d	Drain Bus-Inductance
L_s	Source Bus-Inductance
L_{via}	Via Inductance
ΔZ	Determinant of the Z-Parameter Matrix
K	Rollett's Stability Factor
f_K	Unity Stability Factor Frequency
h_{21}	Short Circuit Current Gain
Z_{22}	Open Circuit Output Impedance
ζ	Damping Factor
f_k	Kink Frequency
S_{22}	Output Reflection Coefficient
Z_{out}	Output Impedance
Z_0	Characteristic Impedance

$Z_{out,i,low}$ Low Frequency Output Impedance

$Y_{out,i,high}$ High Frequency Output Admittance

Ga₂O₃ Gallium Oxide

Chapter 1

GaN HEMTs - Technology and Overview

Since the late 1950s, for more than half a century now, most of the burden of the microelectronics industry has been shouldered by the Silicon (Si) material system. Power MOSFETs based on Si have been the workhorse for power-electronics and power-delivery market [1]. Si-based Vertical FETs, Bipolar Junction Transistors (BJTs), Laterally Diffused MOSFET (LDMOS) and Insulated Gate Bipolar Transistors (IGBTs) have been used extensively in high power switching-circuits that form building blocks of most power conversion systems [2]. Even though these devices have continuously been under evolution and tailoring in order to push their performance limits, these power devices have reached a performance plateau due to the material constraints of Si, while the efficiency and cost demands of the power-electronics and power-conversion industry are ever so increasing. As a result, the industry has been looking for alternate materials particularly wide band-gap semiconductors such as Silicon Carbide (SiC) and Gallium Nitride (GaN) which present a way forward towards achieving the desired performance [3].

As far as the RF and Microwave sphere of applications is concerned, devices based on III-V materials such as Gallium Arsenide (GaAs) MESFETs, Indium Phosphide (InP) Heterojunction Bipolar Transistors (HBTs), GaAs High Electron Mobility Transistors have been the preferred choice for monolithic microwave integrated



Milcom



Radar



Satcom & Point-to-point Radio



Telecom



Data Link & Tactical Data Link



Broadband Amplifiers

Figure 1.1: Electronic application areas for GaN HEMTs [4].

circuits (MMICs) [5]. In addition, recent advances in Silicon Germanium (SiGe) HBTs and Si CMOS technologies have come up as low-cost solutions for MMICs and shown improved performance while offering high-level integration.

Over the past couple of decades, GaN has emerged as a promising material to cater to the needs of both these domains of contemporary microelectronics i.e RF and Power-Electronics [6]. A lot of avenues, as shown in Fig. 1.1, are opened for GaN HEMTs in the RF and Power-electronics domain so much so that they have emerged as strong candidates to replace the existing technologies for these applications. It is due to some interesting material properties, shown in Fig. 1.2 [7], exhibited by GaN, which are as follows:

1. It has a wide bandgap of 3.4 eV which enables it to withstand high electric fields before reaching breakdown. A wide bandgap also facilitates the high temperature operation of GaN devices [3]. Also, GaN devices are capable of delivering high power which is due to their high breakdown voltages.
2. It has a superior carrier saturation velocity of the order of 3×10^7 cm/s, which leads to high levels of drive currents in GaN devices which translates to higher delivered power [8]. Moreover, lower carrier transit time due to higher saturation velocity also enables the high frequency operation of GaN devices.

	Si	4H-SiC	GaN (Epitaxial)	GaN (Bulk)
Band gap energy, E_g (eV)	1.1 ind.	3.26 ind.	3.42 dir.	3.42 dir.
Electric breakdown field, E_{crit} (10^6 V/cm)	0.3	2.2	2	3.3
Relative dielectric constant, ϵ_r	11.9	10.1	9	9
Thermal conductivity, k (W/K·cm)	1.5	4.9	1.3	2.3
Electron mobility, μ_e (cm ² /V·s)	1350	900	1150 (2000) ^a	1150 (2000) ^a
Saturation velocity, v_{sat} (10^7 cm/s)	1.0	2.0	3	3
$\text{BFM}_{\text{Si}}, \epsilon_r \mu_e E_{\text{crit}}^3$	1	223	190 (330) ^a	850 (1480) ^a
$\text{BHFFM}_{\text{Si}}, \mu_e E_{\text{crit}}^2$	1	45	36 (63) ^a	98 (170) ^a
$\text{JFM}_{\text{Si}}, v_{\text{sat}} E_{\text{crit}}/2$	1	215	400	1090
Maximum estimated operation temperature, T_{\max} (°C)	200	500	700	700

Note: ^aAs most of the GaN power transistors realized today rely on the two-dimensional electron gas (2DEG) properties at the GaN/AlGaN interface, the 2DEG-related data are given in parentheses wherever applicable.

Figure 1.2: Comparison of Physical Parameters of Epitaxial GaN Layers as well as Bulk Ga Crystals against Si and 4H-SiC [7].

On top of these material properties, GaN, upon making a heterostructure with Aluminum Gallium Nitride (AlGaN), shows some even more exciting features which are enumerated as follows:

1. A high density two dimensional electron gas (2DEG) of electrons of the order of $1 \times 10^{13} / \text{cm}^2$ is created at the AlGaN/GaN heterojunction due to spontaneous and piezoelectric polarization [9]. High density 2DEG results into high drive current which eventually results into higher power delivering capabilities of GaN HEMTs.
2. 2DEG created at the heterojunction is of high mobility since there is no need to perform doping to create the 2DEG and therefore there is no scattering due to ionized dopants. It is due to this property of the AlGaN/GaN heterostructure

that AlGaN/GaN HEMTs have a low ON resistance (R_{on}), which leads to GaN HEMTs with much superior power added efficiency [8].

In light of the above mentioned desirable characteristics, GaN looks like the ideal material required to drive the RF and Power-electronics industry. Understandably, a great deal of research effort is dedicated towards the fine-tuning of the GaN technology in order to make it a fully commercial technology. Tremendous progress has been made in the areas of GaN device fabrication, all the way from developing high quality substrates to packaging, which includes the refining of some key device design steps such as epitaxial growth, heterostructure design etc.

But before we delve any further into the physics of operation of GaN devices, let's take a step back to appreciate the long route that GaN as a material has traveled thus far.

1.1 History

Way back in 1938, Juza for the first time synthesized GaN along with nitrides of Copper (Cu_3N) and Indium (InN) [10]. However, it took a great deal of time in making good quality epitaxial films of GaN until the end of 1960s. A lot of research effort was put forth in laboratories in Europe [11], Japan [12] and the United States [13, 14] to understand and improve the growth morphology of GaN aimed towards development of LEDs. Amano *et al.* using Metal-Organic Vapor Phase Epitaxy (MOVPE) in 1986 [15], demonstrated growth of high quality GaN films which after collaborative efforts from Akasaki and Nakamura later culminated into the well known blue LED for which they were decorated with the Nobel Prize [16].

GaN as a potential material for electronic applications was identified by Khan *et al.* [17] and finally a successful demonstration of a GaN HEMT was carried out by them for the first time in 1993 [18]. Ever since, the GaN microelectronics technology has come of age so much so that global GaN semiconductor devices market is expected to be worth \$ 3.5 Billion by 2024 [19]. Fig. 1.3 sketches the key historical milestones in the development of GaN as a popular material for microelectronics

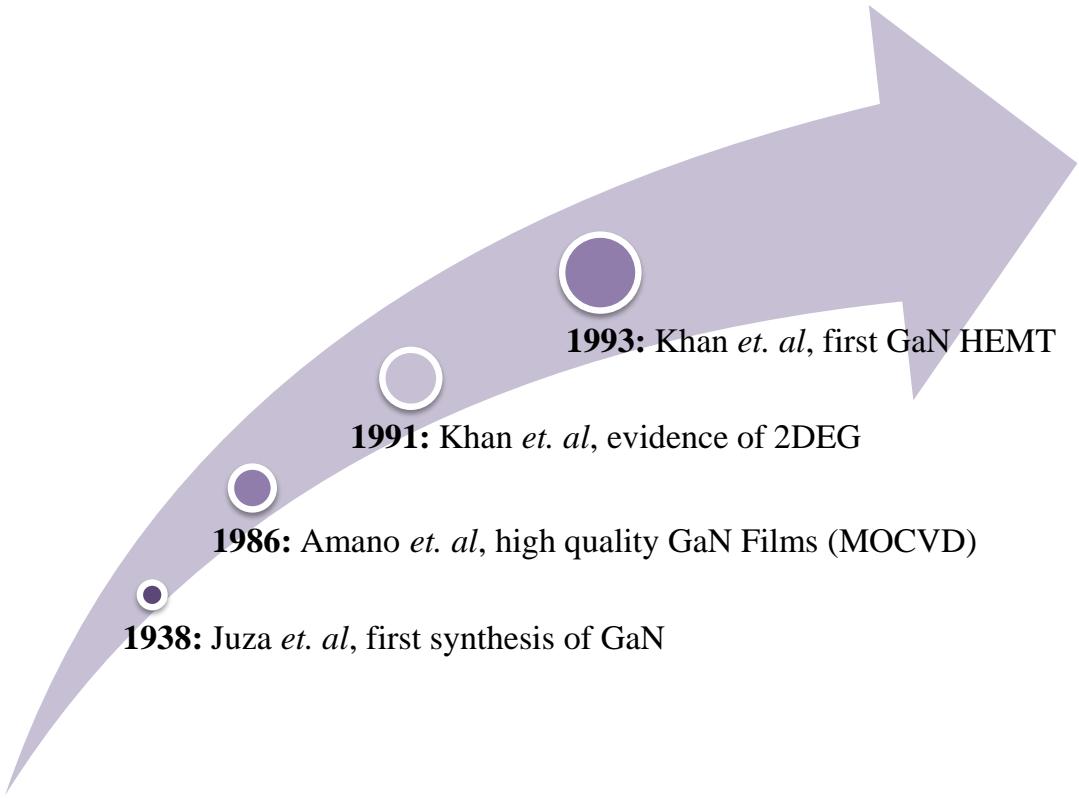


Figure 1.3: Key historical milestones in the development of the GaN as a potential material for the semiconductor industry

applications.

1.2 GaN HEMT Device Structure and Principle of Operation

Shown in Fig. 1.4 is a 2-dimensional cross-sectional representation of a typical GaN HEMT. It is an epitaxial structure in which a GaN buffer layer is grown on top of a high quality substrate using MOCVD or Molecular Beam Epitaxy (MBE). Graded AlN to GaN region is used as a nucleation region to prevent defects and dislocations from getting into GaN from the substrate. Typically, the thickness of the GaN buffer layer is a few microns. The choice of substrate depends upon the type of application that the device is aimed for. Sapphire (Al_2O_3), Si and SiC are the commonly used substrate materials for making GaN HEMTs although most

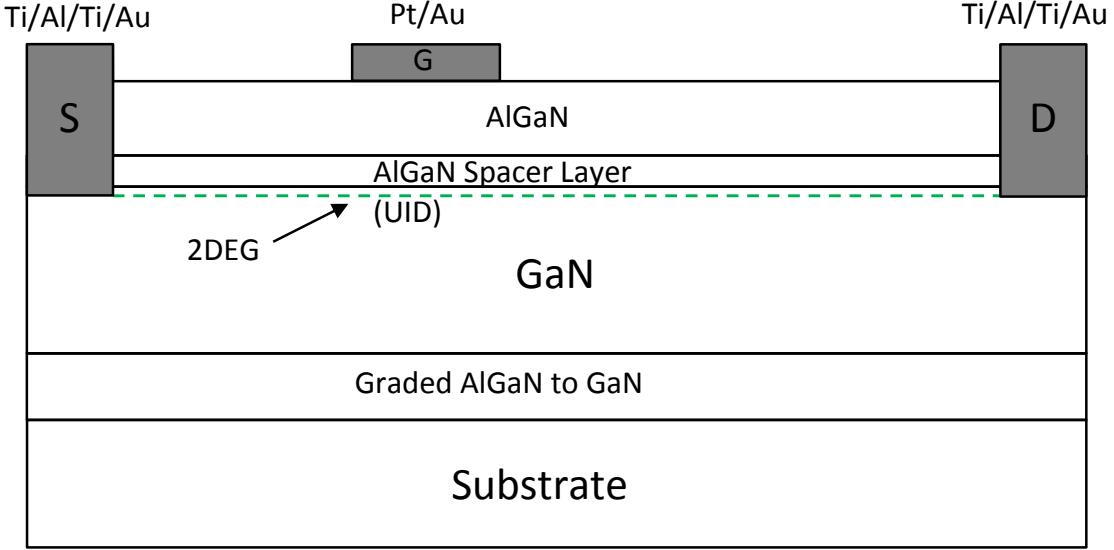


Figure 1.4: Cross sectional view of a conventional GaN HEMT.

recently GaN-on-diamond is being carefully looked at for improved performance metrics [20, 21].

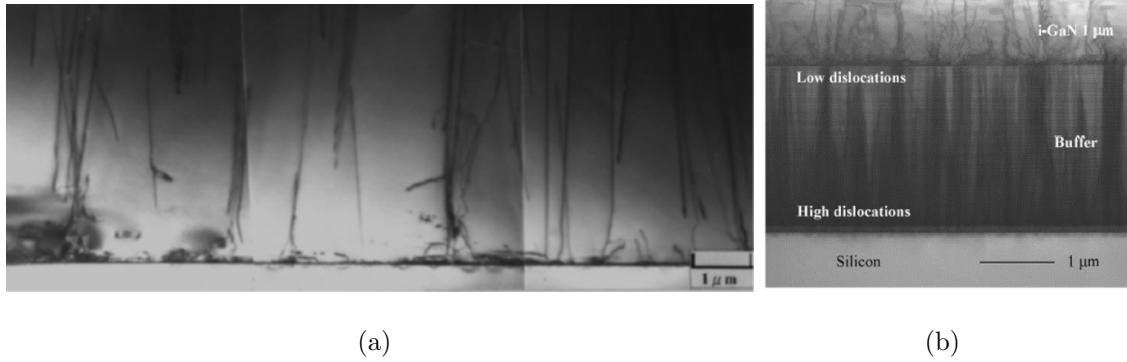


Figure 1.5: TEM images for GaN grown on (a) Sapphire [22] and (b) Silicon [23]. The threading dislocations that penetrate the GaN buffer are seen in both the cases.

Sapphire is a low thermal conductivity material, whose lattice constant and coefficient of thermal expansion (CTE) show a significant mismatch with GaN, which is a downside for a substrate as it leads to threading dislocations into the buffer as shown in Fig. 1.5(a). Nevertheless, it is a relatively economical substrate option which can withstand high growth temperatures and is semi-insulating in nature. Si also suffers from a lattice and CTE mismatch with GaN as reflected by dislocations of

the order of 10^9 /cm² in Fig. 1.5(b), however, Si substrates have certain advantages such as standard processing in Si fabs, availability of large diameter wafers and an acceptable thermal conductivity. On the other hand, SiC wafers have low mismatch values for GaN and have very high thermal conductivity which is a very important feature for a substrate material but SiC wafers are generally smaller and costly.

A thin barrier layer of AlGaN, with a controlled mole fraction of Al, is grown epitaxially on top of GaN to form the heterojunction between AlGaN and GaN, which are two different materials with different bandgaps leading to the formation of the quantum well at the interface. Metallic contacts are used for gate, source and drain as indicated. The 2DEG is formed at the heterojunction between AlGaN/GaN as a consequence of spontaneous and piezoelectric polarization and their interplay with donor type interface states on the AlGaN surface, as explained next.

1.2.1 Polarization

GaN manifests itself in a wurtzite crystal structure in which each Gallium (Ga) atom is bonded tetrahedrally to four Nitrogen (N) atoms as shown in Fig. 1.6(a). However, the tetrahedral is an imperfect one as it lacks inversion symmetry along the [0001] axis. Due to the strong electronegative nature of N, the nature of the Ga-N bond is significantly polar which leads to the formation of a strong macroscopic polarization dipole (P_{SP}) along the [0001] axis within the GaN crystal as shown in Fig. 1.6(b) [9]. This is known as spontaneous polarization.

Shown in Fig. 1.7(a) is a cartoon that illustrates the difference in the basal-plane lattice constant for AlGaN and GaN layers. GaN being the relaxed layer and since AlGaN is on top, it leads to a tensile strain in the AlGaN layer right in the vicinity of the heterojunction which results in the formation of a polarization vector (P_{PE}) in AlGaN in addition to its own P_{SP} dipole. This is known as piezoelectric polarization. All the polarization vectors in the AlGaN/GaN heterostructure are shown by a cartoon in Fig. 1.7(b) for the sake of illustration.

Due to the abrupt change in the net polarization vector at the interface, a sheet of positive polarization charge is created as an outcome of Gauss's Law in

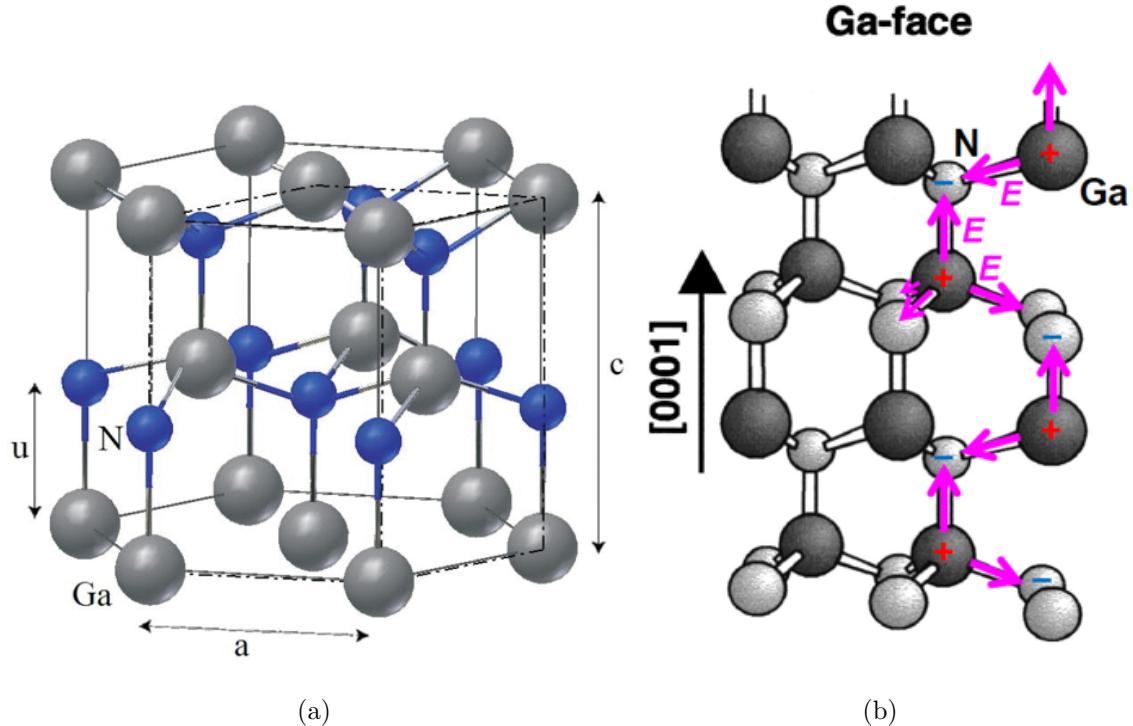


Figure 1.6: (a) Wurtzite crystal structure of GaN which results into lack of inversion symmetry along the [0001] axis. (b) Spontaneous polarization vector due to lack of inversion symmetry along the [0001] axis and strong polar nature of the Ga-N bond [9].

case of Ga-face GaN. The corresponding negative polarization charge develops at the top of the AlGaN barrier as indicated in Fig. 1.7(b). This polarization dipole in the AlGaN layer gives rise to what we know as the 2DEG at the interface which is explained next.

1.2.2 2DEG Formation

Fig. 1.8(a) shows the band diagram for an AlGaN/GaN heterostructure indicating various charge components. The device electrostatics across the heterostructure result in a quantum well within which the 2DEG is formed. Ibbetson *et al.* proposed that, for a truly undoped AlGaN barrier, it is the donor-type surface states at the top of the AlGaN barrier that are the source of electrons in the 2DEG, which essentially is an outcome of charge balance across the heterostructure [25]. There

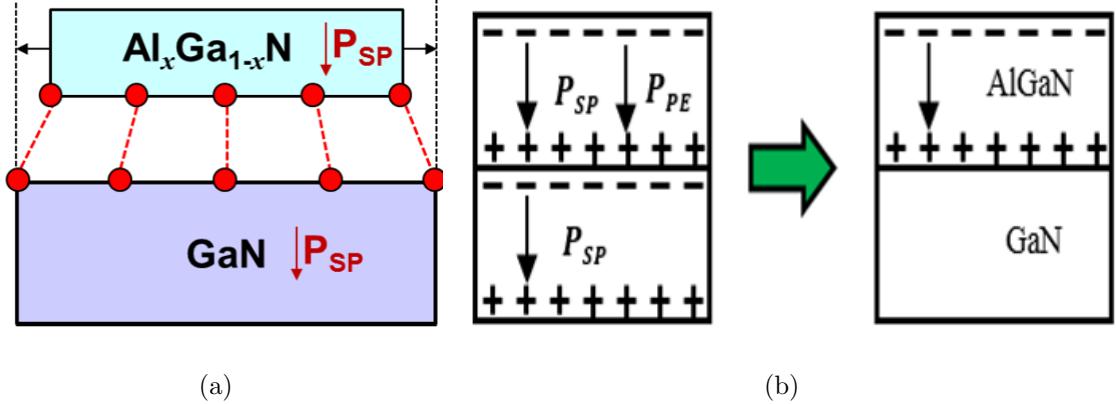


Figure 1.7: (a) Cartoon showing different basal-plane lattice constant for AlGaN and GaN leading to tensile strain in the AlGaN layer [24]. (b) Illustration of spontaneous and piezoelectric polarization vectors in AlGaN/GaN heterostructure that lead to the formation of polarization charges at the AlGaN/GaN heterojunction and the AlGaN surface [9].

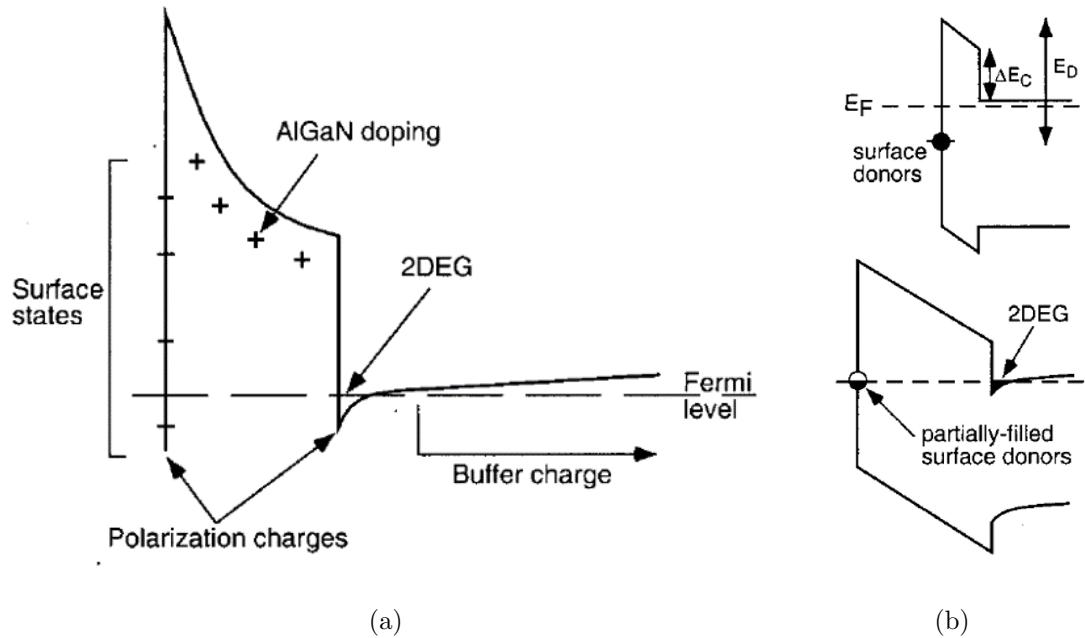


Figure 1.8: (a) Schematic band diagram showing various charge components. (b) Illustration of surface donor model for $t_{bar} < t_{crit}$ and $t_{bar} > t_{crit}$ [25].

is an interplay between the fermi-level (E_F), occupied surface levels (E_D), the GaN conduction band edge and the polarization dipole within the AlGaN barrier.

For the sake of illustration, the cartoon in Fig. 1.8(b) shows that there is a constant unscreened polarization dipole in the AlGaN barrier before the 2DEG is formed, which is the case if the surface states are deep enough to get ionized. $E_F - E_D$ decreases as the barrier thickness increases until minimum critical thickness is reached upon which the surface states start getting ionized, leading to the formation of 2DEG in the quantum well and leaving behind ionized donor states at the barrier. Since these 2DEG electrons are brought about without enforcing any potential at the gate, the device is therefore normally ON or depletion-type.

1.3 Device Characteristics

GaN devices exhibit certain characteristic features that need to be understood if a working model for the same is to be developed. It is essential to pay attention to the various nuances in measured characteristics that arise due to various physical phenomena. In this section, we review some of those characteristics particularly shown by the devices that have been used to perform the modeling and analysis in this thesis.

The devices studied and modeled in this thesis are commercial, state of the art GaN devices. For power-electronics applications, a power GaN HEMT from Toshiba was used whereas Qorvo devices were used for RF modeling, analysis and parameter extraction. The details of these devices are provided in the subsequent chapters of the thesis.

1.3.1 Access Regions and Self-heating

Shown in Fig. 1.9 is the $I_d - V_d$ and corresponding $g_{ds} - V_d$ characteristics for the Toshiba power GaN device taken under pulsed conditions with pulsed width 2 ms and a pulse period of 100 ms. Few important observations can be made from the measured characteristics. The device exhibits R_{on} of the order of few Ω s, which primarily arises due to the presence of access regions at the source and drain ends of the device. These access regions are essentially kept in power devices to enhance

their breakdown voltages which is important for their high power handling capability.

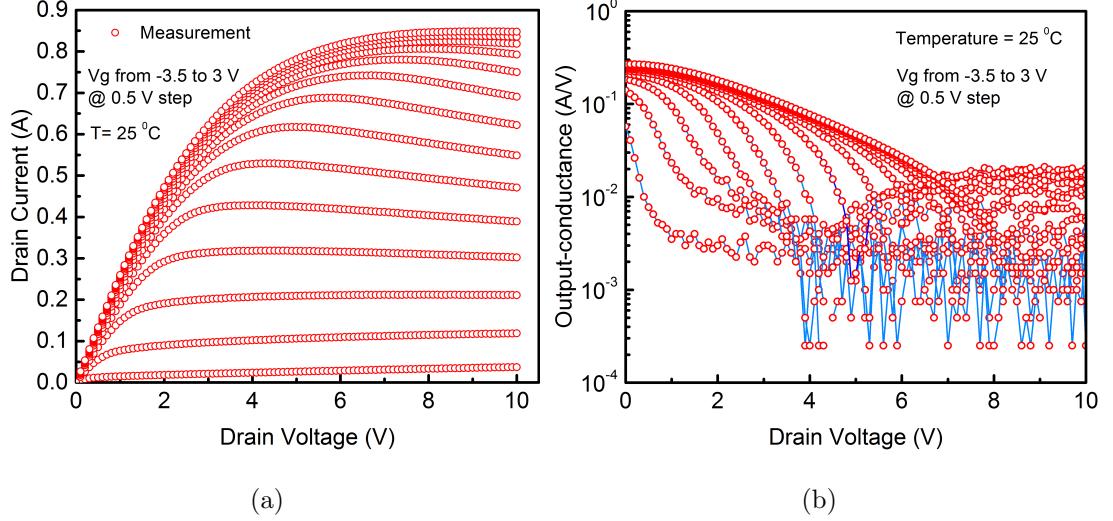


Figure 1.9: Measured (a) $I_d - V_d$ and (b) $g_{ds} - V_d$ characteristics for the Toshiba Power GaN HEMT for various values of V_g from -3.5 V to 3 V in steps of 0.5 V.

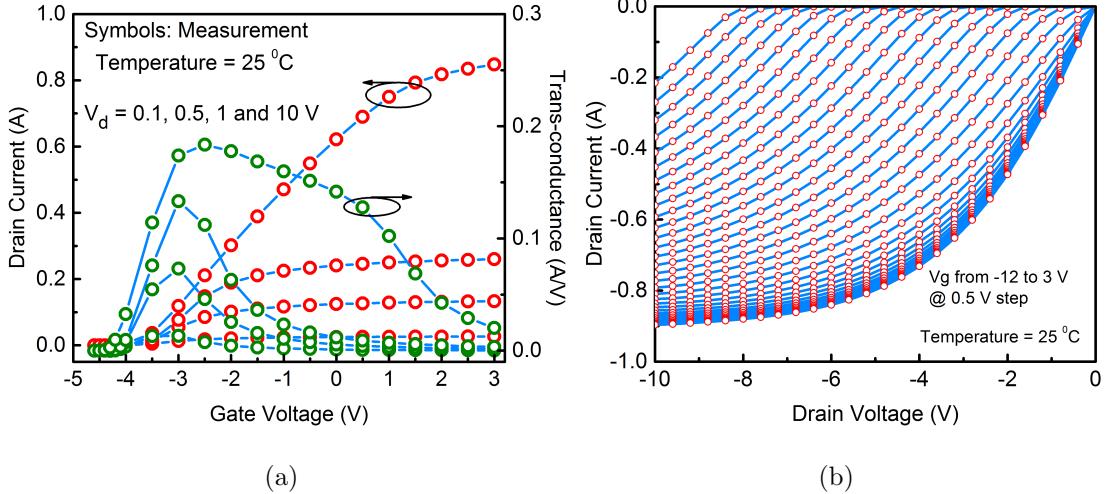


Figure 1.10: Measured (a) $I_d - V_g$ and corresponding $g_m - V_{gs}$ characteristics for V_{ds} 0.1 V, 0.5 V, 1 V and 10 V (b) Reverse $I_d - V_d$ for the Toshiba Power GaN HEMT.

The effect of access region resistances can be better understood by inspecting the $I_d - V_g$ and corresponding $g_m - V_{gs}$ characteristics as shown in Fig. 1.10(a). The plots show that at higher gate voltage, the access region resistance dominates

and current flattens out with increase in V_g . From the transconductance (g_m) plot, different slopes in the moderate to high transition region and in the high region are observed for the higher V_d curve corresponding to $V_d = 10$ V. The first slope degradation in g_m at V_g between -2.5 V and 0.5 V, is primarily due to the self-heating effect, whereas the second slope, for V_g beyond 1 V, is dominated by the velocity-saturation phenomenon in the non-linear access regions.

Although the measurements have been performed in pulsed mode, the self-heating effect is clearly observed in $I_d - V_d$ plots in Fig. 1.9 at higher V_g since the pulsed width is not sufficiently small. The self-heating phenomenon is well known to occur in devices with high drive currents which causes increase in device operating temperature. Under such conditions lattice vibrations get intensified which subsequently results in reduction of electron velocity due to lattice scattering. This is reflected in the form of a current collapse. At high V_g , quasi-saturation behavior in $I_{ds} - V_{ds}$ characteristics is clearly observed as there is very little change in current with increase in V_g [26]. Fig. 1.9(b) shows a sharp dip in the logarithmic g_{ds} plot, which is the signature of self-heating effect in which g_{ds} changes sign at the point of inflection and becomes negative beyond a certain V_d bias.

Power devices, particularly those employed in high power converter circuits, encounter reverse currents due to the presence of inductors in converter circuits. It is therefore important to take a look at the reverse-mode ($V_{ds} < 0$) characteristics of the power GaN device. Significant reverse-mode currents with relatively low R_{on} are seen in Fig. 1.10(b) which essentially obviates the requirement of a free-wheeling diode in converter circuits.

1.3.2 Broad Temperature Operation

GaN power devices, like power devices from other technologies, are aimed at working at very high power levels and in the process, these devices are subjected to very high operational temperatures. As a result, the device behavior exhibits a marked departure from what is seen at nominal temperature. From a circuit design perspective, it is of paramount importance to have a device model that reproduces the

device behavior at high temperatures which could be taken into consideration during the circuit design process. Moreover, the model could also be used for making the device design optimum provided the model is based on the underlying physics of the device. And for that, high temperature measurements are a necessity.

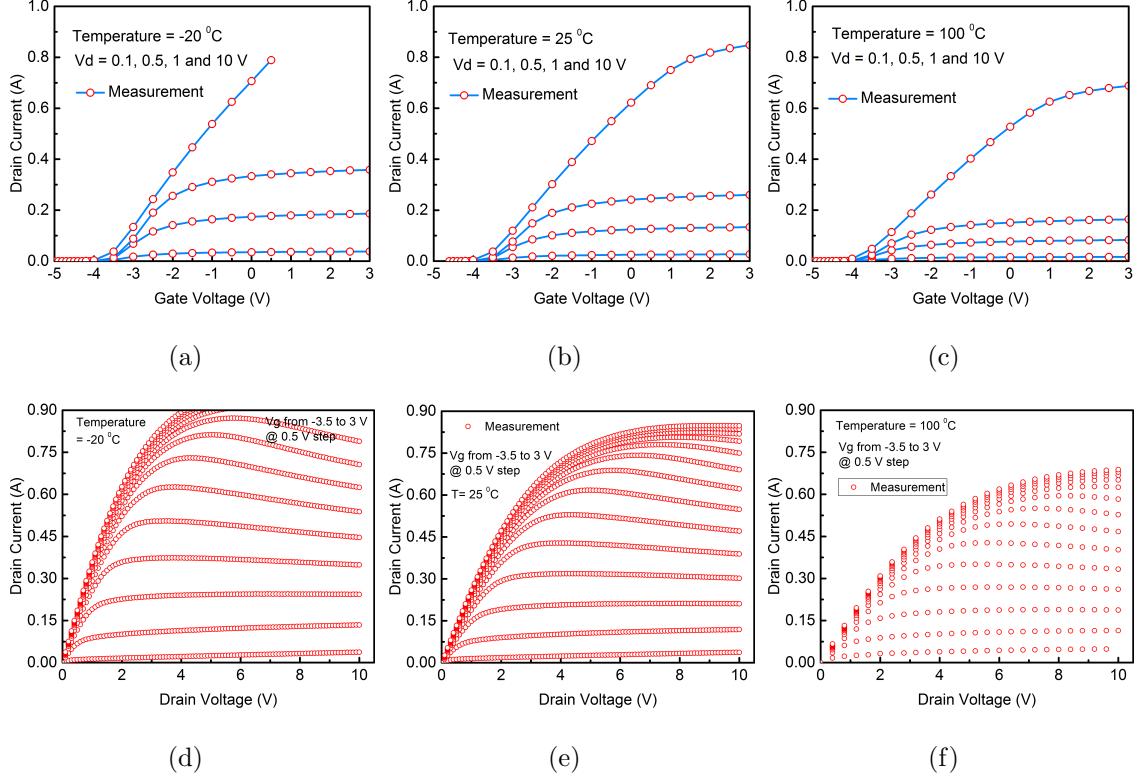


Figure 1.11: $I_d - V_g$ characteristics for the Toshiba power GaN HEMT taken under (a) -20°C (b) 25°C (c) 100°C and corresponding $I_d - V_d$ characteristics in (d), (e) and (f) respectively. R_{on} degradation with reduction in I_{dsat} is observed as measurement temperature is raised.

Shown in Fig. 1.11 are the $I_d - V_d$ characteristics for the GaN power device for multiple gate bias conditions in steps of 0.5 volts. The temperature of the thermal chamber was varied from 25°C to 150°C . Clearly, the gradual increase in R_{on} and decrease in saturation current (I_{dsat}) with progressively changing operating temperature indicates a degraded carrier mobility in the access regions and reduced carrier velocity [27].

The multiple temperature characteristics obtained can be rearranged as shown

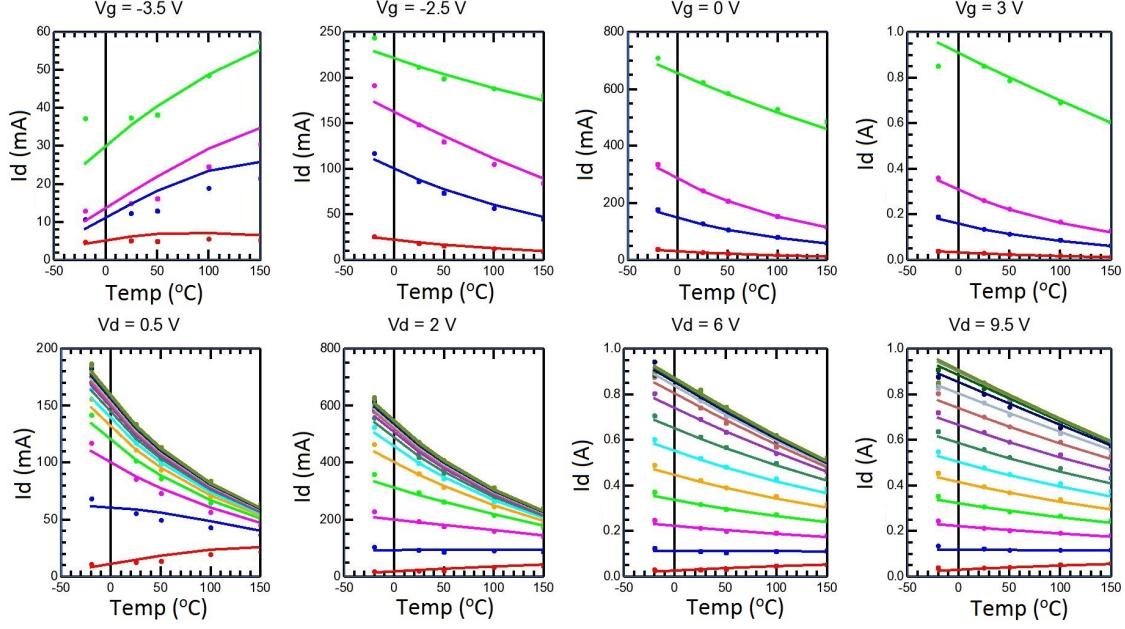


Figure 1.12: I_d for a broad range of temperature (-20° C to 150° C) for (Top) 4 different V_g values with V_d as second order list sweep of 0.1 V, 0.5 V, 1 V and 10 V (Bottom) 4 different V_d values with V_g as second order sweep varying from -3.5 V to 3 V in steps of 0.5 V. Symbols: Measured Data, Lines: Model

in Fig. 1.12 to understand the rate of change of current with varying temperature and it can also be used to perform modeling and parameter extraction for the same.

1.3.3 Trapping

While GaN HEMT technology has made huge strides over the last decade and is steadily on the trajectory of what we know as a "mature" technology, it is still plagued with issues of its own and one of those is the phenomenon of charge trapping. Trapping particularly affects the non-linear RF performance of devices and leads to diminished output power and efficiency [28]. In order to get a flavor of the real-life operating conditions that the RF GaN device is subjected to, the behavior of the device is studied under pulsed conditions which are the closest possible to real-life RF excitations.

Shown in Fig. 1.13 are pulsed $I_d - V_g$ and $I_d - V_d$ for the Qorvo RF GaN device under different quiescent bias conditions. The details of the pulsed measurement

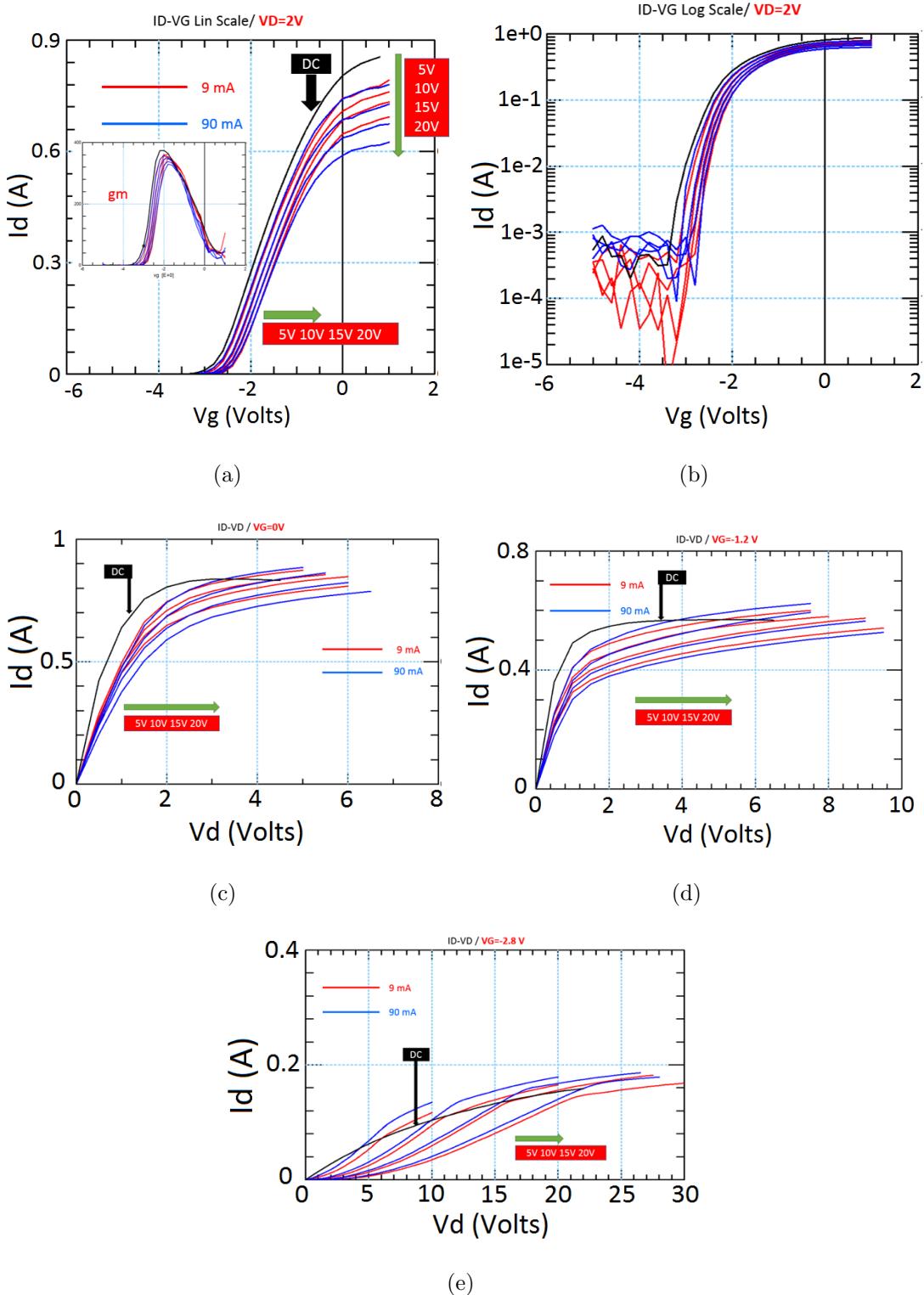


Figure 1.13: Pulsed (a, b) $I_d - V_g$ linear and log scale and (c-e) $I_d - V_d$. 8 different stress conditions are used with $V_{dQ} = 5, 10, 15$ and 20 V and $I_{dQ} = 9$ and 90 mA.

are given in Chapter 4. Few important observations can be made from the pulsed data. Cutoff voltage (V_{off}), R_{on} and subthreshold slope of the device, degrade severely as the device is stressed more i.e the off state gate to drain voltage is increased. This happens because of an increased electric field across the gate-drain electrodes, which causes more electrons to be injected from the gate that end up getting trapped in the surface states located in the access region. The electrons could also get trapped in the GaN buffer. Two well-known offshoots of trapping in GaN HEMTs have been reported - current collapse and knee-walkout. Current collapse refers to the reduction in the device saturation current under pulsed conditions whereas knee walk-out is the increase in the dynamic on resistance of a device for a particular steady-state gate bias condition under strong gate to drain electric field. It manifests in the form of an increased knee voltage (drain saturation voltage) in the pulsed $I_d - V_d$ characteristics. Both these effects vary significantly as functions of the quiescent bias condition as seen in Fig. 1.13(c) - 1.13(e). These bias conditions could be thought of as different bias classes in power amplifiers and under such circumstances, current collapse and knee walk-out could determine the dynamic load-lines, underlining the importance of having an accurate trap model to design first-pass RF power amplifier circuits.

1.4 Design considerations for Power GaN HEMTs

GaN devices are suitable for power applications due to the phenomenal material properties of GaN that facilitate GaN HEMTs with high breakdown voltage (V_{br}), low R_{on} , and lower total gate charge (Q_g). Shown in Fig. 1.14(a) is a comparison of specific on-state resistance ($R_{on} \times A$) versus V_{br} for different device technologies which indicate the superior values for V_{br} for a given R_{on} in GaN HEMTs, which is the primary reason for GaN devices having smaller footprints. Equivalently, low values of $R_{on} \times A$ for a given V_{br} ensure that ON state losses are minimized. Q_g , which limits the maximum obtainable switching speed, is also an important performance indicator as shown in Fig. 1.14(b). The product $R_{on} \times Q_g$, considered as a measure of switching efficiency, is seen to be almost two orders of magnitude smaller than

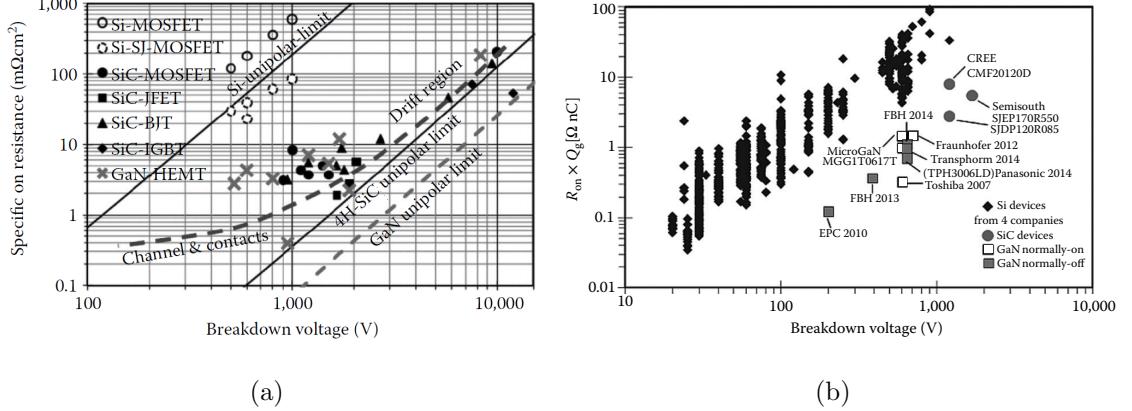


Figure 1.14: Comparison of (a) $R_{on} \times A$ vs V_{br} for different device technologies [29]. (b) $R_{on} \times A$, R_{on} and Q_g vs V_{br} for different device technologies [7]. The product $R_{on} \times A$, R_{on} gives an idea about the switching efficiency of the device which depends on the device losses during on state and the maximum obtainable switching speed, determined by R_{on} and Q_g respectively.

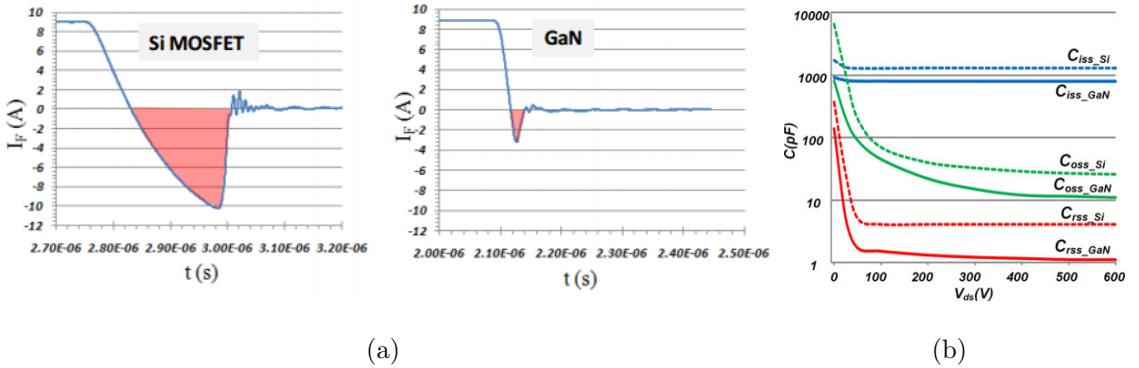


Figure 1.15: Comparison of (a) Q_{rr} [30] and (b) Terminal capacitances [31] for a Si power MOSFET and a GaN HEMT.

that for Si-based devices.

The absence of PN junctions in the device structure ensures that GaN HEMTs offer significantly less reverse recovery charge (Q_{rr}) in comparison to Si as shown in Fig. 1.15(a). Moreover, GaN HEMTs are planar in structure as compared to Si power MOSFETs which essentially are vertical devices. As a result, GaN HEMTs have lower terminal capacitances in comparison to their Si counterparts as illustrated in Fig. 1.15(b). Both these add-ons in GaN technology are instrumental in ensuring

high switching capability of GaN devices.

1.4.1 Field Plates

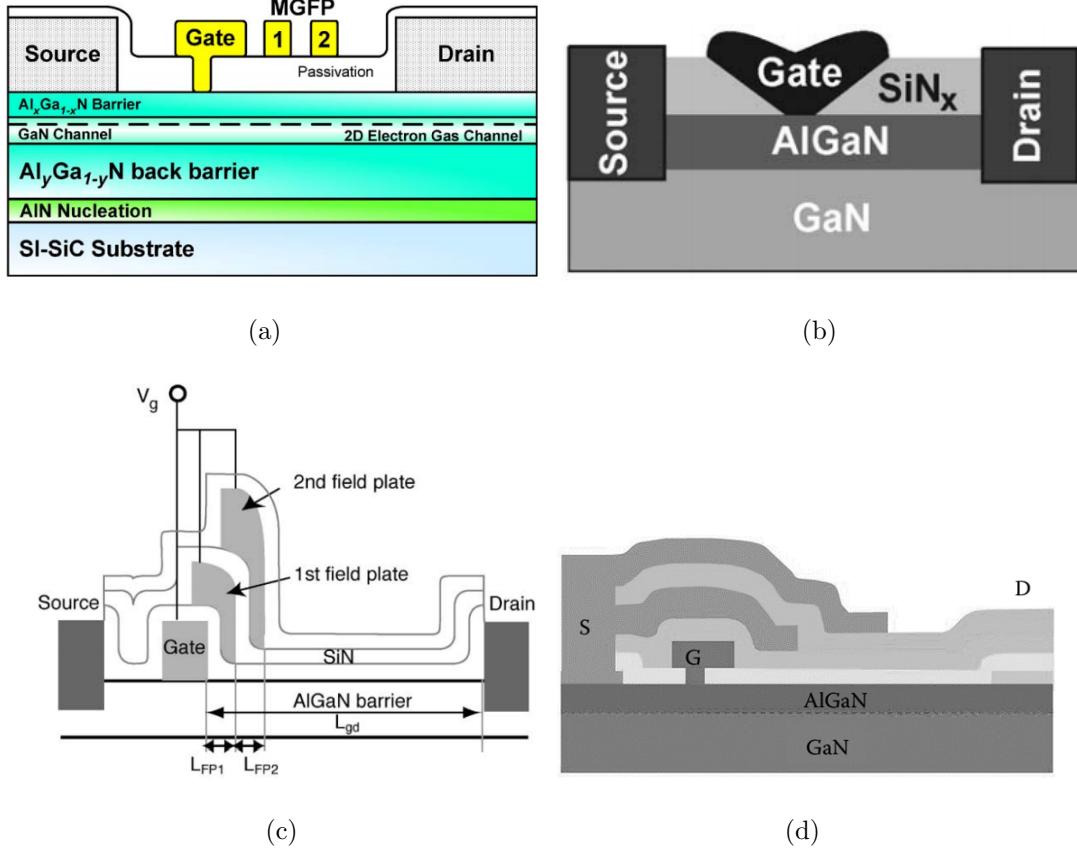


Figure 1.16: Various topologies (a) Multiple Grating FPs [32] (b) Slanted FPs [33] (c) Stacked Gate [34] and (d) Stacked Source FPs [7] in GaN HEMTs .

Field plates (FPs) have been extensively incorporated in GaN HEMTs like any other power device to enhance the V_{br} of the device by redistributing the electric field and therefore avoiding gate-actuated breakdown effects [35]. In recent times, GaN devices have undergone a lot of tailoring with regard to FP implementation in order to optimize performance. State of the art GaN power devices use various FP topologies as shown in Fig. 1.16. The various field plates in a multiple grating FP topology [32], shown in Fig. 1.16(a), can be biased at different potentials to customize field spreading. Slant FPs [33] prevent the peaking of electric field at termination points of FPs since the geometrical distance between the FP and the

channel region is progressively increased as shown in Fig. 1.16(b). Stacked FP layouts [34], as shown in Fig. 1.16(c) and 1.16(d), are also used in advanced devices to have multiple connected FPs to further increase V_{br} . However, it leads to increased inter-electrode capacitances which can be reduced by employing air-bridge type layout.

1.4.2 Modified Epitaxial Buffer Structures

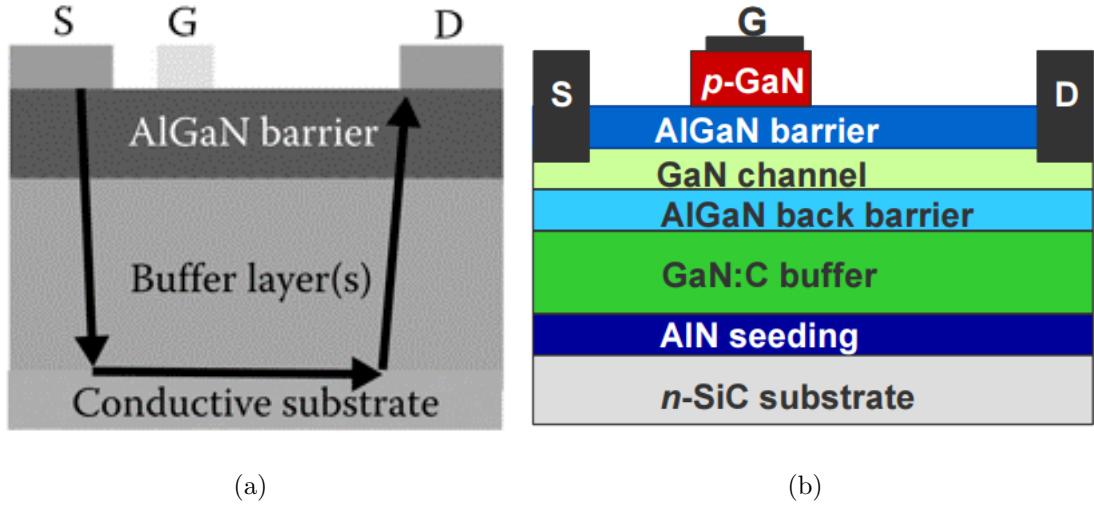


Figure 1.17: (a) Alternate conduction path provided by a conductive substrate (b) Blocking buffer layer deployed to separate the substrate and the GaN channel layer. The buffer layer is Carbon or Iron doped [36].

The substrate layer has a tendency to act as an alternate conduction path, as shown in Fig. 1.17(a), which is detrimental for normal device operation. It can lead to breakdown of the device vertically across the epitaxial layer stack. In order to prevent that from happening, advanced power devices take help of Carbon or Iron doped buffer structures with high vertical blocking strength to create a separation between the substrate and the GaN channel layer thereby minimizing leakage currents through them as illustrated in Fig. 1.17(b) [36]. However, there is a tradeoff that deserves some attention. An increased dopant concentration for better blocking capability comes at the cost of increased R_{on} , that limits the overall switching frequency.

1.4.3 Normally OFF Devices

GaN HEMTs are inherently normally ON in nature due to the existence of 2DEG at the AlGaN/GaN interface without applying any gate bias. This is an undesirable feature as far as power electronic circuits is concerned as it would lead to static power loss as well as it would also complicate the required gate-drive circuit. In order to circumvent this problem, a variety of approaches have been tried which are shown in Fig. 1.18 and summarized as follows:

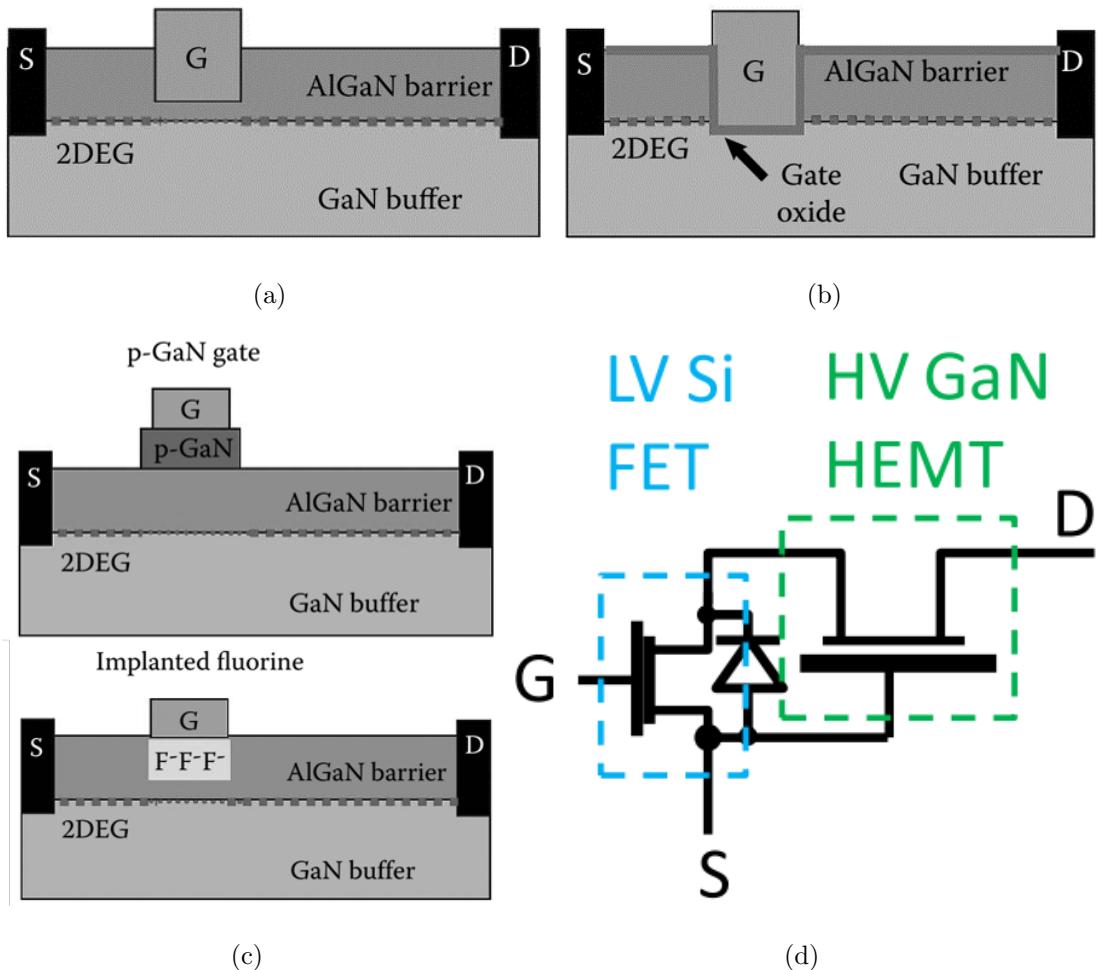


Figure 1.18: Various approaches towards realizing a normally OFF GaN device. (a) Recessed gate technique (b) Bulk inversion technique (c) Charge management technique and (d) Cascode structure technique [7, 37, 38].

1. A recessed gate approach [39], as shown in Fig. 1.18(a), is used in which the

thickness of the AlGaN barrier layer is kept lower than the critical thickness required for the formation of the 2DEG due to spontaneous and piezoelectric polarization, as was discussed earlier. As a result, a positive potential at the gate is required to cause bending of the GaN conduction band at the interface upon which 2DEG formation starts. This technique is often deployed in conjunction with a gate dielectric isolator technique to prevent any potential gate leakage due to recessing of the AlGaN barrier.

2. Complete removal of the AlGaN barrier is done, as shown in Fig. 1.18(b), where an inversion channel is formed upon applying positive gate bias. In this case the current is governed by the bulk properties of GaN and not the 2DEG, which is a significant drawback of the approach. The resulting transistor is only a GaN MOSFET and it is devoid of the fundamental advantages offered by a high density and high mobility 2DEG. It therefore bypasses the very motivation of using a HEMT structure in the first place.
3. A very useful approach that follows from charge neutrality principle is the placement of localized negative charges right below the gate region with the aim of depleting the region of 2DEG at zero bias. As shown in Fig. 1.18(c), a widely used technique involves the insertion of a p-type doped GaN or AlGaN layer between the channel and the gate metal [36]. At no applied gate bias, the inserted layer is depleted which leaves behind fixed negative charges in turn depleting the channel. Another popular method is by implanting fluoride ions underneath the gate which depletes the region of any 2DEG [38].
4. Finally, a more recent approach introduced is the cascode structure where a low voltage Si MOSFET is connected with a normally ON GaN HEMT in cascode configuration as illustrated by Fig. 1.18(d) [37]. The resultant effective transistor is an enhancement-mode transistor with the gate drive the same as that of a MOSFET, however, it requires the packaging of two switching devices in a leaded multichip package, which is its possible downside as it might not be cost effective [40].

1.5 Design considerations for RF GaN HEMTs

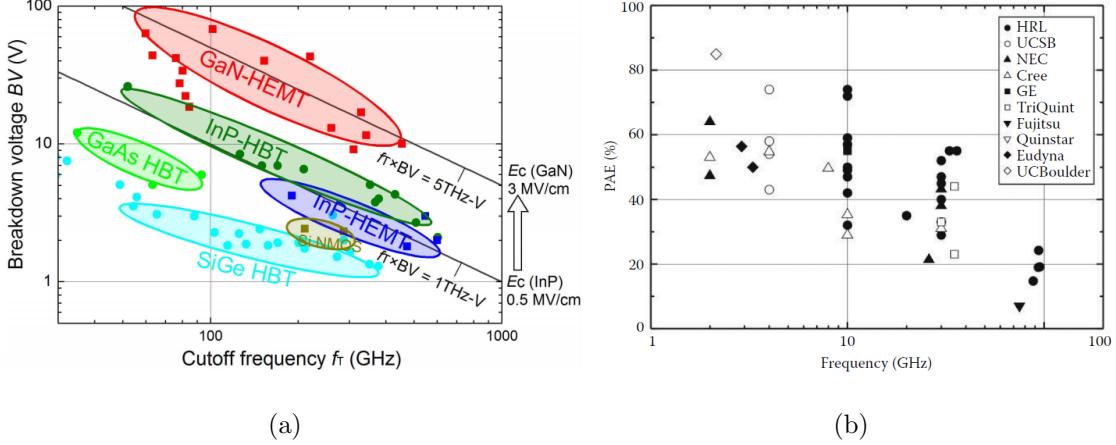


Figure 1.19: Comparison of (a) Breakdown Voltage [41] and f_T and (b) Power Added Efficiency of PAs using different technologies [7]. GaN based HEMTs are seen to have impressive numbers in comparison to device technologies from other material counterparts.

In the RF and microwave domain, GaN-based technology has emerged as formidable option to replace the GaAs-based technology which has reached its performance limits due to material constraints. The key requirements for a device to be considered suitable for RF circuit applications, particularly when the target applications include satellite and wireless communications, are low R_{on} , better linearity and superior values for transit frequency (f_T) and gain [42]. GaN HEMTs fulfill each of these requirements and do exceedingly well in terms of output power and power added efficiency (PAE) in comparison to other contemporary RF technologies such as GaAs pHEMTs, SiGe HBTs etc as shown in Fig. 1.19. Due to a very high carrier velocity in the 2DEG, GaN HEMTs achieve very high f_T values while offering low noise operation due to high gain facilitated by a high density 2DEG. Due to these exciting features, GaN-based RF power amplifiers (PAs) have been successfully demonstrated with state-of-the-art power levels such as 4 W at 15 GHz using Doherty architecture [43], 70 W at Ku Band [44], 20 W at S Band [45] and 60 W at X-Band under pulsed conditions [46].

While the GaN-technology qualifies as mature for the design of state-of-the-

art RF PAs, aggressive scaling of these devices is essential to reduce the electron transit time and thereby boosting f_T . Some important device scaling features for high frequency operation are summarized in Fig. 1.20 [7], which include lateral and vertical scaling to minimize electron transit time and short channel effects respectively, parasitic resistance and capacitance minimization and surface passivation for current collapse mitigation. It should be noted that the requirements for V_{br} in an RF device are less stringent than power devices since higher V_{br} would entail larger size of the device which would translate into larger values of parasitics.

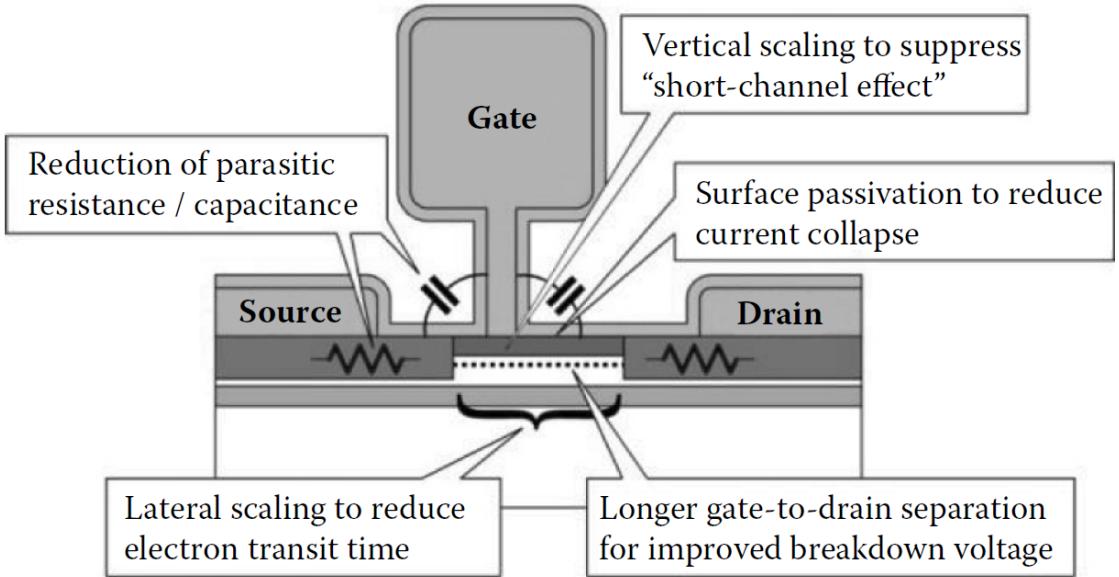


Figure 1.20: Device scaling features for RF operation. It includes vertical and lateral scaling, T-shaped gates, surface passivation and regrown ohmic contact technology [7].

Here, we are going to briefly discuss the conventional design considerations to improve RF device performance, which are:

1.5.1 T-Shaped Gates and Lateral Scaling

Gate resistance (R_g) is a key determinant of the f_T and noise performance of a microwave transistor. As such, T-shaped gate, as shown in Fig. 1.21, is used, which offers the advantage of having a broad overlying gate head to achieve low R_g while

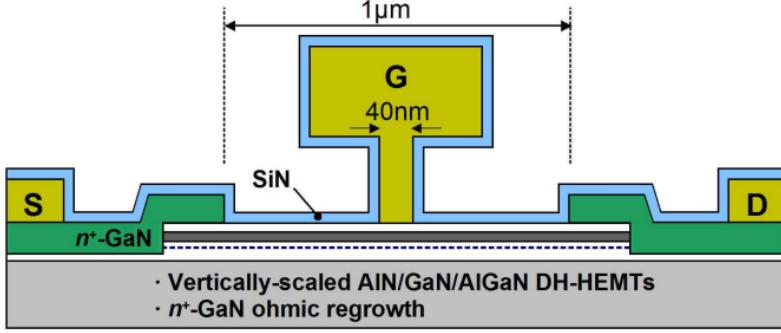


Figure 1.21: Conventional T-shaped gate used to minimize R_g and $C_{p,T}$ [41].

scaling down the gate length (L_g) [41]. However, in the process of aggressively scaling down the T-shaped gate, fringing capacitances ($C_{p,T}$) associated with the T-shaped gate become pretty significant. This calls for an optimized T-gate in terms of its height and width such that R_g and $C_{p,T}$ are both minimized.

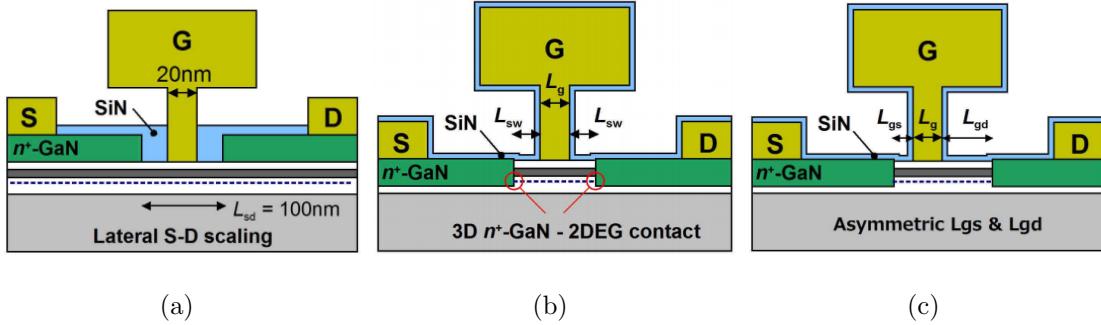


Figure 1.22: Different generations of T-gates used to minimize parasitic capacitances [41]. (a) Self-aligned-gate technology (b) Ohmic contact regrowth technique (c) Asymmetric self-aligned-gate.

Lateral scaling of the devices is essential to boost up the f_T and f_{max} limits of the GaN device by reducing the electron transit delay. Shown in Fig. 1.22(a) to Fig. 1.22(c) are the various successive improvisations in the lateral scaling. Self-aligned-gate technology was used, as illustrated in Fig. 1.22(a), to enable lateral scaling of the source-drain distance (L_{sd}) to suppress drain delay. Using SiN sidewall spacers, an ultrashort gate gets in self-alignment with the source and drain contacts. The topology in Fig. 1.22(b) advances ohmic contacts where a direct contact of 3-D n^+ -GaN to 2DEG is realized. This is known as the ohmic contact regrowth

technique. Finally, in order to accommodate high breakdown fields, moderate L_{gd} and short L_{gs} is preferred as shown in Fig. 1.22(c). This is made possible by an asymmetric self-aligned-gate technology where L_{gs} and L_{gd} are independently controlled to get a balance between high V_{br} and speed.

1.5.2 Vertically Scaled Epitaxial Structure

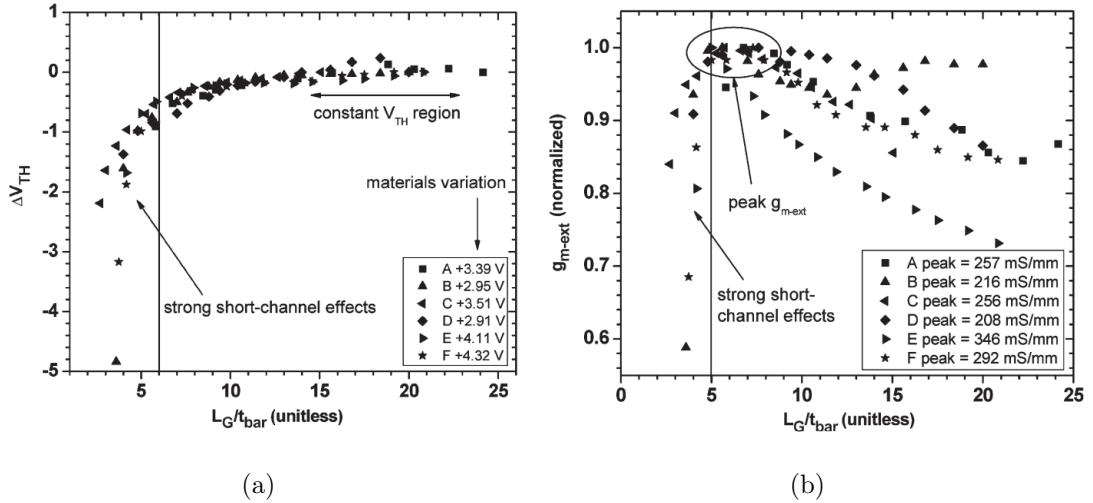


Figure 1.23: (a) V_{off} and (b) g_m as functions of aspect ratio L_g/t_{bar} , indicating the constraint on L_g/t_{bar} during scaling to prevent short channel effects [47].

As an offshoot of lateral scaling of the device, short channel effects in the form of negative shift in V_{off} , reduced g_m , enhanced values for g_{ds} and drain-induced barrier lowering (DIBL) are observed [47]. This necessitates the scaling down of the various epitaxial layers in the GaN device to gain gate control while progressively scaling the device laterally. Fig. 1.23 shows the variation of V_{off} and normalized g_m as a function of the aspect ratio (L_g/t_{bar}), where t_{bar} is the gate to channel distance. The severe V_{off} shift and g_m degradation for low values of L_g/t_{bar} beyond a certain limit makes it essential to vertically scale the device epitaxial layers in order to avoid these short channel effects.

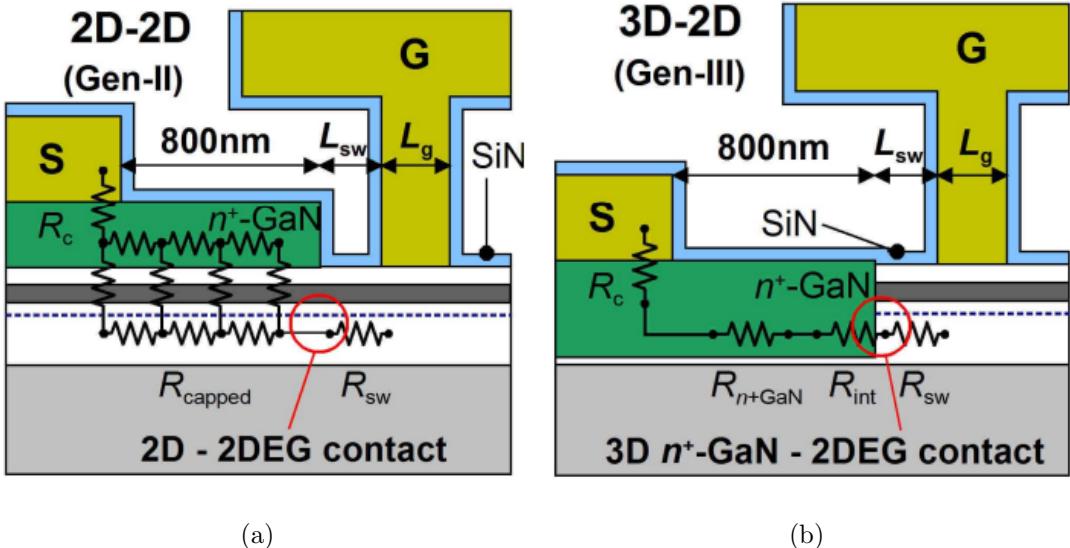


Figure 1.24: Regrown ohmic contacts in (a) 2D-2DEG and (b) 3D-2DEG structures in a GaN HEMT. The interfacial resistance in (a) leads to a higher access resistance in comparison to (b) [41].

1.5.3 Regrown Ohmic Contacts

Regrown ohmic contacts are used for lower source and drain contact resistances as compared to the conventional alloyed ohmic contacts, where a high AlGaN potential barrier is the bottleneck to reducing parasitic resistance proportional to device size scaling. In regrown ohmic contact, n^+ GaN establishes a contact with the 2DEG, leading to a minimal interfacial resistance. These contacts can be deployed in two possible topologies as shown in Fig. 1.24. In the first case, n^+ GaN is regrown on top of the AlGaN barrier, as shown in Fig. 1.24(a). The 2DEG in this case gets in contact with the source 2DEG and there exists a finite access region resistance between the n^+ GaN and the 2DEG. In the second case, as shown in Fig. 1.24(b), the 3D n^+ GaN is direct contact with the 2DEG, thereby supplying the electrons, which leads to lower access region resistance and therefore higher f_T and f_{max} .

1.6 Motivation and Thesis Outline

Now that a brief introduction to the GaN technology and its strong potential for contemporary applications in the power-electronics and RF has been made, it is essential to outline the fundamental objectives of this thesis. While the primary goal of this thesis is to present a single state-of-the-art GaN HEMT Model that could cater to the needs of GaN-based high power and RF circuit designers, a considerable portion of this doctoral work also focuses on the analysis of various GaN device physical phenomena. The thesis is aimed to provide a useful modeling tool and as such it has been structured in a smooth manner going all the way from device physics to model development and parameter extraction. The key objectives identified for this research work are given below:

- Development of a physics-based capacitance model for GaN devices with multiple field-plates. It should be able to accurately reproduce the transient waveforms when used in a switching circuit.
- Demonstration of an end to end RF modeling solution for GaN HEMTs all the way from small-signal to large-signal considerations. Since GaN HEMTs are known to exhibit nonlinear phenomena such as trapping, thereby necessitating a working trap model. Moreover, a systematic parameter extraction flow would be needed before the model actually be used in circuit design.
- Large gate-periphery GaN devices due to their inherently large capacitances and their interaction with the device inductances present an opportunity for the development of alternate parameter extraction methodologies for such devices.
- To gain mathematical understanding of the stability aspect of large gate-periphery GaN HEMTs.
- To gain mathematical insight of kink-effects observed in high frequency device characteristics such as h_{21} and S_{22} and use that to model those effects.

The remaining portion of the thesis has been organized into the following six chapters.

We start with a brief introduction to contemporary GaN HEMT compact models available in the industry in **Chapter 2**. Two models, namely Angelov Model and the MIT Virtual Source GaN HEMT (MVSG) Model, are reviewed to introduce the reader to the type of modeling approach they are constructed around. The former is a purely empirical model while the latter is based on the underlying device physics. The status of the GaN HEMT standardization activity at the CMC is also briefly touched. From an industry point of view, the key requirements for an industry standard model are also discussed. A background of the Advanced SPICE Model for GaN HEMTs (ASM-GaN-HEMT) is given which most of the work in this thesis is carried out.

In **Chapter 3**, surface-potential calculation of the ASM-GaN-Model is used to compute intrinsic charges, and therefore the capacitance contribution, in a dual field-plate GaN HEMT. Numerical simulations are performed for better understanding of capacitance behavior and mixed mode transient simulations are done for further evaluation of the model in a switching circuit. Moreover, validation of capacitance model is done against measured data of state-of-the-art power GaN devices for multiple bias and temperature conditions.

In **Chapter 4**, we report an end to end GaN HEMT based RF modeling solution all the way from DC parameter extraction to simulating large-signal drive-up simulations using a physics-based model. A step-by-step small-signal model extraction procedure is demonstrated which is extensively validated over broad-band S-parameters of commercial RF GaN devices. The RF extraction procedure proposed in this portion of the thesis is distinct from the existing models and very useful from a model user's point of view since it involves the tuning or adjustment of only a handful of parameters, which is primarily facilitated by the strong physical background of the model. A working trap-model, extracted from pulsed-IV measurements, and self-heating model are included in order to realize a more realistic model. Load-pull and harmonic balance simulations are performed to benchmark

the model performance at large-signal RF excitation against corresponding measured data for a state-of-the-art RF GaN device. In addition, statistical simulations are also performed to identify possible causes of variability in a batch of 10 GaN devices.

Certain interesting features are exhibited by large gate-periphery GaN devices due to their large capacitance values and their subsequent interaction with the device inductances. We exploit these features to formulate a novel RF parameter extraction procedure in **Chapter 5**, which differs from the existing methodologies in literature. The primary objective of this methodology is to extract the model using a single set of measured S-parameters, without needing to de-embed the contribution of extrinsic bus-inductances. Additionally, a study on the stability performance and its modeling is also carried out in this portion of the thesis. It is mathematically shown that high via-inductances lead to certain dips in stability as a result of their coupling with the intrinsic drain to source capacitance.

h_{21} and S_{22} are important RF figures of merit. h_{21} determines the f_T of a microwave device while S_{22} is important for the determination of the output matching network. Kink-effects in both these figures of merit have been reported in literature calling for their analysis which could be of importance to RF designers, both in the device and circuit domain. In **Chapter 6**, we analyse and model both these kink-effects using mathematical expressions which are further used to study the impact of various model elements on the location and severity of these kink-effects.

Lastly, in **Chapter 7**, the key accomplishments of the thesis are summarized along with possible extensions and future scope of the research work carried out in the thesis.

Chapter 2

GaN Models and Industry Standardization Status

2.1 Introduction

Semiconductor device model development bears a lot of significance in the micro-electronics industry given the fact that it is an essential ingredient for the design of circuits and devices. A device model can be utilized to direct advanced semiconductor devices all the way from fabrication to first-pass design. In addition, device models provide feedback which is of paramount importance as far as device process advancement and circuit design optimization is concerned [48]. This underlines the importance of the field of device modeling which is a very powerful tool for the streamlining of device technologies and corresponding application circuit performance.

Compact models for semiconductor devices are models whose incorporation in SPICE circuit simulators is relatively simple while being accurate at the same time [49, 50]. These models replicate the device terminal characteristics such as intrinsic currents, capacitances etc. to gain insight into device behavior. Compact models are of great use to circuit designers as well as to technology developers as they use the physical background of compact models to fine-tune the device process steps. Compact models, which are rigorously used by the industry, are therefore

supposed to possess certain qualities for wide-scale use. They need to be fast, accurate and robust with simple extraction methodologies. Scalability property of compact models with regard to geometry, temperature etc. is always a welcome feature which is only possible if the compact models are physics-based in nature. Such models are very handy in being predictive about future device technology nodes as well as in studying their statistical behavior due to process variability.

As was discussed in the previous chapter, GaN HEMTs have made tremendous progress and are making way into the power-electronics and RF circuit domain. While this technology is continuously evolving towards becoming a mature technology, it is imperative for modeling engineers to come up with high fidelity models so that the benefits of this technology could be translated into viable circuit applications. The task of a modeling engineer is a daunting one as it requires expertise of the device physics, different types of characterization and a know-how of various data processing and parameter-extraction software packages.

In view of the potential GaN market, the CMC, which is a consortium of semiconductor companies and Electronic Design Automation (EDA) vendors, has taken up the responsibility of providing industry standard compact models for GaN HEMTs suitable for multiple SPICE modeling frameworks [51]. It has also stipulated certain key features [51] that are deemed to be desirable in a GaN HEMT industry standard model which are enumerated as follows:

1. First and foremost, the model should be physical with dependence on geometrical dimensions.
2. The model should be accurate in capturing the terminal charges and currents for all working modes, including the high-power and sub-threshold regions. Charges and currents need to be modeled accurately across a wide temperature range, with self-heating enabled using a thermal node.
3. The charge model needs to be charge based (in contrast to capacitance based) and charge conserving.
4. Charge and current needs to be self-consistently derived using the same charge

formulation.

5. An accurate model for the Schottky gate currents should be included, just like all the physical noise sources.
6. The model should pass the standard benchmarking Gummel and McAndrew symmetry tests.
7. Since GaN HEMTs are often plagued with trapping effects, the model should be capable of reproducing dynamic trapping effects.
8. The model should feature an accurate representation of the parasitic, bias-dependent resistances and capacitances, taking the true asymmetry of the device into account.
9. The standard model needs to have the capability to model field plates, and large periphery or unit gate width scaling for both trapping and mechanical stress effects.
10. Lastly, and more importantly, the model needs to show good convergence in circuits of an appropriate scale, for both frequency and time-based simulation.

Over the past five years or so, there has been a burst of models for GaN HEMTs for both the application domains, most of which are empirical, table-based, behavioral or neural network based while there are few physics-based or analytical models as well [52–65]. In this chapter, we touch upon the available compact models in the industry and the recent GaN model standardization activity.

2.2 Available Models in Literature

A great deal of research effort has been put forth in the development of GaN HEMT compact models. Most of the RF GaN HEMT models are upgrades of the GaAs FET models, aimed for III-V RF circuit design [66]. However, these models fall short of the desired accuracy in case of GaN HEMTs due to various sources of nonlinearities

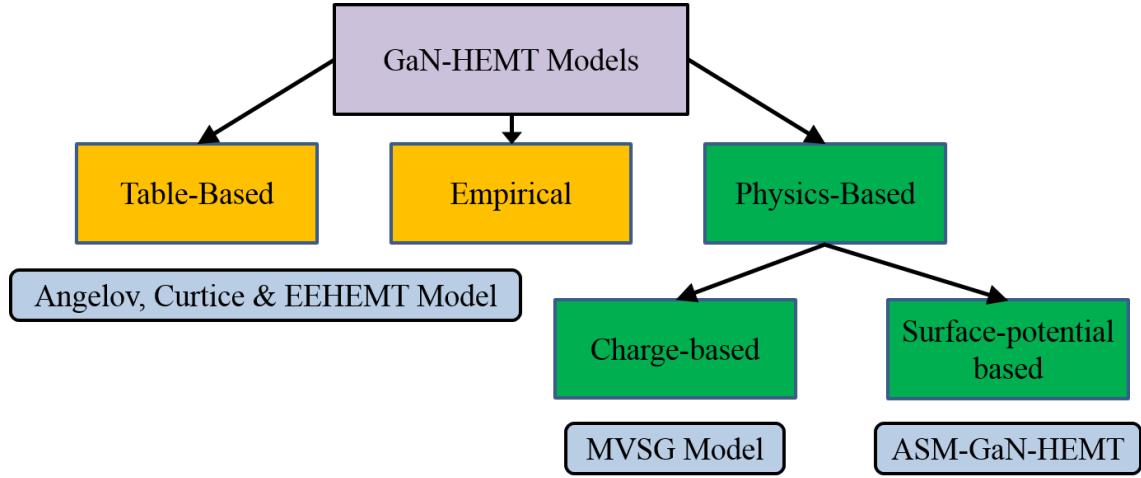


Figure 2.1: Classifications of various GaN HEMT models in the industry. Angelov, Curtice and EEHEMT are the popular empirical models whereas MVSG and ASM-GaN-HEMT models are the recent models that have been considered for industry standardization.

which demands compact models developed while considering the various behavioral nuances in GaN HEMTs [66].

The existing GaN HEMT compact models can be categorized into table-based, empirical and physics-based compact models as illustrated in Fig. 2.1. Table-based models are constructed using device measurements. While these models are accurate, the problem with these models is that they are not predictive and they require complex interpolation functions for the model to work for bias conditions that do not have measured data entries. Empirical models on the other hand are fast and accurate as well, however, they are derived by fitting measured data using mathematical expressions which do not preserve the underlying device physics. Such models usually tend not to be scalable and therefore require a huge number of fitting parameters which complicates the parameter-extraction process. Angelov model [67], Curtice model [68] and EE-HEMT model [69] are the well known empirical models that have so far been used as model standards for GaN HEMTs.

Recently, the interest towards physics-based GaN HEMT compact models, particularly surface-potential based models, has grown in light of the commercial potential of GaN in RF and power-electronic applications and the industry is looking

for them for multiple reasons [51, 66]. First, GaN technology is still on a trajectory towards maturation and a physics-based model would help a great deal in the device design and therefore in the evolution of the GaN technology itself. Second, a physics-based model offers a relatively smaller set of parameters whose flow of extraction is simple and can be related to the intrinsic device physics, leading to a more meaningful model card. Finally, physics-based models are inherently scalable with regard to bias, temperature or geometry, which can be of significance to RF circuit designers so that they can explore a wider design space. Lately, two compact models were chosen by the CMC as standards and to be integrated into commercial SPICE simulators for industrial use. They are MIT Virtual-source GaN HEMT Model (MVSG Model) and our Advanced SPICE Model for GaN HEMTs (ASM-GaN-HEMT Model).

2.2.1 Angelov Model

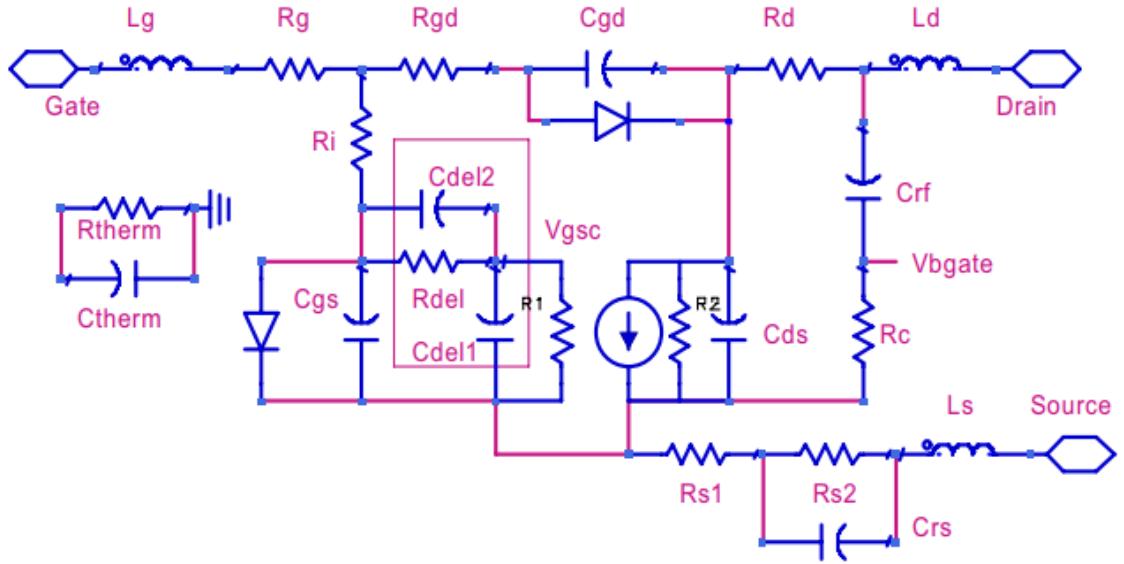


Figure 2.2: Equivalent circuit model of Angelov GaN HEMT model [70].

A very popular model for GaN HEMTs is the Angelov GaN HEMT model [67, 70–75]. It is constructed as a sub-circuit model whose equivalent circuit representation is shown in Fig. 2.2. The key model expressions are reproduced here while a thorough description of the model can be found in [70]. For the drain current, it

employs a $\tanh()$ function to replicate the bell-shaped g_m , given as

$$g_m = g_{mpk}(1 - \tanh^2[p_{1m}(V_{gs} - V_k)]) \quad (2.1)$$

where g_{mpk} , p_{1m} and V_k are fitting parameters. The current is calculated as

$$I_{ds} = I_{pks}(1 + \tanh(\psi_p))\tanh(\alpha V_{ds})[1 + \lambda V_{ds}] \quad (2.2)$$

where I_{pks} and λ are fitting parameters and ψ_p is a power series given as

$$\psi_p = P_1(V_{gs} - V_{pk}) + P_2(V_{gs} - V_{pk})^2 + P_3(V_{gs} - V_{pk})^3 \quad (2.3)$$

where P_1 , P_2 and P_3 are parameters and V_{pk} is gate voltage for maximum g_m .

The intrinsic capacitances (C_{gs} , C_{gd} and C_{ds}) are also computed in terms of ψ as

$$C_{gs} = C_{gsp} + C_{gso}(1 + \tanh(\psi_1))(1 + \tanh(\psi_2)) \quad (2.4)$$

Clearly, it can be observed that this model gives the model user no idea about the device physics whatsoever which makes it difficult to perform the parameter extraction for a particular set of measured data.

The Angelov model has been updated regularly to fit as much measured data as possible, nevertheless, the model is not predictive and as a result presents a challenging task to use it for an array of devices, which is its major drawback in addition to lacking model symmetry due to its empirical nature. Additionally, the Angelov model does not cater well towards capturing nonlinear effects due to trapping. The Angelov model made it to the final four candidates for GaN standardization but due to the above mentioned shortcomings, couldnt fare well beyond that. [76].

2.2.2 MVSG Model

The MVSG model is one of the two recent physics-based compact models that were chosen as industry standard [76]. The MVSG model is charge-based in nature

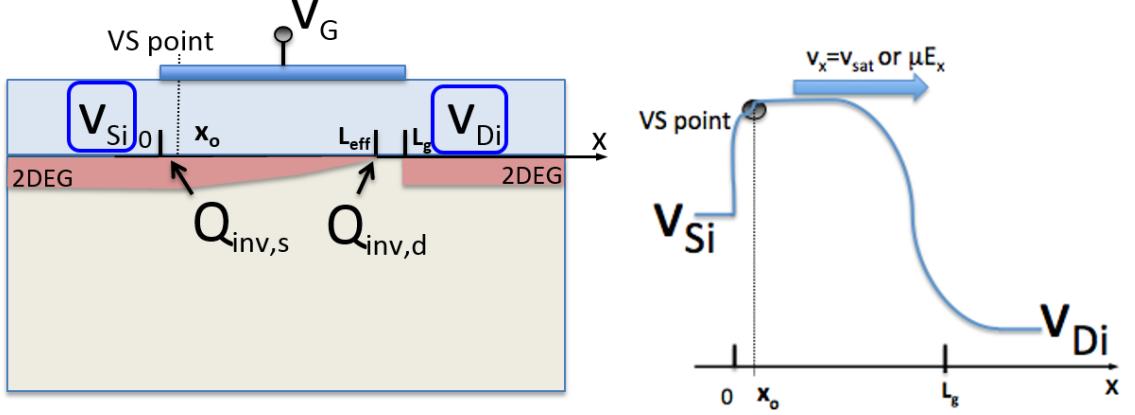


Figure 2.3: (a) Cross section schematic indicating the virtual source and the inversion charges ($Q_{inv,s}$ and $Q_{inv,d}$). (b) Band-profile cartoon to illustrate the VS approach [77].

[77] and passes most of the quality benchmarks of an industry standard model as prescribed by the CMC. It is based on the virtual source (VS) model concept, as illustrated in Fig. 2.3, in which the current in transistor under saturation regime is evaluated as a product of the areal density of charge at the VS ($Q_{i,xo}$) and the injection velocity (v_x) of electrons VS.

The expression for current is given as

$$I_d = W Q_{i,xo} v_x F_{sat} \quad (2.5)$$

where

$$Q_{i,xo} = C_g \eta \phi_t \ln \left(1 + \exp \left[\frac{V_{gx} - (V_T - \alpha \phi_t F_f)}{\eta \phi_t} \right] \right) \quad (2.6)$$

An empirical function (F_{sat}), as given below, is used to smoothly transition from linear to saturation regime.

$$F_{sat} = \frac{V_{ds}/V_{DSAT}}{\left[1 + (V_{ds}/V_{DSAT})^\beta \right]^{1/\beta}} \quad (2.7)$$

The MVSG model has been successfully validated against measured data for DC and RF characteristics [78] and is all set to serve as an industry standard GaN

HEMT model. The other physics-based model that has been chosen to be the GaN HEMT model standard is the ASM-GaN-HEMT model, which is explained in the next section.

2.3 ASM-GaN-HEMT Model

It is a surface-potential-based GaN HEMT compact model that has passed the CMC standard qualification benchmarks after repeated testing and evaluation by various industry players [76]. It has been developed jointly at the Indian Institute of Technology Kanpur, India and Macquarie University, NSW, Australia. This model, like the MVSG, also promises to cater to both the domains of the GaN microelectronics market i.e RF and power-electronics.

2.3.1 ASM Model Core

The fundamental premise of this model is the evaluation of quasi Fermi-level (E_F) as a function of bias in the triangular quantum well at the AlGaN/GaN heterojunction. The following expressions relate E_F and the charge density n_s , which are and outcome of Schrodinger's equation and voltage balance across the AlGaN/GaN heterojunction respectively [79].

$$n_s = DV_{th} \left[\ln \left[\exp \left(\frac{E_F - E_0}{V_{th}} \right) + 1 \right] + \ln \left[\exp \left(\frac{E_F - E_1}{V_{th}} \right) + 1 \right] \right] \quad (2.8)$$

$$n_s = \frac{\epsilon}{qd} (V_{go} - E_F - V_x) \quad (2.9)$$

$$E_{0/1} = \gamma_{0/1} n_s^{2/3} \quad (2.10)$$

where D is the density of states, V_{th} is the thermal voltage, E_0 and E_1 are the two sub-bands being considered within the quantum well, γ_0 and γ_1 are experimentally determined parameters, d is the thickness of the AlGaN barrier, V_{go} is the gate overdrive voltage $V_{gs} - V_{off}$ and V_x is the channel potential at any point x in the

transistor.

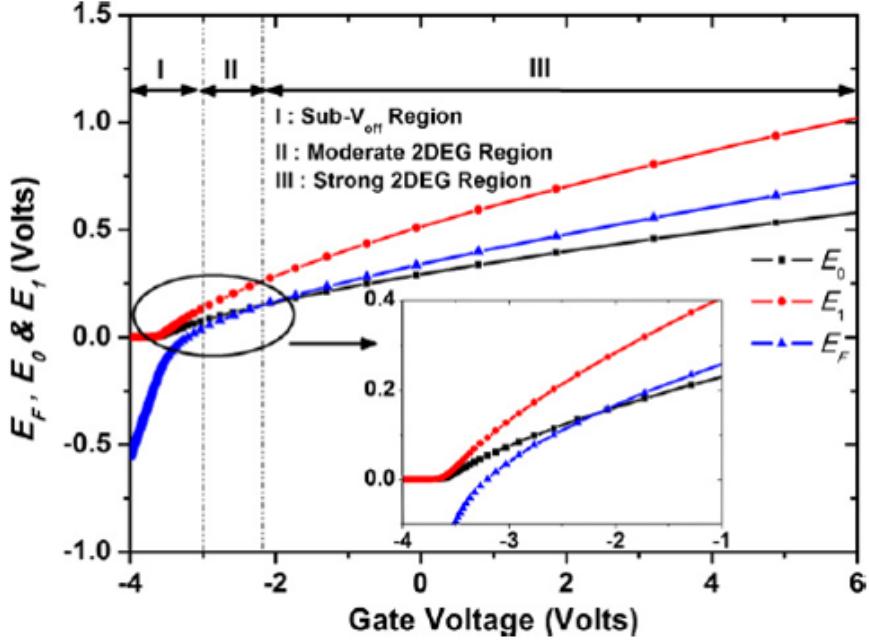


Figure 2.4: Numerical simulation plots for E_F , E_0 and E_1 as V_{gs} is varied. Regions I, II and III are identified based on weak, moderate and high 2DEG density due to relative position of E_F with respect to sub-bands E_0 and E_1 [80].

While it can be understood from the above set of expressions that they are transcendental and therefore cannot be solved analytically, attempts have been made to solve them by starting with certain approximations for E_F , albeit with limited accuracy [79, 81]. A more viable approach was followed by Khandelwal *et al.* [80] in which solution for E_F is derived based on relative position of E_F in comparison to E_0 and E_1 for different bias regions, as shown in Fig. 2.4, and combined into a unified expression as under [80]

$$E_{F,unified} = V_{go} - \frac{2V_{th} \ln(1 + e^{V_{go}/2V_{th}})}{1/H(V_{go,p}) + (C_g/qD)e^{-V_{go}/2V_{th}}} \quad (2.11)$$

This physical quantity, i.e $E_{F,unified}$, henceforth referred to as E_F , is used to evaluate surface potential as $\psi_x = E_F + V_x$, which is further used to calculate device quantities such as charges and currents.

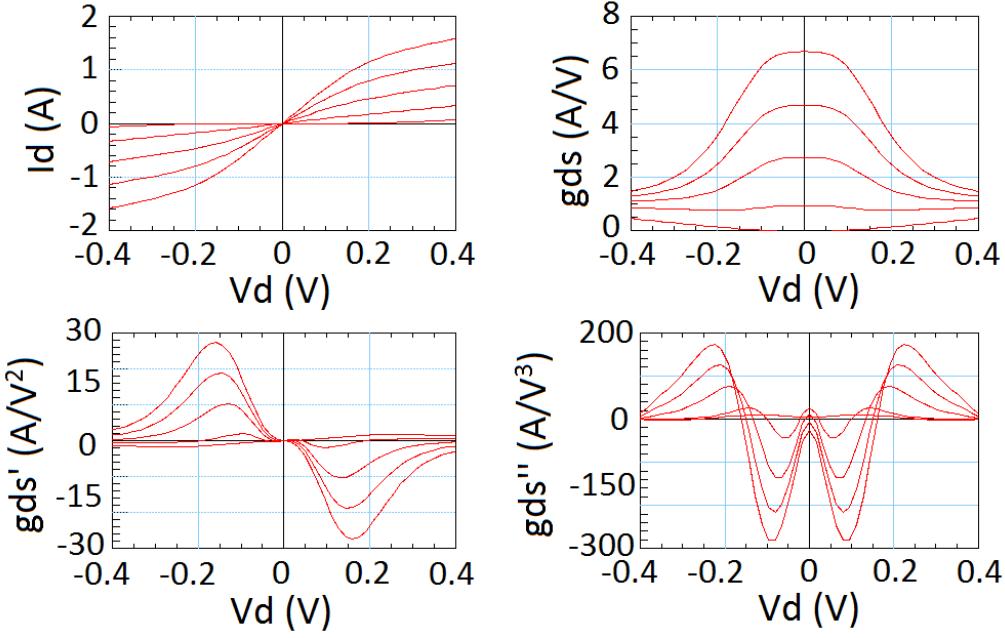


Figure 2.5: Gummel symmetry test showing smooth and symmetric intrinsic current and its multiple order derivatives for the intrinsic $10 \times 90 \mu\text{m}$ GaN device.

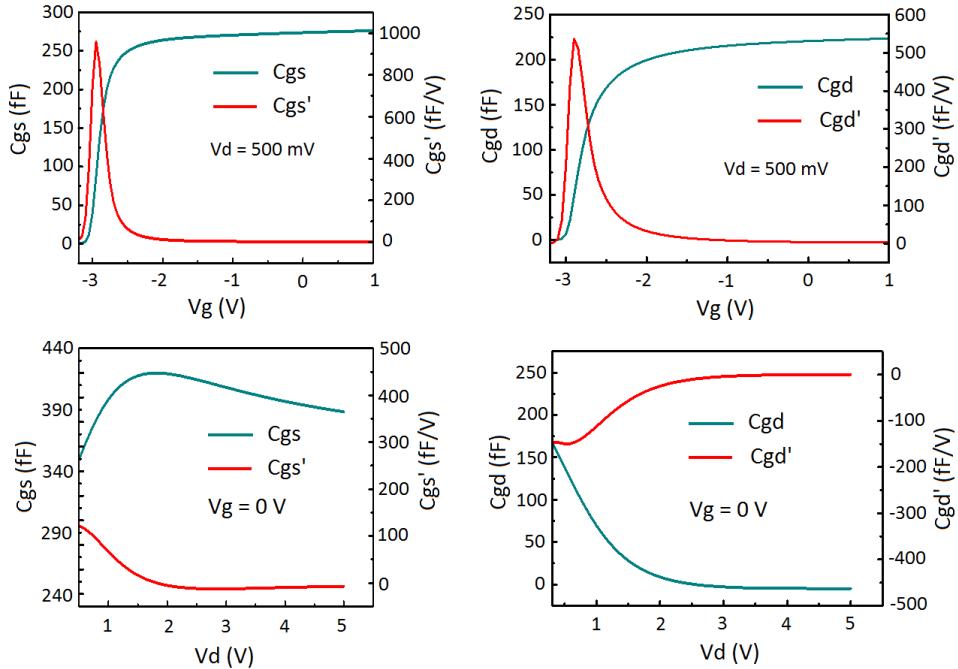


Figure 2.6: Smooth intrinsic capacitances C_{gs} and C_{gd} and their derivatives C'_{gs} and C'_{gd} for the intrinsic $10 \times 90 \mu\text{m}$ GaN device.

2.3.2 Model Performance and Quality

The ASM-GaN-HEMT model fulfils most of the requirements of an industry standard [51]. It is accurate, fast and robust at the same time. Shown in Fig. 2.5 are the gummel symmetry test results which show smooth and symmetric curves for intrinsic current and its successive derivatives for the $10 \times 90 \mu\text{m}$ device. Also, shown in Fig. 2.6 are the smooth intrinsic capacitances and their derivatives for the same device. The model is made more realistic by adding various real device effects.

In this chapter, an introduction to the state-of-the-art GaN compact models available in the industry was given. A review of the conventional GaN models was done where it was pointed out that the Compact Model Coalition is very particular about choosing a physics-based model as a standard due to various advantages offered by physics-based models. The ASM-GaN-HEMT model was also introduced around which most of the work done in this thesis has been carried out, as discussed in the subsequent chapters.

Chapter 3

Modeling and Analysis of Capacitances in GaN HEMTs with Field-plates for Power Electronics Applications

3.1 Introduction

GaN HEMTs are promising to be the workhorse of the future power-electronic and power-management industry, owing to the excellent material properties of the GaN [3, 82–84] such as high values of low-field mobility, saturation velocity, breakdown electric field etc. to name a few. They have asserted their dominance in power converters and high voltage power switches since the Baliga Figure of Merit (BFOM) [85], which is a benchmark metric of performance for power devices, is highly superior for GaN HEMTs than its other material counterparts [82].

It was demonstrated that after incorporating a field-plate (FP) structure in a HEMT, its V_{br} increases which could be maximized with proper optimization of FP length and insulator thickness [35, 86]. Huang *et al.* studied the impact of FPs on trapping behaviour and current collapse mitigation [87] while Chiu *et al.* investigated the impact of varying the length of FPs and gate-to-drain exten-

sions on electrical characteristics [88]. Although FP-HEMTs exhibit lower f_T due to increased gate-to-drain (C_{gd}) and drain-to-source (C_{ds}) capacitances after incorporating gate-connected FP (GFP) and source-connected (SFP) respectively, they show improved breakdown voltage, linearity, stability, reliability and efficiency [82]. In order to push the breakdown voltages of these GaN-based devices further towards the higher side, a lot of device structure tailoring has happened over the years in terms of FP incorporation such as air-bridges [89], slant FPs [33], multiple FPs [32, 34] etc. These evolved structures lead to complexities in the capacitance behavior which may significantly affect the switching performance of these devices. The terminal capacitances i.e. the input (C_{iss}), reverse (C_{rss}) and output (C_{oss}) capacitances, determine the power losses in power switching circuits [90]. Moreover, the C-V profiling gives an idea about the distribution of charge carriers within the material.

For production level tape-out of power-electronic circuits based on advanced Power GaN FP structures, there is an immediate need for an efficient and accurate compact model for GaN HEMTs in order to accomplish accurate and fast simulation. Both these metrics of circuit simulation i.e. the accuracy and speed are determined by the device compact model. Existing literature reports about studies carried out on FP capacitances and their modeling in GaN devices; however, a fully physics-based model without making any compromise on the accuracy is still a hot topic of research [77, 91]. A lot of models have been proposed for GaN HEMTs but they are not physics-based in nature [66, 70]. Physics-based models demonstrated earlier made extensive use of numerical techniques for calculation, hence making computation slower [92], while other models were based on MOSFET's equations and ignored the quantum nature of the 2DEG [93]. Curve-fitting with datasheet [90, 94] and look-up table based [95] methods are already reported to evaluate the terminal capacitances. Recently, Zhang *et al.* modeled the capacitances for Al-GaN/GaN HEMTs but in their analysis they didn't consider the impact of FPs [96]. Cucak *et al.* presented a physics-based analytical model; however, it is significantly inaccurate in predicting the cut-off voltage for the FP while compromising on fitting the capacitance plateaus with measured data [97]. This sets the primary motivation

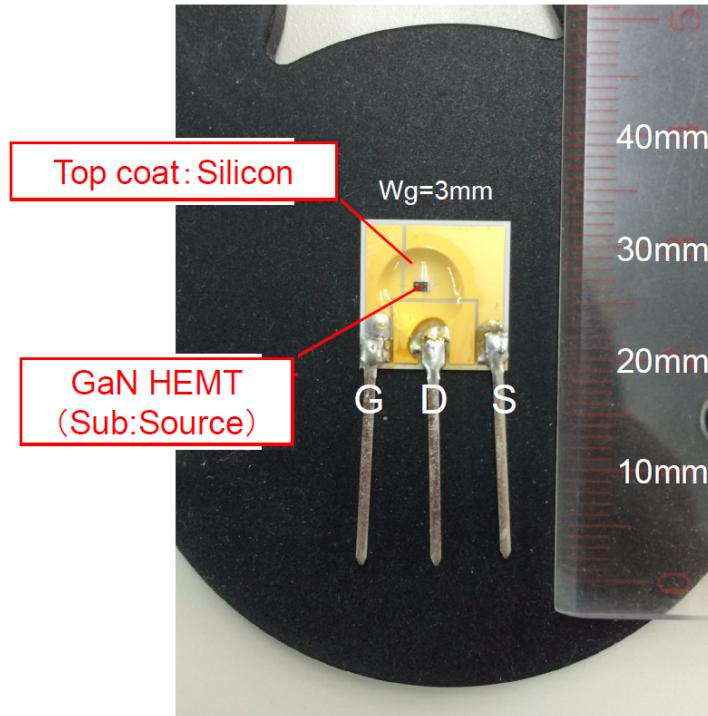
to come up with a FP capacitance model that is based on the underlying device physics. We also use technology computer aided design (TCAD) simulations for analysis, which provides insight to be subsequently used in the model development. To the best of our knowledge, this is the first time a surface-potential (SP) based model for FP capacitance in AlGaN/GaN HEMTs is reported.

3.1.1 Device Description

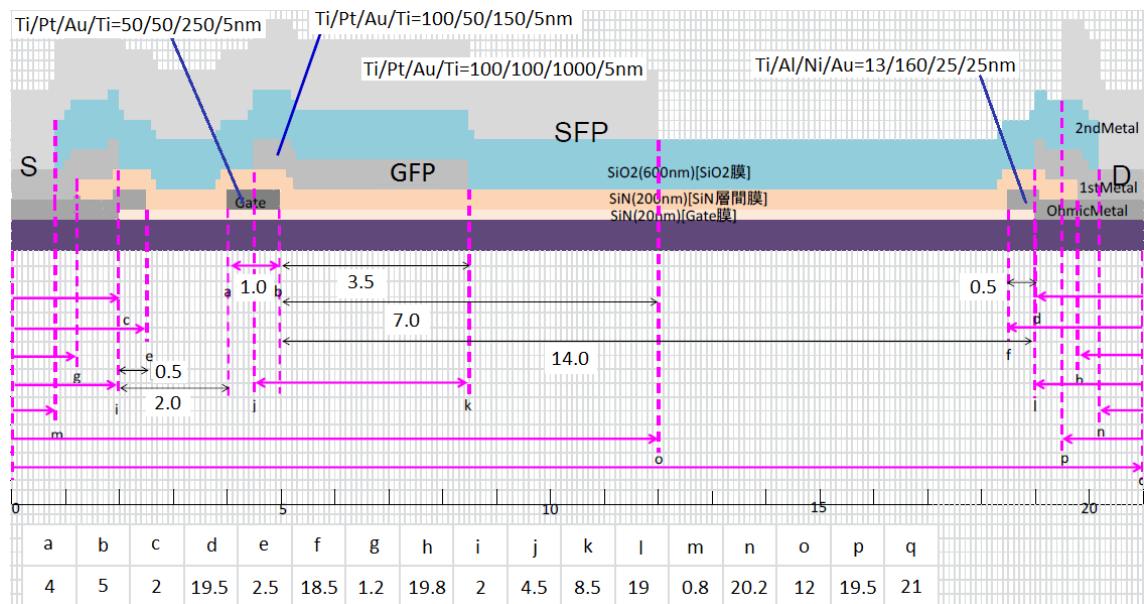
Fig. 3.1(a) shows the device under test (DUT) which is a commercial GaN on Si power device with gate width ($W = 3$ mm) put on direct copper bond board. It has a dual FP structure with GFP and SFP. Shown in Fig. 3.1(b) is a cartoon of the device which bears the following information - the configuration and arrangement of FPs, the respective dimensions of FPs, thicknesses of passivation material Si_3N_4 and SiO_2 , and the metal stack for different electrodes. The DUT has a layered MIS-HEMT structure with a thin epitaxial AlGaN film placed on GaN, forming the heterojunction at the AlGaN/GaN interface. Metallic electrodes are used for gate, source and drain contacts as well as for the GFP and SFP.

3.2 TCAD Simulation

Shown in Fig. 3.2 is the TCAD representation of the AlGaN/GaN FP device performed in Silvaco Atlas [98]. Standard FP topology of having a GFP and a SFP is considered, configured in a fashion similar to that shown in Fig. 3.1(b). Spontaneous polarization charges are added to the top and bottom surfaces of both AlGaN and GaN layers through polarization models. Piezoelectric charge is calculated separately by the strain model based on the lattice mismatch between AlGaN and GaN by having a value of 0.25 for the Al mole-fraction in the AlGaN layer. A self-consistent solution of the Poisson equation and continuity equations is obtained numerically by Atlas while incorporating physical models. Albrecht's Model [99] for bulk mobility is used while field-dependent Mobility Model [100] is also used to account for the saturation of carrier velocity at high lateral fields. Dirichlets



(a)



(b)

Figure 3.1: (a) Power GaN HEMT on Silicon substrate which is used as the device under test (DUT) for capacitance data measurement. It is a three-terminal device with a gate width (W) of 3 mm. (b) Cartoon showing dual field-plate configuration and device dimensions. Si_3N_4 and SiO_2 are used as passivation material.

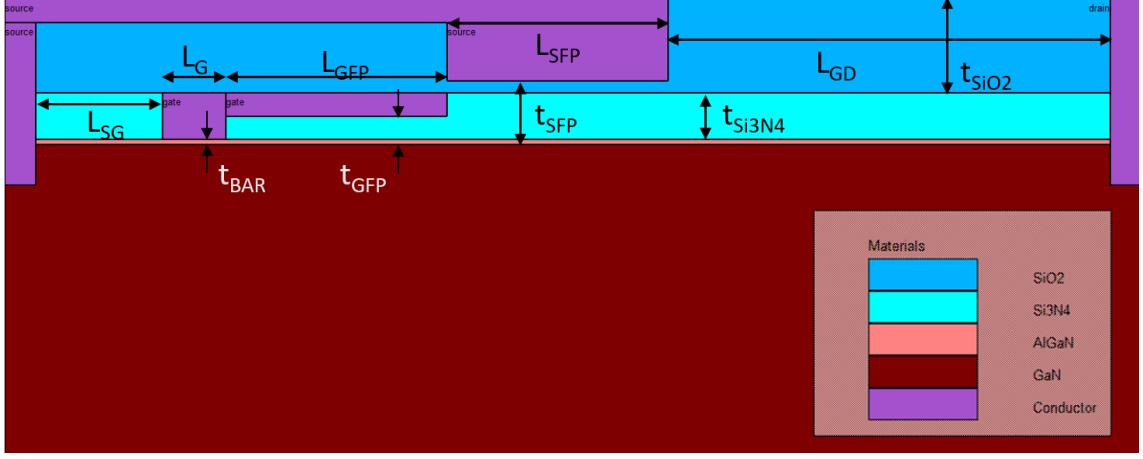


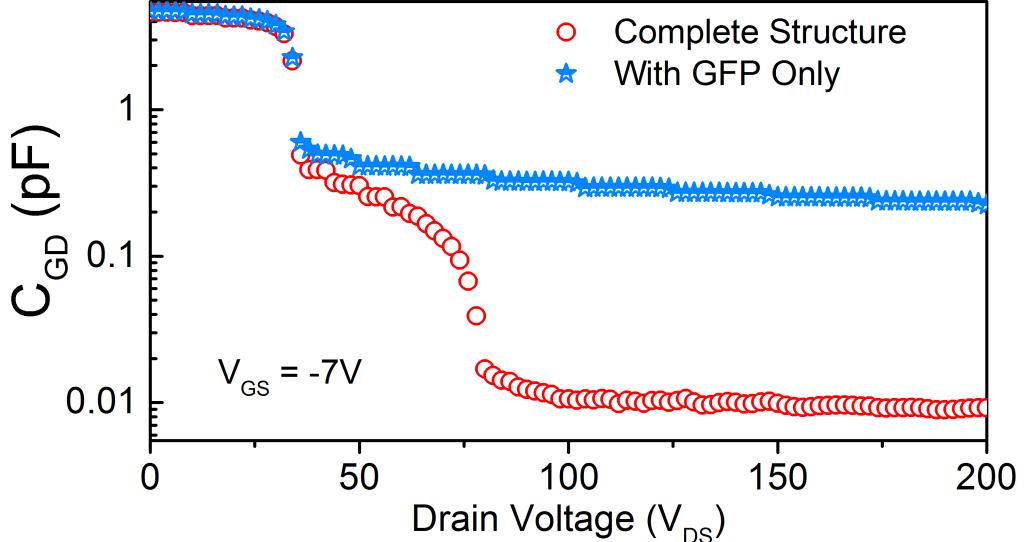
Figure 3.2: Cross-sectional view of the GaN HEMT dual-FP TCAD structure simulated in Silvaco Atlas. The structure dimensions are $L_G = 1 \mu\text{m}$, $W = 3 \text{ mm}$, $L_{GFP} = L_{SFP} = 3.5 \mu\text{m}$, $L_{SG} = 2 \mu\text{m}$, $L_{GD} = 7 \mu\text{m}$, $t_{BAR} = 20 \text{ nm}$, $t_{GFP} = 120 \text{ nm}$ and $t_{SFP} = 270 \text{ nm}$. Effective oxide thickness values for t_{GFP} and t_{SFP} with respect to t_{BAR} are evaluated and used in the model.

boundary condition, which is taken by default in Silvaco, is used for surfaces in order to get continuous electric displacement vector. For contacts, they are defined as ohmic/schottky by using particular values of work-functions.

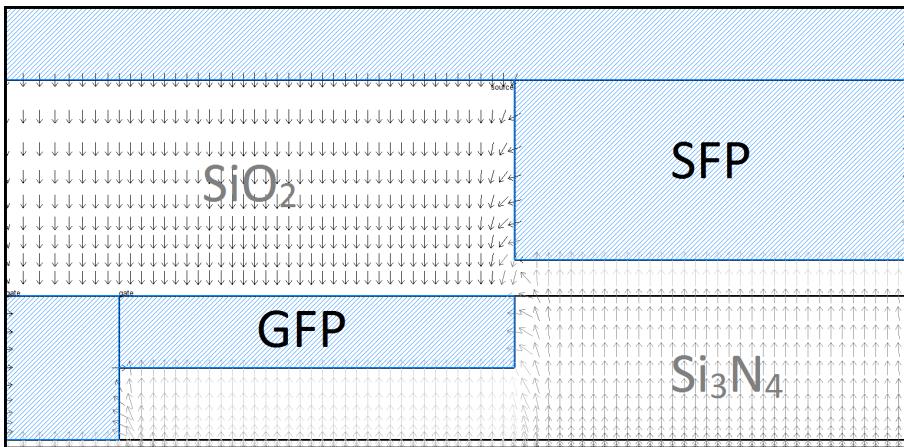
3.2.1 Cross-Coupling Capacitance

It is well known that the incorporation of GFP significantly increases the reverse Miller capacitance (C_{gd}) whereas SFP introduces an additional drain-source capacitance (C_{ds}) in the form of plateau-like features [101]. However, in advanced GaN FP structures, multiple capacitance plateaus are seen [102], the explanation for which is given as follows.

The TCAD simulated sub-threshold C_{gd} plots i.e when $V_{gs} < V_{off}$, for the device with both FPs as well as for the GFP-only structure is shown in Fig. 3.3(a). For the device with both GFP and SFP, the first plateau in C_{gd} corresponds to the progressive extension of depletion region, under the influence of the GFP, towards the drain with increasing V_{ds} , until full depletion of the 2DEG under the GFP occurs. The second plateau appears due to the cross-coupling influence of the GFP on the



(a)



(b)

Figure 3.3: (a) Comparison of the simulated subthreshold C_{gd} for dual-FP and GFP-only structures. The absence of second plateau for single FP structure highlights the cross-coupling phenomenon. V_{gs} is fixed at -7 V, while V_{ds} is swept from 0 to 200 V. (b) Electric field vector plot for $V_{ds} = 40$ V. The appearance of fringing electric field between the vertical wall of the GFP and the 2DEG_{SFP} causes the cross-coupling effect giving rise to second plateau in Fig. 3.3(a).

2DEG under the SFP which is denoted as 2DEG_{SFP}. It can be better understood by observing the C_{gd} for the GFP-only structure, where the second plateau feature seems to be missing, clearly indicating the cross-coupling effect of the GFP on

2DEG_{SFP} in the previous case. Further support to this argument is added by the vector plots shown in Fig. 3.3(b). The field lines emanating from the GFP and terminating at the 2DEG_{SFP} indicating the existence of a capacitive relation. One might argue that fringing field lines would still exist between the GFP and the adjacent 2DEG in the drain access region even in the absence of SFP, which might still lead to some sort of capacitance plateau. However, it is a point worth noting that the access region charge in that case is different from the 2DEG_{SFP} which has a different bias-dependency profile, a different cut-off voltage and is controlled by its own independent gate, which is the SFP. This is what differentiates the usual depletion-type capacitance for the GFP-only device from the plateau shaped cross-coupling capacitance in C_{gd} . The corresponding potential distribution within the device overlayed with electric field vector plots is shown in Fig. 3.4.

The bias-independent parasitic value of C_{gd} , which is due to the fringing field between the drain-electrode and the GFP, increases for the GFP-only structure in comparison to the structure with both FPs. It is because of a significant number

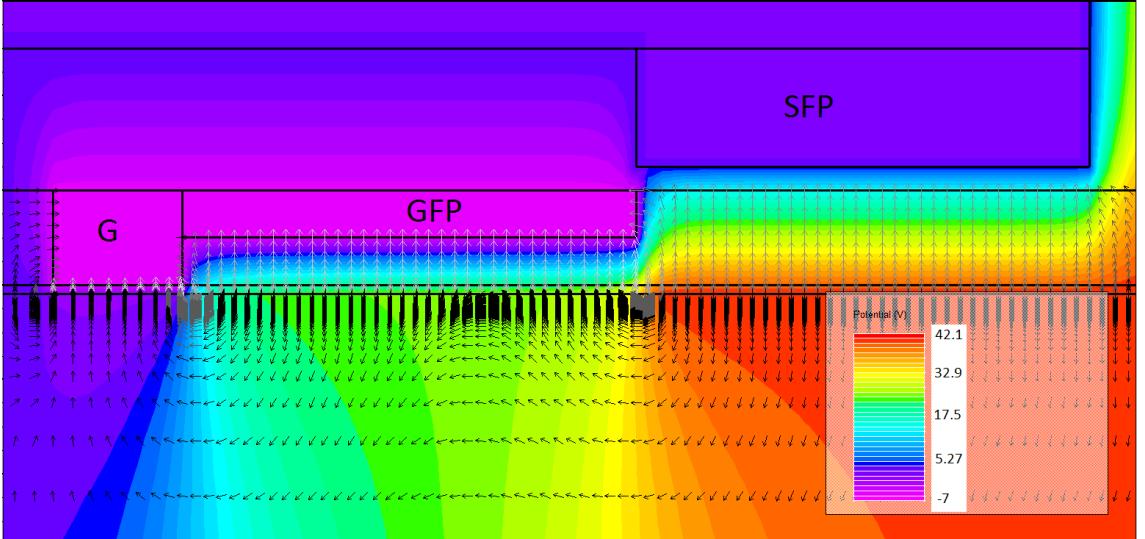


Figure 3.4: Contour plot showing distribution of potential within the device for $V_{gs} = -7$ V, and $V_{ds} = 40$ V. Also, an overlay of the vector plot for electric field lines is shown to understand the electric field strength. The varying grayscale of the vector plots represents a variation in the electric field strength. Grey: strong, black: weak.

of fringing field lines reaching the GFP through the insulator stack, whereas in presence of the SFP, most of them end up at the SFP leading to a reduced fringing capacitance component in C_{gd} , as shown in Fig. 3.5(a) and 3.5(b). Similar cross-coupling phenomenon acts between the SFP and the 2DEG_{GFP} where the 2DEG_{GFP} is coupled with the SFP through the source electrode.

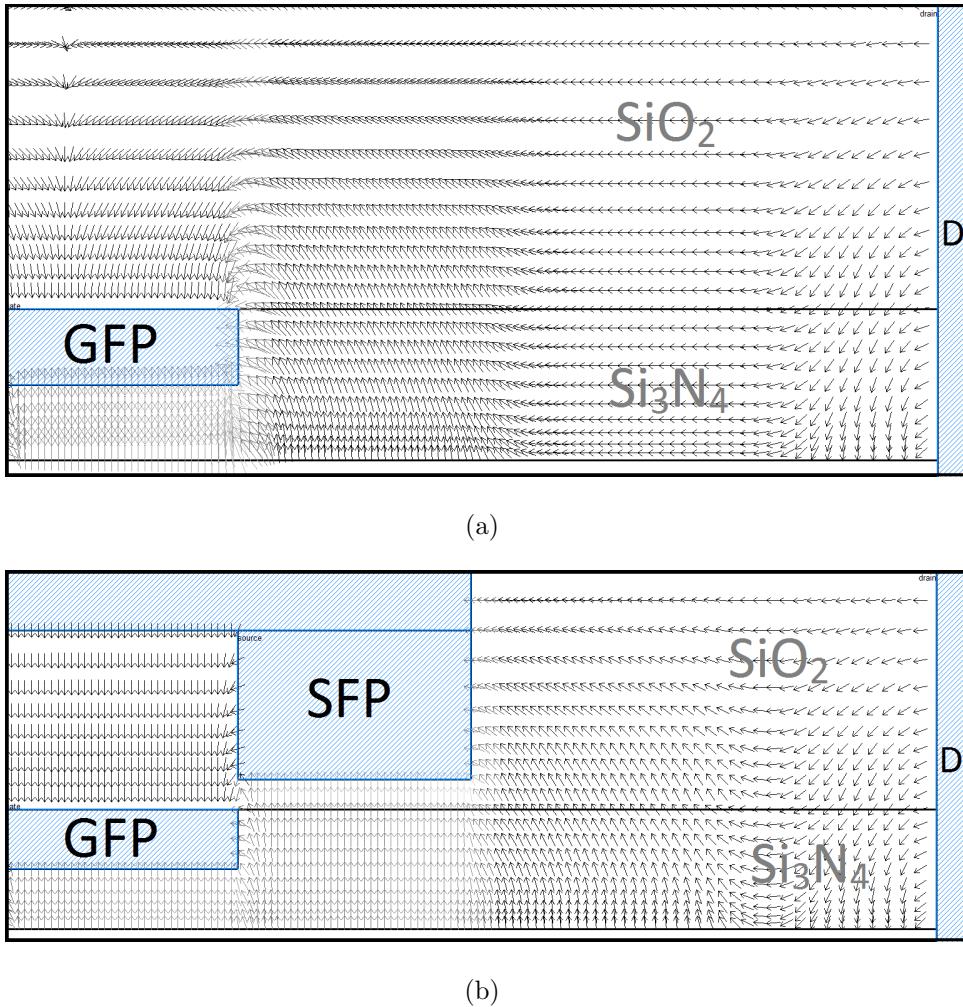


Figure 3.5: Vector plots for electric field lines for $V_{gs} = -7$ V and $V_{ds} = 100$ V
 (a) A significant number of fringing field lines reach the GFP through the insulator stack
 (b) In presence of the SFP, most of them end up at the SFP leading to a reduced fringing capacitance component in C_{gd} . The varying grayscale of the vector plots represents an electric field magnitude of 3.6×10^6 V/cm (gray) to 2.68×10^5 V/cm (black).

3.2.2 Substrate Capacitance

The introduction of a substrate electrode introduces a capacitance between the substrate and the other three intrinsic device nodes namely the gate, drain and source where the GaN buffer acts as a dielectric. The substrate-drain capacitance (C_{subd}), however, needs more attention since it forms a part of the overall output terminal capacitance (C_{oss}), given as

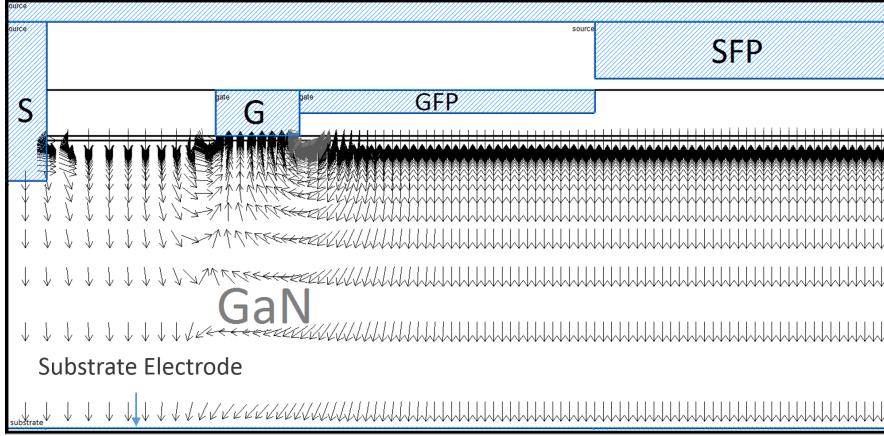
$$C_{oss} = C_{gd} + C_{ds} + C_{subd} \quad (3.1)$$

As shown in Fig. 3.6, a lot of field lines originating from the 2DEG reach the substrate electrode (see Fig. 3.6(a)) whereas in its absence, field lines from the drain side of the 2DEG terminate at the 2DEG on the source side through the GaN buffer (see Fig. 3.6(b)). In Fig. 3.14, as can be observed, C_{subd} manifests a double-plateau behavior similar to that of C_{gd} with each plateau appearing for bias conditions at which some significant 2DEG exists beneath the corresponding FP. It essentially suggests a similarity between the 2DEG and the associated substrate charge towards changing gate and drain biases - an approach that we later follow to model C_{subd} .

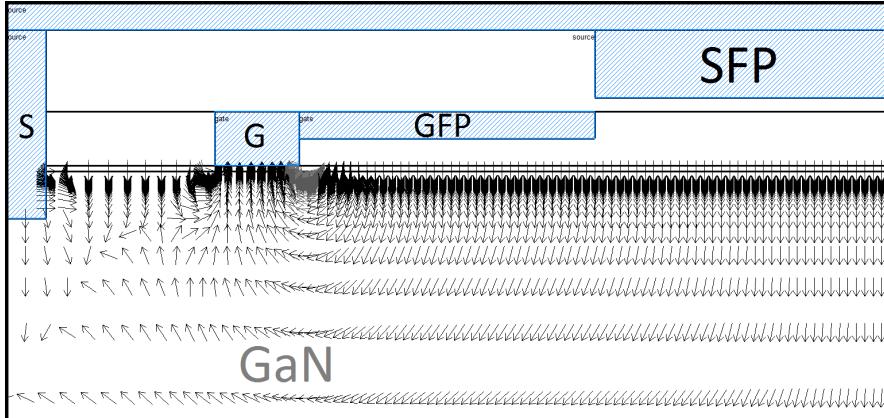
In this simulation study, we directly contact the substrate electrode with the GaN buffer layer even though for a real device there are multiple layers between the GaN buffer and the substrate contact such as Si or SiC substrate, nucleation layer etc. Although, the impact of including further layers under the GaN on the substrate capacitance would only have a quantitative effect in terms of giving a different effective dielectric constant, whereas the qualitative impact would remain the same.

3.3 Model Description

Fig. 3.7(a) shows a not-to-the-scale cross sectional view of the same device. The 2DEG charge, which is formed at the heterojunction due to the combined effect of conduction band discontinuity and spontaneous and piezoelectric polarization in the



(a)



(b)

Figure 3.6: Vector plots for electric field lines for $V_{gs} = -7$ V and $V_{ds} = 20$ V. Field lines originating from the 2DEG reach the substrate electrode (see Fig. 3.6(a) bottom) leading to the existence of C_{subd} whereas in its absence, field lines from the drain side of the 2DEG terminate at the 2DEG on the source side through the GaN buffer. The varying gray-scale of the vector plots represents an electric field magnitude of 1.32×10^6 V/cm (gray) to 1.09×10^5 V/cm (black).

AlGaN/GaN system, gets modulated in the region directly under the GFP due to the vertical field originating from it. The V_{off} needed at the GFP to deplete the 2DEG at the heterojunction corresponds to the equivalent thickness of the AlGaN barrier layer and insulator upon which the GFP rests. Since AlGaN/GaN HEMTs are normally ON devices, so a vertical field from the gate by applying a negative

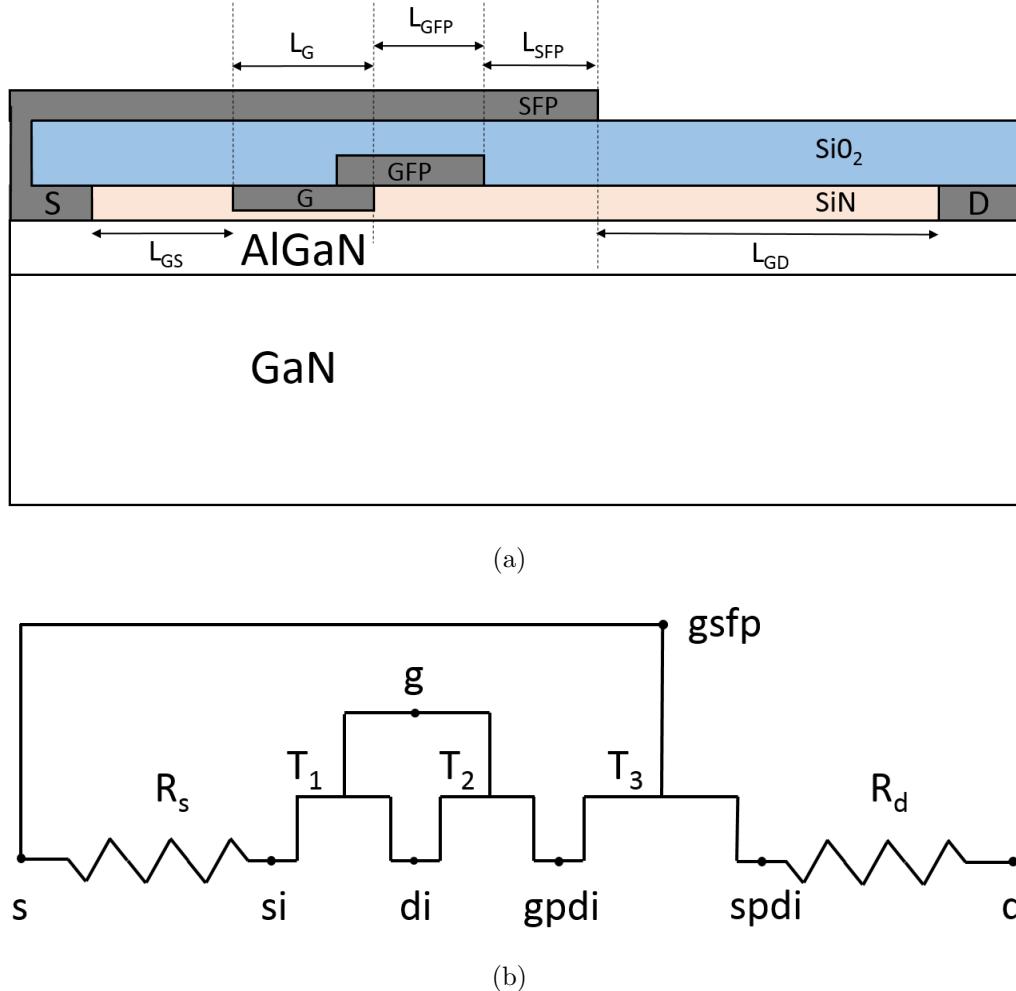


Figure 3.7: Cross-sectional view of the actual dual FP device showing the gate and source FPs and their appropriate connections to gate and source respectively. The device dimensions are $L_G = 1 \mu\text{m}$, $W = 3 \text{ mm}$, $L_{GFP} = L_{SFP} = 3.5 \mu\text{m}$, $L_{GS} = 2 \mu\text{m}$ and $L_{GD} = 12 \mu\text{m}$. (b) Model representation of the device. T_1 , T_2 and T_3 denote Intrinsic, Gate FP and Source FP transistors respectively. The intrinsic nodes within the device are also indicated

bias will force the device to turn off. Therefore, thicker the equivalent barrier with the dielectric same as AlGaN, stronger field is required to suppress the 2DEG, which means more negative will be the V_{off} . Since the barrier thickness under the GFP is more than the intrinsic transistor, the V_{off} for the GFP is therefore more negative. Same can be said for the SFP, which as per similar reasoning should have an even more negative V_{off} . Transistor properties to GFP and SFP can therefore be assigned

due to their 2DEG controlling ability. This forms the basis of our model as shown in Fig. 3.7(b) where the whole device is represented as a series combination of three independent HEMTs - the intrinsic transistor (T_1), the gate FP transistor (T_2), and the source FP transistor (T_3); and two resistors - the gate-source and gate-drain access region resistances R_s and R_d , respectively. We obtain the SP for each of these transistors separately as explained in the next sub-section, from which we evaluate intrinsic charges for each transistor required to find the capacitances. The model displays temperature scaling of its parameters that have a role to play in the temperature dependence of the model, in a way such that there is only a single global parameter set governing the model. For the sake of generality and in order to avoid redundancy in description, the model variables and parameters have been represented with a subscript k , where k is 1 for equations corresponding to T_1 , 2 for T_2 and 3 for T_3 . We represent the direction along the channel from source to drain by x -axis.

3.3.1 Surface-Potential and Intrinsic Charge Calculation

The calculation of the small signal capacitance of a device demands the precise evaluation of the charges that get developed at the various nodes of the device on application of some small signal voltage. These charges are calculated in terms of SP (ψ) using the ASM-GaN-HEMT model [80, 103].

We self-consistently solve the triangular quantum well formed at the heterojunction for its eigen-values using the Schrodinger's and Poisson's equations. Considering the two important sub-bands E_0 and E_1 to be occupied, we use Fermi-Dirac Statistics to obtain the 2DEG charge density for each of the three transistors T_1 , T_2 and T_3 . Solutions for the E_F are obtained for each of the regions of V_g sweep in terms of the gate overdrive voltage $V_{go} = V_g - V_{off}$ and a unified expression for E_F is calculated for each transistor as

$$E_{F,k} = V_{go,k} - \frac{2V_{th} \ln \left(1 + e^{\frac{V_{go,k}}{2V_{th}}} \right)}{1/H(V_{go,p}) + (C_{g,k}/qD)e^{-\frac{V_{go,k}}{2V_{th}}}} \quad (3.2)$$

An iterative re-evaluation of E_F using the Householder's method [104] is done for better accuracy. E_F allows us to calculate the SP ($\psi_k = E_{F,k} + V_{x,k}$) at both ends of the channel as $\psi_{s,k} = E_{F,k}$ and $\psi_{d,k} = E_{F,k} + V_{ds,k}$, with $V_{ds,k}$ being the drain source voltage for transistor T_k . The overall device SP, which is spatially divided into the SP for each of the modeled transistors, is stitched in a continuous fashion by the SPICE simulator.

In order to obtain the capacitances of the device, the intrinsic charges at source (Q_s), drain (Q_d) and gate (Q_g) for each of the modeled transistors are to be accurately evaluated. The following equation gives the gate charge

$$Q_{g,k} = - \int_0^{L_k} W C_{g,k} (V_{go,k} - \psi_k(x)) dx \quad (3.3)$$

where $C_{g,k} = \frac{\epsilon_k}{d_k}$ is the gate capacitance per unit area. d_k is the insulator thickness, while W and L_k are the channel width and channel length of the transistor T_k respectively.

Integrating (3.3), we get the total gate charge given by (3.4). T is the device operating temperature and K_B is the Boltzmann constant.

$$Q_{g,k} = WL_k C_{g,k} \left\{ V_{go,k} - \frac{1}{2} (\psi_{s,k} + \psi_{d,k}) + \frac{1}{12} \frac{(\psi_{d,k} - \psi_{s,k})^2}{V_{goT}} \right\} \quad (3.4)$$

where

$$V_{goT} = V_{go,k} + \frac{K_B T}{q} - \frac{1}{2} (\psi_{s,k} + \psi_{d,k}) \quad (3.5)$$

$Q_{d,k}$ and $Q_{s,k}$ are found using the position and gate-bias dependent channel charge per unit length given by $Q_{ch,k}(V_{go,k}, V_{x,k}) = WC_{g,k}(V_{go,k} - \psi(x))$. This charge is partitioned by the Ward-Dutton scheme wherein the drain and source charges are defined as [105]

$$Q_{d,k} = \int_0^{L_k} (x/L_k) Q_{ch,k} dx \quad (3.6)$$

$$Q_{s,k} = \int_0^{L_k} (1 - x/L_k) Q_{ch,k} dx. \quad (3.7)$$

Using the expression for $Q_{ch,k}$, drain charge can be calculated by the integral

$$Q_{d,k} = \int_0^{L_k} (x/L_k) WC_{g,k} (V_{go,k} - \psi_k(x)) dx \quad (3.8)$$

which upon further transformation results into

$$Q_{d,k} = -\frac{1}{2} WL_k C_{g,k} \left\{ V_{go,k} - \frac{1}{3} (\psi_{s,k} + 2\psi_{d,k}) + \frac{1}{12} \frac{\psi_{ds,k}^2}{V_{goT}} \left(1 + \frac{1}{10} \frac{\psi_{ds,k}}{V_{goT}} \right) \right\} \quad (3.9)$$

Charge conservation maintained between the gate, drain and source terminals allows us to obtain the source charge using (3.4) and (3.9) as

$$Q_{s,k} = -Q_{g,k} - Q_{d,k} \quad (3.10)$$

3.3.2 Modeling of Cross-Coupling and Substrate Charges

As discussed in the previous section, the GFP modulates some part of the 2DEG lying beneath the SFP, leading to some finite amount of cross-coupling charges. Also, it can be observed in Fig. 3.3(a) that the second plateau, which comes into existence due to the presence of a SFP, exhibits a V_{off} corresponding to that of the SFP. From a modeling point of view, this suggests a fraction of the gate charge of the SFP coupled with the GFP. We employ the existing charge expression for SFP and use a dimensionless scaling factor α_{cc} that determines the strength of cross-coupling effect, to evaluate the cross-coupling charge Q_{cc} between the GFP and the 2DEG_{SFP}, given as

$$Q_{cc} = \alpha_{cc} WL_{SFP} C_{g,SFP} \left\{ V_{go,SFP} - \frac{\psi_{s,SFP} + \psi_{d,SFP}}{2} + \frac{(\psi_{d,SFP} - \psi_{s,SFP})^2}{12V_{goT,SFP}} \right\} \quad (3.11)$$

The cross-coupling capacitance can now be evaluated by assigning this charge between the gate of the GFP transistor and source of the SFP transistor, as under

$$C_{GFP-SFP} = -\frac{dQ_{cc}}{dV_{s,SFP}} \quad (3.12)$$

$C_{GFP-SFP}$ is added to C_{gd} leading to the double-plateau features in C_{gd} .

In order to model the substrate capacitances, we associate some charges to the substrate node and divide it into the regional substrate charges corresponding to the intrinsic transistor ($Q_{sub,1}$), GFP ($Q_{sub,2}$) and SFP ($Q_{sub,3}$). Each one of these quantities is basically a scaled value of the 2DEG for each transistor controlled by its own gate. So, effectively we model the substrate as a back-field-plate which to some extent modulates the channel 2DEG, with the GaN layer as the dielectric. We now have three substrate transistors and their corresponding gate charges are evaluated using the gate-charge formulation, given as

$$Q_{g,sub,k} = \beta_k WL_k C_{sub,k} \left\{ V_{go,k} - \frac{1}{2} (\psi_{s,k} + \psi_{d,k}) + \frac{1}{12} \frac{(\psi_{d,k} - \psi_{s,k})^2}{V_{goT}} \right\} \quad (3.13)$$

where β_k is a dimensionless scaling factor and k is 1, 2 and 3 for intrinsic transistor, GFP and SFP respectively.

In order to maintain charge neutrality within the substrate, drain and source nodes of the device, we assign proportionally scaled charges to drain and source nodes. The drain charge is given as,

$$Q_{d,sub,k} = -\beta_k \frac{1}{2} WL_k C_{sub,k} \left\{ V_{go,k} - \frac{1}{3} (\psi_{s,k} + 2\psi_{d,k}) + \frac{1}{12} \frac{\psi_{ds,k}^2}{V_{goT}} \left(1 + \frac{1}{10} \frac{\psi_{ds,k}}{V_{goT}} \right) \right\} \quad (3.14)$$

Charge conservation maintained between the substrate, drain and source terminals allows us to obtain the source charge using (3.13) and (3.14) as

$$Q_{s,sub,k} = -Q_{g,sub,k} - Q_{d,sub,k} \quad (3.15)$$

which ensures that no convergence issues are faced during SPICE simulation,

making the model more robust.

3.3.3 Capacitance Calculation

In order to comprehend the dynamic behaviour of the FP HEMT device, there is need to examine the charging and discharging of the various internal capacitances within the device. So, our task understandably would be to model the gate to source (C_{gs}), gate to drain (C_{gd}) and drain to source (C_{ds}) capacitances between the terminal nodes of the HEMT device with FPs. However, the data that commonly is provided is the bias dependence of terminal capacitances C_{iss} , C_{rss} and C_{oss} which are defined as

$$Crss = C_{gd} \quad (3.16)$$

$$Ciss = C_{gd} + C_{gs} \quad (3.17)$$

$$Coss = C_{gd} + C_{ds} \quad (3.18)$$

Having obtained the intrinsic charges for the individual transistors, we assign them in accordance with Fig. 3.7(b) to the intrinsic nodes within the device (in parenthesis) as shown in Table 3.1. It must be noted that the gate charge for T_3 is assigned to the source node s due to the connection between nodes $gsfp$ and s . We're now in a position to compute all the non-reciprocal device capacitances from the definition

$$C_{mn} = \pm(dQ_m/dV_n) \quad (3.19)$$

where \pm is $+$ for $m = n$ and $-$ for $m \neq n$.

It is important to consider the capacitances due to the access regions, particularly at the drain end C_{accd} due to the extension of the depletion region on the drain end. C_{accd} shows up in C_{ds} , in the form of a depletion capacitance, tailing off gradually for higher drain voltages. We formulate it as

$$C_{accd} = \frac{C_{J0}}{(1 + V_{ds}/V_{bi})^{MZ}} \quad (3.20)$$

where V_{bi} is taken as a parameter. MZ controls the way with which the junction capacitance decays with drain bias and C_{J0} is a parameter that governs the low bias depletion capacitance. Since at low values of V_{ds} , C_{ds} primarily is a bias independent capacitance due to the incorporation of the SC-FP, a parameter AJ is used in restricting C_{accd} at low drain voltages, using a MIN function.

There exists a parallel plate capacitance between the gate/GFP and the overlying SFP. This bias independent capacitance is taken care of by introducing a parameter CFG into the model, which adjusts the minimum value of C_{gs} .

Table 3.1: Charges at intrinsic nodes of the three transistors

Transistor	T_1	T_2	T_3
Terminal			
Gate	$q_{g1}(g)$	$q_{g2}(g)$	$q_{g3}(s)$
Source	$q_{s1}(si)$	$q_{s2}(di)$	$q_{s3}(gpdi)$
Drain	$q_{d1}(di)$	$q_{d2}(gpdi)$	$q_{d3}(spdi)$

3.3.4 Temperature Dependence

Our model accounts for the temperature scaling of its parameters that have a role to play in the temperature dependence of the model, leading us to a single parameter set for temperature ranges 25° C to 150° C. Temperature dependence in our capacitance model for a GaN HEMT with FPs primarily comes about due to variation in $V_{off,k}$ with T . According to [106]

$$V_{off}(T) = \phi_B - \Delta E_c(T) - \frac{\sigma_{pz}(T)d}{\epsilon} - \frac{qN_d d^2}{2\epsilon} \quad (3.21)$$

where ΔE_c is the discontinuity in conduction band between AlGaN/GaN, ϕ_B represents the Schottky barrier, σ_{pz} gives the interface charge density induced due

to polarization and d , ϵ and N_d are the AlGaN layer material parameters carrying usual meaning. The doping density N_d is negligible, since AlGaN is undoped in our case. $\sigma_{pz}(T)$ is a very weak function of temperature and its temperature variation can be ignored to the first order approximation. ΔE_c , being a function of the energy bandgaps of AlGaN ($E_g^{AlGaN}(T)$) and GaN ($E_g^{GaN}(T)$), varies strongly with T as given by [107]

$$\Delta E_c = 0.70 (E_g^{AlGaN}(T) - E_g^{GaN}(T)) \quad (3.22)$$

With these simplifications, we model V_{off} as a linearly varying function of temperature as demanded by the trend shown in experimental data. It is given as [108]

$$V_{off,k}(T) = V_{off,k} - V_{temp,k} \left(\frac{T}{TNOM} - 1 \right) \quad (3.23)$$

where $V_{temp,k}$ is the V_{off} temperature dependence parameter for transistor T_k . The parenthesized T denotes a temperature scaling of the parameter at device operating temperature T while $TNOM$ is the nominal temperature set to 25° C.

C_{ds} shows a variable decay at high drain bias with temperature as is observed from the experimental data. In order to model that we employ temperature dependence for built in voltage V_{bi} and the bias independent depletion capacitance parameter C_{J0} given as

$$V_{bi}(T) = V_{bi} - V_{temp,VBI} \left(\frac{T}{TNOM} - 1 \right) \quad (3.24)$$

$$C_{J0}(T) = C_{J0} - V_{temp,CJ0} \left(\frac{T}{TNOM} - 1 \right) \quad (3.25)$$

where $V_{temp,VBI}$ and $V_{temp,CJ0}$ are parameters for V_{bi} and C_{J0} temperature scaling.

3.4 Parameter Extraction and Model Validation

3.4.1 Parameter Extraction

Table 3.2 has the description of the model parameters along with their extracted values. We begin the $V_{off,k}$ parameter extraction process for device by fitting our model results for V_{gs} dependence of C_{iss} with the experimental data at $V_{ds}=0V$ as shown in Fig. 3.8(a). The figure also has C_{gd} and C_{gs} which are the individual capacitance components that sum up and give C_{iss} . Two hump like features are seen to arise at transistion regions that represent V_{off1} and V_{off2} as pointed out in the plot. Gate length $L_{1,2}$ and insulator thickness $d_{1,2}$ for $T_{1,2}$ determine the magnitude of the two hump like features in Fig. 3.8(a). Greater the gate length, greater would be the capacitance and vice versa for insulator thickness. Here, geometrical device parameters have been used. The parallel plate capacitance parameter CFG controls the bias independent value of C_{iss} for sufficiently negative V_{gs} . It must be noted that due to the absence of an electrical connection between the nodes $gsfp$ and g , no contribution from T_3 is made either to C_{gs} or C_{gd} , even though T_3 remains ON for all V_{gs} values in Fig. 3.8(a). Therefore, for parameters corresponding to T_3 , we rely on other modeling results.

Fig. 3.8(b) illustrates the formation of 2DEG in transistors T_1 , T_2 and T_3 as a function of V_{gs} . V_{ds} is fixed at 0 V, forcing the voltages at intrinsic nodes si , di , $gpdi$ and $spdi$ to 0 V. Since the AlGaN/GaN HEMT is a normally ON device due to its conduction band profile and polarization induction, it needs negative gate voltage in order to turn it OFF. The insulator thickness for T_2 is greater than for T_1 , therefore it requires a more negative voltage at it's gate in order to deplete the 2DEG. It is seen that the cutoff voltages for $T_1(V_{off1})$ and $T_2(V_{off2})$, according to our model, fall around -3 V and -51 V respectively as these are the voltage values where 2DEG starts to build up within the transistor. Same values for cutoff voltages are seen in Fig. 3.8(a). T_3 has a greater insulator thickness than T_2 as seen in Fig. 3.7(a), so a logical extrapolation of the above analysis would suggest an even more negative cutoff voltage (V_{off3}) for T_3 . It must be noted that the gate ($gsfp$) of T_3 is

Table 3.2: Parameters for dual FP HEMT Capacitance Model

Parameter	Description	Value/Remarks
k	Subscript used as index for different transistors	1 for T_1 , 2 for T_2 and 3 for T_3
$TNOM$	Nominal temperature ($^{\circ}$ C)	25
$V_{off,k}$	Cutoff Voltage (V)	$V_{off1}=-3$, $V_{off2}=-51$, $V_{off3}=-75$
L_k	Gate length (μm)	$L_1=1$, $L_2=3.5$, $L_3=3.5$
d_k	Insulator thickness (μm)	$d_1=0.04$, $d_2=0.35$, $d_3=2$
CFG	Parallel Plate Capacitance parameter (pF)	5.8
$V_{temp,k}$	For $V_{off,k}$ temperature dependence (V)	$V_{temp,1}=9.86$, $V_{temp,2}=6.19$, $V_{temp,3}=49.39$
V_{bi}	Built in voltage (V)	0.877
$V_{temp,VBI}$	For V_{bi} temperature dependence (V)	0.297
MZ	Determines the decay in C_{ds} with V_{ds}	0.744
C_{J0}	Decides the zero V_{ds} depletion capacitance (pF)	64.15
$V_{temp,CJ0}$	For C_{J0} temperature dependence (pF)	6.884
AJ	For restricting C_{ds} at low V_{ds} (pF)	3.67

connected to the source node (s) of the overall HEMT device due to the connection between the source and the source FP as shown by Fig. 3.7(a). Therefore, the gate-source voltage (V_{gs3}) for T_3 is clamped to 0 V. This keeps T_3 in the ON state with a substantial 2DEG as seen in Fig. 3.8(b), independent of the overall V_{gs} . This

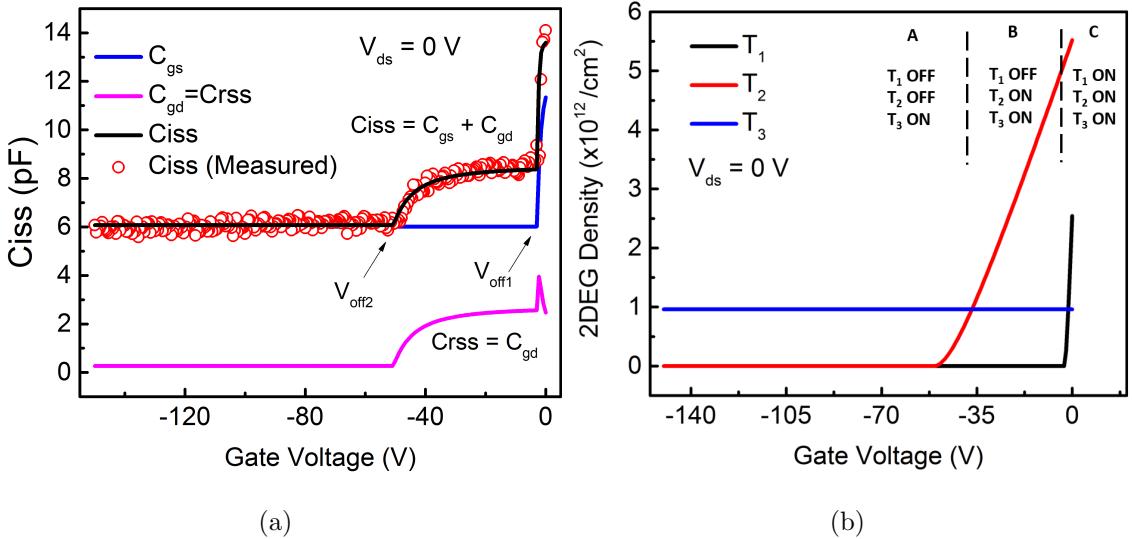
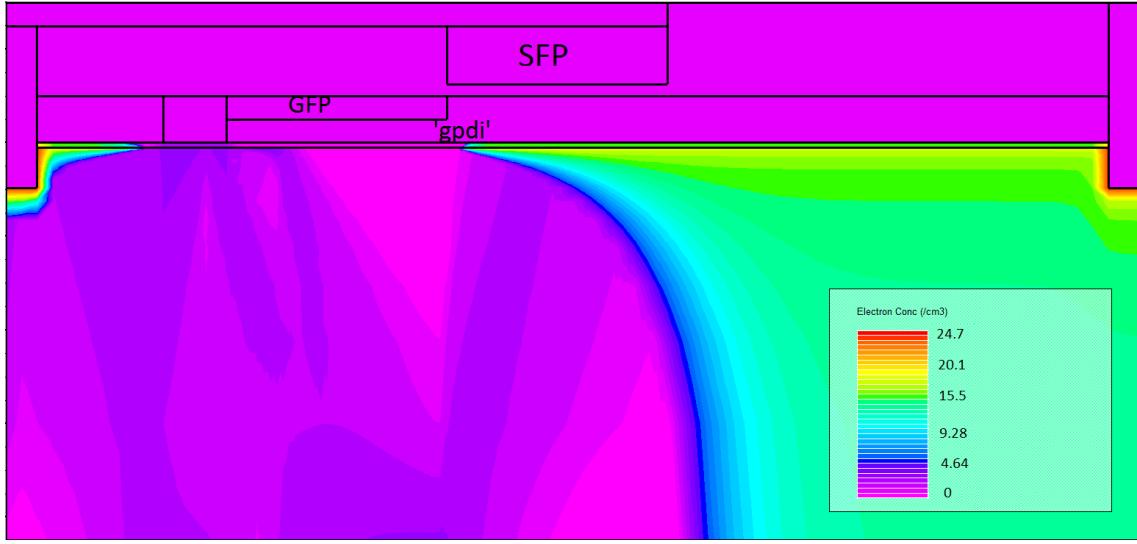


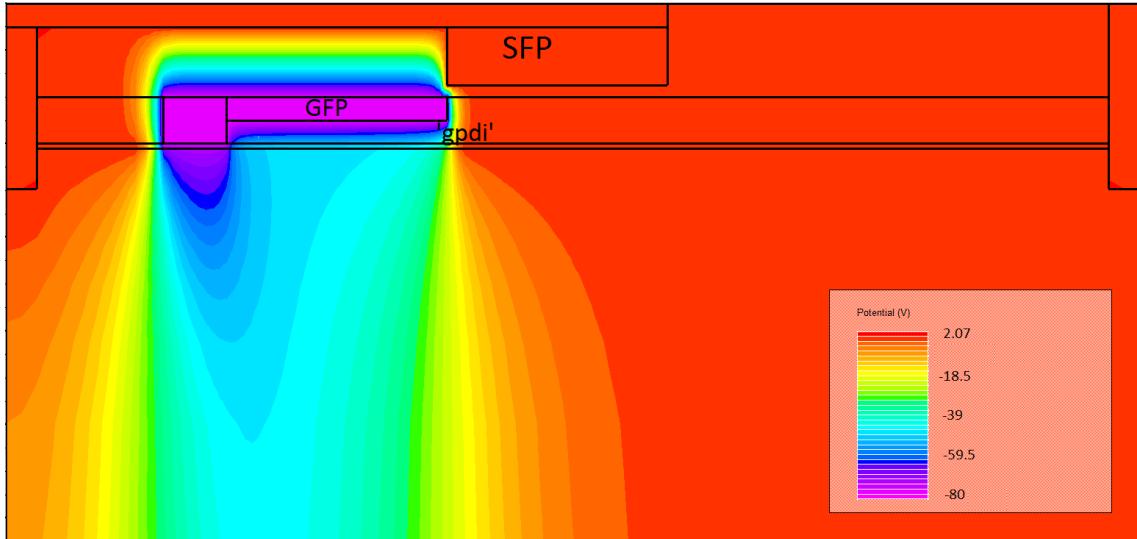
Figure 3.8: (a) Comparison of the modeled C_{iss} - V_{gs} with experimental data. V_{ds} is fixed at 0 V. C_{gs} and C_{gd} , that together add up to give C_{iss} , have also been plotted. (b) 2DEG density for transistors T_1 , T_2 and T_3 as a function of V_{gs} , illustrating cutoff voltages for transistors T_1 and T_2 to be -51 V and -3 V respectively. It is seen that T_3 is ON throughout the V_{gs} sweep. Regions A, B and C for V_{gs} operation have also been indicated.

argument is supported by the TCAD simulated electron concentration and potential distribution plots under strong negative V_{gs} conditions, shown in Fig. 3.9, which suggest a slight reduction in the effective length of T_3 due to the extension of the depletion region under the SFP, nevertheless, the T_3 transistor still remains ON with a significant amount of 2DEG, governed by its own gate, i.e the SFP. Of course, we ignore the length modulation of T_3 to a first order approximation. The entire V_{gs} sweep in Fig. 3.8(b) is divided into three regions namely region A, B and C based on the ON/OFF condition of intrinsic transistors.

In Figs. 3.10(a) and 3.10(b) we show the V_{ds} dependence of the intrinsic drain-source voltage $V_{ds,k}$ and intrinsic gate-source voltages $V_{gs,k}$ respectively, for transistors T_k , where k represents the transistor index. In Fig. 3.10(c), we plot the 2DEG variation for transistor T_k with V_{ds} . All the plots in Fig. 3.10 are coherent and together indicate the ON/OFF condition of transistors for different regions of V_{ds} .



(a)



(b)

Figure 3.9: (a) Electron concentration and (b) Potential distribution simulated for $V_g = -80$ V and $V_{ds} = 0$ V. An extension of the depletion region is seen at the beginning of the SFP, however, most of the transistor T_3 is in ON state. The potential at the gpdi node more or less remains at 0 V.

All the parameters corresponding to T_3 , whose extraction could not be made from results in Fig. 3.8(a), can now be extracted by V_{ds} dependence of C_{iss} , C_{rss} and C_{oss} under sub-threshold condition as shown in plots 3.10(d), 3.10(e) and 3.10(f) of Fig. 3.10. The contributions of GFP and SFP in conjunction with the

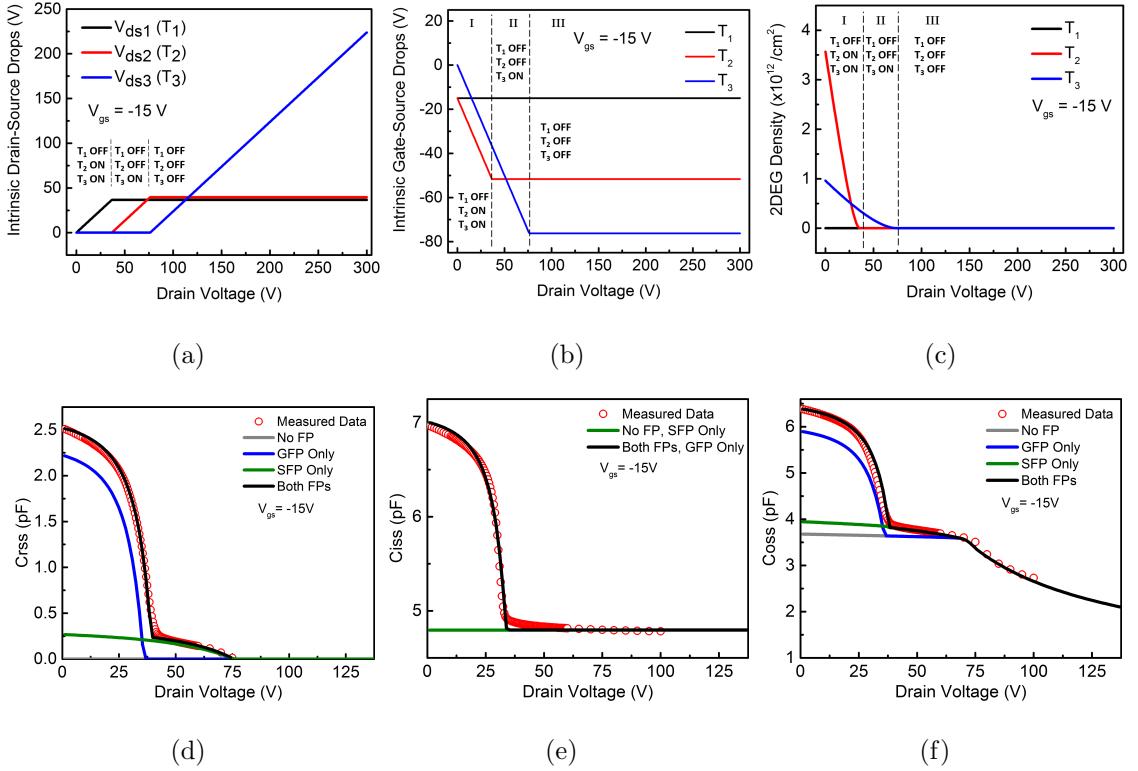


Figure 3.10: Variation of (a) Intrinsic drain-source voltages (b) Intrinsic Gate-Source voltages and (c) 2DEG density for transistors T_1 , T_2 and T_3 with V_{ds} under sub-threshold conditions i.e. $V_{gs} = -15$ V. Regions I, II and III for V_{ds} operation have also been indicated. Comparison of the modeled (d) C_{rss} , (e) C_{iss} and (f) C_{oss} capacitances with experimental data. Contributions made by both the FPs in conjunction with the intrinsic device are also shown. Solid lines are used for model simulations.

intrinsic device towards terminal capacitances is shown. V_{off3} is extracted from the overall V_{ds} dropped almost entirely across T_1 and T_2 , at which SC-FP begins to contribute towards C_{rss} as seen in Fig. 3.10(d). Its value comes out to be $V_s - V_{gpdi} = -75$ V.

3.4.2 Validation against Measured Data

In Fig. 3.11, modeled capacitance results are shown for FP devices with two different widths i.e. $W = 3$ mm and $W = 6$ mm, thereby highlighting the scalable property of

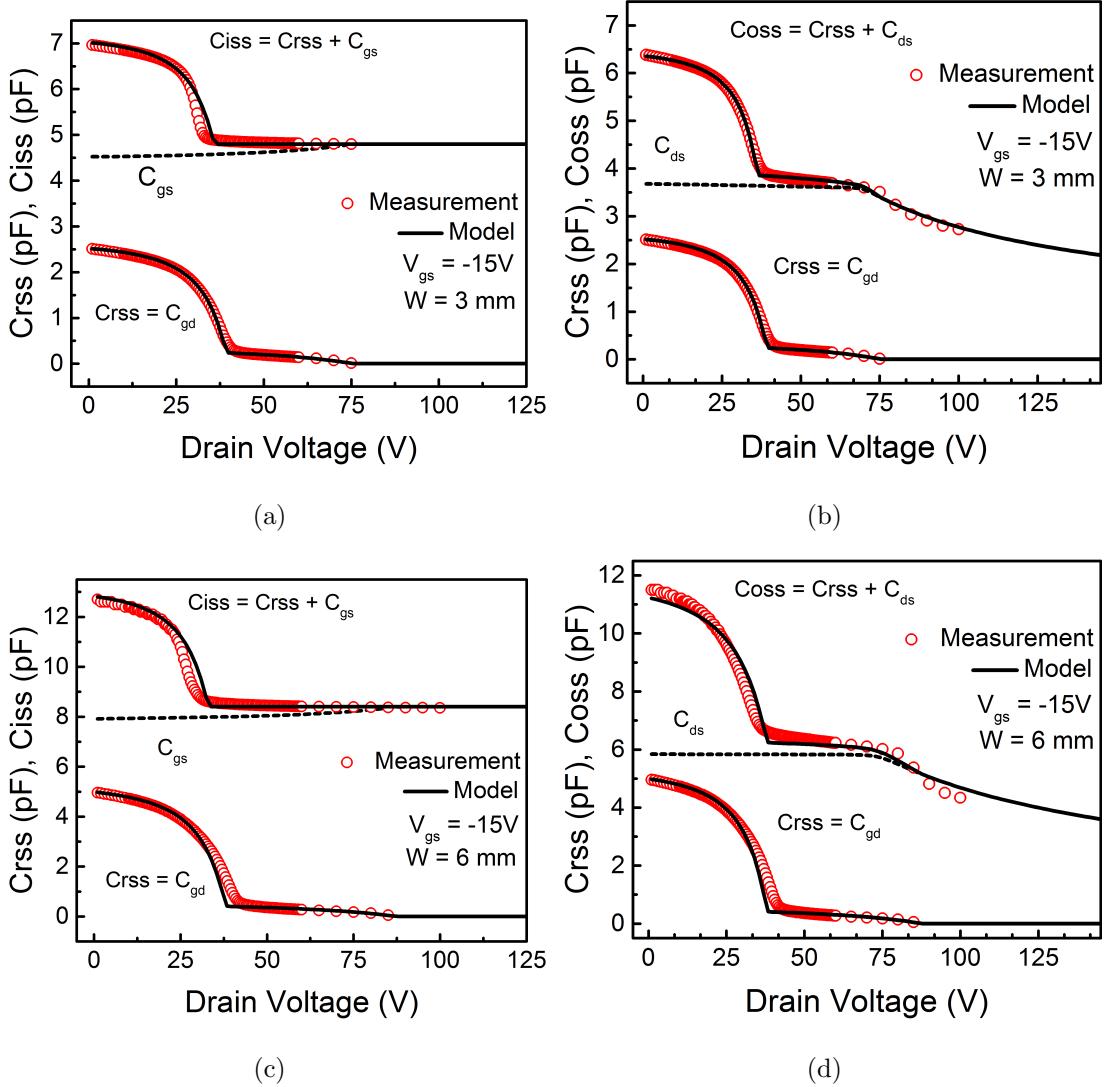


Figure 3.11: Comparison of the modeled (a) C_{iss} - V_{ds} and (b) C_{oss} - V_{ds} with experimental data under sub-threshold conditions for device with $W = 3\text{ mm}$. C_{gs} , C_{gd} and C_{ds} have also been plotted in order to show their contributions to the terminal capacitances under various regions of V_{ds} operation. Corresponding plots for device with $W = 6\text{ mm}$ are shown in (c) and (d) respectively.

the model, which can be ascribed to its physical nature. The individual components to the terminal capacitances i.e. C_{gs} , C_{ds} and C_{gd} have also been plotted. The model is accurate in predicting the cross-coupling plateaus in C_{gd} and the access region capacitance in C_{oss} .

We also validate our model for the temperature dependence of above mentioned

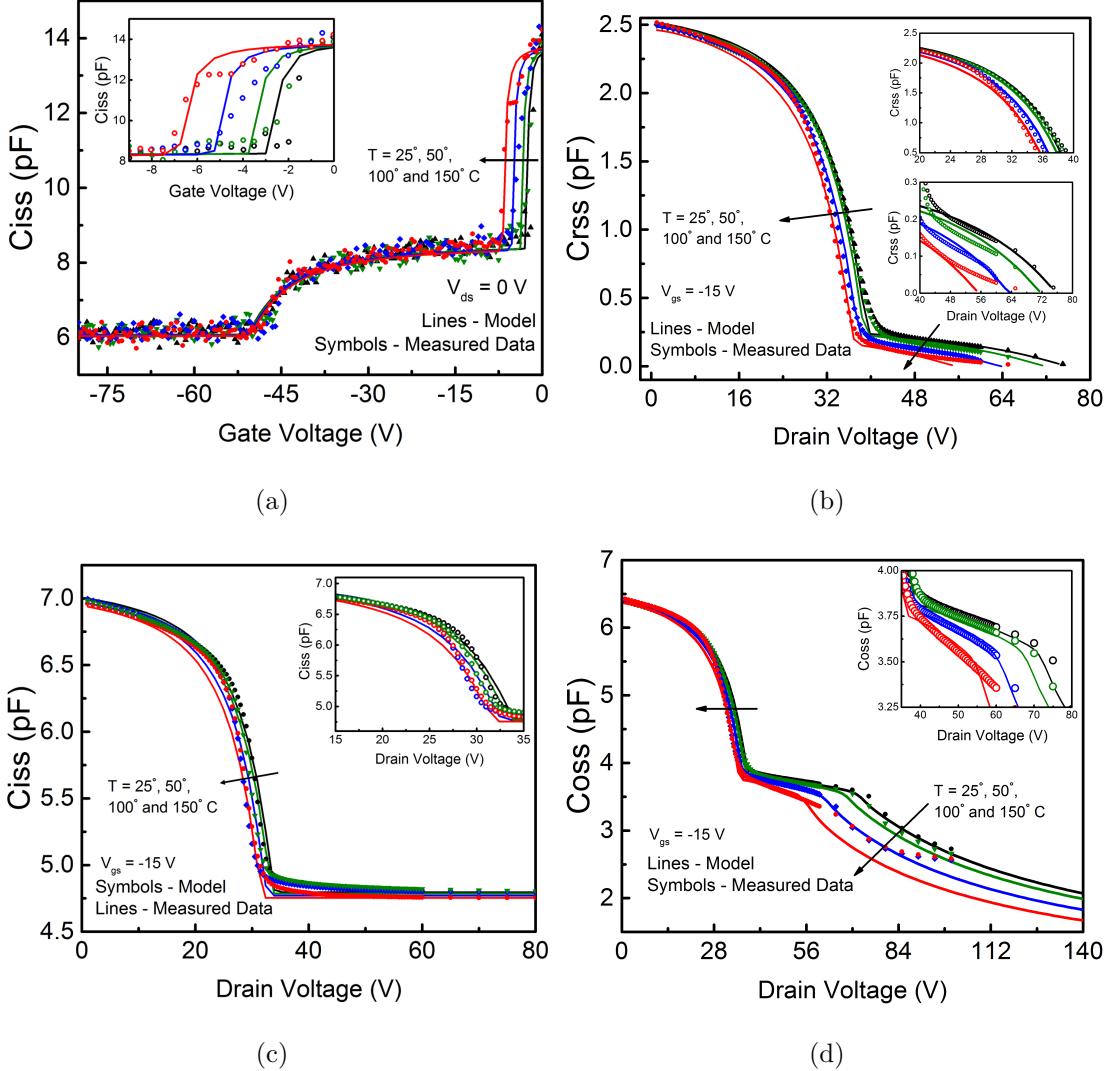
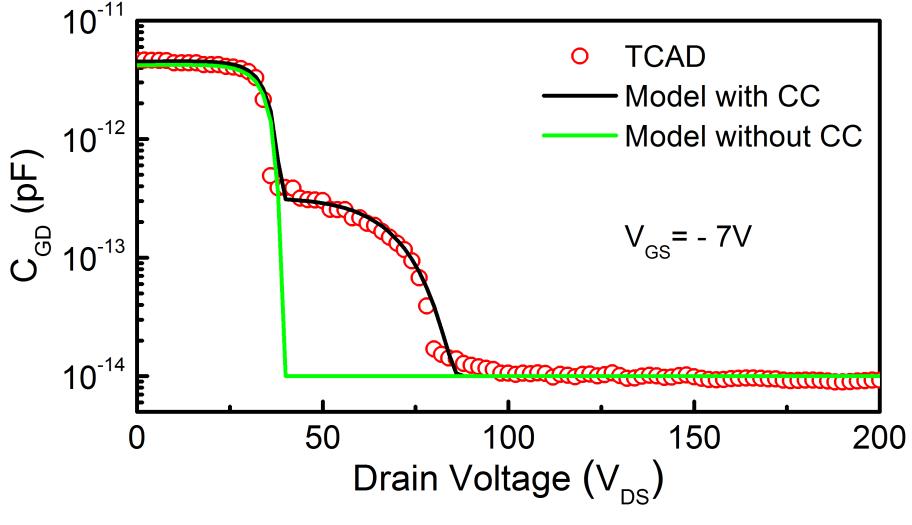
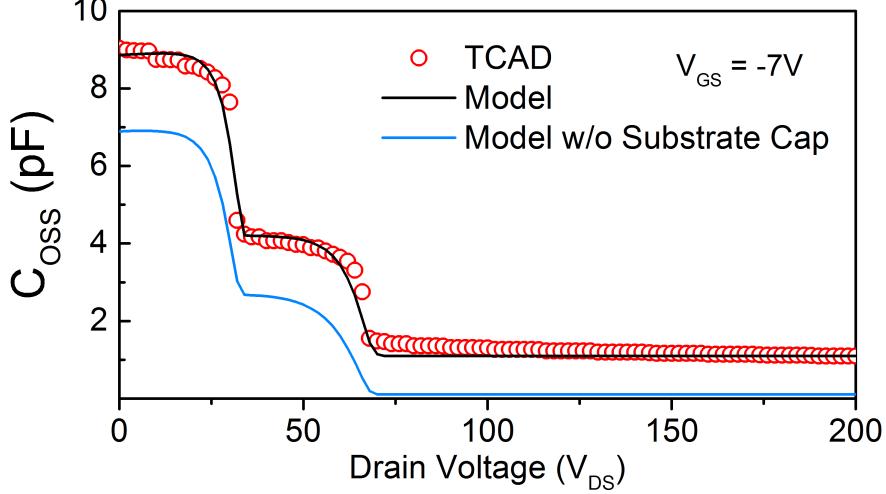


Figure 3.12: Temperature dependence of (a) C_{iss} - V_{gs} (b) C_{rss} - V_{ds} (c) C_{iss} - V_{ds} and (d) C_{oss} - V_{ds} is shown for 25° , 50° , 100° and 150° C. Insets for temperature sensitive ranges have been added for better clarity. Extracted values of temperature dependence parameters $V_{temp,k}$, $V_{temp,VBI}$ and $V_{temp,CJ0}$ are given in Table 3.2.

terminal capacitances in Fig. 3.12. Increase in temperature causes V_{off1} to decrease as observed in Fig. 3.12a and has been modeled in (3.23). The primary reason for V_{off1} variation is decrease in ΔE_c with increase in temperature as explained in (3.21) and (3.22). In Figs. 3.12b, 3.12c and 3.12d, temperature dependence is reflected in decrease of $V_{off2,3}$ for higher temperatures, causing the capacitance humps to shift leftwards. $V_{temp,1,2}$ are extracted from these plots. The depletion capacitance temperature parameters $V_{temp,VBI}$ and $V_{temp,CJ0}$ are extracted from Fig. 3.12d.



(a)

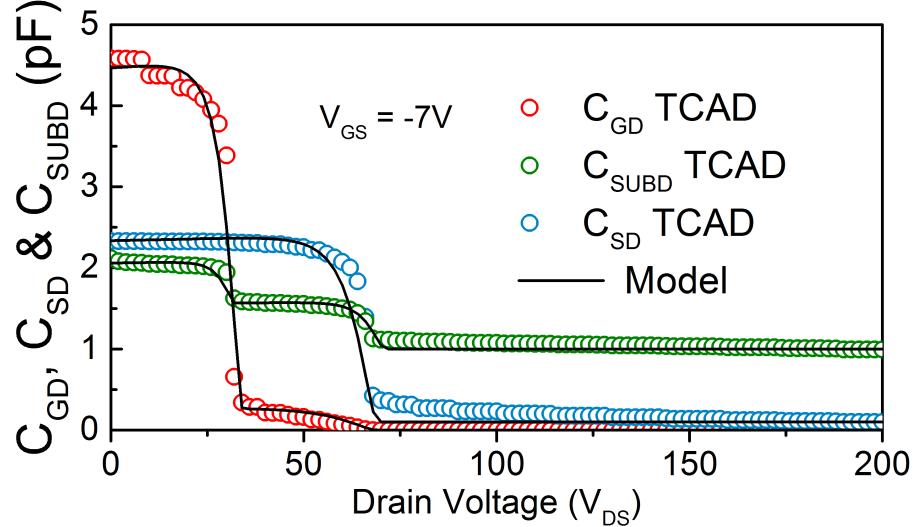


(b)

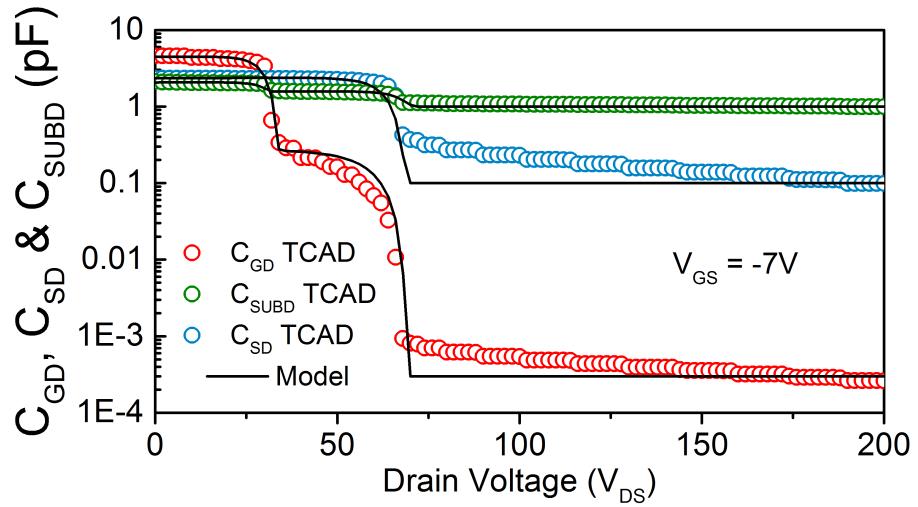
Figure 3.13: (a) Comparison of the modeled C_{gd} , with TCAD data under sub-threshold conditions for GaN FP HEMT. Model without cross-coupling capacitances is also shown in which the second plateau is seen missing. (b) Comparison of the modeled $C_{oss} = C_{gd} + C_{sd} + C_{subd}$ with TCAD data capturing precisely the contribution of C_{subd} .

3.4.3 Validation against TCAD Data

Shown in Fig. 3.13 are the model validation results against TCAD data taken for the device described in section 3.2. The comparison of model with and without the



(a)



(b)

Figure 3.14: Comparison of the modeled C_{gd} , C_{sd} and C_{subd} with TCAD data under sub-threshold conditions for GaN FP HEMT with substrate electrode. (a) Linear scale (b) Logarithmic scale.

cross-coupling capacitances clearly highlights its importance as seen in Fig. 3.13(a). The impact of substrate capacitance is clearly observed in Fig. 3.13(b), where C_{oss} is simulated with and without the substrate capacitance model. Strong correlation is obtained between the modeled and TCAD results as shown in Fig. 3.14 as illustrated by the linear and logarithmic scale plots. Also, the scalability feature of the model

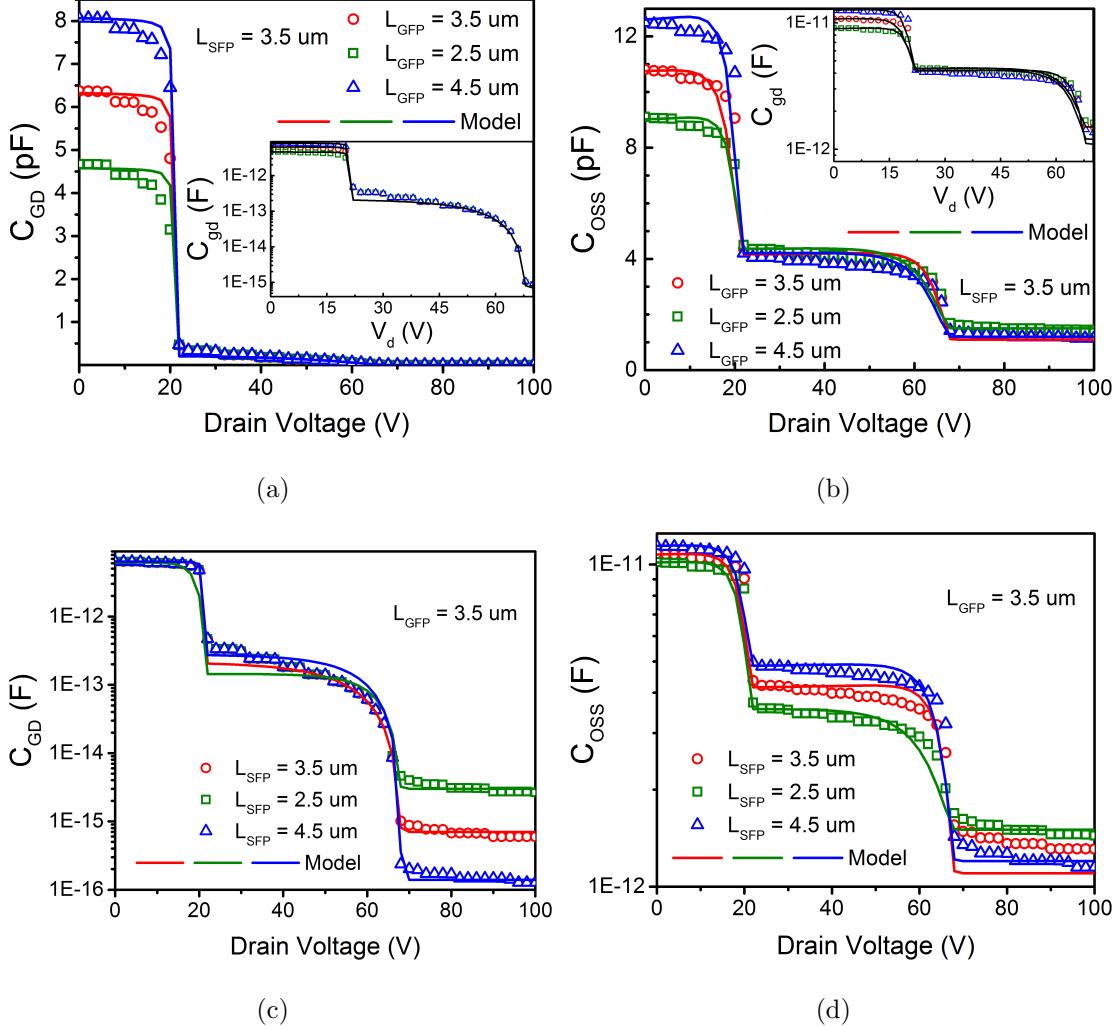


Figure 3.15: Comparison of the modeled (a, c) C_{gd} and (b, d) C_{OSS} with TCAD data under sub-threshold conditions for GaN FP HEMTs with different (a, b) L_{GFP} and (c, d) L_{SFP} . Excellent correlation is obtained between the TCAD and model simulations therefore highlighting scalability feature of the proposed model. Symbols: TCAD, Lines: Model.

is bench-marked with TCAD data extracted for various lengths of FPs (L_{GFP} , L_{SFP}) as shown in Fig. 3.15. The dependence of the capacitance plateaus and the parasitic levels is precisely reproduced by the model for varying FP lengths, thanks to the physical nature of the model. The modeled capacitance plots appear abrupt since each of the plateaus is contributed by a particular FP, however, it must be noted that they are smooth and continuous.

The FP capacitance model is put to use in a circuit simulation as discussed in the next section.

3.5 Mixed-Mode Simulation Setup

Mixed-mode simulations, are a combination of device and SPICE circuit simulations, in which a numerical device model based on physical models is first generated and then put in a SPICE circuit netlist to study its behavior under specific operating conditions. Mixed-mode is a powerful tool to do a thorough examination of the device internal dynamics at particular instants of time, thereby making the task of device as well as circuit optimization significantly easier and inexpensive [109].

The Atlas device discussed in section II is added to the SPICE circuit in Silvaco's mixed-mode utility. As shown in Fig. 3.16, the schematic for a switching demo-circuit is constructed having a typical inductive load, such as in the case of motors, drives etc. Two-level Newtons algorithm is used to numerically solve the circuit and device equations in which a new set of contact voltages for the numerical device is provided by the solution of circuit equations [110]. The device simulator in turn performs the calculation of currents for the numerical device.

3.5.1 Switching Transients

Transient simulations are carried out by applying a 1 MHz pulse, with a pulse-width of 480 ns and 20 ns of rise and fall times at the extrinsic gate. Time-domain waveforms for intrinsic gate (V_{gi}) and drain voltages (V_{di}) and drain current (I_d) are obtained during turn-on and turn-off. Subsequently, we extract the model card for the TCAD device from the $I_d - V_g$, $I_d - V_g$ and $C - V$ data using the parameter extraction procedure described earlier. The same SPICE netlist is used for transient circuit simulation using the model in Keysight's ADS simulator [111] with the same operating conditions as in the mixed-mode netlist. The mixed-mode simulation for a time sweep of 1500 μ s was completed in nearly 3000 seconds using a core-i7 3.4 GHz processor [112], whereas the SPICE simulation using our proposed compact

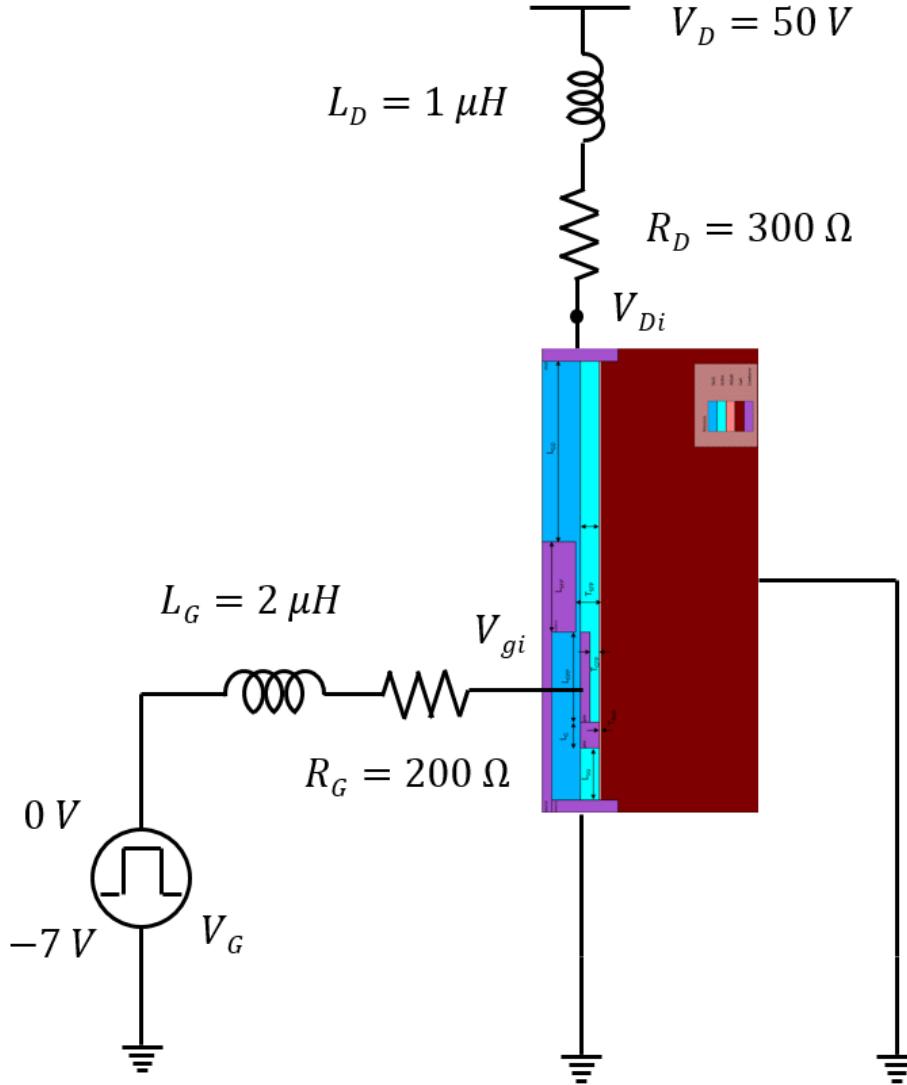


Figure 3.16: Schematic for Mixed-mode simulation using the numerical GaN FP device generated in Atlas. The FP-HEMT is put as the DUT with -7 V and 0 V pulses of 1 MHz at gate. The pulse has a pulse-width of 480 ns, 20 ns rise and fall times. Supply voltage of 50 V is chosen to capture the maximum effect of cross-coupling capacitances on switching transients while an inductive load is put at the drain.

model took 0.65 seconds using Intel Xeon E5 – 2690 2.9 GHz processor [112].

Shown in Fig. 3.17 are the overlay plots for time-domain voltage and current waveforms extracted using mixed-mode and model simulations. During turn-on, the gate drive current (I_{gg}), given as

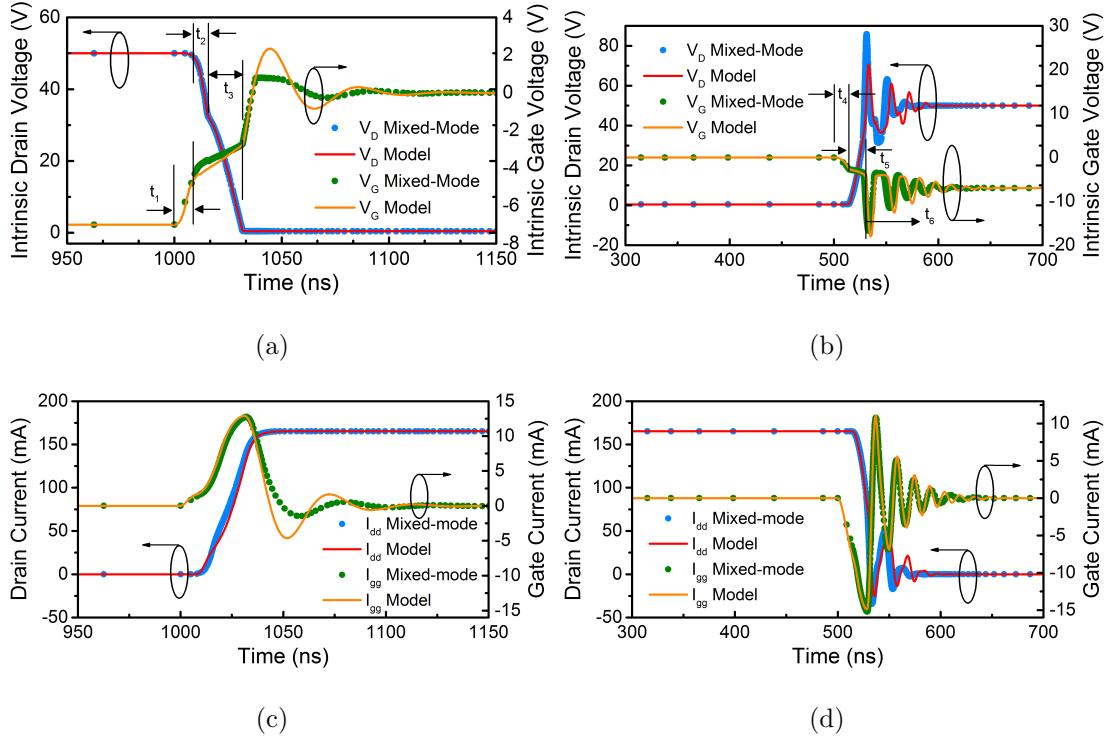


Figure 3.17: Comparison of modeled time-domain waveforms for intrinsic drain voltage, gate voltage and drain current with mixed-mode simulations during turn-on and turn-off. (a), (c) Turn-on by switching applied gate signal from -7 V to 0 V and (b), (d) Turn-off by switching applied gate signal from 0 V to -7 V, keeping applied drain voltage fixed at 50 V. Model accurately predicts drain overshoots due to LC ringing , Miller plateaus due to accurate prediction in sharing of the gate drive current to charge C_{gs} and C_{gd} and the associated gate-drain charge, and the damping of the oscillations.

$$I_{gg} = \frac{d}{dt}(C_{gs}V_{gs} + C_{gd}V_{gd}) \quad (3.26)$$

charges the gate node to the applied gate voltage (V_{gg}) following the standard exponential behaviour given by

$$V_{gs} = V_{gg}(1 - e^{-t/R_g(C_{gs}+C_{gd})}) \quad (3.27)$$

until it reaches the cutoff voltage V_{off} during interval t_1 . Until this point, most of the drive current goes into charging C_{gs} since it is much larger than C_{gd} . After V_{gs}

crosses V_{off} , drain current starts to increase, causing V_d to decrease rapidly. Since C_{gd} is a strongly decreasing function of V_{ds} , and V_{gd} increases as V_{ds} decreases for a fixed V_{gs} , the derivative of $C_{gd}V_{gd}$ in (3.26) becomes significant, causing majority of I_{gg} to charge C_{gd} while keeping V_{gs} more or less fixed. This is known as the Miller-plateau and goes on until the end of interval $t_2 + t_3$, where V_{ds} becomes a constant. We observe a non-zero slope in the Miller-plateau, which can be ascribed to some fraction of I_{gg} charging C_{gs} . Beyond the Miller-plateau, the device is fully ON and V_{gs} continues to rise following (3.27) although with a different time-constant due to higher values for C_{gs} and C_{gd} . Ringing due to LC-oscillations between L_g and input capacitances is also visible beyond t_3 .

As far as the turn-off transients are concerned, V_{gs} in the interval t_4 decreases exponentially from an initial value of V_{gg} , with discharging time-constant corresponding to plateaued values of C_{gs} and C_{gd} since V_{ds} has an initial value of nearly 0 V. It represents the discharging of the input capacitance while the current remains unchanged. A non-zero slope Miller-plateau, similar to that observed while turn-on, is observed during interval t_5 , in which the drain current decreases while C_{gd} keeps discharging. It is during the same interval that the output capacitance C_{oss} gets charged while current drops abruptly. Now that the device is fully off, in interval t_6 , and due to the presence of an inductive load at the drain, which has an intrinsic tendency to oppose any abrupt change in current, the stored inductive energy gets converted into electrical energy in the form of very high voltage developed at the drain, leading to inductive spikes.

3.5.2 Impact of FP Model including Cross-Coupling and Substrate Capacitances

Model predictions are sufficiently accurate to estimate transient characteristics such as the drain overshoots due to LC ringing (see Fig. 3.17(b) and 3.18(b)), Miller plateaus due to accurate prediction in sharing of the gate drive current to charge C_{gs} and C_{gd} (see Fig. 3.17(a) and 3.18(a)) and the associated gate-drain charge, and the damping of the oscillations (see Fig. 3.17(d) and 3.18(d)) in comparison to those

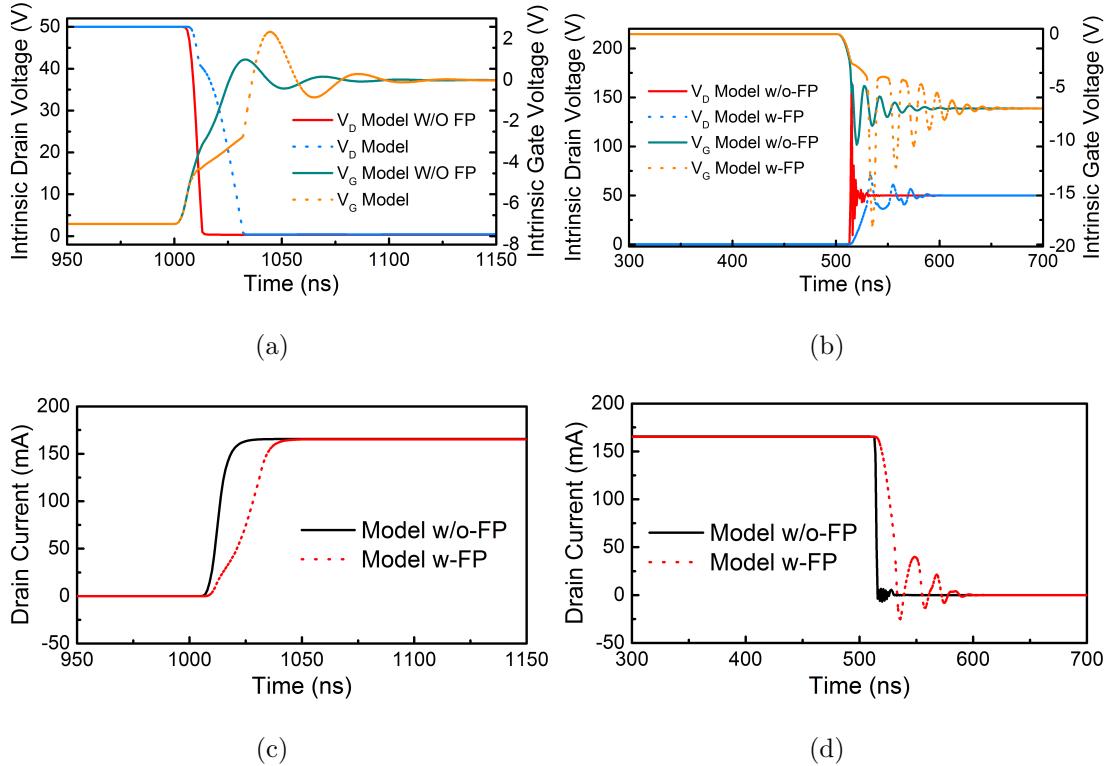
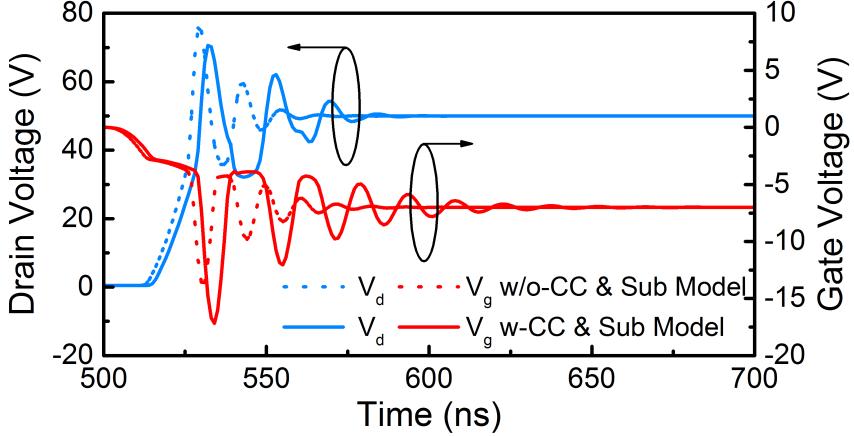


Figure 3.18: Comparison of modeled time-domain waveforms during turn-on and turn-off with and without improved FP Model. (a), (c) Turn-on by switching applied gate signal from -7 V to 0 V and (b), (d) Turn-off by switching applied gate signal from 0 V to -7 V , keeping applied drain voltage fixed at 50 V . Significant difference in the slew-rate as well as ringing of current and voltage waveforms is observed by including the FP model.

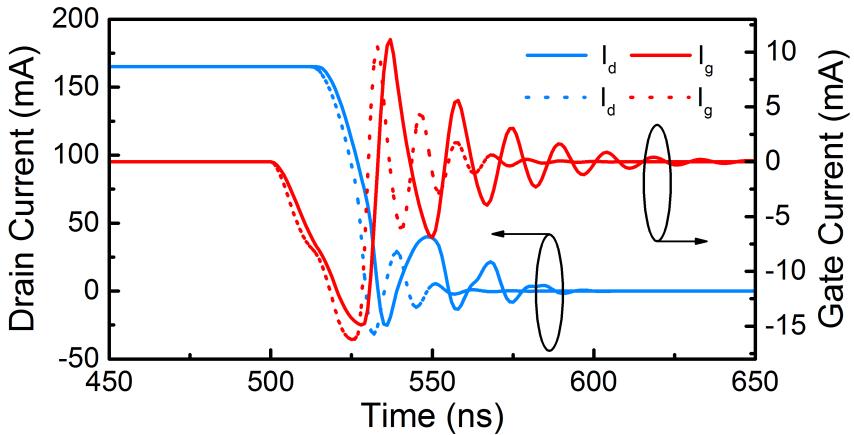
predicted by mixed-mode simulations. Slight mismatch is observed in the turn-off waveform which could be ascribed to a mismatch in the gate resistance between the mixed-mode and modeled characteristics.

A comparison of the transient waveforms during turn-off with and without the improved FP model is presented in Fig. 3.18, which illustrates the significance of the FP model. V_d was set to 50 V in the simulation to ensure that the excursions in V_{di} sweep the bias range for which impact of cross-coupling and substrate capacitances would be noticeable.

To understand the significance of the cross-coupling and substrate capacitances in particular, turn-off transients simulated with and without the cross-coupling and



(a)



(b)

Figure 3.19: Comparison of modeled time-domain waveforms during turn-off with and without cross-coupling and substrate capacitances. Even though the differences may not seem as much as observed in Fig. 3.18, however, from a power-electronics application point of view, differences in slew rates of 25 – 30 % as well as 10 – 15 ns of difference in settling times of waveforms is significant.

substrate capacitances in the model are shown in Fig. 3.19. It represents different rates of charging of the C_{oss} . Due to the different values of C_{oss} in both the cases, the slew-rate as well as the extent of overshoots and their damping is noticeably different for intrinsic voltages and currents at the drain and gate nodes, therefore necessitating the inclusion of cross-coupling and substrate capacitances in the overall FP model for GaN HEMTs.

Summary

To summarize, a surface-potential-based model for the capacitances in a HEMT device with gate and source FPs has been developed. The model is physics based and essentially predicts the contributions due to FP incorporation and captures well the transition regions in the C-V behaviour. The feedback trans-capacitance C_{gd} and drain-source capacitance C_{ds} under sub-threshold conditions due to GFP and SFP respectively are observed which show their presence in the terminal capacitances of the device. The model was validated against experimental data for two different gate widths and excellent fits are obtained for a wide range of bias and temperature conditions. The capacitances due to cross-coupling phenomenon and the substrate electrode were also studied. Thorough examination of these two features was performed using TCAD simulations. Appropriate mathematical expressions were presented to account for charges associated with cross-coupling and substrate electrode capacitances for which existing surface-potential calculation was used. Further, a mixed-mode simulation of an inductive-load demo-circuit was carried out in Silvaco's Mixed-mode for the sake of validation of the proposed model under transient behavior. Comparative analysis of the transient simulations was made by using the model with and without cross-coupling and substrate capacitances. Excellent correlation between model and mixed-mode simulations was observed

Chapter 4

Multi-bias RF Large-Signal Modeling of GaN HEMT and Parameter Extraction Flow

4.1 Introduction

The previous chapter was dedicated towards developing a capacitance compact model for a power GaN device which could be deployed in a power-electronic application. The focus of this chapter is towards the RF specific requirements from a modeling perspective. While it has been made clear that GaN enjoys a special status among material choices for design of RF and microwave transistors [8, 101], a logical move in the modeling community would be to provide suitable RF models for the emerging GaN technology. The models need to be accurate in determining the broadband S-parameters for various biasing conditions. And since large signal operation of a device invokes its non-linear nature, the models should be also capable of reproducing the key nonlinearities. From an RF power amplifier point of view, these models should be precise in determining the optimum load impedances, the gain compressions and harmonics. It would also make perfect sense if it is supplemented by a straightforward model parameter extraction flow.

The existing literature is replete with a plethora of RF large-signal models that

are primarily empirical, table-based, artificial neural-network based or X-parameter based models [70, 113–124]. High fidelity physics-based compact models for GaN HEMTs, particularly surface-potential-based, are desirable and the industry is looking for them for multiple reasons [51, 66] as was outlined in Chapter 2 earlier.

In this chapter, we aim to present the small-signal and large-signal performance of the RF model constructed around the surface-potential-based core of the ASM-GaN-HEMT Model discussed earlier. Moreover, we present a simple RF model parameter extraction procedure wherein only the parasitic components of the intrinsic capacitances are to be extracted using RF measured data whereas the complex bias dependent model is naturally taken care of by fitting the DC-characteristics, which is due to the dependence of the intrinsic charges and current on a single quantity i.e the surface-potential. As a result, the extraction procedure does not require any complex optimization programs [118, 122] as opposed to various empirical or artificial neural network based models in which the current source and intrinsic capacitances are essentially disconnected and bias-independent. This serves as our primary motivation for a physics-based RF compact model for GaN HEMTs that could be readily used as an industry standard for design of state-of-the-art RF circuits.

From an industry point of view, designs need to be yield-oriented. However, device variability usually leads to a significant bottleneck in this regard. In order to get a flavor of the potential reasons of variability, a small exercise of performing a statistical simulation using the described RF large-signal model is done towards the end of this chapter.

The rest of the chapter is organized as follows: We briefly revisit the model description in Section 4.2 and its DC parameter extraction flow is presented in Section 4.3. Trapping and self-heating effects and their modeling are discussed in Section 4.4. In Section 4.5, we carry out the extraction of the multi-bias RF small-signal model valid for a broadband frequency range whereas large-signal performance of the model is studied in Section 4.6. Statistical simulation using the large-signal model is carried out in section 4.7.

4.2 Model Description

The analytical surface-potential (ψ) calculation of the ASM-GaN-HEMT model is used to construct the RF GaN model. The intrinsic gate (Q_{gi}) and drain (Q_{di}) charges are obtained in terms of ψ , as gathered below

$$Q_{gi} = WLC_g \left\{ V_{go} - \frac{1}{2} (\psi_s + \psi_d) + \frac{1}{12} \frac{(\psi_d - \psi_s)^2}{V_{goT}} \right\} \quad (4.1)$$

$$Q_{di} = -\frac{1}{2} WLC_g \left\{ V_{go} - \frac{1}{3} (\psi_s + 2\psi_d) + \frac{1}{12} \frac{\psi_{ds}^2}{V_{goT}} \left(1 + \frac{1}{10} \frac{\psi_{ds}}{V_{goT}} \right) \right\} \quad (4.2)$$

Similarly, drain current I_{ds} is obtained from drift-diffusion framework as given under

$$I_{ds} = \frac{\mu_{eff}}{\sqrt{1 + \theta_{sat}^2 \psi_{ds}^2}} \frac{W}{L} C_g N_f V_{goT} \psi_{ds} (1 + \lambda V_{ds}) \quad (4.3)$$

where

$$V_{goT} = V_{go,k} + \frac{K_B T}{q} - \frac{1}{2} (\psi_{s,k} + \psi_{d,k}) \quad (4.4)$$

Real device effects given in Fig. 4.1 such as velocity saturation, drain induced barrier lowering (DIBL), mobility degradation, channel length modulation (CLM) are incorporated to realize a more realistic device that captures most of the device behavioral nuances.

It is worth mentioning that the feature of having a simultaneous solution for the drain current as well as the capacitances offers a significant advantage in terms of parameter extraction at RF as well as accuracy of the S-Parameter simulations. Empirical models lack such an advantage, since the modeling approach followed in such cases involves isolated expressions for capacitances, transconductance, output conductance etc.

The access region (AR) resistance model [125] is appended to the core model in order to capture the significant modulation of the ON-resistance in GaN devices

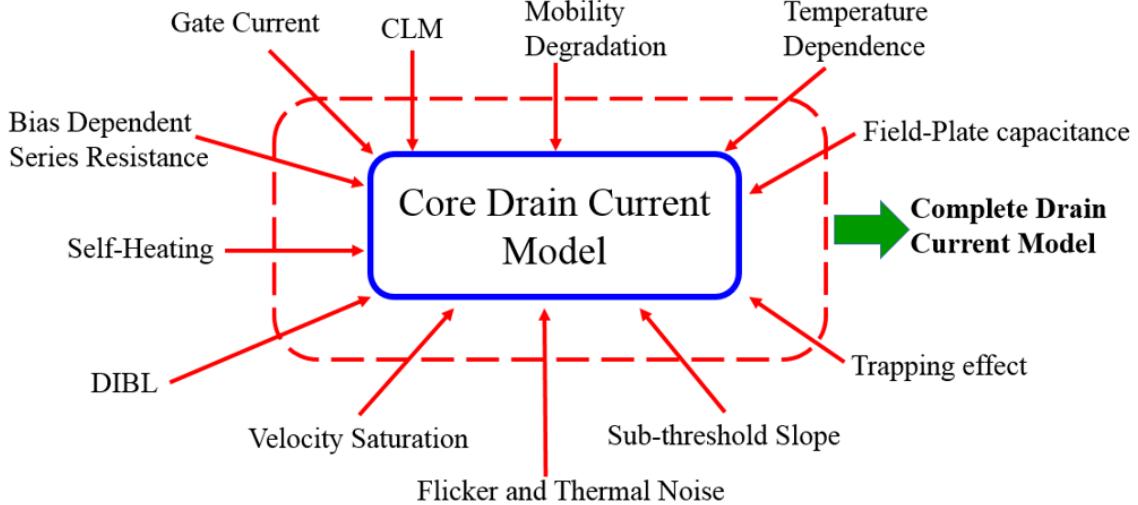


Figure 4.1: Various non-idealities in device behaviour added to the core surface-potential-based drain current model to realize a more realistic device.

due to large ARs particularly at drain so as to support a high breakdown voltage. The current flowing in the AR could be written as a product of AR charge ($N_{s0,A}$) and AR carrier velocity (v_A) as

$$I_{acc} = q \cdot N_{s0,A} \cdot v_A \quad (4.5)$$

Increasing the gate voltage would increase the 2DEG under the gate and lead to increased channel current. Since the AR is an ungated region, $N_{s0,A}$ would not change significantly with any change in V_g . Therefore, in order to support the increased current, v_A would have to change, which initially increases linearly as the potential (V_{AR}) across the AR is increased, and finally saturating to a value $v_{sat,A}$. Therefore, I_{acc} can be written as

$$I_{acc} = qN_{s0,A} \cdot \frac{v_{sat,A} (V_{AR}/V_{AR,sat})}{[1 + (V_{AR}/V_{AR,sat})^\gamma]^{1/\gamma}} \quad (4.6)$$

where $V_{AR,sat} = L_{AR} \cdot (v_{sat,A}/U_{0,A})$ is the voltage across the AR at which the velocity saturates and γ is a parameter that ensures the smooth transition from linear dependence of v_A to a saturated value.

The maximum current supported in the access region would, therefore, be

$$I_{acc,sat} = q \cdot N_{s0,A} \cdot v_{sat,A} \quad (4.7)$$

The low current AR resistance ($R_{ds,0}$) can be calculated as

$$R_{ds,0} = \frac{L_A}{qN_{s0,A}U_{0,A}} \quad (4.8)$$

And the overall AR resistance $R_{ds,A}$ upon rearranging the above set of expressions can be written as

$$R_{ds,A} = \frac{V_{AR}}{I_{acc}} = \frac{R_{ds,0}}{[1 - (I_{acc}/I_{acc,sat})^\gamma]^{1/\gamma}} \quad (4.9)$$

The total AR resistance upon adding the contact resistance (R_c) is finally represented as

$$R_{ds,A} = \frac{R_c}{WN_f} + \frac{L_A}{qWN_fN_{s0,A}U_{0,A}} / \sqrt{1 - \left(\frac{I_{ds}}{WN_fN_{s0,A}v_{sat,A}} \right)^2} \quad (4.10)$$

where L_A is the AR length and $U_{0,A}$ is the AR mobility.

4.3 DC Parameter Extraction

It is well known that various physical effects within the device are intertwined and, therefore, collectively influence the values of parameters. It makes the direct extraction of parameters complicated for the users, and may demand significant number of device measurements for the parameter extraction process. For instance, in order to extract parameters that govern the AR resistances, a set of TLM measurements might come very handy, however, absence of such data might make it tedious to directly extract not only AR resistance model parameters but also other parameters as well.

In this work, we turn our focus on certain key model parameters, listed in Table 4.1, and extract their values using fitting or data identification under different bias

Table 4.1: Key DC Model Parameters

Parameter	Description	Extracted Value
V_{off}	Cutoff Voltage	-2.86 V
N_{factor}	Subthreshold Slope Factor	0.202
C_{dscd}	SS Degradation Factor	0.325 V ⁻¹
η_0	DIBL Parameter	0.117
V_{dscale}	DIBL Parameter	2.981
U_0	Low Field Mobility	33.29 mm ² /V · s
$N_{s0,A}$	AR 2DEG density	1.9e + 17 /m ²
$v_{sat,A}$	AR saturation velocity	157.6k cm/s
R_{th0}	Thermal Resistance	22 Ω

regions so that the different physical effects can be decoupled. The device under test (DUT) is a 125 nm GaN device with a gate periphery of $10 \times 90 \mu\text{m}$, and AR lengths of 200 nm and $1.7 \mu\text{m}$ between the gate-to-source and gate-to-drain nodes respectively. Figs. 4.2 and 4.3 have the intermediate plots where in parameters are extracted by identification from data or tuning within certain bias ranges.

To start with, Fig. 4.2(a) has the $I_d - V_g$ plot in linear and log scale for multiple V_d conditions. V_{off} can be identified from the data as the V_g value at which I_d begins to rise, marking the end of the subthreshold region. It can also be quantified using the well-known g_m -derivative or constant current method. The extracted value of V_{off} should correspond well with the $I_d - V_g$ log plot. This gives a good starting value of V_{off} and can be fine-tuned for better fitting. In the same plot, parameters N_{factor} , C_{dscd} , η_0 and V_{dscale} can be extracted from the log scale curves under subthreshold region. N_{factor} is the subthreshold slope parameter and can be optimized to fit the subthreshold slope for low V_d values. Once N_{factor} has been set, the parameter η_0 can be optimized to adjust DIBL or V_{off} -degradation with increasing V_d . Alternately, η_0 can be extracted from inspecting the data. The shift in subthreshold curves between linear and saturation V_d values for same current should give a rough estimate of η_0 whereas V_{dscale} determines the rate at which V_{off}

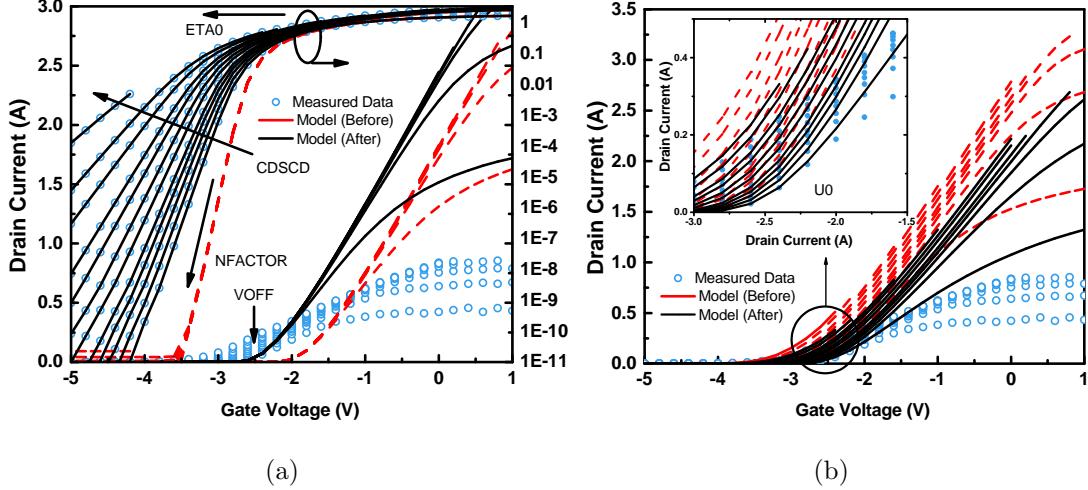


Figure 4.2: Step by step DC Parameter Extraction Flow using multiple bias $I_d - V_g$ plots. (a) V_{off} identification from $I_d - V_g$ linear data. Optimization of N_{factor} , η_0 and C_{dscd} from logarithmic scale $I_d - V_g$ plot after V_{off} is extracted. (b) U_0 is optimized to fit the low V_g conditions. The model results before and after the extraction of parameters are shown in red and black respectively.

changes with increasing V_d . The degradation in subthreshold slope with increasing V_d is decided by C_{dscd} .

The low field mobility parameter U_0 is adjusted by fitting the low V_d and low V_g data conditions in the $I_d - V_g$ linear plot so that mobility as a result of degradation from the vertical field as well as field along the channel can be safely assumed to be U_0 . The Fig. 4.2(b) and its zoomed inset highlight the fitting results after optimizing U_0 .

The AR parameters $N_{s0,A}$ and $v_{sat,A}$ are extracted from $I_d - V_d$ linear and saturation regions respectively as shown in Fig. 4.3(a) and 4.3(b). $N_{s0,A}$ is instrumental in deciding the ON-resistance whereas $v_{sat,A}$ settles the saturation current level. Self-heating effect (SHE) is modeled using the standard R – C network approach, which consists of a thermal resistance (R_{th0}) and a thermal capacitance (C_{th0}). The change in voltage at the thermal node gives the rise in temperature (ΔT), which is added to the nominal temperature (T_{NOM}) at which the device is operating. The negative slope for high current $I_d - V_d$ regions in the DC–IV plots, shown in Fig. 4.3(c),

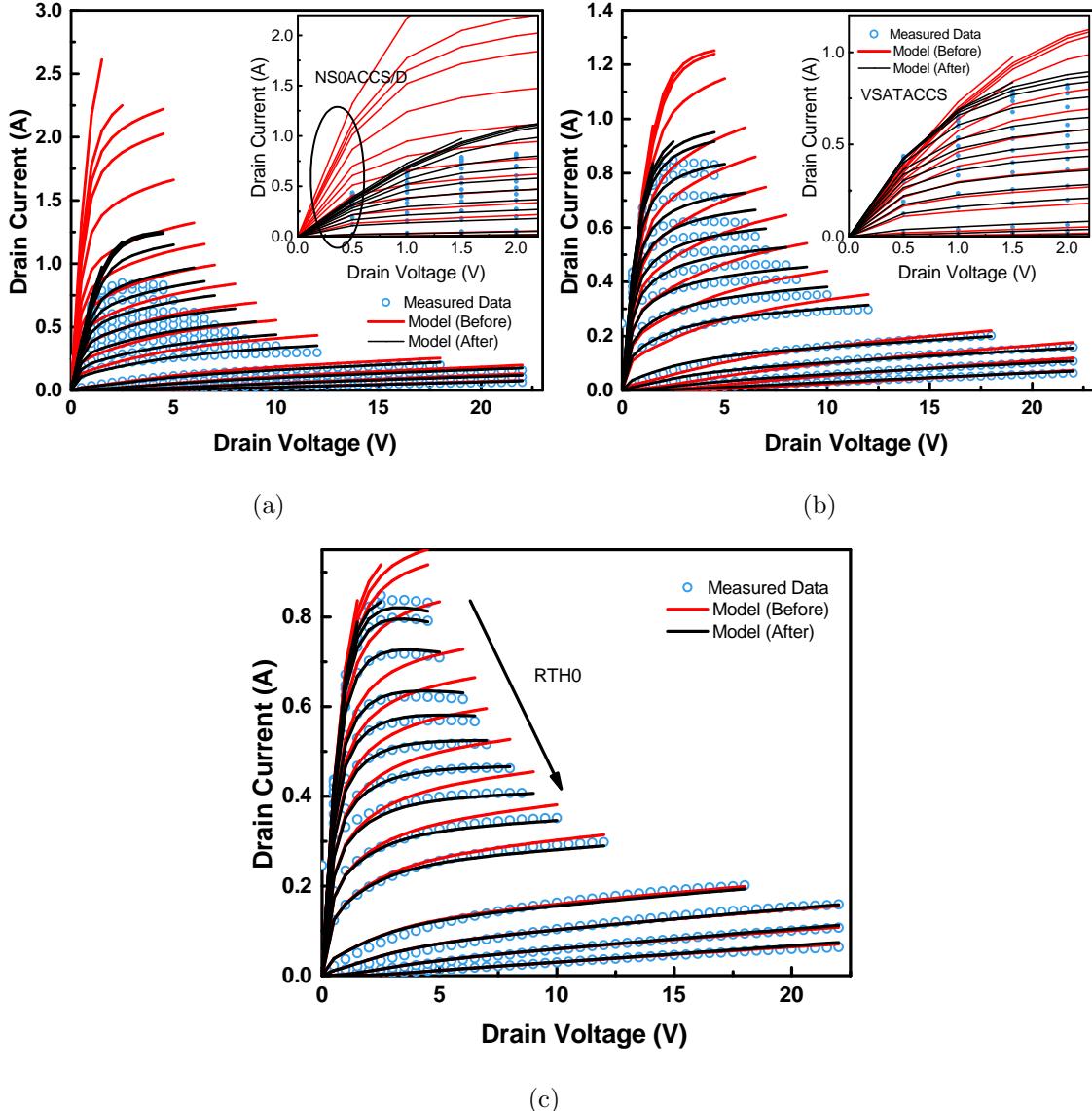


Figure 4.3: Step by step DC Parameter Extraction Flow using multiple bias $I_d - V_d$ plots. (a) The ON-resistance in the linear region of the $I_d - V_d$ plot is fitted by adjusting $N_{s0,A}$. (b) $v_{sat,A}$ is extracted by fitting the saturation current in $I_d - V_d$. (c) R_{th0} is adjusted to fit self-heating. The model results before and after the extraction of parameters are shown in red and black respectively.

illustrates the SHE as predicted by the model and allows extraction of parameter R_{th0} . The flow described above is summarized in Fig. 4.4.

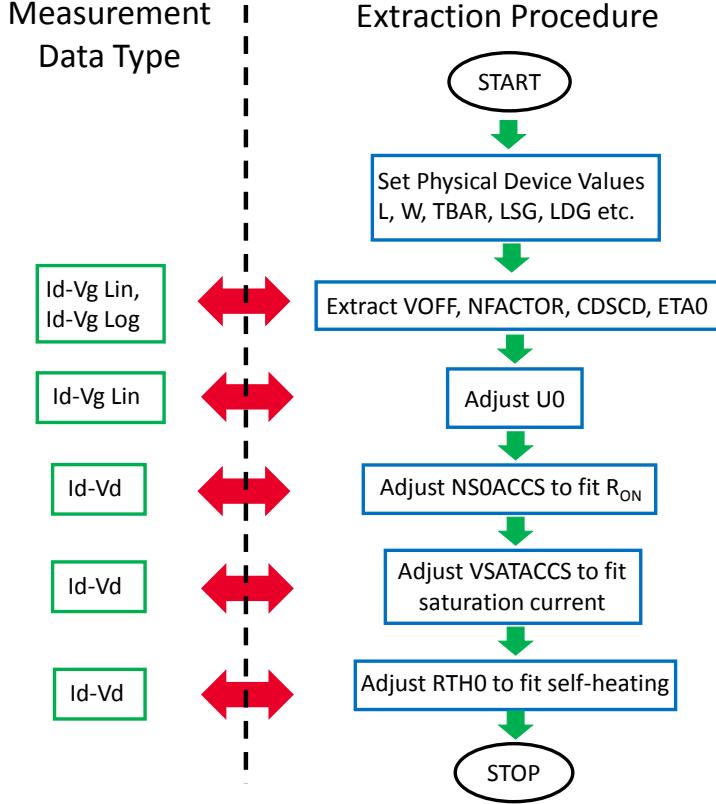


Figure 4.4: DC Parameter extraction flow as described in Section 4.3 to fit not only the drain current but also to obtain intrinsic capacitances. The AR model is incorporated into the intrinsic model as shown in Fig. 4.3.

4.4 Modeling of Self-heating and Trapping Effects

4.4.1 Self-heating Model

Since the DUT is a high power RF transistor, it is supposed to have high drive currents which is enabled by a very high density and high mobility 2DEG at the AlGaN/GaN interface. This leads to an increase in the device temperature which affects the subsequent device behavior which generally manifests as a current slump at high drain biases as shown in Fig. 4.3(c). This phenomenon is known as self-heating effect.

In order to model the self-heating phenomenon a standard R-C network approach is employed, which consists of a thermal resistance (R_{th0}) and a thermal capacitance (C_{th}) as shown in Fig. 4.5. The thermal node voltage gives the rise in

temperature (ΔT), which is added to the nominal temperature (T_{NOM}) at which the device is operating [26]. R_{th0} is extracted from the DC $I_d - V_d$ measurements as shown in Fig. 4.3(c).

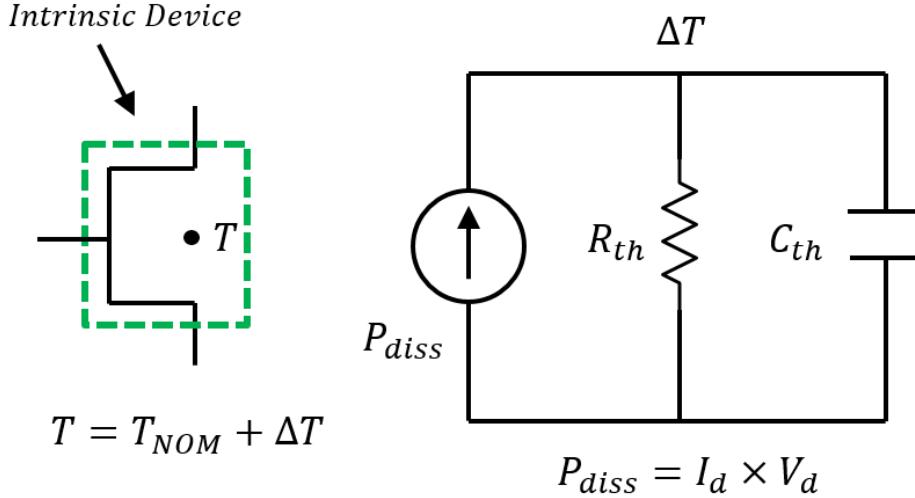


Figure 4.5: $R - C$ thermal network used to model the Self Heating Effect. The value of ΔT generated, which is a function of the dissipated power, is fed back into the compact model to update the operating temperature.

4.4.2 Trap Model

An accurate trap model is crucial in order to estimate the large-signal RF behaviour of GaN HEMTs. A reduction in output power of RF power amplifiers as compared to the expected theoretical output power ($V_{pp}I_{pp}/8$) is ascribed to the various manifestations of trapping such as current collapse, knee walkout, drain-lag, gate-lag etc [28, 126–128]. Pulsed IV characterization in dual-pulse mode at a pulse frequency of 1000 Hz with a duty-cycle of 0.02 %, as indicated in Fig. 4.6, is performed under multiple quiescent drain and gate bias conditions such that both the gate and the drain voltages are pulsed simultaneously from the quiescent bias point. The pulse width of 200 ns and the measurement window of 40 ns within these 200 ns is short enough to ensure iso-thermal and iso-dynamic measurement of the pulsed-IV characteristics. From Fig. 4.7 we observe that the four most important parameters, in which dispersion due to trapping should be modeled, are V_{off} , η_0 , C_{dsqd} and the

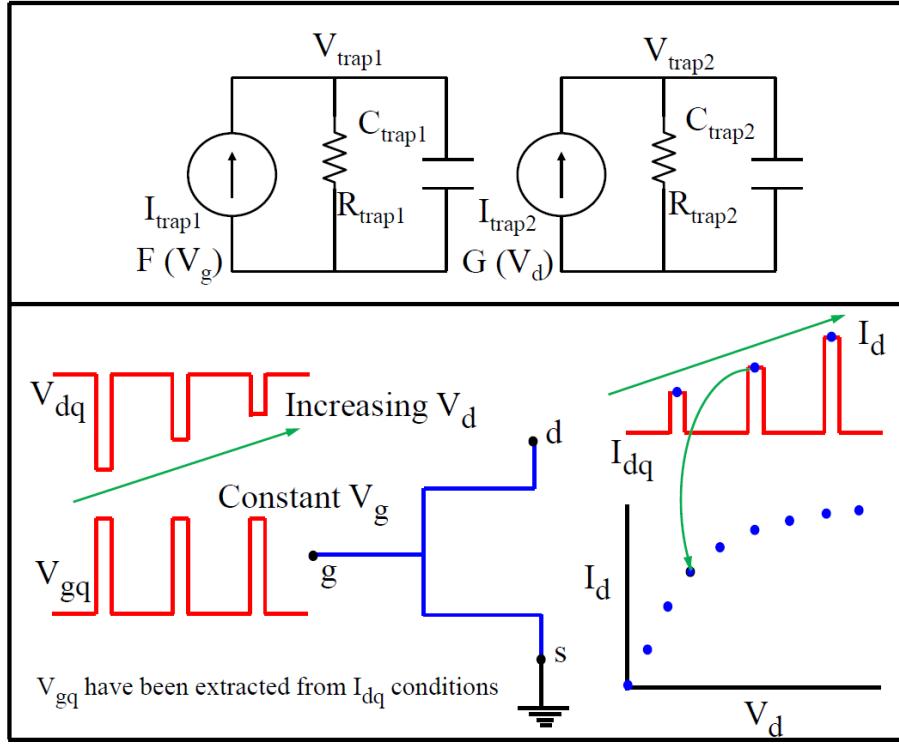


Figure 4.6: (I) Two R – C sub-circuits used for modeling trapping effects, one each for gate-lag and drain-lag. The voltages $V_{trap1,2}$ are fed back into the compact model to update its key parameters as shown in (4.11). (II) The dual-pulsed scheme to do the pulsed-IV simulation.

drain/source AR resistances (R_{ds}). We model this with 2 R – C sub-circuits shown in Fig. 4.6. The node voltages V_{trap1} and V_{trap2} , which represent effects due to gate and drain lag respectively, are fed back into the model to update V_{off} , η_0 , C_{dscd} and R_{ds} , given as

$$V_{off}(Trap) = V_{off} + (V_{OFFTR} \cdot V_{trap2}) \quad (4.11)$$

$$\eta_0(Trap) = \eta_0 + (\eta_{0TR} \cdot V_{trap2}) \quad (4.12)$$

$$C_{dscd}(Trap) = C_{dscd} + (C_{DSCDTR} \cdot V_{trap2}) \quad (4.13)$$

$$R_{ds}(Trap) = R_{ds} - (R_{TR1} \cdot V_{trap1}) + (R_{TR2} \cdot V_{trap2}) \quad (4.14)$$

where V_{OFFTR} , η_{0TR} , C_{DSCDTR} , R_{TR1} and R_{TR2} are used as parameters. Shown in Fig. 4.7 are accurate model fits for pulsed $I_d - V_g$ and $I_d - V_d$ for multiple quiescent bias conditions, validating the proposed trap model.

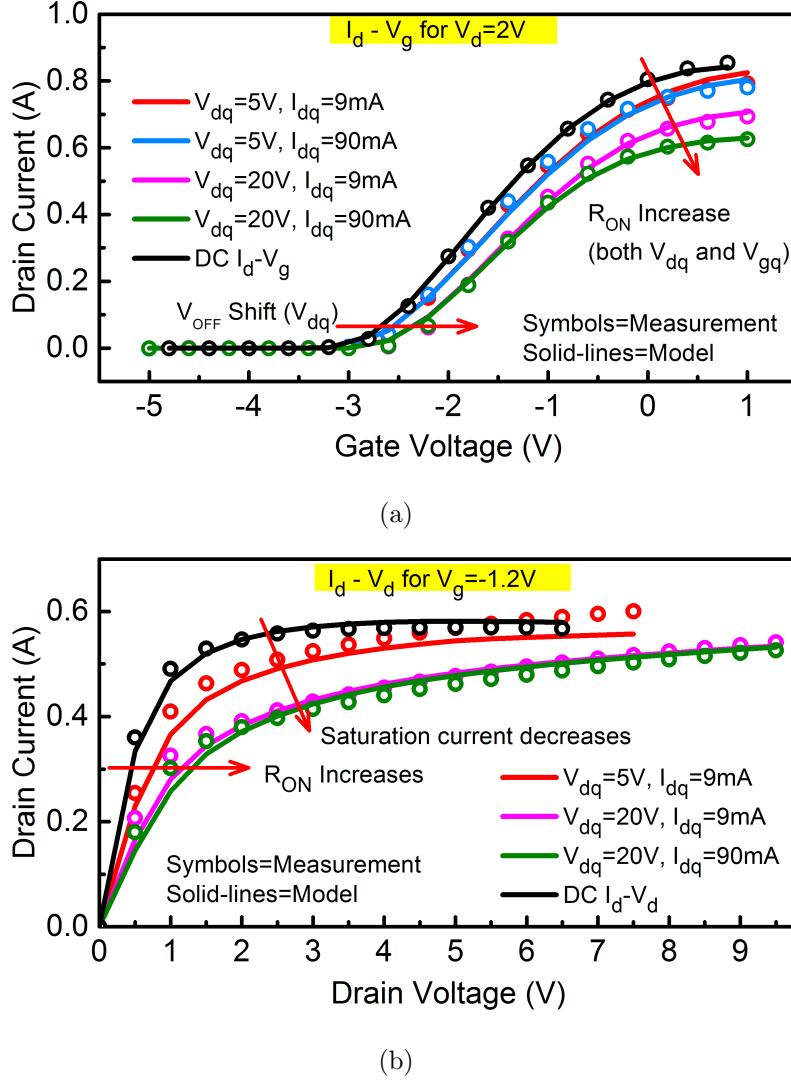


Figure 4.7: Correlation between measured and modeled (a) Pulsed $I_d - V_g$ and (b) Pulsed $I_d - V_d$ characteristics using the trap model. Accurate fits are seen for multiple quiescent bias conditions ($V_{dq} = 5, 20$ V and $I_{dq} = 10, 100$ mA/mm), which is essential for the non-linear RF behavior of the model.

4.5 RF Parameter Extraction

RF small-signal equivalent circuit SS-EC is shown in Fig. 4.8. The overall SS-EC has gate (GMF) and drain (DMF) manifolds or pads, feeding the signals to gate and drain ports respectively. It also has the source manifold (SMF) or via-holes, through which the source-pad is connected to the back-plane metallization. Beyond the manifolds are bus-inductances L_{xg} , L_{xd} and L_{xs} that represent the connection

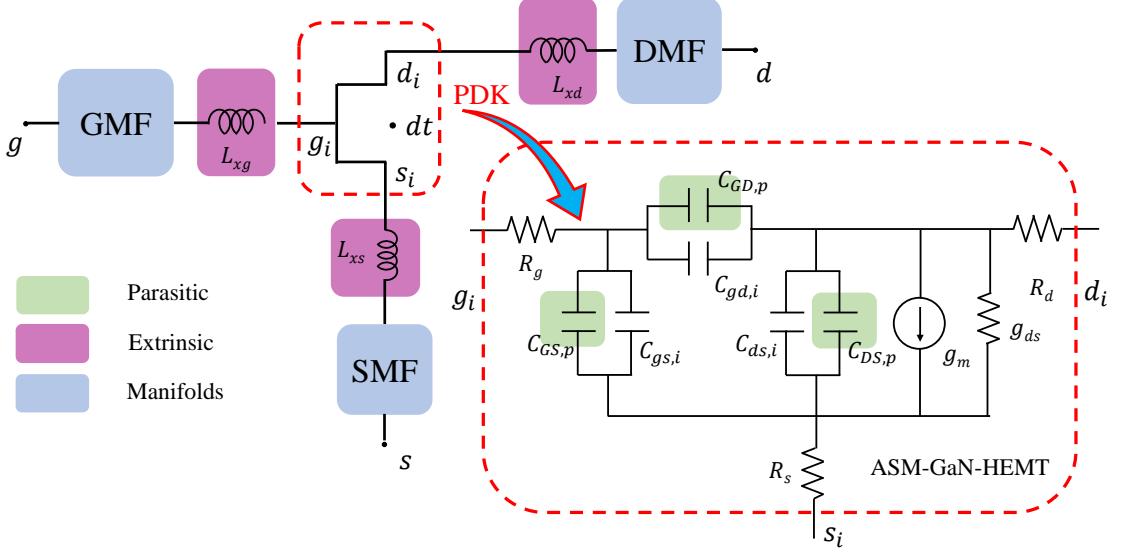


Figure 4.8: Small Signal Equivalent Circuit Model of the overall device including the intrinsic device as described by the ASM-HEMT model PDK. Access resistances R_g , R_d and R_s are included in the intrinsic core model whereas only the bus-inductances form the extrinsic level parasitics. Standard transmission line models are used for manifolds.

between the pads and the actual DUT, which itself is governed by the process design kit (PDK). The zoomed inset shows the equivalent circuit representation of the intrinsic DUT featuring parasitic capacitances $C_{GS,p}$, $C_{GD,p}$ and $C_{DS,p}$ and access resistances R_g , R_d and R_s .

With the bulk of the parameter extraction exercise done for DC–IV in Section 4.3, the transconductance (g_m), output conductance (g_{ds}), intrinsic capacitances ($C_{gs,i}$, $C_{gd,i}$ and $C_{ds,i}$) and intrinsic gate resistance ($R_{g,i}$) are simultaneously determined since they depend on a single quantity i.e ψ . Additionally, AR resistances, R_d and R_s , are also fitted while extracting values for $N_{s0,A}$ and $v_{sat,A}$ during DC parameter extraction. So, we now are only left with the task of extracting the parasitic capacitances and the gate finger resistance ($R_{g,f}$) in addition to the inductances.

Keysight’s ADS simulator is used to perform all the model simulations. Broadband S-parameters (0.5 – 50 GHz) measured under multiple bias conditions are used for RF parameter extraction. The lumped-element representations of the XMF and

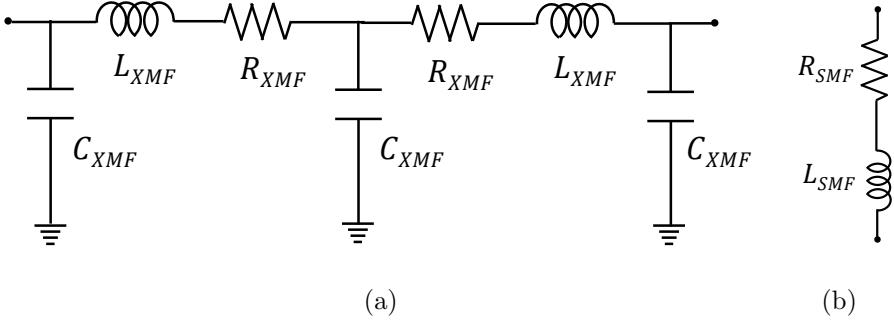


Figure 4.9: (a) The Gate/Drain Manifold and (b) Via-holes or the Source Manifold.

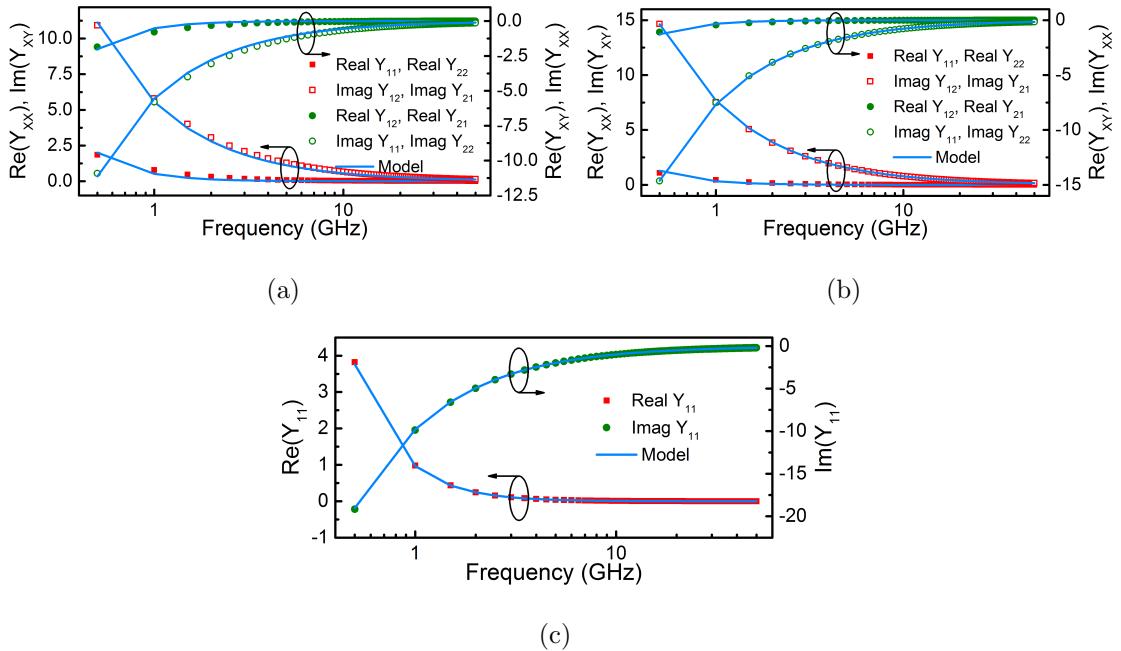


Figure 4.10: Measured and modeled Y-parameters for (a) GMF (b) DMF and (c) SMF. For (a, b) the Y-parameters are symmetric and X & Y are 1 or 2.

the SMF are shown in Fig. 4.9(a) and 4.9(b) respectively, where X could be G or D. Shown in Fig. 4.10 are the measured and modeled fits for manifold Y-parameters using the symmetrical lumped manifold models shown in Fig. 4.9. The manifolds are deembedded and S-parameters for each of the manifolds in the form of 2-port S-parameter files are obtained using on-wafer Thru Reflect Line (TRL) deembedding [129, 130].

The extrinsic-level measurements, obtained after deembedding the manifolds, are henceforth employed for parameter extraction. We start with the intrinsic ele-

ment extraction following the standard low-frequency Y-parameter based approach [131]. It must be noted that due to the inclusion of the AR model in the core model, as explained in Section 4.3, we can use it to our advantage by omitting R_s and R_d from the intrinsic SS–EC since their effect on g_m and g_{ds} is already captured. This significantly simplifies our hand-analysis for RF parameter extraction without compromising on the accuracy due to omission of AR resistances as reported in [131].

We start with a low frequency approximation of ignoring the bus inductances in the SS-EC and derive the Y-parameters as

$$Y_{11} = \frac{\omega^2 C_{gg}^2 R_g}{1 + \omega^2 C_{gg}^2 R_g^2} + \frac{j\omega C_{gg}}{1 + \omega^2 C_{gg}^2 R_g^2} \quad (4.15)$$

$$Y_{12} = -\frac{\omega^2 C_{gd} C_{gg} R_g}{1 + \omega^2 C_{gg}^2 R_g^2} - \frac{j\omega C_{gd}}{1 + \omega^2 C_{gg}^2 R_g^2} \quad (4.16)$$

$$Y_{21} = \frac{g_m - \omega^2 C_{gd} C_{gg} R_g}{1 + \omega^2 C_{gg}^2 R_g^2} - \frac{j\omega(C_{gd} + g_m C_{gg} R_g)}{1 + \omega^2 C_{gg}^2 R_g^2} \quad (4.17)$$

$$\begin{aligned} Y_{22} = g_{ds} + & \frac{\omega^2 (C_{gs} C_{gd} R_g + R_g C_{gd} C_{gg} (1 + g_m R_g))}{1 + \omega^2 C_{gg}^2 R_g^2} \\ & + j\omega C_{ds} + \frac{j\omega C_{gd} (1 + g_m R_g) + j\omega^3 C_{gs} C_{gd} C_{gg} R_g^2}{1 + \omega^2 C_{gg}^2 R_g^2} \end{aligned} \quad (4.18)$$

where $C_{gg} = C_{gs} + C_{gd}$ & $C_{mn} = C_{mn,i} + C_{mn,o}$, with m, n being node g, d or s . At low frequencies (< 10 GHz), we can ignore the terms $\omega^2 (C_{gs} C_{gd} R_g + R_g C_{gd} C_{gg} (1 + g_m R_g))$, $j\omega^3 C_{gs} C_{gd} C_{gg} R_g^2$, $\omega^2 C_{gd} C_{gg} R_g$ and $\omega^2 C_{gg}^2 R_g^2$ to simplify (4.15–4.18) to extract SS-EC elements.

The overlays of measured and modeled plots for intrinsic SS-EC elements plotted against frequency are shown in Fig. 4.11. The values of the parasitic capacitances are adjusted to settle the levels of the capacitance plots, whereas the trap-model takes care of the g_{ds} dispersion. The only dispersion in g_m at low frequencies

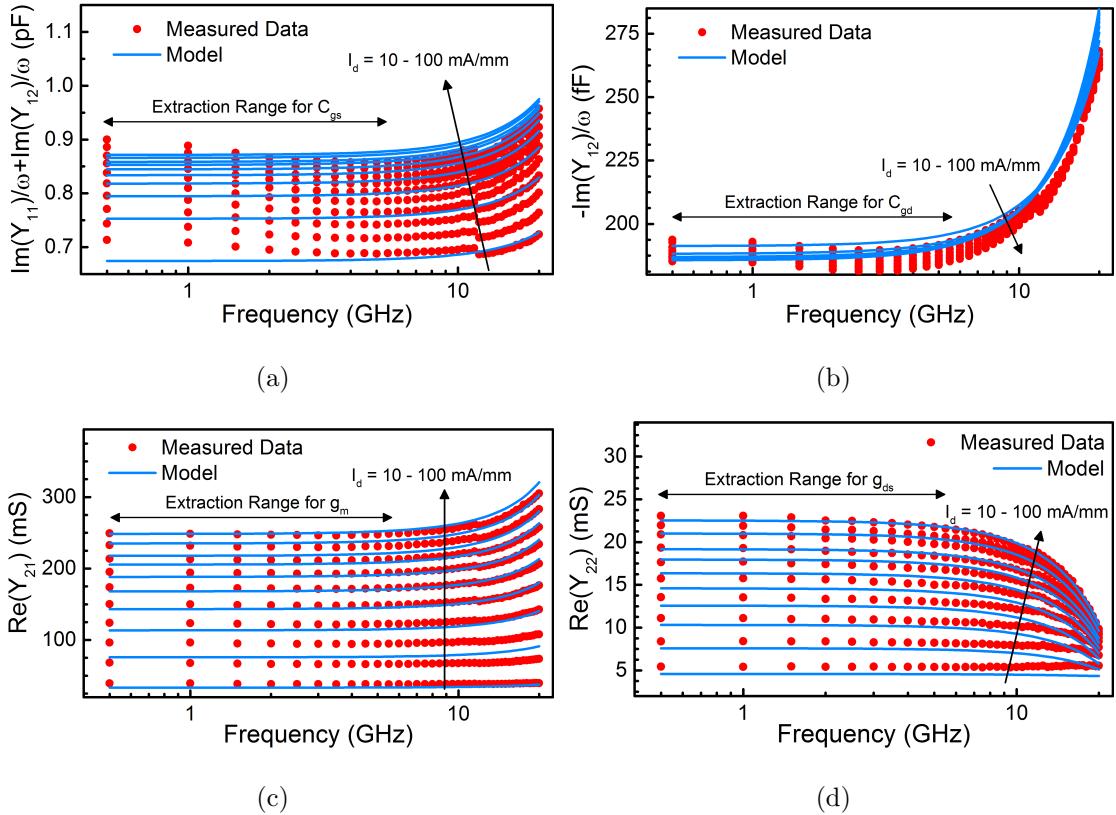
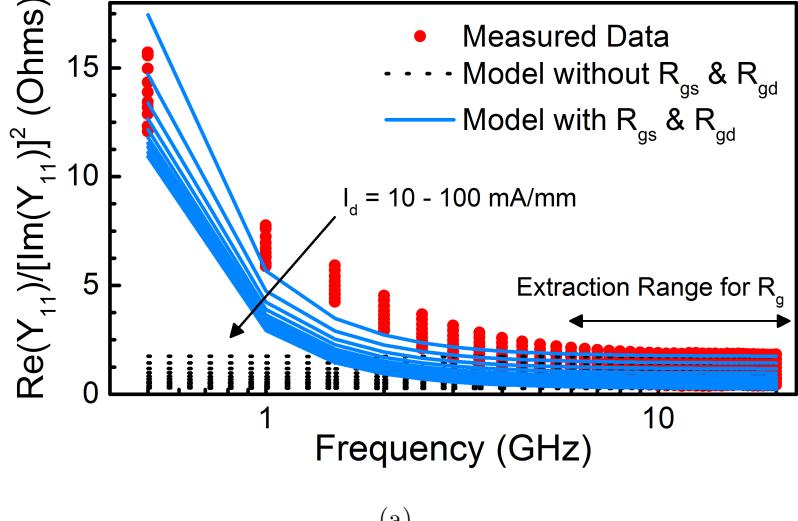


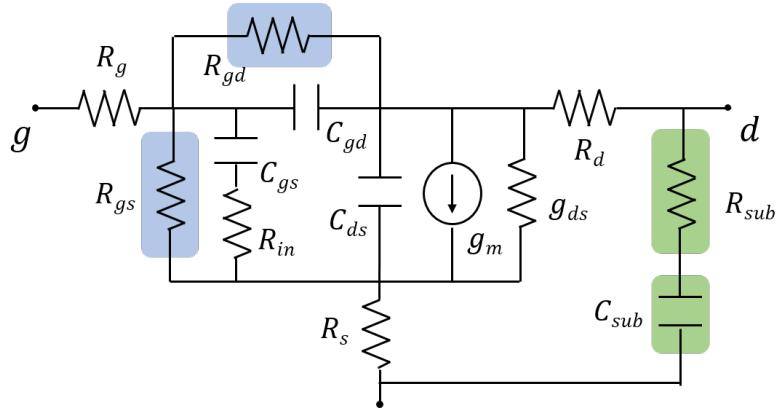
Figure 4.11: Extracted SS-EC (a) C_{gs} (b) C_{gd} (c) g_m and (d) g_{ds} for $V_d = 5$ V and 10 gate bias conditions. Parasitic capacitances are adjusted to values given in Table 4.2 to fit model and measured data for (a–b). A sufficiently broad frequency range (≈ 10 GHz) is observed for extraction for which frequency-independent behavior of SS-EC elements is seen after which inductive effects dominate.

in our model is due to self-heating, and decided by the values of self-heating parameters R_{th0} and C_{th0} . However, their bias dependence is already taken care of by the core surface-potential-based model. The quasi-independence of these elements against frequency, which is a standard benchmark to verify the validity of the proposed RF model, is observed for nearly 10 GHz giving us a significant extraction range before which inductive effects come into the picture.

It must be noted that R_g increases abruptly as we move to lower frequencies (see Fig. 4.12(a)), which can be ascribed to the differential gate-channel resistances seen in GaN devices due to current flowing through gate-source and gate-drain diodes [132]. We model it by including large resistors R_{gs} and R_{gd} across gate-source



(a)



(b)

Figure 4.12: Large resistors R_{gs} and R_{gd} are included in the intrinsic SS-EC to capture the differential gate resistance accounting for current flowing through the gate-source and gate-drain Schottky diodes respectively. Their inclusion significantly impacts the overall gate resistance (R_g) at low frequencies as shown in Fig. 4.12(a). R_{sub} and C_{sub} are included to capture the substrate loss at the output port. It must be noted that AR resistances R_s and R_d have been omitted since their impact is already embedded in g_m and g_{ds} as described in Section 4.3.

and gate-drain terminals as shown in Fig. 4.12(b). Nonetheless, we still find a substantial frequency range for extraction of gate finger resistance $R_{g,f} = R_g - R_{g,i}$ as illustrated in Fig. 4.12(a). The extracted values of parasitic capacitances and resistances are shown in Table 4.2.

Table 4.2: Extracted Capacitances and Resistances

$C_{GS,p}$	$C_{GD,p}$	$C_{DS,p}$
510 fF	165 fF	182 fF
$R_{g,f}$	R_{gs}	R_{gd}
0.5 Ω	19 kΩ	19 kΩ

Substrate loss is captured using the standard RC series network across the drain and source nodes as shown in Fig. 4.12(b). The substrate network affects the g_{ds} -dispersion observed at low frequencies which in turn affects S_{22} of the device. Ideally, the time constant corresponding to the RC substrate network should be determined by low frequency Y-parameters. Since the broadband S-parameter measured data for the device at our disposal starts from 500 MHz, we therefore cannot extract the exact values of R_{sub} and C_{sub} . So, a convenient time constant is chosen such that it accounts for gds-dispersion well below 500 MHz while giving the best fits at the same time. In our case, its value was set to 50 μ s or 20 kHz.

It is interesting to note that the extrinsic inductances and the bias-dependent intrinsic capacitances resonate at higher frequencies, a manifestation of which is the occurrence of dips and peaks in extrinsic-level Y-parameters, as shown in Fig. 4.13 as an illustrative example. These features can be used to extract the bus-inductances, tabulated in Table 4.3, in order to match the peaks corresponding to measured and modeled Y-parameters. As can be seen, the model is highly accurate in capturing the resonating behavior for multiple bias conditions due to varying capacitances with bias, thereby acting as an alternate way of validating the model extraction procedure. The negative value of L_{xs} can be ascribed to an improper calibration or de-embedding of the pad parasitics.

Table 4.3: Bus-Inductances (pH)

L_{xg}	L_{xs}	L_{xd}
10.1	-6.08	8.25

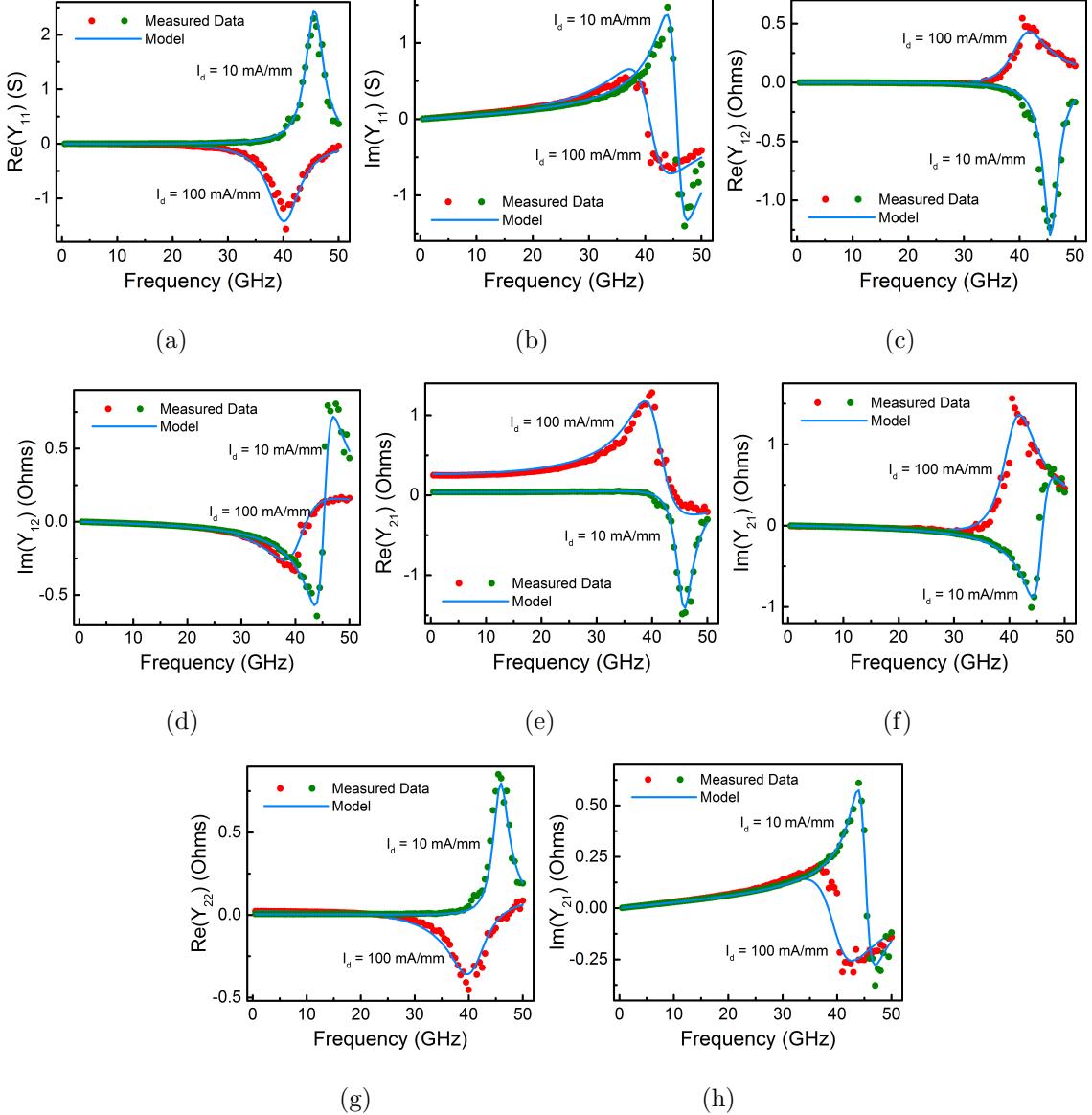


Figure 4.13: Comparison between modeled and measured broadband extrinsic-level Y-parameters. Y_{11} are shown here for illustration. The model accurately captures the peaks and dips and their bias dependence which is a manifestation of the interaction between the intrinsic capacitances and the extrinsic inductances. The values of bus-inductances can be fine-tuned to fit the peaks/dips in measured and modeled extrinsic-level Y-parameters.

To conclude the RF parameter extraction process, overlays of the broadband S-Parameters for a frequency range of 0.5 – 50 GHz are shown in Fig. 4.14. The results shown are for 20 different bias conditions: 5 V and 20 V at drain with 10

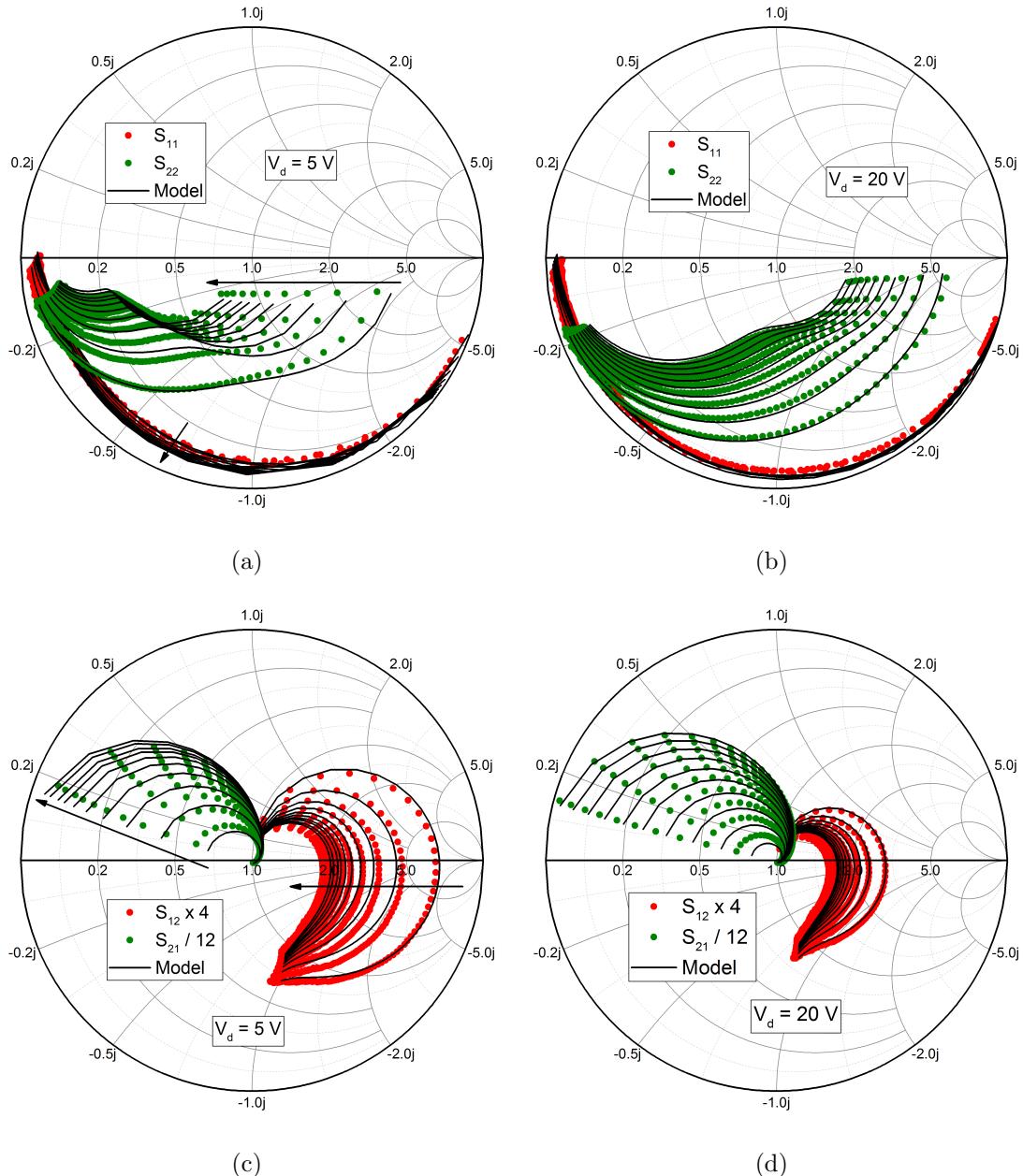


Figure 4.14: Comparison between modeled and experimentally measured data of broadband extrinsic-level S-Parameters for frequency 0.5 – 50 GHz. Smith plots for S_{11} and S_{22} (a–b), S_{12} and S_{21} (c–d) are shown for 2 different drain-bias conditions, with 10 different gate biases ($I_d = 10 - 100 \text{ mA/mm}$) for each drain condition. The model is accurate in capturing the bias dependence of S-parameters which validates the accuracy of the core intrinsic model as well as the RF parameter extraction procedure. The arrows indicate the direction of increasing I_d .

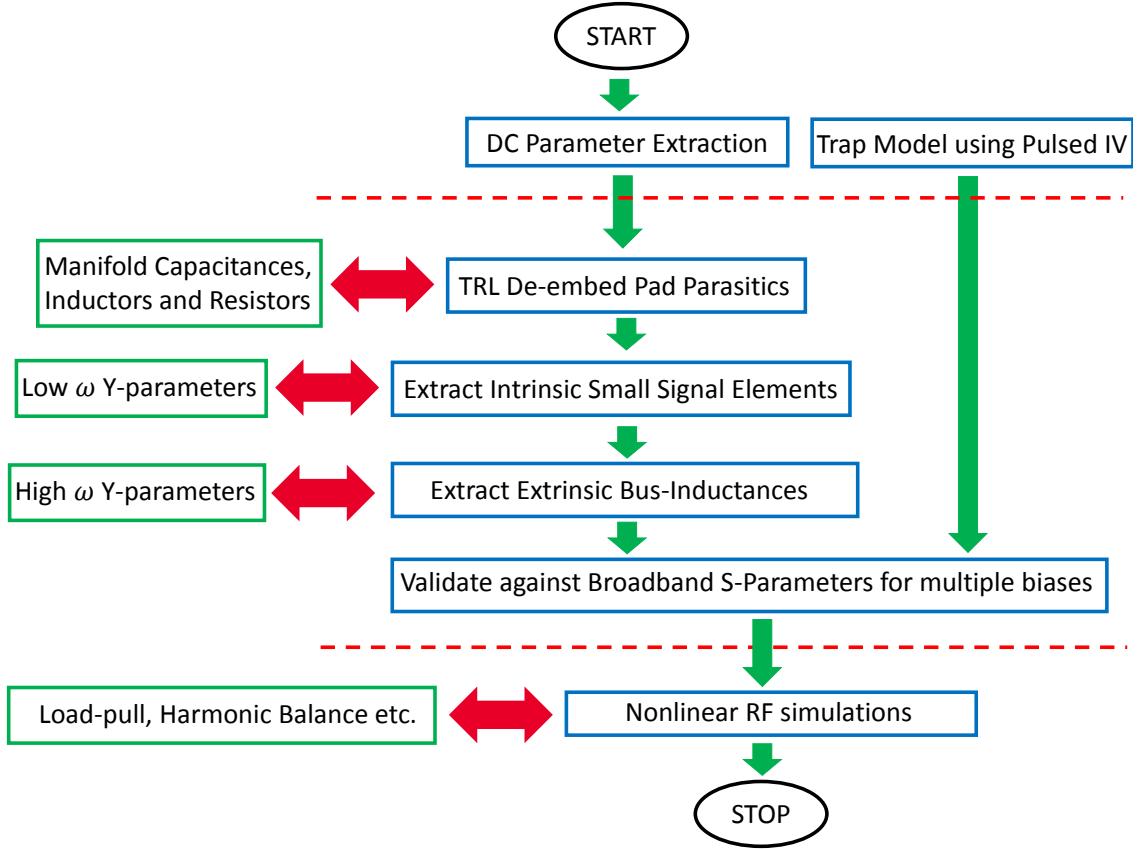


Figure 4.15: RF Parameter extraction flow as described in Section 4.5 to extract the RF small signal model for the GaN device. The flow is straightforward and does not require any optimization and is validated by accurate correlation between measured and modeled broadband S-parameters as shown in Fig. 4.14.

different voltage values at gate, that give a quiescent current spanning over an order of magnitude (10 – 100 mA/mm). A high level of correlation between the measured data and the model for a wide variety of bias conditions is observed, which is an important model capability as far as design of various PA classes under varying drain supply voltages is concerned. Also, the model is accurate in predicting the bias-dependence of the kink-effect in S_{22} , which can be of significance in design of the output matching network for PAs [133]. The entire parameter extraction flow is straightforward and does not require any optimization algorithms as is summarized in Fig. 4.15.

4.6 Large-Signal Model Behavior

To examine the large-signal performance of the proposed model, correlations between measured and model generated Output-Power (P_{OUT}) and Power-Added-Efficiency (PAE) load-pull plots are made. Shown in Fig. 4.16 is the ADS load-pull schematic

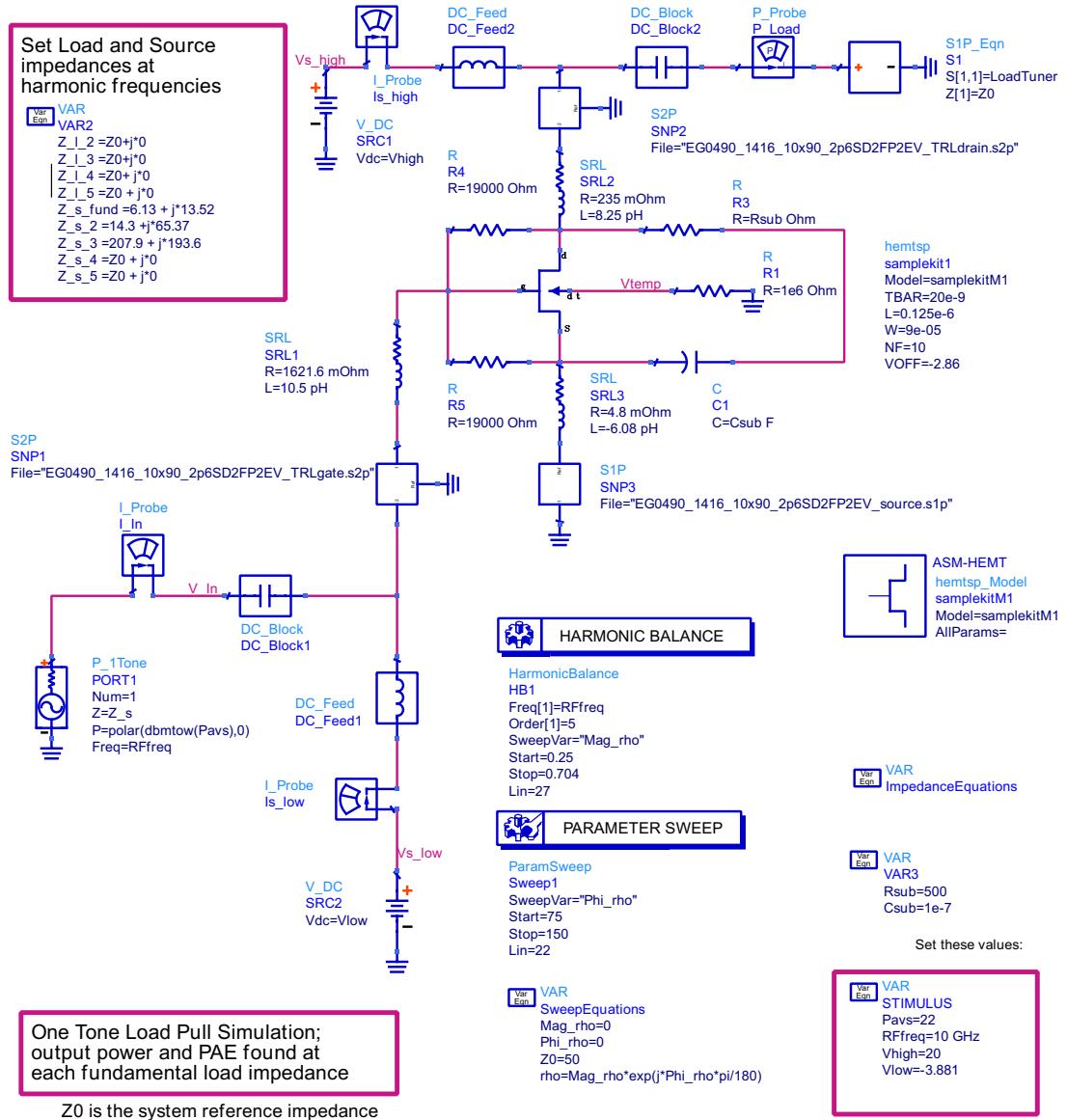


Figure 4.16: ADS schematic for simulating load-pull contours using the embedded model. Right in the centre is the DUT which is governed by the ASM-GaN-HEMT PDK. Bias conditions, operating frequency, source impedance values are indicated in the red boxes.

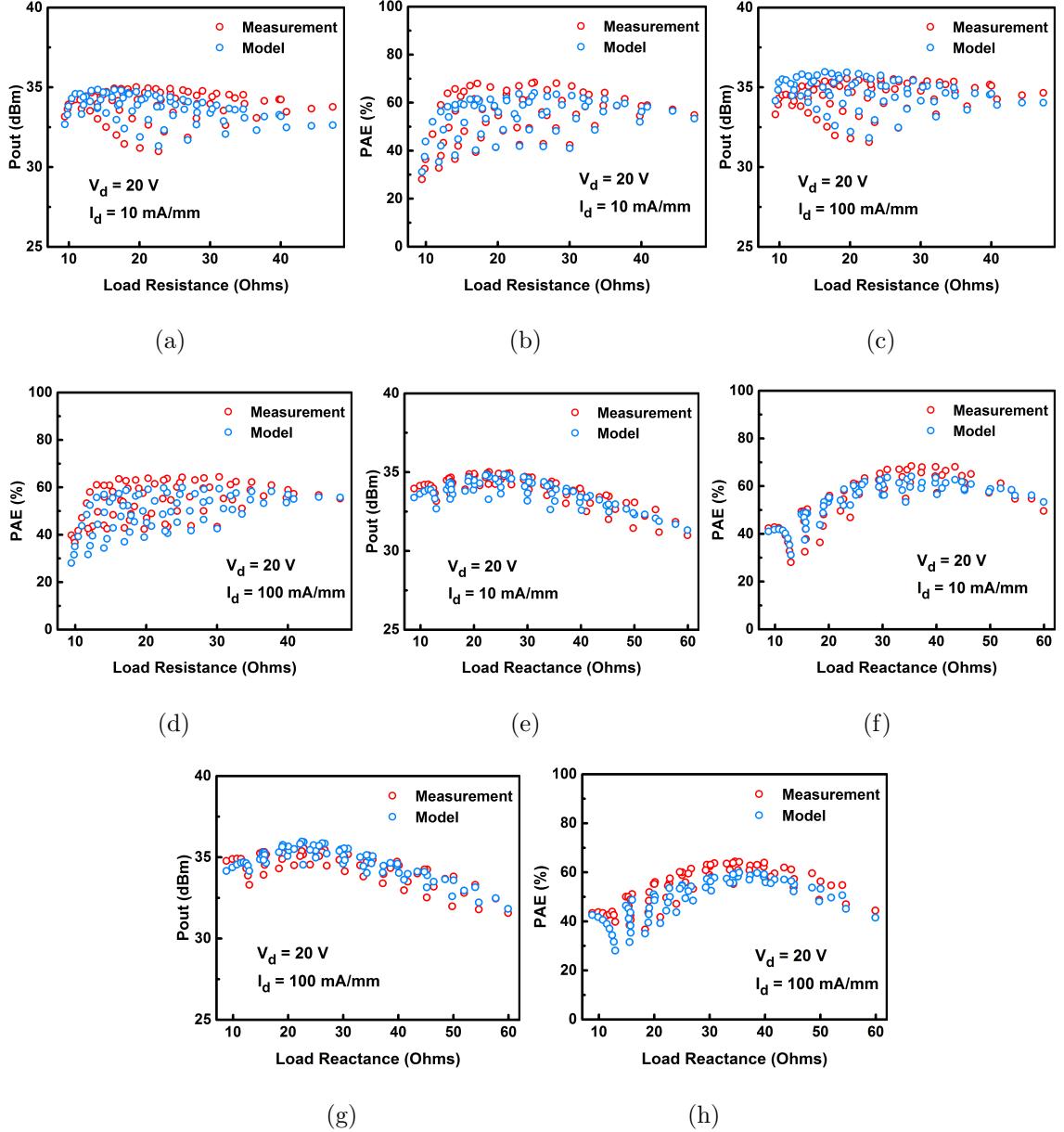


Figure 4.17: Discrete load-sweeps for P_{OUT} and PAE against real and imaginary loads for multiple bias conditions, at 10 GHz signal frequency. The model accurately predicts the P_{OUT} and PAE maxima as well as their mutual tradeoffs upon varying the load resistance/reactance.

using the model PDK and device extrinsic components. The measured load-pull data is obtained using load tuners from Focus Microwaves with an input-power (P_{IN}) level of 22 dBm at 10 GHz fundamental frequency. Figs. 4.17(a)-4.17(h) provide a deeper clarity on the impact of load impedances on P_{OUT} and PAE, wherein the load-pull

data is reinterpreted into discrete load sweeps and compared for both measured data and model estimations. The variation of P_{OUT} and PAE and their mutual trade-offs as real and imaginary parts of the load are swept is captured accurately by the model.

Table 4.4: Load Impedances

	Freq	10 mA/mm	100 mA/mm
Max. PAE	f_0	$22.46 + j38.54$	$30.53 + j34.35$
	f_1	$40.61 - j93.39$	$37.32 - j73.44$
	f_2	$11.39 - j0.07$	$14.77 + j10.83$
Max. P_{OUT}	f_0	$19.57 + j22.83$	$19.57 + j22.83$
	f_1	$253.48 - j65.72$	$253.48 - j65.72$
	f_2	$15.66 - j31.21$	$15.66 - j31.21$

Given in Table 4.4 are the values of optimum load impedances obtained through load-pull contours for maximum P_{OUT} and PAE under different gate bias conditions. In Fig. 4.18(a)-4.18(d), the overlays for measured and modeled contours exhibit high degree of resemblance which highlights the capability of the proposed model to capture the non-linear nature of GaN HEMTs responsible for predicting P_{OUT} and PAE. Since the load-pull data is measured at pad-level, the model representation requires us to append the extracted manifolds from Section 4.5 to the extrinsic-level model in the ADS simulator as shown in Fig. 4.16.

Finally, power-sweep simulations are performed to study the model performance when the device is driven into compression as shown in Fig. 4.19. The load impedances are set for maximum PAE. The model does a decent job in predicting the non-linear behavior of the device particularly gain compression after the device hits the non-linearity and the subsequent peaking of PAE at power back-off. Such accuracy is achieved for multi-bias conditions with the help of precise modeling of trapping and self heating phenomena during large signal operation. These results indicate the readiness of the model to be used as an industry standard for GaN

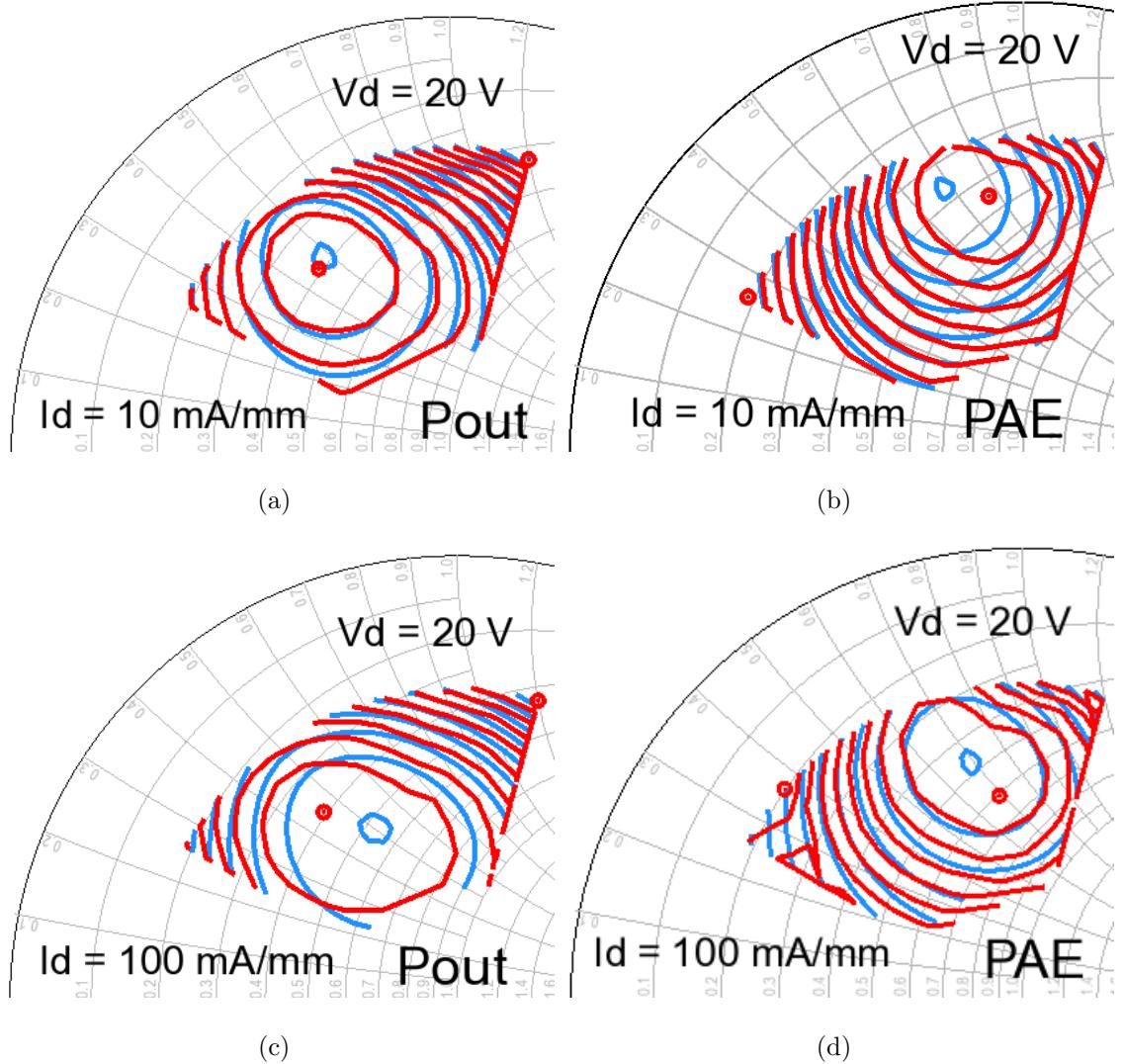


Figure 4.18: Comparison of measured and modeled P_{OUT} (a, c) and PAE (b, d) load-pull contours for $V_d = 20$ V at two current densities $I_d = 10$ and 100 mA/mm. The smith chart region is sampled for $0.26 < \text{Magnitude}(\Gamma) < 0.71$ and $70^\circ < \text{Phase}(\Gamma) < 160^\circ$ for standard $50\ \Omega$ impedance. The model accurately predicts the P_{OUT} and PAE maxima as well as their mutual tradeoffs upon varying the load impedance. Maximum P_{OUT} : 35.02 dBm (10 mA/mm) and 35.55 dBm (100 mA/mm). Maximum PAE: 68.85 % (10 mA/mm) and 64.43 % (100 mA/mm). Red Contours: Measured data, blue contours: Model.

HEMT based state-of-the-art RF circuit design.

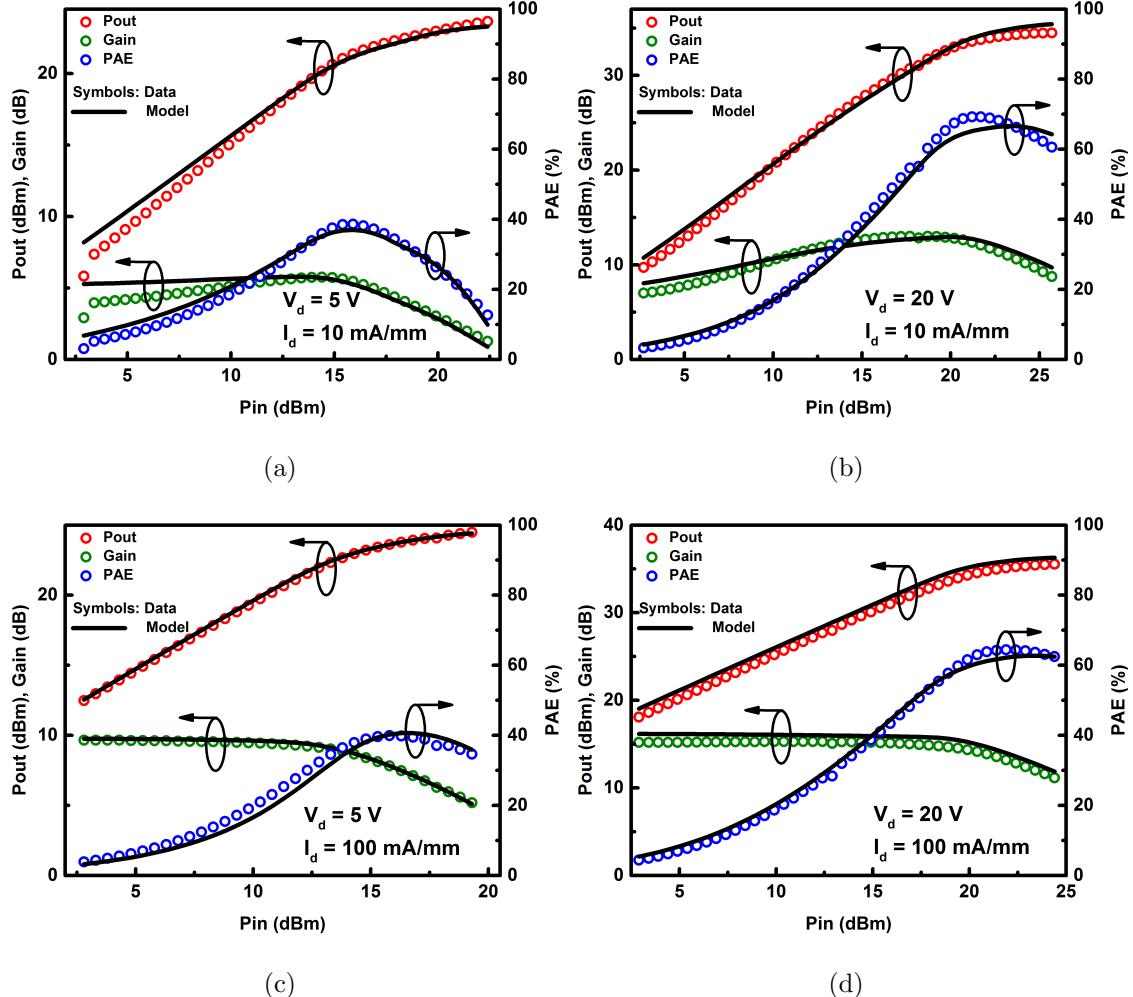


Figure 4.19: Comparison between modeled and measured P_{OUT} , Gain and PAE as functions of available input power (P_{IN}) for $V_d = 5$ and 20 V with two gate bias conditions $I_d = 10$ and 100 mA/mm. The frequency of the 22 dBm RF input signal is 10 GHz and the values of the load impedances are set for maximum PAE. The strength of the nonlinear model lies in accurately reproducing gain-compression for multiple bias conditions.

4.7 Statistical Simulation using Large Signal Model

4.7.1 Sensitivity Analysis

In order to harness these extremely promising properties of GaN HEMTs, RF circuit designers need a highly accurate, computationally efficient and robust device

model. Due to variations in the performance of the active device, there is need of a model that replicates with high fidelity the statistical nature of the design so that production-level yield-oriented optimized RF circuit design is achieved. In the past, statistical models have been proposed which are based on empirical or table based models and as a result do not offer any interesting take-aways since the model parameters rarely bear any physical significance [134–136]. Here, we perform a Monte-Carlo simulation using our physics-based model named the Advanced SPICE Model for GaN High Electron Mobility Transistors (ASM-HEMT).

In order to accomplish a reasonably meaningful statistical simulation, it is imperative to pinpoint the key parameters that are going to be varied to check for the statistical behaviour. We use our physics-based model to get a deeper insight by carrying out a sensitivity analysis using Keysight’s ADS simulator to check for the most sensitive model parameters affecting output power (P_{out}) and power added efficiency (PAE). The initial model parameter set is already extracted for a commercial GaN HEMT, with the model parameter description given in Table 4.5 [103]. Each of the parameters are individually varied within $\pm 1\%$ of the nominal value while keeping the values of the rest of the parameters fixed. Shown in Fig. 4.20 are the sensitivity bar-charts for P_{out} and PAE. As can be seen, parameters V_{off} , R_{TRAP2} , C_{GSO} , C_{GDO} , N_{factor} and η_0 seem to be influencing P_{out} and PAE whereas parameters corresponding to access region resistance, thermal resistance, and more importantly the device geometrical parameters (L , L_{SG} , L_{DG} and W) are relatively insignificant.

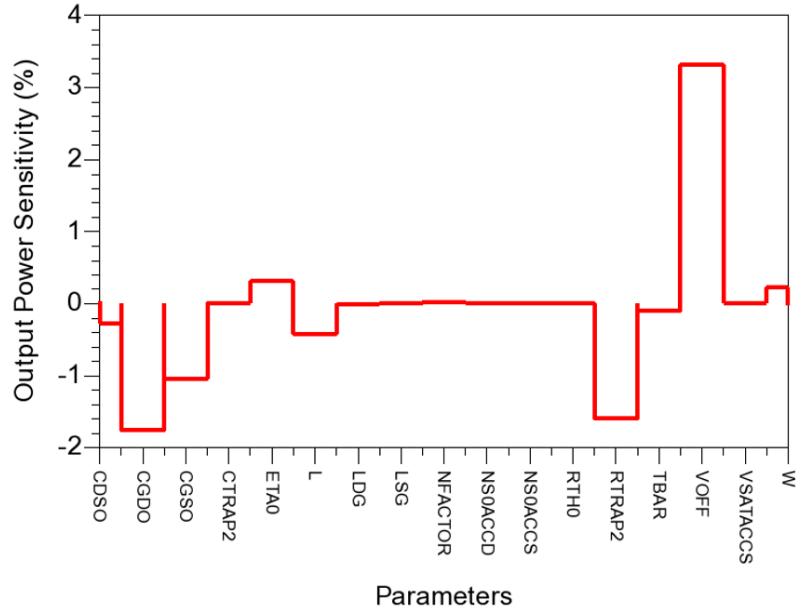
Both P_{out} and PAE depend strongly on fluctuations in V_{off} since it limits the current excursions in the I-V plane. Fluctuations in V_{off} among different devices obtained after same process control parameters may arise due to different polarization charges induced at the edges of the AlGaN barrier or even due to the variation in the thickness of the AlGaN barrier itself. The overlap capacitances, particularly C_{GDO} and C_{GSO} determine the small signal behaviour of the model at RF which also reflects in the large signal simulations as suggested by the sensitivity bar-charts. This is the only significant manifestation of having structural variability among dif-

Table 4.5: Model Parameter Description

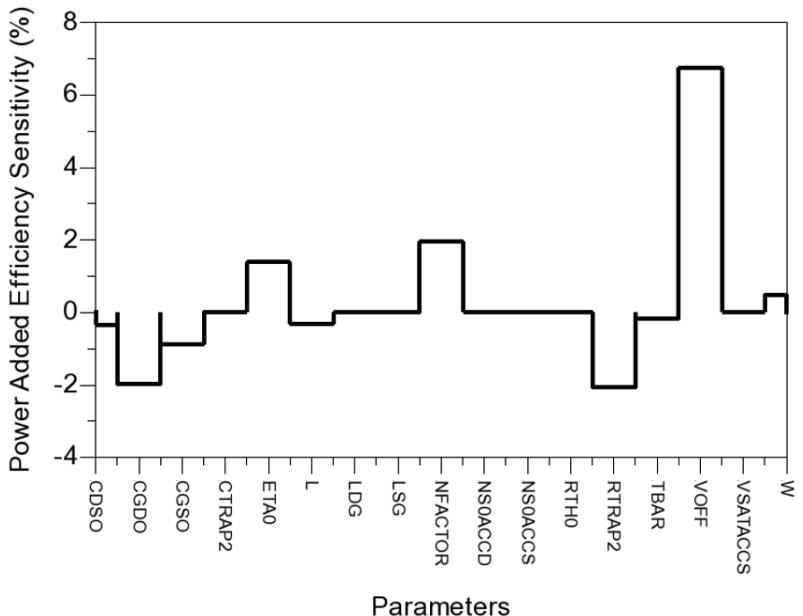
Model ment	Ele- ment	Description
W		Width
L		Length
$L_{SG,DG}$		Gate-Source, Gate-Drain Access Region Length
T_{BAR}		AlGaN Barrier Thickness
V_{off}		Cutoff Voltage
U_0		Low field Mobility
N_{factor}		Subthreshold Slope Factor
η_0		DIBL
$N_{s0,A}$		Access Region 2DEG Density
$V_{sat,A}$		Access Region Carrier Saturation Velocity
$R_{SC,DC}$		Source, Drain Contact Resistances
R_{TH}		Thermal Resistance
R_{TRAP2}		Trap Resistance
C_{TRAP2}		Trap Capacitance
C_{GSO}		Gate-Source Overlap Capacitance
C_{GDO}		Gate-Drain Overlap Capacitance
C_{DSO}		Drain-Source Overlap Capacitance

ferent devices. We note that PAE is sensitive as far as its relation with subthreshold parameters N_{factor} and η_0 is concerned, which may primarily be due to the variation in the dissipated DC power within the device.

Trapping severely affects the large signal performance at RF as indicated by Fig. 4.20. In our model, trapping is captured by an RC network to mimic drain lag as shown in Fig. 4.6. The input to the RC is a function of the drain voltage (V_d) and the trap voltage (V_{trap}) developed across the RC is fed back into the model to



(a)



(b)

Figure 4.20: Sensitivity bar-charts for (a) P_{OUT} and (b) PAE for individually varying parameters listed in Table 4.5 by 1% from the nominal value. The most sensitive parameters can be easily identified. An interesting observation to be made is the relatively less sensitivity of P_{OUT} and PAE towards fluctuations in geometrical parameters whereas V_{off} , R_{TRAP2} , C_{GSO} and C_{GDO} are highly significant.

Table 4.6: Parameters extracted for 10 GaN devices

Parameter	μ	$\sigma\%$
V_{off}	-2.86 V	1
N_{factor}	0.202	0.0
η_0	0.117	0.0
C_{GSO}	610 fF	2
C_{GDO}	225 fF	2
R_{TRAP2}	2.4 Ω	2

update various quantities such as V_{off} , subthreshold slope, access region resistance parameters etc as suggested by pulsed IV measured data available in literature [126, 127]. It must be noted that the GaN devices for which the model parameters are extracted and used for this work, are passivated and therefore has minimal gate-lag effects. The variability in trap behaviour of the devices may come about due to randomness in trap densities, different trap-detrap time constants, trap locations in the buffer or due to time-degradation etc.

4.7.2 Monte Carlo Simulation

After having identified the model parameters to which P_{OUT} and PAE were sensitive, we use measured P_{OUT} and PAE data for a batch of 10 GaN HEMTs on a single wafer and extract values for model parameters V_{off} , R_{TRAP2} , C_{GSO} , C_{GDO} , N_{factor} and η_0 . Their means (μ) and standard deviation percent ($\sigma\%$) are given in Table 4.6. It must be noted that the value of $\sigma\%$ for N_{factor} and η_0 are zero, since we kept their values fixed for all devices as they are core model parameters. Nevertheless, we proceed to Monte Carlo simulations in Keysight’s ADS Simulator for 250 trials which is sufficient for achieving a decent confidence level. The inputs to the Monte Carlo controller are the above given 4 parameters with standard deviation percent the same as presented in Table 4.6. The distribution followed by the input parameters around the nominal value is set to Gaussian, as shown in Fig. 4.21.

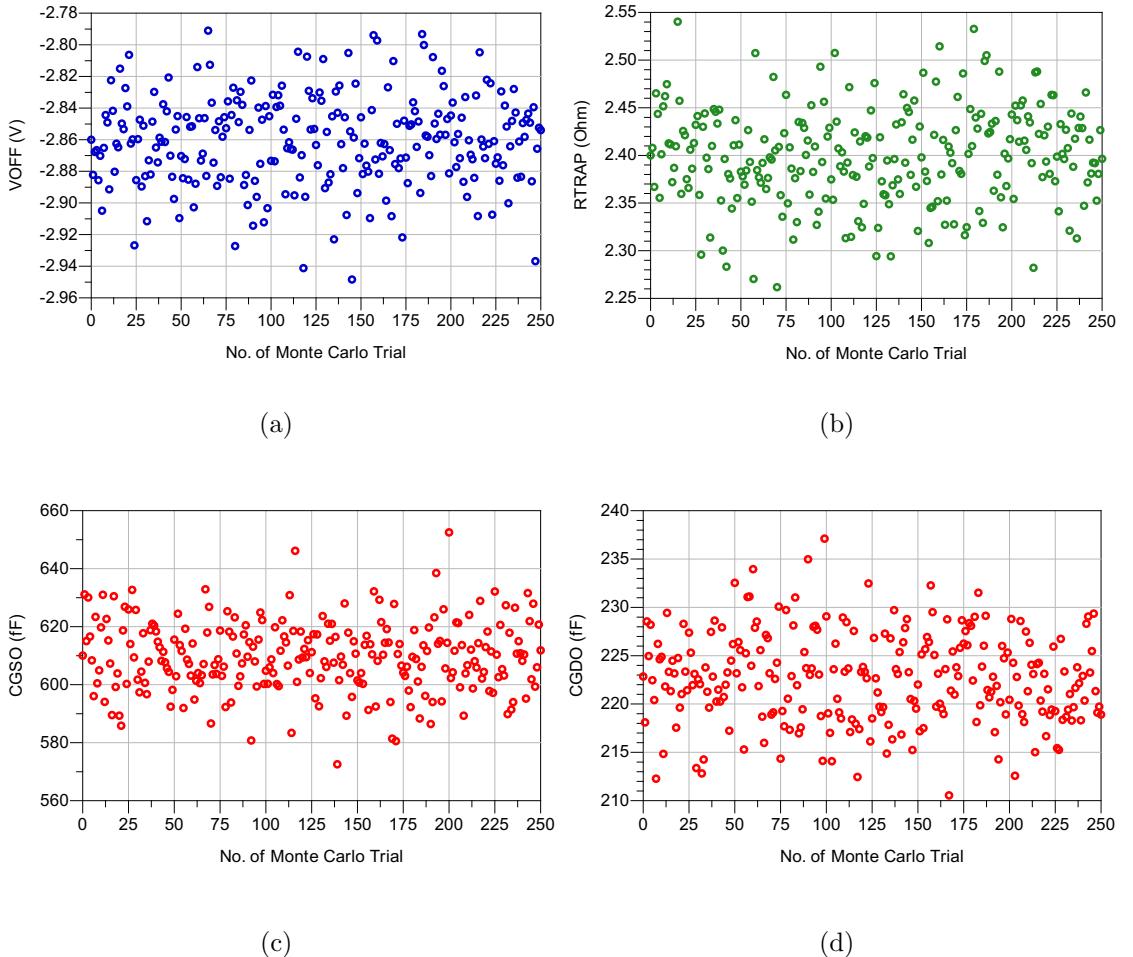


Figure 4.21: Values of parameters (a) V_{off} (b) R_{TRAP2} (c) C_{GSO} and (d) C_{GDO} for 250 Monte Carlo trials.

Comparison between modeled and measured statistical results for P_{OUT} & gain (Fig. 4.22) and PAE & I_{dd} (Fig. 4.23) is shown for 3 different bias conditions - $V_d = 5$ V and 10 V and $I_{ds} = 9$ mA and 90 mA. The input RF power at a frequency of 10 GHz is swept from 2.5 – 22.5 dBm and the load terminations are extracted from loadpull measurements for optimum P_{OUT} and PAE. The measured traces are seen to fall well within the bounds defined by the curves simulated using the model thereby depicting a high accuracy of the model. It is also seen that in certain cases, the modeled traces are more dispersed i.e having a greater standard deviation than the measured traces, which indicates a relatively modest sample size of measured data and therefore more constricted than the modeled traces. The accuracy of

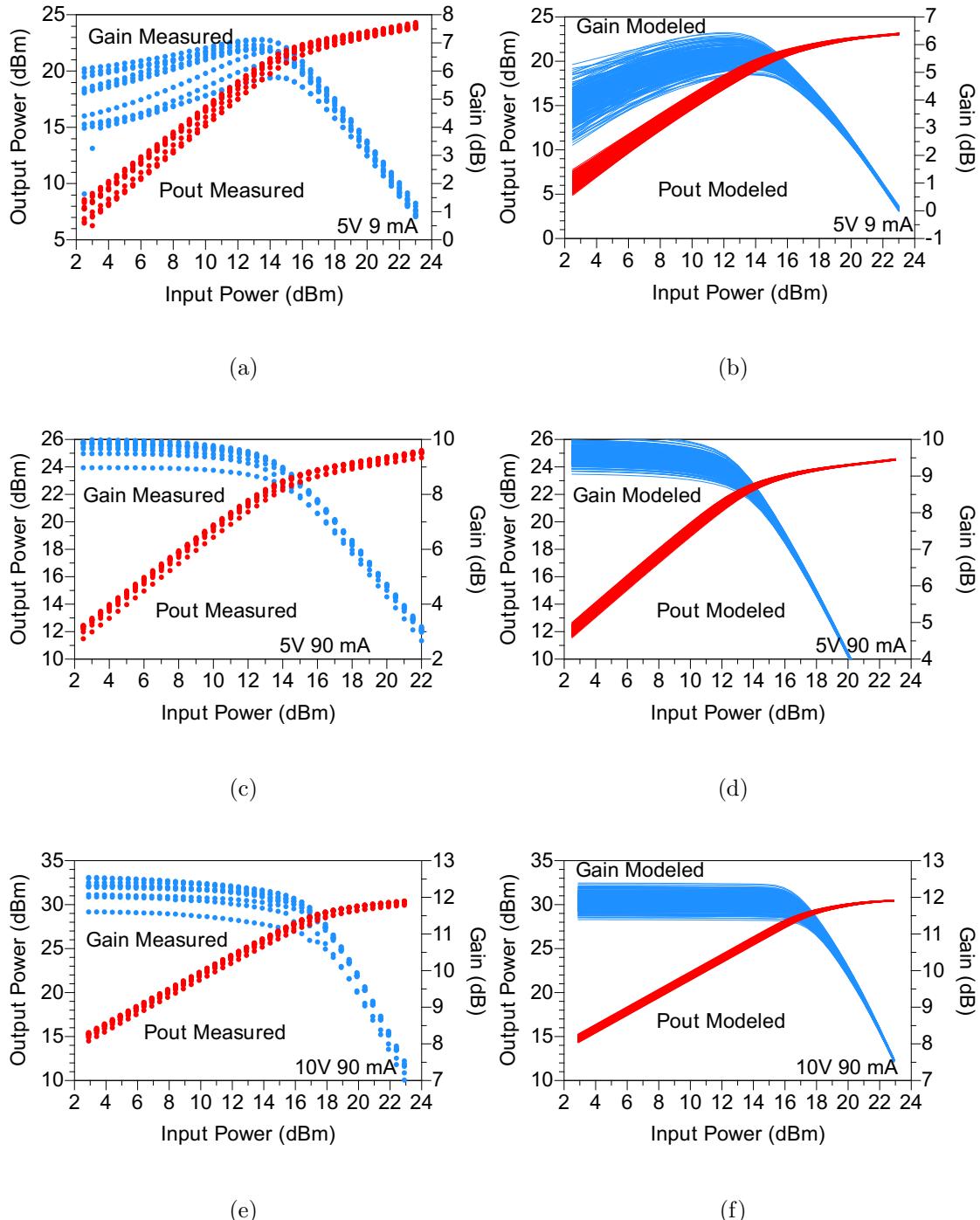


Figure 4.22: Comparison of measured statistical data (a, c, e) for P_{OUT} and Gain with modeled statistical results (b, d, f). The modeled curves are for 250 trials whereas measured data is for a batch of 10 GaN devices fabricated on a single wafer.

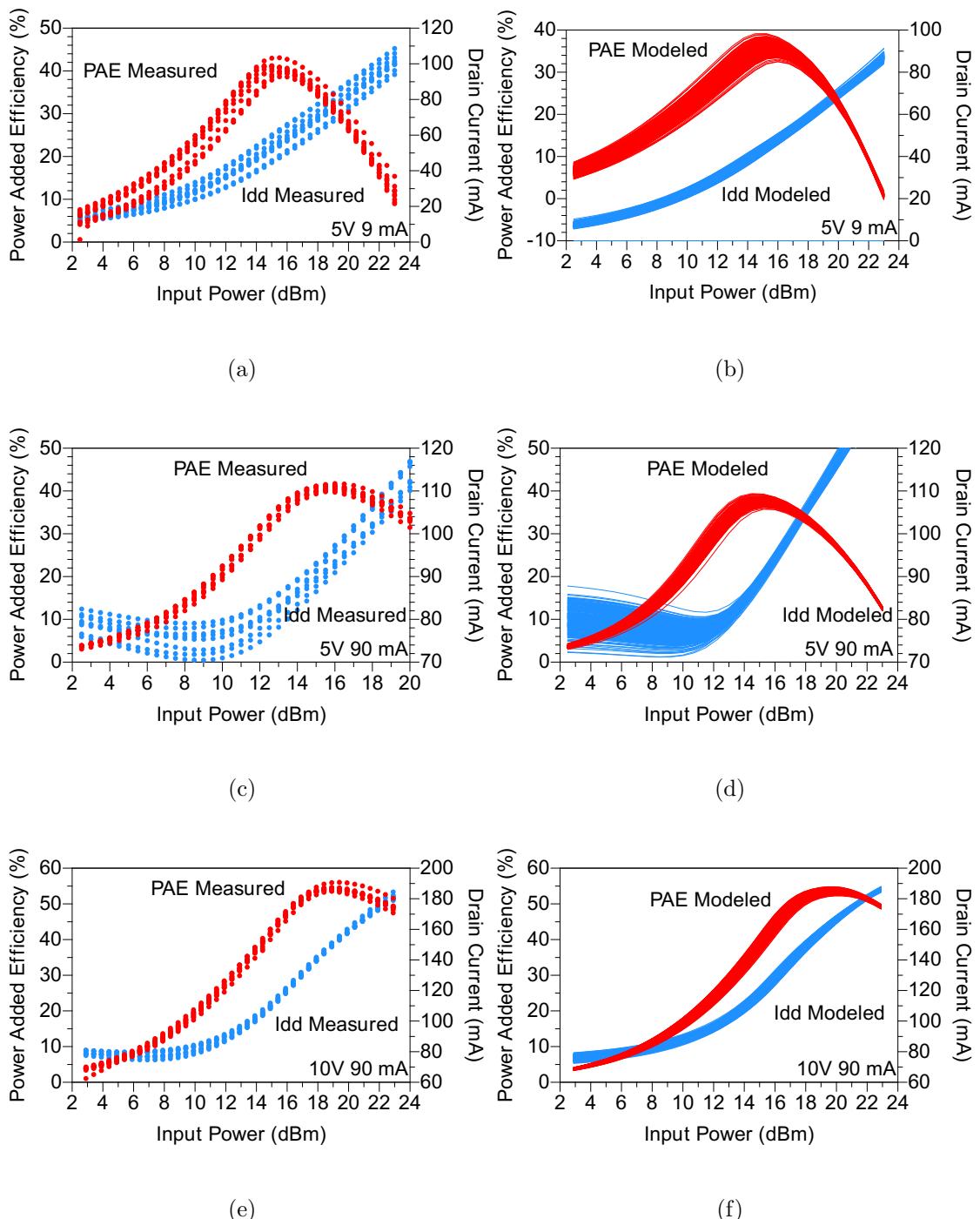


Figure 4.23: Comparison of measured statistical data (a, c, e) for PAE and I_{dd} with modeled statistical results (b, d, f). Validation is done for 3 different bias conditions with $V_d = 5$ V and 10 V and $I_{ds} = 9$ and 90 mA.

the statistical simulation obtained highlights the sensitivity analysis performed to narrow down and identify parameters that impact statistical performance under large signal RF conditions.

Summary

A surface-potential-based RF large-signal model for GaN HEMTs was demonstrated and successfully validated against measured data for a commercial GaN device. It was shown that fitting the model for DC-IV characteristics would automatically generate the small-signal equivalent circuit for RF simulation due to the self-consistency between the device intrinsic charges and current, except for the extraction of parasitic capacitance and gate resistance, which need to be extracted using standard procedures. Additionally, trapping effects were modeled using RC circuits and broadband S-parameters were used to validate the RF model. Furthermore, the model capability to predict load-pull contours and their corresponding maxima for varying load-impedances was shown, which could be handy for an accurate first-pass power amplifier design. Statistical simulation for large signal RF performance of GaN HEMTs using the presented model was done to analyse the impact of variability. A sensitivity analysis was performed to identify key model parameters that determine the statistical nature of harmonic balance power sweeps. It was seen that the effect of fluctuations in geometrical dimensions was minimal and could therefore be ignored. However, the impact of trapping, which is severe in GaN HEMTs as well as stochastic in nature, was identified and included in the Monte Carlo simulation. In addition, variations in overlap capacitances were also seen to be critical in determining the statistical results. Excellent results were obtained upon comparison with measured data for commercial GaN HEMTs.

Chapter 5

Study of Z-parameters for Large Gate-periphery GaN HEMTs

5.1 Introduction

Small-signal parameter extraction for microwave transistors forms a key ingredient of their overall modeling process since it is a prerequisite to the subsequent large-signal modeling [137]. Also, it is common knowledge that an accurate extraction procedure for a particular small-signal equivalent circuit is crucial as far as the design of a circuit, examination of the corresponding process technology and device performance optimization are concerned. The traditional approach to extract the small-signal model involves evaluating series extrinsics using linear regressions of real and imaginary parts of Z-parameters ($[Z]$) followed by the extraction of the intrinsic model elements using low-frequency Y-parameters, after de-embedding the calculated extrinsic parasitics [118, 119, 138]. This approach is widely used, however, it requires the device to be biased at certain conditions, for instance the forward cold-FET technique to extract the inductances [139].

In this chapter, we demonstrate an alternate procedure to analytically extract the GaN HEMT RF small-signal model using a single set of measured $[Z]$ data for a large gate periphery device, which exhibits the following interesting properties:

1. The imaginary parts of $[\mathbf{Z}]$ exhibit local minima that depend on the values of the extrinsic as well as the intrinsic device components.
2. The determinant of the extrinsic $[\mathbf{Z}]$ matrix becomes purely real or imaginary at certain frequencies.

For devices with larger gate-peripheries, these features appear within the frequency range of $[\mathbf{Z}]$ measured data due to their relatively larger capacitances as opposed to smaller periphery devices, in which these features appear at much higher frequencies. Since GaN devices are aimed at higher power operations, they are usually of larger peripheries and therefore exhibit such characteristics. Here, we use these features to our advantage in extracting the total extrinsic model for GaN HEMTs.

The rest of the chapter is organized as follows: The small-signal model extraction technique is discussed in Section 5.2, wherein mathematical expressions for Z-parameters for a GaN device are developed and used for parameter extraction. Stability analysis and modeling is carried out in Section 5.3.

5.2 Small-signal Model Extraction Technique

5.2.1 Extrinsic-level Small-signal Equivalent Circuit

Fig. 5.1 shows the small-signal equivalent circuit (SS–EC) depiction of the extrinsic level GaN device after de-embedding the pad parasitics. L_g , L_s and L_d represent the bias-independent bus inductances that feed the signal to the intrinsic device, whereas the capacitances (C_{gs} , C_{gd} and C_{ds}), transconductance (g_m) and output conductance (g_{ds}) constitute the intrinsic model core. We also incorporate the gate resistance (R_g) and the access region resistances ($R_{d/s}$) into our core current model. As a result, their impact is embedded in the modified intrinsic device components particularly $g_m(R_{d/s}, R_g)$ and $g_{ds}(R_{d/s}, R_g)$. This significantly simplifies our task by ignoring them in our derivation without compromising on the model accuracy.

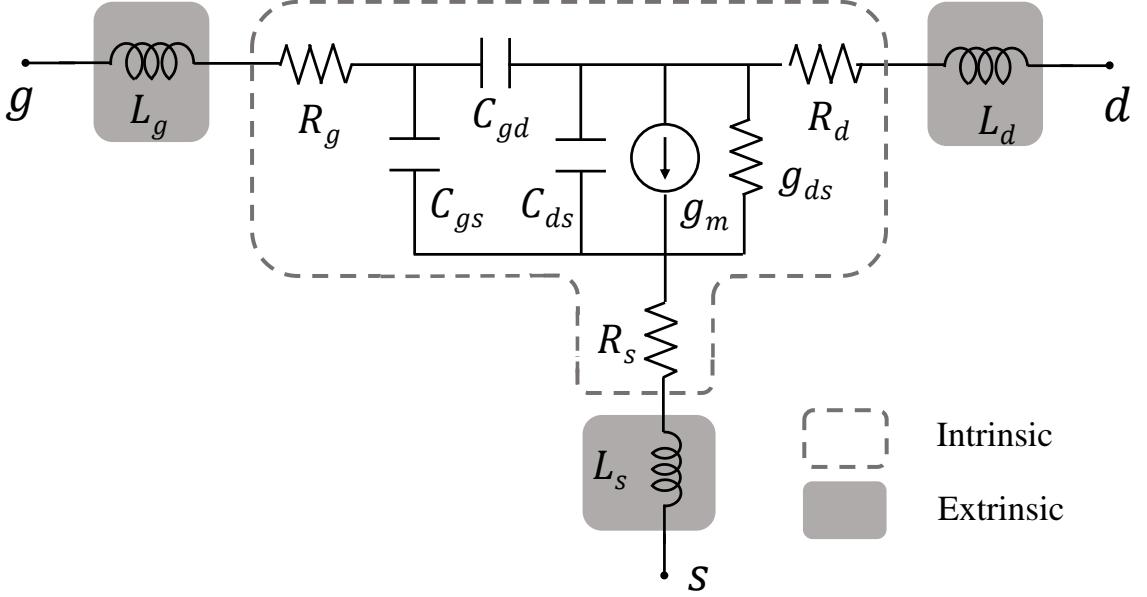


Figure 5.1: SS-EC depiction of the extrinsic-level pad-deembedded GaN device. R_g , R_d and R_s are shown in the schematic, however, their contribution is embedded in the core current model [125].

5.2.2 Extraction Procedure

The extraction procedure presented here is purely mathematical and employs the set of measured broadband S-parameter data for a commercial GaN device, which is subsequently converted into Z-parameters. The SS-EC discussed above is used to derive the expressions for the [Z] matrix elements, gathered below as

$$Z_{11}^e = \frac{\alpha C_{dd} - g_{ds} C_{eq}^2 + j[\omega(L_{gg}(\alpha^2 + \omega^2 C_{eq}^4) - C_{dd} C_{eq}^2) - \alpha g_{ds}/\omega]}{\alpha^2 + \omega^2 C_{eq}^4} \quad (5.1)$$

$$Z_{12}^e = \frac{\alpha C_{gd} + j\omega[L_s(\alpha^2 + \omega^2 C_{eq}^4) - C_{gd} C_{eq}^2]}{\alpha^2 + \omega^2 C_{eq}^4} \quad (5.2)$$

$$Z_{21}^e = \frac{\alpha C_{gd} + g_m C_{eq}^2 + j[\omega(L_s(\alpha^2 + \omega^2 C_{eq}^4) - C_{gd} C_{eq}^2) + \alpha g_m/\omega]}{\alpha^2 + \omega^2 C_{eq}^4} \quad (5.3)$$

$$Z_{22}^e = \frac{\alpha C_{gg} + j\omega[L_{dd}(\alpha^2 + \omega^2 C_{eq}^4) - C_{gg} C_{eq}^2]}{\alpha^2 + \omega^2 C_{eq}^4} \quad (5.4)$$

where $C_{gg(dd)} = C_{gs(ds)} + C_{gd}$, $L_{gg(dd)} = L_{g(d)} + L_s$, $C_{eq}^2 = C_{gg} C_{dd} - C_{gd}^2$ and $\alpha = g_{ds} C_{gg} + g_m C_{gd}$.

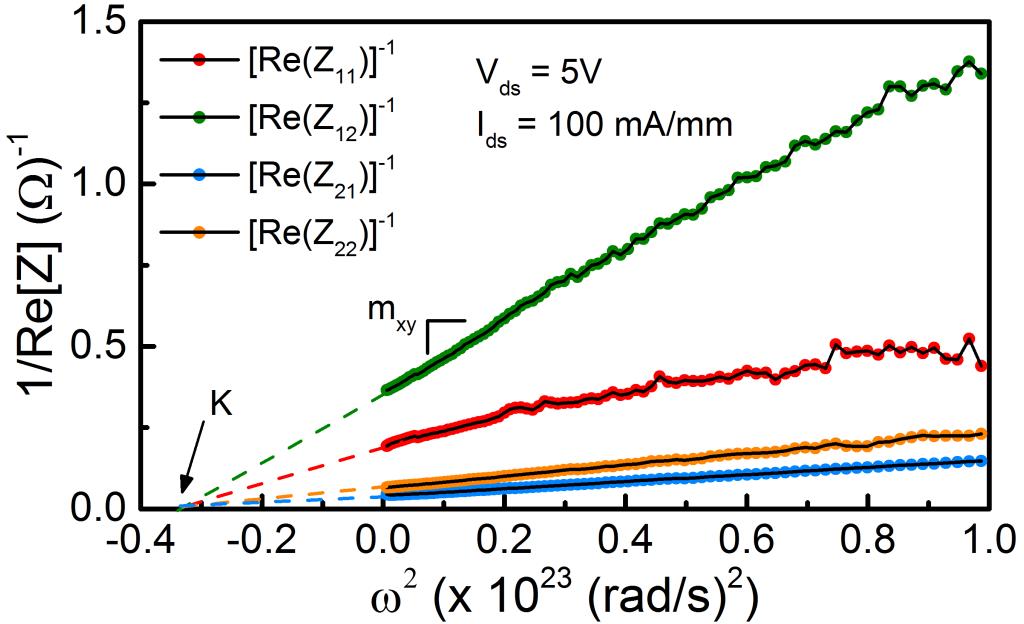


Figure 5.2: Measured data for Inverse of $\text{Re}(Z_{xy})$ plotted against ω^2 for a $10 \times 90 \mu\text{m}$ device, from which $m_{11} = 4.24$, $m_{12} = 10.05$, $m_{21} = 0.815$, $m_{22} = 1.818 (\times 10^{-24} \Omega^{-1}\text{s}^2/\text{rad}^2)$ and $K = 0.368 (\times 10^{23} \text{ rad}^2/\text{s}^2)$ can be extracted.

The inverse of $\text{Re}(Z_{xy})$ as a function of ω , can be obtained using mathematical rearrangement of the above expressions as

$$\frac{1}{\text{Re}(Z_{11}^e)} = \underbrace{C_{eq}^4 / (\alpha C_{dd} - g_{ds} C_{eq}^2)}_{m_{11}} \left(\omega^2 + \underbrace{\alpha^2 / C_{eq}^4}_{K} \right) \quad (5.5)$$

$$\frac{1}{\text{Re}(Z_{12}^e)} = \underbrace{\frac{C_{eq}^4}{\alpha C_{gd}}}_{m_{12}} \left(\omega^2 + \underbrace{\alpha^2 / C_{eq}^4}_{K} \right) \quad (5.6)$$

$$\frac{1}{\text{Re}(Z_{21}^e)} = \underbrace{C_{eq}^4 / (\alpha C_{gd} + g_m C_{eq}^2)}_{m_{21}} \left(\omega^2 + \underbrace{\alpha^2 / C_{eq}^4}_{K} \right) \quad (5.7)$$

$$\frac{1}{\text{Re}(Z_{22}^e)} = \underbrace{\frac{C_{eq}^4}{\alpha C_{gg}}}_{m_{22}} \left(\omega^2 + \underbrace{\alpha^2 / C_{eq}^4}_{K} \right) \quad (5.8)$$

where xy , is 11 through 22. As can be observed, the expressions in (5.5) are linear functions of ω^2 , with slopes m_{xy} and a common intercept α^2 / C_{eq}^4 , denoted by K . Corresponding measured values of inverse of $\text{Re}(Z_{xy})$ are shown in Fig. 5.2 from

which m_{xy} and K can be extracted.

We now have five conditions with their respective measured quantities (m_{11} , m_{12} , m_{21} , m_{22} and K) and five unknowns (C_{gs} , C_{gd} , C_{ds} , g_m and g_{ds}). Plugging in $K = \alpha^2/C_{eq}^4$ into the expressions for m_{xy} gives us

$$m_{11}(C_{dd} - g_{ds}/\sqrt{K}) = m_{12}C_{gd} = m_{21}(C_{gd} + g_m/\sqrt{K}) = m_{22}C_{gg} = \alpha/K \quad (5.9)$$

Also, $K = \alpha^2/C_{eq}^4$ gives

$$\sqrt{K} = \alpha/C_{eq}^2 = (g_{ds}C_{gg} + g_mC_{gd})/(C_{gg}C_{dd} - C_{gd}^2) \quad (5.10)$$

$$\Rightarrow C_{gg}/C_{gd} = (C_{gd} + g_m/\sqrt{K})/(C_{dd} - g_{ds}/\sqrt{K}) \quad (5.11)$$

Eq. (5.9) in conjunction with (5.10) indicates the insufficiency of distinct conditions required to obtain an explicit expression for each of the five intrinsic elements. Consequently, after solving (5.9) and (5.10) we get the following expressions, however, in terms of the auxiliary variable α defined earlier.

$$C_{gd} = [1/m_{12}](\alpha/K) \quad (5.12)$$

$$C_{gs} = [(m_{12} - m_{22})/(m_{12}m_{22})](\alpha/K) \quad (5.13)$$

$$C_{ds} = m_{22}\sqrt{K} + [(m_{22} - m_{12})/(m_{12}^2)](\alpha/K) \quad (5.14)$$

$$g_m = [(m_{12} - m_{21})/(m_{12}m_{21})](\alpha/\sqrt{K}) \quad (5.15)$$

$$g_{ds} = m_{22}K + [(m_{22}/m_{12}^2) - (1/m_{11})](\alpha/\sqrt{K}) \quad (5.16)$$

In order to circumvent this ill-conditioned problem, and since L_g , L_s and L_d are also unknown, we need to introduce additional conditions which are as follows. Given below in (5.17–5.18) are expressions for the imaginary parts of Z_{22} and $Z_{22} - Z_{12}$ respectively and their corresponding measured values are shown in Fig. 5.3.

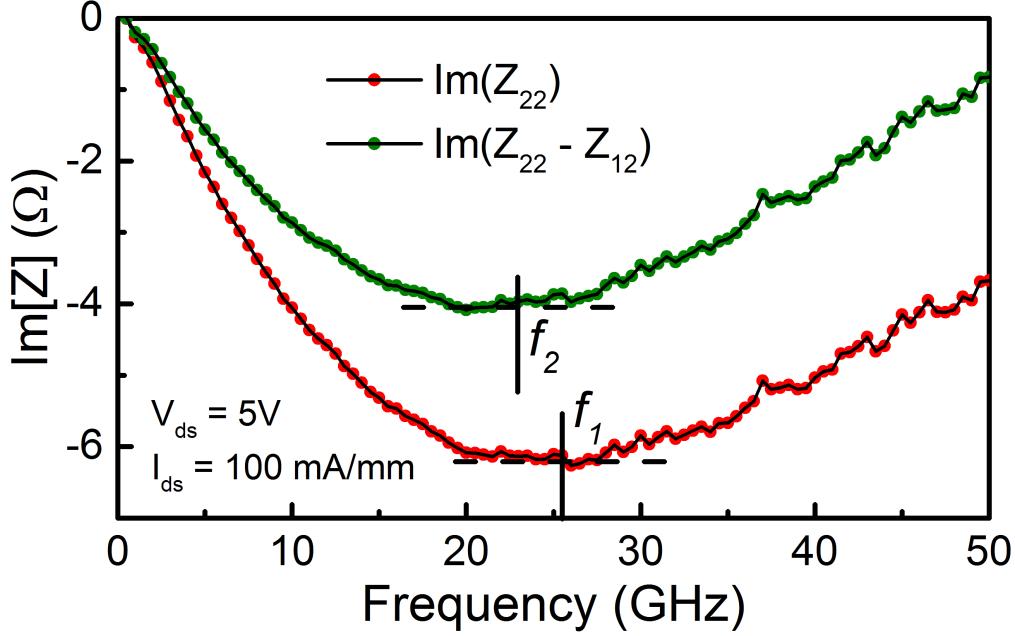


Figure 5.3: Measured data for $\text{Im}(Z_{22})$ and $\text{Im}(Z_{22} - Z_{12})$ for a $10 \times 90 \mu\text{m}$ device, which exhibits local minima at frequencies $f_1 = 25.2 \text{ GHz}$ and $f_2 = 24 \text{ GHz}$ respectively.

$$\text{Im}(Z_{22}) = \omega L_{dd} - (\omega C_{gg} C_{eq}^2) / (\alpha^2 + \omega^2 C_{eq}^4) \quad (5.17)$$

$$\text{Im}(Z_{22} - Z_{12}) = \omega L_d - (\omega C_{gs} C_{eq}^2) / (\alpha^2 + \omega^2 C_{eq}^4) \quad (5.18)$$

Eq. (5.17) and (5.18) can be used by taking their frequency-derivatives and equating them to zero at the local minima of $\text{Im}(Z_{22})$ and $\text{Im}(Z_{22} - Z_{12})$ as shown in Fig. 5.3, to get

$$L_{dd} = C_{gg} C_{eq}^2 \left(\frac{\alpha^2 - 4\pi^2 f_1^2 C_{eq}^4}{(\alpha^2 + 4\pi^2 f_1^2 C_{eq}^4)^2} \right) \quad (5.19)$$

$$L_d = C_{gs} C_{eq}^2 \left(\frac{\alpha^2 - 4\pi^2 f_2^2 C_{eq}^4}{(\alpha^2 + 4\pi^2 f_2^2 C_{eq}^4)^2} \right) \quad (5.20)$$

Plugging in the values from (5.12 – 5.16), we get the expressions for L_{dd} , L_d and L_s in terms of the extracted m_{xy} and K values and the local minima frequencies

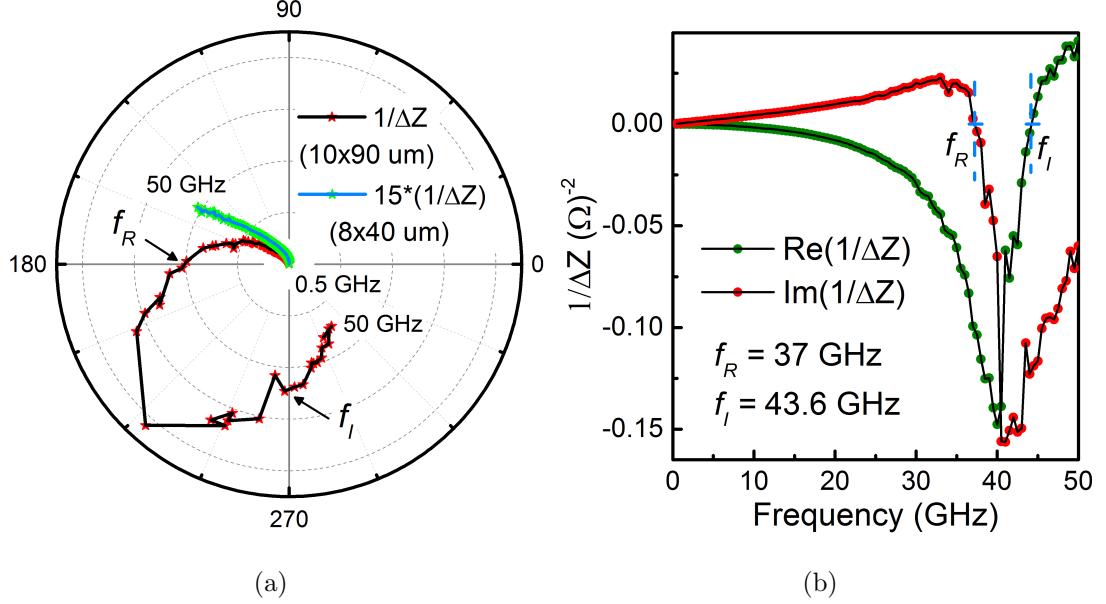


Figure 5.4: Measured data for $1/\Delta Z$ in (a) Polar and (b) Rectangular co-ordinates. The plots indicate that ΔZ becomes purely real at $f_R = 37$ GHz and imaginary at 43.6 GHz, which can be used to arrive at conditions given in (22–23). $1/\Delta Z$ for a smaller device ($8 \times 40 \mu\text{m}$) is also shown in (a), for which f_R and f_I are absent within the measured frequency range, indicating the unsuitability of the extraction method for the $8 \times 40 \mu\text{m}$ device.

f_1 and f_2 , as

$$L_{dd} = \frac{1}{m_{22}\sqrt{K}} \frac{K - \omega_1^2}{(K + \omega_1^2)^2} \quad (5.21)$$

$$L_d = \frac{1}{\sqrt{K}} \left(\frac{1}{m_{22}} - \frac{1}{m_{22}} \right) \frac{K - \omega_2^2}{(K + \omega_2^2)^2} \quad (5.22)$$

$$L_s = L_{dd} - L_d \quad (5.23)$$

We further derive, as given in (5.24) below, the expression for the determinant (ΔZ) of the $[Z]$ matrix, whose corresponding measured $1/\Delta Z$ data is shown in Fig. 5.4, which indicates that ΔZ becomes purely real and imaginary at frequencies f_R and f_I respectively. Also shown in Fig. 5.4(b) are corresponding $1/\Delta Z$ measurements for a small GaN device with a gate periphery of $8 \times 40 \mu\text{m}$, for which f_R and f_I are absent within the measured frequency range, indicating the unsuitability of

the extraction method for the $8 \times 40 \mu\text{m}$ device.

$$\begin{aligned}\Delta Z^e &= \frac{[1 + \omega^2\beta + j\omega\gamma - \omega^2L_{eq}^2(j\omega\alpha - \omega^2C_{eq}^2)]}{j\omega\alpha - \omega^2C_{eq}^2} \\ \beta &= 2L_sC_{gd} - L_{gg}C_{gg} - L_{dd}C_{dd} \\ \gamma &= g_{ds}L_{dd} + g_mL_s\end{aligned}\quad (5.24)$$

So, two additional conditions can be introduced by equating the imaginary and real parts of ΔZ^e to zero at frequencies f_R and f_I to give (5.25) and (5.26) as under

$$\alpha + ((2L_sC_{gd} - L_{gg}C_{gg} - L_{dd}C_{dd})\alpha + (g_mL_s + g_{ds}L_{dd})C_{eq}^2)\omega_R^2 = 0 \quad (5.25)$$

$$L_{eq}^2 = L_{gg}L_{dd} - L_s^2 = \frac{\alpha\gamma - C_{eq}^2(1 + \omega_I^2\beta)}{\omega_I^2(\alpha^2 + \omega_I^2C_{eq}^4)} \quad (5.26)$$

Eq. (5.25) can be solved for L_{gg} in terms of α by substituting expressions from (5.12 – 5.16) as

$$L_{gg} = \frac{m_{22}K}{\alpha\omega_R^2} + m_{22}L_s \left(\frac{1}{m_{12}} + \frac{1}{m_{21}} \right) - \frac{m_{22}}{m_{11}}L_{dd} \quad (5.27)$$

Together (5.26) and (5.27) can be solved to get the expression for α in terms of all the known values, given in (5.28) below as,

$$\alpha = \frac{(1/\omega_R^2 - 1/\omega_I^2) \left(m_{22}L_{dd}K - \sqrt{K}/(K + \omega_I^2) \right)}{L_s^2 + (m_{22}/m_{11})L_{dd}^2 - m_{22}(1/m_{21} + 1/m_{12})L_{dd}L_s + \chi/\omega_I^2\sqrt{K}} \quad (5.28)$$

$$\chi = (m_{22}/m_{12}^2 - 1/m_{11})L_{dd} + (1/m_{21} - 1/m_{12})L_s \quad (5.29)$$

The above expression can finally be used to evaluate all other quantities, thereby completing the extraction procedure. The small-signal model parameters extracted and optimized for best fits for three bias points A ($V_d = 5\text{V}$, $I_d = 10 \text{ mA/mm}$), B ($V_d = 5\text{V}$, $I_d = 100 \text{ mA/mm}$) and C ($V_d = 10\text{V}$, $I_d = 10 \text{ mA/mm}$) are

tabulated in Table 5.1. The negative source inductance can be ascribed to an improper calibration or de-embedding of the pad parasitics. Lastly, Fig. 5.5 shows the comparison of measured and modeled S-parameters using parameter values given in Table 5.1, thereby validating the extraction procedure.

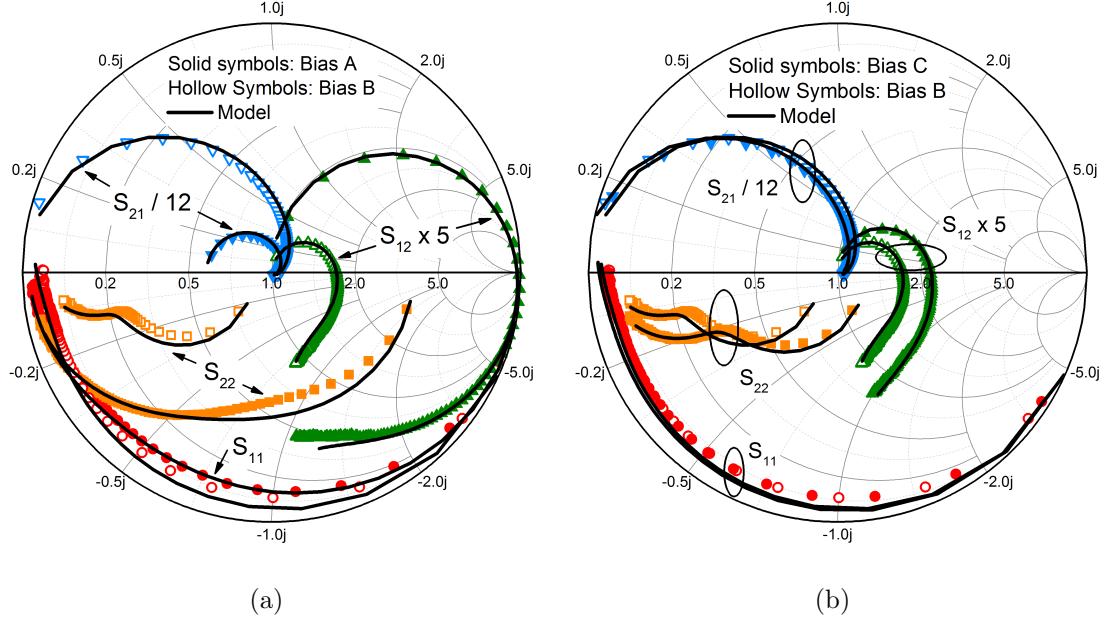


Figure 5.5: Multiple bias validation of the extracted model using broadband S-parameters (0.5 - 50 GHz). (a) Comparison between bias A and B for V_g dependence (b) Comparison between bias B and C for V_d dependence. The model simulations have been carried out using parameter values tabulated in Table 5.1. Excellent correlation is observed between model and measured data, validating the extraction procedure.

Table 5.1: Extracted Parameters

Bias	$g_m(S)$	$C_{gs}(\text{pF})$	$C_{gd}(\text{pF})$	$C_{ds}(\text{pF})$	$g_{ds}(S)$	$L_g(\text{pH})$	$L_s(\text{pH})$	$L_d(\text{pH})$
A	0.04	0.36	0.115	0.255	0.005	19.3	-5.2	12.1
B	0.25	0.55	0.125	0.22	0.023	19.3	-5.2	12.1
C	0.22	0.66	0.1	0.19	0.016	19.3	-5.2	12.1

5.3 Stability Analysis

A standard RF power amplifier design flow consists of various steps such as biasing, stability analysis, load-pull, impedance-matching and yield-optimization, among others [42]. It is customary to check for potential regions of instability, which might throw the circuit into unwanted oscillations [140–142]. Stability is also a serious concern from a device characterization point of view, since a potentially unstable device can be used only under a particular set of passive terminations. An examination of the device for instability, using the Rollett's stability factor (K) [143], significantly reduces the complexity of the subsequent circuit design to ensure stable operation.

Previous stability studies were dedicated to RF CMOS transistors and their K-factor analysis was restricted to the intrinsic device level only [144, 145]. Here, we explore the impact of extrinsic inductances, primarily the source via inductance (L_{via}) that is known to degrade the high frequency gain [146], on the stability performance of RF transistors. Often, the gate-to-drain capacitance (C_{gd}) is considered to be the key source of device instability which understandably happens due to the formation of the feedback loop [147]. Here, we mathematically show that not only C_{gd} but also the drain-to-source capacitance (C_{ds}), and its subsequent interaction with L_{via} , is critical in determining the device stability, as explained in the next section. The impact of C_{ds} is more noticeable in devices with larger gate-peripheries due to their relatively larger values, making the interaction between the L_{via} and C_{ds} more significant.

A well-known method to circumvent the device instability problem is to have increased values of gate-resistance (R_g) [144]. However, R_g for multi-finger devices is much lower than their single-finger counterparts [148]. Therefore, it becomes imperative to study the stability of large gate-periphery RF transistors in context of a multi-finger layout.

In this section, the impact of source via-inductances on stability performance of microwave transistors, particularly GaN HEMTs, is studied using a small-signal equivalent circuit model. While Rollett's stability factor (K-factor) measurements for a commercial GaN device suggest a reduction in the unity-stability-factor fre-

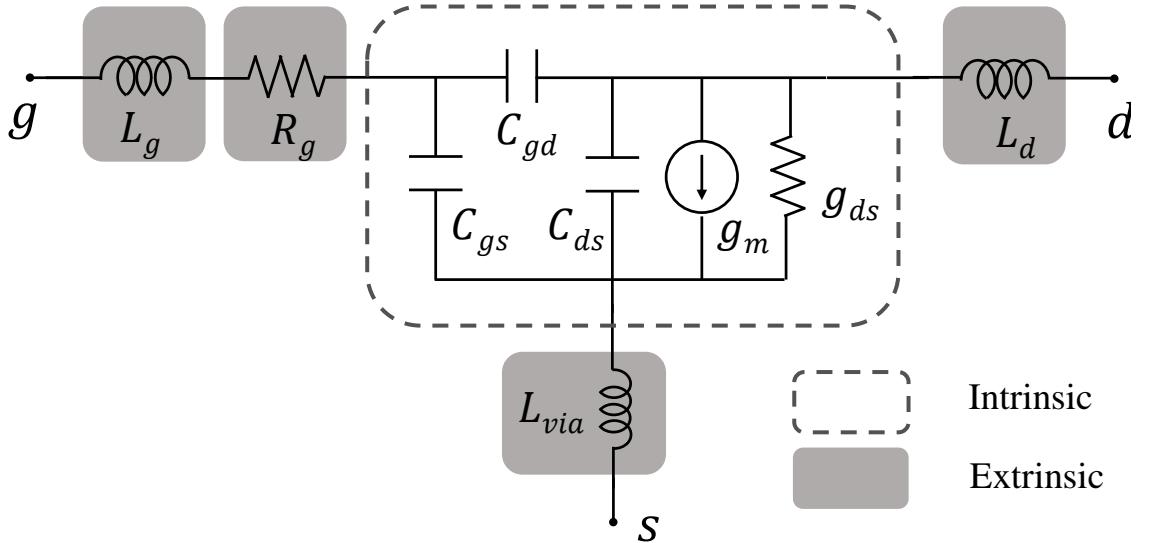


Figure 5.6: Small Signal Equivalent Circuit (SS-EC) Model of the device. The dashed region represents the intrinsic device as described by our surface-potential-based model. The capacitances (C_{gs} , C_{gd} and C_{ds}), output conductance (g_{ds}) and the transconductance (g_m) are calculated self-consistently from $\psi(V_g, V_d)$. g_m and g_{ds} , in addition to being functions of bias-dependent ψ , are functions of the access region resistances [125]. Bus inductances L_g and L_d and via-inductance L_{via} are also included.

quency for an increased via-inductance, anomalous features that are a manifestation of interaction between the via-inductance and the intrinsic device components, are observed in the form of peaks and valleys, indicating potential regions of device instability.

The study of stability factor in this chapter has been done using a SS-EC like the one shown in Fig. 5.1, however in a simplified form as shown in Fig. 5.6, where the drain and source access region resistances are ignored to make the analysis simpler. However, as mentioned earlier, their effect is already embedded into the drain current source. We use mathematical expression to express K-factor in terms of the device intrinsic and extrinsic components and use it to study the stability behavior as a function of the via-inductance, while also considering the impact of the gate resistance and the drain to source capacitance. Furthermore, the physics-based RF model presented in Chapter 4 is comprehensively validated in terms of its

ability to model K-factor for broadband multi-bias conditions.

5.3.1 Small Signal Model And Stability Factor

Shown in Fig. 5.6 is the simplified Small Signal Equivalent Circuit (SS–EC) representation of the GaN device. While R_d and R_s are omitted in the SS–EC, it must be noted that R_g is included in the analysis. L_{via} denotes the lumped inductance due to the via-holes which connect the source-pads to back-plane metallization.

Gathered below in (5.30–5.33) are the expanded expressions for extrinsic Z-parameters for the SS–EC.

$$Z_{11}^e = \frac{\alpha C_{dd} - g_{ds}C_{eq}^2 + R_g(\alpha^2 + \omega^2 C_{eq}^4) + j[\omega(L_{gg}(\alpha^2 + \omega^2 C_{eq}^4) - C_{dd}C_{eq}^2) - \alpha g_{ds}/\omega]}{\alpha^2 + \omega^2 C_{eq}^4} \quad (5.30)$$

$$Z_{12}^e = \frac{\alpha C_{gd} + j\omega[L_{via}(\alpha^2 + \omega^2 C_{eq}^4) - C_{gd}C_{eq}^2]}{\alpha^2 + \omega^2 C_{eq}^4} \quad (5.31)$$

$$Z_{21}^e = \frac{\alpha C_{gd} + g_m C_{eq}^2 + j[\omega(L_{via}(\alpha^2 + \omega^2 C_{eq}^4) - C_{gd}C_{eq}^2) + \alpha g_m/\omega]}{\alpha^2 + \omega^2 C_{eq}^4} \quad (5.32)$$

$$Z_{22}^e = \frac{\alpha C_{gg} + j\omega[L_{dd}(\alpha^2 + \omega^2 C_{eq}^4) - C_{gg}C_{eq}^2]}{\alpha^2 + \omega^2 C_{eq}^4} \quad (5.33)$$

The well-known Rollett's stability factor (K) used as a stability criterion ($K \geq 1$ and $\Delta \leq 1$) and given as [143]

$$K = \frac{2Re[Z_{11}]Re[Z_{22}] - Re[Z_{12} \times Z_{21}]}{|Z_{12} \times Z_{21}|} \quad (5.34)$$

can be evaluated in terms of the SS–EC elements by plugging in the values from (5.30–5.33) to get

$$K_e = \frac{\gamma + (C_{gg}g_{ds} + C_{gd}g_m)(g_m L_{via} + 2R_g C_{gg})}{\sqrt{\gamma(\gamma + 2(C_{gg}g_{ds} + C_{gd}g_m)g_m L_{via} + g_m^2/\omega^2)}} \quad (5.35)$$

where $C_{gg(dd)} = C_{gs(ds)} + C_{gd}$, $C_{eq}^2 = C_{gs}C_{gd} + C_{gs}C_{ds} + C_{gd}C_{ds}$, $\alpha = C_{gg}g_{ds} + C_{gd}g_m$, and $\gamma = C_{gd}^2 + \omega^2 L_{via}^2(\alpha^2 + \omega^2 C_{eq}^4) - 2\omega^2 L_{via}C_{gd}C_{eq}^2$.

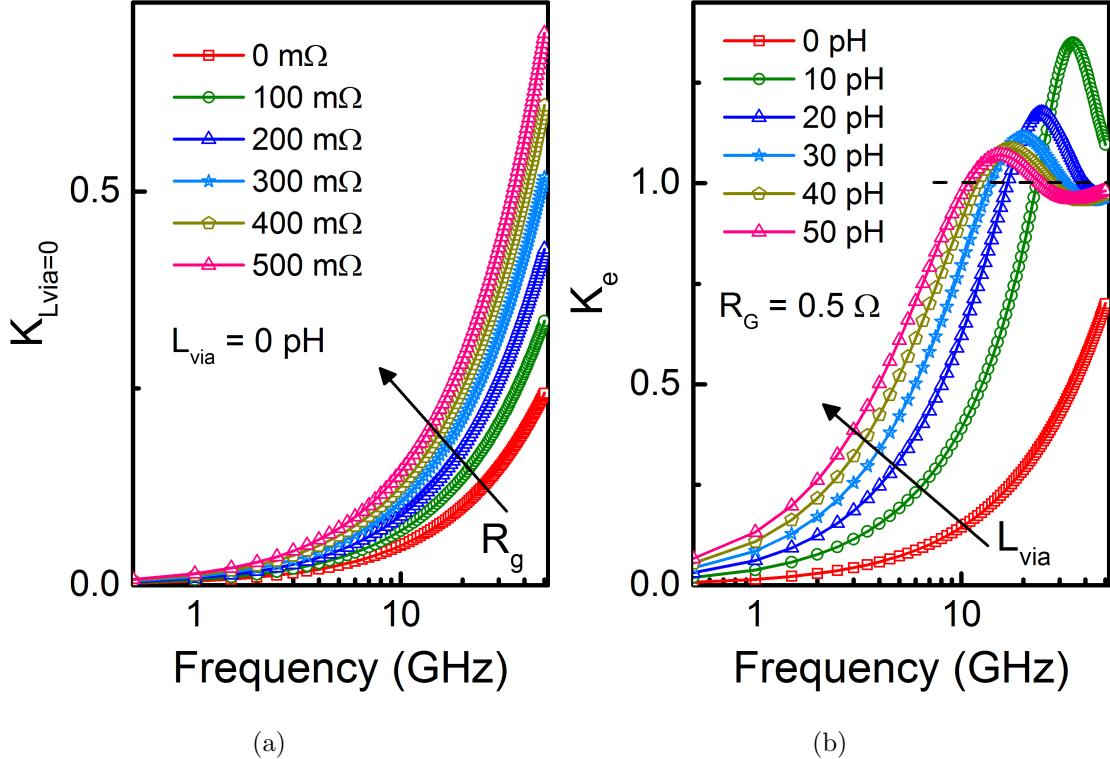


Figure 5.7: Plots of (a) (5.36) and (b) (5.35) obtained as R_g and L_{via} are increased respectively. Increasing R_g increases $K_{L_{via}=0}$ whereas increasing L_{via} causes the emergence of a peak-valley pair after f_K , which could potentially make the device unstable within the valley region. The values of the intrinsic SS–EC components used for both the plots are $C_{gs} = 0.8$ pF, $C_{gd} = 0.2$ pF, $C_{ds} = 0.25$ pF, $g_m = 250$ mS and $g_{ds} = 25$ mS.

It is interesting to note that K_e expressed in (5.35), is only a function of L_{via} and the intrinsic SS-EC elements while it is independent of L_g and L_d . If L_{via} is made zero, (5.35) reduces to a much simpler expression, given in (5.36) as

$$K_{L_{via}=0} = \frac{\omega [C_{gd} + 2R_g C_{gg} (C_{gg}g_{ds} + C_{gd}g_m) / C_{gd}]}{\sqrt{g_m^2 + \omega^2 C_{gd}^2}} \quad (5.36)$$

which upon making $R_g = 0$ further reduces to

$$K_{L_{via}=0, R_g=0} = \frac{\omega C_{gd}}{\sqrt{g_m^2 + \omega^2 C_{gd}^2}} \quad (5.37)$$

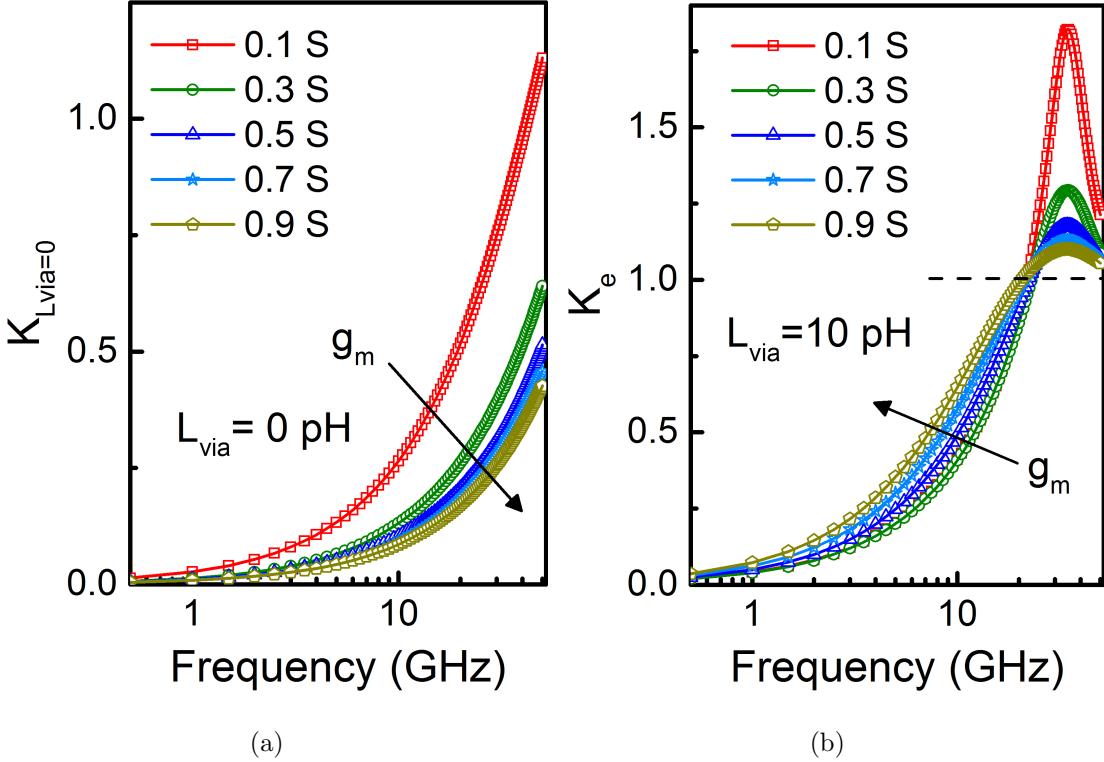


Figure 5.8: Plots of (a) (5.36) and (b) (5.35) obtained as g_m is increased. $K_{L_{via}=0}$ decreases as g_m is increased whereas when $L_{via} \neq 0$ only the extent of the peak beyond f_K is diminished, while no overall degradation of K is observed. The values of the other intrinsic SS–EC components used for both the plots are same as in Fig. 5.7.

An observation from (5.36) can be made that a unilateral device with $C_{gd} = 0$ would be unconditionally stable since it would have no feedback path to be a potential source of instability. It can also be inferred from (5.36) and (5.37) that increasing R_g has a positive impact on the device stability behavior, which is reflected in Fig. 5.7(a). However, it is slightly difficult to understand through a mere inspection of (5.35) the impact of L_{via} on K_e . Nevertheless, through a plot of (5.35) using previously extracted parameters for a commercial GaN device [149], as shown in Fig. 5.7(b), we notice that increasing L_{via} reduces the unity-stability-factor frequency (f_K), thereby improving device stability bandwidth. Additionally, the plots in Fig. 5.7(b) also reveal the emergence of a pair of peak and an ensuing valley, which results due to the interaction of L_{via} with device intrinsic components. It

is this valley which pushes K_e below 1, even after having crossed 1 for a much lower frequency, hence making device potentially unstable for a significant range of frequency.

Shown in Fig. 5.8(a) and 5.8(b) are plots of (5.36) and (5.35) respectively, where g_m is varied. It is seen that in the absence of L_{via} , increasing g_m decreases K , whereas in its presence, only the extent of the peak beyond f_K is diminished, while no overall degradation of K is observed.

The presence of L_{via} also has an indirect impact on K_e , by changing the nature of dependence of K on C_{ds} . We notice from (5.36) that $K_{L_{via}=0}$ is independent of C_{ds} , whereas increasing C_{ds} in presence of L_{via} severely degrades K_e by deepening the valley, even though f_K is progressively reduced, as shown in Fig. 5.9.

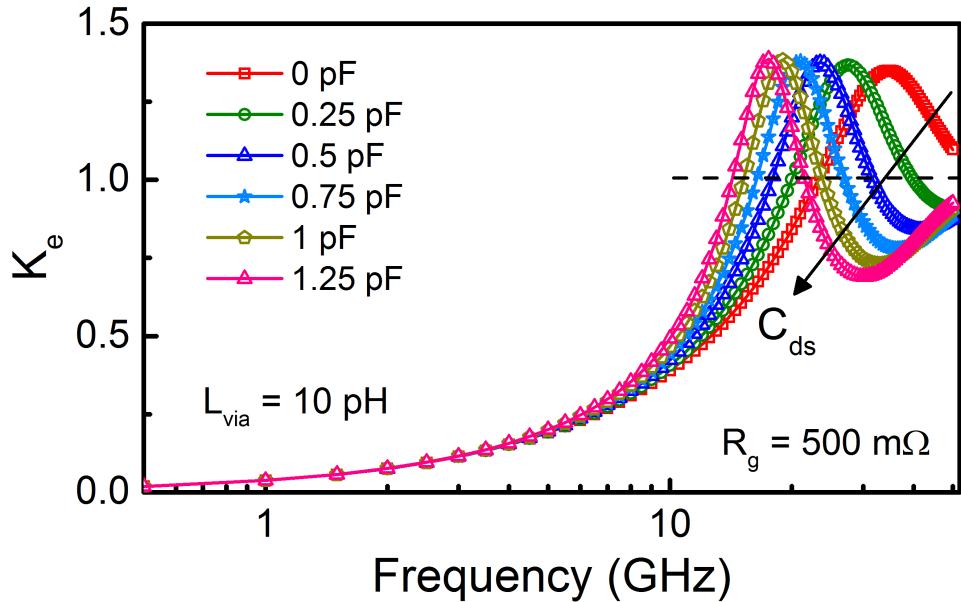


Figure 5.9: Plots of (5.35) obtained as C_{ds} is increased. f_K is reduced, however, it is accompanied by deepening of the valley. Therefore, C_{ds} should be minimized to improve the device stability performance. The values of the other intrinsic SS–EC components used for both the plots are same as in Fig. 5.7.

In order to circumvent the problem posed by the emergence of the valley, while minimizing f_K by increasing L_{via} , a qualitative solution that is suggested by (5.35) would be to maintain a proportionate relationship between L_{via} and R_g such that the term $2\alpha C_{gg} R_g$ also increases as L_{via} is scaled up, thereby increasing the numerator

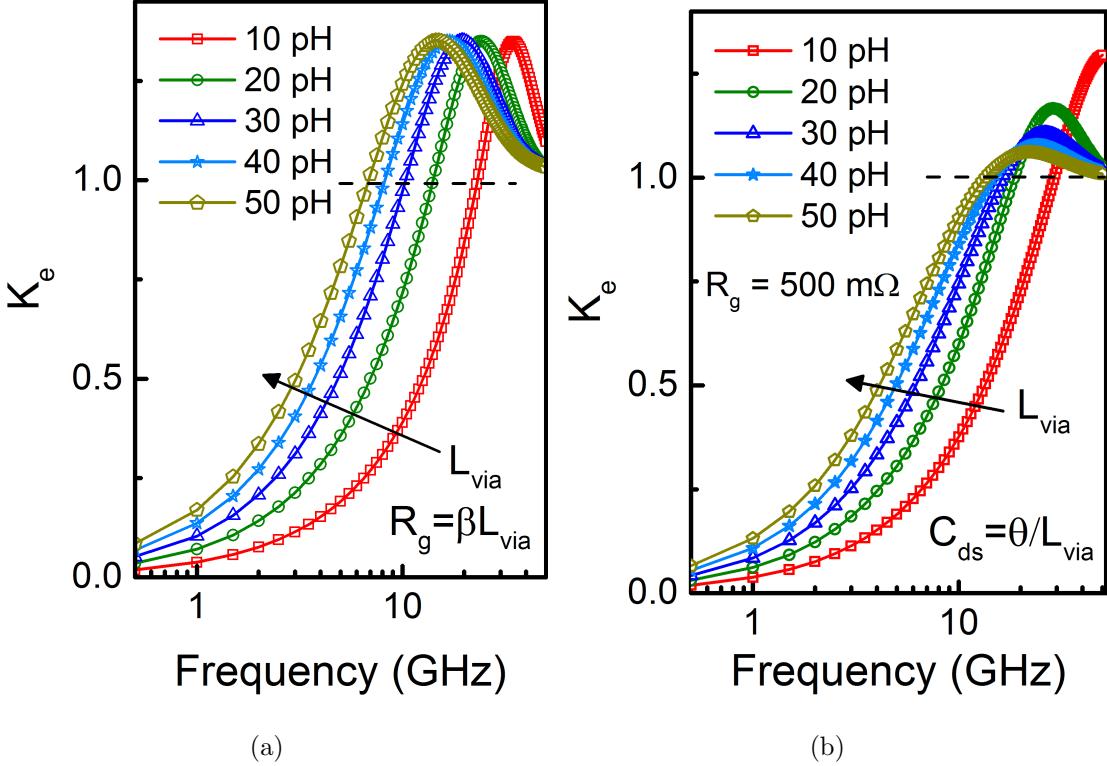
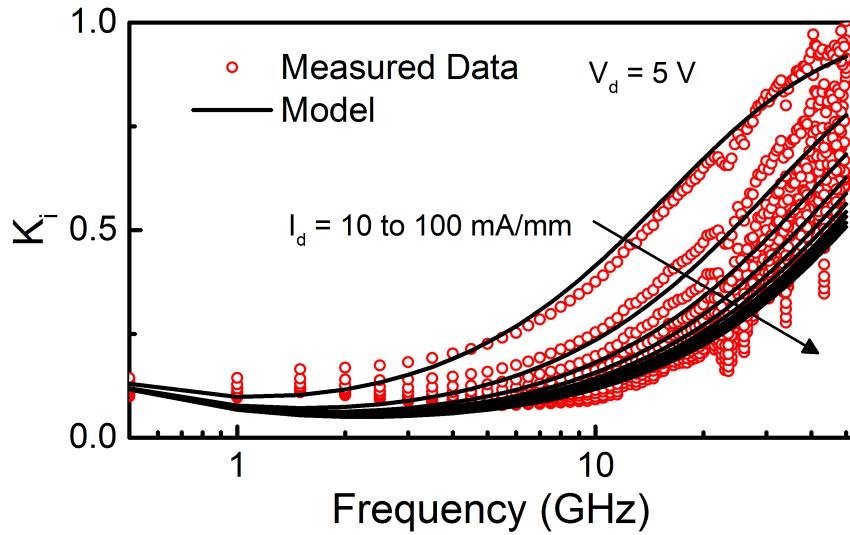


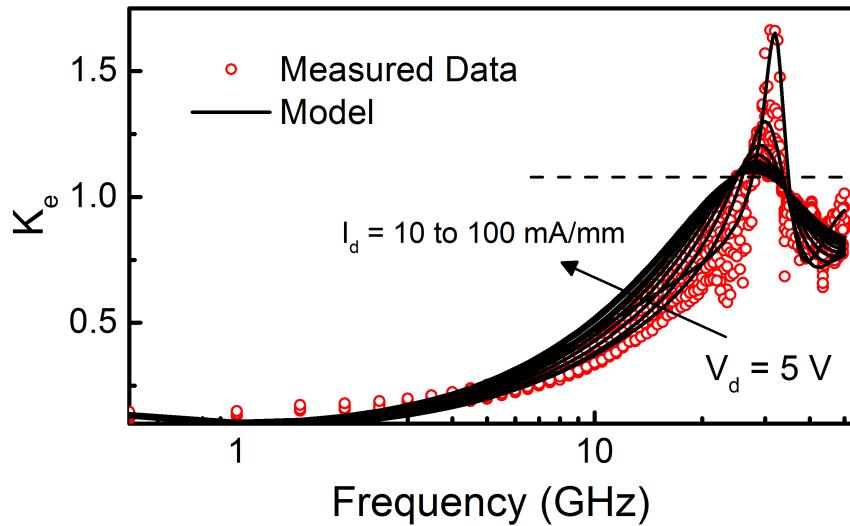
Figure 5.10: Plots of (5.35) obtained as L_{via} is increased together with a proportional (a) scaling up of R_g and (b) scaling down of C_{ds} , in order to prevent the degradation in K_e due to the valley as L_{via} is increased. $\beta = 0.05 \Omega/\text{pH}$ and $\theta = 2.5 \text{ pHF}$.

in (5.35). As an illustrative example, shown in Fig. 5.10(a) is the K_e as L_{via} is gradually increased, while $R_g = \beta L_{via}$, keeping β fixed. It is seen that f_K reduces without K_e dropping below 1, which ensures the unconditional stability of the device, although the noise performance as well as the power gain of the device would be compromised. Alternately, proportionately scaling down C_{ds} as L_{via} is increased, as shown in Fig. 5.10(b), can be done to reduce f_K and prevent the degradation of K_e without compromising on the noise or power gain performance. The impact of C_{ds} on stability could be of importance in advanced GaN structures particularly those with source-connected field-plates, where increased values of C_{ds} are observed.

Finally, shown in Fig. 5.11(a) and 5.11(b) are the measured overlays of K at intrinsic and extrinsic levels respectively for a commercial $10 \times 90 \mu\text{m}$ GaN HEMT taken for multiple current densities ($10 - 100 \text{ mA/mm}$). The peak-valley pair is



(a)



(b)

Figure 5.11: Measured and modeled overlays of (a) Intrinsic and (b) Extrinsic K-factor for a $10 \times 90 \mu\text{m}$ GaN device, taken for operating current densities of $10 - 100 \text{ mA/mm}$ for a frequency range of $0.5 - 50 \text{ GHz}$. The intrinsic K-factor is seen to degrade with increasing current density. The extrinsic K-factor exhibits the peaks and valleys which emerges due to the presence of the via-inductance. Excellent model agreement is observed with measured data for different bias conditions. The contribution of gate contact resistance (0.5Ω) was deembedded from the extrinsic measured data.

clearly visible within the observed frequency range (0.5 - 50 GHz) for the extrinsic measured data, in which K_e drops below 1, clearly indicating the impact of L_{via} . Modeled overlays using the ψ -based model are also shown in Fig. 5.11 in which excellent model agreement is observed with measured data across multiple bias conditions. The bias-dependence of each small-signal element in the model is governed by a central bias-dependent physical quantity i.e. the surface-potential ($\psi(V_g, V_d)$), which in turn is a function of the bias-dependent quasi-Fermi level ($E_F(V_g, V_d)$) as discussed earlier in Chapter 2.

Summary

We presented a new approach to extract the small-signal model for a GaN HEMT using a single set of broadband Z-parameters. The proposed method is purely analytical and exploits some interesting characteristics in the extrinsic-level Z-parameters that are particularly seen in large gate-periphery devices due to their inherently larger intrinsic capacitances and their interaction with the bus inductances. Our method allows for a simultaneous extraction of the intrinsic as well as the extrinsic small-signal model components and can be used for any bias condition.

Also, the impact of source via-inductance on the stability performance of GaN HEMTs was studied using a small signal equivalent circuit model. Peaks and valleys, which could potentially make the device unstable, were pointed out as a manifestation of the interaction of the via-inductance with the intrinsic device components. These features are more noticeable in GaN devices due to their large gate peripheries. We also concluded that the C_{ds} in conjunction with the via-inductance has a detrimental effect on the stability factor as it deepens the valley. Therefore, if the via-inductance is increased to reduce f_K , C_{ds} should be proportionally scaled down so that the K-factor isn't degraded due to the valley. This analysis could be important from the perspective of design of source field-plated devices which exhibit increased C_{ds} .

Chapter 6

Kink-effects in RF Characteristics of GaN HEMTs - Analysis and Modeling

6.1 Introduction

This chapter is addressed towards analyzing and modeling the two major kink-effects reported in microwave devices - in h_{21} and S_{22} . h_{21} is an important figure of merit since it determines the unity current gain frequency (f_T) of a microwave device whereas S_{22} is crucial in determining the output matching network. Kink effects in both of these quantities therefore need to be considered which could be of importance to RF designers, both in the device and circuit domain. Here, both these effects are studied using mathematical expressions, which are further used to understand the impact of various model elements on the location and severity of these kink-effects.

We discuss a novel approach towards understanding the Kink-Effect (KE) in the Bode-plot of short circuit current gain (h_{21}) observed for microwave transistors, particularly GaN HEMTs. We ascribe the origin of the KE to the presence of a pair of complex conjugate poles at the frequency of interest, introduced due to the extrinsic parasitic inductances and their interaction with the device intrinsic elements

such as the capacitances and transconductance, and develop simplified mathematical expressions that govern the behaviour of the kink. We also present a physics-based compact model that is capable of capturing the KE and extensively validate the model against measured data for a GaN device under multi-bias conditions, thereby advocating the strong physical background of the model. We conclude by demonstrating the impact of various elements of the small signal model on the kink based on the developed mathematical hypothesis for KE.

The presence of KE in the Smith-plot of S_{22} severely affects the design of the output matching network for amplifiers based on these devices which calls for a precise consideration of this effect [133]. It originates due to the ambivalent nature of the output impedance of the intrinsic device, wherein it changes its nature from a low frequency series RC network to a high frequency parallel RC network, giving rise to a kink at the frequency where the contours corresponding to low and high frequency approximations intersect each other. The output impedance is a complicated function of the various intrinsic elements of the device small signal model, and all the device intrinsic characteristics in our model arise from a physics-based framework, therefore, making multi-bias validation of the kink-behaviour with measured data possible with sufficient ease.

6.2 Kink Effect in h_{21}

Kink-effects in the magnitude of the hybrid parameters of GaN HEMTs in the form of dips in h_{11} and h_{12} and peaks in h_{21} and h_{22} are observed, as shown in Fig. 6.1, similar to what was previously reported [150] for GaAs devices. Additionally, kink-effects in S_{22} have also been observed and modeled for GaN HEMTs [151]. Here, we address the KE in the high frequency region of the Bode-plot of h_{21} , which is highly detrimental for the device microwave behavior and is known to impact high frequency figures of merit particularly f_T . Crupi *et al.* attributed the KE to the phase cross-over of the open circuit output impedance (Z_{22}) [152]. Here, we essentially enhance that idea through an alternate approach i.e. by directly

evaluating the expression for h_{21} and calculating the complex conjugate pair of poles to identify the resonant frequency. We further exploit the pole-zero approach to quantify the severity of the kink by deriving the mathematical expression for its conditional existence at the frequency where the complex conjugate pair of poles is located. It is done by computing the damping factor (ζ) in terms of the small signal model elements. Secondly, we present a physics-based compact model, as against look-up and table based models used in the previously reported works [152, 153], to accurately predict the KE for GaN devices under a wide array of bias conditions, which is crucial from an RF circuit design perspective.

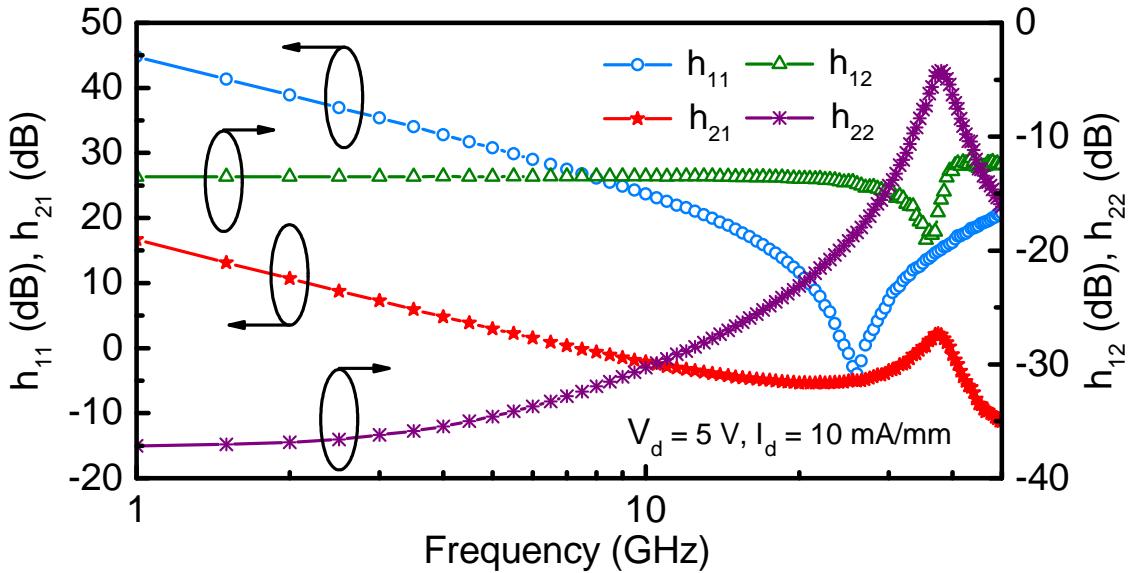


Figure 6.1: Kink effects observed in magnitude of all the four hybrid parameters for a $10 \times 90 \mu\text{m}$ GaN device, for $I_d = 10 \text{ mA/mm}$. Dips in h_{11} and h_{12} and peaks in h_{21} and h_{22} are seen, similar to those previously reported for GaAs devices [150].

6.2.1 Kink-Effect Theory and Formulation

The small signal equivalent circuit (SS–EC) representation of the device is shown in Fig. 6.2. The elements within the dashed box represent the bias dependent intrinsic components of the device, governed by our surface-potential-based model named the ASM-HEMT Model, which is formulated in a Verilog-A code discussed earlier in Chapter 2. The bias-independent extrinsic parasitic elements are shown outside

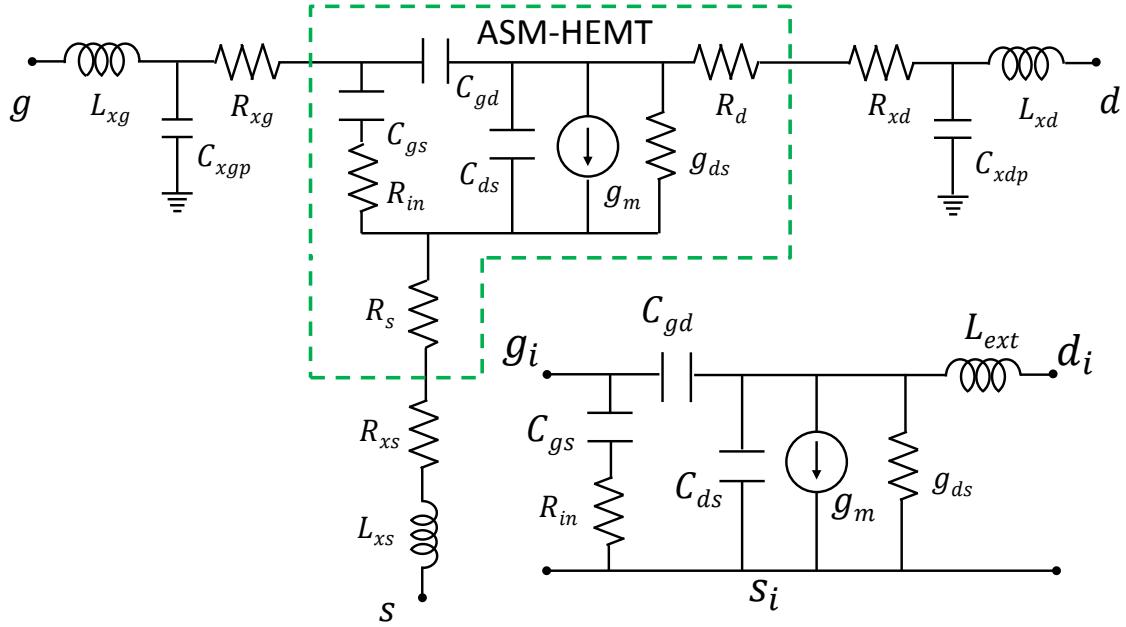


Figure 6.2: Small Signal Equivalent Circuit (SS–EC) Model of the device. The dashed region represents the intrinsic device as described by the ASM-HEMT model. The capacitances, output conductance and the transconductance are calculated self-consistently from the surface potential as discussed in Chapter 2 earlier. Bias independent extrinsic elements are also shown. Also shown is simplified SS–EC of the intrinsic device without access region resistances [125], omitted only in our hand analysis to obtain easier parameter extraction, in conjunction with the effective extrinsic inductance L_{ext} .

the dashed box. In Fig. 6.2, next to the overall device SS–EC, a simplified SS–EC is shown where we focus only on the capacitances (C_{gs} , C_{gd} and C_{ds}), the transconductance (g_m) and output conductance (g_{ds}) of the intrinsic device. L_{ext} , which represents the effective inductance presented by the source (L_{xs}) and drain (L_{xd}) inductances, is appended at the intrinsic drain node in order to realize the impact of the extrinsic inductive elements upon interaction with the intrinsic components. It must be noted that the access region resistances are included in the overall model simulation [125], however omitted only in the hand analysis to avoid complicated and lengthier expressions for (6.1–6.9).

The h_{21} calculated for this SS–EC is given in (6.1) as,

$$h_{21} = \frac{(g_m/C_{gd}) - s - s^2 R_{in} C_{gs}}{s [s^2 A + sB + (1 + C_{gs}/C_{gd})]} \quad (6.1)$$

$$A = \{C_{eq} + R_{in} C_{gs} (g_{ds} + sC_{ds})\} L_{ext} \quad (6.2)$$

$$B = R_{in} C_{gs} + [g_m + g_{ds} (1 + C_{gs}/C_{gd})] L_{ext} \quad (6.3)$$

where $C_{eq} = C_{gs} + C_{ds} + (C_{gs} C_{ds}/C_{gd})$. However, it is a point worthy to note that the non-quasistatic effects, which are captured by including a resistor R_{in} in series with C_{gs} , are generally observed at much higher frequencies (> 100 GHz) whereas the KE in h_{21} is seen at relatively lower frequencies (≈ 50 GHz) [150, 154]. We can, therefore, reduce (6.1) by ignoring the contribution of R_{in} to obtain (6.4)

$$h_{21} = \frac{(g_m/C_{gd}) - s}{s [s^2 L_{ext} C_{eq} + sg'_m L_{ext} + (1 + C_{gs}/C_{gd})]} \quad (6.4)$$

where $g'_m = g_m + g_{ds} (1 + C_{gs}/C_{gd})$. As can be seen, it is a single zero and 3-pole system with the zero z_1 located at $\omega = g_m/C_{gd}$ ($\approx 10^{12}$ rad/s) and one of the poles p_1 at $\omega = 0$.

The locations of other two poles p_2 and p_3 are given as

$$p_{2,3} = \frac{-g'_m L_{ext} \pm \sqrt{g'^2_m L_{ext}^2 - 4L_{ext} C_{eq} (1 + C_{gs}/C_{gd})}}{2L_{ext} C_{eq}} \quad (6.5)$$

The term $g'^2_m L_{ext}^2$ in the square root is much smaller than the second term for a HEMT device, particularly in our case of extracted values of SS–EC elements, and hence can be ignored, leaving behind a much simpler expression for poles $p_{2,3}$ as

$$p_{2,3} \approx \pm j \sqrt{\frac{1 + C_{gs}/C_{gd}}{L_{ext} (C_{gs} + C_{ds} + C_{gs} C_{ds}/C_{gd})}} \quad (6.6)$$

Since C_{gd} is generally much smaller than C_{gs} in saturation region, we can further simplify the expression as

$$p_{2,3} \approx \pm j \frac{1}{\sqrt{L_{ext} (C_{gd} + C_{ds})}} \quad (6.7)$$

The above expression represents a pair of complex conjugate poles p_2 and p_3 . It is this pair of poles which causes the emergence of a kink in h_{21} bode-plot. It happens when the ζ , which marks the boundary between complex (oscillatory motion) and real (exponential motion) roots, for this second order system becomes less than 0.5 [155, 156]. ζ can be obtained from (6.4) and the condition for emergence of kink can be written as

$$\zeta = \frac{g'_m}{2} \sqrt{\frac{L_{ext}}{(C_{gs} + C_{ds} + C_{gs}C_{ds}/C_{gd}) (1 + C_{gs}/C_{gd})}} \leq 0.5 \quad (6.8)$$

We can simplify this condition by considering C_{gd} as a relatively smaller quantity in comparison to C_{gs} , given as

$$\zeta \approx \frac{\{g_m + g_{ds} (1 + C_{gs}/C_{gd})\} C_{gd}}{2C_{gs}} \sqrt{\frac{L_{ext}}{C_{ds}}} \leq 0.5 \quad (6.9)$$

This simplified expression for ζ gives an accurate behaviour followed by the kink, if the various model elements were to vary, as shown in the next section.

6.2.2 Comparison with measured data

We have implemented the model formulations in Verilog-A and performed simulations in Keysight's ADS circuit simulator. To start with, Fig. 6.3 shows an extensive comparison of the measured and modeled results for h_{21} of a $10 \times 90 \mu\text{m}$ device for 20 different bias conditions - 2 different values of drain voltage V_d (5V and 20 V) with 10 different values of gate voltage V_g ($I_{ds} = 10$ to 100 mA/mm) for each value of V_d . For each of the sub-plots, h_{21} starts off by falling at 20 dB/dec due to the pole $1/s$ at $\omega = 0$, rises in the form of a kink as ω approaches the complex pair of poles $p_{2,3}$, and then upon extrapolating, further falls steeply at 60 dB/dec after having crossed $p_{2,3}$ [152]. The kink is observed to be severe for V_g values that result in low I_{ds} , which is understandable since low g_m reduces ζ and therefore a greater peaking as suggested by (6.9). The kink-frequency (f_k) increases with increasing V_d , which can be ascribed to reduced C_{gd} and C_{ds} with increasing V_d , causing $p_{2,3}$ to shift towards higher frequencies as governed by (6.7). Moreover, it is seen that for

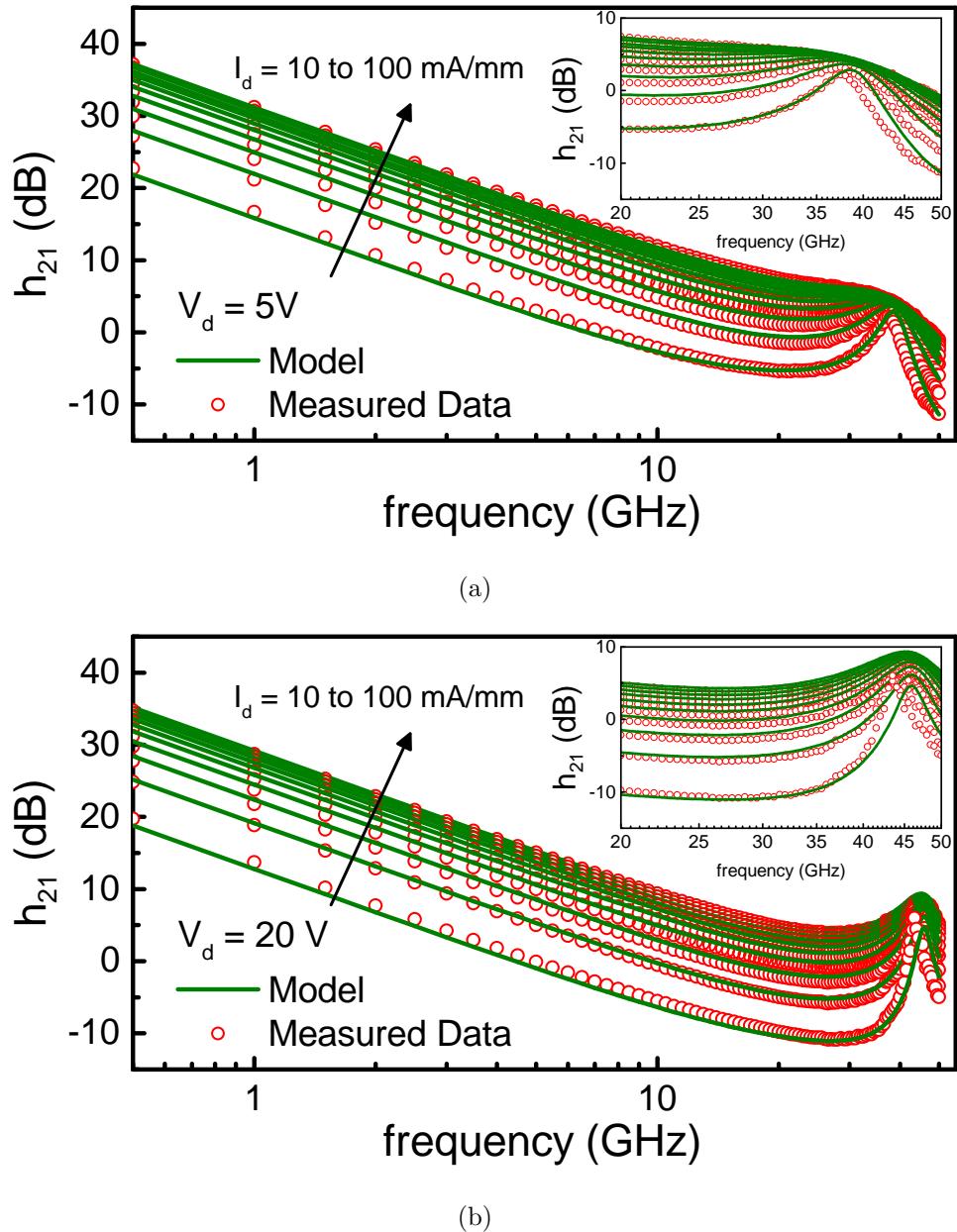


Figure 6.3: Broadband Bode plots of h_{21} for a frequency range of 500 MHz to 50 GHz for a $10 \times 90 \mu\text{m}$ device. Two different V_d values (a) 5 V (b) 20 V, each with ten V_g values. h_{21} drops at -20 dB/dec, before reaching the pair of complex poles, where kink is observed. The measured and modeled results are in excellent agreement.

V_g values with higher I_{ds} the kink emerges before f_T which signifies the importance of modeling the KE in h_{21} . Precise modeling of the KE with various bias conditions emphasizes the accuracy of bias dependence of the modeled device characteristics.

6.2.3 Variation with Model Elements

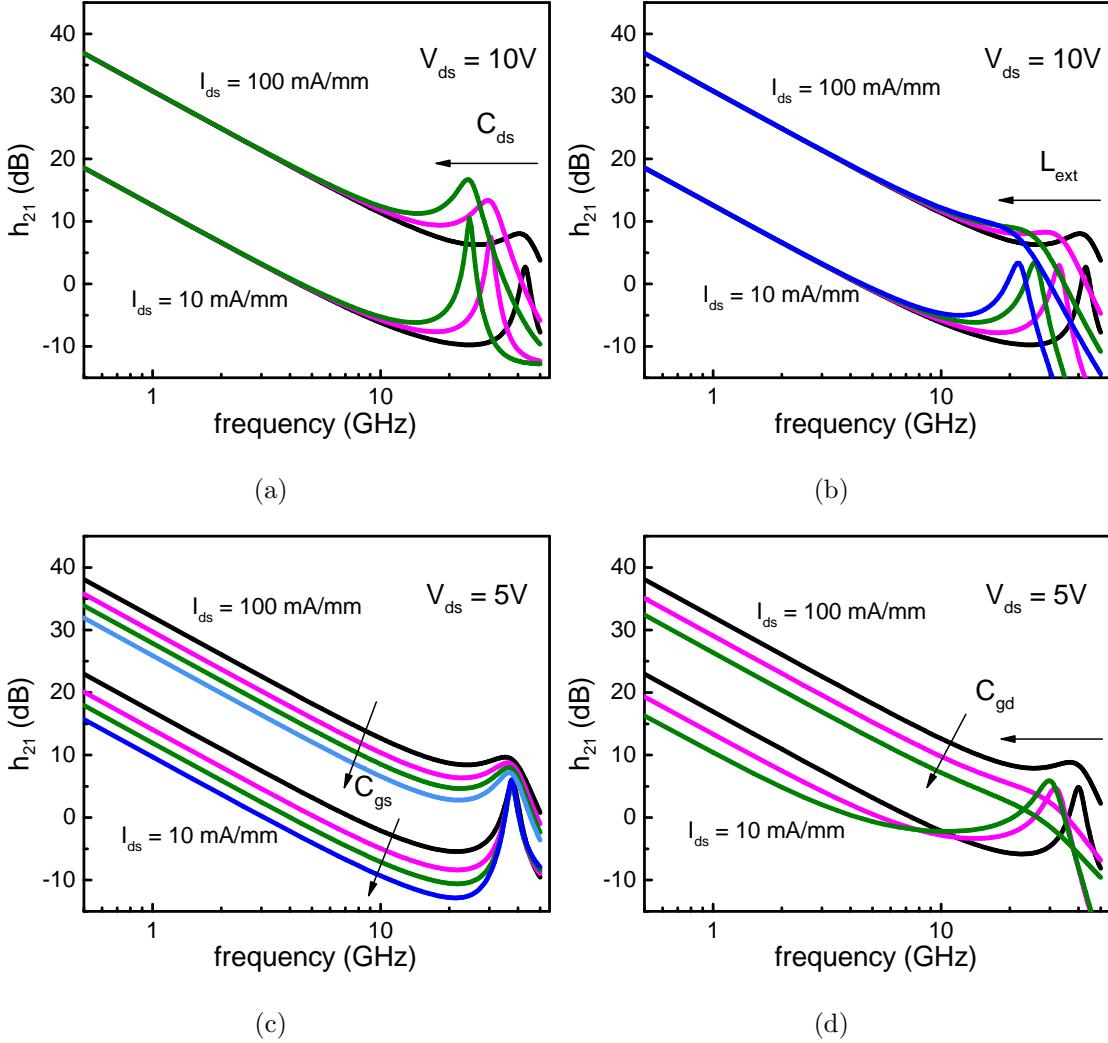


Figure 6.4: Simulated h_{21} bode-plots highlighting the impact on the kink by individually varying (a) C_{ds} , (b) L_{ext} , (c) C_{gs} and (d) C_{gd} . The arrows indicate the direction of increasing values of model elements. The location of the kink as well as its severity is seen to be obeying trends in accordance with (6.7) and (6.9) respectively.

The impact of variation in various small signal model elements on the nature of the kink is highlighted in Fig. 6.4. The results are in accordance with (6.7) and (6.9). As is seen, the kink sharpens and shifts to lower frequencies as C_{ds} is increased. Increasing L_{ext} causes a similar effect as far as the shifting of the kink frequency is concerned, however, it causes a smoothing of the kink for high V_g values

since it increases ζ and eventually pushes it beyond 0.5, whereas for low V_g values no smoothing of the kink is observed since low g_m is the dominant term in restricting ζ below 0.5. Increasing C_{gs} increases the prominence of kink as it reduces the overall gain as well as ζ , however C_{gs} variation has no impact on the location of the kink since the simplified expression for $p_{2,3}$ is independent of C_{gs} . C_{gd} variation effects the location of the kink as dictated by (6.7). Increase in C_{gd} smoothens the kink for high V_g values, which is obvious since it increases ζ but has little impact on the sharpness of the kink for low V_g values, where low g_m dominates in restricting ζ .

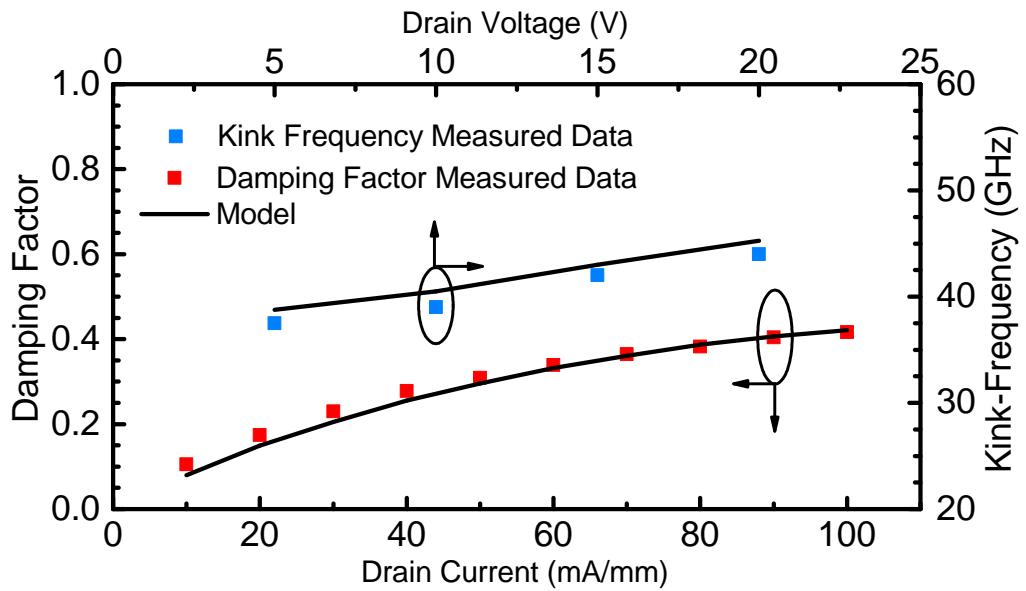


Figure 6.5: Comparison of measured and modeled bias-dependence of kink-frequency (f_k) (for $I_d = 10$ mA/mm) and damping factor (ζ) (for $V_d = 5$ V), as functions of V_d and I_d respectively. Small signal elements extracted using methodology described in Chapter 4 are plugged in (6.7) and (6.9) to get f_k and ζ .

Shown in Fig. 6.5 is a good quantitative agreement between the predicted and measured f_k and ζ variations with bias, obtained using (6.7) and (6.9). Parameter extraction methodology presented in Chapter 4 is used to extract the values of small signal elements that are plugged in (6.7) and (6.9). The model accurately captures f_k vs V_d and ζ vs I_d .

6.3 Kink Effect in S_{22}

The presence of this kink in the Smith-plot of S_{22} severely affects the design of the output matching network for amplifiers based on these devices which calls for a precise consideration of this effect. The kink-effect originates due to the ambivalent nature of the output impedance of the intrinsic device, wherein it changes its nature from a low frequency series RC network to a high frequency parallel RC network. It gives rise to a kink at the frequency where the contours corresponding to low and high frequency approximations intersect each other, as illustrated in Fig. 6.6.

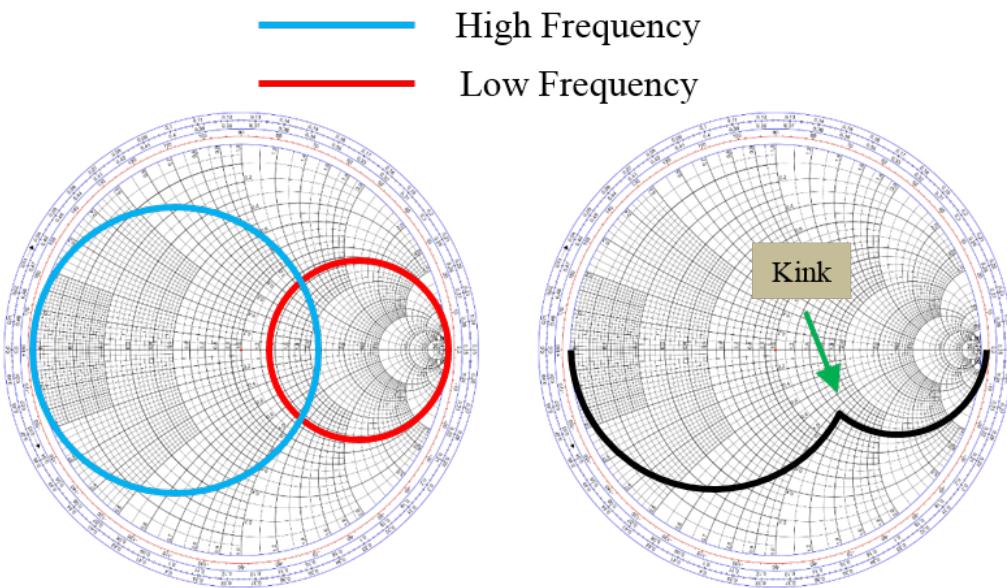


Figure 6.6: Smith plot cartoons illustrating formation of kink at the intersection of impedance and admittance circles corresponding to series RC and parallel RC networks respectively.

The output impedance is a complicated function of the various intrinsic elements of the device small signal model, and all the device intrinsic characteristics in our model arise from a physics-based framework, therefore, making multi-bias validation of the kink-behaviour with measured data possible with sufficient ease.

It has been observed that there exists a kink in the Smith-plot of the scattering parameter (S_{22}) for microwave transistors. Previous studies carried out on this phenomenon have thoroughly investigated the cause for this anomalous observation

[153,157,158]. The following points summarize the extract of their analysis regarding the kink-effect:

1. The kink originates due to the anomalous nature of the output impedance (Z_{out}), which manifests itself as a series-RC network at low-frequency and a parallel-RC network at high-frequency. The low and high frequency approximations of Z_{out} follow constant resistance ($r + \frac{1}{j\omega C}$) and constant conductance ($g + j\omega C$) contours respectively, leading to emergence of a kink at a frequency which represents the point of intersection of the two contours.
2. The effect is purely due to the intrinsic device and the extrinsic parasitic elements of the device only affect the shape of kink [151].
3. The intrinsic elements of the device small signal model determine the value of Z_{out} . S_{22} , being a strong function of Z_{out} , therefore gets influenced by variation in the intrinsic device characteristics such as the transconductance (g_m), capacitances (C_{gs} , C_{gd} and C_{ds}) etc.
4. Increasing g_m and C_{gd} cause the kink to become more pronounced whereas an increase in C_{gs} shifts the kink towards the open circuit load on the Smith-chart. However, the kink-effect diminishes upon increasing C_{ds} .

Crupi *et al.* proposed a technique to quantify the strength and thereby get a deeper insight of the kink-effect. Moreover, they demonstrated a model that reproduces this kink behaviour in S_{22} [153]. However, their core calculations i.e. the drain current, intrinsic charges etc. were based on a look-up table (LUT) model [159]. The limitation that a LUT based model is faced with is its dependence on interpolation functions to compute values for operating conditions for which the data is missing. Furthermore, LUT based models are limited in usage when it comes to scalability.

Since GaN based HEMTs inherently exhibit superior g_m as against transistors from GaAs and Si based technologies, they tend to show prominence of the kink-effect in S_{22} . As a consequence, the design of broadband output matching networks

for RF power amplifiers based on GaN HEMTs tends to get complicated. A compact model that very well captures this feature as well as how this behaviour changes with different operating bias conditions, different device geometries etc. is a must if we are to use such a device in the large signal operation at microwave frequencies.

6.3.1 S_{22} Kink-Effect Theory

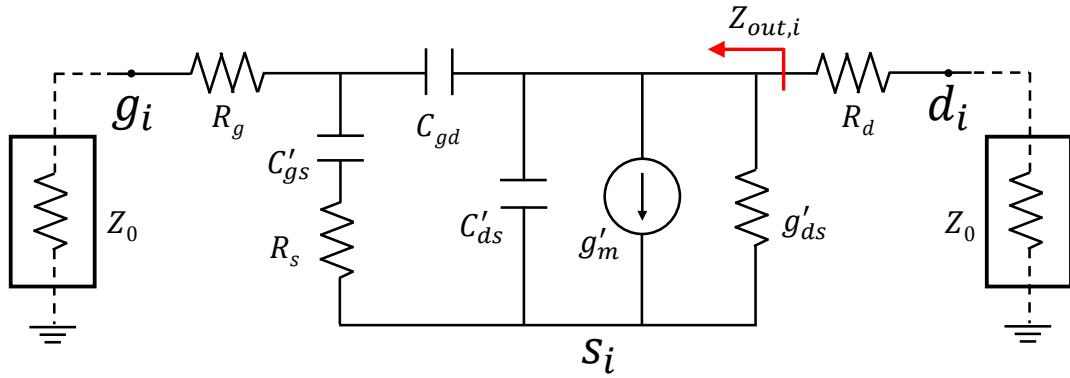


Figure 6.7: SS-EC of the intrinsic device with transformation of R_s absorbed as shown. g'_m , g'_{ds} , C'_{gs} and C'_{ds} are the intrinsic values divided by $1 + g_m R_s$. Both the ports are terminated with Z_0 .

The small signal equivalent circuit (SS-EC) representation of the device is shown in Fig. 6.7. It is a simplified version of the one shown in Fig. 6.2 where only the intrinsic part is considered since the KE in S_{22} originates from the intrinsic SS-EC [157]. Here R_s is absorbed in and each one of C_{gs} , C_{ds} , g_{ds} and g_m in the transformed intrinsic network gets divided by a factor of $1 + g_m R_s$ and updated to C'_{gs} , C'_{ds} , g'_{ds} and g'_m respectively. Both the input and the output ports are terminated with the characteristic impedance (Z_0). The output impedance (Z_{out}) can be derived for this SS-EC and written as

$$Z_{out}(s) = \left[g'_{ds} + sC'_{ds} + \frac{sC_{gd}}{G_0} \left(\frac{g'_m + sC'_{gs}}{1 + sC'_{gs}R_s} + \frac{1}{Z_0 + R_g} \right) \right]^{-1} \quad (6.10)$$

$$G_0 = sC_{gd} + \frac{1}{Z_0 + R_g} + \frac{sC'_{gs}}{1 + sC'_{gs}R_s} \quad (6.11)$$

S_{22} can now be calculated in terms of Z_0 as

$$S_{22}(s) = \frac{Z_{out}(s) - Z_0}{Z_{out}(s) + Z_0} \quad (6.12)$$

The expression in (6.10) at low and high frequencies leads to $Z_{out,i,low}(s)$ and $Y_{out,i,high}(s)$ respectively, given as

$$Z_{out,i,low}(s) = \frac{1}{g'_{ds}} + \frac{1}{g'_m + 1/(Z_0 + R_g)} + \frac{1}{sC_{gd}[1 + g'_m(Z_0 + R_g)]} \quad (6.13)$$

$$Y_{out,i,high}(s) = \frac{1}{Z_{out,i,high}(s)} = g'_{ds} + \frac{g'_m C_{gd}}{C'_{gs} + C_{gd}} + sC'_{ds} + \frac{sC_{gd} C'_{gs}}{C'_{gs} + C_{gd}} \quad (6.14)$$

A careful examination of the above two expressions reveal that $Z_{out,low}$ and $Y_{out,high}$ attain the form $r + (1/j\omega C)$ and $1/(g + j\omega C)$ respectively, leading to the formation of the kink.

6.3.2 Comparison with Measured Data

S-parameter measurements for the same Qorvo GaN device, discussed in Chapter 4, is used for the sake of model validation. The S-parameter are simulated from 500 MHz to 50 GHz. To start with, Fig. 6.8 shows an extensive comparison of the measured and modeled results for S_{22} of the $10 \times 90 \mu\text{m}$ device for 40 different bias conditions - 4 different values of drain voltage V_d (5 V to 20 V) with 10 different values of gate voltage V_g ($I_{ds} = 10$ to 100 mA/mm) for each value of V_d .

For each of the sub-plots, the kink-effect gains prominence as V_g is increased. This is primarily due to an increased values of g_m for higher V_g . Moreover, the Z_0 on the Smith-chart corresponding to the kink frequency shifts towards the short circuit load as V_g increases which is due to a strong increase in the drain conductance (g_{ds}) with increasing V_g . In Fig 6.8, as V_d is increased and keeping V_g fixed, the kink starts to diminish since the gate-drain capacitance C_{gd} follows a decreasing trend.

The accurate modeling of the kink-effect with various bias conditions emphasizes the accuracy of bias dependence of the modeled device characteristics such as

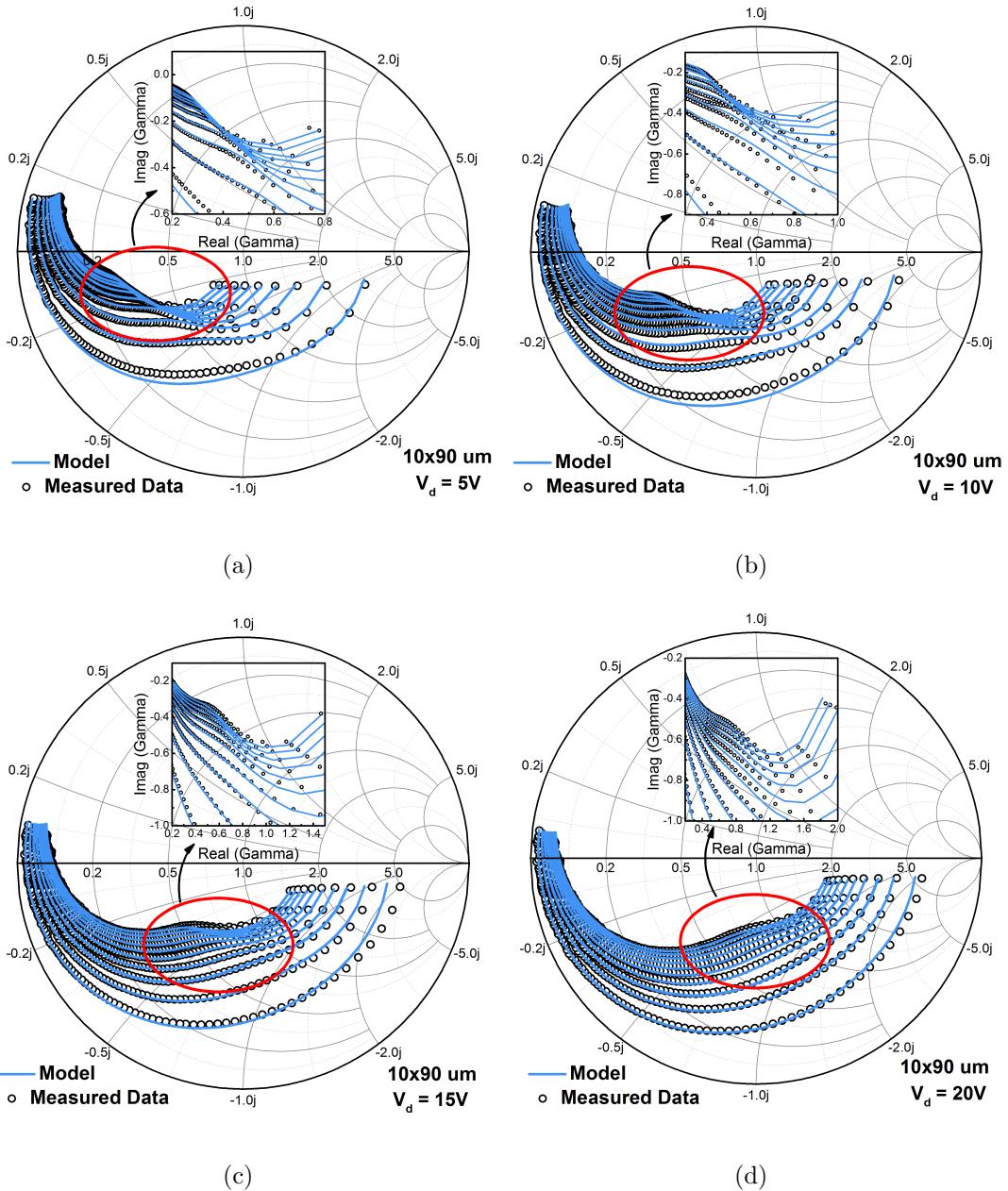


Figure 6.8: Broadband Smith-Plots of S_{22} for a frequency range of 500 MHz to 50 GHz for a $10 \times 90 \mu\text{m}$ device. Results are shown for four different V_d values (a) 5 V (b) 10 V (c) 15 V (d) 20 V, each with ten V_g values (Outer contours: 10 mA/mm, Inner Contours: 100 mA/mm). The kink-effect is more pronounced as V_g increases which is due to higher g_m for higher V_g , as long as self heating is not achieved. With increasing V_d , the kink loses prominence due to a corresponding decrease in C_{gd} with drain bias. Insets are added for better clarity of the region of interest.

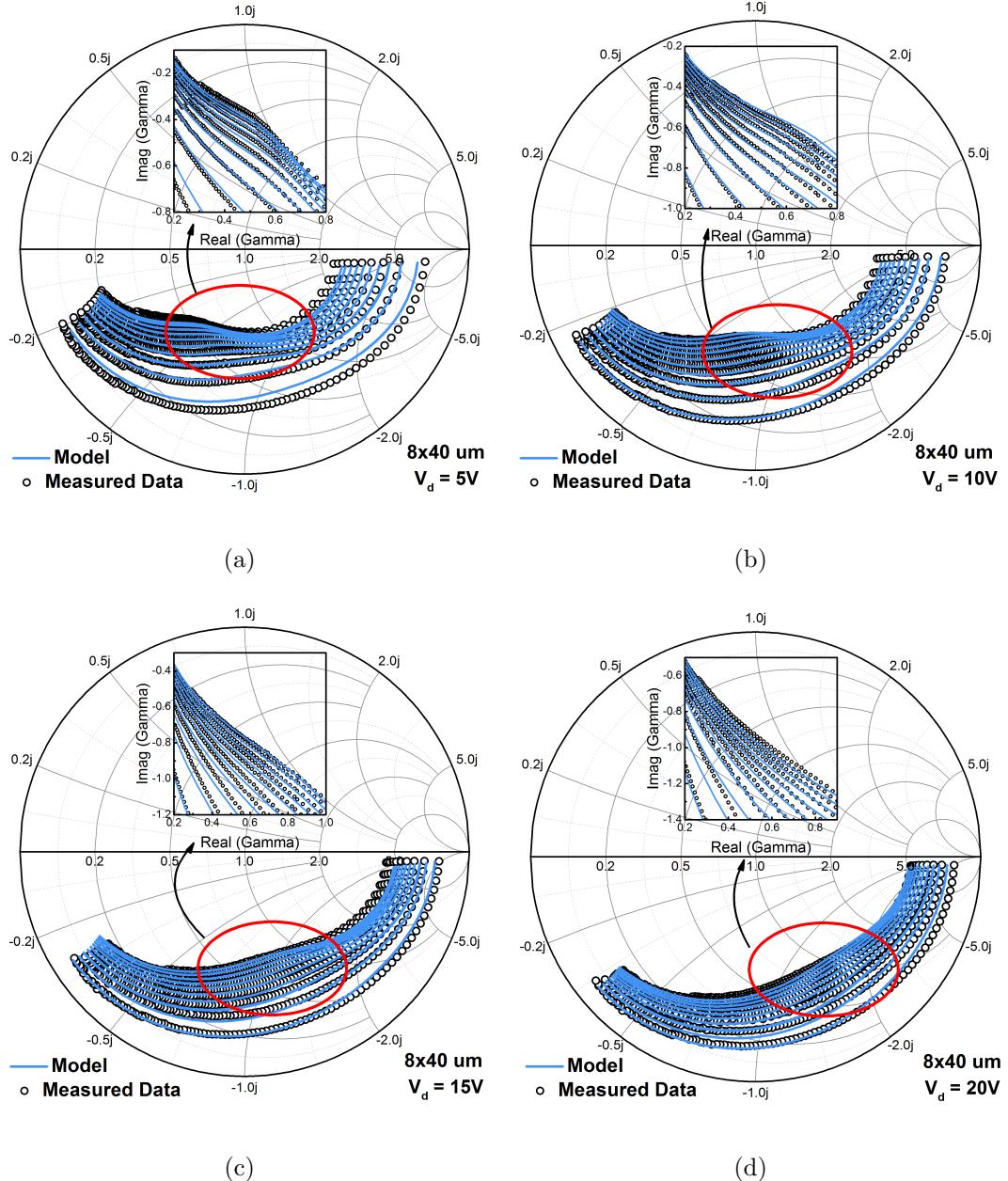


Figure 6.9: Broadband Smith-Plots of S_{22} for a frequency range of 500 MHz to 50 GHz for a $8 \times 40 \mu\text{m}$ device. Results are shown for four different V_d values (a) 5 V (b) 10 V (c) 15 V (d) 20 V, each with ten V_g values (Outer contours: 10 mA/mm, Inner Contours: 100 mA/mm). The trend followed by the kink with respect to bias conditions is similar to that in Fig. 6.8, although the kink is less pronounced for this device which can be attributed to lower value of C_{gd} for the $8 \times 40 \mu\text{m}$ device.

the transconductance and the intrinsic capacitances that are instrumental in determining the Z_0 and therefore the kink in S_{22} as well.

In order to have scalability with respect to geometry in the model, it is important that the validation is carried out for different device physical parameters. In Fig. 6.9, similar results are shown for a device with relatively smaller gate periphery - $8 \times 40 \mu\text{m}$. Parameters extracted for this device are proportionally scaled which again highlights the key advantage of scalability offered by a compact model with a physical background. The trends followed by the kink in response to changes in V_g and V_d are similar to our observations in Fig. 6.8, however, the kinks for the $8 \times 40 \mu\text{m}$ device for same bias conditions look less prominent as compared to the $10 \times 90 \mu\text{m}$ device, which is obvious since there is a significant decrease in g_m for the former.

Summary

We presented a pole-zero approach to understand the Kink-Effect in h_{21} for GaN HEMTs, which originates due to the existence of a complex pair of poles and the subsequent instability caused at the frequency of interest. We derived simplified mathematical expressions to calculate the location of the kink as well as the conditions that may lead to its severity. Additionally, we modeled this Kink-Effect using our physics-based compact model, and extensively validated the modeled results with multi-bias measured data. An analysis was also done to highlight as to how the kink responds to variations in different model elements or bias conditions.

The model's capability of predicting the kink observed in the S_{22} Smith-plot of GaN HEMTs was also demonstrated. A thorough validation in a multi-bias setup was extensively carried out with measured data for two different GaN devices with different gate peripheries ($10 \times 90 \mu\text{m}$ and $8 \times 40 \mu\text{m}$) and an excellent agreement between measured and modeled results was obtained. Our results for the changing behavior of the kink with respect to changing bias and geometry conditions advocate the strong accuracy in the modeling of the intrinsic device characteristics that play an important role in determining the kink in S_{22} .

Chapter 7

Conclusion

7.1 Key Findings

GaN today is the most promising material to be used for making transistors in the power-electronics and the RF domain. It is imperative for the device modeling community to come up with high fidelity modeling solutions such that suitable harnessing of the promising GaN technology can be accomplished by translating them into viable circuit applications. It was also stated that the Compact Model Coalition (CMC) has been overseeing the development of an industry standard GaN HEMT model for wide-scale use across the academia and the industry. Major part of this thesis has gone into the development of an industry standard model fulfilling all the stringent requirements set by CMC. The key take-aways and vital contributions of this thesis are summarized as follows:

- Analysis and modeling of the capacitance behavior in Field-plated Power GaN HEMTs was done in order to precisely capture their switching behavior in high power applications.
- TCAD and Mixed model simulations were used to study the impact of Field-plates on switching waveforms when the GaN HEMT was used in an inductive load switching circuit.
- A complete modeling solution and parameter extraction methodology, all the

way from DC to RF large-signal simulations, was demonstrated and successfully validated with a broad array of measurements.

- Statistical simulation was carried out using the described GaN HEMT model to identify key sources of variability.
- Novel extraction technique was proposed based on certain interesting characteristics shown by large gate-periphery GaN HEMTs.
- It was proposed that in large gate-periphery microwave devices, including GaN HEMTs, the impact of via inductances on intrinsic device stability was significant as it couples with the drain to source capacitance to lead to dips in the Rollett's stability factor.
- A pole-zero approach to modeling and analyzing the Kink-Effect in h_{21} of GaN HEMTs was reported.
- The model's capability to accurately capture the Kink-Effect in S_{22} of GaN HEMTs for multiple bias and geometry conditions was also demonstrated.
- Lastly, and more importantly, the model was successfully pushed towards becoming an Industry Standard for wide scale usage and testing by various EDA vendors.

7.2 ASM-GaN-HEMT Modules

A close collaboration with the industry helped a great deal in staying up to date with the state-of-the-art tools and practices in the area. Some key learnings and important modules that were incorporated in the ASM-GaN-HEMT Model are briefly described in this section.

Keysight's ICCAP modeling software [160], which is the bread and butter of device modeling engineers, was exhaustively used during this thesis. It is a highly sophisticated tool to incorporate models formulated in advanced languages such as Verilog-A as well as load measured data at the same time, thereby providing the

platform for parameter extraction. It also has a powerful programming framework based on the parameter extraction language (PEL), which is very handy in customizing and macro-programming for making turnkey extraction solutions for industry standards. The detailed parameter extraction methodology developed in this work has been implemented in this tool.

All the modules developed in this thesis were implemented in Verilog-A, which is a widely used hardware description language (HDL) used in the industry. A working understanding of some key concepts and practices [161], such as code-modularity for specific model effects and block function calls for particular model calculations, was obtained during the course of this doctoral thesis. For instance, the field-plate model was implemented as a separate module. The use of the FP model is made user friendly by having various flag-mods (FPMOD) that condition the connection of the FP to either the gate or the source electrode, based on the structure. The individual set of calculations such as evaluation of surface-potential at drain and source for each FP transistor was done using functional calls, each one with a unique set of parameters as arguments corresponding to each FP transistor. Likewise, the Trap Model (TRAPMOD) and Self Heating Model (SHMOD) were also incorporated as separate modules.

The Access Region Resistance Model (RDSMOD) was incorporated within the Verilog-A code, therefore, making it a part of the intrinsic core current model. Its benefit was realized during the RF parameter extraction as it allowed for simplified expressions for transistor Y-parameters.

The ASM-GaN-HEMT Model Process Design Kit (PDK) was developed in Keysight's Advanced Design System (ADS) [111]. The essentials of library definitions, model parameter definitions in AEL files, and design kit integration were understood during the PDK development process which was further put to use in running small-signal and large-signal RF simulations. ADS was also used in Thru Reflect Load (TRL) measurement based de-embedding of the pad parasitics and manifolds using s2p 'de-embed' components.

While most of the measured data presented in the thesis was received from

CMC as part of the standardization activity, nevertheless, familiarity with the minute nitty gritties of DC and RF characterization was also attained at Nanolab, IIT Kanpur.

7.3 Scope for Future Work

Based on the research work carried out in this thesis on Modeling and Analysis of GaN HEMTs, following aspects are identified as future research in these areas:

- The ASM-GaN-HEMT model was successfully shown to work well with large signal simulations such as load pull and harmonic balance. It would be an interesting problem to study and model the linearity aspect of GaN HEMTs using the discussed model. Key linearity indicators such as intermodulation distortion and third order intercept point could be simulated using the physics-based model to understand potential bottlenecks in linearity behavior of GaN HEMTs and to look for possible solutions from a device or circuit design point of view.
- GaN-based FinFETs have recently emerged as devices for suppressed short channel effects [162] and high electron velocity [163]. Improved electrostatics boost up the RF performance and linearity in comparison to the traditional planar HEMTs [164]. It would be a nice exercise to come up with a physics-based model for these devices.
- The RF sub-circuit used might seem to capture the characteristics up to 50 GHz or more. However, a more complex network for applications on the higher side of 100 GHz might be required, of course at the expense of an increased node count which would reduce simulation speed.
- An RC sub-circuit based trap model is incorporated to account for trapping effects in GaN HEMTs. A physics-based fully analytical trap model valid for multiple geometry, stress and bias conditions could be a possible area of extending the ASM-GaN-HEMT Model.

- A thorough and exhaustive benchmarking and validation of the ASM-GaN-HEMT Model can be done at circuit-level to get a flavor of the robustness of the model as far as convergence is concerned. Designing and hardware-prototyping of RF power amplifiers and power converters would prove to be an excellent model evaluation step.
- Recently, Gallium Oxide (Ga_2O_3) has been identified as a promising contender for the next generation power devices [165,166]. There would soon be a demand for good compact models for the same. The ASM-GaN-HEMT model could be used as a starting point as it is capable of modeling transistors for power-electronics and RF applications and, therefore, could cater to emerging device technologies as well.

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