MOSFET Modeling Adapted for Switched Applications Using a State-Space Approach and Internal Capacitance Characterization

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Abstract— **This paper presents a new approach to MOSFET modeling using a state-space technique. The model is based on discrete elements whose values are extracted from measurements, datasheet parameters and SPICE® equations. The switching characteristics of the component are strongly determined by the gate-drain capacitance (C_{GD}). With help of thorough impedance measurements, characterization of this capacitance as a function of the applied external voltages is possible. Simulations and measurements show good agreement and the model gives possibilities for e.g. controller design thanks to the state-space implementation.**

Keywords-component; Semiconductor device measurements, Semiconductor device modeling, MOSFET switches, State space methods.

I. INTRODUCTION

When considering a power MOSFET intended for switching applications, many different models and simulation software are available if the behavior of the component needs to be simulated. Some common simulation languages that can be implemented in a Simulink® environment are SimElectronics®, SimPowerSystems® and PLECS® that all use some kind of simplified MOSFET model. All these languages are good at modeling larger systems but when it comes to detail modeling and characterization of the internal stray elements and EMI prediction, they show clear deficits due to extensive simplifications. Perhaps the most widespread program used for analog electric simulations is SPICE® which covers many different component models, including MOSFET's. However, the MOSFET model originally incorporated in SPICE® is intended for laterally diffused structures which make it unsuitable for power MOSFET that have a vertically diffused structure mainly due to its complex gate capacitance. Semiconductor manufacturers have solved this by making a black-box model which consists of several internal elements without physical coupling. It is concluded that these models show rather good compliance with measurements; but the black-box solution makes them unsuitable for detailed modeling where stray-elements needs to be taken into account. SABER® from Synopsys® might be an alternative, but since many of the models are encrypted or operate with the same principle as the SPICE® model, the usage for evaluative purpose and analytical controller design can once again be considered limited. The purpose of this article is to present a more detailed power MOSFET model comprising of discrete elements proposed. The model is adapted for switching applications and implemented via state-space modeling which makes it useful for e.g. controller design [1]

II. MOSFET MODELING USING THE STATE-SPACE APPROACH

Many studies have been performed in how the switching behavior of a power MOSFET can be modeled with various approaches. The usage of these models tend to be somewhat limited and most important of all, the practical applications have been limited due to e.g. complex parameter extraction procedures. The model proposed in this article aims at representing the MOSFET with simple discrete circuit elements in combination with already known equations.

In many circuit simulators are Modified Nodal Analysis (MNA) used to solve a consistent set of simultaneous equations obtained by invoking Kirchhoff's current law for each node in the circuit [2, 3]. Gaussian elimination and LU factorization are then applied to solve the resulting equation. Practical electric circuits contain many nonlinear elements such as diodes and transistors. The common approach to solve these elements, e.g. diode characteristics, is by linearization using the Newton-Raphson method. This method is known to be very fast, but also to have convergence problems when e.g. semiconductor junctions with exponential relationships are included. The focus of this article is not aimed at speed of the solver or simple implementation but rather at investigating the stability of the system by using transfer functions and developing suitable controller structures. These properties make state space representation more suitable rather than nodal analysis. The general state-space equations can be expressed as

$$\begin{aligned} \dot{x}(t) &= f(x(t),u(t)) \\ y(t) &= g(x(t),u(t)) \end{aligned} \tag{1}$$

where *x(t)* is the states, *u(t)* is the input to the system and *y(t)* is the output of the system.

The MOSFET model proposed consists of discrete elements and is depicted in Fig. 1. The main elements are the current generator, I_{DS}, determining the static behavior based on the well-known SPICE® equations [4], and the capacitors C_{GS}, C_{GD}, C_{diode} that are dominant when determining the dynamic behavior. The applied external voltages gives rise to charge accumulations in e.g. the channel region and space charge region within the semiconductor; hence the representation as capacitors.

All external connectors have a resistance (R_S, R_D and R_G) that represent the ohmic losses in each terminal. In addition to the resistance in each terminal, a parasitic series inductance, L_G, L_D and L_S, is introduced. The inductance in each terminal (in e.g. bonding wires and package connectors) is not negligible at fast transitions such as a switching event; hence there is a need for a parasitic inductance in the model. The internal bode diode present in the Power MOSFET [5] is represented by a current generator, I_{diode},, that in combination with R_{diode} and C_{diode} forms a *pn*-junction structure based on the model and equations in SPICE® [4].

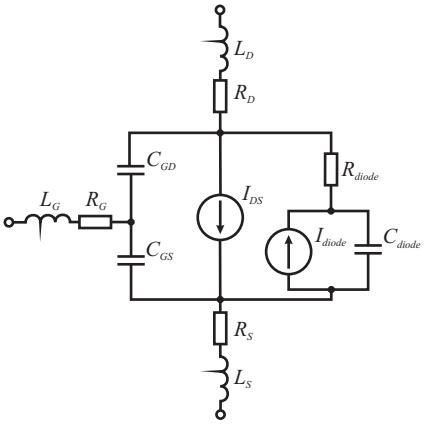

Figure 1. Internal structure of the proposed MOSFET model.

The structure of the proposed model is rather straightforward and similar models have been described in e.g. [6] and [7]. The novelty presented in this article is the thorough characterization of C_{GD} and how it is affected by high current flow. If the datasheet is consulted for capacitance information, the only operating area taken into account is when the MOSFET is turned off (V_{GS}=0V). Measurements show that the capacitance when V_{GS}=0V show some deviations, most likely due to statistic variations and measurements uncertainty, but the most significant difference is seen when V_{GS} is increased. The reverse transfer capacitance (also known as gate-drain capacitance) which is the most crucial component for correct switching behavior shows a significant increase as V_{GS} increases. This statement is verified in [8, 9, 10] where the gate-drain capacitance (C_{GD}) is characterized as a function of both V_{GS} and V_{DS}. This is an important property since the area of application for this model is switching circuits where the MOSFET will operate in saturated, active and turned off regions.

The circuit contains six energy storing elements whose voltage or current are selected to form the state matrix

$$x(t) = \begin{bmatrix} v_{CGS} \\ v_{CGD} \\ v_{Cdiode} \\ i_G \\ i_D \\ i_S \end{bmatrix} \quad (2)$$

where the current through an inductor or the voltage over a capacitor will constitute a state. In order to implement the proposed MOSFET model in Matlab®/Simulink®, nodal analysis in combination with voltage loop analysis is used to form equations for the state derivatives. For a functional circuit, the MOSFET model is implemented in a circuit together with appropriate external elements to form a switching circuit with a purely resistive load. The inputs ($u(t)$) and the outputs ($y(t)$) of the system are selected in an appropriate way to form a state-space model of the total system.

III. Parameter Extraction

To be able to simulate the performance of the component, parameter extraction needs to be performed. The procedure suggested here is based on three different sources of information; datasheets provided by the manufacturer, SPICE® models provided by the manufacturer and component measurements. The main idea is to keep the procedure as simple as possible and to use sources of data that are available for the end-user of the component such as a datasheets, SPICE® models or other sources of information provided by the manufacturer. A flowchart of how the suggested procedure can be performed is found in Fig. 2.

At first, the datasheet is analyzed where the package of the component is specified. The value of the parasitic inductor in each terminal (L_G, L_D and L_S) is not investigated in detail; instead is typical values used in all forthcoming simulations. This inductance is strongly dependent on the package type and

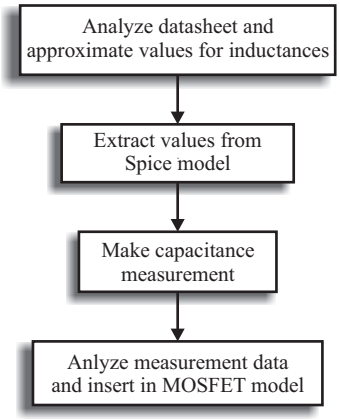

Figure 2. Procedure for extracting model parameters.

can according to [11] and [12] be approximated to 5-15nH for a regular TO-247 package and more than 30nH for larger IGBT power module packages [13]. For all coming simulations where nothing else is specified from the manufacturer, the terminal inductance is set to 5nH since only low power components are considered. In addition to information about inductances, the datasheet also contains information about the voltage dependent capacitors C_{GS}, C_{GD}, and C_{DS}. As described earlier, this information is only valid for one specific operating point and is therefore not suitable for switching applications. However, there is one exception; the gate-source capacitance, C_{GS}. This capacitance can be considered almost constant [5, 14], hence is this value extracted from graphs usually provided in the datasheet.

Once the parasitic inductances and the gate-source capacitance are extracted from the datasheet, the SPICE® model provided by the manufacturer is used for parameter extraction. Since the proposed model uses the same equations to calculate the drain-source current as SPICE®, the parameters found in the manufacturer SPICE® model can be reused. Also, data for the parasitic body diode and terminal resistances can usually be found in the manufacturer SPICE® model. The main difference between the SPICE® model and the proposed MOSFET model is the voltage dependent capacitor C_{GD}. The data for this capacitor needs to be measured by an impedance analyzer. Once the measurements are done, data is extracted in order to make the gate-drain capacitance dependent on both gate-source and drain-source voltage, C_{GD} (v_{GS}, v_{DS}).

IV. MOSFET Model Under Static Conditions.

To test the parameter extraction procedure, the HEXFET® power MOSFET IRF520N from International Rectifier Inc. was chosen for verification. The static behavior is verified using the output characteristics from the datasheet. The output characteristics correspond quite well both for the SPICE® model and the proposed model, see Fig. 3 where simulation results from the proposed model are presented. The results from both models correspond to each other since they are based on the same equations and use the same input data taken from the SPICE® model provided by the manufacturer.

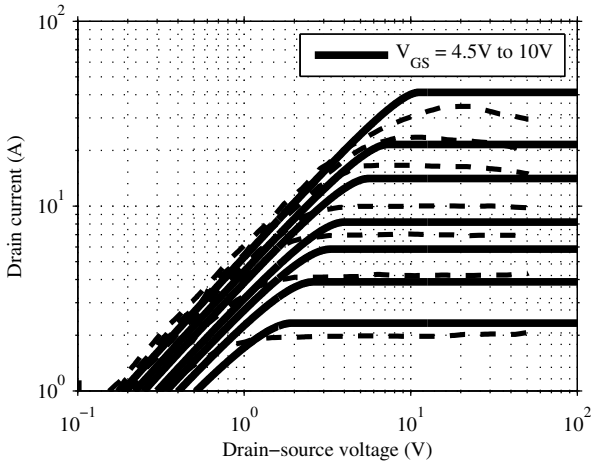

Figure 3. IRF520N output characteristics, comparison between proposed MOSFET model (solid line) and datasheet (dashed line).

However, if measurements of a real component are considered, it is clearly seen that that the output characteristics deviates significantly from the datasheet values, see Fig. 4. This has mainly to do with two issues; the chip temperature

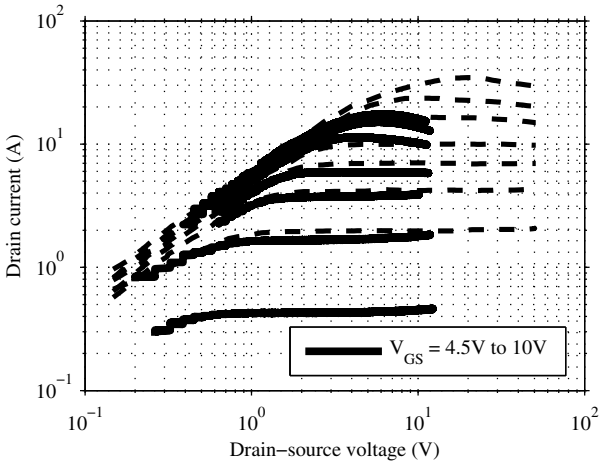

Figure 4. IRF520N output characteristics, comparison between measurements (solid line) and datasheet (dashed line).

and the threshold level of the component. The difference in threshold level can on component level be deduced to variation in process parameters such as oxide thickness and doping concentration. Beyond the manufacturing variations, the threshold level also shows a dependence on the chip temperature. The total mechanism of how the threshold voltage varies is complicated and is out of scope for this application; it is important to determine how the variations influence the system in which the component comprises.

The conclusion drawn from these simulations is that the output characteristics are strongly dependent on the individual component. According to the datasheet, the span in which the threshold voltage can vary is rather large. For the selected MOSFET (IRF520N) the threshold voltage may vary between V_{th}=2V and V_{th}=4V. The component selected for this investigation had a slightly higher threshold voltage ($V_{th} \approx$ 3.6V) than the typical value ($V_{th} \approx$ 2.79V) specified in the datasheet. This deviation does not influence the switching behavior in a significant way since the dynamic event is dominated by the capacitive and inductive parts of the component. .

V. MOSFET model Under Dynamic Conditions.

To describe the total switching characteristics, the capacitors in the model must be given a characteristic that makes them nonlinearly voltage dependent. When consulting the datasheet it only presents the internal capacitances, (C_{GS}, C_{GD} and C_{DS}), as a function of the applied voltage for one operating point (usually named *Ciss*, *Coss* and *Crss* that refers to the input capacitance, output capacitance and reverse transfer capacitance respectively) [15, 16]. If a positive gate-source voltage is applied a depletion layer followed by an inversion layer will be formed. These accumulations of charges within the semiconductor changes the capacitance

characteristics see Fig. 5 where the gate-drain capacitance (also known as *Crss*) is plotted as a function of V_{DS} for three different gate-source voltages.

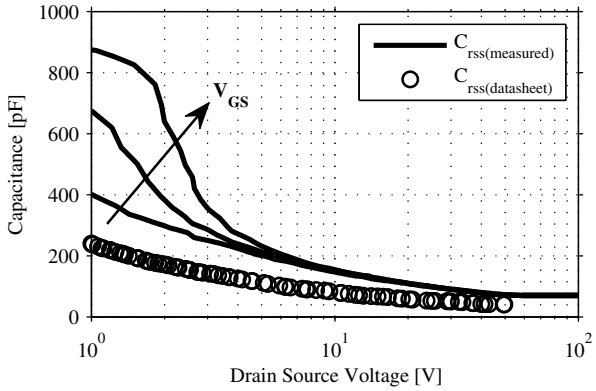

Figure 5. Reverse transfer capacitance (*Crss*) as a function of applied drain-source voltage. V_{GS} is varied from 0V to 2V.

By performing thorough measurements with an impedance analyzer (HP4395) it is concluded that the value of the gate-drain capacitance can be depicted according to Fig. 6 and Fig. 7 where the gate-drain capacitance is shown as a function of applied gate-source and drain-source voltages for the power MOSFET IRF520N. Note that the value of the gate-drain capacitance to some extent is based on extrapolations of measurement data due to lack of voltage handling capacity of the impedance analyzer.

If the switching event is analyzed in detail, the operating points found during the course of events can be plotted in the same graph as the gate-drain capacitance, see Fig. 6 for a turn-on event and Fig. 7 for a turn-off event.

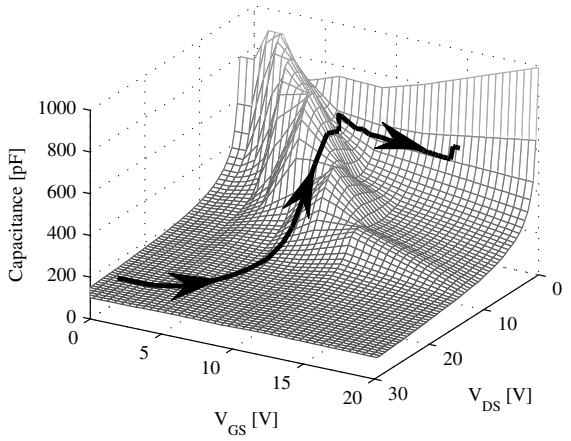

Figure 6. Gate-drain capacitance (C_{GD}) as a function of applied drain-source (V_{DS}) and gate-source (V_{GS}) voltages. Turn-on event marked as a line.

As mentioned in the previous section, the gate-source capacitance can be considered almost independent of the gate-source bias voltage [4] since it mainly consists of the parallel plate capacitor formed by the gate electrode, the substrate and the gate-oxide as a dielectric in between. Since the proposed model only deals with positive voltages on the gate terminal the terminal, the gate-source capacitance value is chosen to be extracted from the datasheet.

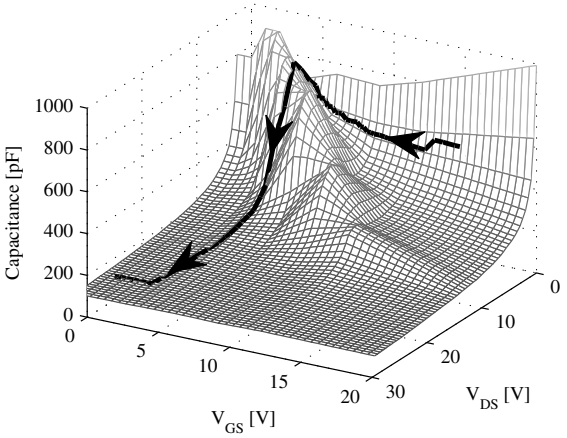

Figure 7. Gate-drain capacitance (C_{GD}) as a function of applied drain-source (V_{DS}) and gate-source (V_{GS}) voltages. Turn-off event marked as a line.

The last element that needs to be determined is the drain-source capacitor. This capacitor is determined by the size of the junction area between *p*-type well and the *n*-type substrate layer which has the same electric potential as the source. This capacitor shows similar behavior as the capacitance in a *pn*-junction diode; therefore it is found suitable to obtain the *cv*-characteristics from the SPICE® model where a body diode is incorporated. The equations governing the body diode junction capacitance are classical SPICE® equations described in e.g. [4]. The parameter values in these equations are taken from the SPICE® model delivered by the manufacturer.

VI. Simulation Results

In order to verify the validity of the proposed MOSFET model, results from simulations are compared with measurements. It is thereby concluded that the black-box SPICE® model provided by the manufacturer shows a switching behavior that corresponds rather well with measurements, see Fig. 8 and Fig. 9.

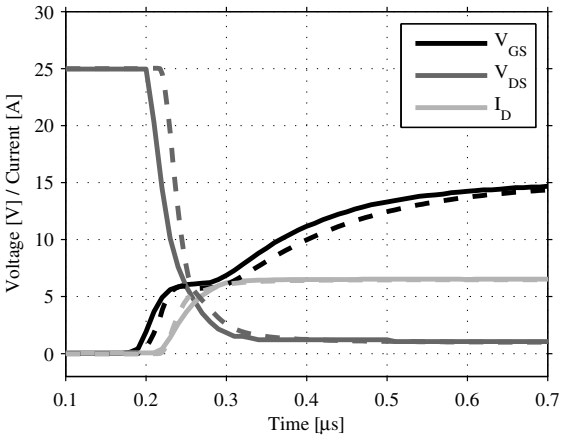

Figure 8. Switching circuit with IRF520N and purely resistive load (R_{gate} = 110Ω, R_{load} = 3.7Ω, V_{bat}=25V, V_{gate} =15V). Measurements: solid line. SPICE model: dashed line.

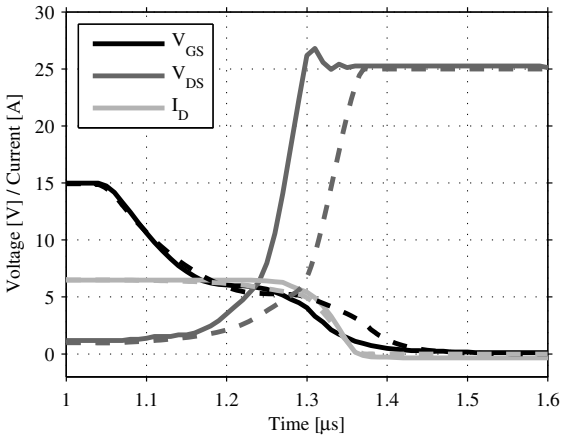

Figure 9. Switching circuit with IRF520N and purely resistive load (R_{gate} = 110Ω, R_{load} = 3.7Ω, V_{bat}=25V, V_{gate} =15V). Measurements: solid line. SPICE model: dashed line.

The most noticeable difference is seen during the turn-off event. As the gate-source voltage reaches the miller-region and levels out, the drain-source voltage starts to fall. In the measurement, this event takes shorter time which most likely is caused by a difference in the gate-drain capacitance as the MOSFET turns off.

Fig. 10 and Fig. 11 show a comparison between measurements and simulations with the proposed MOSFET model. The conclusion drawn from the measurements is that the internal capacitances, mostly C_{GD}, are of great importance when it comes to characterizing the MOSFET model. The proposed model is valid for the entire operating range of the component which makes it suitable for switching applications where a detailed characterization of the switching event is needed, e.g. when predicting the EMI performance.

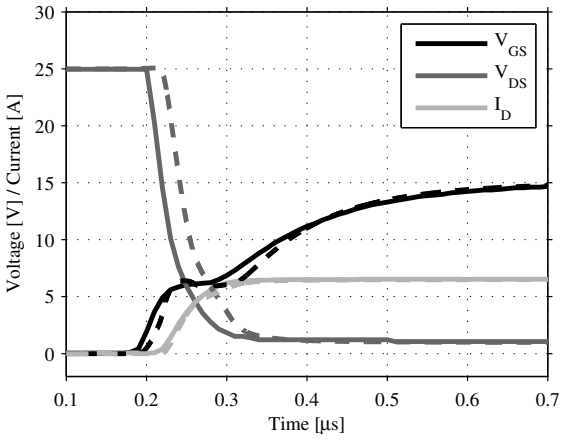

Figure 10. Switching circuit with IRF520N and purely resistive load (R_{gate} = 110Ω, R_{load} = 3.7Ω, V_{bat}=25V, V_{gate} =15V). Measurements: solid line. Proposed MOSFET model: dashed line.

VII. CONCLUSIONS

The conclusion drawn from the measurements is that the internal capacitances, mostly the gate-drain capacitance, is of great importance when it comes to characterizing a MOSFET model adapted for a switching event. The behavior of the proposed model corresponds well both to the SPICE® black-box model and laboratory measurements. The proposed model is valid for the entire operating range of the component thanks to the thorough characterization of C_{GD}. This in combination with the fact that the model can be used for deriving a suitable controller makes it suitable for analyzing switching applications and e.g. predicting EMI performance.

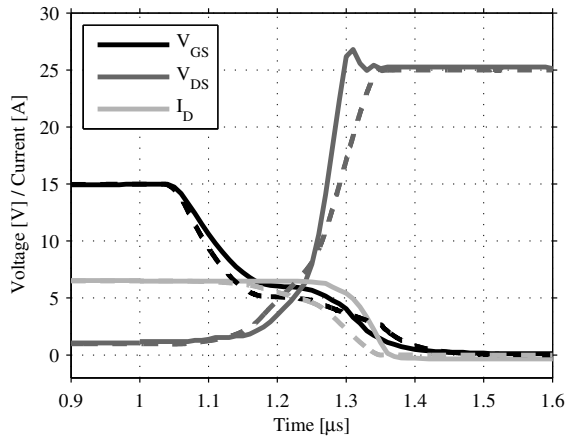

Figure 11. Switching circuit with IRF520N and purely resistive load (R_{gate} = 110Ω, R_{load} = 3.7Ω, V_{bat}=25V, V_{gate} =15V). Measurements: solid line. Proposed MOSFET model: dashed line.

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