Chapter 2
Model Level 0: Switching Behavior of Power MOSFETs

This chapter describes the model level 0 introduced in the previous chapter. One main goal is to provide the reader with sufficient knowledge on the adopted modeling approach, characteristics, basic structure, advantages, and drawbacks of its use and associated analysis methods.

Within the scope of the investigations, the chapter includes simulation results corresponding to state-of-the-art SRBCs for VRs, which are compared to extensive experimental data. The validation assesses the accuracy of the model to reproduce switching waveforms and estimate power losses.

The purposes of the model are thus to accurately represent the behavior of the power MOSFETs in the switched converter, understand fast switching phenomena, identify mechanisms of power losses, and quantify their effects. To meet all these requirements, model level 0 is based around an accurate behavioral model of power MOSFETs.

Furthermore, those circuit components of the switched converter that may potentially influence the operation of the power switches are properly modeled according to the analysis demands. The model description of these circuit elements is provided in the different sections of the chapter.

For its complexity and relevant importance in the converter circuit though, most of the chapter is devoted to the modeling of the power MOSFETs. The proposed MOSFET model consists of a proper combination of individually identified device interterminal elements,[1] such as the capacitances, channel and body diode, each of which are characterized and represented by means of lumped elements. The superposition of the electrical effects produced by these elements effectively reproduces the behavior at the terminals of the device. One of the benefits of this implementation is that it provides consistent simulations of the MOSFETs internal operation corresponding to each of the extracted device characteristics. Such ability aids the purpose of elucidating switching phenomena and their impact on the converter performance.

Besides the basic structure, composition and adopted approach, the description of the converter components includes the derivation of model parameters, which

[1] All circuit elements considered herein are assumed time invariant, unless otherwise specified.

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result from experimental characterization and, alternatively, accurate device physics simulations. Both methods will be briefly outlined and their use compared and justified for each particular case.

The resulting converter model combines power switches, gate drivers, input/output filters and layout parasitic elements to form a complex lumped network structure that may be solved with circuit simulators such as SPICE. In addition to the power circuit, a PWM control and gate drive logic with dead time adjustments are implemented in the simulator to enable switching synchronization and power balance control. The control module further incorporates an algorithm for the estimation of initial values of the state variables so as to simulate switching cycles in steady-state conditions. This allows skipping the transient time of a usually large number of switching periods, which in turn significantly reduces simulation times.

The analysis of simulated waveforms will not only be the basis to understand fast switching operation but also to identify and quantify associated loss mechanisms. Special emphasis is given to a proposed systematic procedure to perform the loss breakdown by separation of loss components. Although the losses not related to the power MOSFETs are not addressed in detail, the results of the loss extraction yield quantities associated to several identified loss mechanisms which happen to be critical to identify key parameters influencing the performance of the overall converter.

The proposed loss breakdown and analysis methods will be illustrated with various case examples that demonstrate the benefits of the approach to help investigate switching phenomena, identify major loss contributors, and propose measures to improve converter performance.

2.1 Power MOSFET Model for Circuit Simulations

Given the need to effectively combine device behavior and circuit analysis in one single simulation environment, the goal is to develop an accurate power MOSFET model for circuit simulators that features device analysis capabilities. As highlighted in Chap. 1, empirical models appear to be the right choice for this purpose as they offer a proper balance trade-off between required computation power and simulation accuracy, which cannot be met with device physics simulations in mixed mode.

Thus, the following is a description of an adopted behavioral modeling approach. The proposed model aims at reproducing the device behavior at its terminals by proper combination of individual device characteristics. By means of the right testing conditions, such characteristics can be derived from experimental measurements resulting in DC output characteristics in first and third quadrant, avalanche breakdown (ABD), capacitances, gate resistance, package impedances, and body diode reverse recovery (RR). Numerical device simulation is principally an alternative method to obtain one or more of these characteristics by means of rather simple simulation setups, as it shall be shown later on. Once available, the data may be represented in terms of look-up tables, fitting functions, and differential

equations. These can then be combined in a simulation model that reproduces the actual device behavior at its terminals, to which the original testing conditions have been applied. The resulting empirical model is meant for circuit simulators like SPICE in order to cope with rather complex circuit environments.

The accuracy of the loss predictions of the complete circuit and individual loss contributors is determined by the employed characteristics and can be tailored to the analysis demands. In this regard, both characterization methods (i.e., measurements and device physics simulations) play different roles. Within experimental limits, measurements allow validating device simulations. The latter in turn is not only useful to replace cumbersome measurements; it also enables to cover characterization ranges that go beyond experimental limits and hence to complete the desired characteristics. In cases where no experimental data are available, like for instance in the process development of a novel technology, device physics simulations may be the only means to generate accurate characterization data.

The following sections outline implementation issues of the behavioral model, describe methods for comprehensive device characterization, which is the crucial part of the approach, and explain analysis opportunities by means of simulation examples.

2.1.1 Model Structure and Implementation

The dynamic behavior of the power MOSFET may be represented with the lumped network structure of Fig. 2.1. Note that, for simplicity, all parasitic lumped elements associated to the package, substrate, and polysilicon gate are at this point omitted. As shown in the circuit diagram, three current sources are parallel connected to individually model the channel, body diode, and ABD current contributions. These are i_{cn}, i_{dio}, and i_{AB}, respectively. Added to these current paths, the model further considers the three equivalent parasitic terminal capacitances of the MOSFET, namely C_{GS}, C_{GD}, and C_{DS}. In order to properly represent the behavior of each individual characteristic, the elements of the model may be dependent on interelectrode voltages v_{DS} and v_{GS}. In particular, diode current i_{dio} may additionally

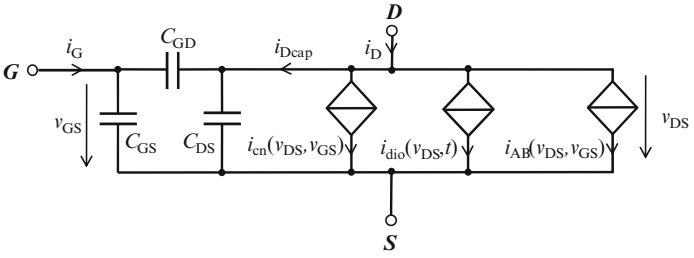

Fig. 2.1 Circuit diagram of the power MOSFET model for circuit simulations. For simplicity, package-related parasitic elements and gate and substrate resistances are omitted

be time dependent so as to represent the dynamics of RR, as it shall be described in detail later.

Establishing appropriate criteria to de-embed the terminal currents into the defined current contributions is a primary aspect of the modeling approach. This is extensively discussed in the next section in the context of model parameter extraction. This section focuses on the model implementation in circuit simulators.

Regarding DC output characteristics, the channel current is defined in both first and third quadrants, i.e., both directions of drain current flow. The channel behavior considerably varies in each quadrant, for which different empirical functions are utilized. In the first quadrant it follows that,

$$i_{q1}(v_{\mathrm{DS}}, v_{\mathrm{GS}}) = A_{\mathrm{die}} \cdot c_0(v_{\mathrm{GS}}) \cdot \left[\begin{array}{l} \tanh\left(\dfrac{\mathrm{v_{DS}} \cdot \mathrm{c_2(v_{GS})}}{1 + \mathrm{v_{DS}} \cdot \mathrm{e}^{\mathrm{c_1(v_{GS})}}} \right) + \cdots \\ \quad + v_{\mathrm{DS}} \cdot c_3(v_{\mathrm{GS}}) + c_4(v_{\mathrm{GS}}) \cdot (\mathrm{e}^{\kappa_{\mathrm{e}} \cdot v_{\mathrm{DS}}} - 1) \end{array} \right]. \quad (2.1)$$

Coefficients c_0–c_4 are dependent on v_{GS}. Together with constant κ_{e}, these coefficients are determined from fitting procedures of the original MOSFET characteristics. The resulting relations with v_{GS} are implemented with look-up tables. Parameter A_{die} is the effective active chip area of the power device, which is introduced in the equation to enable die area scaling. This feature will be extended throughout the rest of the model components and frequently employed in subsequent analysis.

Third quadrant operation is highly influenced by the so-called body-effect, which describes the changes in the threshold voltage as function of a negative v_{DS} [1]. The analysis of this effect in high-density trench power MOSFETs is provided in Appendices A and B.

An empirical equation that reproduces the channel DC behavior under the influence of the body-effect is as follows:

$$i_{q3}(v_{\mathrm{DS}}, v_{\mathrm{GS}}) = A_{\mathrm{die}} \cdot v_{\mathrm{DS}} \cdot \mathrm{e}^{c_7(v_{\mathrm{GS}})} \cdot [1 - \tanh(c_5(v_{\mathrm{GS}}) \cdot (v_{\mathrm{DS}} - c_6(v_{\mathrm{GS}})))]. \quad (2.2)$$

Similar to (2.1), c_5–c_7 correspond to fitting coefficients. Expressions (2.1) and (2.2) fully describe the DC characteristics of the channel. Combining them yields the expression for the channel current

$$i_{\mathrm{cn}}(v_{\mathrm{DS}}, v_{\mathrm{GS}}) = i_{q1}(v_{\mathrm{DS}}, v_{\mathrm{GS}}) \cdot \max(v_{\mathrm{DS}}, 0) + i_{q3}(v_{\mathrm{DS}}, v_{\mathrm{GS}}) \cdot \min(v_{\mathrm{DS}}, 0). \quad (2.3)$$

Note that functions max and min restricts the use of the functions to their respective boundary limits.

Besides the channel current, the third quadrant DC output characteristics are further composed by the body diode current. Its DC component is assumed to be uniquely dependent on v_{DS} since the drain current dependence on the gate voltage

is entirely attributed to the channel. This is justified in the Appendices A and B by means of extensive simulations and experimental analysis. Thus, in DC operation it follows that

$$i_{\text{dio\_dc}}(v_{\text{DS}}) = i_{\text{dio}}(v_{\text{DS}}, t \to \infty). \tag{2.4}$$

The right-hand side of (2.4) represents the body diode's response to a step function. The implementation of the DC diode current is based on (2.2) at a given gate voltage, that is,

$$i_{\text{dio\_dc}}(v_{\text{DS}}) = i_{q3}(v_{\text{DS}}, V_{\text{GSd}}), \tag{2.5}$$

where V_{GSd} is usually well below zero. As it shall be illustrated later in this chapter, condition $V_{\text{GSd}} \leq -5V$ is sufficient in the devices characterized so far.

Similarly, the ABD is implemented by a diode function in the first quadrant as follows:

$$i_{\text{AB}}(v_{\text{DS}}, v_{\text{GS}}) = -i_{\text{dio\_dc}}(\min(-v_{\text{DS}} + V_{\text{AB0}} - \kappa_{\text{AB}} \cdot v_{\text{GS}}, 0)). \tag{2.6}$$

Constants V_{AB0} and κ_{AB} allow adjusting the avalanche voltage level as well as its dependence on v_{GS}.

In the next section, the use of (2.1)–(2.6) will be illustrated to fit the characteristics of a particular MOSFET technology. The equations are suitable for most of the vertical MOSFET structures studied thus far. However, certain device technologies may involve the definition of alternative empirical functions.

The latter is also the case for the dynamic model of the body diode, which is defined as an extension of its DC characteristics by means of the following integral equation

$$i_{\text{dio}}(v_{\text{DS}}, t) = \beta_{\text{rr}} \cdot i_{\text{dio\_dc}}(v_{\text{DS}}) + \frac{1}{t_{\beta\text{rr}}} \int_0^t (i_{\text{dio\_dc}}(v_{\text{DS}}) - i_{\text{dio}}(v_{\text{DS}}, t))\, \mathrm{d}t + I_{\text{dio0}}. \tag{2.7}$$

Empirical equation (2.7) compactly represents the dynamics of RR, which may be adjusted by parameters β_{rr} and $t_{\beta\text{rr}}$. The empirical model is an adaptation of the simple diode model from Lauritzen [2]. A detailed description of the model performance and comparison to other implementation approaches are provided in Appendix C. Note that forward recovery is neglected since it has not been observed in the studied low-voltage devices.

The diode capacitance is implicitly described by the model element C_{DS}. The implementation of this and the other nonlinear capacitances in circuit simulators is generally nontrivial as it frequently involves a rather complex custom design by means of basic built-in functions and components. The realization method of interest is that one which best compromises simulation accuracy, speed, and

convergence. Nonetheless, one of the most common approaches is the use of equivalent voltage controlled current sources, as described in [3, 4]. In such configuration, the interconnection of nodes D–S and G–S is established solely by variable current sources, which may be linked to look-up tables[2] and interpolation functions to define the voltage-dependent capacitances. Consequently, any series connection of inductances to these nodes is potentially susceptible to generate convergence problems because the piece-wise approximations yield time-discontinuous derivatives of the drain and gate currents.

In this regard, a more topologically stable configuration implies the use of current-controlled voltage sources for the capacitance implementation. To achieve this, the capacitance network from the model of Fig. 2.1 needs to be transformed to an alternative equivalent circuit. Let the capacitance currents of the MOSFET be expressed in vector form as follows:

$$\begin{pmatrix} i_{\mathrm{G}} \\ i_{\mathrm{Dcap}} \end{pmatrix} = C \cdot \begin{pmatrix} \frac{\mathrm{d}v_{\mathrm{GS}}}{\mathrm{d}t} \\ \frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t} \end{pmatrix}, \tag{2.8}$$

where,

$$\boldsymbol{C} = \boldsymbol{C}(v_{\mathrm{GS}}, v_{\mathrm{DS}}) = \begin{pmatrix} C_{\mathrm{iss}} & -C_{\mathrm{rrs}} \\ -C'_{\mathrm{rss}} & C_{\mathrm{oss}} \end{pmatrix}, \tag{2.9}$$

$$C_{\mathrm{iss}} = C_{\mathrm{iss}}(v_{\mathrm{GS}}, v_{\mathrm{DS}}) = C_{\mathrm{GS}}(v_{\mathrm{GS}}, v_{\mathrm{DS}}) + C_{\mathrm{GD}}(v_{\mathrm{GS}}, v_{\mathrm{DS}}), \tag{2.10}$$

$$C_{\mathrm{oss}} = C_{\mathrm{oss}}(v_{\mathrm{GS}}, v_{\mathrm{DS}}) = C_{\mathrm{GD}}(v_{\mathrm{GS}}, v_{\mathrm{DS}}) + C_{\mathrm{DS}}(v_{\mathrm{GS}}, v_{\mathrm{DS}}), \tag{2.11}$$

$$C_{\mathrm{rss}} = C_{\mathrm{GD}}, \tag{2.12}$$

$$C'_{\mathrm{rss}} \cong C_{\mathrm{rss}}. \tag{2.13}$$

The latter expresses the reciprocity property [5] of the capacitance matrix from (2.9), which has been observed in all devices analyzed thus far.

The capacitances may be conveniently specified in terms of relative values as follows:

$$\begin{pmatrix} C_{\mathrm{GS}} \\ C_{\mathrm{GD}} \\ C_{\mathrm{DS}} \end{pmatrix} = A_{\mathrm{die}} \cdot \begin{pmatrix} C_{\mathrm{GSsp}} \\ C_{\mathrm{GDsp}} \\ C_{\mathrm{DSsp}} \end{pmatrix}. \tag{2.14}$$

[2]Unlike in the case of the channel and body diode, look-up tables are employed for the full representation of the capacitances since no suitable empirical function was found. Generally, simple fitting functions are preferred over look-up tables for better scaling capabilities, compactness, and computation speed, particularly when multivariable dependencies need to be implemented and high accuracy is required.

The vector to the right of (2.14) contains specific capacitance values given in Farads per unit area.

The implementation of the nonlinear capacitances as voltage sources implies expressing (2.8) in integral form, that is,

$$\begin{pmatrix} v_{GS} \\ v_{DS} \end{pmatrix} = \int_0^t C^{-1} \cdot \begin{pmatrix} i_G \\ i_{Dcap} \end{pmatrix} \cdot dt + \begin{pmatrix} V_{GS0} \\ V_{DS0} \end{pmatrix}, \tag{2.15}$$

where V_{GS0} and V_{DS0} are the initial conditions of state variables v_{GS} and v_{DS}.

Based on the above transformation, the general model of Fig. 2.1 may be equivalently represented as shown in Fig. 2.2. This structure differs from the previously exposed in that the MOSFET capacitances are implemented by means of two current-dependent voltage sources, which offers three major advantages. First, current discontinuities through the terminals of the structure can no longer occur due to the integral form of the impressed voltage across terminals D–S and G–S. Second, initial conditions can be readily defined, which contrasts with the implementation based on current sources. And third, implementation is simplified since only two voltage sources are required to represent three capacitances.

The proposed implementation can be further simplified by just combining terms and expressing capacitive current i_{Dcap} as follows:

$$i_{Dcap}(v_{DS}, v_{GS}, t) = i_D - i_{Dnc}(v_{DS}, v_{GS}, t), \tag{2.16}$$

where i_{Dnc} defines the noncapacitive term of the drain current, that is,

$$i_{Dnc}(v_{DS}, v_{GS}, t) = i_{cn}(v_{DS}, v_{GS}) + i_{dio}(v_{DS}, t) + i_{AB}(v_{DS}, v_{GS}). \tag{2.17}$$

Thus, Fig. 2.3 shows the resulting simplified power MOSFET model structure composed by just two dependent voltage sources governed by (2.1)–(2.17). The model can be readily implemented in circuit simulators such as PSpice, which allows the declaration of all required nonlinear functions, integral operations, and use of 2D look-up tables for the definition of the voltage-dependent capacitances.

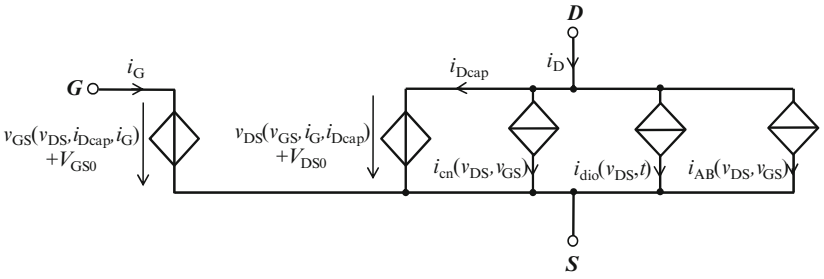

Fig. 2.2 Model of Fig. 2.1 with nonlinear capacitances represented as voltage-dependent sources

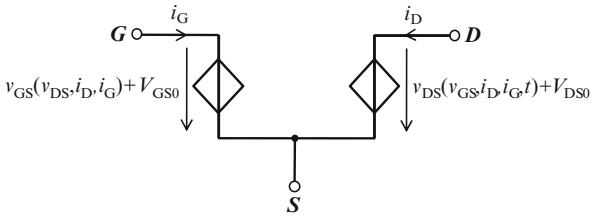

Fig. 2.3 Simplified circuit implementation of proposed power MOSFET model for circuit simulations

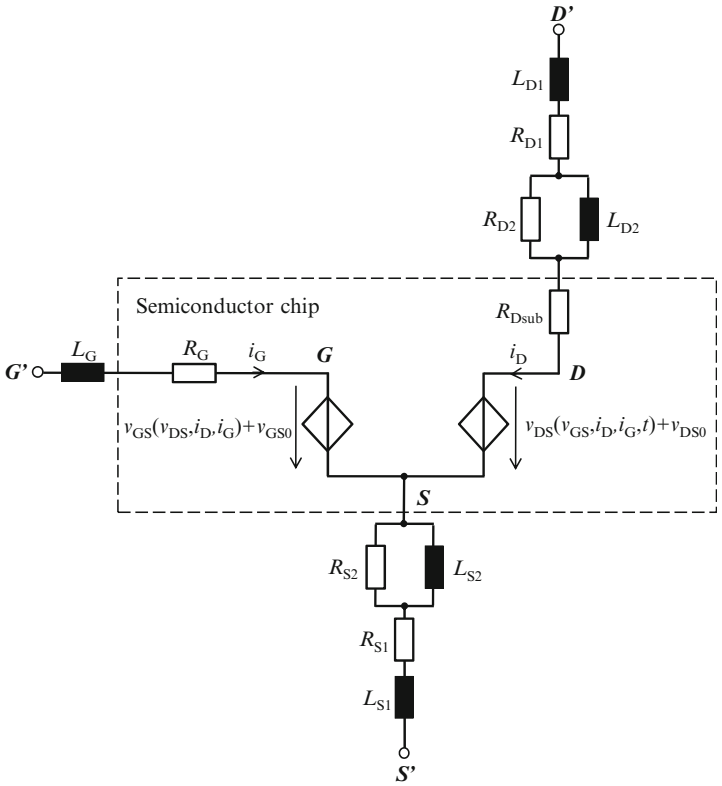

Fig. 2.4 Proposed power MOSFET model for circuit simulations, including package parasitic elements, and both gate and substrate resistances

The complete dynamic power MOSFET model including all parasitic resistances and inductances from chip and package is depicted in Fig. 2.4. The highlighted area corresponds to the portion of the semiconductor chip, which includes substrate resistance R_{Dsub} and polysilicon gate resistance R_G in addition to the elements considered in Fig. 2.1. While substrate resistance R_{Dsub} may scale with A_{die}, gate resistance R_G strongly depends on the gate busbar layout design, as it shall be seen later in this section.

The rest of the model representation corresponds to the package and electrode equivalent parasitic elements. Therefore, electrodes labeled as G', D', and S' correspond to the terminals of the MOSFET package. The network formed by elements L_{D2}, R_{D2} and L_{S2}, R_{S2} represents the skin losses and proximity effects of the package interconnections, e.g., bond wires. At high-switching frequency, package loss dissipation due to these magnetic effects may be substantial, and thus need to be considered. In the gate terminal, such effects are frequently neglected since the polysilicon gate resistance dominates.

2.1.2 Model Data Acquisition

Although the required model data may be obtained either by measurements or by device physics simulations, there are differences in the ranges that can be covered with the two approaches. Table 2.1 summarizes the required characteristics and methods for their acquisition. The resolution and extension of the gathered data may be adapted to the modeling needs which, for the present purpose, go far beyond the information usually contained in datasheets.

The characterization techniques may involve postprocessing algorithms to ultimately subtract the model parameters from the raw data (see (2.1)–(2.17)). The extraction procedures of each device characteristic are described in the following subsections.

2.1.2.1 Gate Resistance and Package Impedances

Parasitic inductances of device package and polysilicon gate resistance are experimentally derived from scattering parameters (or S-parameters) measurements, which describe the electrical behavior of impedance networks when undergoing various steady-state stimuli by small signals. Assuming an equivalent impedance network at the terminals of the MOSFET, the measured S-parameters can be processed to

Table 2.1 MOSFET device characterization by measurements and device physics simulations

MOSFET characteristics	Measurements	Device physics simulations
Gate resistance Package impedances	S-parameter extraction with vector network analyzer	N/A[a]
DC output characteristics (channel, body diode, ABD, and substrate resistance)	Curve tracer based on voltage ramps or voltage pulses	DC parameter sweep simulations
Interelectrode capacitances	Impedance analyzer measurements for $V_{GS} < V_{TH}$ Measurement of currents resulting from applied voltage ramps	Transient simulations of current response to applied voltage ramps
Body diode RR	Half-bridge in clamped inductive switching mode	Transient simulations of resistive or inductive turn-off

[a]device physics simulations are presented in Appendix E to estimate package impedances

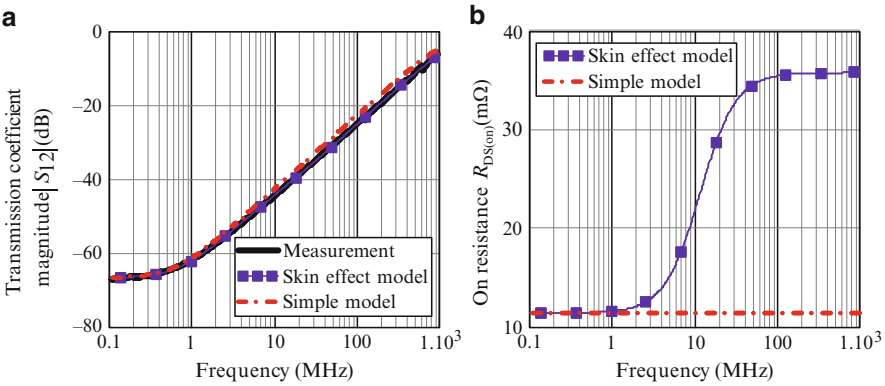

Fig. 2.5 (a) Drain-source transmission coefficient magnitude of a MOSFET in on-conduction, (b) extracted on resistance. Experiment performed at $v_{GS} = 6$ V. Measurement and fitting results. DUT: PHD77NQ03T from NXP Semiconductors (DPak encapsulation). Fitting results refer to model of Fig. 2.6: $L_1 = 2.13$ nH, $R_1 = 11$ mΩ, $L_2 = 0.33$ nH, $R_2 = 24$ mΩ

quantitatively determine the elements constituting such a network under different bias conditions.

S-parameter measurements are performed with *a vector network analyzer* (VNA). The principle of operation of VNAs enables to effectively measure the terminal impedance of the device under test (DUT) without the influence of interconnection parasitic impedances. With a well-calibrated setup, the VNA allows characterization of low impedance packages at frequencies of interest, which may extend into the GHz range. Proper interconnections of the DUT to the VNA are essential to achieve consistent measurements at high frequency. The setup employs RF cables to connect the VNA ports to a test fixture for coplanar microstrip lines, to which the DUT is suitably attached.

Figure 2.5a illustrates the magnitude of the transmission coefficient corresponding to the terminal drain–source impedance of an ON state power MOSFET mounted on DPak. The transmission coefficient of the series R–L lumped structure (i.e., referred to as "simple model" in Fig. 2.5) cannot finely match the experimental results due to the presence of skin effects at the package terminals, which translate into an effective inductance reduction as frequency increases. The lumped skin effect model of Fig. 2.6 allows a simple and yet more accurate representation of the measured response, as Fig. 2.5a illustrates[3] [6, 7]. A look at the real part of the estimated impedance reveals the strong resistance dependency on frequency, which clearly manifests already in the MHz range, as Fig. 2.5b depicts. The curve

[3]The phase of the impedance is not considered for parameter fitting since the distributed nature of the underlying skin effect cannot be accurately represented with the proposed models. A far more complex ladder network may be required for that purpose. The simple lumped-based skin effect model aims at representing the fundamentals of such magnetic phenomena by first-order approximations. Estimations of the loss contribution of this effect will dictate whether the approximations are satisfactory enough or, on the contrary, further model refinements are demanded.

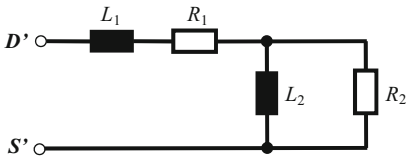

Fig. 2.6 Terminal drain–source equivalent impedance network of a MOSFET in ON conduction considering package skin effect

is characterized by two values, R_1 and R_2, which define the resistance of the network at low and high frequency, respectively. A transition between the two values occurs at intermediate frequencies. The transition interval is given by the inverse time constants R_1/L_1 and R_2/L_2.

The skin effect may be mostly attributed to the source terminal since the drain is contacted through the mounting base, whose equivalent inductance may be negligible.

The results of the characterization suggest limiting the DPak to applications where switching frequencies are well below 1 MHz. At sufficient low switching frequencies, the CtrlFET package loss contribution as a consequence of the output inductor ripple current may be approximately estimated from the following expression,

$$P_{\mathrm{DPak(ac)}}|_{\mathrm{CtrlFET}} \cong (R_2)^{-1} \cdot \left(L_2 \frac{V_{\mathrm{in}} - V_{\mathrm{o}}}{L_{\mathrm{o}}}\right)^2 \cdot \left(\frac{V_{\mathrm{o}}}{V_{\mathrm{in}}}\right). \tag{2.18}$$

According to the proposed skin effect model, the square term in (2.18) equals the voltage across R_2 during the ON state of the CtrlFET when assuming steady-state operation. A similar expression may be deduced for the SyncFET. Given the extracted values of Fig. 2.5, $P_{\mathrm{DPak(ac)}}$ of both devices result in less than 1 mW for typical applications (i.e., down conversion of 12–1 V). Expression (2.18) may no longer be accurate at high-switching frequencies as the ON times approach time constant L_2/R_2. Nonetheless, the simplified skin effect model is helpful to qualitatively represent the increase of ON resistance with the switching frequency.

A far more sophisticated skin effect model may be obtained through the use of FE software tools that enable to numerically solve multidimensional Eddy current problems. Appendix E describes how this is achieved to study the parasitic inductance and dynamic resistance of MOSFETS packages and PCB layouts. A quasi-static formulation of Maxwell's equations can be further developed for the performance estimation of the output inductor, as described in Appendix E.

Figure 2.7 illustrates some of the results derived from FE harmonic analysis, where a MOSFETs package impedance is evaluated in combination with a portion of a PCB track, as representative arrangement from a realistic application. Details of the layout arrangement are provided in Appendix E. The double layer PCB with return ground plane allows to effectively neglect the PCB inductance.

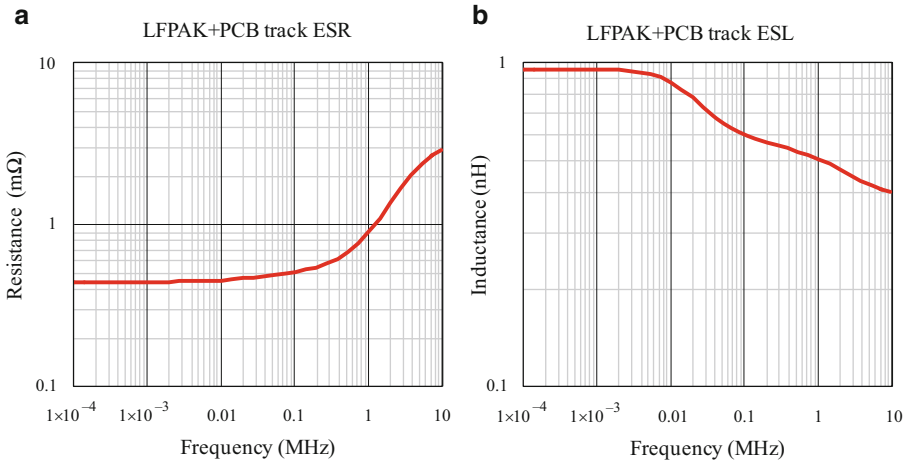

Fig. 2.7 Frequency dependence of the equivalent series resistance (a), and inductance (b) (from drain to source) of the LFPAK plus PCB section with ground plane. Simulation results (see Appendix E for details)

Table 2.2 Measurement extraction of parasitic elements from various MOSFET packages

Package type	Package inductance neglecting skin effects (nH)	
D2Pak	Drain	$L_D = 0$
	Source	$L_S = 5$
	Gate	$L_G = 7$
DPak	Drain	$L_D = 0$
	Source	$L_S = 3.5$
	Gate	$L_G = 4.5$
LFPak	Drain	$L_D = 0$
	Gate	$L_G = 1.1$
	Source	$L_S = 0.5$

As such, the curve from Fig. 2.7b mainly accounts for the MOSFETs ESL corresponding to the package leadframe of the source contact. The extracted value varies around 500 pH in the high-frequency range. The ESR increases rapidly above 200 kHz, reaching five times the DC values at 5 MHz. Unlike the case of the ESL, the ESR contribution of PCB layout cannot be neglected, as shown in Appendix E.

Table 2.2 summarizes the results from VNA measurements of three different power MOSFET packages. To simplify the comparison, skin effects are neglected and so every terminal parasitic inductance can be simply represented with a single lumped inductor. Note that the source inductance of the LFPak matches the simulation results from Fig. 2.7a at 1 MHz.

Besides the extraction of model parameters, S-parameter measurements can further be exploited for device design and failure diagnosis related to manufacturing processes. Effects such as spreading resistance of bounding connections and split

gate [8] can be detected and assessed with no influence of large series parasitic inductances.

A parameter that has an effect on the gate resistance is the gate mask structure, i.e., the gate busbars that distribute the gate current over the area of polysilicon. Figure 2.8 shows some layout examples of possible gate busbar designs. A design criterion for layout optimization may be based on the best compromise between occupied semiconductor area and uniform current distribution. Regarding the later, S-parameter measurements may be used to determine whether or not a design is adequate for current distribution by analyzing the transmission coefficients. Ideally, in case of a uniform current density all cells switch simultaneously. This should be translated into a frequency response equivalent to a simple series R–L–C network, as shown in the example of Fig. 2.9 for the case of an optimum gate busbar design. Note that the value at the resonant frequency yields the gate resistance of the device.

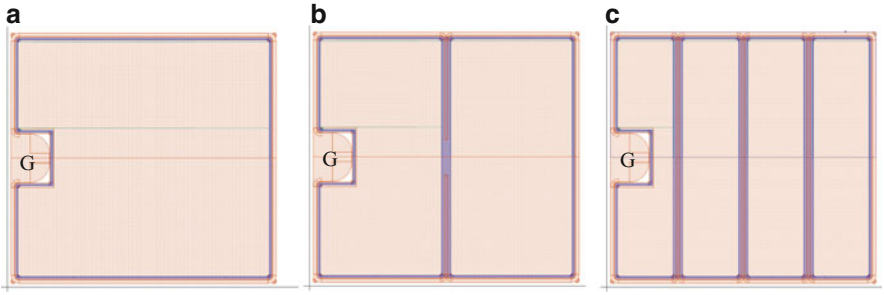

Fig. 2.8 Example of different gate mask structures; (**a**) metal contact along the chip periphery only, (**b**) with one additional center busbar, (**c**) with three additional uniformly distributed parallel busbars

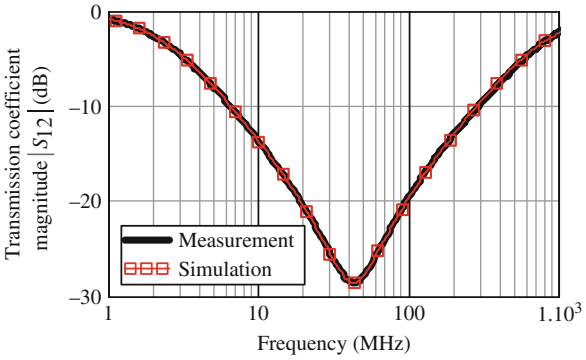

Fig. 2.9 Magnitude of the transmission coefficients of an optimized gate mask layout. Gate-drain terminal measurement and fitting results. The following parameters correspond to a series R–L–C network: $L = 5.18$ nH, $R = 0.97\ \Omega$, $C = 2.76$ nF

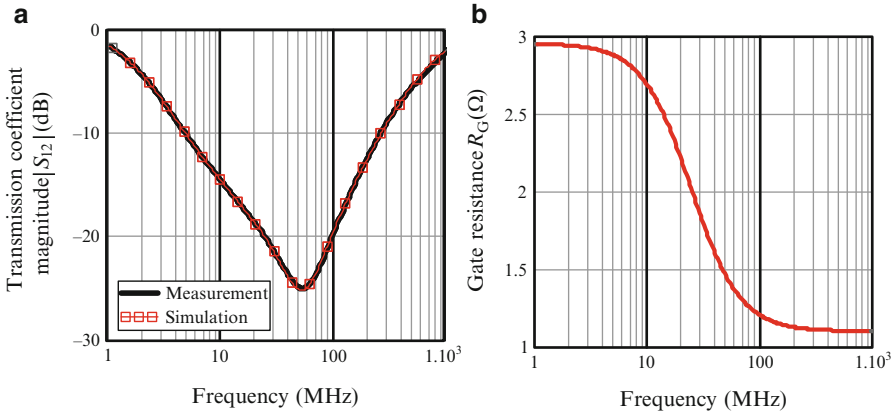

Fig. 2.10 (a) Gate-drain transmission coefficient magnitude of a MOSFET with nonoptimized gate mask. (b) Extracted gate resistance. Terminal gate-drain measurement and fitting results. The following parameters refer to model of Fig. 2.11: $L_1 = 5.18$ nH, $R_1 = 1.1\ \Omega$, $R_2 = 6.85\ \Omega$, $C_1 = 1.8$ nF, $C_2 = 1.95$ nF

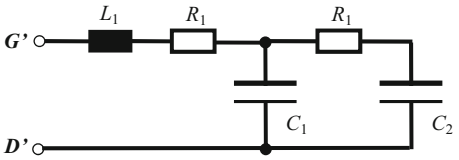

Fig. 2.11 Terminal gate-drain impedance equivalent network corresponding to a MOSFET with split gate effect, as illustrated in Fig. 2.10

Transmission measurements could, however, result in a rather strong frequency dependence of the real part of the gate-source impedance, which indicates a nonuniform current distribution. This is illustrated in the case example of Fig. 2.10 corresponding to a device with nonoptimized gate mask layout. The frequency-dependent gate resistance of Fig. 2.10b results from the impedance network of Fig. 2.11, the parameters of which are determined to match the measured transmission coefficients of the terminal gate-drain impedance, as Fig. 2.10a shows. The model represents two portions of the device that commute asynchronously in the application. This is the split gate effect, which is undesirable in most applications since it leads to increased switching losses [8].

2.1.2.2 DC Output Characteristics

Static characteristics include channel, forward body diode, and reverse ABD currents. These can be derived from either measurements or device physics simulations. The later may be necessary when the devices are not physically available (e.g., not yet fabricated or prototyped) or the accuracy of the measurement method in certain regions of operation becomes too low.

Regarding experimental characterization, the accurate measurement of the DC output characteristics is particularly a challenging issue because of device self-heating [9]. Dedicated curve tracers have been developed that improve the accuracy of some commercially available solutions. The proposed measurement approach presented in [10] is proven to mitigate self-heating while covering the full dynamic range of operation in both first and third quadrants.

ABD characteristics are separately obtained with a dedicated current pulse driver. The approach can capture ABD levels up to 50 V with pulse widths of less than 2 µs. Since the shape of the ABD is irrelevant for the purpose of this work, only a few points of the characteristics in the low current regime are measured, thereby avoiding the need of stressing the DUT. Note that in the measurements, gate voltage and junction temperature dependencies are taken into account.

Regarding device physics simulations, DC output characteristics are readily obtained from parameter sweep bias point calculations. With proper calibration of the device physics model, the simulations are accurate and representative of real behavior, as Fig. 2.12 illustrates.

Once the DC output characteristics are obtained, model parameters need to be calculated so that the fitting functions proposed in Sect. 2.1.1 match the raw data. In the first quadrant, the curves describing the channel characteristics (i.e., data below avalanche voltage) are used to determine by fitting procedures the parameters of (2.1). Figure 2.13 shows the results of a typical match. In the high v_{DS} range (Fig. 2.13a), the empirical function reproduces effects such as channel length modulation (or short-channel effect) and early avalanche, known from the physics of the device [11]. Furthermore, when fitting experimental raw data, the best agreement in the low v_{DS} range (Fig. 2.13b) is typically obtained when assuming a series

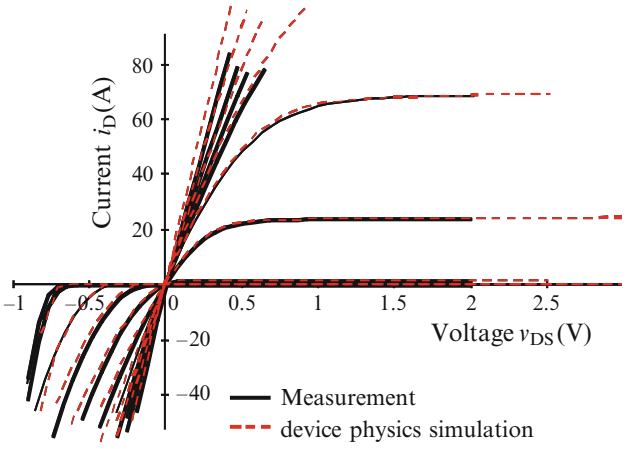

Fig. 2.12 First and third quadrant DC output characteristics ($i_{cn} + i_{dio}$) resulting from device physics simulations and measurements of a trench power MOSFET at 25°C (PHB96NQ03LT from NXP Semiconductors). Package resistance is considered in the comparison

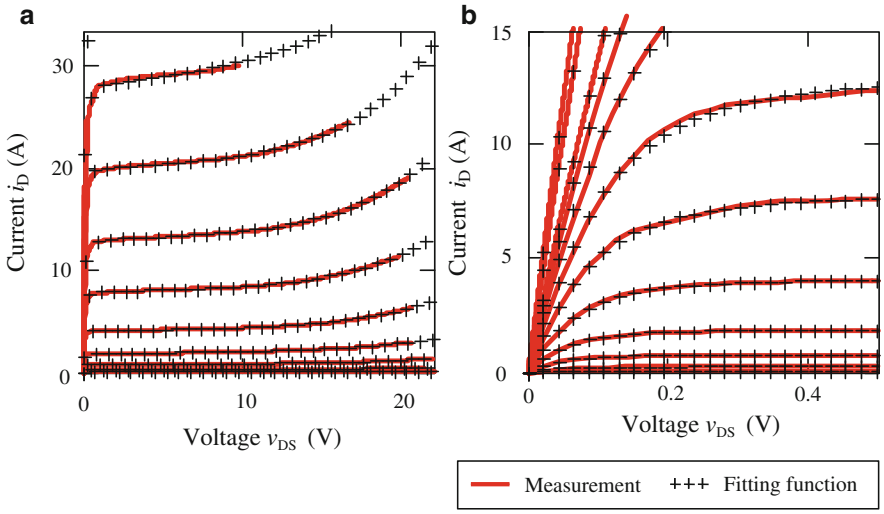

Fig. 2.13 First quadrant output characteristics (channel current) of a commercial device (PH3330 from NXP Semiconductors). at 25°C junction temperature. Comparison between measurements and fitting function (2.1) after calibration of model parameters. (a) Drain-source voltage range 0−20V. (b) Drain-source voltage range 0−0.5V

linear resistor to the channel. This extracted quantity is associated to the substrate resistance (R_{Sub} from Fig. 2.4).

Model parameter adjustments for the third quadrant undergo the de-embedding of the drain current into the channel and body diode contributions. For consistency with the MOSFETs body-effect theory (see Appendix A for details), the body diode characteristics are assumed to be independent on the gate voltage. The criterion to extract the body diode current from the sensed drain current is to assume that the channel current is negligible for gate voltages well below zero. In this operating region, any existing drain current is attributed to minority carriers in the body region. Figure 2.14 shows the result of de-embedding the drain current into the two current components of a simulated trench MOSFET structure. As it can be observed, the channel current can be a significant portion of the total current for subthreshold levels above zero volts. This will have a major impact on the switching dynamics, as it shall be described later.

Similarly to the first quadrant channel current, the parameters of the fitting functions for the third quadrant are calculated to accurately match the corresponding extracted current components. This completes the full static model calibration since the adjustments of the body diode fitting function are basically the same as for the ABD characteristics (see (2.6)).

2.1.2.3 Interelectrode Capacitances

Hard-switching applications particularly require accurate modeling of the nonlinear interelectrode capacitance [12] introduced in Sect. 2.1.1. This is because switching losses depend primordially on the value and shape of these capacitances, which are

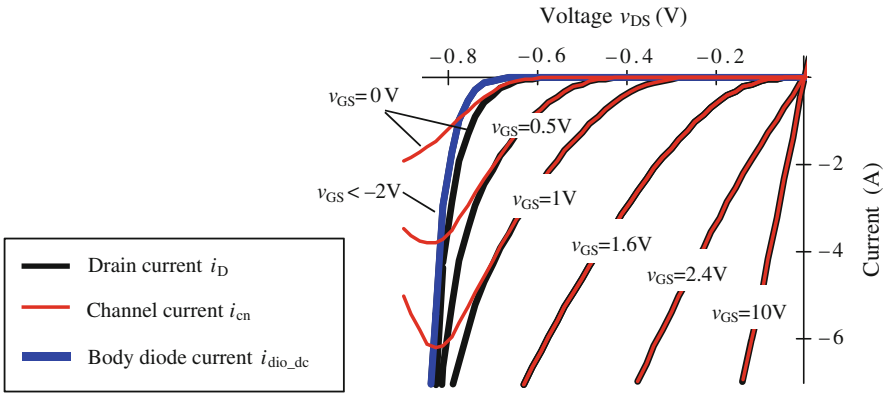

Fig. 2.14 Typical third quadrant output characteristics of high power trench power MOSFETs. Drain current de-embedding into channel and body diode currents. Data derived from 2D device physics simulations of a trench MOSFET cell with scale factor corresponding to a 1 mm^2 active area

generally dependent on both gate and drain voltages. Such dependence makes favorable the identification of operating regions of capacitive influence, thus enabling the possibility of finely defining the critical areas while simplifying others outside the ranges of interest. Important areas of operation are determined from the switching trajectories of the MOSFETs, as illustrated in the state plane diagram of Fig. 2.15. The highlighted areas correspond to the blocking and active regions of the devices. While the former may be experimentally covered by means of small signal impedance analyzers, measurements in the active region essentially involve signal excitation by power sources. Among the various alternatives, the proposed approach measures the current response to large signal voltage ramps, which are generated by means of a linear capacitor and a constant current source as charging pump. In addition, SMT capacitors are employed as high frequency shorts that allow the simplification of the capacitance extraction. These capacitors are connected in close proximity to the DUT so as to mitigate the effect of interconnect and package parasitic inductances. This is important because the ramp slope is limited by the disturbances caused by these parasitic elements. Note that steep ramps are desirable to increase the sensitivity of the measurement and reduce self-heating. Figure 2.16 shows the simplified diagram of the measurement setup, which is valid for both impedance analyzer and voltage ramps. The terminal voltage of the DUT and switches S_i and S_o are controlled by the measurement instrument, which can be automated to cover the entire capacitance range. In order to achieve this, the measurement instrument must be capable of providing not just the excitation signals and measurement means but also the DC bias voltage sources. Two of them are required for small signal measurements, whereas only one may be necessary in combination with the voltage ramp approach.

The measurement instrument is configured such that it allows various contact configurations between the DUT, excitation signal, and bias voltages. The full capacitance range is obtained by means of six different measurements, the configurations

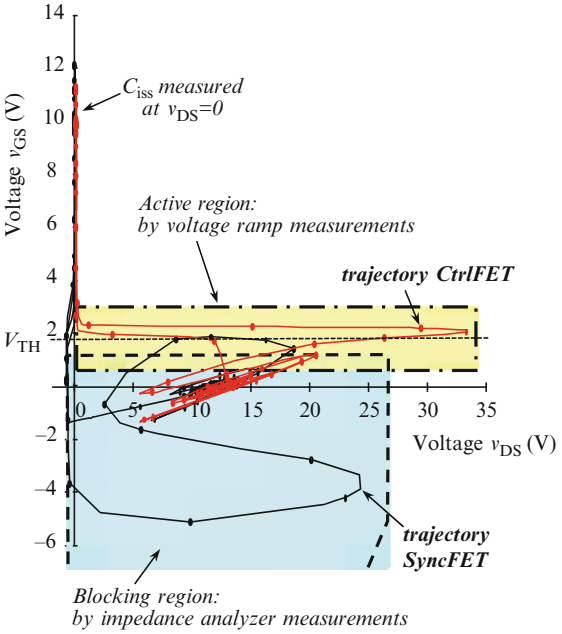

Fig. 2.15 State space diagram of MOSFET voltages. Trajectories result from simulations of typical switching events in a VR application

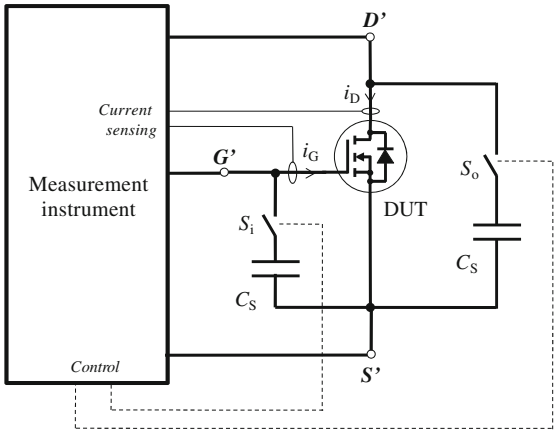

Fig. 2.16 Setup for extraction of MOSFET capacitances. Measurement instrument may comprise an impedance analyzer or a voltage ramp generator with current sensing means

of which are summarized in Table 2.3. Measurements C_a to C_c are carried out with an impedance analyzer and two DC bias voltages for v_{DS} and v_{GS}. The combination of these three measurements allows the extraction of three capacitances. Other measurement combinations are possible. The measurement covers the entire blocking region well below V_{TH} (typically for $v_{GS} < 1$ V). In addition, input capacitance C_{iss} can be determined for the particular case of $v_{DS} = 0$, which is important during ON conduction. Besides the advantage of not requiring high frequency capacitance

Table 2.3 Summary of methods for MOSFET capacitance extraction in both blocking (shaded rows) and active regions of device operation

Reference capacitance	Excitation	Measurement	Switch states		Extracted capacitance
			S_i	S_o	
C_a	Small AC signal G–S	Impedance Z_{GS}	0	0	$C_{GS} + \left(\frac{1}{C_{GD}} + \frac{1}{C_{DS}}\right)^{-1}$
C_b	Small AC signal D–S	Impedance Z_{DS}	0	0	$C_{DS} + \left(\frac{1}{C_{GD}} + \frac{1}{C_{GS}}\right)^{-1}$
C_c	Small AC signal G–D	Impedance Z_{GD}	0	0	$C_{GD} + \left(\frac{1}{C_{GS}} + \frac{1}{C_{DS}}\right)^{-1}$
C_d	Ramp voltage G–S	Gate current i_G	0	1	$C_{iss} = C_{GS} + C_{GD}$
C_e	Ramp voltage D–S	Gate current i_G	1	0	$C_{rss} = C_{GD}$
C_f	Ramp voltage D–S	Drain current i_D	1	0	$C_{oss} = C_{DS} + C_{GD}$

shorts, these three independent measurements relate to the inverse of the capacitance matrix of (2.9) with the following simple equations:

$$C^{-1} = \begin{pmatrix} m_2 & m_0 \\ m_0 & m_1 \end{pmatrix}, \tag{2.19}$$

$$\begin{pmatrix} m_0 \\ m_1 \\ m_2 \end{pmatrix} \equiv \begin{pmatrix} m_0(v_{DS}, v_{GS}) \\ m_1(v_{DS}, v_{GS}) \\ m_2(v_{DS}, v_{GS}) \end{pmatrix} = \begin{pmatrix} -2 & 1 & 1 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{pmatrix} \cdot \begin{pmatrix} C_c^{-1}(v_{DS}, v_{GS}) \\ C_b^{-1}(v_{DS}, v_{GS}) \\ C_a^{1}(v_{DS}, v_{GS}) \end{pmatrix}. \tag{2.20}$$

The coefficients in matrix $\boldsymbol{C}^{-1}$ determined from voltage ramps, i.e., measurements C_d to C_f, involve more complex relations, as it can be deduced from (2.9). This may lead to a lower accuracy of the calculated matrix coefficients as a consequence of inherent noise in the raw data. Furthermore, measurement C_f in the active region can only be accurate as long as the channel current is comparatively low with respect to the capacitive current. This can be seen from the following expression for the output capacitance calculation:

$$C_f \equiv C_{oss}(v_{DS}, v_{GS}) = \left.\frac{i_D(v_{DS}, v_{GS}) - i_{cn}(v_{DS}, v_{GS})}{\frac{dv_{DS}}{dt}}\right|_{v_{GS}=\text{const.}}. \tag{2.21}$$

The above expression clearly evidences that any uncertainty in the prediction of the channel current will lead to an error of C_{oss} that increases in proportion to the subtracted magnitude relative to the capacitive current. Therefore, in practice, and due to the limited voltage ramp slope, the maximum gate voltage is typically limited slightly above V_{TH}. On the other hand, the drain voltage must be maintained below the ABD voltage level, and above the body diode conduction for negative values of v_{GS}. Note that the body diode stored charge in forward conduction is assumed to be dominated by minority charges in the quasi-neutral regions of the

device. The effects of these charges are analyzed and modeled separately in the next section.

In case of C_{iss} and C_{rss}, the covered ranges are typically wider than for C_{oss} since the measured gate current is not subject to the subtraction of large quantities, as the following equations suggest:

$$C_d \equiv C_{\mathrm{iss}}(v_{\mathrm{DS}}, v_{\mathrm{GS}}) = \left.\frac{i_{\mathrm{G}}(v_{\mathrm{DS}}, v_{\mathrm{GS}})}{\frac{\mathrm{d}v_{\mathrm{GS}}}{\mathrm{d}t}}\right|_{v_{\mathrm{DS}}=\mathrm{const.}}, \tag{2.22}$$

$$C_e \equiv C_{\mathrm{rss}}(v_{\mathrm{DS}}, v_{\mathrm{GS}}) = \left.\frac{i_{\mathrm{G}}(v_{\mathrm{DS}}, v_{\mathrm{GS}})}{\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}}\right|_{v_{\mathrm{GS}}=\mathrm{const.}}. \tag{2.23}$$

Both measurements C_e and C_f require DC voltage bias for the gate-source, whereas measurement C_d needs it for the drain–source. The ability to keep constant values depends on the ramp slope, the value of C_{S} and the parasitic elements between the DUT and C_{S}.

Figure 2.17 shows an example of extracted reverse and input capacitance of a measured device in both blocking and active regions. Consistent experiments demonstrate that the voltage ramp approach allows extending the capacitance range into areas corresponding to switching trajectories of up to 30 A loads. The voltage ramp measurements partially cover the blocking region in order to compare the results of the two methods. Further data validation is possible by comparing

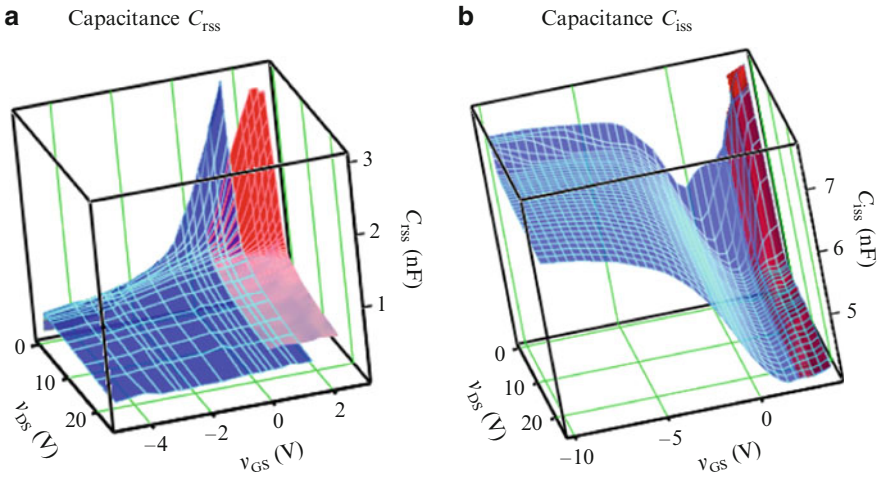

Fig. 2.17 MOSFET capacitance extraction in both blocking and active regions of device operation resulting from combining impedance analyzer and voltage ramps measurement approaches. Data extended into the active region (i.e. gate-source voltage higher than 2V are derived from voltage ramp measurements. Experimental results of device PH3330 from NXP Semiconductors at 25°C (a) Transfer capacitance, (b) input capacitance

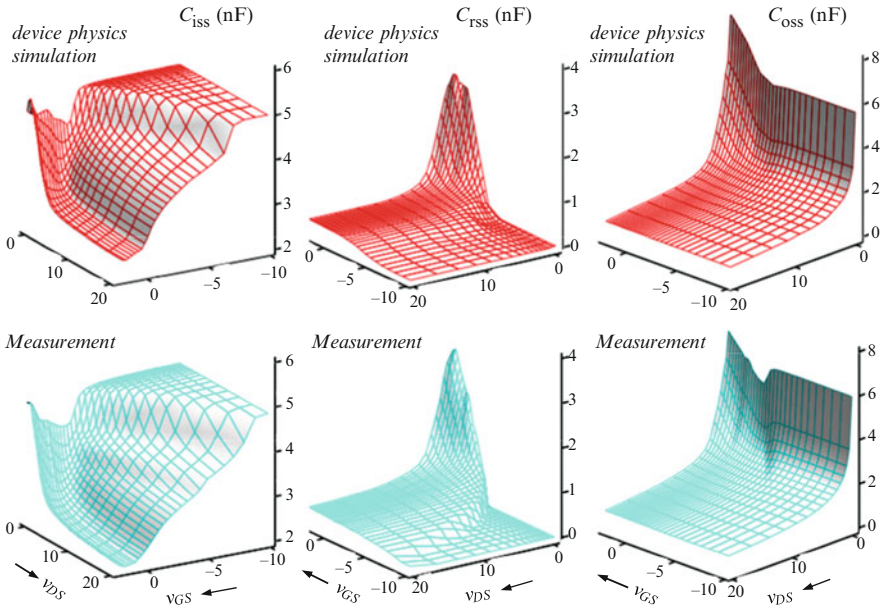

Fig. 2.18 Comparison of capacitance extraction results from device physics simulations and measurements of a trench MOSFET at 25°C

the shape of the capacitance curves with device physics simulations, as shown in Fig. 2.18. In order to extract the capacitance from the device physics model, transient simulations are performed based on the same principles applied for the measurements in the active region. As Fig. 2.18 shows, the results are comparable both in magnitude and shape. Because of this close correlation, device physics simulations can be further employed to extend the data beyond the experimental limits of the measurement approach. This includes the output capacitance in the active region.

2.1.2.4 Body Diode Reverse Recovery

The proposed dynamic lumped diode model defined in (2.7) is suitable for the representation of RR characteristics of low-voltage trench MOSFETs. As it has been shown, the model has a very simple structure, it is easy to implement in a circuit simulator and, as it will be shown in this section, it predicts with virtually no error transient responses of both device physics simulations and measurements.

The model derives from the lumped charge model proposed by Lauritzen and Ma [2], as described in Appendices B and C. It employs parameters β_{rr} and $t_{\beta rr}$, both of which need to be adjusted by empirical methods. To carry out this task, practically all other MOSFET characteristics are demanded in advance. It includes the capacitance characteristics, channel conduction in the third quadrant, DC body diode forward characteristics and package parasitic elements (the latter only in case

of experimental characterization). This implies that both β_{rr} and $t_{\beta rr}$ are usually the last parameters of the MOSFET model to be derived. These parameters are adjusted by curve fitting of a reference RR transient, which may be derived from either device physics simulations or measurements. In either case, curve fitting may involve a procedure to de-embed the body diode diffusion current from the total drain current.

RR may be produced by resistive or inductive loads. Both modes are equally valid for the extraction of the model parameters. For convenience, parameter extraction by device physics simulations is illustrated with a resistive recovery setup, whereas inductive RR will be analyzed experimentally.

Figure 2.19 shows the circuit diagram of a resistive RR setup, which can readily be arranged for device physics transient simulations. Note that parasitic elements are ignored to facilitate the characterization. Thus, $v_{DS'} = v_{DS}$ and $v_{GS'} = v_{GS}$.

Simulation examples of the proposed circuit arrangement are shown in Fig. 2.20. The transient curves result from both device physics simulations and SPICE simulations of the behavioral model with properly adjusted RR parameters. In all cases, the body diode is forward biased with the same initial current. The plots in the left column show the impact of the di/dt drain current variation while keeping v_{GS} constant. On the other hand, the plots in the right column illustrate variations of v_{GS} at constant di/dt. Regarding voltage and current waveforms, the simple RR model together with the capacitance and static characteristics agree with the device physics simulations. The variations of di/dt and gate voltage do not imply the modification of the RR parameters. However, the RR current at zero v_{GS} is already lower than at negative v_{GS}. At v_{GS}= 1 V, the body diode current (as it appears from the device terminal) vanishes completely. These effects are studied in detail in Appendix B.

Calculation of RR current from experimental waveforms involves more steps than from device physics simulations, because of transient voltage drops at the package impedances of the real device. Namely, the source inductance may cause a voltage drop affecting v_{GS}, which cannot be avoided since the gate impedance makes impressing this "internal" voltage impossible. This means that the gate current cannot be kept zero and all capacitance characteristics are involved in the experiment. Here, the measured $v_{DS'}$ is applied to the model in order to compare drain and gate currents resulting from measurements and SPICE simulations of the behavioral model. The simulated v_{GS} trace in Fig. 2.21 indicates that, depending on gate voltage fluctuations due to capacitance characteristics and package inductances, measurements can only be performed up to a certain value of $v_{GS'}$ that is far below threshold. Hence, Fig. 2.21 illustrates the limits of experimental RR

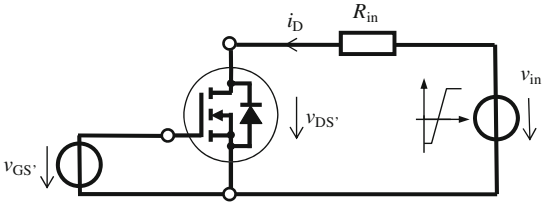

Fig. 2.19 Setup for resistive reverse recovery (RR)

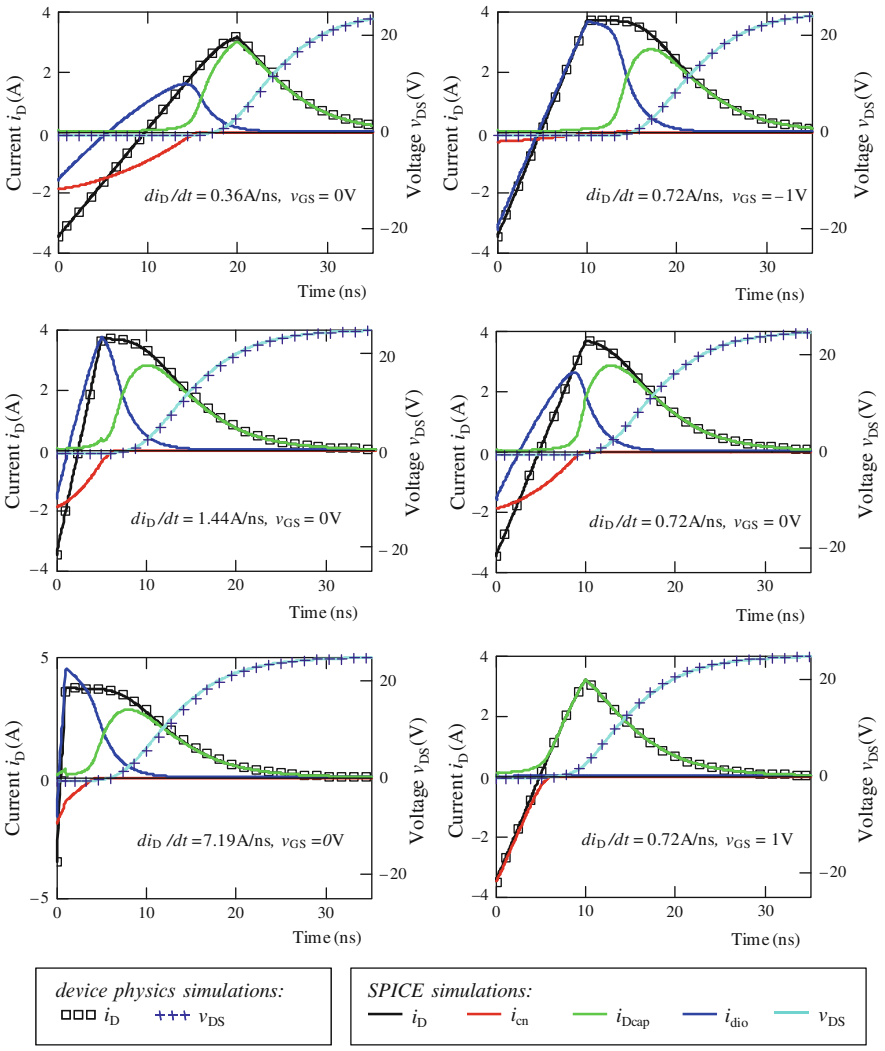

Fig. 2.20 Comparison of resistive RR resulting from device physics simulations and SPICE simulations of the proposed behavioral model. Left column: d*i*/d*t* variations; right column: v_{GS} variations. Data refers to a 25 V, 5 mΩ logic level n-channel trench MOSFET at 25°C. Extracted model parameters: $t_{\beta rr} = 2$ ns, $\beta_{rr} = 7.8$

characterization. However, within those limits, i.e., at sufficiently low gate voltage $v_{GS'}$, measurements show good agreement with device simulations in terms of RR parameters β_{rr} and $t_{\beta rr}$. Since these parameters as resulting from device simulations show no dependence on gate voltage, measurements at a sufficiently negative $v_{GS'}$ may yield all required data.

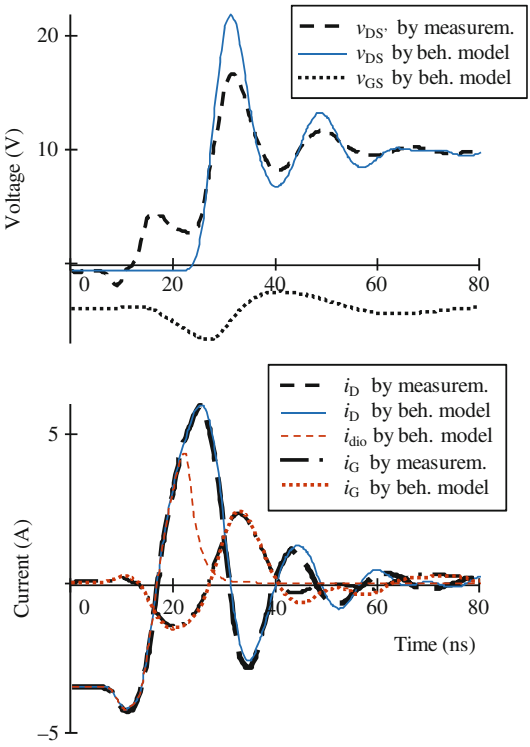

Fig. 2.21 Inductive RR transient. Comparison between measured and SPICE simulations of behavioral model at $v_{GS'} = -4$ V and $di_D/dt = 1$ A/ns at time = 15 ns. MOSFET type: PHB96NQ03LT from NXP Semiconductors. Extracted model parameters: $t_{\beta rr} = 2$ ns, $\beta_{rr} = 8$

2.2 Switched Converter Test Board

MOSFET performance must be evaluated under the conditions established by the application at hand. Particularly, the main focus is on the analysis of the half-bridge of SRBCs for VRs. All the elements of the switched circuit that may influence the behavior of the MOSFETs have to be considered. These include the gate drivers, dead time control, PCB layout parasitic elements, input filter capacitors, and output inductor. In order to investigate the interaction of these elements with the MOSFETs, a number of SRBC test boards are prototyped that experimentally aid the analysis of various power MOSFET discrete solutions. These prototype boards are taken as reference to build a SRBC lumped model for circuit simulators that integrates the proposed MOSFET model of Sect. 2.1. To accomplish this, relevant components comprising the test circuit are individually characterized and modeled according to the analysis demands. Combining them properly in a simulator environment will result in a circuit model setup that enables to meet two goals: First, a thorough validation of the MOSFET model by means of experimental data; and second, a realistic representation of the switched converter for investigations on switching behavior. Further details of the test boards are described in Appendix G with a summary of their main features and specifications.

2.2.1 Gate Driver

The gate circuit and control for driving the power MOSFETs are key elements influencing switching performance. Thus, fine adjustments of their related parameters will be critical in the design phase of the switched converter. Regardless of the circuit topology, important aspects to be considered in the gate drive design are the gate impedance, maximum gate current, ON and OFF state voltage levels, and driving losses. These driver characteristics are considered in the circuit diagram of Fig. 2.22, corresponding to a conventional gate drive topology. It consists of a half-bridge configuration that enables the commutation of the power device by driving its gate between two voltage levels, V_{drvp} and V_{drvn}. For convenience, V_{drvn} usually corresponds to zero volts, whereas V_{drvp} strongly depends on the driving demands and requires to be optimized accordingly. These two voltage levels are provided from what are considered ideal voltage sources. Nonetheless, parasitic inductances are included in the half-bridge, which model the interconnection impedance of these usually external voltage sources to the drive circuit.

Like in most high speed gate drivers, MOSFET devices (M_{p} and M_{n}) are the preferred transistor type for the implementation of the half-bridge switches. These drive MOSFETs are driven by buffers connected to the control circuitry. The driving voltages of these buffers (V_{drvpi} and V_{drvni}) are relevant for the estimation of the generated losses [13].

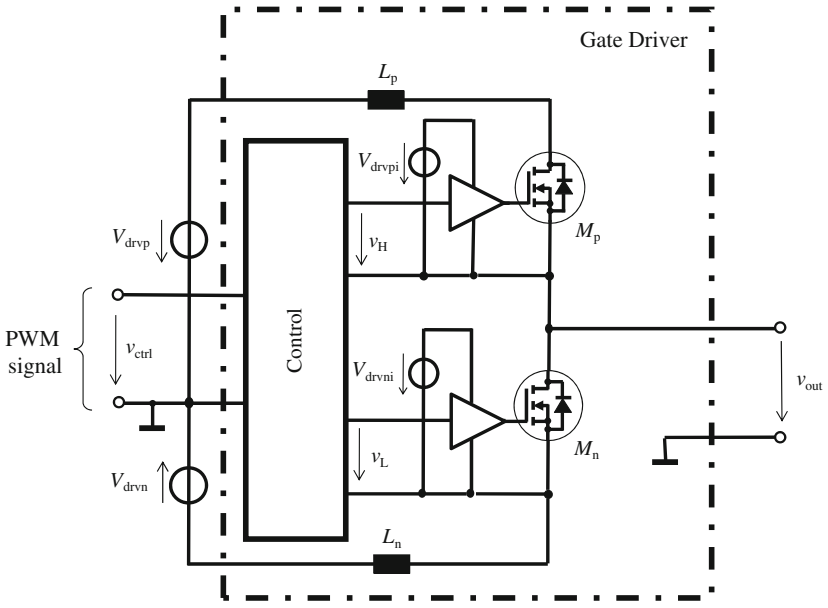

Fig. 2.22 Circuit diagram of MOSFET gate driver

Special emphasis is given to the modeling of M_p and M_n, for they may limit the gate driving current, thus representing a main barrier to the increase of switching frequency. Furthermore, the gate switches can be major sources of losses in the gate circuit. One reason of this is that, even though the gate switches can reach ZCS operation, switching losses may still be significant as consequence of the parasitic input and output charges. The representations of these charges as linear capacitors are frequently sufficiently good approximations to determine the total charge related losses. In addition, the channel of these gate devices has to be modeled so that the behavior in the first quadrant is properly represented with the ohmic, active, and blocking regions.

Similarly as described in Sect. 2.1.1, but to a higher level of simplification, the gate drive circuit implementation of Fig. 2.22 results in the circuit diagram of Fig. 2.23. As it can seen, each driver MOSFET in the half-bridge circuit is modeled with an output capacitor, current-dependent source (i.e., channel current) and a series resistance. The gate of these MOSFETs consists of a series connection of a voltage-dependent source, a gate resistor and a linear capacitor representing the input capacitance of the device. The voltage source is managed by input control signal v_{ctrl} and the gate voltage of its associated device from the half-bridge. The condition for the turn-on is such that shoot-through is avoided, as expressions (2.24) and (2.25) reflect.

Expression (2.26) is a simplified version of (2.1) to represent the DC output characteristics of a MOSFET in the first quadrant. Parameters l_S and R_{on} are defined to conveniently adjust the levels and shape of the curves. Figure 2.24 shows that the characteristics represented by (2.26) realistically reproduce the saturation effects observed in conventional gate drivers. Computing the derivative of (2.26) with respect to v_{DS} yields the dynamic resistance, which depends on the applied current as illustrated in Fig. 2.25.

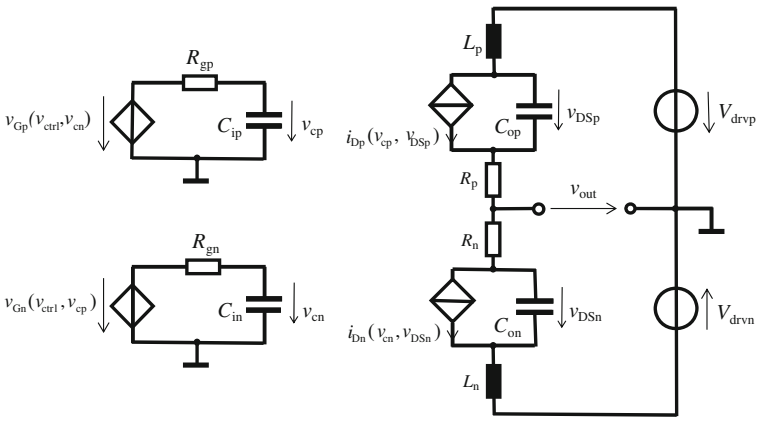

Fig. 2.23 MOSFET gate driver implementation in circuit simulator

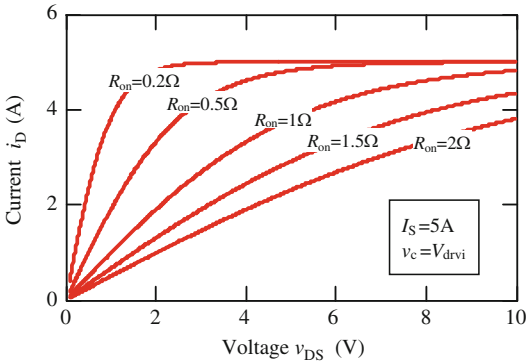

Fig. 2.24 DC static characteristics of driver MOSFETs based on (2.26)

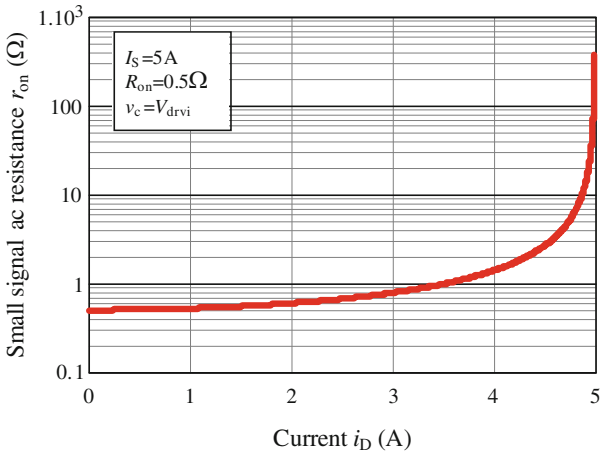

Fig. 2.25 ON state resistance of drive MOSFETs defined as the derivative of (2.26) with respect to v_{DS}

$$v_{Gn}(v_{ctrl}, v_{cp}) = \begin{cases} V_{drvni} & \text{if } (v_{ctrl} = 0 \ \& \ v_{cp} < V_{THp}), \\ 0 & \text{otherwise}, \end{cases} \tag{2.24}$$

$$v_{Gp}(v_{ctrl}, v_{cn}) = \begin{cases} V_{drvpi} & \text{if } (v_{ctrl} = 1 \ \& \ v_{cn} < V_{THn}), \\ 0 & \text{otherwise}, \end{cases} \tag{2.25}$$

$$i_D(v_c, v_{DS}) = I_S \cdot \frac{v_c}{V_{drvi}} \tanh\left(\frac{v_{DS}}{I_S \cdot R_{on}}\right). \tag{2.26}$$

Linear input and output capacitance values for M_p and M_n are calculated based on the following average expression:

$$C_{av} = \frac{1}{|V_f - V_i|} \int_{V_i}^{V_f} C_x(v)\, dv. \tag{2.27}$$

Thus, $C_{av} \cdot |V_f - V_i|$ corresponds to the total charge stored in or removed from nonlinear capacitor C_x. The value of C_{av}, like the rest of parameters of the driver model, can be usually derived from the datasheet of the employed driver, since it contains all required information referent to the characteristics of the gate switches. The datasheet information may be complemented with specific measurement tests to extract additional driver characteristics such as idle losses, as described in [14].

The proposed model, as such, allows the study of interactions between the elements of the driver and power MOSFET in the circuit simulator, as it shall be described later in this chapter.

2.2.2 Input/Output Filters

Of key relevance to the switching performance of the MOSFETs are the input filter capacitors, mainly by virtue of their contributions to the parasitic inductances of the half-bridge loop. The input filter of the test boards (see Appendix G) is used as illustration in the following discussion. Such a filter comprises a capacitor bank of three different types of parallel decoupling capacitors; the OSCON is the one type of capacitors used to supply most of the DC energy content during the ON state period of the CtrlFET. The other two types are ceramic capacitors of various dimensions featuring low ESR and ESL to provide high frequency decoupling capabilities. The equivalent circuit of the impedance network seen at the terminals of the filter is represented in Fig. 2.26. The parameters of the network are determined from curve fitting of the frequency response measured with a VNA. Figure 2.27 compares the results of the measured and simulated transmission coefficient from the scattering matrix. The resonances at 4.5 and 16 MHz correspond to SMD ceramic capacitors, which effectively contribute to significantly lower the impedance well above the resonance of the OSCON capacitors (i.e., ≈100 kHz).

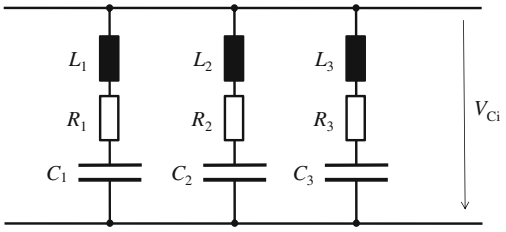

Fig. 2.26 Equivalent input filter capacitor representation of test board (see Appendix G)

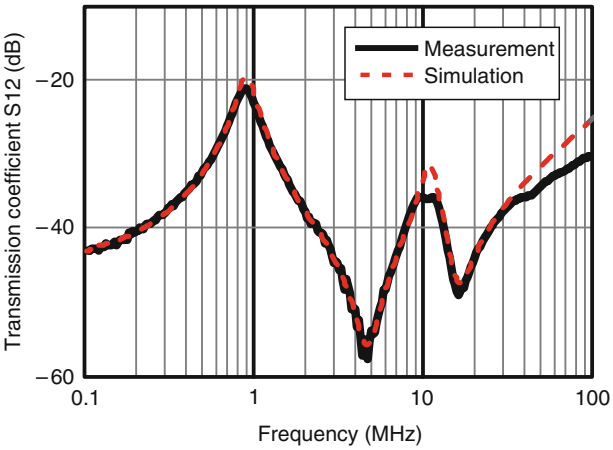

Fig. 2.27 Frequency response of input filter capacitor. Measurement response derives from VNA. Simulations correspond to circuit of Fig. 2.26. Values: $L_1 = 150$ pH, $L_2 = 217$ pH, $L_3 = 4.9$ nH, $R_1 = 4.5$ mΩ, $R_2 = 1.6$ mΩ, $R_3 = 6.5$ mΩ, $C_1 = 620$ nF, $C_2 = 5{,}243$ nF, $C_3 = 8{,}400$ nF. Capacitances C_2 and C_3 are derived from impedance analyzer measurements due to the limited frequency range of the VNA

The output filter can be highly simplified for the study of MOSFET performance. The most important simplification is the replacement of the output filter capacitors by an ideal voltage source, thereby neglecting any influence that the output ripple may have on MOSFET switching. The current ripple, however, must be taken into account for the estimation of both ON conduction and switching losses. For this it is sufficient to model the output choke as an ideal inductance. A series resistor may be simply added to cope with the resistance of the track, contacts, and winding. A more accurate model of the output inductor will be considered latter for the estimations of the overall converter losses.

2.2.3 PCB Layout Impedance Characterization

One of the main concerns of hard-switching SRBCs is the energy loss produced by the parasitic inductances in the half-bridge. It is therefore essential to determine the magnitude of such parasitic elements. The main purpose of this section is to obtain an equivalent lumped network of the half-bridge PCB layout from the test boards. The main difficulty of this task is to discern the impedance contribution of the track portions constituting the half-bridge circuit layout. This is accomplished by the time domain measurement method described in [15]. The technique basically consists of generating high amplitude oscillations at resonant frequencies close to those excited in the application. To achieve this, the power MOSFETs are replaced by accurately characterized linear capacitors of low ESR and ESL. A high power

driver is then used to inject pulses from the side of the input filter capacitor, thereby generating oscillations between the parasitic layout inductance and the reference capacitors. Track inductances can therefore be determined by measuring sections of the PCB with differential probes in such a way that disturbances are minimized (e.g., reduction of coupling effects in the sensing probes). The estimated inductances derive from fitting procedures of the measured signals. The resulting PCB electrical model consists of a series of equivalent lumped inductors related to certain areas of the layout. Figure 2.28 illustrates the results of a characterized test board, where portions of the half-bridge and gate circuit are represented. Reference voltages $v_{\mathrm{drv(s)}}$, $v_{\mathrm{drv(c)}}$, and $v_{\mathrm{DSx(c)}}$ are probing points for switching waveform measurements, whereas V_{Ci} corresponds to the input filter capacitor voltage, as indicated in Fig. 2.26. Resistance R_{sh} is incorporated for current sensing means. Note that when measuring the voltage across this shunt resistor, the influence of its ESL (i.e., inductor L_{sh}) must be taken into account for determining the current waveform. Further details of the PCB layout design are provided in Appendix G.

The derived circuit and MOSFET models can be experimentally validated by measuring V_{Ci}, $v_{\mathrm{drv(s)}}$, $v_{\mathrm{drv(c)}}$, v_{sh}, and $v_{\mathrm{DSx(s)}}$. The resulting waveforms from V_{Ci}, $v_{\mathrm{drv(s)}}$, and $v_{\mathrm{drv(c)}}$ are then used in the simulator as time-dependent voltage excitation

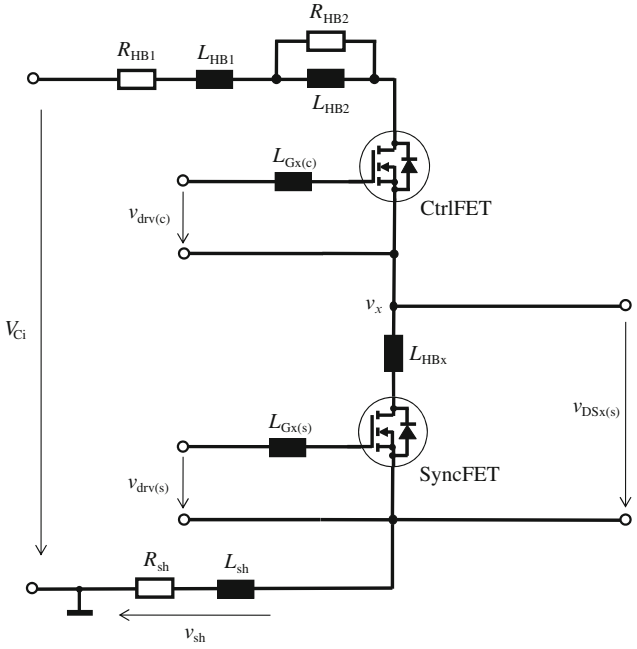

Fig. 2.28 Lumped model representation of half-bridge and gate drive layout parasitic elements from switching test board (see Appendix G, Sect. G.1). Package parasitic elements of MOSFETs are not represented. Extracted values: $R_{\mathrm{HB1}} = 3.5\ \mathrm{m\Omega}$, $L_{\mathrm{HB1}} = 1.5\ \mathrm{nH}$, $R_{\mathrm{HB2}} = 75\ \mathrm{m}$, $L_{\mathrm{HB2}} = 500\ \mathrm{pH}$, $L_{\mathrm{Gx1}} = 250\ \mathrm{pH}$, $L_{\mathrm{Gx2}} = 250\ \mathrm{pH}$, $L_{\mathrm{HBx}} = 600\ \mathrm{pH}$, $L_{\mathrm{sh}} = 170\ \mathrm{pH}$, $R_{\mathrm{sh}} = 100\ \mathrm{m\Omega}$

sources. Thus, predictions of v_{sh} and $v_{DSx(s)}$ are produced and compared to the corresponding measured data in order to assess the accuracy of the models. Such validation procedure will be discussed in more detail in Sect. 2.4.

2.3 Switched Converter Simulation Setup

This section presents the final circuit representation of the SRBC based on the previously introduced models of the power MOSFETs, PCB layout, gate drivers, and input/output filters. Control circuitry is additionally included to allow automatic adjustments of the dead times as well as regulation of steady-state conditions that effectively enhance simulation performance.

Since the main purpose of the converter model is to investigate the performance of the power MOSFETs in the application, special emphasis is given to properly represent the elements of the circuit influencing the behavior of the power devices, such as the half-bridge impedance, gate drivers, and output choke. The rest of the elements from the switched circuit are simplified or completely neglected so as to improve tractability and explicitness. Regarding control aspects, disturbances such as the load transient and other similar dynamic events are not taken into consideration. Namely, the analysis is devoted to the nominal operating conditions, which involve periodic steady-state waveforms.

Figure 2.29 shows the proposed simulation setup of the SRBC. The block diagrams of the input filter capacitors and half-bridge PCB layout contain the models of Sects. 2.2.2 and 2.2.3, respectively. The MOSFET subcircuit model is based on the diagram of Fig. 2.4.

The gate driver and control system of Fig. 2.29 is depicted in more detail in the diagram of Fig. 2.30. Two main blocks are identified. The MOSFET driver control regulates the state of the half-bridge switches according to a PWM input signal. Furthermore, the dead times of the switched node leading and falling edges (FEs) can be programmed to predefined values. The controller thus keeps the body diode conduction times of the SyncFET constant and independent on the circuit conditions. The operation is as follows: the simulation starts in the first switching cycle with an initial guess for the delay times between switching actions of the gate signals. In the same switching cycle the controller monitors the internal drain– source voltage of the SyncFET (i.e., $v_{DS(s)}$ of Fig. 2.4) to determine the body diode conduction times, (e.g., time during which $v_{DS(s)}$ less than -0.6 V). In the next switching cycle the delay time is readjusted to correct for the difference between the programmed and sensed body diode conduction times. This is done individually for both the leading and FEs of the PWM signal. Thus, each transition edge can be independently adjusted with different dead time values.

The control signal outputs are connected to buffers that drive the power MOSFETs. The implementation of these gate buffers is as described in Sect. 2.2.1. Additionally, $L_{drv(c)}$, $L_{drv(s)}$, $R_{drv(c)}$, and $R_{drv(s)}$ may represent PCB layout

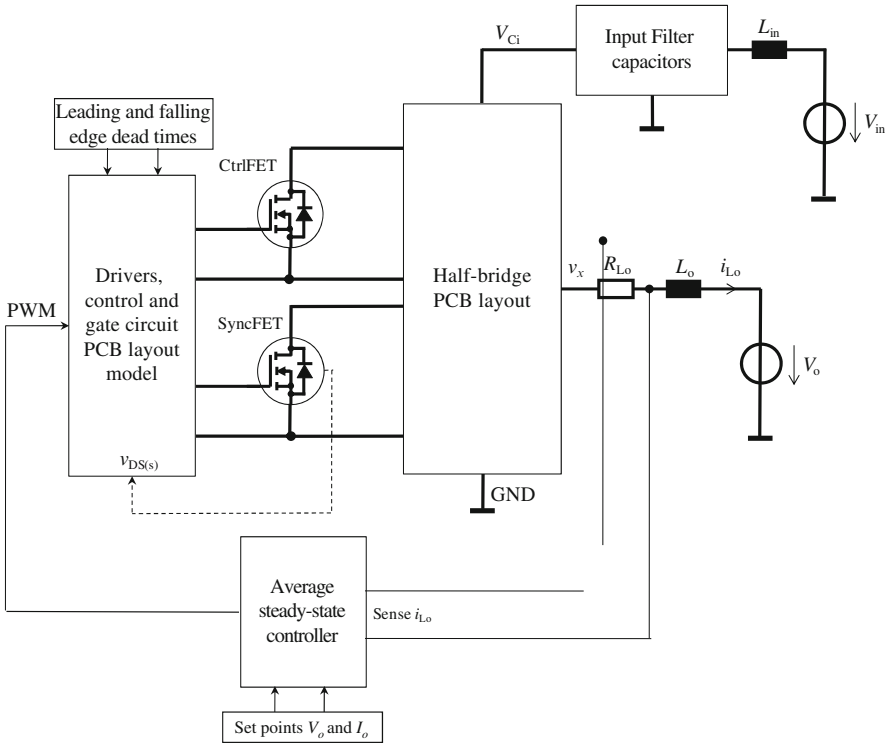

Fig. 2.29 Simulation setup diagram of the SRBC

parasitic elements or external components added for current sensing and other test purposes.

The main purpose of the average steady-state controller is to provide a PWM signal that leads to the specified steady-state conditions in the least number of switching cycles, thereby minimizing simulation times. The steady-state conditions occur when the following two conditions are met,

$$\frac{1}{T_s}\int_{t_x}^{t_x+T_s} i_{Lo}\cdot \mathrm{d}t = I_{Lo} = I_o, \tag{2.28}$$

$$\frac{1}{T_s}\int_{t_x}^{t_x+T_s} v_{Lo}\cdot \mathrm{d}t = V_{Lo} = 0, \tag{2.29}$$

where v_{Lo} is the voltage across output inductor L_o and I_o is the load current. Two control variables are required to satisfy the above two conditions. On the one hand, the average current through the output choke is regulated by the switching period of the PWM signal, which must equal to the target value once steady-state has been reached. On the other hand, the average voltage across the inductor is controlled by means of the duty cycle ON time, or in other words, CtrlFET ON time.

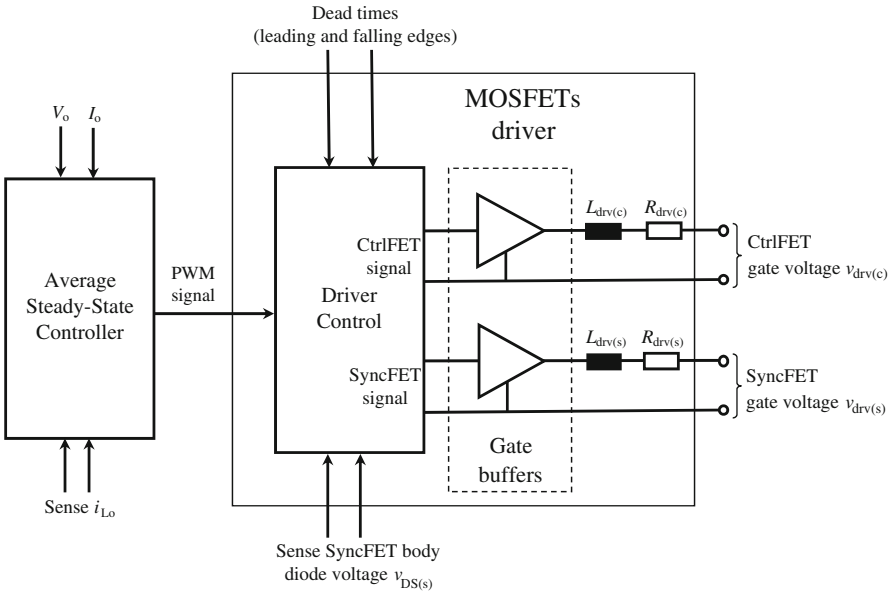

Fig. 2.30 Block diagram of driver and average steady-state controller. Implementation in a circuit simulator for transient analysis

The operation of the average steady-state controller is illustrated in Fig. 2.31. The simulation starts at the beginning of the switching period, which is defined as the leading edge (LE) of the PWM signal. The initial guess for the output coil current ($i_{Lo0(G)}$) at that time is as follows:

$$i_{Lo0(G)} = I_o - \frac{I_{o(pp)}}{2} + \frac{V_o + I_o \cdot R_{sp}}{L_{sp}} .t_{dCr}, \tag{2.30}$$

where $I_{o(pp)}$ is the peak-to-peak output current ripple, R_{sp} and L_{sp} are the total resistance and inductance of the SyncFET and output paths, respectively (i.e., including all parasitic components). Time t_{dCr} is the delay existing between the PWM and the CtrlFET signal at the LE transition. The initial guess for the CtrlFET ON time is as follows:

$$t_{on(G)} = \frac{V_0}{V_{in}} \cdot T_s + t_{dCr} - t_{dCf}. \tag{2.31}$$

Time t_{dCf} is the delay time between the PWM and the CtrlFET signal at the FE transition.

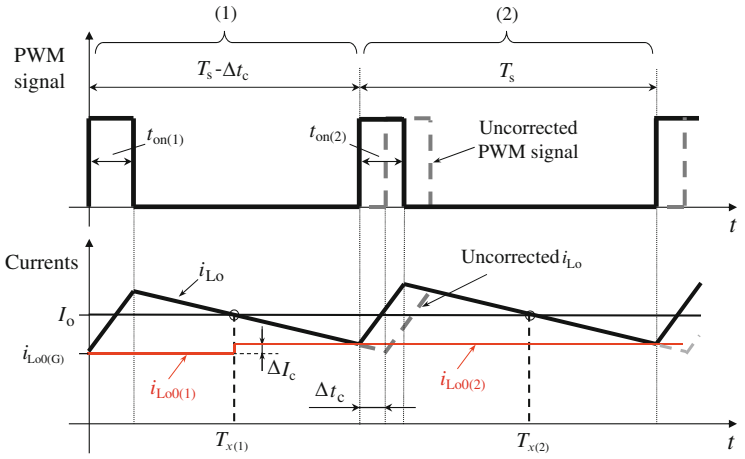

Fig. 2.31 Example of operation of the average steady-state controller

The controller computes the average values of i_{Lo} and v_{Lo} from the actual switching cycle and estimates both CtrlFET ON time and minimum output inductor current for the next period as follows:

$$t_{on(2)} = t_{on(1)} - \frac{V_{Lo(1)}}{V_{in}} \cdot T_s, \tag{2.32}$$

$$i_{Lo0(2)} = i_{Lo0(1)} + I_o + \frac{V_{Lo(1)}}{L_o} \cdot T_s - I_{Lo(1)}. \tag{2.33}$$

Note that subindexes (1) and (2) refer to the past and present switching cycles, respectively. Conditions $t_{on(2)} = t_{on(1)}$ and $i_{Lo0(2)} = i_{Lo0(1)}$ are given when steady state is reached, that is to say, when (2.28) and (2.29) are both satisfied.

Equations (2.32) and (2.33) are calculated by the controller at particular time instants corresponding to those at which the inductor current equals the load current during the SyncFET ON times. This is indicated in Fig. 2.31 with times $T_{x(1)}$ and $T_{x(2)}$. Thus, the averaged state variables of the output coil at the actual switching cycle can be calculated as follows:

$$I_{Lo(1)} = \frac{1}{T_s} \cdot \left(\int_0^{T_{x(1)}} i_{Lo}(t) \cdot \mathrm{d}t + \int_{T_{x(1)}}^{T_s} i_{Lo}(t) \cdot \mathrm{d}t \right). \tag{2.34}$$

The first integral in (2.34) is numerically calculated during the simulation run. The calculation makes use of the simulated current waveform data that are available until that time instant. The second integral corresponds to a section of the ON time

of the synchronous MOSFET where no switching events occur. It is therefore possible to calculate it analytically as follows:

$$\int_{T_{x(1)}}^{T_s} i_{Lo}(t)\cdot dt=\frac{V_o}{R_{sp}}(T_s-T_{x(1)})-\frac{L_{sp}}{R_{sp}}\left(I_o+\frac{V_o}{R_{sp}}\right)(e^{-(R_{sp}/L_{sp})\cdot(T_s-T_{x(1)})}-1). \tag{2.35}$$

Equation (2.35) defines the integral current through a series RL circuit with constant voltage source V_o and initial current condition I_o. Similarly for $V_{Lo(1)}$,

$$V_{Lo(1)} = \frac{1}{T_s}\cdot\left(\int_0^{T_{x(1)}} v_{Lo}(t)\cdot dt + \int_{T_{x(1)}}^{T_s} v_{Lo}(t)\cdot dt\right), \tag{2.36}$$

$$\int_{T_{x(1)}}^{T_s} v_{Lo}(t)\cdot dt = L_o\left(I_o+\frac{V_o}{R_{sp}}\right)(e^{-(R_{sp}/L_{sp})\cdot(T_s-T_{x(1)})}-1). \tag{2.37}$$

In the illustration of Fig. 2.31 it is assumed that the average output coil current in the first cycle is lower than I_o, whereas $V_{Lo(1)}$ is zero. At time $T_{x(1)}$, current ΔI_c, corresponding to the difference between I_o and the average current through L_o, is added to $i_{Lo0(1)}$ as correction for the next cycle. The next cycle starts as soon as i_{Lo} reaches the new $i_{Lo0(2)}$ value. Note that in order to start the next cycle with a higher current, the period of the first cycle must be lower than T_s. The controller reaches its target in the second switching cycle since ΔI_c is zero and thus the switching period must equal T_s.

2.4 Model Validation

This section evaluates the accuracy of the proposed MOSFET model by comparing switching waveform and power loss simulations with experiments performed on a synchronous buck converter test board. The prototype circuit is specially designed to carry out studies on switching behavior of MOSFETs mounted on LFPak or other compatible discrete packages (for details of the test board, see Appendix G). A number of different test conditions are rigorously examined, which involve variations of the load current, input voltage, and driver parameters such as the ON state voltage and dead times.

Figure 2.32 represents the equivalent circuit of the test board, the parameters of which derive from the characterization techniques described in the previous sections of this chapter. The input filter and drivers are, however, not represented in the circuit model as described in Sects. 2.2.2 and 2.2.3. Instead, some of the measured signals are employed in the simulation as excitation voltage sources, which represent the behavior at the terminals of the drivers and input filter. Thus, the simulation setup and validation process of the MOSFET model is considerably simplified.

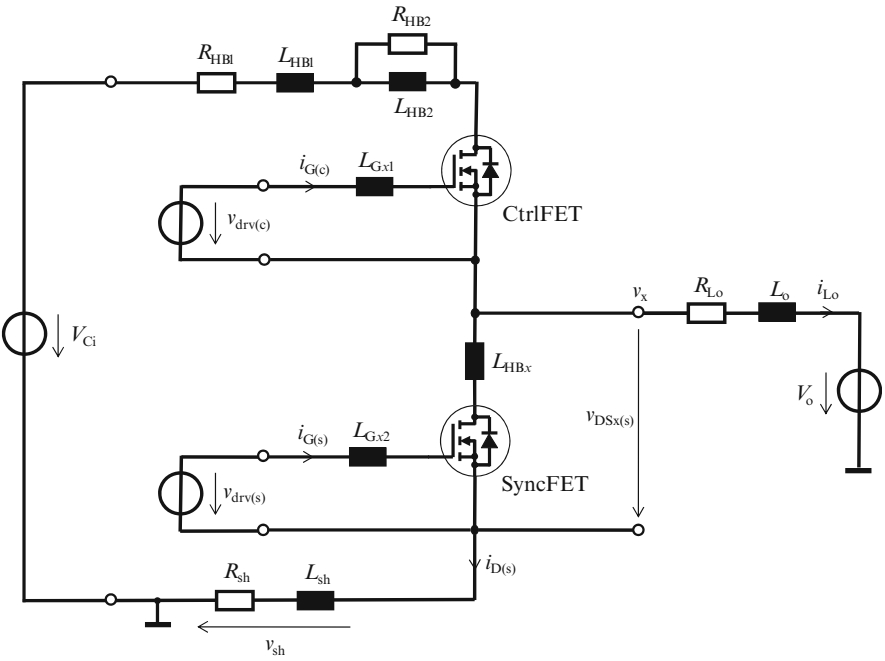

Fig. 2.32 Circuit model of a synchronous buck converter prototype for the validation of the proposed power MOSFET model. Extracted values: $R_{Lo} = 4.3\ \text{m}\Omega$ (total inductor + PCB), $L_o = 1$ µH. See Fig. 2.28 for the rest of the component values

In this arrangement, simulation results of the switch node voltage, gate currents, SyncFET drain current, and output inductor current waveforms are compared to their corresponding experimental waveforms.

Most of the measurements are performed with a digital oscilloscope and a number of high bandwidth differential probes. Steady-state switching signals are sensed corresponding to gate drive voltages $v_{drv(c)}$ and $v_{drv(s)}$, input and output voltages V_{Ci} and V_o, and switched node voltage v_x. Additionally, gate currents $i_{G(c)}$ and $i_{G(s)}$ as well as drain current $i_{D(s)}$ are monitored by voltage measurements across shunt resistors in the respective gates and half-bridge paths. Particularly, the SyncFET drain current shunt is modeled by means of resistor R_{sh} and parasitic inductor L_{sh}. The latter represents the ESL of the shunt device. Since the induced voltage across such inductance may be substantial during the switching times, its contribution must be subtracted from the measured voltage across the shunt in order to determine the correct magnitude of the current.

On the other hand, measuring output inductor current i_{Lo} may be alternatively realized with the use of transformer current probes since the relatively high inductive path of the output inductor allows the inclusion of clip-and-probe type

of sensors. In these experiments, a 500 MHz DC current probe is conveniently clamped around the leads of the output coil to measure i_{Lo}.

Part of the validation process consists in evaluating the ability of the model to predict the switching performance of two commercial low-voltage power MOSFETs (SyncFET PH3330L and CtrlFET PH8030L from NXP semiconductors). The sample parts used in the experiments were previously characterized and modeled according to the methods presented in Sect. 2.1.

The prototype circuit is operated at 1 MHz switching frequency, 12 V input voltage and 1.5 V output voltage, unless otherwise specified. The ambient temperature operation is $\sim$30°C and uniform throughout the PCB and components thereon. This temperature level corresponds to that of the MOSFETs characterization conditions, which is maintained throughout the experiments by operating the converter only for a limited number of switching periods necessary to perform noise-reduced-by-averaging readings in steady-state operation.

Figures 2.33 and 2.34 attest the accuracy of the model to precisely reproduce the switched node voltage and SyncFET drain current for a 10 A load current and 7 V input voltage. The model predicts the high ringing caused by the influence of the large half-bridge loop inductance, which is over 3.5 nH. The 100 mΩ shunt resistor for the SyncFET drain current sense contributes significantly to the rapid damping of such oscillation. The simulated output inductor current also matches the experimental data, which presents low ripple, thereby simplifying the loss calculations of the inductor losses later on.

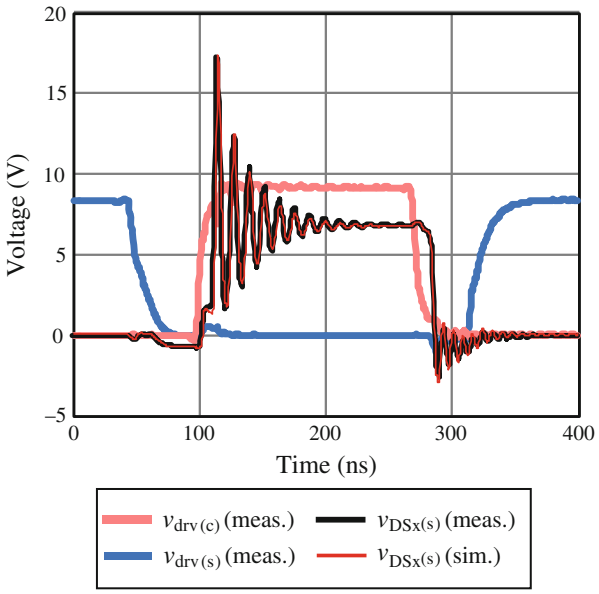

Fig. 2.33 Measurements and simulations of converter voltage waveforms. Switch node leading and falling edge (FE) transitions

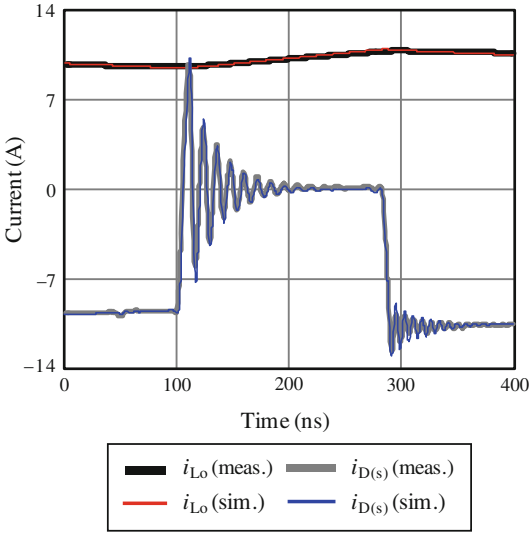

Fig. 2.34 Measurements and simulations of converter current waveforms. Switch node leading and FE transitions

A more detailed assessment of the model performance in terms of switching transient predictions is provided in Figs. 2.35–2.39. In Fig. 2.35, switch node LE transients are evaluated for various dead times. The strong impact of this driver parameter observed on the measured waveforms is precisely predicted by the model, even in cases of fast switching speeds leading to current commutations around 3.6 A/ns and RR peaks of 8 A. This gives strong credit to the basis of the model approach established by the superposition of responses from individually represented device characteristics.

Further proofs of the correct applicability of this principle is provided in Fig. 2.36, which shows matching waveforms of unsought switching effects like shoot-through and ABD.

Additional comparisons of the switched node LE transition are given in Fig. 2.37, from where it can be acknowledged that measured responses to variations of the load current as well as CtrlFET gate voltage are consistently reproduced in the simulator.

Similar performance predictions are deduced from evaluations of switch node FE transients. Figures 2.38 and 2.39 show how simulation and experimental waveforms match up well for a number of test conditions, which include variations of the CtrlFET gate voltage as well as the input voltage.

A detail description of the observed phenomena will be presented in the next sections based on simulation results of the converter operation.

The proposed model can also be harnessed for the purpose of quantifying and analyzing power losses. Loss predictions are assessed by means of carrying out power measurements of the test circuit. In this study, and in order to avoid excessive

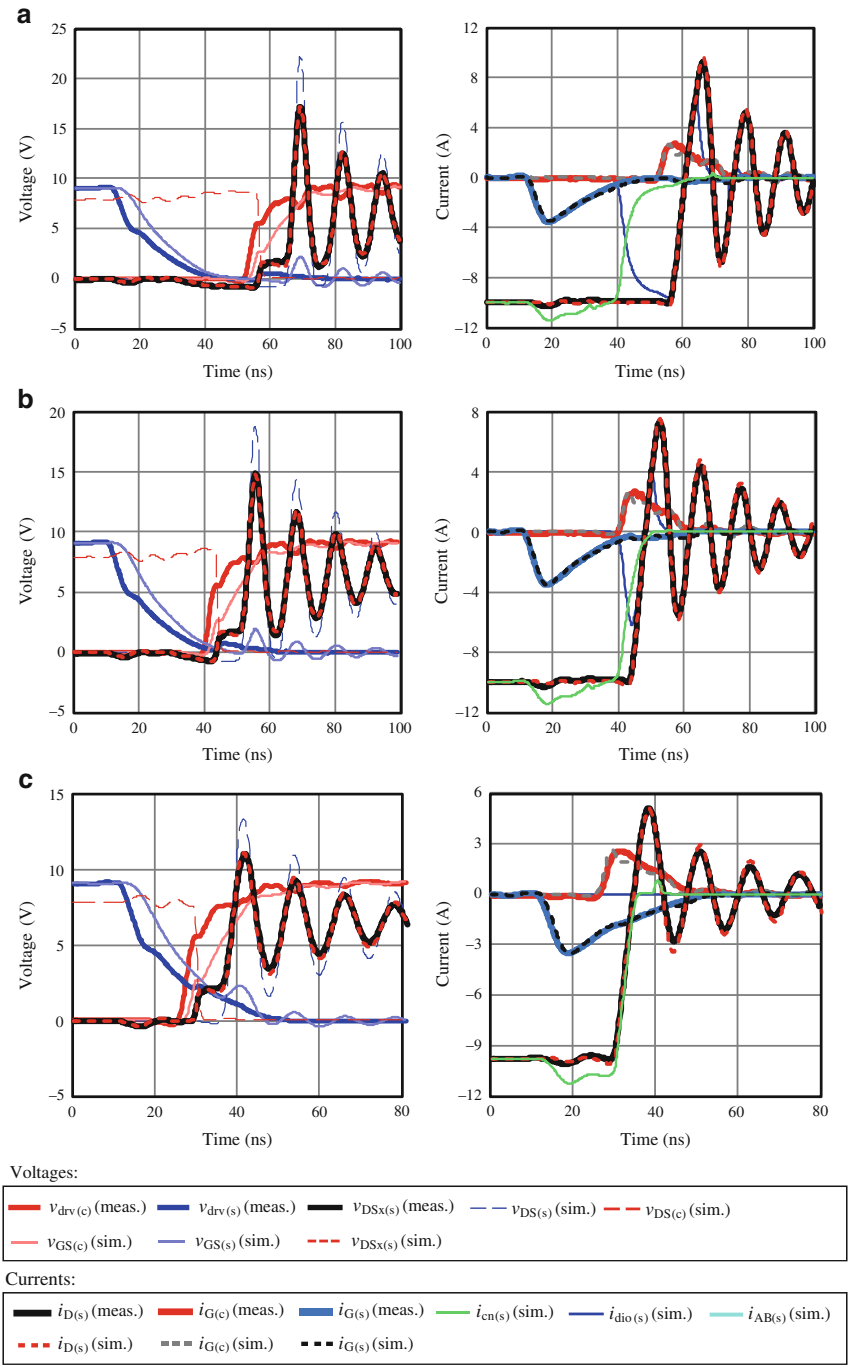

Fig. 2.35 Measurement and simulation waveforms of a SRBC test board. Switch node leading edge (LE) transient. Variation of dead time: (**a**) long dead time with RR, (**b**) moderate dead time with reduced RR, (**c**) short dead time with no RR

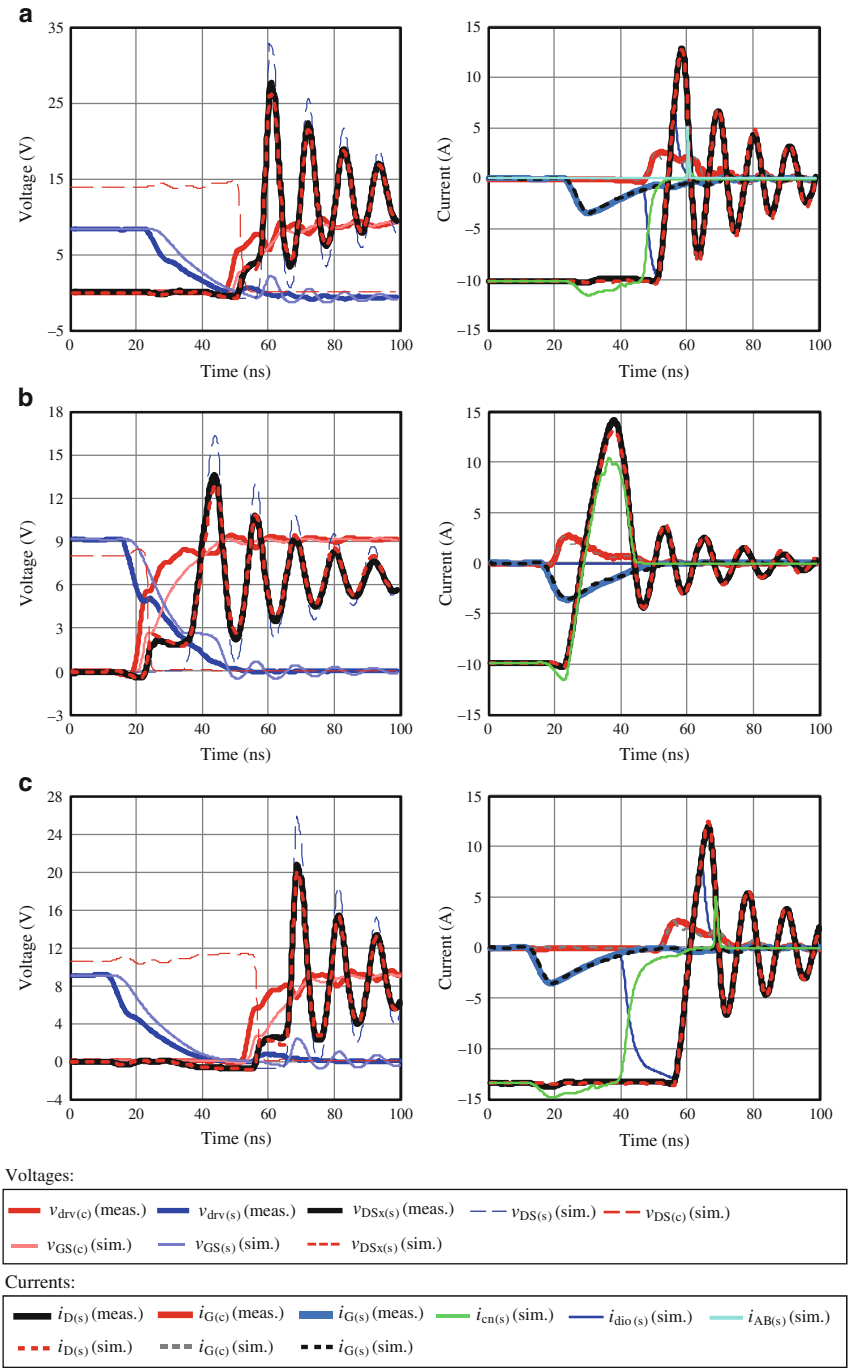

Fig. 2.36 Measurement and simulation waveforms of a SRBC test board. Switch node LE transient. (**a**) Avalanche breakdown (ABD); (**b**) Shoot-through due to short dead time; (**c**) SyncFET gate bounce (GB) shoot-through

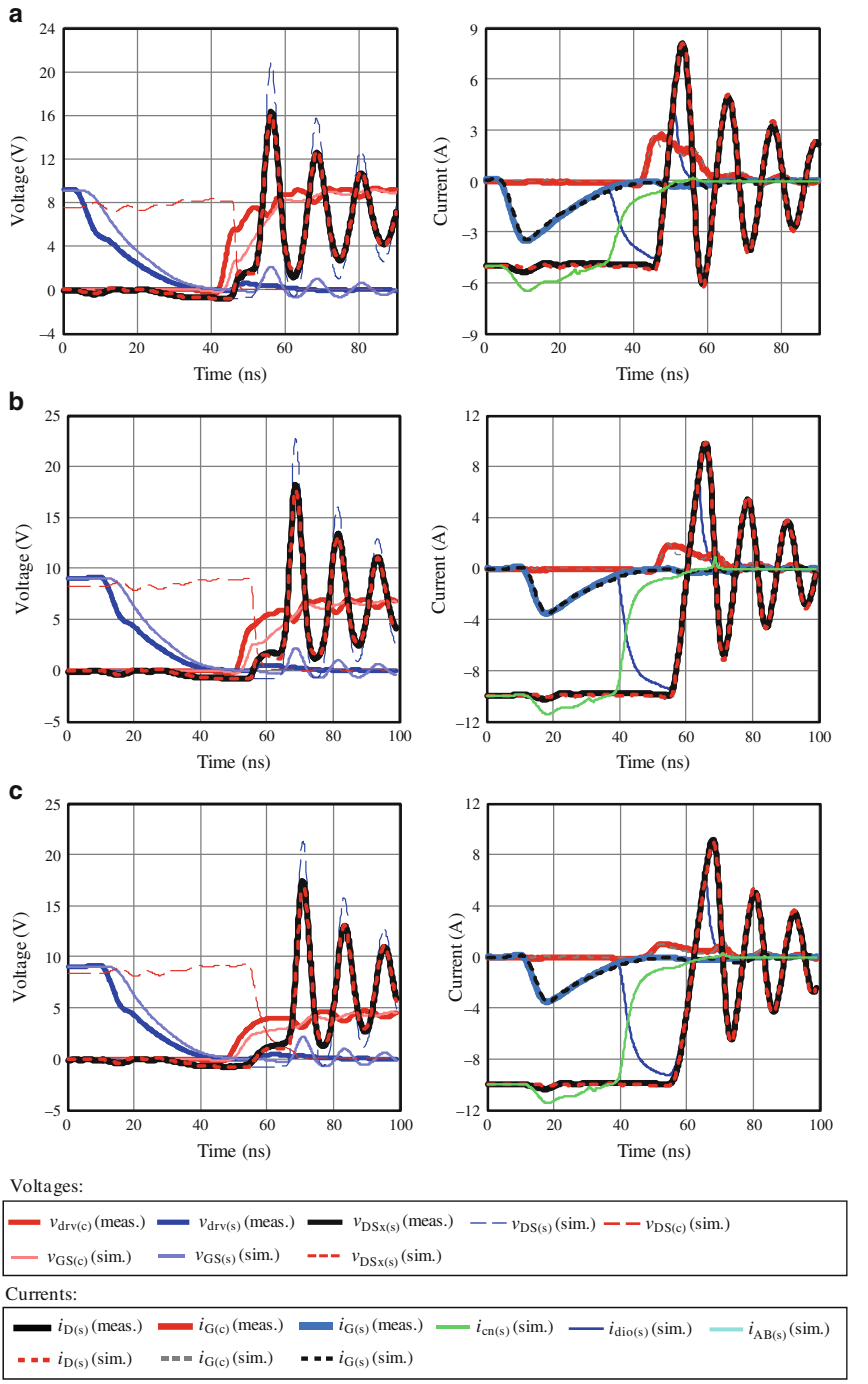

Fig. 2.37 Measurement and simulation waveforms of a SRBC test board. Switch node LE transient. (**a**) Moderate load current; (**b**, **c**) variation of CtrlFET gate voltage

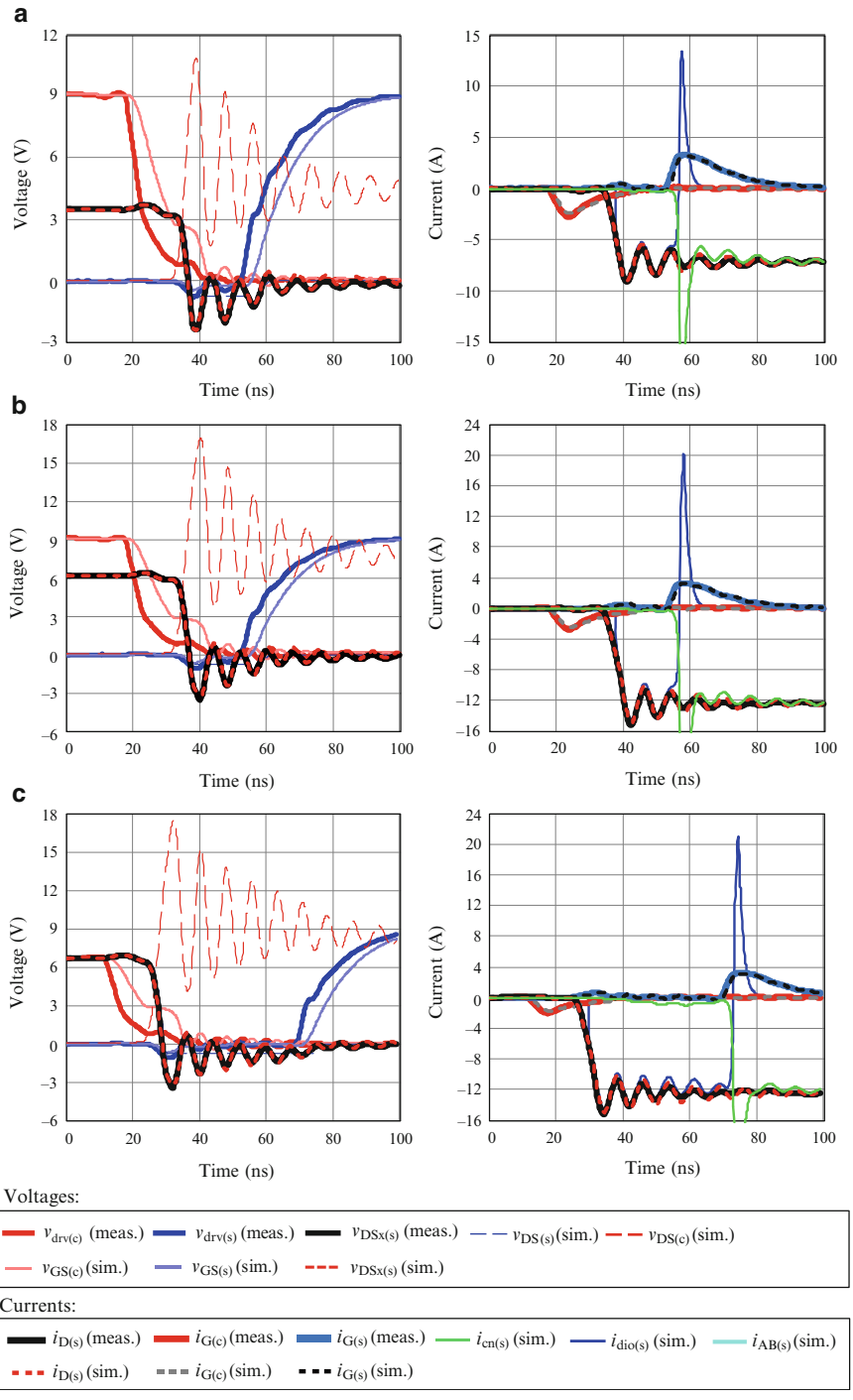

Fig. 2.38 Measurement and simulation waveforms of a SRBC test board. Switch node FE transient. (**a**, **b**) Variation of input voltage; (**b**, **c**) variation of gate voltage

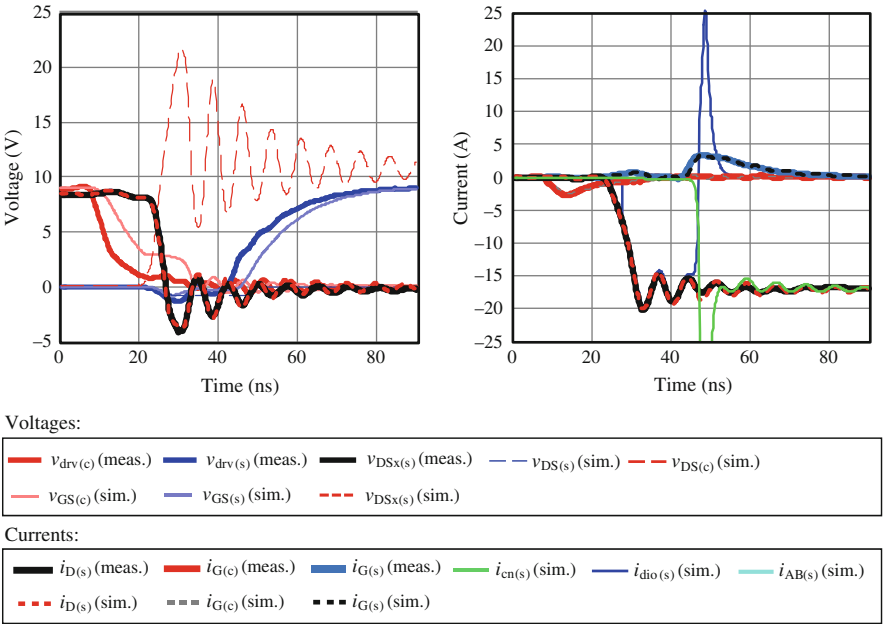

Fig. 2.39 Measurement and simulation waveforms of a SRBC test board. Switch node FE transient. Example of fast switching turn-off

losses, the shunt resistors (i.e., R_{sh} from Fig. 2.28) are removed from the circuit. The remaining resistance in the shunt path at 1 MHz is estimated in ∼1.5 mΩ, whereas ESL L_{sh} reduces from 170 to 70 pH. This in turn translates in faster switching times and a lower damping of the switching node ringing compared to the waveforms of Figs. 2.33 and 2.34, as it can be observed from Figs. 2.40 to 2.42 corresponding to the waveforms at 21 A load current and 12 V input voltage. A close look at Fig. 2.41 reveals the good agreement between experimental and simulated waveforms of voltage $v_{DSx(s)}$, thus providing evidence of the model's capability to predict switching behavior under realistic high current, high frequency operating conditions.

The total power consumption is measured at the voltage supply of the gate drivers and converter input. The losses of the input inductor and interconnection cables are also accounted for. The resulting magnitude is combined with the additionally measured output power in order to determine the efficiency of the converter circuit.

Simulated power losses are readily obtained from the steady-state switching waveforms. Additional losses in the driver ICs are estimated from datasheet information. Losses in the input filter capacitors also need to be taken into account. These are basically calculated from the equivalent circuit of Fig. 2.26 and the simulated CtrlFET drain current.

Figure 2.43 compares simulated and measured results of the converter performance for a conversion rate of 12/1.5 V at 1 MHz. The good agreement between the

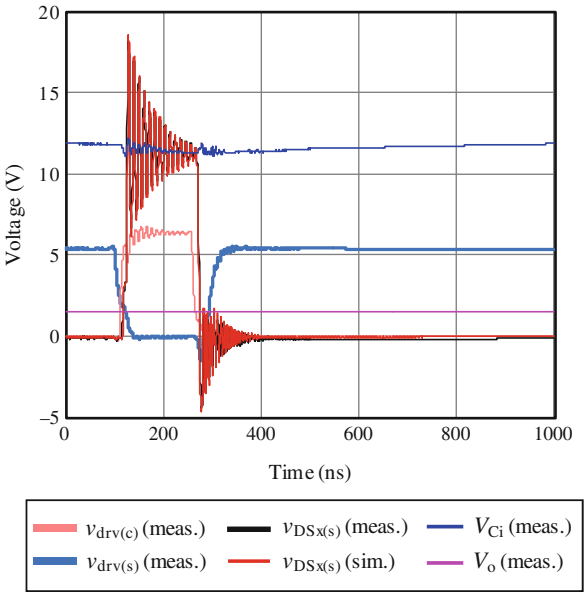

Fig. 2.40 Simulated and measured steady-state voltage waveforms of a SRBC test board

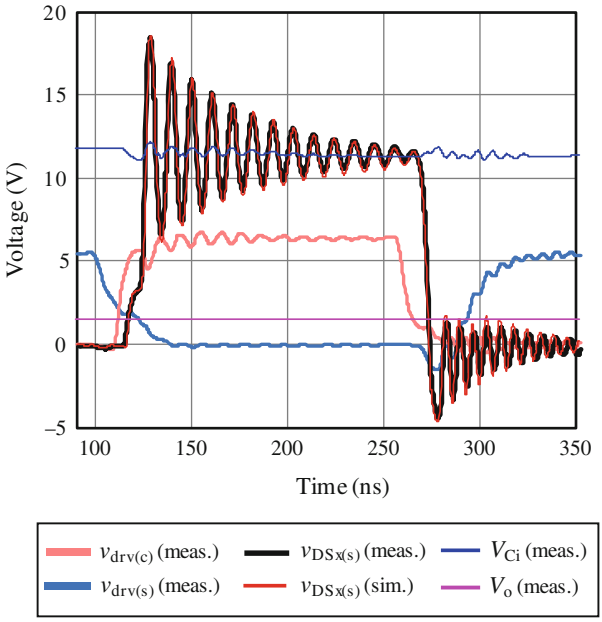

Fig. 2.41 Simulated and measured steady-state voltage waveforms of a SRBC test board. Details of transient response corresponding to waveforms of Fig. 2.40

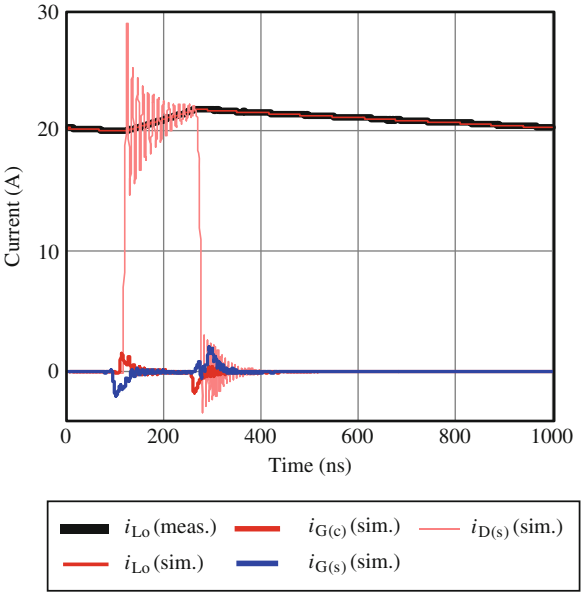

Fig. 2.42 Simulated and measured steady-state current waveforms of a SRBC test board

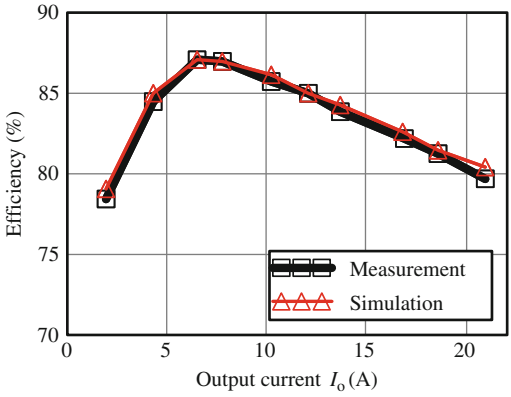

Fig. 2.43 Measured and simulated efficiency (12–1.5 V) of a SRBC test board. Junction temperature operation of the MOSFETs is forced to be 30°C (ambient temperature) in the entire load range

two curves in the entire load range pitches the accuracy of the MOSFET model to a level comparable to device physics simulations, with the additional advantage of the model to enable rather advanced studies on circuit analysis.

Total losses may readily be broken down into loss locations, as shown in the plot of Fig. 2.44. The curves show that major contributions are the heat generated in the power MOSFETs, with similar contributions of the CtrlFET and SyncFET at the highest load range. The significant loss contribution of the PCB is attributed to the rather long tracks of the layout design necessary to accommodate the shunt resistors and probing devices. The thickness of the copper tracks is only 40 µm

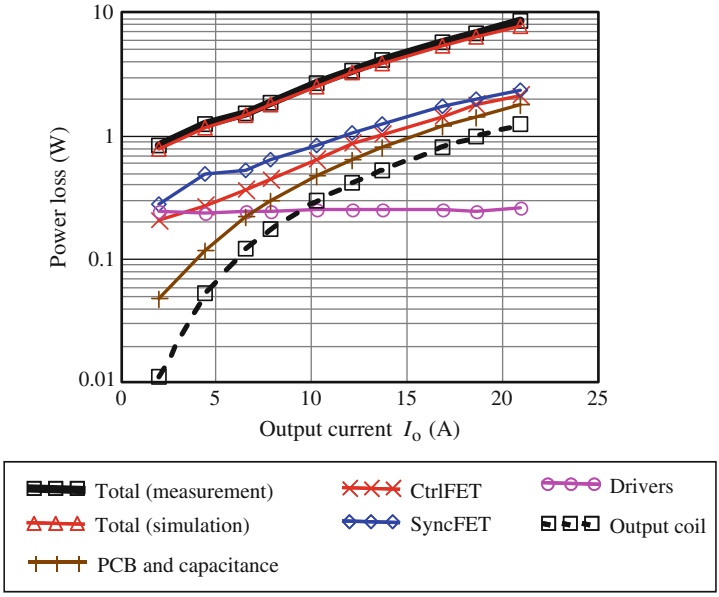

Fig. 2.44 Total and loss breakdown corresponding to efficiency curve of Fig. 2.43

so as to facilitate the soldering of parts, a task that needs to be performed rather frequently for the evaluations of multiple MOSFET technologies. Another significant loss contributor is the output inductor, which is attributed to a DC ESR of ~2.8 mΩ (i.e., the largest portion of the total R_{Lo} from Fig. 2.32). For the characteristics of the power choke, all other inductor losses are negligible.

A yet more rigorous power loss validation will be performed later on in the next chapters with the use of dedicated test boards for loss analysis. In these experiments, the contribution of the power MOSFETs will be predominant, thus allowing for a more accurate assessment of the model predictions.

Focusing the attention on the power MOSFET losses, Fig. 2.45 shows the simulated loss energy evolution of the two devices within a switching cycle under two different load currents. A couple of conclusions can be directly drawn from such pattern behavior. First, at high loads, CtrlFET turn-off loss predominates. And second, the CtrlFET turn-on induces some sort of losses in the SyncFET, likely attributed to either shoot-through or ABD. An examination of these and other relevant loss mechanisms is provided in the next section.

2.5 Analysis of Switching Behavior

This section exploits the developed models to study switching phenomena of power MOSFETs. The analysis aims at identifying the mechanisms of power losses under realistic operating conditions. Once determined and understood, the quantification

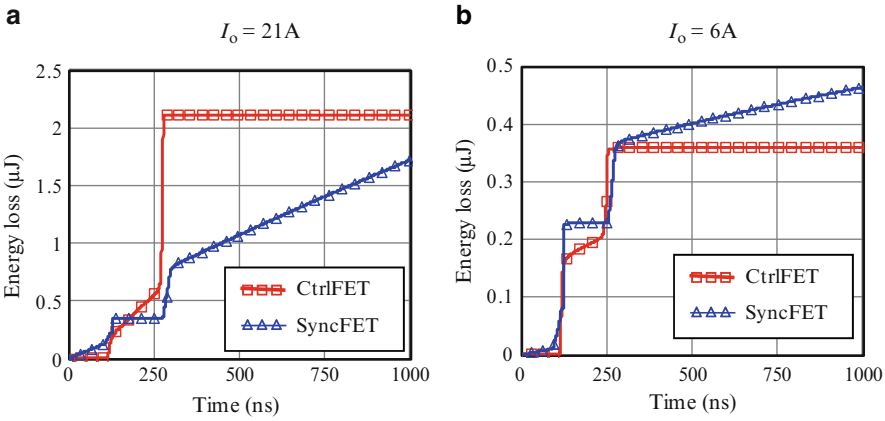

Fig. 2.45 Simulated energy loss profile at two different load currents corresponding to the estimated power losses of Fig. 2.44 (a) load current equals 21A, (b) load current equals 6A

of their effects will be consistently deduced from a method of loss separation, which is extensively described in Appendix D.

The methodology of analysis will be illustrated with three case examples that may be representative of VR applications. The first example will serve as basis for describing fundamental switching phenomena as well as identifying and quantifying loss mechanisms. Results of the loss quantification will lead to the identification of performance improvement options, which will be briefly examined.

The second case example will be applied to illustrate the strong interaction between complex loss mechanisms and the device characteristics. Special emphasis is given to the impact of RR and shoot-through-related losses with regard to the body-effect in power MOSFETs.

In the third illustration, losses are explored in a DrMOS compatible multichip module to demonstrate the importance of RR and its repercussion on other loss mechanisms such as ABD and gate bounce (GB) shoot-through.

2.5.1 Loss Breakdown

Table 2.4 lists specific parameter values of VRs for a laptop application. Corresponding simulated steady-state switching waveforms of one of the VR phases are shown in Fig. 2.46. As already observed in Fig. 2.45, the energy loss curves give again clear signs of significant losses occurring during the switching times. Unlike the losses in the ON conduction times, a thorough examination of the switching behavior is required in order to understand the mechanisms causing such sudden loss increase. This is the main purpose of the following subsections, which provide a comprehensive description of nanosecond-scale switching behavior as well as the identification and quantification of related loss mechanisms.

Table 2.4 Relevant parameter values of a case example to illustrate switching loss mechanisms. Other parameter values not shown are typical of VRs for laptops

General specifications	$V_{in} = 19$ V, $V_o = 1.5$ V, $I_o = 20$ A (max. per phase)	
Power MOSFETs	SyncFET	Trench MOSFET technology, 8.6 mm^2 active die area, LFPak
	CtrlFET	Trench MOSFET technology, 3.6 mm^2 active die area, LFPak
Gate drivers	SyncFET	Driving voltage: 0–5 V, 1.2 Ω turn-on resistance, 1.2 Ω turn-off resistance, 3.5 nH gate inductance turn-on, 2.5 nH gate inductance turn-off, 500 pH source inductance
	CtrlFET	Driving voltage: 0–5 V, 1.5 Ω turn-on resistance, 2 Ω turn-off resistance, 4 nH gate inductance turn-on, 2.5 nH gate inductance turn-off, 500 pH source inductance
Programmed dead times	Switch node LE: 30 ns, switch node FE: 30 ns	
Input/output filters	Total half-bridge inductance: 2.8 nH, $F_s = 300$ kHz, output inductance ripple current: $0.4I_o$	
Temperature operation	75°C uniform throughout the entire switched circuit	

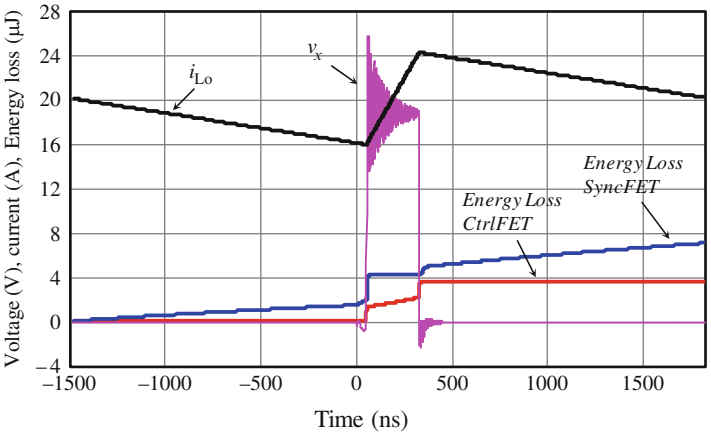

Fig. 2.46 Simulated switching period of a SRBC for laptop VRs

2.5.1.1 Switching Time Subintervals

Figures 2.47 and 2.48 show detailed switching waveforms of the switch node leading and FE transients corresponding to the simulation of Fig. 2.46. From the nature of the converter switching operation in continuous conduction mode, the switching period may be divided into the following time intervals:

– Dead time intervals t_0–t_1 and t_7–t_8 (DT): During the switch node LE transition, interval DT is defined between the FE of driving voltage $v_{drv(s)}$ and the beginning of CtrlFET conduction. Reversely, DT at the switch node FE transition starts as soon as the CtrlFET gate voltage falls below V_{TH}, and ends when $v_{GS(s)}$

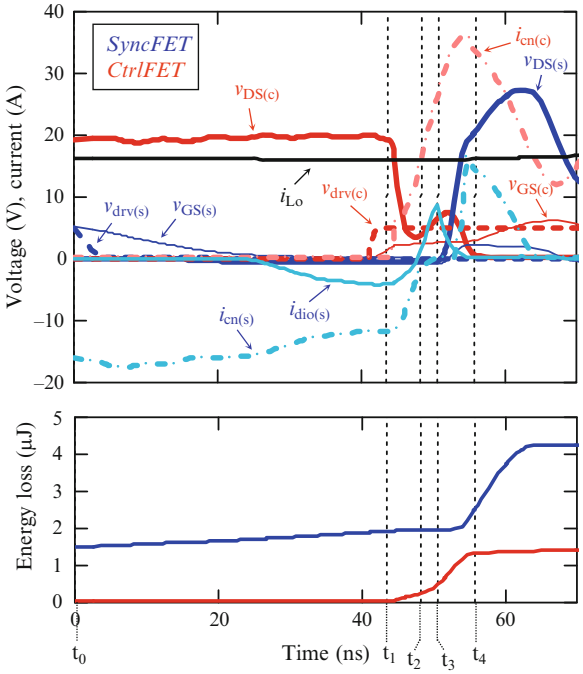

Fig. 2.47 Switch node LE transition of simulation of Fig. 2.46

reaches 90% of the ON state driving voltage. Note the difference between the definition of DT and the programmed dead times of the controller.

– Current hard-switching intervals t_1–t_2 and t_6–t_7 (CHS): It defines the di/dt switching transient. At the LE phase, CHS starts as soon as CtrlFET turns on, and ends when the SyncFET drain current reaches zero. CHS at the FE transition starts when the drain–source voltage across the SyncFET reverses and ends as soon as CtrlFET blocks. By this definition, CHS at the FE phase may not be present in a fast switching condition where the CtrlFET blocks before the SyncFET body diode is forward biased.
– Reverse recovery intervals t_2–t_3 (RR): It may occur at the LE transition due to reverse conduction of the SyncFET body diode. By definition, it starts at the end of the CHS interval and ends when the body diode reverse current reaches a maximum. The RR interval at the FE phase is not considered.
– Voltage hard-switching intervals t_3–t_4 and t_5–t_6 (VHS): It corresponds to the Miller plateau interval of the CtrlFET. At the LE transition, it starts at the end of the RR interval, and ends when the CtrlFET gets into the ohmic region. At the FE transition, the VHS starts when CtrlFET enters the active region, i.e., when voltage v_x starts rising, whereas it ends when the SyncFET body diode is forward biased, i.e., CHS starts. By definition, the VHS in the LE phase may

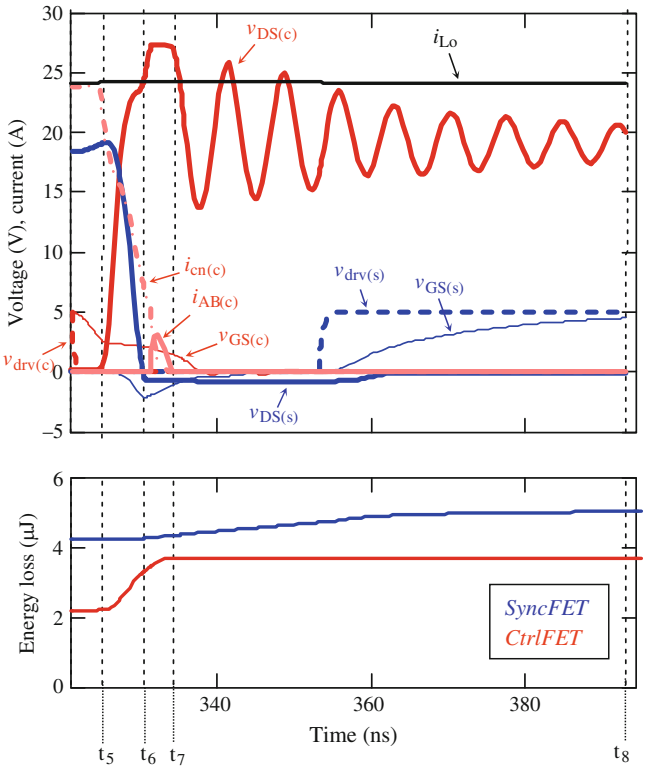

Fig. 2.48 Switch node FE transition of simulation of Fig. 2.46

not be present under conditions of fast switching where the CtrlFET enters ohmic region before v_x starts rising.

– Ohmic intervals t_4–t_5 and t_8–t_1: These are the intervals where the MOSFETs operate in the ohmic region.

The following subsections describe the switching operation of the MOSFETs during intervals CHS, RR, and VHS as these correspond to the switching periods of highest loss increase.

CHS and RR at LE Transition (t_1–t_3)

The CtrlFET takes over the output current at a speed (di/dt) that is determined by the characteristics of the gate drive and half-bridge circuits. Particularly, the source inductance plays a critical role as switching speed limiter. Namely, during the drain current rise the induced voltage across L_s feedbacks into the gate and lowers the driving charge current. A moderate di/dt may already produce significant losses in

the CtrlFET since the SyncFET drain–source voltage remains clamped by the action of the body diode and thus the voltage stress across the CtrlFET may be high. The increase of di/dt reduces the CHS time and the voltage stress across the CtrlFET by the induced voltage across the parasitic half-bridge inductances, which thus behave as turn-on snubbers. Accordingly, the absolute maximum di/dt is approximately given by the ratio of the input voltage to the total half-bridge loop inductance. At this switching speed the voltage stress in the CtrlFET is minimized.

The CtrlFET drain current may continue rising beyond i_{Lo} due to the RR and output capacitance charge of the SyncFET, which may cause significant overshoot currents.

The RR charge effectively extends the hard-switching time by the time defined by interval RR. RR results from body diode conduction during DT and CHS. The example of Fig. 2.47 corresponds to a moderate RR effect due to a significant SyncFET channel conduction in the third quadrant prior to the switching event.

VHS at LE Transition (t_3–t_4)

The voltage across the SyncFET starts rising rapidly. The speed depends not only on the CtrlFET driver conditions but also on the half-bridge inductance, input voltage V_{in} and the RR current waveform, particularly the maximum reverse peak current and the steepness of the recovery tail. The higher the latter two values are, the larger the overshoot voltage will be across the SyncFET.

A high dv/dt may cause the input capacitance of the SyncFET to be charged above the threshold voltage, thereby turning on the device sporadically and producing shoot-through, as illustrated in Fig. 2.47. This loss mechanism is referred to as GB. When GB occurs, the dv/dt dramatically reduces as the drain current finds an alternative path through the channel. If, on the other hand, the gate voltage does not reach the threshold level, the output capacitance of the SyncFET may rise further until avalanching the device. Due to the nonlinearity of C_{oss} the maximum peak voltage may reach values well above $2V_{\mathrm{in}}$ even at moderate switching speeds. The optimum turn-on switching speed is therefore conditioned by RR, avalanche, and GB.

The drain current through the SyncFET starts decreasing when the voltage across the output capacitance is sufficiently high. The negative di/dt induces a voltage across the source inductance of the SyncFET that tends to turn the device on. Thus, the L_{s} feedback worsens GB during the current decay.

The voltage across the CtrlFET decreases as the device is driven into the ohmic region. The stored energy in the output capacitance during this transient is mostly dissipated into the channel of the device. This current adds to i_{Lo}, C_{oss}, and RR currents from the SyncFET. Thus, although the voltage stress across the device may be lower than V_{in} at the beginning of the interval, the channel conducts a current higher than i_{Lo}.

VHS at FE Transition (t_5–t_6)

The output capacitances of both MOSFETs perform as turn-off snubbers since current i_{Lo} is shared between the CtrlFET channel and these capacitances. The stored energy in the SyncFET is recovered as it is delivered to the load. The capacitance current increases with the switching speed, thereby reducing the current through the channel of the CtrlFET. The SyncFET C_{GD} discharge current may flow through C_{GS} causing the gate voltage to become negative, as shown in Fig. 2.48. This stored energy in C_{GS} is dissipated in the gate circuit.

CHS at FE Transition (t_6–t_7)

The stored energy in the inductances of the half-bridge path causes an over voltage stress in the CtrlFET during the current commutation, which may result in ABD.

2.5.1.2 Identification of Switching Loss Mechanisms

From the previous analysis, several switching loss mechanisms can be identified and classified as: Snubbed hard-switching (SHS), half-bridge charging (HBC), gate charging (GC), RR, GB, and ABD. The following provides a definition and description of each one of them.

Load Current Hard-Switching (or Snubbed Hard-Switching SHS)

Hard-switching appears as a forced commutation of the output inductor current loop produced by the action of the switches. Particularly, for continuous unidirectional energy transfer from source to load, ZVS cannot be inherently established in the CtrlFET by active rectification. In contrast, the CtrlFET controls the state of the switched node voltage as in a diode-clamped inductive load configuration, where the SyncFET performs the rectification function. Fundamentally, during the current commutation phase (di/dt phase), the voltage across the switched node remains unchanged by way of the SyncFET freewheeling path. Only when the output current is fully taken by the CtrlFET, the switch node is unclamped and the voltage across the device starts changing, thus leading to the dv/dt phase. Such operating condition implies high stress and losses in the CtrlFET for high voltage across the device is present when the full load current flows through it.

The switching behavior of the CtrlFET differs from the aforementioned principle when the half-bridge parasitic elements are taken into account. As described in the previous section, the half-bridge inductances reduce the voltage stress across the

device at turn-on, whereas it increases it at turn-off. Reciprocally, the output capacitances of the MOSFETs produce over currents through the CtrlFET at turn-on, yet they reduce them at turn-off. The MOSFET turn-on is therefore characterized by low voltage and high current, whereas the turn-off by low current and high voltage.

SHS-related loss accounts for a portion of the channel CtrlFET loss during the intervals CHS and VHS. This portion corresponds to the loss contribution of the input voltage and output (load) current components, and thus it disregards the contributions corresponding to both the overshoot current at turn-on (i.e., output capacitance and RR currents), and the overshoot voltage at turn-off (i.e., induced voltage across the half-bridge inductances), which are accounted for as different loss mechanisms.

Half-Bridge Charging (Both Capacitive and Inductive)

HBC is related to the losses produced by the output capacitances of the MOSFETs and the half-bridge loop inductances.

The SyncFET output capacitance is charged up from the input voltage supply at the LE transition, causing a resonant current flow in the half-bridge loop. The energy of the oscillation is dissipated in the parasitic resistances of the circuit.

The CtrlFET output capacitance further generates power losses in the Ctrl FET channel at the LE transient, when the device turns on. The energy dissipation corresponds to the stored charge in this capacitance prior to turn-on. The ringing produced in the FE phase is also related to the CtrlFET output capacitance, whose associated loss energy is accounted for.

Lastly, the stored energy in the half-bridge loop inductance is fully dissipated in the FE transition, mostly in the CtrlFET as it produces overshoot voltages capable of even avalanching the device.

Gate Charging

Power losses are produced in the resistances of the gate circuit at turn-on and turn-off. The induced voltage across L_s and the dv/dt across drain–source terminals further produce current in the gate, which contribute to the overall gate drive losses of each device.

Reverse Recovery

As described in the previous section, the RR enlarges the hard-switching interval by the time defined by times t_2 and t_3 from Fig. 2.47. Thus, the total power losses occurring in the half-bridge during this interval are considered RR related. Further losses result from the RR tail current during the subsequent intervals. The RR-related

losses in the CtrlFET channel might be particularly significant during the hard-switching intervals.

Gate Bounce

GB-related losses may occur in the LE phase due to a spurious turn-on of the SyncFET during the VHS and subsequent intervals. Both MOSFETs are affected by the shoot-through. Note that GB-related losses might also be produced in the FE transition due to a spurious turn-on of the CtrlFET.

Avalanche Breakdown

Due to the voltage overshoot, ABD may occur in both SyncFET and CtrlFET during the LE and FE transitions, respectively.

A summary of all identified loss mechanisms and corresponding abbreviations is provided in Table 2.5.

2.5.1.3 Loss Quantification

The assessment of the above identified loss mechanisms involves assignment of quantities in a meaningful and systematic manner. This may be accomplished by regarding the losses in every dissipative element of the MOSFET model as the individual contribution of the different current loops of the switched circuit, each of which may be associated to one or more loss mechanisms at a given time instant. The way in which this is carried out is described in detail in Appendix D. The method allows breaking down the power losses by loss mechanisms, as illustrated in the example of Fig. 2.49.

The loss breakdown provides a powerful means to determine major loss contributions, thus aiding the identification of potential improvement options. In the given example, the major contributor is the ON conduction loss of the output

Table 2.5 Summary of loss mechanisms and abbreviations

Loss mechanism	CtrlFET	SyncFET
Load current ON conduction	OnCIoc	OnCIos
Load current hard-switching	SHS	–
Half-bridge capacitance charging	HBCc	HBCs
Half-bridge inductance charging	HBC(L)	
Gate charging	GCc	GCs
Reverse recovery	–	RRs
GB shoot-through	GBc	GBs
Avalanche breakdown	ABDc	ABDs

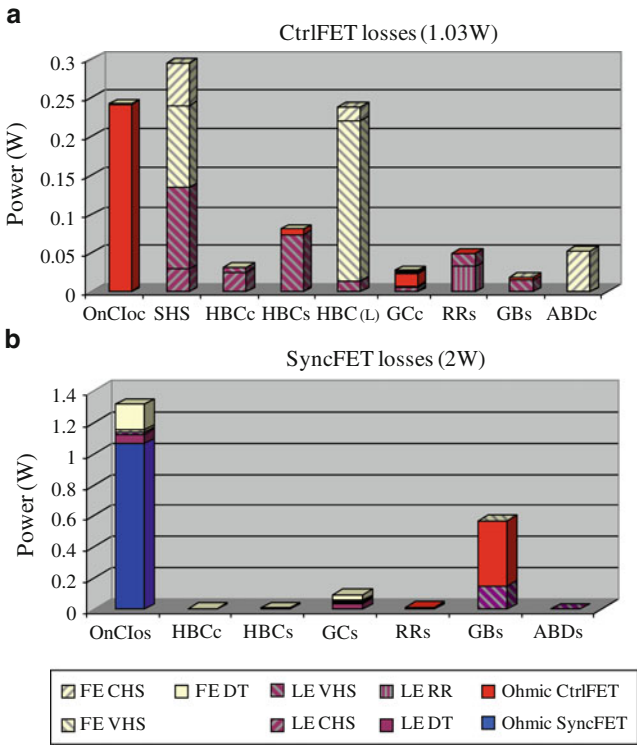

Fig. 2.49 Quantification of loss mechanisms corresponding to simulation of Fig. 2.46 (a) CtrlFET losses, (b) SyncFET losses

current in the SyncFET, which accounts for the 38.5% of the overall power dissipation in the circuit. Most of the losses occur during the ohmic time interval of the device. A significant portion though is caused due to body diode conduction during the FE dead time interval. The difference in power dissipation between LE and FE dead times is mainly attributed to the output current ripple, i.e., the output current during FE is about 8 A higher than during LE.

The second most relevant loss mechanism is GB, which accounts for 18.5% of the total losses. Note that most of these losses occur in the SyncFET.

SHS is on the other hand a predominant loss mechanism in the CtrlFET, followed by the ON conduction of the output current. Further significant losses are produced by the half-bridge loop inductance in the FE transient. The voltage stress in the CtrlFET is such that the device avalanches. The heat produced by this latter mechanism though is not large compared to the channel losses (i.e., HBC(L)). In the LE phase, the amount of output capacitance current and RR-related losses are moderated and primordially occur in the CtrlFET. GC is a minor contributor in both devices.

According to the above observations, measures may be taken to effectively improve the circuit performance. Clearly, a first major action is to reduce the

SyncFET ON conduction losses by, for instance, increasing the die size of the device. If the maximum chip size cannot be further increased in the package, parallel discrete devices may be used, instead.

In addition, the small contribution of gate charge loss suggests the increase of the SyncFET gate voltage to further reduce the ON channel resistance.

Another potential improvement target is to reduce SyncFET GB by either reducing the gate impedance or the C_{GD}/C_{GS} ratio or both. Achieving any of them without increasing C_{GD} allows faster switching, thus further enhancing switching performance. Note, however, that the reduction of GB may give rise to SyncFET avalanche due to an increase of the LE voltage overshoot across the device. Thus, the avalanche voltage level should be increased. As a rule of thumb, the ABD level should be about $2.5V_{in}$.

Another gate drive aspect observed in the loss chart is the insignificance of the gate charge loss compared to the channel losses, which suggest that the optimum gate voltage for the switches may be higher than 5 V in this particular case.

Finally, the reduction of FE CtrlFET losses may be achieved by increasing the output capacitance of the CtrlFET, thereby enhancing the turn-off snubber function.

An analysis of variations of these parameters yields a more concrete proposal of improvement options listed in Table 2.6. Note that the MOSFET dies are artificially scaled by means of parameter A_{die} from (2.1), (2.2), and (2.14). Likewise, each model parameter may be individually parameterized. The loss profiles of Fig. 2.50 show the effectiveness of the applied measures. The overall power loss is reduced by 0.85 W, which translates into a conversion efficiency increase from 90.6 to 93%.

2.5.2 *Influence of the Body-Effect on Switching Losses*

Gate bias refers to an offset voltage at gate-source during the OFF state of the MOSFET (voltage V_{drvn} from Fig. 2.22). Although such gate bias does not alter the ON state conduction losses, it may influence the transient behavior regarding RR, ABD, and GB by virtue of the MOSFETs body-effect.

Table 2.6 Proposed modifications of the SRBC parameters corresponding to case example of Table 2.4

Power MOSFETs	SyncFET	Three parallel discrete (LFPak) Trench MOSFETs of 8.6 mm^2 active die area each Reduction of C_{GD} by factor of 3 Increase of avalanche voltage by 13 V Increase of ON resistance by factor of 2 (compromised in order to allow for points 2 and 3)
	CtrlFET	Increase of C_{DS} by factor of 3
Gate drivers	SyncFET	Increase of driving voltage: 0–8 V
	CtrlFET	Increase of driving voltage: 0–8 V

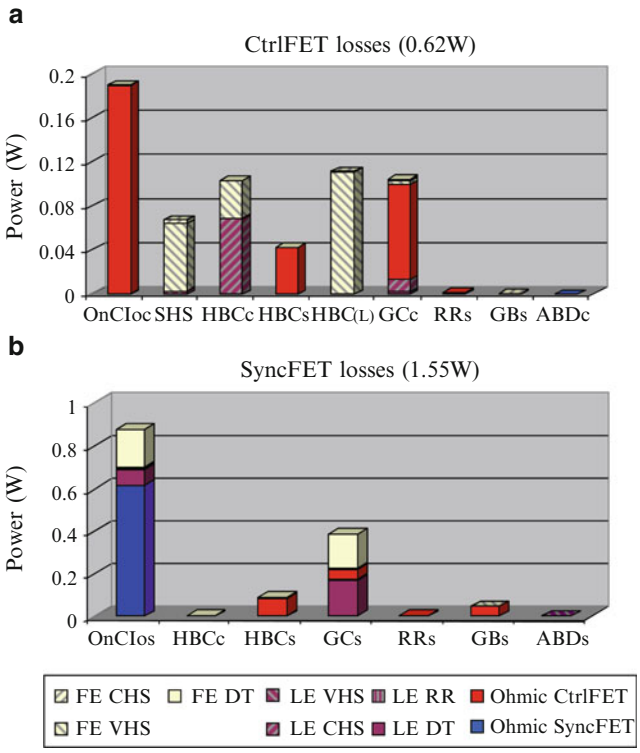

Fig. 2.50 Simulated loss breakdown of the laptop case example after applying proposed improvement options of Table 2.6 (a) CtrlFET losses, (b) SyncFET losses

To investigate this, the LE transient of the SRBC is analyzed by means of circuit simulations based on the proposed MOSFET model of Sect. 2.1. For the sake of highlighting the effects under consideration, a number of elements of the switched circuit are simplified. This is the case of the input filter, which is modeled with an ideal voltage source in series with an inductance. Since only the LE transition is simulated, the output filter and load is replaced by an ideal constant current source of value I_o. The gate driver circuits are represented by ideal trapezoidal voltage sources $v_{drv(c)}$ and $v_{drv(s)}$ in series with the gate parasitic elements and L_s.

Table 2.7 lists parameter values of the simulation setup, including the assignments for two cases discussed below (A, B). Parameter of variation in both cases is gate bias v_{drvn}. Note that the dead times are considerably long so as to ensure body diode conduction prior to CtrlFET turn-on.

Case A ($L_s = 0.5$ nH) deals with the impact of the gate bias on RR only. Increasing source inductance L_s in case B ($L_s = 2$ nH) raises the drain–source voltage $v_{DS(s)}$ in order to further introduce ABD and gate bouncing, which allows investigating their interaction with RR.

Table 2.7 Relevant parameter values of a case example for the analysis of the body-effect in switching transient behavior

General specifications	$V_{in} = 10$ V, $I_o = 10$ A	
Power MOSFETs	SyncFET	Trench MOSFET technology, 8.6 mm^2 active die area, LFPak (case A), and modified LFPak with $L_s = 2$ nH (case B)
	CtrlFET	Trench MOSFET technology, 3.6 mm^2 active die area, LFPak
Gate drivers	SyncFET	Driving voltage: v_{drvn} to $v_{drvn} + 5$ V, 1 Ω turn-on resistance, 0.4 Ω turn-off resistance, 2 nH series inductance
	CtrlFET	Driving voltage: 0–10 V, 1 Ω turn-on resistance, 0.4 Ω turn-off resistance, 2 nH series inductance
Programmed dead times	Switch node LE: 25–30 ns	
Input/output filters	Total half-bridge inductance: 1.2 nH (case A), 4.2 nH (case B) output inductance ripple current: 0 A	
Temperature operation	25°C uniform throughout the entire switched circuit	

Other parameter values not shown are typical of VRs for laptops

2.5.2.1 Impact on Reverse Recovery

Figure 2.51 shows simulations of a SRBC during the LE transition corresponding to the case A of Table 2.7 [16]. The six plots show voltages in the left column, whereas currents and cumulated loss power in the right column. Three gate bias values are considered as follows: $v_{drvn} = -1$, 0, and 1 V. Threshold voltage V_{TH} is 2 V.

The blue and red traces of the left plots show driver voltages $v_{drv(c)}$ and $v_{drv(s)}$, as well as resulting gate voltages $v_{GS(c)}$ and $v_{GS(s)}$ at the dies of the two transistors (bold traces). In all three simulations gate voltage $v_{GS(s)}$ reaches its OFF state value, i.e., bias voltage v_{drvn}, well before gate voltage $v_{GS(c)}$ starts rising. Usually, such sequence implies body diode conduction of the SyncFET. Gate voltage $v_{GS(c)}$ shows in all three cases the typical turn-on plateau, caused by the di/dt and dv/dt intervals. Only the amplitudes of switch node and die voltage v_x and $v_{DS(s)}$ show a strong response to the gate bias. The current waveforms of the right plots allow explaining this behavior. The bold traces show the total drain current $i_{D(s)}$, as well as the contributions of channel and diode $i_{cn(s)}$ and $i_{dio(s)}$. In case of the positive gate bias (still well below threshold), the current through the channel does not commutate to the body diode as a consequence of the body-effect. Accordingly, there is no sign of RR, and the current overshoot is substantially reduced, i.e., to as much as one-third compared to the case with negative gate bias $v_{drvn} = -1$ V. The reduction of the current overshoot in turn means less voltage ringing.

Although the body diode at zero gate bias still carries the full load current (the share of channel and body diode current strongly depends on the total current), RR is already much reduced compared to the transient at negative gate bias. Since the RR parameters are unchanged in both cases, it implies that a significant portion of RR current must freewheel internally through the channel already at $v_{GS(s)} = 0$ V.

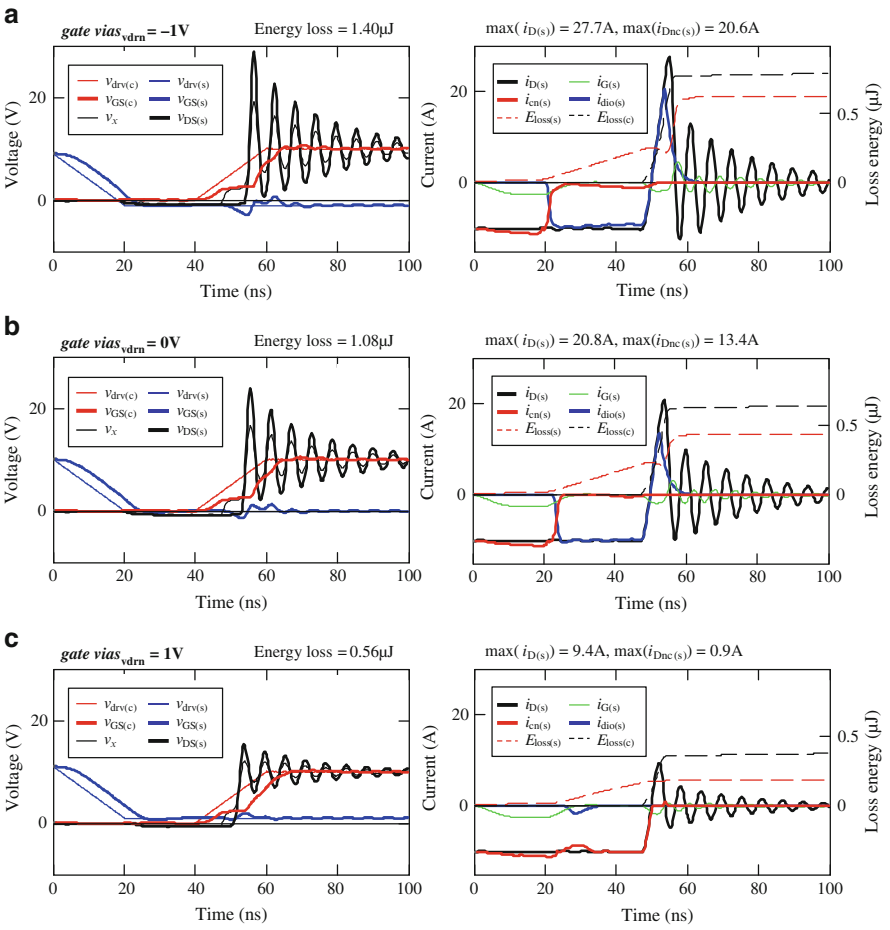

Fig. 2.51 Simulation of switch node LE switching transition. Parameters of Table 2.7 (case A, $L_s = 0.5$ nH) at various subthreshold gate bias values (a) Gate bias = −1 V, (b) gate bias = 0 V, (c) gate bias = 1 V

The dashed lines in the right plots represent the losses of both MOSFETs during the displayed switching transient ($E_{loss(c)}$, $E_{loss(s)}$). The decrease of the current overshoot leads to a significant decrease in losses (0.56 µJ at $v_{drvn} = 1$ V, compared to 1.4 µJ at $v_{drvn} = -1$ V). Because of the improvement in third quadrant conduction that the body-effect produces, the synchronous rectifier losses are also reduced at positive gate bias during the dead times.

From channel current $i_{cn(s)}$ and gate voltage $v_{GS(s)}$ waveforms at $v_{drvn} = 1$ V, it can be seen a slight shoot-through as consequence of GB, i.e., spurious turn-on of the channel as a result of the increased gate bias. For its importance, this is studied to a greater extent in the next section.

2.5.2.2 Impact on Gate Bounce

There are several sources of gate voltage fluctuations. Firstly, a dv/dt at drain–source terminals produces a gate current as a consequence of reverse transfer capacitance C_{rss}. Assuming a positive voltage ramp across v_{DS}, an initial gate voltage v_{drvn}, and an open gate, gate voltage v_{GS} varies according to the following expression:

$$v_{\mathrm{GS}} = \int_{v_{\mathrm{DS0}}}^{v_{\mathrm{DS1}}} \frac{C_{\mathrm{rss}}}{C_{\mathrm{iss}}} \mathrm{d}v_{\mathrm{DS}} + V_{\mathrm{GS0}}. \tag{2.38}$$

Figure 2.52 plots the results for three gate bias values and shows a strong dependence of GB on the bias, given by the crossings of the curves with the threshold voltage line V_{TH}.

A second cause for GB may be an inductive voltage drop at the source inductance due to a positive di/dt. This is illustrated in the simulation example of Fig. 2.53, where the source inductance of the SyncFET has been intentionally increased to highlight such effect. The curves clearly indicate that source inductance may potentially induce GB-related shoot-through. In contrast to the trends observed in Fig. 2.52, GB worsens at negative gate bias and virtually vanishes at positive v_{drvn}. This indicates the dominance of the di/dt-related influence on GB.

The increased inductive voltage drop across L_{s} may have an additional negative implication on switching losses due to ABD. Figure 2.54 plots the measured breakdown voltage vs. gate voltage, which shows, for the device under consideration, a decrease of the avalanche value as the gate voltage grows negative. Regarding both $v_{\mathrm{GS(s)}}$ and $v_{\mathrm{DS(s)}}$ at $v_{\mathrm{drvn}} = -1$ V from Fig. 2.53, worst-case conditions are given because peak drain–source and minimum gate-source voltage occur at the same time.

The total losses during the LE transition are lower in case B compared to case A, resulting from decreased losses in the CtrlFET due to the snubber effect of the higher source inductance (which may in turn increase losses at the FE transient). The SyncFET, however, again benefits from the positive gate bias, since RR is reduced.

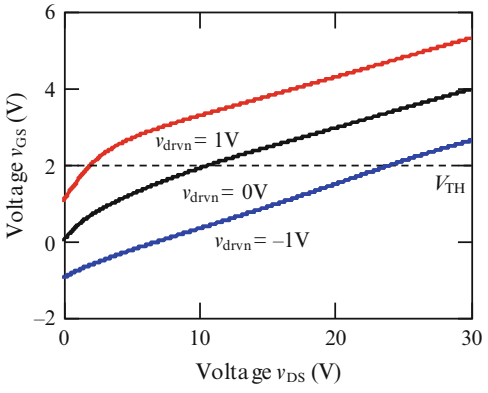

Fig. 2.52 Evaluation of (2.38). Comparison of various gate bias values with regard to GB caused by a dv/dt ramp at the drain–source terminals. The capacitance data refer to the characteristics shown in Fig. 2.18. Data refer to a 25 V logic level n-channel trench MOSFET at 25°C

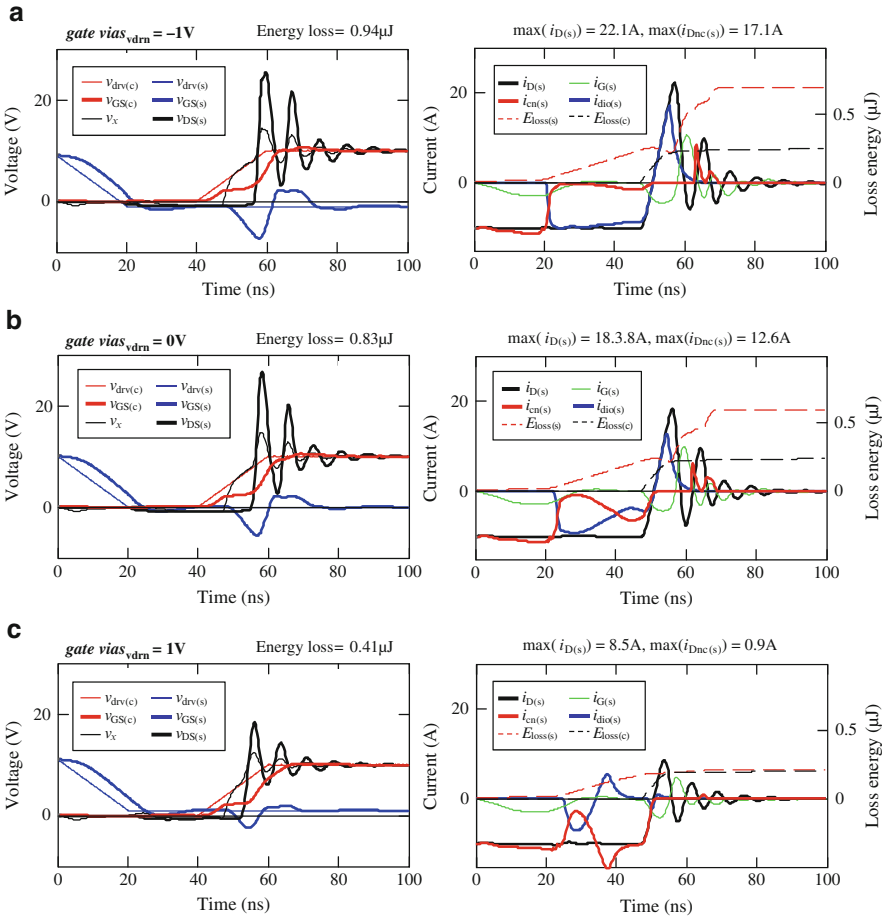

Fig. 2.53 Simulation of LE switching transition Parameters of Table 2.7 (case B, $L_s = 2$ nH) at various subthreshold gate bias values (a) Gate bias = −1 V, (b) gate bias = 0 V, (c) gate bias = 1 V

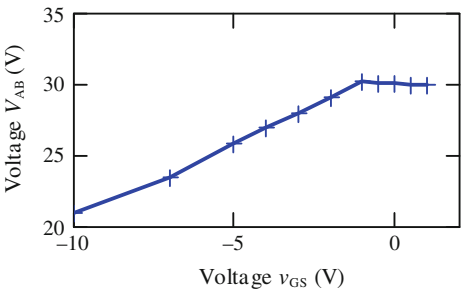

Fig. 2.54 ABD voltage as function of gate voltage. Measurement data of a 25 V logic level n-channel trench MOSFET at 25°C

The simulations at zero and positive gate bias further show that, during third quadrant operation, minor gate voltage variations may alter the drain current sharing between channel and body diode. In case of the positive gate bias of Fig. 2.53, RR occurs already during the dead time, which, however, cannot be observed if only total drain current $i_{D(s)}$ is monitored. This is not new as it was also manifested in the FE transitions of Figs. 2.38 and 2.39.

2.5.3 *Loss Analysis of a Multichip Module*

This section illustrates the use of the proposed MOSFET model to assess power loss and identify potential improvement options in a multichip powertrain module. The switched-circuit model is based on the IC PIP212-12M from NXP Semiconductors. Table 2.8 lists related parameter values relevant to the analysis. They refer to simplified representations of rather complex circuit models used for the gate drives, half-bridge layout and input filter. Note as well that some of the IC-related parameter values may not be accurate in correspondence with commercially available parts.

Parameter sweep simulations of the input filter inductance L_{HB}, CtrlFET gate resistance, and SyncFET RR peak have been carried out. The latter is possible by adequate adjustments of the coefficients from the RR model expression (see Sect. 2.1.2).

Figure 2.55 illustrates the impact that RR has on the SyncFET losses. The loss dependence is mainly attributed to channel losses at high $R_{G(s)}$ (Fig. 2.55a), and to ABD at low $R_{G(s)}$ (Fig. 2.52b). Further postprocessing of the simulated data

Table 2.8 Relevant parameter values of simulated MCM (PIP212-12M) unless otherwise specified

General specifications	$V_{in} = 12$ V, $V_o = 1$ V, $I_o = 30$ A (max. per phase)	
Power MOSFETs	SyncFET	Trench MOSFET technology, 25 mm^2 active die area
	CtrlFET	Trench MOSFET technology, 3.6 mm^2 active die area
Gate circuit	SyncFET	Driving voltage: 0–6 V, 1.2 Ω gate resistance, 2.5 nH gate inductance turn-on, 1.5 nH gate inductance turn-off, 100 pH source inductance
	CtrlFET	Driving voltage: 0–7 V, 1.7 Ω gate resistance, 3 nH gate inductance turn-on, 1.5 nH gate inductance turn-off, 100 pH source inductance
Package resistance (bond wires)	SyncFET	0.25 mΩ DC resistance (0.35 mΩ at 125°C)
	CtrlFET	1 mΩ at $F_s = 1$ MHz and $d = 0.08$
Programmed dead times	Switch node LE: 10 ns, switch node FE: 30 ns	
Input/output filters	Total half-bridge inductance (L_{HB}): 1.6 nH, $F_s = 1$ MHz, 150 nH output filter inductor	
Temperature operation	30°C uniform throughout the entire switched circuit	

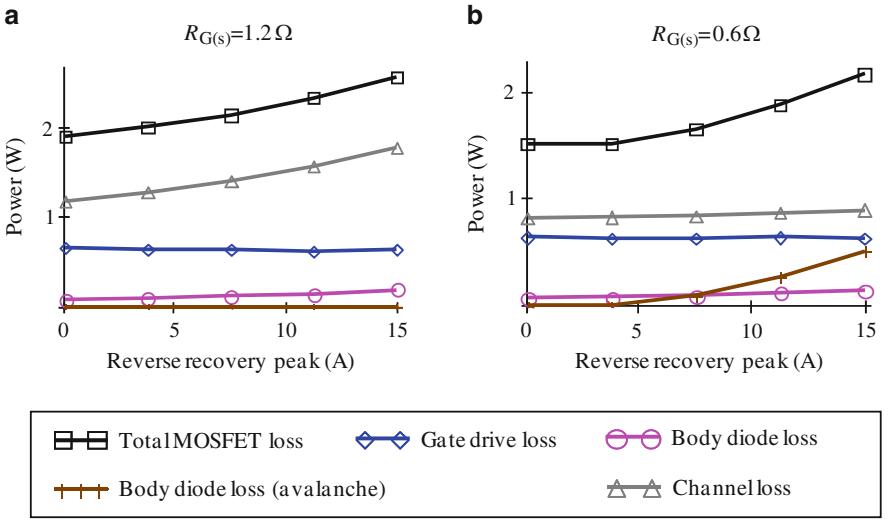

Fig. 2.55 SyncFET power loss as function of reverse recovery and various gate resistances with $L_{HB} = 3$ nH

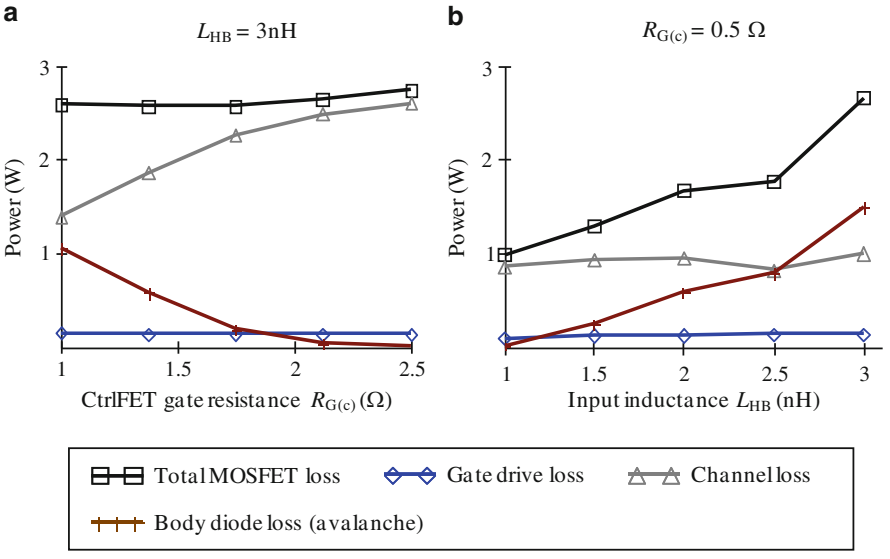

Fig. 2.56 CtrlFET power loss; (**a**) as function of CtrlFET gate resistance; (**b**) as function of total parasitic half-bridge loop inductance

yields the separation of power losses into loss mechanisms and time intervals, as shown in Fig. 2.56. Such a loss breakdown approach reveals that the increase of channel losses observed in Fig. 2.55a is mainly due to GB shoot-through (see Sect. 2.5.1.2).

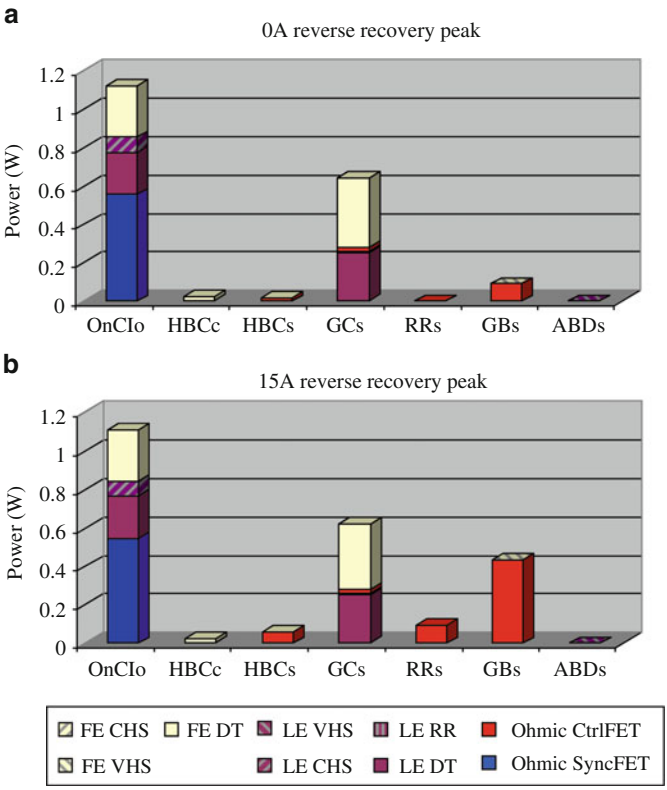

Fig. 2.57 SyncFET loss breakdown corresponding to simulations of Fig. 2.55a. See Table 2.5 for loss breakdown abbreviations (a) no RR, (b) 15A RR peak current

Figure 2.57a exemplifies that the increase of the CtrlFET switching speed may not always lead to an overall loss improvement, even though the gate drive loss may remain unchanged. That is, while the reduction of $R_{G(c)}$ increases the switching speed and thus minimizes hard-switching losses, it may also induce the ABD of the CtrlFET. This is observed in the loss bars of Fig. 2.58. Note that significant losses occur during the FE transition, which suggests the need for reducing L_{HB} to enable further significant improvements, as shown in Fig. 2.56b.

These results justify the implementation of an adaptive dead time control that effectively mitigates losses due to RR and related loss mechanisms. ABD, GB shoot-through, and RR represent major obstacles toward efficient fast switching. Their reduction is therefore essential to continue developing devices with lower Q_{Gt} and R_{DSon}. It suggests the need for refined figure of merits that take into consideration further insights of loss mechanisms in the application. Parameters involved in the optimization may be device related (e.g., Q_{rr}) and also circuit related (e.g., L_{HB}).

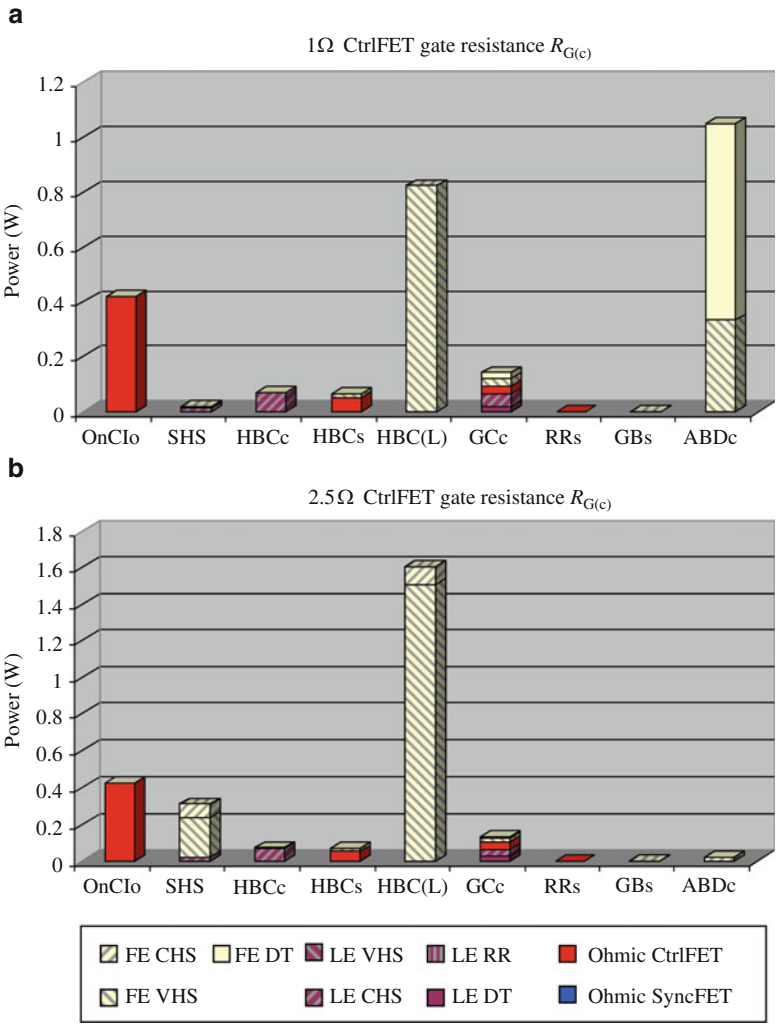

Fig. 2.58 CtrlFET loss breakdown corresponding to simulations of Fig. 2.56a. See Table 2.5 for loss breakdown abbreviations (a) 1 Ω gate resitance, (b) 2.5 Ω gate resistance

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