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Introduction to Nonlinear Circuits and Networks

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Dedicated to Robert M. Fano, Lan J. Chu
and Richard B. Adler

Foreword

To be written

Dr. Leon O. Chua

Preface

The purpose of this course-based text book is to revisit classic concepts in nonlinear circuit theory, from an introductory standpoint:

1. The book is completely self-contained and does not assume any prior knowledge of circuit theory. It is simply assumed that the reader has taken a first-year undergraduate (elementary) course in differential and integral calculus, along with elementary physics courses in classical mechanics and electrodynamics.
2. The book also covers topics that are not typically found in standard circuit textbooks, such as nonlinear operational amplifier circuits and memristor networks.
3. Nonlinear chaotic circuits are also discussed because we believe that chaotic circuits elegantly illustrate "applications" of concepts from circuit theory.
4. Each chapter has a set of illustrative examples, along with a set of exercises. We will have a set of (maximum 20-minute) lecture videos and video solutions to end-of-chapter exercises online: `http://www.youtube.com/user/bharathberkeley/IntroToNonlinearCircuitsAndNetworks` The purpose of these supplementary videos is to walk the reader through major concepts in each chapter, and thereby enhance understanding of nonlinear circuits and networks.

Over the course of a teaching career spanning 10 years at the University of California (UC) Berkeley, Dr. Muthuswamy has coordinated with Dr. Leon O. Chua and others to reintroduce nonlinear circuit theory at an elementary level. Much of the material in this book is thus derived from Dr. Chua's EE100 (Electronic Techniques for Engineering) lecture materials. This course was offered by electrical engineering and computer sciences department at UC Berkeley for non-electrical engineering majors. Therefore, the material in this book can be adopted for an introductory course in circuit theory.

At the University of California, Berkeley, we were able to cover the material in this book in one semester. The material on chaotic circuits was used as a source of projects. For schools that are based on the shorter quarter system (10 weeks of instruction), we would suggest splitting the material in this book into two courses. The first course could cover chapters 1 and 2 (network elements). The second course

would cover chapters 3, 4 and 5, where chapters 3 and 4 discuss techniques of network analysis followed by chapter 5 as a source of course projects. Another option would be to cover resistive networks in the first course and dynamic networks in the second course. Specifically:

1. First course - resistive networks: Only excluding material on dynamic elements in chapters 1 and 2 (sections 1.9.3, 1.9.4, 1.9.5, 2.2.3, 2.2.4, 2.3, 2.4) and covering all of chapter 3.
2. Second course - dynamic networks: Cover dynamic elements in chapters 1 and 2, followed by chapters 4 and 5.

Hence the way we have organized the chapters is based on the fact that, in circuit theory, the laws of elements are distinct from the laws of networks.

Our goal in writing this book is simple: a student who thoroughly understands the concepts in this book will be well prepared for any follow-up course in circuit theory.

Bharathwaj Muthuswamy, Santo Banerjee

Acknowledgements

There are a plethora of folks that we have to thank. From Dr. Muthusamy's perspective, first and foremost, he would like to thank his MS and PhD advisor Dr. Leon O. Chua for all his support and guidance. Particularly for this book, Dr. Chua guided us in organizing the content. His advice to extract simple yet novel concepts on nonlinear circuits theory from his classic works, "Introduction to Nonlinear Circuit Theory" and "Linear and Nonlinear Circuits", paved the way for this book.

Ferenc Kovac and Carl Chun from the University of California, Berkeley (Cal) have been both professional and personal mentors throughout the years. Dr. Pravin Varaiya was also instrumental for Dr. Muthuswamy's success at Cal. From Dr. Muthuswamy's academic career in Wisconsin, interactions with Dr. Jovan Jevtic and Dr. Gerald Thomas have been motivational and inspiring. Dr. Muthuswamy would also like to thank his colleagues at Tarana Wireless for their support in writing this book. Particularly: Rabin, Steve W., Anthony M., Andy L., Arvind, R. J., Nilesh, Samson, Aaron, Paragh, Bryan, Kamaraj, Beric, Chandra and Emy. The interactions that Dr. Muthuswamy has with them and other Tarana employees every day are priceless.

This book is the result of a conversation that Dr. Muthuswamy had with Dr. Gadiyar and Dr. Ganesan from the Vellore Institute of Technology in the summer of 2014. Their suggestion was to "capture the nonlinear circuits knowledge" of Dr. Leon O. Chua. Thus, capturing that knowledge is the primary purpose of this book. Hence this book is also a dedication to the original "pillars" of the Berkeley EECS community - Dr. Chua, Dr. Desoer and Dr. Kuh.

We would also like to thank the anonymous reviewers for helping us reformulate the content of this book, so as to make it sustainable. Without Springer's support throughout the writing process, this book would not have been possible.

Dr. Muthuswamy would also like to thank his family for their moral support throughout the process: wife Deepika, daughters Shambavi and Thejasvi; father M.G. Muthuswamy, mother Chandra Muthuswamy, brother Karthikeyan Muthuswamy and sister-in-law Mamta. Last but not the least, Dr. Muthuswamy would like to thank his spiritual advisor, Rajan Kurunthappan and family, for their continued unconditional support over the last two decades.

Contents

Acronyms

KVL	Kirchhoff's Voltage Law
KCL	Kirchhoff's Current Law
CCVS	Current Controlled Voltage Source
CCCS	Current Controlled Current Source
VCVS	Voltage Controlled Voltage Source
VCCS	Voltage Controlled Current Source

Mathematical Notation

The mathematical notation used in this book is standard [11]; nevertheless, this section clarifies the notation used throughout the book.

1. Lowercase letters from the Latin alphabet ($a-z$) are used to represent variables, with italic script for scalars and bold invariably reserved for vectors. The letter t is of course always reserved for time. n is usually reserved for the dimension of the state. j is used for $\sqrt{-1}$, in accordance with the usual electrical engineering convention. Mathematical constants such as π, e, h (Planck's constant) have their usual meaning. Other constant scalars are usually drawn from lower case Greek alphabet. SI units are used.
2. Independent variable in functions and differential equations is time (unless otherwise stated) because physical processes change with time.
3. Differentiation is expressed as follows. Time derivatives use Leibniz's ($\frac{dy}{dx}$, for example) or Newton's notation: one, two or three dots over a variable corresponds to the number of derivatives and a parenthetical superscripted numeral for higher derivatives. Leibniz's notation is used explicitly for non-time derivatives.
4. Real-valued functions, whether scalar- or vector-valued, are usually taken (as conventionally) from lowercase Latin letters f through h, r and s along with x through z.
5. Vector-valued functions and vector fields are bold-faced as well, the difference between the two being indicated by the argument font; hence $\mathbf{f}(x)$ and $\mathbf{f}(\mathbf{x})$ respectively.
6. Constant matrices and vectors are represented with capital and lowercase letters respectively, from the beginning of the Latin alphabet. Vectors are again bolded.
7. In the context of linear time-invariant systems the usual conventions are respected: A is the state matrix $B(b)$ is the input matrix (vector).
8. Subscripts denote elements of a matrix or vector: $\mathbf{d}_i$ is the i^{th} column of D; x_j is the j^{th} element of $\mathbf{x}$. Plain numerical superscripts on the other hand may indicate exponentiation, a recursive operation or simply a numbering depending on context. A superscripted T indicates matrix transpose. I is reserved for the identity matrix. All vectors are assumed to be columns.

9. Σ_i is used for summations, sampling interval is symbolized by T and $\in$ denotes set inclusions.
10. Calligraphic script ($\mathscr{R}$ etc.) is reserved for sets which use capital letters. Elements of sets are then represented with the corresponding lowercase letter. Excepted are the well known number sets which are rendered in doublestruck bold: $\mathbb{N}$, $\mathbb{Z}$, $\mathbb{Q}$, $\mathbb{R}$ and $\mathbb{C}$ for the naturals, integers, rationals, reals and complex numbers respectively. The natural numbers are taken to include 0. Restrictions to positive or negative subsets are indicated by a superscripted $+$ or $-$. The symbol $\stackrel{\triangle}{=}$ is used for definitions. $\forall$ and $\exists$ have the usual meaning of "for all" and "there exists" respectively.

Conventions Used In The Book

Each chapter starts with an epigraph, the purpose is to evoke the intellectual curiosity of the reader. Chapters are divided into sections and subsections for clarity.

Figures and equations are numbered consecutively. The convention for a definition is shown below.

Definition 0.1. Definitions are typeset as shown.

The book has a variety of solved examples, in light gray shade.

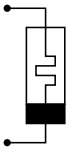
Solved Examples

All references are placed at the end of each chapter for convenience. We use a number surrounded by square brackets for in-text references, example [5]. Important terminology and concepts are highlighted **boldfaced**. In the electronic copy of this book, online URLs are colored and hyperlinked in midnight blue for ease of access. Computer code is in `verbatim font`.

The mathematical plots were generated using ipython, the source is available online at the companion website `http://www.harpgroup.org/IntroToNonlinearCircuitsAndNetworks/`. We utilize QUCS (Quite Universal Circuit Simulator), a functional open-source circuit simulator, that is introduced in lab component for Chapter 1. Figures were generated using a combination of xcircuit, xfig and PNG screen captures in OS X that were converted to EPS.

On a concluding remark, when you find typos in the book please contact the authors with constructive comments: bharath.berkeley@gmail.com, santoban@gmail.com.

Chapter 1
Two-Terminal Network Elements



Chua, L. O. *Memristor - The Missing Circuit Element [2]*

Abstract This chapter will set the stage for the rest of this book. We will start by discussing what is the aim of circuit theory, what are the fundamental circuit variables and when the techniques in this book are valid: the lumped circuit approximation holds and the frequencies of interest are not too high. We will discuss the concepts of Kirchhoff's laws, basic circuit topology, Tellegen's theorem and two-terminal circuit elements.

1.1 The Discipline of Circuit Theory

Circuit[1] theory is a fundamental engineering discipline that pervades all electrical engineering [5]. For the present, by physical circuit, we mean any interconnection of electrical devices. Familiar examples of electrical devices include resistors, diodes, transistors, operational amplifiers (opamps) etc. The goal of circuit theory is to predict the electrical behavior of physical circuits. The purpose of these predictions is to improve their design: in particular, to decrease their cost and improve their performance under all conditions of operation (e.g., temperature effects, aging effects, possible fault conditions, etc.).

Probably the most fascinating aspect is that lumped circuit theory uses only four fundamental circuit variables: current, charge, voltage and flux-linkage (flux). Moreover, current and voltage are related to charge and flux (Eqs. (1.3) and (1.4) respectively). Thus, fundamentally we have only four elements that are characterized by a mathematical relation between the above mentioned four circuit variables at the element's terminals [8], as shown in Fig. 1.1 [12].

Hence to start our study of circuit theory, we will first discuss the fundamental circuit variables, the topic of section 1.2.

[1] Throughout this book, we will use circuits and networks interchangeably, the justification will be discussed in section 1.6.

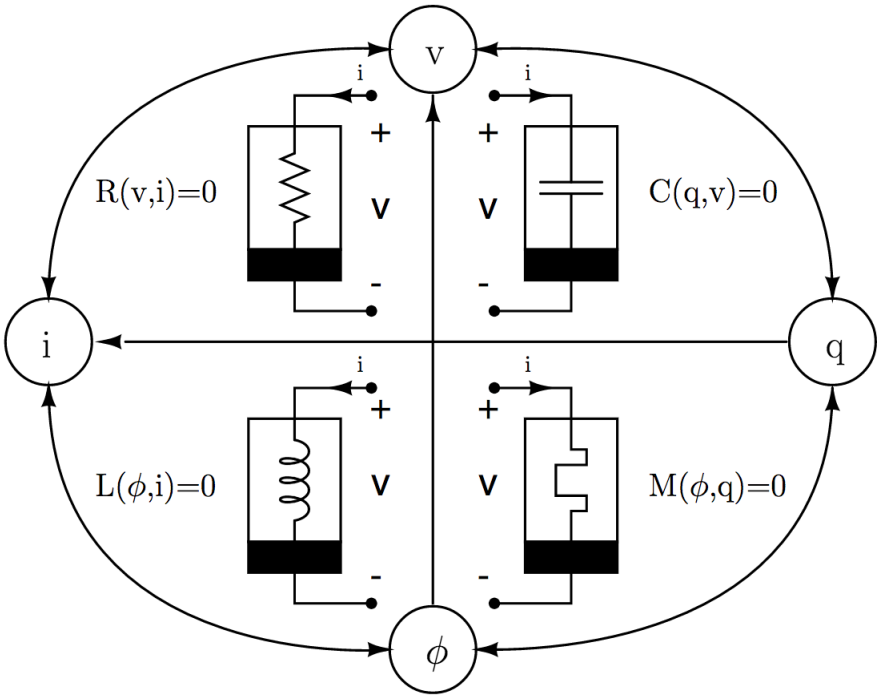


Fig. 1.1: The four fundamental two-terminal circuit elements along with the associated reference directions (section 1.4) relate the fundamental circuit variables, through the **laws of elements**. The elements starting counterclockwise from the top-left are the **resistor**, **inductor**, **memristor** and **capacitor**. Note that current is defined as the rate of flow of charge and voltage is defined as the rate of change of flux-linkage, refer to section 1.2. The symbols used for the fundamental circuit elements are standard for nonlinear circuit elements, the reader may be familiar with the circuit symbol for the linear counterparts (excluding the memristor), see section 1.9.4.

1.2 Fundamental Circuit Variables

We could say the advent of electricity [1] occurred with the discovery that dry substances such as amber tend to repel or attract each other upon being rubbed by different materials such as silk. This phenomenon was first explained by postulating the existence of a certain basic electrical quantity called the "electric charge" (charge), mathematical symbol q, which may be either positive or negative. Like charges exert a force of repulsion and unlike charges exert a force of attraction. The practical unit of charge is called the **coulomb** and has been defined to be equivalent

to the total charge possessed by 6.24×10^{18} electrons. Charge can be measured by instruments such as the electroscope.

Since charged bodies exert forces on one another, energy or work is involved whenever one charged body is moved in the vicinity of another charged body. Hence if w is the work done by moving a charge q from point j to point k (assuming w is independent of the path taken)[2], the potential difference or voltage between these points is defined as the work per unit charge.

$$v_{jk} = \frac{w}{q} \tag{1.1}$$

Observe that the magnitude of the charge is arbitrary; only the ratio between work and charge is important. Hence, the incremental work dw required to move an incremental test charge dq from point j to point k must also satisfy Eq. (1.1). Thus:

$$v_{jk} = \frac{dw}{dq} \tag{1.2}$$

We will delete the subscripts j and k when there is no possibility of confusion and simply express voltage as v. The unit of voltage is called the **volt** and is measured using a voltmeter.

Charges can be caused to flow from one charged body to another by connecting a conducting wire between the two bodies. Hence, the quantity "rate of flow of charge" becomes very useful, and it has been given the name current with symbol i. By definition,

$$i = \frac{dq}{dt} \tag{1.3}$$

The unit of current is the **ampere**. One ampere represents a charge flowing at the rate of one coulomb per second. Current flow can be measured by an ammeter.

In 1819, Hans Christian Oersted discovered that current flowing through a wire produced a force on a compass needle in the vicinity of the wire. This indicates that the current (or moving charge) produces a magnetic field. This effect can be explained by the generation of a magnetic flux λ by the current. If the conductor is wound into a coil of n turns, then by defining $\phi = n\lambda$ to be the flux-linkage, Faraday discovered that the voltage between the two terminals of the coil is given by

$$v = \frac{d\phi}{dt} \tag{1.4}$$

The unit of flux-linkage is the **weber**. Flux-linkage can be measured by a fluxmeter.

[2] This assumption is valid only if the simultaneity postulate is satisfied, we will discuss more in section 1.3.

1.3 The Simultaneity Postulate in Lumped Circuit Theory

Having discussed the fundamental circuit variables, the next question we need to address is: when are the techniques discussed in this book valid? The answer to this question is of paramount importance because the domain of application for circuit theory is extremely broad. For example, the size of circuits varies enormously: from very large-scale integrated circuits which include over a billion transistors on a chip the size of a fingernail to telecommunication circuits and power networks that span continents [5]. Throughout this book we shall consider only **lumped circuits** [5]. For a physical circuit to be considered lumped, its physical dimension must be small enough so that, for the problem at hand, **electromagnetic waves propagate across the circuit virtually instantaneously**. Consider the following example:

Example 1.3.1 Consider an audio circuit whose highest frequency of interest is $f = 20$ KHz. Discuss the lumped circuit approximation.
Solution: For electromagnetic waves, $f = 20$ KHz corresponds to a wavelength of:

$$\begin{aligned}\lambda &= \frac{c}{f} \\ &= \frac{3\times 10^8\ m/s}{2.0\times 10^4\ s^{-1}} \\ &= 15\ km\end{aligned}$$

Based on the calculations above, even if the circuit is spread across a tennis court, the size of the circuit is very small compared to the shortest wavelength of interest λ.

Definition 1.1. Lumped circuit approximation is valid if $d \ll c \cdot \Delta t$, where d is the largest dimension of the circuit, Δt the shortest time of interest and c is the velocity of light.

When the conditions in definition 1.1 are satisfied, electromagnetic theory proves [8] and experiments show that the lumped circuit approximation holds; namely, throughout the physical circuit the current $i(t)$ through any device terminal and the voltage difference $v(t)$ across any part of terminals, at any time t, are well-defined[3].

[3] Unless otherwise stated, we will assume from now on throughout the book that analogous statements are true for $q(t)$ and $\phi(t)$. In this case, we can equivalently discuss $q(t)$ through any device terminal and $\phi(t)$ across any part of the terminals.

Example 1.3.2 Consider a circuit on a chip whose extent is 1 mm. Let the shortest signal time of interest be 0.1 ns. Discuss the lumped circuit approximation from definition 1.1.
Solution: Again, since electromagnetic waves travel at the speed of light, the time it would take for the electromagnetic wave to travel 1 mm is:

$$\begin{aligned} t &= \frac{d}{c} \\ &= \frac{1 \times 10^{-3}\ m}{3 \times 10^{8}\ m/s} \\ &= 3.\bar{3}\ ps \end{aligned}$$

Therefore the propagation time in comparison with the shortest signal time of interest is negligible and hence the lumped circuit approximation is valid.

Based on examples 1.3.1 and 1.3.2, roughly speaking, the higher the frequency of operation, the smaller must be the device's physical dimension in order for the lumped circuit approximation to be satisfied. From an electromagnetic theory point of view, a lumped circuit reduces to a point since it is based on the approximation that electromagnetic waves propagate through the circuit instantaneously. For this reason, in lumped circuit theory, the respective locations of the elements of the circuit will not affect the behavior of the circuit. The approximation of a physical circuit by a lumped circuit is analogous to the modeling of a rigid body as a particle: in doing so, all data relating to the extent (shape, size, orientation, etc.) of the body are ignored by the theory.

In situations where lumped approximation is invalid, the physical dimensions of the circuit must be considered. To distinguish such circuits from lumped circuits we call them **distributed circuits**, typical examples are transmission lines and waveguides. In distributed circuits, the circuit variables depend not only on time, but also on space variables such as length and width. We need electromagnetic theory for predictions of the behavior of distributed circuits and hence they will not be discussed in this book.

1.4 Reference Directions

One of the most basic concepts in physical science is that any physical quantity is invariably measured with respect to some "assumed" frame of reference [8]. In electrical network theory, the frame of reference takes the form of an assumed reference direction of the current i and an assumed reference polarity of the voltage v. A thorough understanding of the concept of reference current direction and reference voltage polarity is absolutely essential in the study of nonlinear network theory. It is a fact that a large percentage of the mistakes committed by students of network the-

ory can be traced to either the students' underestimation of the full significance of reference current directions and voltage polarities or the students' failure to maintain a consistent set of references.

The simplest way to understand the concept of assumed reference direction and polarity is through the experiment illustrated in Fig. 1.2. We will discuss reference voltage polarity, an analogous discussion holds for the reference current direction. Suppose we are given a black box with a pair of **accessible ports** or **terminals** $a-b$, as shown in Fig. 1.2, and we are required to measure the voltage across terminals $a-b$. Let us measure the voltage by connecting $a-b$ to the vertical input terminals of an oscilloscope. Since one of the two vertical input terminals of an oscilloscope is marked with a positive sign while the other is marked with a negative sign, the question that immediately arises is which of the two terminals of the black box should we connect to the positive terminal of the oscilloscope in order to obtain the desired information?

The answer is that it does not matter. In order to see this, suppose we **arbitrarily assume** terminal b is connected to the positive terminal as shown in Fig. 1.2 (a). The assumption that terminal b is at the positive terminal does not mean that terminal b is at a higher potential than terminal a. It does mean however that if at any time $t = t_1, v(t_1) > 0$, then the potential at b is higher than the potential at a. On the other hand, if $v(t_1) < 0$, then the potential at b at $t = t_1$ is actually lower than the potential at a. For example, if the voltage $v(t)$ displayed on the oscilloscope (in volts) is given by

$$v(t) = 10\sin \pi t \tag{1.5}$$

then terminal b is at a higher potential than terminal a during the time interval $0 < t < 1$ s. But during the time interval $1 < t < 2$ s, terminal b is at a lower potential than terminal a.

Let us now consider what happens when we assume terminal a is connected to the positive terminal of the oscilloscope, instead of terminal b, as shown in Fig. 1.2 (b). Since this connection is opposite to the connection in Fig. 1.2 (a), it is clear that the voltage displayed on the oscilloscope (in volts) is given by:

$$v(t) = -10\sin \pi t \tag{1.6}$$

Thus in either case, the final answers are identical. We can therefore conclude that in order to specify the voltage between any pair of terminals unambiguously, we may arbitrarily assume any one of the two possible terminals to be positive. By analogy, we can conclude that in order to specify the current through any wire unambiguously, we may arbitrarily assume any one of the possible two directions to be positive.

Let us consider next a two-terminal black box N and assume a reference direction for the terminal current i and a reference polarity for the terminal voltage v, see Fig. 1.3. Since the references for both i and v are arbitrary, there are four distinct sets of combinations of references. There is no reason to prefer any one combination over

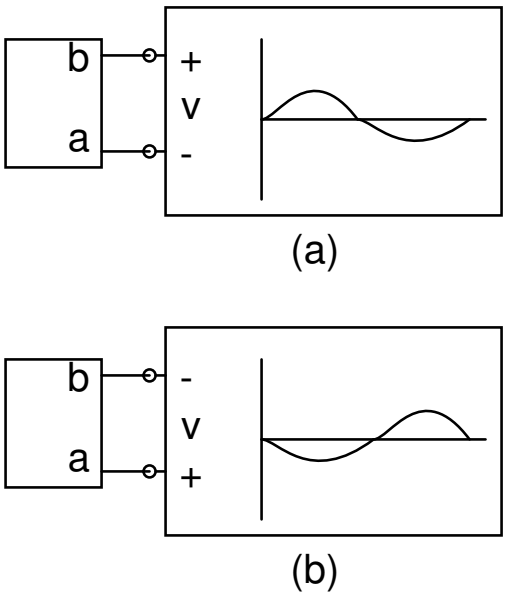


Fig. 1.2: An experiment demonstrating that regardless of which terminal of the black box is chosen to be positive, the actual voltage across terminals $a-b$ can be unambiguously specified for all time.

the others. However, in practice, it is usually convenient to choose the combination so that **positive** power represents power **entering** the black box.

From classical mechanics, we know that power is defined by Eq. (1.7).

$$p = \frac{dw}{dt} \tag{1.7}$$

But,

$$\begin{aligned} vi &= \frac{dw}{dq}\frac{dq}{dt} \\ &= \frac{dw}{dt} \end{aligned} \tag{1.8}$$

Thus we have:

$$p(t) = v(t)i(t) \tag{1.9}$$

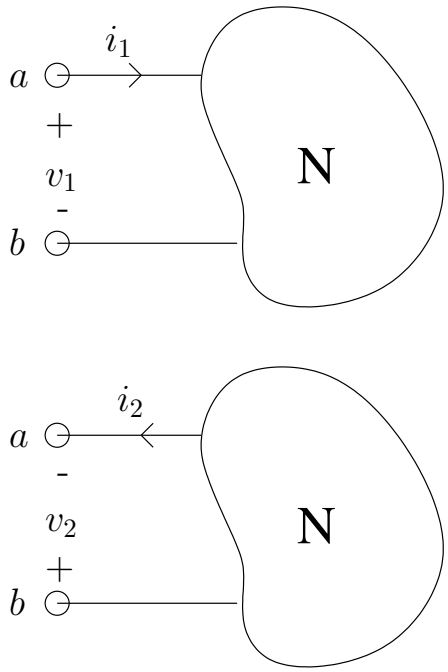


Fig. 1.3: Two possible sets of reference direction for the passive sign convention from definition 1.2.

From the simultaneity postulate, the same current must leave the negative terminal[4]. Hence, based on this observation, we have definition 1.2.

Definition 1.2. Associated Reference Direction or Passive Sign Convention: Whenever the reference direction for the current i in a two-terminal black box is in the direction of the reference voltage drop v across the black box ($v > 0.i > 0$), we use a positive sign in any expression that relates voltage to current. Otherwise, we use a negative sign.

Thus definition 1.2 implies that the allowable reference combination must be either of the form shown in Fig. 1.3.

1.5 Kirchhoff's Laws

When circuit elements are interconnected to form a circuit, there are some governing laws that all elements in the network must obey. We shall refer to these laws as

[4] This is also a consequence of Kirchhoff's Current Law, see section 1.5.2.

the **laws of interconnection**. Before we discuss these laws, we need the following definitions:

Definition 1.3. A **node** is a point in a circuit where two or more circuit elements are interconnected.

Definition 1.4. A **path** is a trace of adjoining elements, with no elements included more than once.

Definition 1.5. A **closed node sequence** is a path whose last node is the same as the starting node.

Definition 1.6. A **loop** is a closed node sequence that traverses only through two-terminal elements.

Definition 1.7. A **branch** is a path that connects two nodes.

Definition 1.8. A **connected circuit** is one in which any node can be reached from any other node, by traversing a path through the circuit elements.

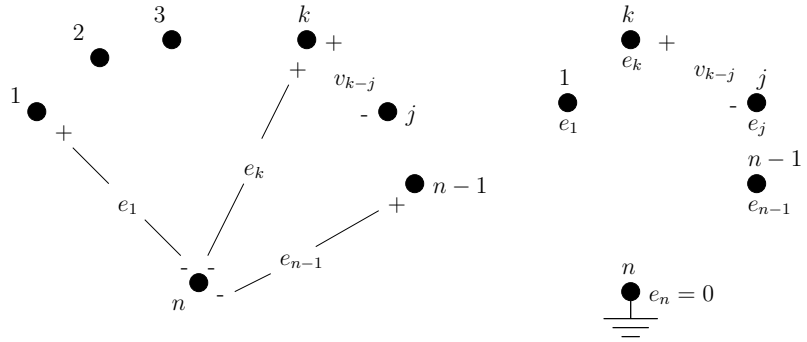


Fig. 1.4: Labeling node-to-ground voltages for a circuit with n nodes.

Now, given any connected lumped circuit having n nodes, we may choose (arbitrarily) one of the nodes as a **ground** node, i.e., as a reference for measuring electric potentials. Note that a circuit does not have to be physically connected to ground for proper functionality, think about circuits inside our mobile phones.

With respect to the chosen ground node, we define $n-1$ node-to-ground voltages as shown in Fig. 1.4. Since the circuit is a connected lumped circuit, these $n-1$ voltages are well-defined and, in principle, physically measurable quantities. Henceforth, we shall label them $e_1, e_2, \ldots, e_{n-1}$ and dispense with the $+$ and $-$ signs indicating voltage reference direction. Note that $e_n = 0$ since node n is chosen as the ground node.

Let v_{k-j} denote the voltage difference between node k and node j as shown in Fig. 1.4. Kirchhoff's voltage law states:

1.5.1 Kirchhoff's Voltage Law (KVL)

Definition 1.9. KVL: For all lumped connected circuits, for all choices of ground node, for all times t, for all pairs of nodes k and j,

$$v_{k-j}(t) = e_k(t) - e_j(t) \tag{1.10}$$

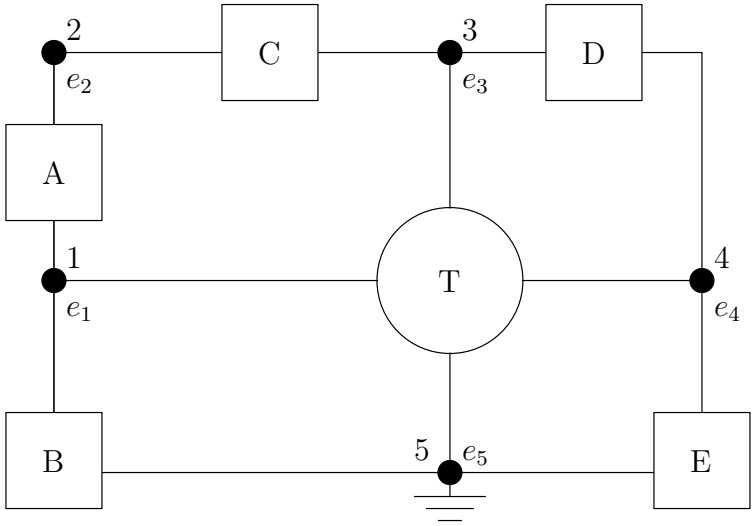


Fig. 1.5: Circuit for example 1.5.1.

Example 1.5.1 Write KVL expressions for the circuit in Fig. 1.5.
Solution: The connected circuit in Fig. 1.5 is made of 5 two-terminal elements and 1 four-terminal element. There are five nodes. Choosing (arbitrarily) node 5 as the ground node, we define the four node-to-ground voltages e_1, e_2, e_3 and e_4. Therefore by KVL, we may write the following seven equations (for convenience, we drop the dependence on t):

$$
\begin{aligned}
v_{1-2} &= e_1 - e_2 \\
v_{2-3} &= e_2 - e_3 \\
v_{3-4} &= e_3 - e_4 \\
v_{1-4} &= e_1 - e_4 \\
v_{4-5} &= e_4 - e_5 = e_4 \\
v_{5-1} &= e_5 - e_1 = -e_1
\end{aligned} \tag{1.11}
$$

Note that $v_{1-2}, v_{2-3}, v_{3-4}, v_{4-5}, v_{5-1}$ are the voltages across the two-terminal elements A, C, D, E, B respectively; v_{1-4}, v_{4-5} and v_{5-1} are the voltages across the node pairs (1,4); (4,5) and (5,1) of the four-terminal element T respectively.

If we add the last three equations in Eq. (1.11), we find that:

$$v_{1-4} + v_{4-5} + v_{5-1} = 0 \tag{1.12}$$

Hence for this particular closed node sequence, the sum of the voltages is equal to zero.

Note also that if we add the first three and last two equations in Eq. (1.11), we find the sum of voltages around a loop is zero:

$$v_{1-2} + v_{2-3} + v_{3-4} + v_{4-5} + v_{5-1} = 0 \tag{1.13}$$

Example 1.5.1 shows that we can state KVL in terms of closed node sequences:

Definition 1.10. KVL (closed node sequences): For all lumped connected circuits, for all closed node sequences, for all times t, the algebraic sum of all node-to-node voltages around the chosen closed node sequence is equal to zero.

1.5.2 Kirchhoff's Current Law (KCL)

A fundamental law of physics asserts that electrical charge is conserved: There is no known experiment in which a net electric charge is either created or destroyed. KCL expresses this fundamental law in the context of lumped circuits. To state KCL, we first need the definition of a gaussian surface.

Definition 1.11. A **gaussian surface** $\mathscr{L}$ is a two-sided closed surface, that has an "inside" and an "outside".

To express the fact that the sum of the charges inside $\mathscr{L}$ is constant, we shall require that at all times, the algebraic sum of all the currents leaving the surface $\mathscr{L}$ is equal to zero.

Definition 1.12. KCL: For all lumped circuits, for all $\mathscr{L}$, for all times t, the algebraic sum of all the currents **leaving** $\mathscr{L}$ at time t is equal to zero.

We will choose $\mathscr{L}$ so that it cuts only the wires which connect the circuit elements, as discussed in example 1.5.2.

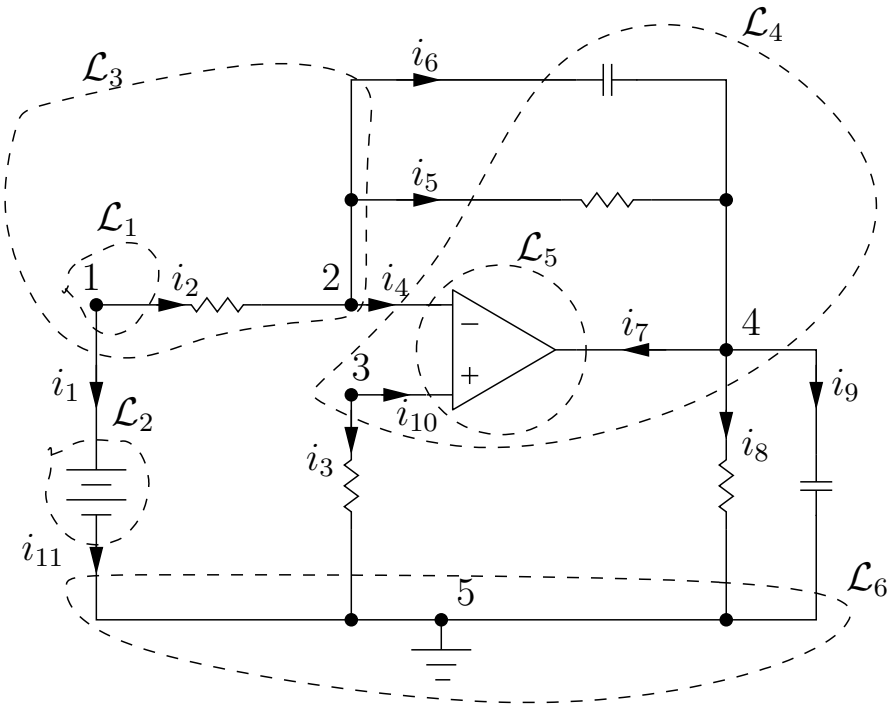


Fig. 1.6: An opamp circuit illustrating gaussian surfaces and KCL.

Example 1.5.2 Write KCL expressions for the circuit in Fig. 1.6.
Solution: In Fig. 1.6, we have used two-terminal elements and a three-terminal ideal operational amplifier (opamp) (that we will discuss in section 2.5). In the figure, we have drawn six gaussian surfaces $\mathscr{L}_1, \mathscr{L}_2, \cdots, \mathscr{L}_6$. We will use these surfaces to illustrate KCL.

For $\mathscr{L}_1$, KCL states:

$$i_1(t) + i_2(t) = 0 \quad \forall t \tag{1.14}$$

Note that $\mathscr{L}_1$ contains only node 1 in its "inside". Thus a node may be considered as a special case of $\mathscr{L}$, i.e., the surface is shrunk to a point.

For $\mathscr{L}_2$, KCL states:

$$-i_1(t)+i_{11}(t)=0 \tag{1.15}$$

Note that $\mathscr{L}_2$ encloses a two-terminal element. Thus we make the conclusion that for a **two-terminal element**, the current entering the element from one node at any time t is equal to the current leaving the element from the other node at t.

For $\mathscr{L}_3$, KCL states:

$$i_1(t)+i_4(t)+i_5(t)+i_6(t)=0 \tag{1.16}$$

For $\mathscr{L}_4$, KCL states:

$$i_3(t)+i_8(t)+i_9(t)-i_4(t)-i_5(t)-i_6(t)=0 \tag{1.17}$$

For $\mathscr{L}_5$, KCL states:

$$-i_4(t)-i_7(t)-i_{10}(t)=0 \tag{1.18}$$

Note that these are the three currents pertaining to the opamp. Thus choosing an $\mathscr{L}$ that encloses any n-terminal element, we state that the algebraic sum of the currents leaving or entering the n-terminal element is equal to zero at all times t. n-terminal elements will be covered in more detail in Chapter 2.

For $\mathscr{L}_6$ (that encloses only the reference node), KCL states:

$$-i_3(t)-i_8(t)-i_9(t)-i_{11}(t)=0 \tag{1.19}$$

We conclude this section by stating KCL for nodes:

Definition 1.13. KCL (node law): For all lumped circuits, for all $\mathscr{L}$, for all times t, the algebraic sum of currents **leaving** any node is equal to zero.

1.6 From Circuits to Graphs: The Definition of a Network

It should be clear from our discussions of KVL and KCL that the equations arising from laws of interconnection are independent of the type of elements in a network. We will now state the definition of a network.

Definition 1.14. A **network** is any interconnection of circuit elements.

Only the network connection diagram, the **topology**, needs to be specified in order to obtain the equations to the laws of interconnection. The topology of a circuit is best exhibited by way of a **graph**.

Definition 1.15. A **graph** $\mathscr{G}$ is specified by a set of nodes $\{1,2,\cdots,n\}$ together with a set of branches $\{\beta_1,\beta_2,\cdots,\beta_n\}$.

If each branch is given an orientation, indicated by an arrow on the branch, we call the graph directed. For example, a two-terminal element and the associated **element graph** is shown in Fig 1.7.

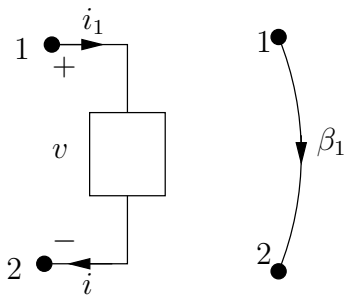


Fig. 1.7: A two-terminal element and its associated element graph representation.

Notice that the element graph for a two-terminal element has two nodes and one branch. Also note that the directions of the current flow through and voltage drop across the two-terminal element are specified using the passive sign convention from definition 1.2.

For a given circuit, if we replace each element by its associated element graph, we obtain the **directed circuit graph** or **digraph** $\mathscr{G}$. In this book, whenever we refer to a network, we mean the associated digraph of the circuit. We can use either the digraph or the circuit for analysis. Hence, throughout this book, we will use "circuits" and "networks" interchangeably. Nevertheless, there are results in circuit theory such as Tellegen's theorem in section 1.6.1, that are more obvious from the network associated with a given circuit.

Example 1.6.1 Write KCL and KVL expressions for the digraph in Fig. 1.8.
Solution: It is interesting to note that since the circuit contains a three-terminal element, the digraph bears little resemblance to the circuit. In fact, given the digraph, without specifying which nodes belong to the three-terminal element, it is not possible to reconstruct the circuit. This observation is false if the circuit contains only two-terminal elements.

KCL gives:

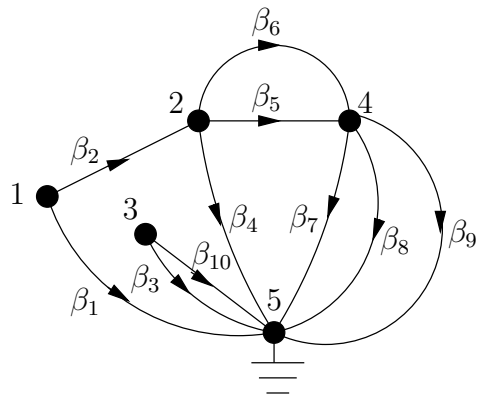


Fig. 1.8: Digraph associated with the circuit in Fig. 1.6. Detailed derivation of the opamp digraph will be covered in section 2.5.

$$\begin{aligned} i_1 + i_2 &= 0 \\ -i_2 + i_4 + i_5 + i_6 &= 0 \\ i_3 + i_{10} &= 0 \\ -i_5 - i_6 + i_7 + i_8 + i_9 &= 0 \end{aligned} \tag{1.20}$$

Let us rewrite Eq. (1.20) in matrix form:

$$\begin{pmatrix} 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & -1 & -1 & 1 & 1 & 1 & 0 \end{pmatrix} \begin{pmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \\ i_6 \\ i_7 \\ i_8 \\ i_9 \\ i_{10} \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix} \tag{1.21}$$

Let:

$$A \triangleq \begin{pmatrix} 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & -1 & -1 & 1 & 1 & 1 & 0 \end{pmatrix} \tag{1.22}$$

Thus, Eq. (1.21) can be written as:

$$A\mathbf{i} = \mathbf{0} \tag{1.23}$$

Matrix A is called the **incidence matrix**.

We can express all ten branch voltages in terms of the reference node by using KVL:

$$\begin{aligned} v_1 &= e_1 \\ v_2 &= e_1 - e_2 \\ v_3 &= e_3 \\ v_4 &= e_2 \\ v_5 &= e_2 - e_4 \\ v_6 &= e_2 - e_4 \\ v_7 &= e_4 \\ v_8 &= e_4 \\ v_9 &= e_4 \\ v_{10} &= e_3 \end{aligned} \tag{1.24}$$

Rewriting Eq. (1.24) in matrix form:

$$\begin{pmatrix} 1 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & -1 \\ 0 & 1 & 0 & -1 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{pmatrix} \begin{pmatrix} e_1 \\ e_2 \\ e_3 \\ e_4 \end{pmatrix} = \begin{pmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_5 \\ v_6 \\ v_7 \\ v_8 \\ v_9 \\ v_{10} \end{pmatrix} \tag{1.25}$$

Comparing Eqs. (1.21) and (1.25), we can see that the constant matrix on the LHS of Eq. (1.25) is A^T. Hence Eq. (1.25) can be written as:

$$A^T\mathbf{e} = \mathbf{v} \tag{1.26}$$

Much more will be said about topological concepts in circuit theory throughout this book. Specifically, element graphs for multi-terminal elements will be discussed in Chapter 2. We will formalize the matrix formulation of Kirchhoff's laws in Chapter 3, before we discuss formal techniques of circuit analysis.

1.6.1 Tellegen's Theorem

A beautiful illustration of the generality of the digraph approach is Tellegen's theorem. Before formally stating the theorem, consider the circuits in Fig. 1.9.

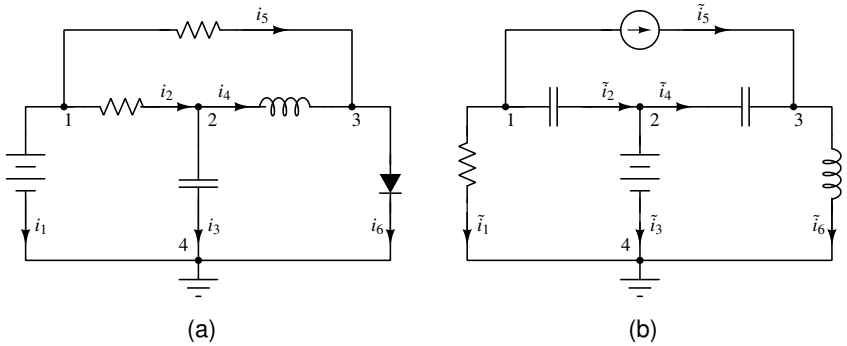


Fig. 1.9: Circuits for understanding Tellegen's theorem.

KVL and KCL in matrix form for the circuit in Fig. 1.9 (a) are:

$$\begin{aligned} A^T\mathbf{e} &= \mathbf{v} \\ A\mathbf{i} &= \mathbf{0} \end{aligned} \tag{1.27}$$

where:

$$A = \begin{pmatrix} 1 & 1 & 0 & 0 & 1 & 0 \\ 0 & -1 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & -1 & -1 & 1 \end{pmatrix} \tag{1.28}$$

Let the branch power $v_k i_k$ be summed for all N branches of the circuit. Then, by Eq. (1.27):

$$\begin{aligned} \sum_{k=1}^{N} v_k i_k &= \mathbf{v}^T\mathbf{i} \\ &= (A^T\mathbf{e})^T\mathbf{i} \\ &= \mathbf{e}^T(A\mathbf{i}) \\ &= 0 \end{aligned} \tag{1.29}$$

In deriving Eq. (1.29), the familiar rules $(AB)^T = B^TA^T, (A^T)^T = A, \mathbf{e}^T\mathbf{0} = 0$ of vector algebra have been used.

The result in Eq. (1.29) should not be surprising since we have derived the conservation of power in a circuit from Kirchhoff's laws.

Consider however the circuit of Fig. 1.9 (b) which has the same topological configuration, same reference directions and numbering, and hence the same A as the circuit in Fig. 1.9 (a). Hence, the incidence matrix for the circuit in Fig. 1.9 (b) is also given by Eq. (1.28). Let the electrical quantities of the circuit be $\tilde{\mathbf{i}}, \tilde{\mathbf{v}}, \tilde{\mathbf{e}}$ in Fig. 1.9 (b). Then:

$$\begin{aligned} A^T\tilde{\mathbf{e}} &= \tilde{\mathbf{v}} \\ A\tilde{\mathbf{i}} &= \mathbf{0} \end{aligned} \tag{1.30}$$

Now consider:

$$\begin{aligned} \sum_{k=1}^{N} v_k\tilde{i}_k &= \mathbf{v}^T\tilde{\mathbf{i}} \\ &= (A^T\mathbf{e})^T\tilde{\mathbf{i}} \\ &= \mathbf{e}^T(A\tilde{\mathbf{i}}) \\ &= 0 \end{aligned} \tag{1.31}$$

While the LHS of Eq. (1.31) has the dimensions of power, the quantity is physically meaningless since v_k and $\tilde{i}_k$ exist in two different circuits.

Similarly, we can show:

$$\tilde{\mathbf{v}}^T\mathbf{i} = 0 \tag{1.32}$$

Eqs. (1.31) and (1.32) are general forms of Tellegen's theorem, which we will now formally state.

Theorem 1.1. *Tellegen's theorem*
Consider an arbitrary circuit. Let the associated digraph $\mathscr{G}$ have b branches. Using passive sign convention, let $\mathbf{v} = (v_1, v_2, \cdots, v_b)^T$ be **any** set of branch voltages satisfying KVL for $\mathscr{G}$ and let $\mathbf{i} = (i_1, i_2, \cdots, i_b)^T$ be **any** set of branch currents satisfying KCL for $\mathscr{G}$. Then:

$$\sum_{k=1}^{b} v_k i_k = 0 \tag{1.33}$$

Equivalently:

$$\mathbf{v}^T\mathbf{i} = 0 \tag{1.34}$$

Tellegen's theorem has significant applications in general resistive circuit analysis. We will prove Theorem 1.1 and apply it to circuit analysis in Chapter 3.

1.7 Circuit Theory from Electromagnetic Field Theory

Now that we have an understanding of the laws of interconnection, we will have a short discussion in this section on how to arrive at these laws, by using the fact that circuit theory is an approximation of electromagnetic field theory. Although we are only concerned with lumped circuits in this book, this section is useful because the approximation techniques used have roots in the very important concept of modeling [8].

Engineers and scientists seldom analyze a physical system in its original form. Instead, they construct a model which approximates the behavior of the system. By analyzing the behavior of the model, they hope to predict the behavior of the actual system. The primary reason for constructing models is that physical systems are usually too complex to be amenable to a practical analysis. In most cases, the complexity of a system is due in part to the presence of many nonessential factors. **The basic principle of modeling consists, therefore, of extracting only the essential factors.**

We will start discussing modeling of the fundamental circuit elements in section 1.8 and continue the discussion throughout the book. But, with respect to the laws of interconnection, namely KCL and KVL, we need to only discuss how these laws extract only the essential factors from electromagnetic field theory [8].

From the node form of KCL in definition 1.13, we know that the sum of the currents flowing out of a node must be equal to zero. From field theory, the surface integral of the current density over a closed surface must be equal to zero, if no charge accumulates inside that surface. Definition 1.3 of a node implies that a node is a theoretical abstraction of a physical interconnection of wires: a node does not have any circuit elements such as capacitors associated with it. Hence, no charge can accumulate on a node, and the sum of currents leaving the node must be equal to zero.

KVL from definition 1.10 is equivalent to Faraday's law of induction from Maxwell's theory of electromagnetism. This equivalence, however, is not directly evident as the relation between KCL and the law of conservation of charge. Indeed, KVL depends on how the branch voltages are defined in terms of the electromagnetic field. The details are beyond the scope of this book. But, we can get an intuitive idea by considering the fact that we defined branch voltage as the difference between node-to-ground voltages in Eq. (1.10). In fact, a practical device for measuring branch voltage - the voltmeter - is connected such that voltage is measured across a pair of nodes. Hence a voltmeter is designed to measure the line integral of the electric field along the path formed by the connecting leads. Thus, the sum of voltages around a closed loop in a circuit has the electromagnetic equivalent of the electric field around a closed path. The electric field involved in this integration is, by assumption, equal (or approximately so) to the negative gradient of a scalar potential [8]. Therefore, the line integral of the electric field should vanish, and this gives us KVL.

1.8 Characterization of a Two-Terminal Black Box

Now that we have discussed interconnection of circuit elements, it is time to discuss the circuit elements themselves. Although we will encounter many physical devices of varying complexity throughout this book, we will model them as black boxes [8]. These boxes may possess many terminals, but **only two of these are accessible to the external world in the sense that the device may be excited only through these terminals**. For our purpose, it is convenient to imagine that the device is enclosed in a box and that the two accessible terminals are brought out by two connecting wires, with the symbol shown in Fig. 1.10 (a).

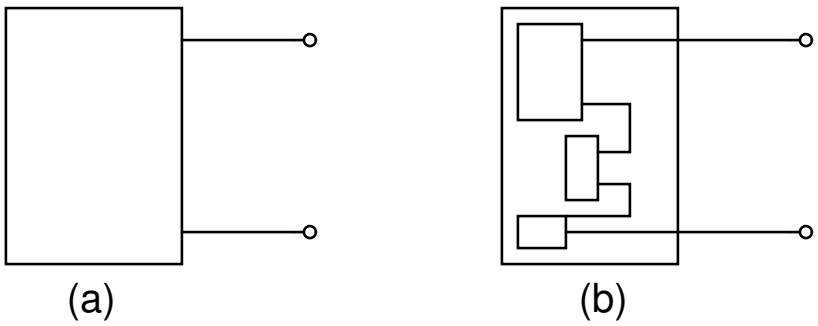


Fig. 1.10: Symbolic representation of two-terminal black boxes.

It is important to emphasize that the content of the black box may be as simple as a light bulb, or as complicated as an arbitrary interconnection of black boxes as shown in Fig .1.10 (b).

The choice of the term "blackbox" is quite appropriate here because the box is really black inside in the sense that we cannot see its contents. As a matter of fact, unless we open the box and peep inside, there is no way of determining its contents. However, as engineers, we are not so much interested in the contents of the box as in knowing what the box is capable of and how it behaves externally when it is connected with other black boxes into a network. In other words, we are primarily interested in predicting the external behavior of the black box. Our first step toward such an analytical approach is to "characterize" the black box. **To properly characterize a blackbox, it is paramount that we choose the correct set of terminal variables.** We will illustrate this idea in this section by modeling a "spring" from basic physics, refer to Fig. 1.11.

Suppose we did not know that in reality we had a spring inside the black box and we were asked to predict the behavior of the external terminals when an arbitrary force $f(t)$ is applied to one end (terminal) of the spring while the other end (terminal) is fixed against a wall. The mechanical variables of interest here are the displacement x (displacement to the right of the initial 0 position is assumed posi-

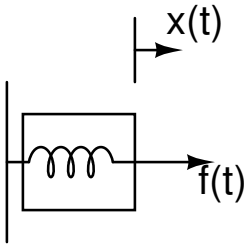


Fig. 1.11: An example illustrating the characterization of a mechanical black box.

tive, as shown in Fig. 1.11), velocity v of the terminal that is free to move and the force f (positive for tension, negative for compression).

Clearly the only way we can hope to characterize this black box (other than opening the box) is to start performing some experiments. Suppose we begin by applying a constant force $f = A$ and measure the corresponding velocity v. This would give us a point in the velocity-vs-force plane ($f - v$ plane). By repeating the above experiment with several values of the force f, we obtain the data show in Fig. 1.12.

We might be tempted to draw a smooth curve through these data points (which in this case happens to be the f axis) and claim to have characterized the black box in the sense that given any constant force f, we can analytically predict the associated velocity.

However a little thought will show that we have not really characterized the black box yet, for if, instead of applying a constant force we apply a slowly varying sinusoidal force, $f(t) = A\sin(t)$. The characteristics in Fig. 1.12 would predict that $v = 0$.

This is of course contrary to what we observe experimentally: namely, $v(t) = (A/k)\cos(t)$, where k is the spring constant. We might hope that this inconsistency can be resolved by plotting all points (f, v). Nevertheless we will again quickly conclude that the length of both axes of the resulting ellipse depends on the amplitude A of the applied force f. For each A we will obtain an unique ellipse and thus we will eventually fill the entire $f - v$ plane. Even if we could draw an infinite set of ellipses, we would be able to predict the velocity only if f is sinusoidal. Using these ellipses to predict v due to non-sinusoidal f would again yield incorrect answers. We must now realize that the useful information we obtained from this experiment is that the black box cannot be characterized by a curve in the $f - v$ plane.

Suppose we try another set of variables, say the force f and displacement x. Repeating the experiments, we will find that **provided f(t) does not change rapidly, the black box can be characterized by a displacement-vs-force ($f - x$) curve.**

After experiencing the length of time needed to carry out the above experiments, we can now begin to appreciate the utility of such a conclusion; namely, the charac-

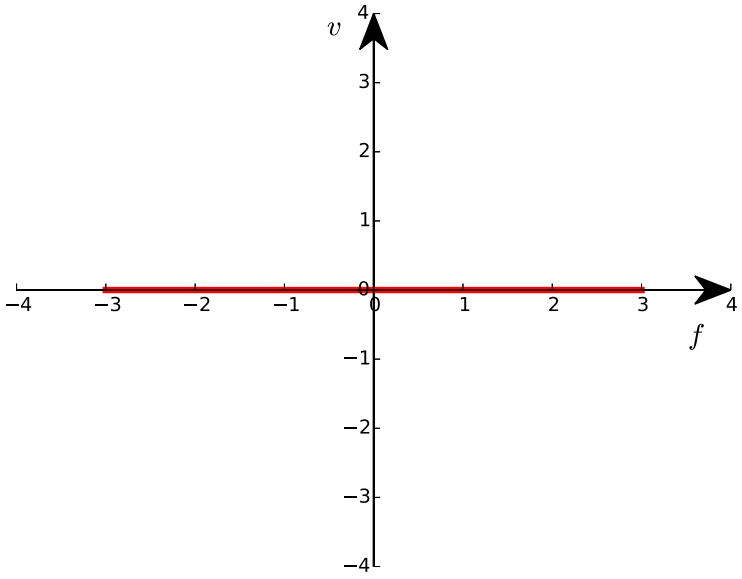


Fig. 1.12: force-velocity plot for constant force $f = A$.

terization of the black box permits an analytical solution and thereby eliminates the need to carry out any further experiments.

Observe however that our conclusion is based on the assumption that $f(t)$ does not change rapidly. If we were to repeat our experiment with higher-frequency sinusoidal waveforms, as well as non-sinusoidal waveforms which change rapidly, we will find deviations from our conclusions drawn using low frequency waveforms. This will suggest that our earlier assumption, that f does not change rapidly, is indeed necessary. In order to emphasize this restriction, it is a common practice to call a black box characterization as **static characterization**, in contrast to a **dynamic characterization** for higher frequencies. Hence for the black box in Fig. 1.11, the $f - x$ curve is the static characteristic.

Since the deviation of the measured characteristic from the static characteristic increases slowly with frequency rather than abruptly, it is impossible to pick a definite frequency above which the static characteristic does not hold. Neither it is possible to find a single dynamic characteristic that would hold for all frequencies. Hence a certain amount of scientific judgment is involved in deciding whether a certain static characteristic curve can be used to satisfactorily solve a given problem. It is encouraging, however, to know that a large percentage of practical networks can indeed be analyzed using only static characteristics. Moreover, even in cases

where the static characteristic fails to give satisfactory solutions, we shall show in future chapters that we can often patch up the error by including "parasitic elements", namely, elements which are undesirable but which are invariably present in the black box in small quantities. Thus, in this book, **we will assume all characteristics are static and will utilize parasitic elements to model the necessary dynamic characteristics. We shall henceforth delete the adjective "static".**

For the example in Fig. 1.11, the parasitic element consists of the mass associated with the spring. At low frequencies, the mass being quite small, has relatively no effect on the $f-x$ characteristic. However as the frequency of the external force increases, the acceleration of the spring increases and the inertia force due to the mass becomes appreciable.

1.9 Two-Terminal Elements

From the previous section, we know that it is essential to choose the correct set of variables for characterizing a blackbox. For two-terminal elements, the circuit variables of interest are those that can be measured externally. Hence the terminal voltage v and terminal current i are of primary interest because they can be readily measured. The charge q and flux-linkage ϕ are also of interest because they can be indirectly measured by **integrating** the measured current $i(t)$ and voltage $v(t)$ respectively. From these measurements, we shall then try to establish a relationship, if any, between each pair of **independent** variables.

i and q are related by Eq. (1.3); v and ϕ are related by Eq. (1.4). Hence the only remaining combinations consist therefore of the relationship between the following variables.

1. Relationship between v and i, this is the two-terminal resistor shown in the top-left corner of Fig. 1.1.
2. Relationship between ϕ and i, this is the two-terminal inductor shown in the bottom-left corner of Fig. 1.1.
3. Relationship between ϕ and q, this is the two-terminal memristor shown in the bottom-right corner of Fig. 1.1.
4. Relationship between v and q, this is the two-terminal capacitor shown in the top-right corner of Fig. 1.1.

We will now discuss each of these elements in detail. But, before we begin our discussion of two-terminal elements, a note about $time-varying$ elements: each of the four fundamental circuit elements we will discuss can be time-varying. For instance, a time-varying resistor is defined by the relation: $f_R(v,i,t)=0$. A very simple example is a potentiometer (or variable resistor), whose arm is being rotated by say a motor. Nevertheless, the analysis of a nonlinear network containing time-varying elements is a very difficult mathematical problem requiring advanced mathematics. Hence we will restrict discussion in this book to nonlinear time-invariant elements.

1.9.1 Resistors

The **linear resistor** is probably the most familiar circuit element that one encounters in basic physics. This device satisfies Ohm's law: that is, the voltage across such an element is proportional to the current flowing through it. We represent it by the symbol shown in Fig. 1.13 where the current i through the resistor and the voltage v across it are measured using the passive sign convention from definition 1.2.

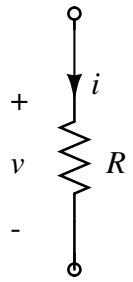


Fig. 1.13: Symbol for a linear resistor with resistance R.

Ohm's law states that at all times.

$$v(t) = Ri(t) \text{ or}$$
$$i(t) = Gv(t) \tag{1.35}$$

where the constant R is the **resistance** of the linear resistor (measured in the unit of ohms (Ω)) and G is the **conductance** measured in units of siemens (S).

Eq. (1.35) can be plotted on the $i-v$ plane or $v-i$ plane[5] as shown in Fig. 1.14.

There are two special cases of linear resistors which deserve special mention, namely, the **open circuit** and **short circuit**.

Definition 1.16. A two-terminal resistor is called an open circuit iff its current i is identically zero irrespective of the voltage v; i.e. $f(v,i) = i = 0$.

The characteristic of an open circuit is the v axis in the $v-i$ plane, with zero slope ($G = 0$). In the $i-v$ plane, it has an infinite slope, $R \to \infty$, refer to Fig. 1.15

Definition 1.17. A two-terminal resistor is called a short circuit iff its voltage v is identically zero irrespective of the current i; i.e. $f(v,i) = v = 0$.

The characteristic of a short circuit is the i axis in the $v-i$ plane, with $G \to \infty$. In the $i-v$ plane, the characteristic has zero slope, $G = 0$, refer to Fig. 1.16.

[5] When we say $x-y$ plane, we denote specifically x as the horizontal axis and y as the vertical axis of the plane. This is consistent with the conventional usage where the first variable denotes the abscissa and the second variable denotes the ordinate.

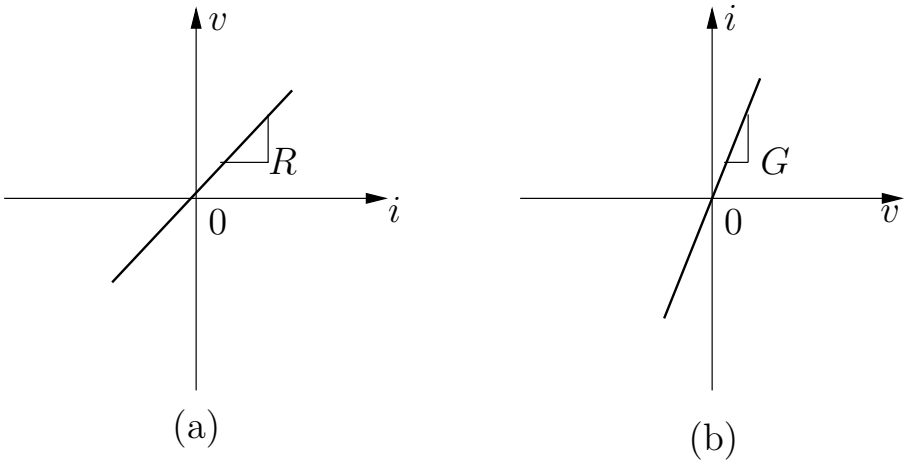


Fig. 1.14: Linear resistor characteristic plotted on the (a) $i-v$ and (b) $v-i$ plane.

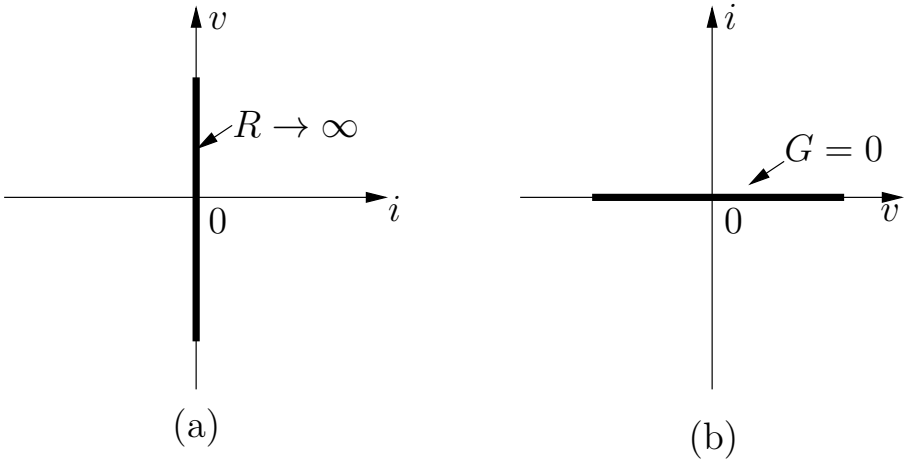


Fig. 1.15: Characteristic of an open circuit.

Comparing Figures 1.15 and 1.16, we see that the curve of the open circuit in one plane is identical to the curve of the short circuit in the other plane. For this reason, the open circuit is said to be the **dual** of the short circuit and vice-versa.

Example 1.9.1 A linear resistor with resistance of 100 Ω is given. What is its dual?

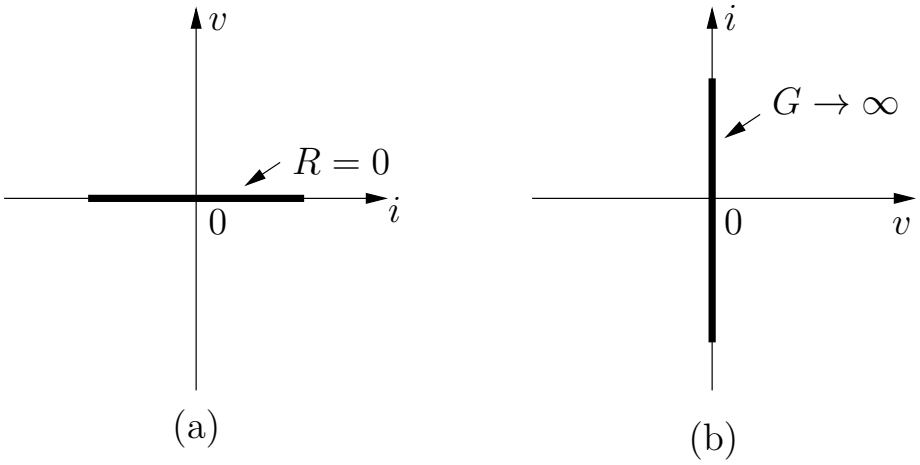


Fig. 1.16: Characteristic of a short circuit.

Solution: Consider a linear resistor with resistance $R = \frac{1}{100}\ \Omega$. The $i-v$ and $v-i$ characteristics are plotted in Fig. 1.17. Notice how the $i_1 - v_1$ characteristic of the resistor with $R = 100\ \Omega$ is equivalent to the $v_4 - i_4$ characteristic of the resistor with $R = \frac{1}{100}\ \Omega$. Similarly, the $v_2 - i_2$ characteristic for resistor with $R = 100\ \Omega$ is equivalent to the $i_3 - v_3$ characteristic for resistor with $R = \frac{1}{100}\ \Omega$. Hence the dual is a resistor with $R = \frac{1}{100}\ \Omega$.

From Eq. (1.9), the power delivered to a linear resistor at time t by the remainder of the circuit to which it is connected is:

$$\begin{aligned} p(t) &= v(t)i(t) \\ &= Ri^2(t) \\ &= Gv^2(t) \end{aligned} \tag{1.36}$$

Thus the power delivered to a linear resistor is always non-negative if $R \geq 0$. We say that a linear resistor is passive iff its resistance is non-negative. Thus a passive resistor always absorbs energy from the remainder of the circuit.

But from Eq. (1.36) we can see the power delivered to a linear resistor is negative if $R < 0$; i.e., as current flows through it, the resistor delivers energy to the remainder of the circuit. Therefore we call such a linear resistor with negative resistance an active resistor.

While linear passive resistors are familiar to everyone, linear active resistors are perhaps new to some readers. They are one of the basic circuit elements in the

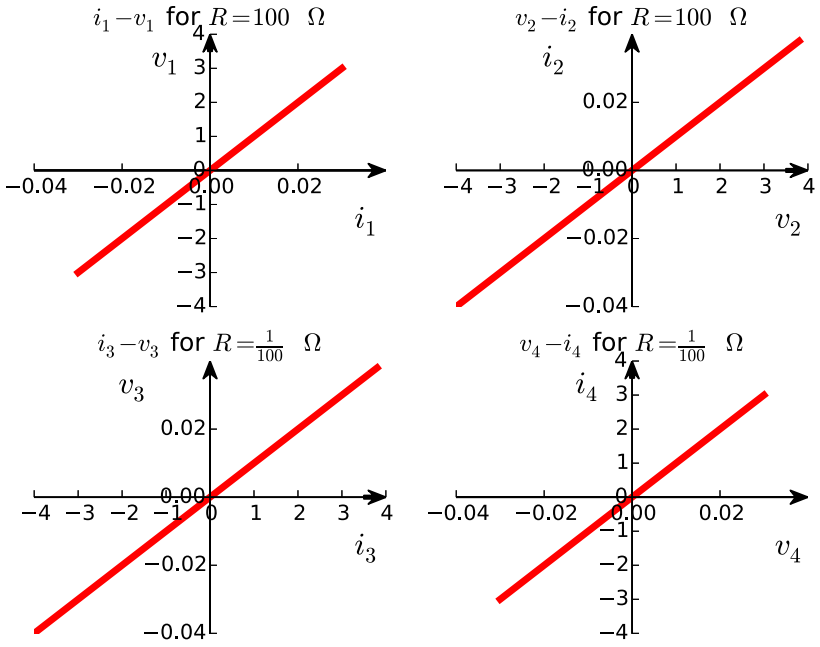


Fig. 1.17: $R = 100\ \Omega$ and $R = \frac{1}{100}\ \Omega$ are duals of each other. v_n is in volts and i_n is in amps.

design of negative resistance oscillators. We will show how to synthesize piecewise-linear negative resistors using opamps in section 2.5.3.2. We will discuss oscillator design in later parts of the book. For the present we only wish to mention that the linear active resistor is useful in modeling nonlinear devices and circuits over certain ranges of voltages, currents and frequencies.

While the linear resistor is perhaps the most prevalent circuit element in electrical engineering, nonlinear devices which can be modeled with nonlinear resistors have become increasingly important. Hence we will now define the concept of a nonlinear resistor in the most general way. Note that in keeping with the theme of the book, linear resistors (elements) will only be discussed as special cases of nonlinear resistors (elements).

In general, a two-terminal element will be called a resistor if its voltage v and current i satisfy the relation in Eq. (1.37):

$$\mathscr{R} = \{(v,i) : f_R(v,i) = 0\} \tag{1.37}$$

This relation is called the $v-i$ characteristic of the resistor and can be plotted graphically in the $v-i$ (or $i-v$) plane. We have already done so for linear resistors. The circuit symbol for the nonlinear resistor was shown in Fig. 1.1, reproduced in Fig. 1.18.

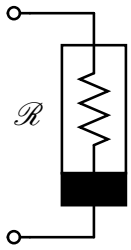


Fig. 1.18: Nonlinear resistor $\mathscr{R}$.

Note that in view of the nonsymmetrical nature of the circuit symbol for the nonlinear resistor (and nonlinear elements in general), we may avoid drawing the associated voltage (flux) polarity and current (charge) direction signs beside the symbol, **provided we agree to assume that the darkened edge is the negative terminal and current (charge) enters the positive terminal**. This convention will be followed in this book, when adding polarities and directions will clutter the circuit diagram.

Now we can generalize the concept of duality to nonlinear resistors: we say that the dual of a given resistor is another resistor whose $v-i$ characteristic in the $v-i$ plane is the same as that of the given resistor in the $i-v$ plane. We will revisit this concept of duality throughout the book and study it in detail in section 4.1.1, since it helps us in understanding and analyzing circuits of great generality.

In order to be able to use nonlinear resistors effectively in a practical design, it is necessary to understand some basic properties. We will illustrate these properties by considering a prototypical example of a nonlinear resistor, the *pn*-junction diode (henceforth referred to as diode).

Although we model diodes as nonlinear resistors, they are so important in circuit theory that they have their own symbol, shown in Fig. 1.19/ A typical $v-i$ characteristic is shown in Fig. 1.20.

In typical applications, the device is operated to the right of point A, where A is near the "knee" of the diode. In this range, the current obeys the diode junction law in Eq. (1.38).

$$i(v) = I_s[e^{\frac{v}{V_T}} - 1] \tag{1.38}$$

where I_s is a constant on the order of microamperes and it represents the reverse saturation current. The parameter $V_T = \frac{kT}{q}$ is called the thermal voltage, where q is

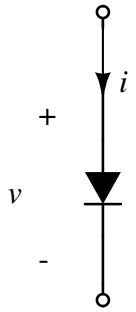


Fig. 1.19: Circuit symbol for a diode.

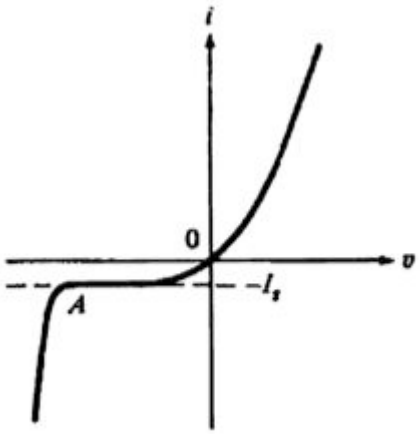


Fig. 1.20: Diode $v-i$.

the charge of an electron, k is Boltzmann's constant and T is the temperature in K. At room temperature, V_T is approximately 0.026 V.

In Eq. (1.38), we have a nonlinear resistor whose current i is expressed as a function of its voltage v. This means that for any given voltage v, the current i is uniquely specified. A nonlinear resistor having this property is called a **voltage-controlled nonlinear resistor**. By contrast, if the voltage is a single-valued function of the current $v = v(i)$, we have a **current-controlled nonlinear resistor**. Another important property shared by some $v-i$ curves is their symmetry with respect to the origin. Such elements are called **bilaterial resistors** because in this case, the two terminals may be interchanged without effecting the $v-i$ curve (see exercise 1.2).

Finally, if for each pair of points (v_1, i_1) and (v_2, i_2) on the curve, we observe that whenever $v_2 > v_1$ then $i_2 > i_1$, then the corresponding element is said to be **strictly monotonically increasing resistor**. An example is a linear passive resistor.

Note that while Eq. (1.38) represents a good model for the diode at low frequencies (recall section 1.8), we need to use additional circuit elements, capacitors, inductors and linear resistors to model the device at higher frequencies. A very important physical property of the diode, namely charge-storage effects are modeled by memristors. Memristors will be discussed in section 1.9.4.

Many practical diode circuits can be analyzed by a very simply piecewise-linear diode model, called the **ideal diode model**, described analytically by Eq. (1.39).

$$\begin{aligned} i &= 0 \quad \forall v < 0 \\ v &= 0 \quad \forall i > 0 \\ p &= vi = 0 \quad \forall v, i \end{aligned} \tag{1.39}$$

Observe that the last constraint is introduced to eliminate any point in the fourth quadrant from becoming a part of the $v-i$ curve. It is also important to observe that an ideal diode becomes an open circuit for $v < 0$ and a short circuit for $i > 0$.

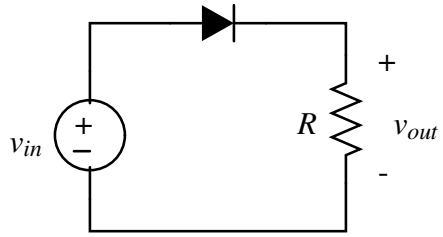


Fig. 1.21: Circuit for example 1.9.2.

Example 1.9.2 Consider the circuit shown in Fig. 1.21. Discuss what would be the output voltage $v_{out}(t)$ if $v_{in}(t) = \sin(\pi t)$, assuming the ideal diode model.

Solution: The circuit in Fig. 1.21 is the first step in converting an AC (alternating current or time-varying) voltage into a DC (direct current or constant) voltage, a process called rectification. The terms AC and DC are so named because in AC, the electric charge (and hence voltage) reverses (or alternates) direction periodically. In DC, the electric charge flows in only one direction.

The output voltage v_{out} for a sinusoidal v_{in} is shown in Fig. 1.22. When the input voltage $v_{in}(t)$ is positive, the diode becomes a short circuit and $v_{out}(t) = v_{in}(t)$. When the input voltage is negative, the diode becomes an open circuit and $v_{out}(t) = 0$. The result is that the output voltage becomes zero during every other half cycle.

The circuit in Fig. 1.21 is called a half-wave rectifier, since the negative half cycle is simply zeroed out, instead of being rectified.

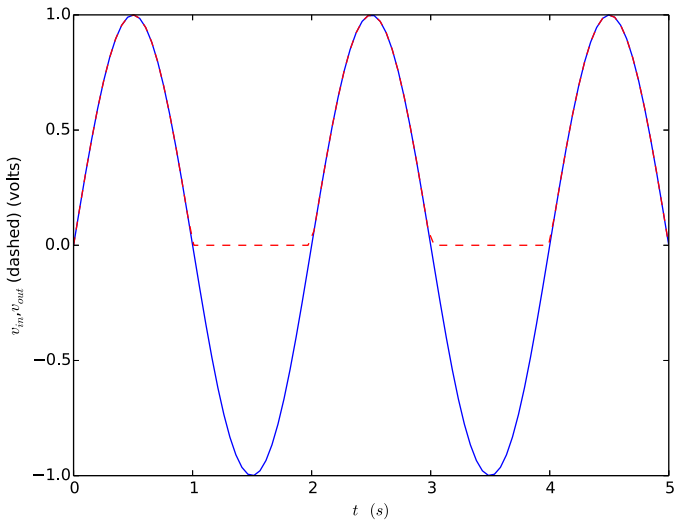


Fig. 1.22: $v_{in}(t)$ (solid) and $v_{out}(t)$ (dashed) for the circuit in Fig. 1.21.

Although the rectifier in example 1.9.2 uses an ideal diode, the above example illustrates a universal principle of creative design: first arrive at an idealized network (which is usually much easier to come by) and then introduce physical non-idealities as necessary.

1.9.2 Independent Sources

Note that in example 1.9.2, we encountered a sinusoidal **voltage source**. Sources are a very important class of two-terminal devices because electrical energy must be supplied in order to move the charges which constitute current i. Of course energy cannot be created or destroyed, electrical sources simply transform some other form of energy into electrical energy. For instance, a battery transforms chemical energy into electrical energy. We will encounter two[6] types of sources[7]:

[6] We will not use charge and flux-linkage sources in this book.

[7] We will postpone discussion of the very important class of dependent sources till section 2.5.2, after we have discussed two-port representation in section 2.2.1.

Definition 1.18. An independent voltage source is a two-terminal device whose terminal voltage v is always equal to some given function of time $v_s(t)$; regardless of the value of current flowing through it.

The dual of the independent voltage source is the independent current source.

Definition 1.19. An independent current source is a two-terminal device whose terminal current i is always equal to some given function of time $i_s(t)$; regardless of the value of voltage across its terminals.

The circuit symbol(s) for independent voltage and current sources are shown in Fig 1.23.

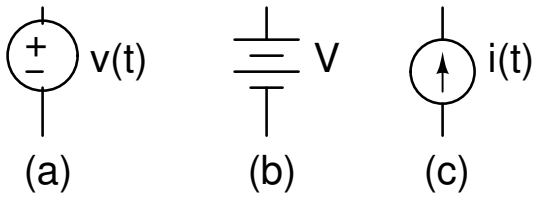


Fig. 1.23: Symbols for independent voltage and current sources. An independent DC voltage source can also be indicated by the standard battery symbol shown in (b).

On many occasions, we shall find it convenient to consider a DC voltage source and a DC current source as nonlinear resistors. This interpretation is valid because, by definition, a DC voltage source with terminal voltage E can be represented by the vertical line $v = E$ in the $v - i$ plane. Similarly, a DC current source with terminal current I can be represented by the horizontal line $i = I$ in the $v - i$ plane.

1.9.3 Inductors and Capacitors

In this section, we introduce inductors and capacitors. To emphasize the "dual" character of these two elements, we will use a two-column format so that each statement on the left is the dual of the one on the right. Once the reader gets used to the idea of duality, they need only read one column while mentally reflecting on the dual statement in the other column.

An inductor is defined by

$$\mathscr{L} = \{(\phi, i) : f_L(\phi, i) = 0\} \qquad (1.40)$$

A capacitor is defined by

$$\mathscr{C} = \{(q, v) : f_C(q, v) = 0\} \qquad (1.48)$$

The circuit symbol for an inductor is shown in Fig. 1.24, reproduced from Fig. 1.1.

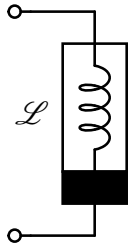


Fig. 1.24: Nonlinear inductor $\mathscr{L}$.

If Eq. (1.40) can be solved for i as a single-valued function of ϕ, namely:

$$i = \hat{i}(\phi) \tag{1.41}$$

the inductor is said to be **flux-controlled**. If Eq. (1.40) can be solved as a single-valued function of i, namely:

$$\phi = \hat{\phi}(i) \tag{1.42}$$

then the inductor is said to be **current-controlled**. If the function $\hat{\phi}(i)$ is differentiable, we can apply the chain rule in Eq. (1.42) to obtain:

$$v = L(i)\frac{di}{dt} \tag{1.43}$$

where

$$L(i) \triangleq \frac{d\hat{\phi}(i)}{di} \tag{1.44}$$

The circuit symbol for the capacitor is shown in Fig. 1.27, reproduced from Fig. 1.1.

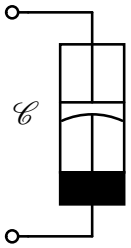


Fig. 1.27: Nonlinear capacitor $\mathscr{C}$.

If Eq. (1.48) can be solved for v as a single-valued function of q, namely:

$$v = \hat{v}(q) \tag{1.49}$$

the capacitor is said to be **charge-controlled**. If Eq. (1.48) can be solved as a single-valued function of v, namely:

$$q = \hat{q}(v) \tag{1.50}$$

then the capacitor is said to be **voltage-controlled**. If the function $\hat{q}(v)$ is differentiable, we can apply the chain rule in Eq. (1.50) to obtain:

$$i = C(v)\frac{dv}{dt} \tag{1.51}$$

where

$$C(v) \triangleq \frac{d\hat{q}(v)}{dv} \tag{1.52}$$

Example 1.9.3 Analyze the system shown in Fig. 1.25, where we have a conducting wire wound around a toroid made of a non-metallic material.

Example 1.9.3 Analyze the system shown in Fig. 1.28, where we have two flat parallel metal plates separated by a distance d.

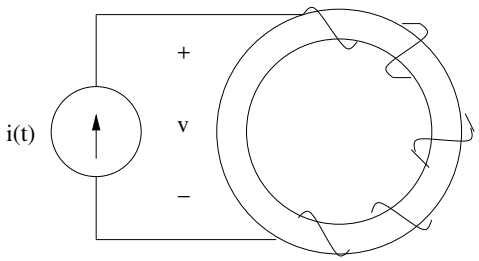


Fig. 1.25: Toroidal inductor.

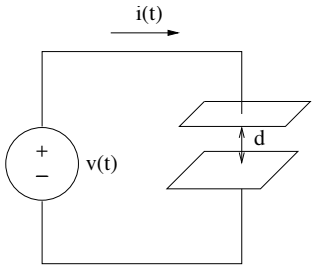


Fig. 1.28: Parallel-plate capacitor.

Solution: When a current $i(t)$ is applied, we recall from physics that a flux equal to $\phi(t) = Li(t)$ is induced at time t and circulates around the interior of the toroid. The constant of proportionality is given approximately by $L = \mu_0 \frac{N^2 A}{l}\ H$ where $\mu_0 = 4\pi \cdot 10^{-7}\ H/m$ is the permeability of the core, N is the number of turns of the coil, A is the cross-sectional area in m^2 and l is the midcircumference along the toroid in m. Hence, in Eq. (1.44), we will have $L(i) = L$ (a constant) and thus we have the classic linear time-invariant inductor from circuit theory, with the relation:

$$v = L\frac{di}{dt} \qquad (1.45)$$

For the properties below, we will assume linear time-invariant inductors and address properties for the nonlinear counterparts in chapter 4.

Memory Property:

Suppose we apply a voltage source $v(t)$ across an inductor L. The inductor current can be obtained by integrating Eq. (1.45) (assuming $i(t \to -\infty) = 0$):

Solution: When a voltage $v(t)$ is applied, we recall from physics that a charge equal to $q(t) = Cv(t)$ is induced at time t on the upper plate, and an equal but opposite charge is induced on the lower plate at time t. The constant of proportionality is given approximately by $C = \varepsilon_0 \frac{A}{d}\ F$ where $\varepsilon_0 = 8.85 \cdot 10^{-12}\ F/m$ is the permittivity of free space, A is the plate area in m^2 and d is the separation of the plate in m. Hence, in Eq. (1.52), we have $C(v) = C$ (a constant) and thus we have the classic time-invariant capacitor from circuit theory, with the relation:

$$i = C\frac{dv}{dt} \qquad (1.53)$$

For the properties below, we will assume linear time-invariant capacitors and address properties for the nonlinear counterparts in chapter 4.

Memory Property:

Suppose we connect a current source $i(t)$ in series with capacitor C. The capacitor voltage can be obtained by integrating Eq. (1.53) (assuming $v(t \to -\infty) = 0$):

$$i(t) = \frac{1}{L}\int_{-\infty}^{t} v(\tau)d\tau \; t \geq t_0 \qquad (1.46)$$

Hence the inductor current depends on the entire past history of $v(\tau)$. Therefore the inductor has **memory**.

Suppose however that current $i(t_0)$ at some time $t_0 < t$ is given, then we get:

$$i(t) = i(t_0) + \frac{1}{L}\int_{t_0}^{t} v(\tau)d\tau \; t \geq t_0 \qquad (1.47)$$

In other words, instead of specifying the entire past history, we need only specify $i(t)$ at some conveniently chosen initial time t_0. In effect, the initial condition $i(t_0)$ summarizes the effect of $v(\tau)$ from $\tau \to -\infty$ to $\tau = t_0$, on the present value of $i(t)$. We can draw an equivalent circuit symbolizing the memory effect as shown in Fig 1.26.

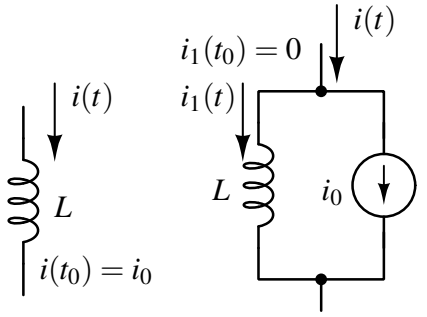


Fig. 1.26: Initial condition transformation for L.

Continuity Property:
Suppose we apply a voltage source described by a discontinuous square wave across an inductor, then the current through the inductor is given by Eq. (1.47). Assuming that $i(t_0) = 0$, we will obtain continuous inductor current waveform. This "smoothing" phenomenon turns out

$$v(t) = \frac{1}{C}\int_{-\infty}^{t} i(\tau)d\tau \; t \geq t_0 \qquad (1.54)$$

Hence the capacitor voltage depends on the entire past history of $i(\tau)$. Therefore the capacitor has **memory**.

Suppose however that voltage $v(t_0)$ at some time $t_0 < t$ is given, then we get:

$$v(t) = v(t_0) + \frac{1}{C}\int_{t_0}^{t} i(\tau)d\tau \; t \geq t_0 \qquad (1.55)$$

In other words, instead of specifying the entire past history, we need only specify $v(t)$ at some conveniently chosen initial time t_0. In effect, the initial condition $v(t_0)$ summarizes the effect of $i(\tau)$ from $\tau \to -\infty$ to $\tau = t_0$, on the present value of $v(t)$. We can draw an equivalent circuit symbolizing the memory effect as shown in Fig 1.29.

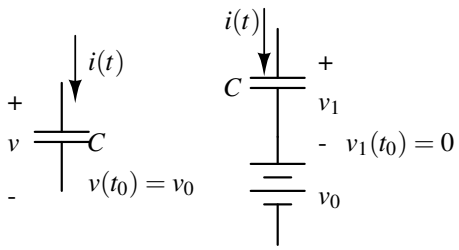


Fig. 1.29: Initial condition transformation for C.

Continuity Property:
Suppose we apply a current source described by a discontinuous square wave through a capacitor, then the voltage across the capacitor is given by Eq. (1.55). Assuing $v(t_0) = 0$, we will obtain continuous capacitor voltage waveform. This "smoothing" phenomenon turns out to

to be a general property.

If the voltage waveform $v_L(t)$ across a linear time-invariant inductor L remains bounded in a closed interval $[t_a, t_b]$, then the current waveform $i_L(t)$ through the inductor is a continuous function in the open interval (t_a, t_b). In particular, for any time T satisfying $t_a < T < t_b$, $i_L(T^-) = i_L(T^+)$.

be a general property.

If the current waveform $i_C(t)$ in a linear time-invariant capacitor C remains bounded in a closed interval $[t_a, t_b]$, then the voltage waveform $v_C(t)$ across the capacitor is a continuous function in the open interval (t_a, t_b). In particular, for any time T satisfying $t_a < T < t_b$, $v_C(T^-) = v_C(T^+)$.

The continuity property for inductors and capacitors is so important that we will prove the continuity property for a capacitor (the inductor follows by duality).

Consider Eq. (1.55). Substituting $t = T$ and $t = T + dt$ into Eq. (1.55) where $t_a < T < t_b$ and $t_a < T + dt \leq t_b$, and subtracting, we get:

$$v_C(T + dt) - v_C(T) = \frac{1}{C} \int_T^{T+dt} i_C(\tau) d\tau \tag{1.56}$$

Since we have assumed $i_C(t)$ to be bounded in $[t_a, t_b]$, there is a finite constant M such that $|i_C(t)| < M$, $\forall t \in [t_a, t_b]$. It follows that the area under the curve $i_C(t)$ from T to $T + dt$ is at most $M dt$ (in absolute value), which tends to zero as $dt \to 0$. Hence Eq. (1.56) implies $v_C(T + dt) \to v_C(T)$. Therefore $v_C(t)$ is continuous at $t = T$.

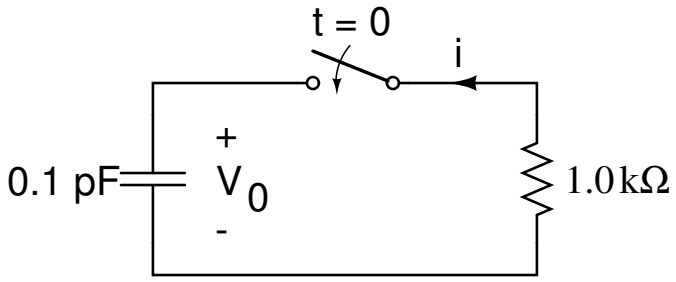


Fig. 1.30: Figure for example 1.9.4.

Example 1.9.4 Find the value $i(0^+)$ in Fig. 1.30, assuming the capacitor is precharged to $0.5\,V$ and the ideal switch instantaneously closes at $t = 0$.
Solution:
Since the capacitor is precharged to $0.5\,V$, $v_0(0^-) = 0.5\,V$. By the continuity property for capacitors, $v_0(0^+) = 0.5\,V$. Since we have a linear resistor, by Ohm's law and the passive sign convention:

$$\begin{aligned} i &= -\frac{0.5\,V}{1.0\,k\Omega} \\ &= -0.5\,mA \end{aligned} \tag{1.57}$$

The continuity property will be further utilized in Chapter 4, where we apply it to solve[8] a variety of circuits that exhibit switching discontinuities.

1.9.4 Memristors

Looking at Fig. 1.1 and based on our discussions of the other fundamental circuit elements, it is only **natural** that, by **symmetry** arguments, there exists a fourth fundamental circuit element for establishing a $\phi - q$ relationship:

$$\mathscr{M} = \{(\phi, q) : f_M(\phi, q) = 0\} \tag{1.58}$$

Such an element was defined by Dr. Chua in 1971 [2]. Nevertheless investigations of this element began in earnest only after HP's announcement in 2008 [22]. HP's memristor is a very specific TiO_2 based device, and most works nowadays are focused on memristors as a form of resistive random-access memory.

We will rather study general characteristics of this device. Interestingly, literature survey gives a wealth of insight into this device, and hence we will begin our study with the very first citations of Chua's seminal work.

Dr. Penfield, in a MIT technical report [18], mentions the memristor in connection with the Josephson junctions. Throughout the late 20th century, a plethora of research [10], [16], [17], [24] regarding the "phase-dependent conductance" in Josephson junctions were carried out. But a proper memristor approach to interpreting the "phase-dependent conductance" occurred only with Peotta and Di Ventra's seminal paper in 2014 [19]. However, before we examine the ideal memristor in Josephson junctions, we will state some important properties of the memristor [2].

Consider a function of q based on Eq. (1.58):

$$\phi = g(q) \tag{1.59}$$

Differentiating both sides of Eq. (1.59) with respect to time and applying the chain rule, we get:

[8] By "solve" a circuit, we mean to find the voltage across and current through every branch for all times t.

$$\begin{aligned}\frac{d\phi}{dt} &= \frac{dg(q)}{dt} \\ &= \frac{dg}{dq}\frac{dq}{dt}\end{aligned} \tag{1.60}$$

From Eq. (1.3), $i = \frac{dq}{dt}$ and from Eq. (1.4), $v = \frac{d\phi}{dt}$. Hence we have the memristor $v-i$ relation in Eq. (1.61).

$$v(t) = M(q(t))i(t) \tag{1.61}$$

$M(q(t))$ in Eq. (1.62) is defined as the **incremental memristance**, we can analogously define a $W(\phi(t))$ as **incremental menductance**[9].

$$i(t) = W(\phi(t))v(t) \tag{1.62}$$

We can make the following observations from Eq. (1.61) (analogous observations hold for Eq. (1.62)):

1. $M(q(t)) = M(\int_{-\infty}^{t} i(\tau)d\tau)$. Hence the fact that memristor stands for "memory-resistor" can be justified: the value of the memristance at any time t depends on the time integral of the memristor current from $-\infty$ to t. Therefore while the memristor behaves like an ordinary resistor at a **given instant** of time, its **resistance depends on the complete past history (or memory)** of memristor current.
2. In the very special case where the memristor $\phi - q$ curve is a straight line, we obtain $M(q) = R$, the memristor reduces to a linear time-invariant resistor.

Point 2. above illustrates why the memristor is not relevant in linear circuit theory: unlike the other three fundamental circuit elements (resistor, inductor, capacitor), **a memristor is a fundamentally nonlinear device, a linear memristor is simply a resistor**. Hence techniques from nonlinear circuit theory are essential to understanding memristor functionality.

We can now discuss the phase-dependent conductance in Josephson junction as an ideal memristor. Before doing so we will derive the Josephson relation from first principles, since not only does this relation utilize fundamental physical principles, but it also helps us practice our definitions of the fundamental circuit variables.

Consider the Josephson junction (JJ) shown in Fig. 1.31.

From basic physics, we know that energy E is quantized from the Planck-Einstein relation:

$$E = h\nu \tag{1.63}$$

Rewriting Eq. (1.63), we get:

[9] To avoid clutter, we will use the terms memristance and menductance from now on. We will reserve the use of "incremental" for clarity purposes.

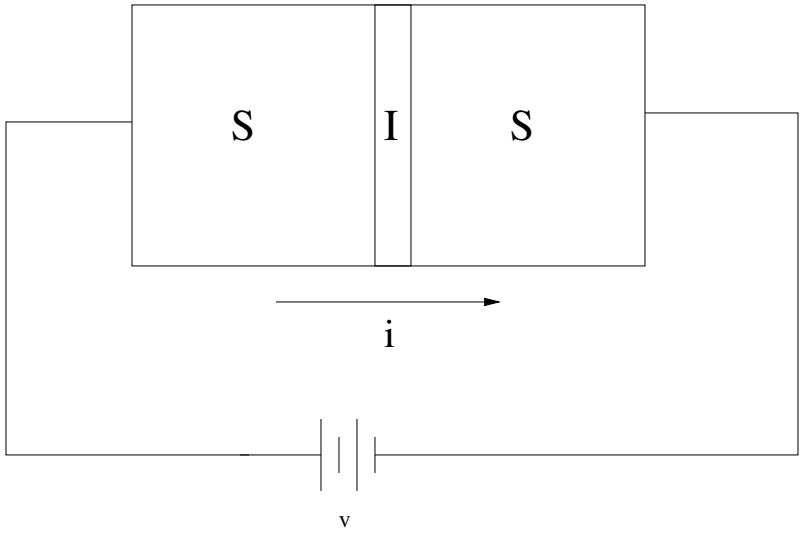


Fig. 1.31: A Josephson junction formed by using a superconductor-insulator-superconductor setup. The barrier I is thin enough (on the order of a few angstroms) that superconducting Cooper pairs can tunnel across the junction when $v = 0$ [9].

$$E = h\frac{\omega}{2\pi} \tag{1.64}$$

In Eq. (1.63), ν is frequency in Hz and in Eq. (1.64), ω is angular frequency in rad/s.

In a physical JJ in the superconducting state, a quantum mechanical phase difference Φ is established between the two superconductors. Therefore, we have:

$$E = \frac{h}{2\pi}\frac{d\Phi}{dt} \tag{1.65}$$

Based on Eq. (1.1), we have:

$$2e^{-}v = \frac{h}{2\pi}\frac{d\Phi}{dt} \tag{1.66}$$

We have used $2e^{-}$ because Cooper pairs carry the charge in the superconducting state. Using Eq. (1.4), defining $\hbar \stackrel{\triangle}{=} \frac{h}{2\pi}$ and simplifying, we get:

$$\frac{d\phi}{dt}\left(\frac{2e^{-}}{\hbar}\right) = \frac{d\Phi}{dt} \tag{1.67}$$

In Eq. (1.67), we can define $\phi_0 \stackrel{\triangle}{=} \phi / \frac{\hbar}{2e^-}$. In other words, the quantum mechanical phase difference across the junction is quantized as a function of the magnetic flux through the loop ($\frac{h}{2e^-}$ is the magnetic flux quantum): $\Phi = \phi_0$. Eq. (1.67) is the **fundamental Josephson relation**.

The current i through the junction can be written [9] as:

$$i(v) = I_c \sin(\phi_0) + \sigma_0(v)v + \varepsilon \cos(\phi_0)v + \cdots \tag{1.68}$$

In Eq. (1.68), I_c, ε are constants based on the physical superconducting materials and $\sigma_0(v)$ is the nonlinear conductance for the particular JJ. But, the important point is to notice how the current i will be non-zero even if the voltage across the junction is zero! This is due to the Josephson current $I_j = I_c \sin(\phi_0)$. The mindful reader should have noticed that we can model a JJ as a nonlinear inductor, when $v = 0$.

But the important point is that the third term in Eq. (1.68) can be written as:

$$i_3(v) = W(\phi_0)v \tag{1.69}$$

This equation is precisely the equation of an ideal memristor (the device is technically a menductor). But there are two issues in trying to design an ideal memristor:

1. The Josephson current I_j is usually much larger when compared to the memristance term i_3.
2. The memristance term is non-zero only when the voltage across the junction is non-zero. And in this case, it is oscillating at a very high frequency[10].

Nevertheless, Peotta and Di Ventra propose an elegant approach [19] to isolate the memristance term: utilize two Josephson junctions of different material, connected in parallel, to cancel the Josephson current.

But how do we identify a memristive two-terminal blackbox? The answer lies in our definition : since $v(t)$ ($i(t)$) has to be zero whenever $i(t)$ ($v(t)$) is zero for a memristor (menductor), under periodic excitation, a memristor distinctly displays a Lissajous figure in the $v-i$ plane.

However, in the case of the ideal memristor in the Josephson junction, we still have the issue of the $\cos\phi_0$ term oscillating at very high frequencies for practical measurements. Thus, are there other memristive devices that we can easily study experimentally?

The answer is yes! For studying other memristive devices, we will use the generalization of an ideal memristor to a general memristive device, as defined by Chua and Kang [3].

An nth-order current-controlled memristive one-port is represented by:

$$\begin{aligned} \dot{x} &= f(x,i,t) \\ v &= R(x,i,t)i \end{aligned} \tag{1.70}$$

[10] Private email communication from Dr. Brian Josephson to Dr. Muthuswamy on March 14th 2014.

An nth-order voltage-controlled memristive one-port is represented by:

$$\begin{aligned} \dot{x} &= f(x,v,t) \\ i &= G(x,v,t)v \end{aligned} \tag{1.71}$$

A variety of physical devices are memristive in nature. We will examine one of these devices: a discharge tube, whose resistance is a function of the number of conduction electrons n_e [12]. Consider Eq. (1.72):

$$\begin{aligned} v_M &= R(n_e)i_M \\ \dot{n}_e &= -\beta n + \alpha R(n_e)i_M^2 \end{aligned} \tag{1.72}$$

v_M is the voltage across the discharge tube, i_M is the current flowing through it and n_e is the number of conduction electrons. $R(n_e) = \frac{F}{n_e}$. α, β, F are parameters depending on the dimensions of the tube and the gas fillings. Comparing Eqs. (1.70) and (1.72), we can clearly see that a discharge tube can be modeled as a current-controlled memristor.

Fig. 1.32 shows a simulated $v_M - i_M$ curve and Fig. 1.33 shows an oscilloscope screenshot of a measured discharge tube characteristic.

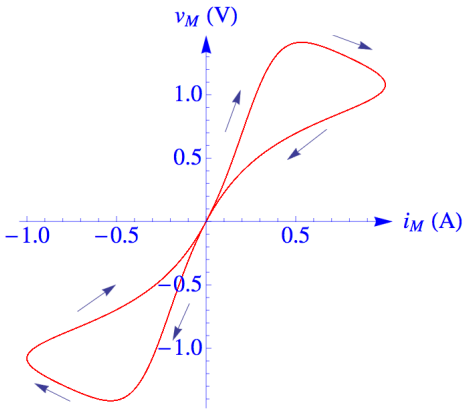


Fig. 1.32: Simulated Lissajous figure for $i_M(t) = \sin(\omega t)$ in Eq. (1.72), with $\alpha = 0.1, \beta = 0.1, F = 1, \omega = 0.063$.

We will have more to discuss about other memristive devices such as thermistors in section 4.3.2.

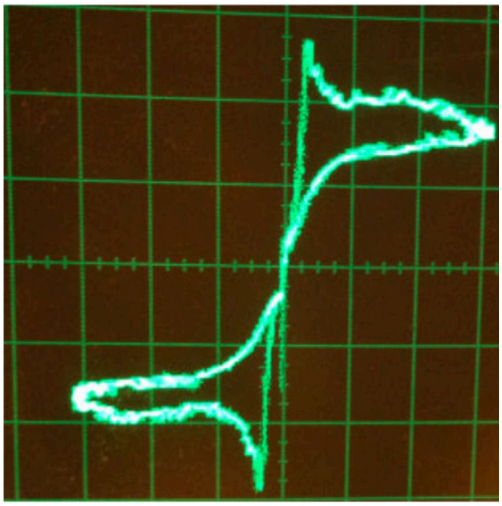


Fig. 1.33: Measured discharge tube characteristics. We have plotted v_M on the Y-axis (2 V/div) and have scaled i_M to voltage for ease of plotting on the X-axis (5 V/div).

1.9.5 Periodic Table of Circuit Elements

Sections 1.9.1 through 1.9.4 have helped us discuss the four fundamental circuit elements in Fig. 1.1. The elements are fundamental in the sense that no element from this basic set can be derived from the other three elements [4].

In fact, we can generalize Fig. 1.1 to **higher-order** circuit elements. As a motivating example, consider Eq. (1.73) of the Duffing oscillator. This oscillator is used to model a variety of phenomena in science. We will discuss a circuit implementation of this oscillator in section 5.2.

$$\ddot{v} + \delta\dot{v} + v(\beta + \alpha v^2) = i(t) \tag{1.73}$$

Since we are forcing a current input on the RHS, each expression on the LHS of Eq. (1.73) represents current. Thus, by KCL, we simply have three elements in parallel to an ideal current source.

From Eq. (1.53), we know that the current through a capacitor is proportional to the first derivative of the voltage across it. Hence, $\delta\dot{v}$ in Eq. (1.53) can be modeled by a linear time-invariant capacitor. We will learn when we synthesize this oscillator in section 5.2 that a tunnel diode has a cubic $i(v)$ and hence can be used to synthesize the $v(\beta + \alpha v^2)$ term. But, does there exist a two-terminal element whose current through the terminals is proportional to the **second derivative** of the voltage across it?

Although the current answer to the question is "we do not know", Eq. (1.73) shows the **necessity** of defining such a circuit element. Of course, one could also ask: why not simply build an analog computer that solves Eq. (1.73)? The answer is: the analog computer will not help us study the underlying physical phenomenon. As an analogy, consider a mass-spring-damper model of a second-order system. The equivalent analog computer implementation is simply a "signal flow" graph and cannot yield insightful information, say, the energy transfer between the mass and the spring.

Hence, we need to expand our repertoire of fundamental circuit elements from Fig. 1.1, by introducing a sufficiently rich family of elementary circuit elements [6] which play the same role as the set of basis vectors to define a vector space.

The key concept is the following definition.

Definition 1.20. A two-terminal or one-port black box characterized by a constitutive relation in the $v^{(\alpha)} - i^{(\beta)}$ plane is called an (α, β) element, where $v^{(\alpha)}$ and $i^{(\beta)}$ are variables derived from voltage $v(t)$ and current $i(t)$ below.

$$v_k^{(\alpha_k)}(t) \triangleq \begin{cases} \frac{d^{\alpha_k} v_k(t)}{dt^{\alpha_k}} & \text{if } \alpha_k > 0 \\ v_k(t) & \text{if } \alpha_k = 0 \\ \int_{-\infty}^{t} \int_{-\infty}^{\tau_{k-1}} \cdots \int_{-\infty}^{\tau_2} v_k(\tau_1) d\tau_1 d\tau_2 \cdots d\tau_{\alpha_k} & \text{if } \alpha_k < 0 \end{cases} \tag{1.74}$$

$$i_k^{(\beta_k)}(t) \triangleq \begin{cases} \frac{d^{\beta_k} i_k(t)}{dt^{\beta_k}} & \text{if } \beta_k > 0 \\ i_k(t) & \text{if } \beta_k = 0 \\ \int_{-\infty}^{t} \int_{-\infty}^{\tau_{k-1}} \cdots \int_{-\infty}^{\tau_2} i_k(\tau_1) d\tau_1 d\tau_2 \cdots d\tau_{\beta_k} & \text{if } \beta_k < 0 \end{cases} \tag{1.75}$$

The circuit symbol for $v^{(\alpha)}$-$i^{(\beta)}$ element is shown in Fig 1.34.

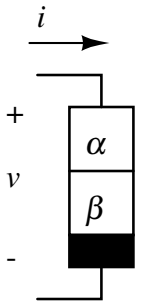


Fig. 1.34: Two terminal or one-port representation of (α, β) element.

In other words, based on Eqs. (1.74) and (1.75), we can make the following observations:

1. Every (0,0) element is a resistor $\mathscr{R}$

2. Every (-1,0) element is an inductor $\mathscr{L}$
3. Every (0,-1) element is a capacitor $\mathscr{C}$
4. Every (-1,-1) element is a memristor $\mathscr{M}$

Thus, based on our discussion so far and KCL, a circuit equivalent of Eq. (1.73) is shown in Fig. 1.35.

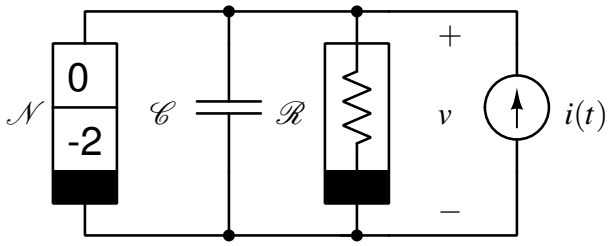


Fig. 1.35: A circuit realization of the Duffing oscillator

We will revisit and synthesize (α,β) elements in section 2.5.5, once we understand how to use opamps in circuit synthesis. It turns out that we need only two opams to synthesize the $v^{(0)} - i^{(-2)}$ element!

It is instructive to visualize the (α,β) elements in the form of a "periodic table" in Fig. 1.36, that expands the basic four element quadrangle from Fig. 1.1.

In Fig. 1.36, all elements printed in the same color belong to the same element "species" and, notice that there are only four colors. The justification for the "periodic table" label and a rigorous analysis of Fig. 1.36 will be done in section 4.5.

1.10 Series and Parallel Connections of Resistors

We are now in a position to consider a special but very important class of circuits: circuits formed by series and parallel connections of two-terminal resistors. First, we wish to generalize the concept of the $v-i$ characteristic of a resistor to that of a two-terminal circuit made of two-terminal resistors, or more succinctly, a **resistive one-port**. We will demonstrate that the series and parallel connections of two-terminal resistors will yield a one-port whose $v-i$ characteristic is again that of a resistor. We say that two resistive one-ports are equivalent iff their $v-i$ characteristics are the same.

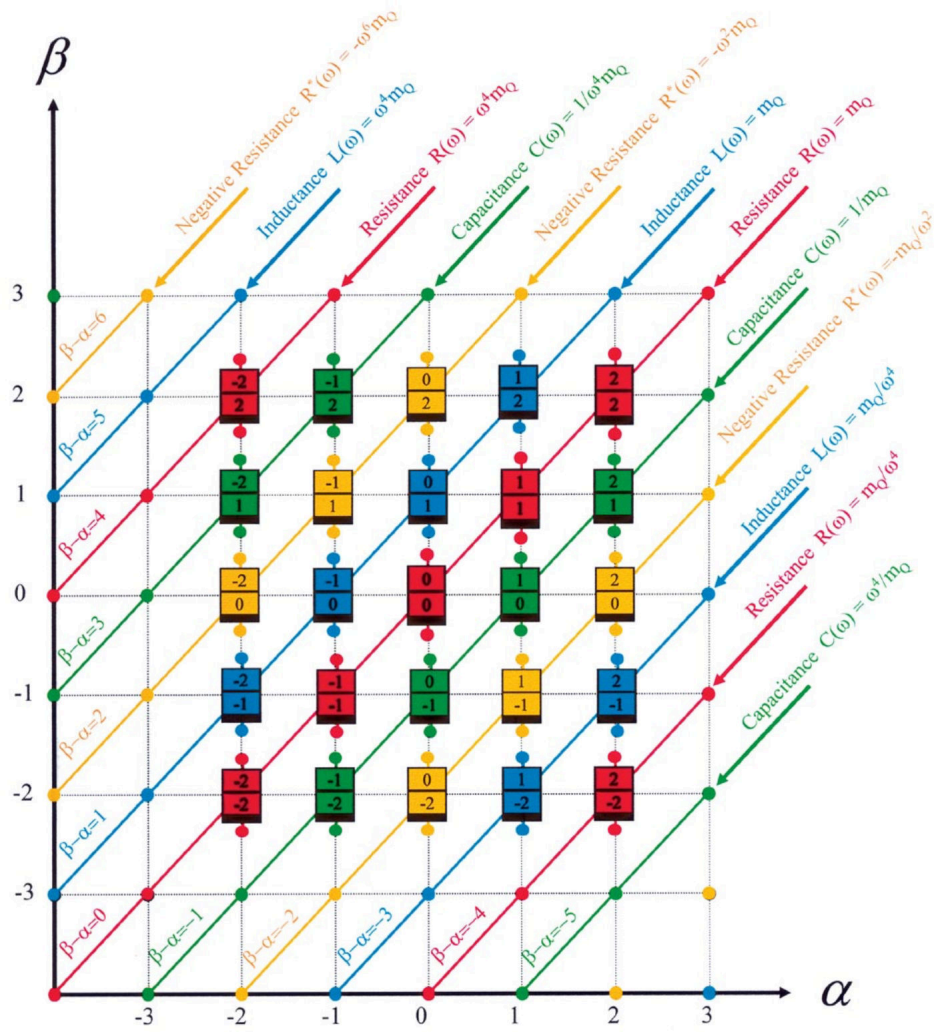


Fig. 1.36: The periodic table of all two-terminal (α, β) elements, adopted from [6]. m_Q is defined as a small-signal slope about an operating point, and will be rigorously discussed in section 4.5.

When we talk about resistive one-ports, we naturally use **port voltage** and **port current** as the pertinent variables. The $v - i$ characteristic of a one-port in terms of its port voltage and port current is often referred to as the **driving-point or DP characteristic**[11] of the one-port. The reason we call it the DP characteristic is that

[11] We will discuss DP characteristics in detail in section 3.7.1.

we may consider the one-port as being driven by an independent voltage source v_s or an independent current source i_s. In the former, the input is $v_s = v$ and the response is the current i. In the latter, the input is $i_s = i$ and the response is v.

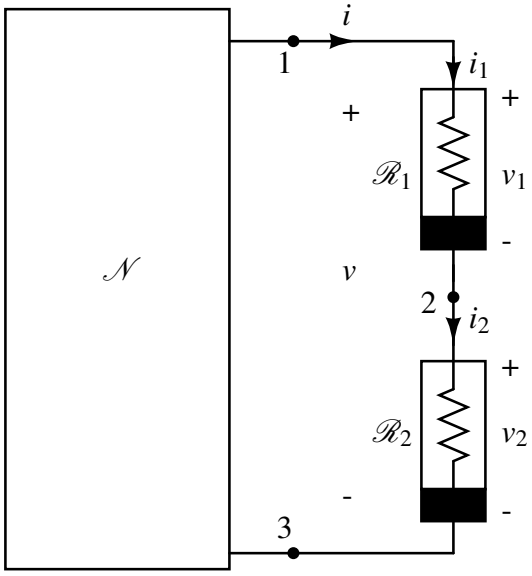


Fig. 1.37: Two nonlinear resistors connected in series together with the rest of the circuit $\mathscr{N}$.

Consider the circuit shown in Fig. 1.37 where two nonlinear resistors $\mathscr{R}_1$ and $\mathscr{R}_2$ are connected at node 2. Nodes 1 and 3 are connected to the rest of the circuit, which is designated by $\mathscr{N}$. Looking towards the right from nodes 1 and 3, we have a one-port which is formed by the **series connection of two resistors** $\mathscr{R}_1$ and $\mathscr{R}_2$. For our present purposes, the nature of $\mathscr{N}$ is irrelevant. We are interested in obtaining the DP characteristic of the one-port with port voltage v and port current i.

Let us assume that both resistors are current-controlled, i.e.,

$$\begin{aligned} v_1 &= \hat{v}_1(i_1) \\ v_2 &= \hat{v}_2(i_2) \end{aligned} \tag{1.76}$$

Notice that these are the laws of elements. Next, applying KVL for the node sequence $1-2-3-1$ gives:

$$v = v_1 + v_2 \tag{1.77}$$

Applying KCL to nodes 1 and 2 gives:

$$i = i_1 = i_2 \tag{1.78}$$

Combining Eqs. (1.76), (1.77), (1.78), we obtain:

$$v = \hat{v}(i)$$
$$\text{where } \hat{v}(i) \stackrel{\triangle}{=} \hat{v}_1(i) + \hat{v}_2(i) \tag{1.79}$$

Note that Eq. (1.79) can be extended to n nonlinear resistors $\mathscr{R}_n$ in series. Thus, we can conclude that:

1. KVL requires the port voltage v to be equal to the sum of the branch voltages of the resistors.
2. KCL forces all branch currents to be equal to the port current.
3. If each resistor is current-controlled, the resulting DP characteristic of the one-port is also a current-controlled resistor.

Example 1.10.1 Determine $\hat{v}(i)$ if the two terminals of $\mathscr{R}_1$ in Fig. 1.37 are turned around.
Solution: The new circuit is redrawn in Fig. 1.38. Hence, the $v-i$ characteristic for $\mathscr{R}_1$ is now:

$$v_1 = \hat{v}_1(-i_1) \tag{1.80}$$

KVL gives:

$$v = -v_1 + v_2 \tag{1.81}$$

Thus, we have:

$$v = -\hat{v}_1(-i) + \hat{v}_2(i) \tag{1.82}$$

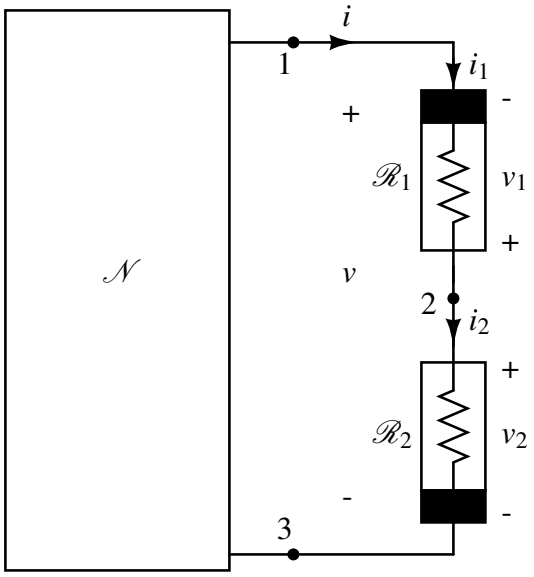


Fig. 1.38: Circuit for example 1.10.1.

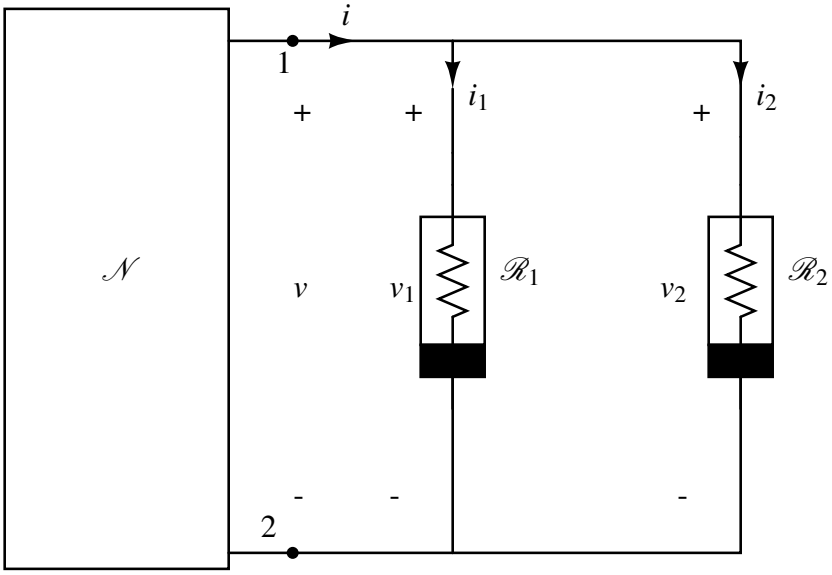


Fig. 1.39: Two nonlinear resistors connected in parallel together with the rest of the circuit $\mathscr{N}$.

Consider the circuit shown in Fig. 1.39 where two nonlinear resistors $\mathscr{R}_1$ and $\mathscr{R}_2$ are connected across nodes 1 and 2 to the rest of the circuit, which is designated by $\mathscr{N}$. Looking towards the right from nodes 1 and 2, we have a one-port

which is formed by the **parallel connection of two resistors** $\mathscr{R}_1$ and $\mathscr{R}_2$. For our present purposes, the nature of $\mathscr{N}$ is irrelevant. We are interested in obtaining the DP characteristic of the one-port with port voltage v and port current i.

Let us assume that both resistors are voltage-controlled, i.e.,

$$\begin{aligned} i_1 &= \hat{i}_1(v_1) \\ i_2 &= \hat{i}_2(v_2) \end{aligned} \tag{1.83}$$

Notice that these are the laws of elements. Next, applying KVL gives:

$$v = v_1 = v_2 \tag{1.84}$$

Applying KCL at node 1 gives:

$$i = i_1 + i_2 \tag{1.85}$$

Combining Eqs. (1.83), (1.84), (1.85), we obtain:

$$\begin{aligned} i &= \hat{i}(v) \\ \text{where } \hat{i}(v) &\stackrel{\triangle}{=} \hat{i}_1(v) + \hat{i}_2(v) \end{aligned} \tag{1.86}$$

Note that Eq. (1.86) can be extended to n nonlinear resistors $\mathscr{R}_n$ in parallel. Thus, we can conclude that:

1. KVL forces all branch voltages to be equal.
2. KCL requires the port current i to be equal to the sum of the branch currents of the resistors.
3. If each resistor is voltage-controlled, the resulting DP characteristic of the one-port is also a voltage-controlled resistor.

The careful reader would have noticed that Eqs. (1.76) to (1.78) and Eqs. (1.83) to (1.85) are duals of each other! In other words, if we make the substitutions for all the v's with i's and for all the i's with v's in one set of equations, we obtain precisely the other set. For this reason, we can extend and generalize the concept of duality introduced earlier for resistors to circuits.

In table 1.1, we list two sets of terms S and S^* which we have encountered and which are said to be dual to one another.

Before we end this section, we would like to solve an example that illustrates a variety of concepts from this chapter.

Example 1.10.2 In Fig. 1.40, determine the value of I.
Solution: Before attempting to solve any problem, it is a good idea to **understand** the problem and **devise a plan of action**. We then **carry out the plan** and **check our answer** [20].

Table 1.1: Dual terms

S	S^*
Branch Voltage	Branch Current
Resistance	Conductance
Current-controlled resistor	Voltage-controlled resistor
Open circuit	Short circuit
Independent voltage source	Independent current source
Inductor	Capacitor
KVL	KCL
Port voltage	Port current
Series connection	Parallel connection

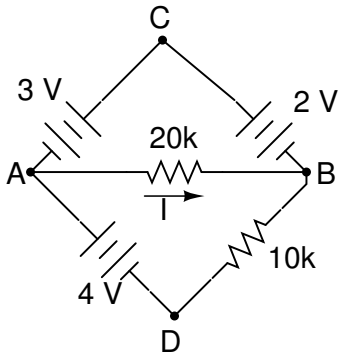


Fig. 1.40: Circuit with only linear elements

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In this case, a quick examination of the problem will indicate that we need to determine the current through a linear resistor and hence if we know the voltage across it, we can apply Ohm's law.

Starting at node B and applying KVL, we get:

$$v_{AB} + 3 - 2 = 0 \tag{1.87}$$

Notice our judicious choice of voltage polarity as v_{AB} and not v_{BA}. This choice is no accident: in this problem, the current direction has been clearly specified, so we must choose v_{AB} to comply with the passive sign convention definition from definition 1.2.

We can in fact now carry out the plan and get the result as:

$$\begin{aligned} I &= \frac{v_{AB}}{20\,k} \\ &= -0.05\,mA. \end{aligned} \tag{1.88}$$

Notice a negative I implies the voltage drop across the resistor is opposite to the direction we picked.

How do we check our answer? One approach would be to make sure that the power delivered is equal to power absorbed. This is essential because our circuit is a closed system. We need to first find the current through the branch $B-D-A$. This can be done by finding the voltage across the $10\ k$ resistor which in turn can be found by using KVL around $D-A-C-B-D$:

$$4+3-2-v_{BD}=0 \tag{1.89}$$

Thus $v_{BD}=5\ V$. Hence the current through the $10\ k$ is $I_{BD}=0.05\ mA$. KCL at node B gives $I_{CB}=0.1\ mA$. We now have all the necessary variables to find the power associated with each element, keeping in mind the passive sign convention form definition 1.2.

$$\begin{aligned} P_{3\,V} &= -0.3\ mW \\ P_{2\,V} &= +0.2\ mW \\ P_{4\,V} &= -0.2\ mW \\ P_{10\,k} &= +0.25\ mW \\ P_{20\,k} &= +0.05\ mW \\ \Sigma &= 0\ mW \end{aligned} \tag{1.90}$$

Hence we should have good confidence that our answer is correct. We will discuss more circuit analysis techniques based on energy (including expressions for energy stored in an inductor etc.) and power in section 4.6.

1.11 Conclusion

In this chapter, we discussed the fundamental circuit variables, elements and Kirchhoff's laws. To summarize:

1. We will assume the lumped circuit approximation.
2. We will follow a black box approach and model static (or "low frequency") characteristics. We will use parasitic components as necessary to model "high frequency" effects. We emphasize that "low frequency" and "high frequency" depend on the particular device being modeled.
3. The laws of interconnection (KVL, KCL) are independent of the laws of elements.
4. Elements are said to be in series when they have the same current flowing through them.

5. Elements are said to be in parallel when they have the same voltage across them.

In the next chapter, we will move on to study multi-terminal elements, particularly the transistor, operational amplifier and transformer.

Exercises

1.1. Given the $v-i$ characteristic Γ of a resistor $\mathscr{R}$ on the $v-i$ plane, show that the dual characteristic is obtained by reflecting Γ about the 45° line through the origin.

1.2. Find a necessary and sufficient condition for a nonlinear two-terminal element (resistor, inductor, capacitor and memristor) to be bilateral.

1.3. A certain $v-i$ curve is described by an equation $v = 10i+5$. Is this a linear resistor?

1.4. Discuss mechanical analogies to the four fundamental circuit elements. For the memristor, a good starting point is the classic paper by Oster and Auslander [15].

1.5. This exercise (courtesy of Dr. Oldham from UC Berkeley [14]) is designed to test the reader's fundamental understanding of the conceptual material from this chapter, and is very similar to example 1.10.2. As a result, the reader should strive to find the correct solution mentally, without the use of pen and paper.

Find the values of the indicated variables below.

1. V_{AB} in Fig. 1.41.

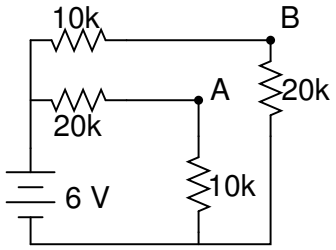

Fig. 1.41

2. V_{CD} in Fig. 1.42.
3. Power associated with the 500 $k\Omega$ resistor in Fig. 1.43.
4. Equivalent resistance at AB in Fig. 1.44.

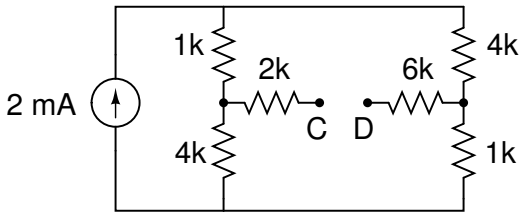

Fig. 1.42

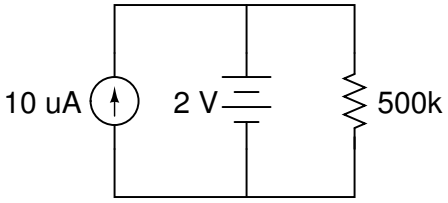

Fig. 1.43

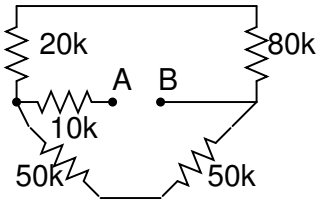

Fig. 1.44

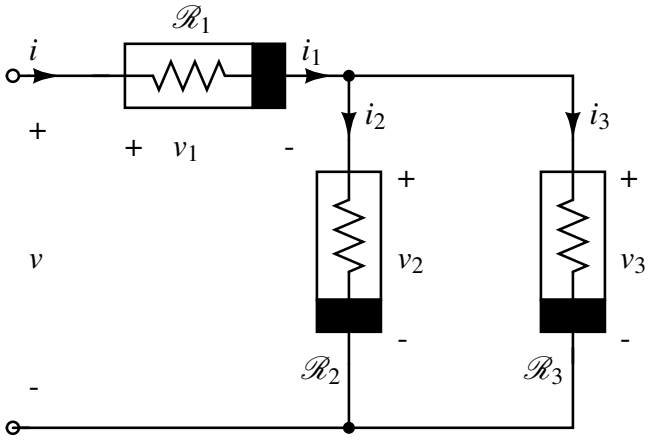

Fig. 1.45: A ladder circuit with nonlinear resistors.

1.6. Consider the circuit in Fig. 1.45. Assuming $\mathscr{R}_1$ is current-controlled ($v_1 = \hat{v}_1(i_1)$), $\mathscr{R}_2$ and $\mathscr{R}_3$ are voltage-controlled ($i_2 = \hat{i}_2(v_2), i_3 = \hat{i}_3(v_3)$), determine the characteristic for $\mathscr{R}$.

1.7. Based on the ideas from section 1.10, discuss:

1. $\mathscr{L}_n$ inductors in series and parallel
2. $\mathscr{C}_n$ capacitors in series and parallel
3. $\mathscr{M}_n$ memristors in series and parallel

1.8. The current in the circuit in Fig. 1.46 [13] is known to be $i_0 = 5e^{-2000t}(2\cos 4000t + \sin 4000t)\ mA$ to $t \geq 0^+$. Find the values of $v_1(0^+)$ and $v_2(0^+)$.

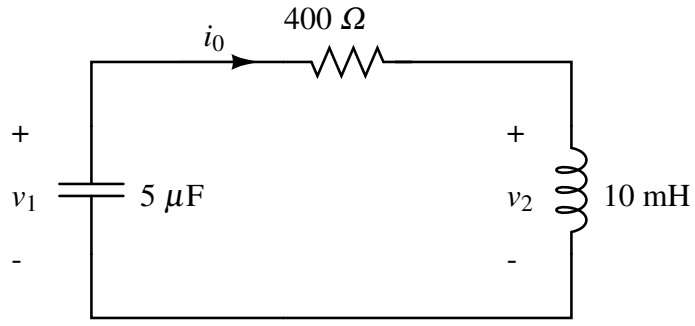

Fig. 1.46

1.9. At $t = 0$, a series-connected capacitor and inductor are placed across the terminals of a black box, as shown in Fig. 1.47 [13]. For $t > 0$, it is known that:

$$i_0 = 1.5e^{-16000t} - 0.5e^{-4000t}\ A \tag{1.91}$$

If $v_1(0) = -50\ V$, find and sketch v_0 for $t \geq 0$.

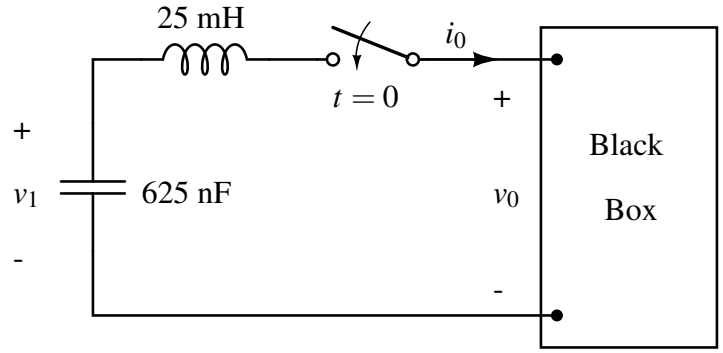

Fig. 1.47

Lab 1: Introduction to QUCS (Quite Universal Circuit Simulator)

Objective: To successfully install QUCS
Theory:
The goal of circuit simulation is to predict the behavior of a circuit before we physically construct the circuit.

A variety of circuit simulators exist. In keeping with the introductory nature of this text, we would like to use a circuit simulator that is easy to use, has a robust graphical user interface (GUI) and is supported across multiple platforms (Windows, OS X and Linux based computers). Moreover, as stated in the online QUCS FAQ [21], classic SPICE based simulators have a variety of limitations that QUCS aims to overcome.

In this lab component, we simply install QUCS and make sure that the program is functional.

Lab Exercise:

1. Download and install the correct version of QUCS from [21] for your platform. Detailed instructions are in Appendix A.
2. Start QUCS. If successful, you should see Fig. 1.48.

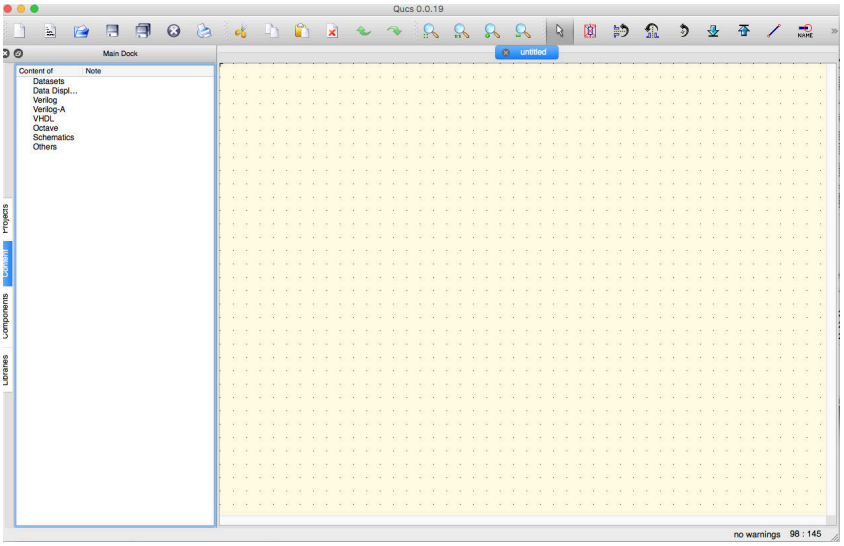

Fig. 1.48: QUCS startup screen in OS X Sierra.

3. Once you start QUCS, we encourage you to read the associated documentation [21] and try some of the sample simulations. More will be explained about the different simulation (transient etc.) throughout the book.

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Appendix A
Installing QUCS

In this appendix, we will discuss how to install QUCS [1]. Note that QUCS has a lot of components, many of which we will not use. Nevertheless, we will install all components for completeness.

A.1 Windows

Please install the official Windows QUCS package from the download section in the QUCS homepage [1].

A.2 OS X

Please install the official OS X QUCS package from the download section in the QUCS homepage [1].

A.3 Linux

If you are using Linux, make sure you have a reliable internet connection, as we will be installing from source. If you are on a Linux platform, we will assume that you are comfortable with basic command line tools such as `tar, apt-get` etc. and have `sudo` access.

The instructions below are specifically for Ubuntu 14.04 distribution, but they should be applicable to any of the popular Linux distributions.

1. The first step is to download the latest QUCS tarball (v0.0.19 as of this writing) from [1] in your home folder.

2. Extract and unzip the tarball:

```
$ tar xvzf qucs-0.0.19.tar.gz
```

3. Change into the QUCS directory and go through `README.md`.
4. You may need to install missing dependencies via the Debian package manager. In our case, we had to install the following packages:

```
$ sudo apt-get install gperf libxml-libxml-perl libxml2
    libxml2-dev libgd-perl octave texlive-collection-mathextra
     texlive-math-extra texlive-science
```

5. Next, we need to install `ADMS`. To do, clone the repository from github into your root folder, configure and install:

```
$ git clone https://github.com/Qucs/ADMS.git
$ export LD_LIBRARY_PATH=/usr/local/lib
$ cd ADMS
$ sh bootstrap.sh
$ ./configure --enable-maintainer-mode
$ make
$ sudo make install
$ sudo ldconfig
```

6. Configure, make and install QUCS:

```
$ cd ~/qucs-0.0.19/
$ ./configure
$ make
$ sudo make install
```

References

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Solutions

For step-by-step solutions to all problems, please visit online material at: http://www.youtube.com/user/bharathberkeley/IntroToNonlinearCircuitsAndNetworks

http://www.springer.com/978-3-319-67324-0

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