H.U. ELE 764 Lecture Notes

Hacettepe University
Electrical and Electronics Engineering Department

ELE 764
Special Topics in Electrical and Electronics Engineering

Lecture Notes

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SWITCH MODE POWER SUPPLIES (SMPS)

I. INTRODUCTION

1.1 Linear vs Switch Mode Power Supplies

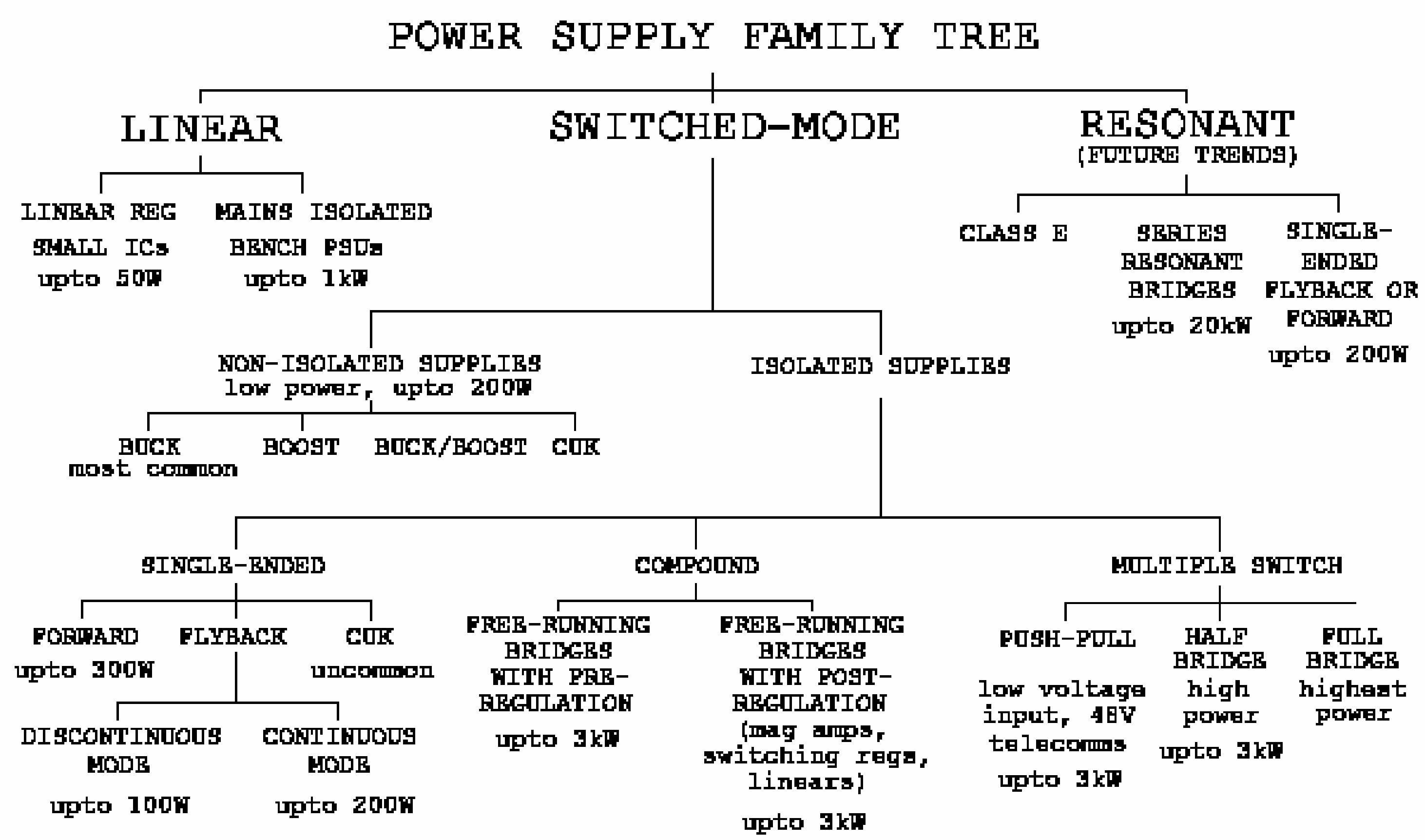
1.2. Overview of Switching Power Supplies

1.3. Functional Circuit Blocks of an Off-Line Switcher

1.4. Basic Switch Mode DC-DC Converters

- ***1.4.1. Step-down (Buck) Converter,***
- ***1.4.2. Step-Up (Boost) Converter,***
- ***1.4.3. Step-down/Step-up (Buck-Boost) Converter***

SWITCH MODE POWER SUPPLIES (SMPS)



SWITCH MODE POWER SUPPLIES (SMPS)

I. INTRODUCTION

1.1 Linear vs Switch Mode Power Supplies

- *For many years, the world of power supply design moved away from the use of linear power supplies to the more practical SMPS. The linear power supply contains a mains transformer and a dissipative series regulator. This means the supply has extremely large and heavy power frequency (50/60 Hz) transformers, and also very poor conversion efficiencies as serious drawbacks.*

- *Typical efficiencies of 35-65% are standard for a linear supply. This compares with efficiencies up to 95% currently available using SMPS design.*

I. INTRODUCTION

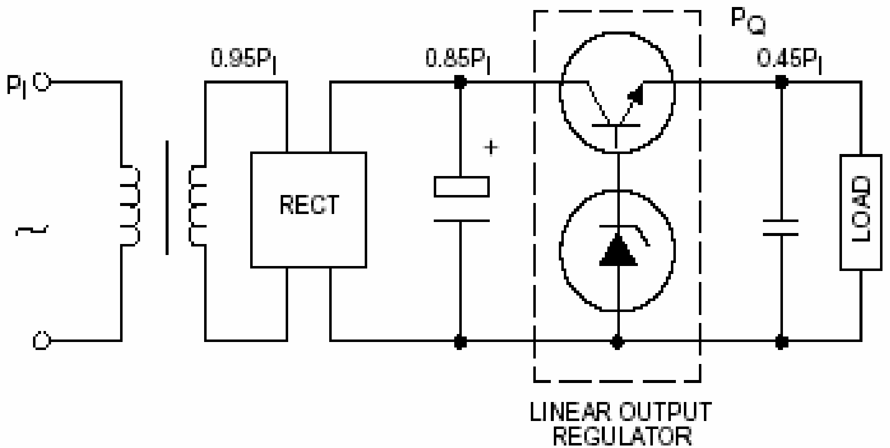
- ***Furthermore, by employing high switching frequencies, the size of the power transformer, and associated filtering components in the SMPS are drastically reduced as compared to linear.***

- ***For example, an SMPS operating at 20 kHz produces a 4 times reduction in component size, and this increases to about 8 times at 100 kHz. This means that an SMPS design can produce very compact and lightweight power supplies.***

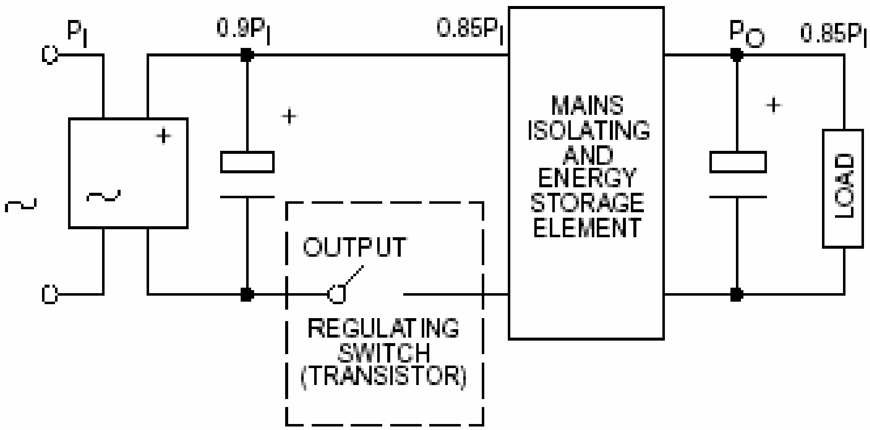
- ***Size reduction is now an essential requirement for the majority of electronic systems. The supply must slot into an ever shrinking space left for it by electronic system designers*** *(up to 40 – 50 W/in^3).*

I. INTRODUCTION

1.1 Linear vs Switch Mode Power Supplies



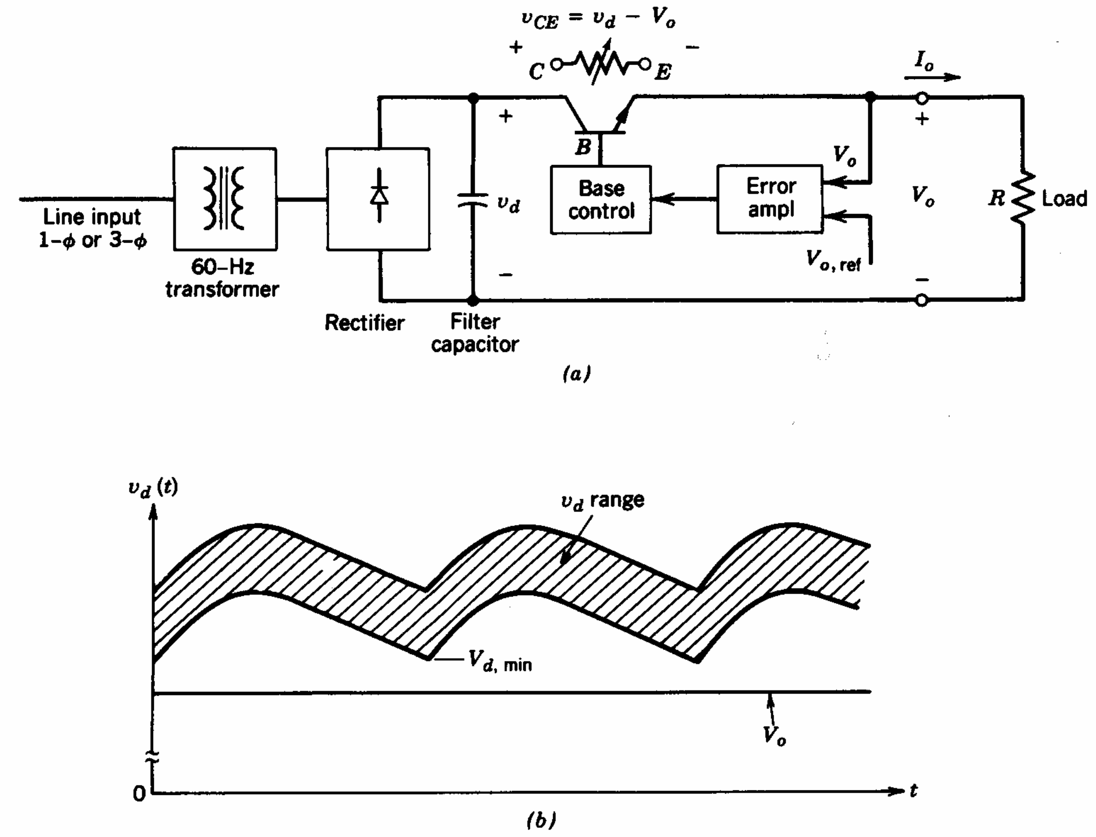
a. Conventional Supply — 45% Efficiency



Switched-Mode Supply — 80% Efficiency

I. INTRODUCTION

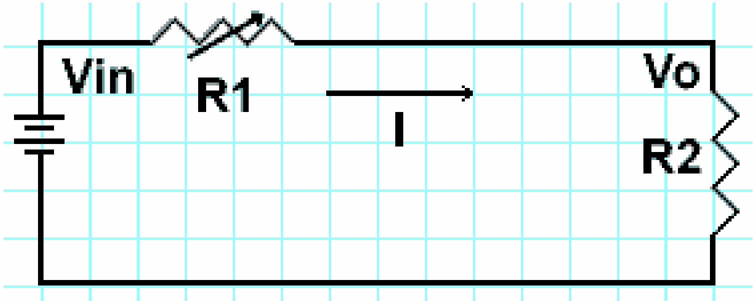
Linear power supply



- Very poor efficiency and large weight and size

I. INTRODUCTION

Series regulator :



ıtor

Given:

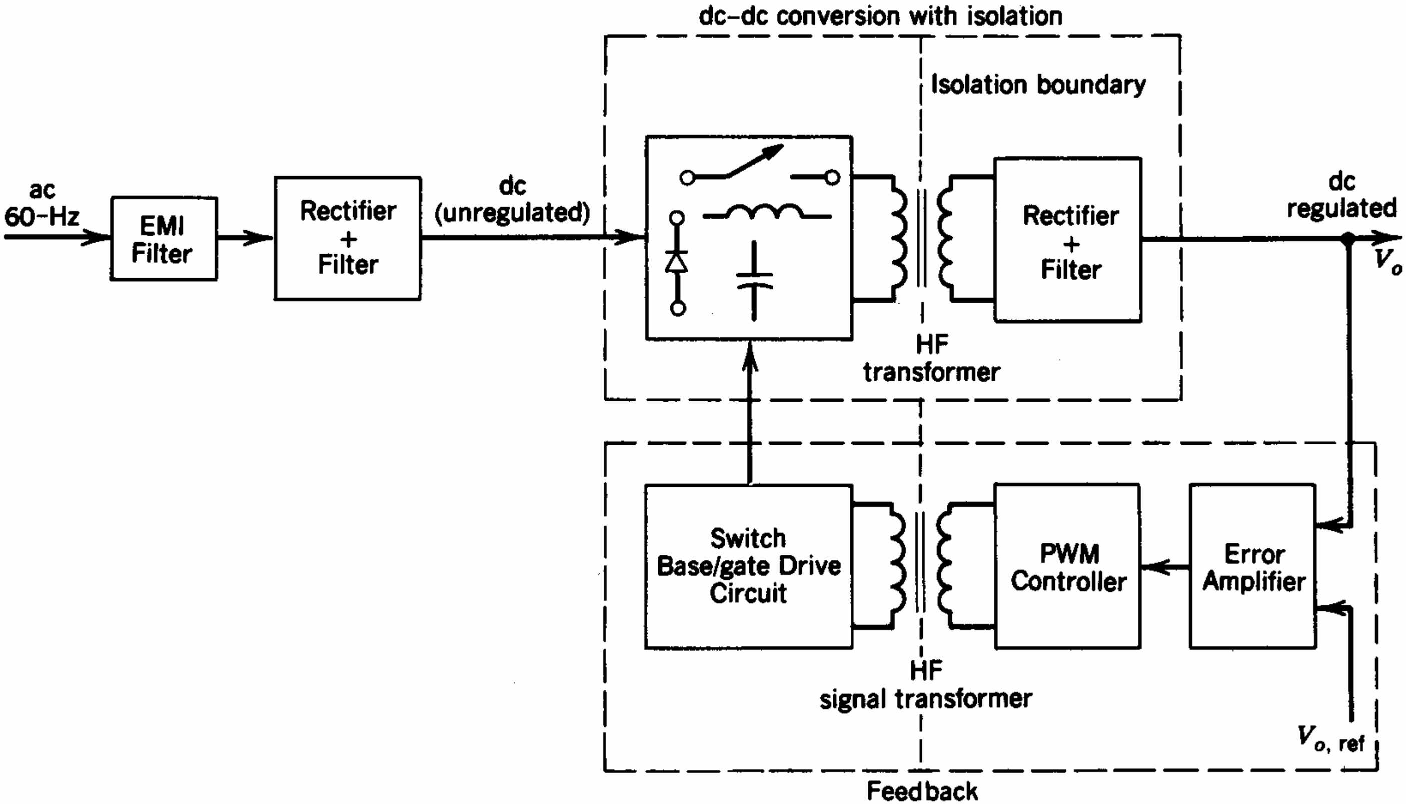
- Vin = 12 Vdc
- R2 = 0.25 ohm
- Vo = 5 Vdc

Solving and listing the parameters of interest:

- I = 20 A
- R1 = 0.35 ohms
- Pin = 240 W
- Pout (R2) = 100 W
- Power R1 = 140 W
- Efficiency = Pout/Pin = 0.417 => 42%

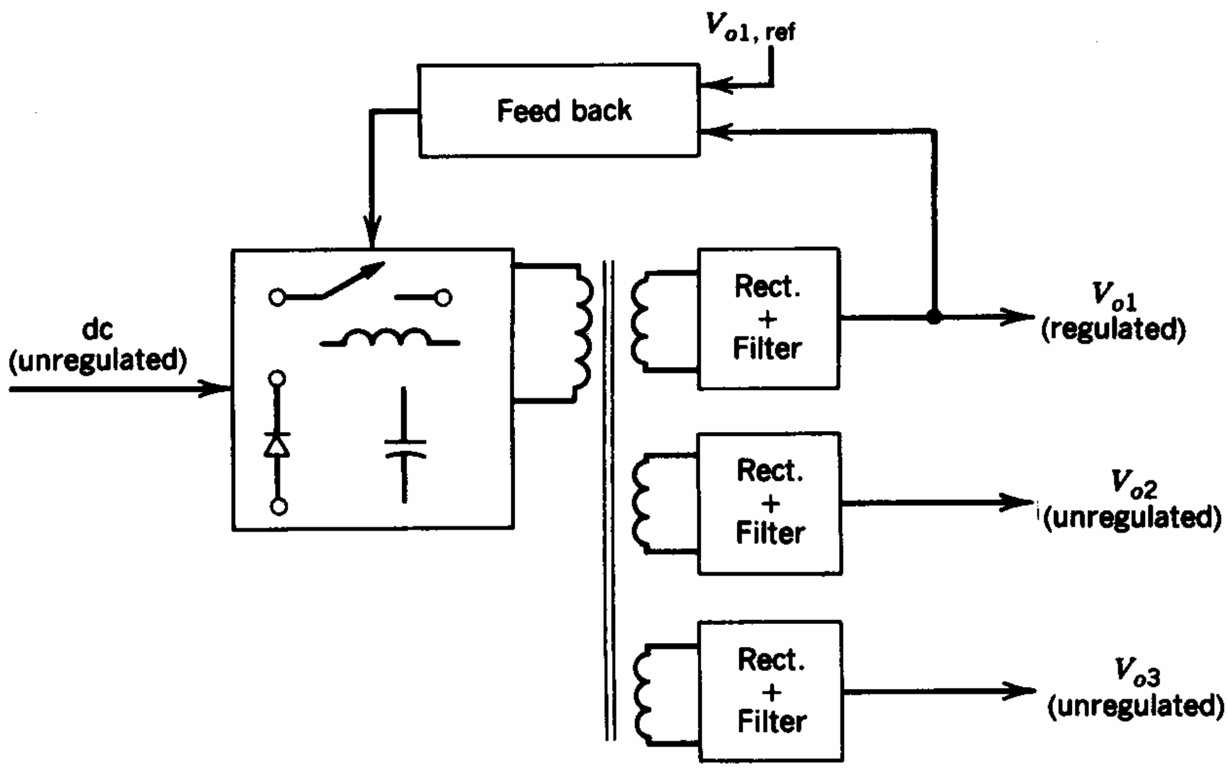
I. INTRODUCTION

Switch-mode power supply



I. INTRODUCTION

Switch-mode power supply with multiple outputs



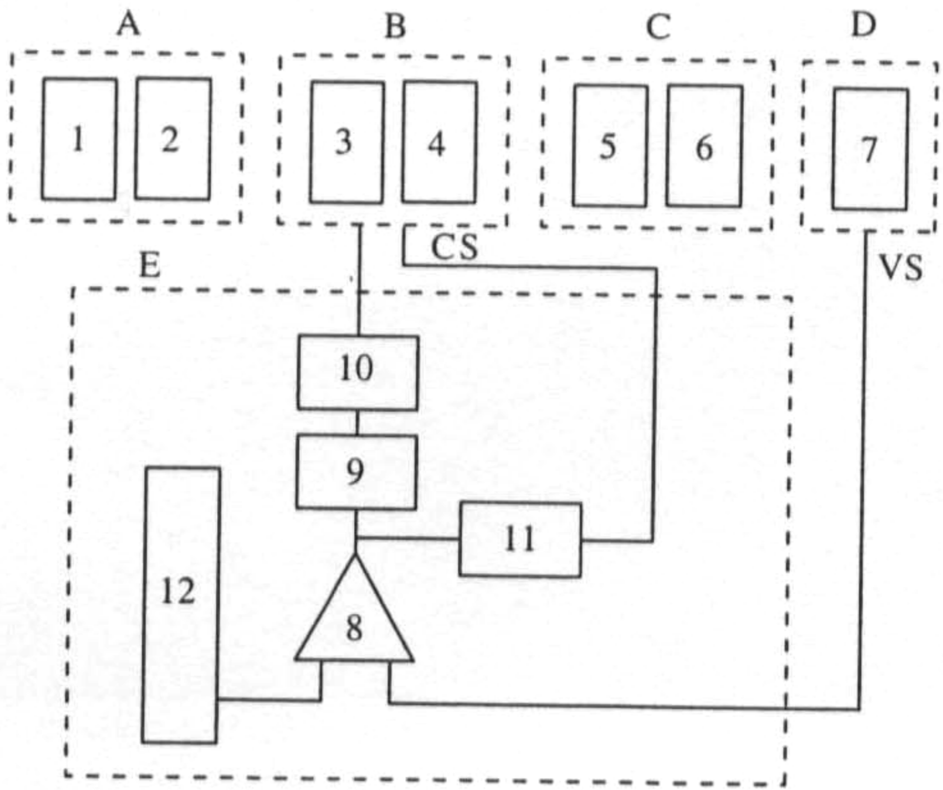
I. INTRODUCTION

- ***At the heart of the converter is the high frequency inverter sectio where the input supply is chopped at very high frequencies, then filtered and smoothed to produce dc outputs.***
- ***The circuit configuration which determines how the power is transferred is called the TOPOLOGY of the SMPS. The topology consists of an arrangement of transformer, inductors, capacitors, and power semiconductors (MOSFET or IGBT power transistors and power rectifiers).***
- ***Presently, there is a wide choice of topologies available, each having its own advantages, and disadvantages, making it suitable for a specific power supply application. Basic operation principles, advantages, drawbacks, and application areas will be discussed in the following sections.***

I. INTRODUCTION

1.2. Overview of SMPS

1.2.1. Functional circuit blocks of an off-line SMPS



I. INTRODUCTION

Functional circuit blocks of an off-line SMPS

Circuit Block A: The Front End Rectifier and Filter

The purpose of this block is to provide a raw dc voltage from the input ac. It consists of the rectifier (1) and the filter (2). The rectifier is usually the diode bridge rectifier. The block 2 is a filter used to bring down the ripple content in the rectified voltage to an acceptable level. It is usually a bank of electrolytic capacitors. The bank of capacitors will also retain the voltage for a short time in the event of momentary interruption in the AC input. The capacitor value can be chosen suitably to make the output of SMPS insensitive to power supply interruptions.

I. INTRODUCTION

Functional circuit blocks of an off-line SMPS

Circuit Block B: The switching converter

This block converts the unregulated DC into high frequency PWM AC of the required voltage level, by repetetive switching. Switching frequencies may be as high as hundred kHz or more. The switching is achieved by block 3, which is a configuration of power semiconductor switches. The most popular switching device for SMPS is at the present time the power MOSFET because of the very high switching frequency. IGBT is an alternative device, which has higher power handling capability, but at lower f's than the MOSFET.

I. INTRODUCTION

Functional circuit blocks of an off-line SMPS

Circuit Block 4 is the high frequency transformer. It serves to provide the required voltage level on the output side. It also serves to provide electrical isolation of the regulated output from the input ac supply. The core material of the transformer is a high frequency material such as ferrite, iron powder, amorphous metal etc…

There are several switching circuit topologies suitable for the switching converter block of an SMPS, as will be overviewed later.

I. INTRODUCTION

Functional circuit blocks of an off-line SMPS

Circuit Block C: Output Rectifier and Filter

The input of this circuit block is the HF PWM AC from the secondary side of the ferrite power transformer (4). Circuit block 5 is the rectifier that converts this AC to DC. The frequency capability of the rectifying diodes is to be very high. Block 6 is the output filter. This usually consists of a high frequency ferrite core inductor and a bank of electrolytic capacitors.

Circuit Block D: Voltage and current sensing

I. INTRODUCTION

Functional circuit blocks of an off-line SMPS

Circuit Block D: Voltage and current sensing

Since the output voltage is to be automatically regulated, it is necessary for the controller to sense the output voltage. In this block, the voltage sensing circuit is shown labelled 7. For practical operation of the SMPS, it is also necessary to sense the current, first to provide a current limiting feature, that will automatically limit the max. output current in the case of an overload or short circuit at the output. In many designs, the current limiting is implemented by 'pulse by pulse current limiting technique. This means that the max. current is limited in every switching cycle.

I. INTRODUCTION

Functional circuit blocks of an off-line SMPS

Second, for sensing the current when the type of closed loop control used for the SMPS is the 'current mode control'. This calls for sensing the instantaneous current in every switching cycle.

For these reasons, it is common practice to sense the inst. current in the switching converter itself, in block B, rather than sensing the output current. A convenient way is to use a low resistance shunt in series on the primary side of the transformer, and sense the voltage drop across it. For high powers, LEM Hall-effect type current sensors are also used.

I. INTRODUCTION

Functional circuit blocks of an off-line SMPS

Circuit Block E: The closed loop controller

The primary function of the controller is to sense the output voltage, and compare it with an accurate reference, amplify any error between the two, and implement PWM of the switching elements to negate the error. Controllers for SMPS are available commercially as IC (from TI, Motorola, SGS…) Two basic functions of such an IC are the output voltage regulation, and pulse by pulse current limiting. The IC's also provide additional features such as overvoltage, undervoltage lock out, soft start etc...

I. INTRODUCTION

Functional circuit blocks of an off-line SMPS

Circuit Block E: The closed loop controller

The circuit module 8 is an OPAMP that compares the sensed output voltage against the internal reference voltage, and amplifies any error. The output of this error amplifier adjusts the timing pulses generated in the timing circuit 9, thus determining the switching instants of the power switches.
In this manner, the error amplifier implements automatic regulation of output voltage by PWM.
The timing pulses output from 9 ususally cannot drive directly the power switches, the driver block 10 provides the required drive power (some ICs include drivers).

I. INTRODUCTION

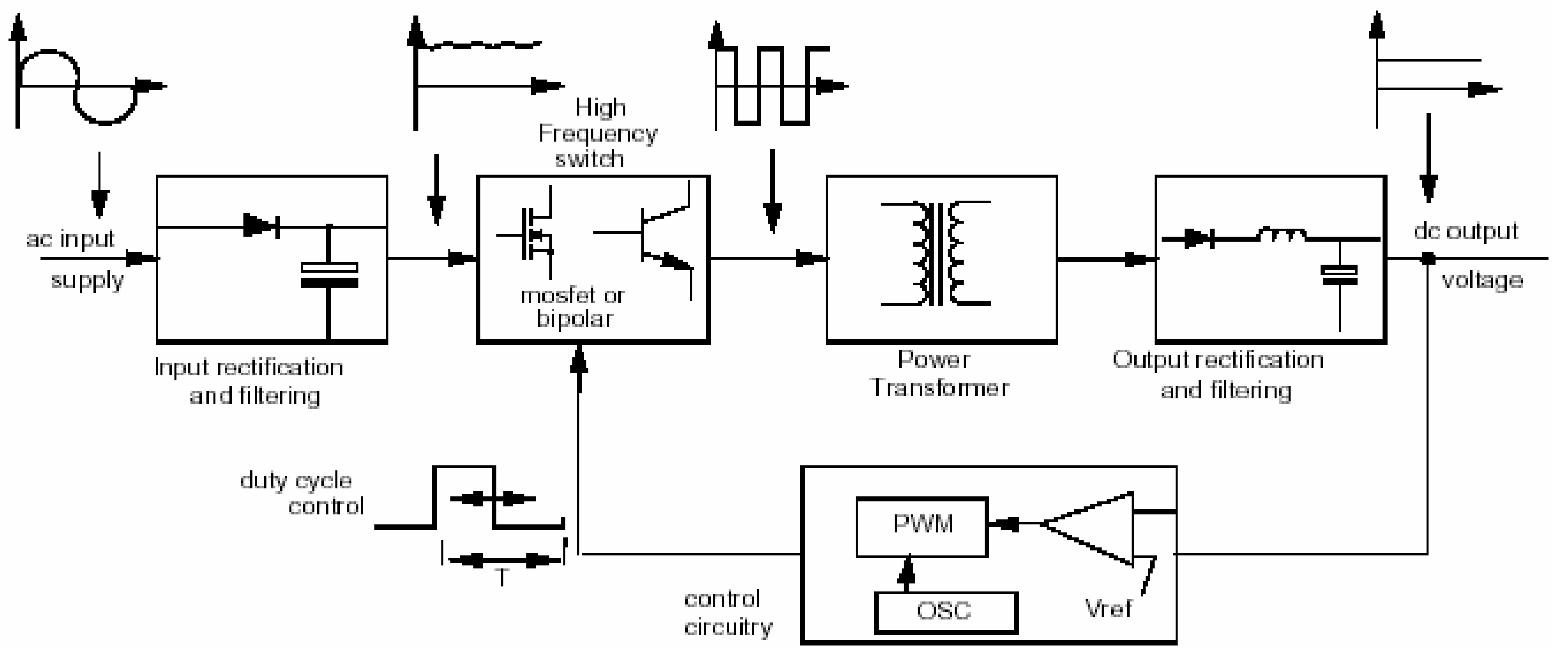
Functional circuit blocks of an off-line SMPS

The circuit module 11 implements pulse-by-pulse current limiting. The required current limit value has to be set externally, as one of the inputs to block 11, which compares the set value with the sensed inst. value.

As long as sensed value is below the set value, block 11 is inactive. But if sensed value is greater than or equal to the set limit value, the output from 11 will override the output of the voltage error amplifier, and initiates the switching of power semiconductor(s) in such a way that no further increase of current is possible in that switching cycle.

I. INTRODUCTION

1.3. Block Diagram of a Basic SMPS



I. INTRODUCTION

- ***Usually, in an off-line SMPS, the ac supply (50/60 Hz mains) is first rectified, and then filtered by the input reservoir capacitor to produce a rough dc input supply. This level can fluctuate widely due to variations in the mains.***

- ***In addition, the capacitance on the input has to be fairly large to hold up the supply in the case of a severe drop in the mains.***

- ***The unregulated dc is fed directly to the central block of the supply, the high frequency power switching section.***

- ***The SMPS can also be configured to operate from any suitable dc input, in this case the supply is called a dc to dc converter.***

I. INTRODUCTION

- ***Fast switching power semiconductors such as MOSFETs and IGBTs are driven on and off, and switch the input voltage across the primary of the power transformer.***

- ***The drive pulses are usually of a fixed frequency, and variable duty cycle. Hence a voltage pulse train of suitable magnitude and duty ratio appears on the transformer secondaries.***

- ***This voltage pulse train is then appropriately rectified, and then smoothed by the output filter, either a capacitor or an LC filter arrangement, depending upon the topology used. This transfer of power has to be carried out with the lowest losses possible, to maintain high efficiency. Thus, optimum design of the passive and magnetic components, and selection of the correct power semiconductors is critical.***

I. INTRODUCTION

➢ *Regulation of the output to provide a stabilized dc supply is carried out by the control/feedback block.*

➢ *Generally, most SMPS operate on a fixed frequency PWM basis where duration of the ON time of the drive to the power switch is varied on a cycle by cycle basis. This compensates for the changes in the input supply and output load.*

➢ *The output voltage is compared to an accurate reference supply, and the error voltage produced by the comparator is used by dedicated control logic to terminate the drive pulse to the main power switch(es) at the correct instant. This will provide a very stable dc ouput supply.*

I. INTRODUCTION

- *It is essential that delays in the control loop are kept to a minimum, otherwise stability problems would occur. Hence, very high speed components must be selected for the loop.*

- *In most applications, the SMPS topology contains a power transformer. This provides isolation, voltage scaling through turns ratio, and the ability to provide multiple outputs.*

- *In the transformer-coupled supplies, in order to keep the isolation barrier intact, some type of electronic isolation is required in the feedback. This is usually achieved by using a small pulse transformer or an opto-isolator, hence adding to the component count.*

I. INTRODUCTION

- ***However, there are non-isolated topologies (without transformers) such as the buck, and the boost converters, where the processing power is achieved by inductive energy transfer alone.***

- ***A topology is the arrangement of the power devices and their magnetic elements. Each topology has unique properties which make it best suited for certain application.***

Some topologies are best used for AC/DC of line converters at low output power (200 W). Some are a better choice for high AC input voltages (> 220 V AC). Some have advantages for higher DC output voltages (> 200 V), or in applications where there are more than 4 or 5 different output voltages.

I. INTRODUCTION

1.4. Basic Switch-Mode DC-DC Converter Topologies

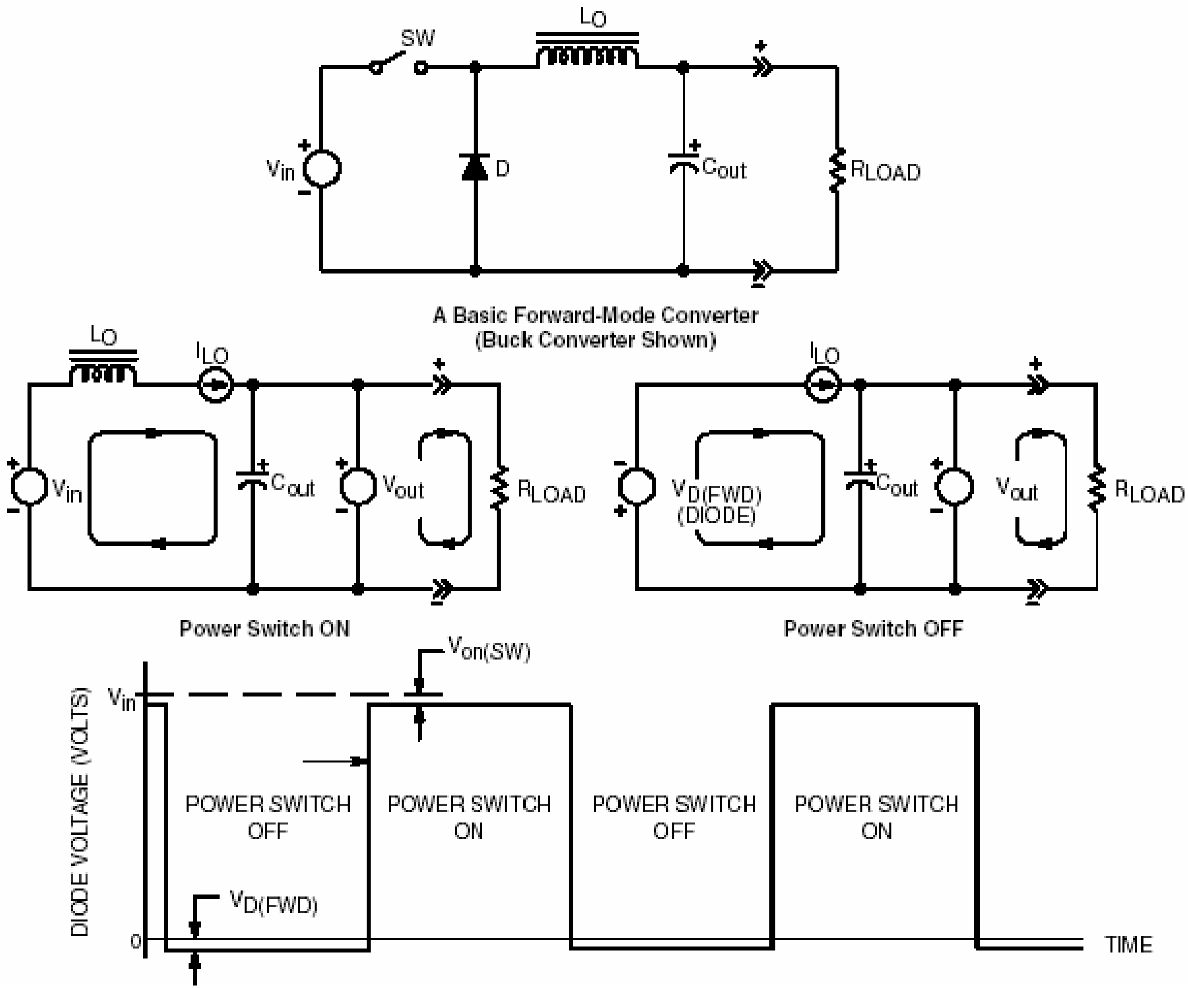
1.4.1 – 1.4.3. Non-Isolated Switching RegulatorTopologies:

According to the position of the switch and the rectifier, different types of voltage converters can be made:

- *Step down 'Buck' converter*
- *Step up 'Boost' converter*
- *Step up / Step down 'Buck-Boost' converter*

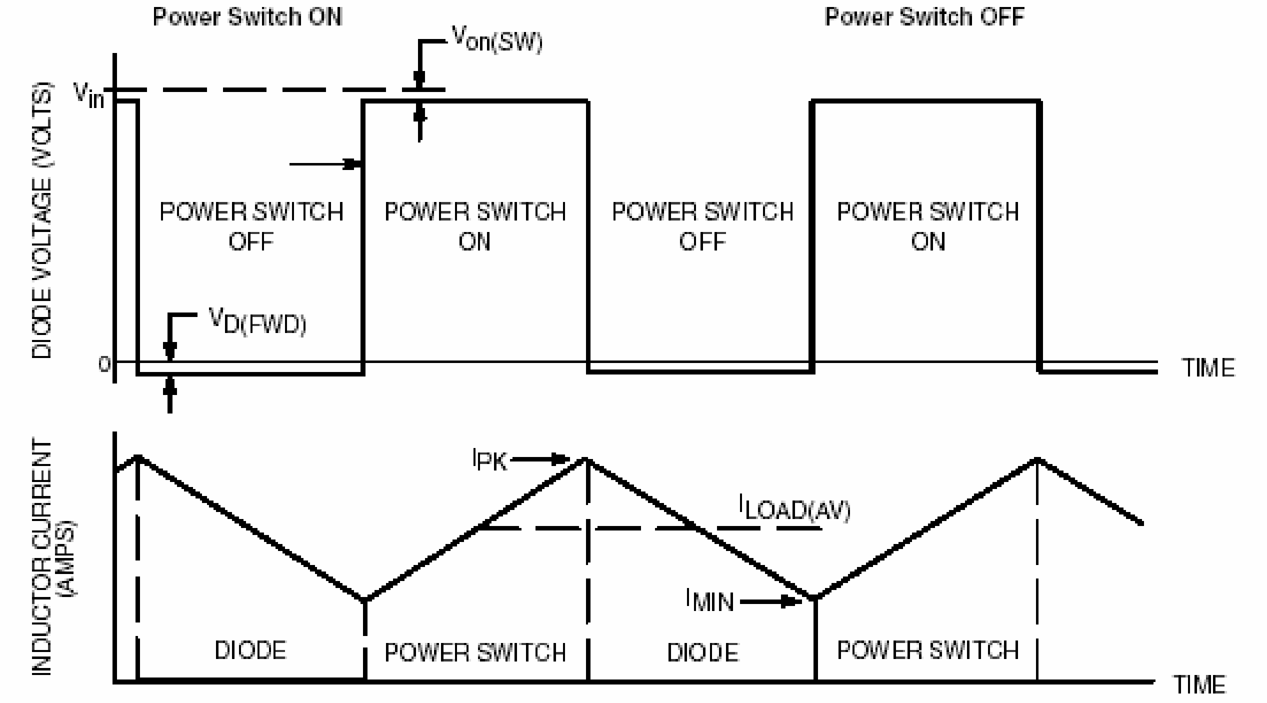
I. INTRODUCTION

1.4.1. BUCK CONVERTER



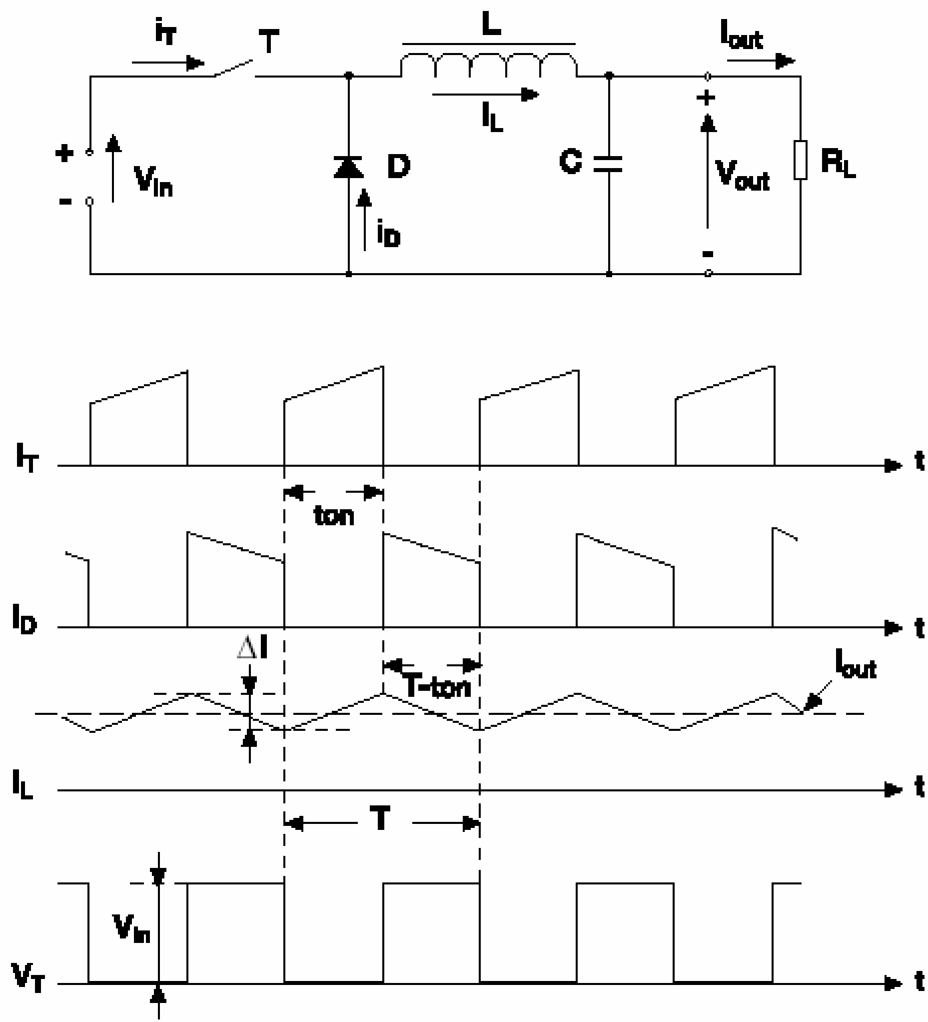
I. INTRODUCTION

Buck Converter Operation



I. INTRODUCTION

Buck Converter Waveforms:



I. INTRODUCTION

Buck Converter

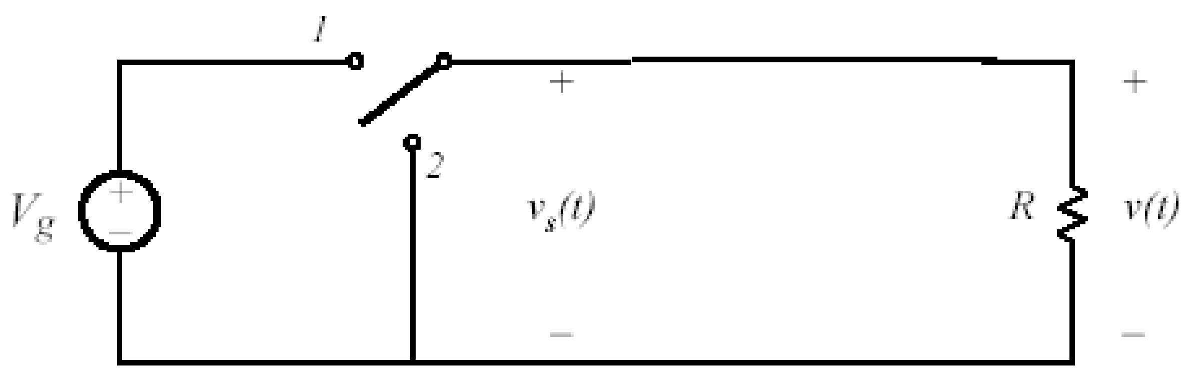
The power device is switched at a frequency $f = 1/T$ with a conduction duty cycle $D = t_{on} / T$. The output voltage can also be expressed as: $V_{out} = V_{in} D$.

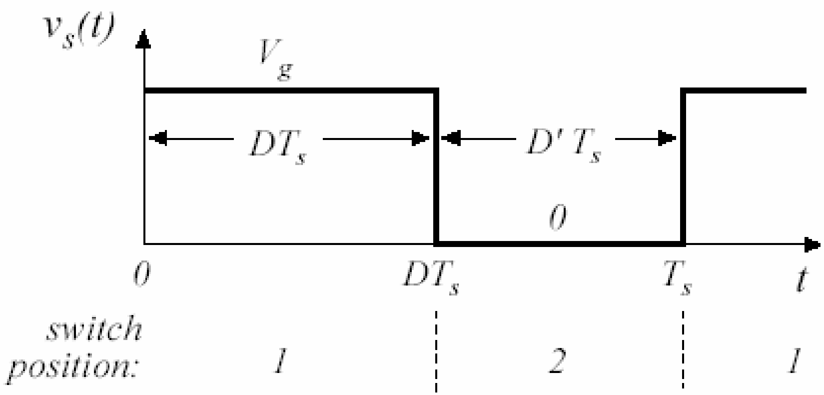
Device selection:

- ***Power Switch:*** V_{ce} or $V_{dss} > V_{in\,max}$
- ***Rectifier:*** $V_{RRM} \geq V_{inmax}$; $I_{fav} \geq I_{out}(1- D)$

I. INTRODUCTION

Step-down dc-dc converter operation



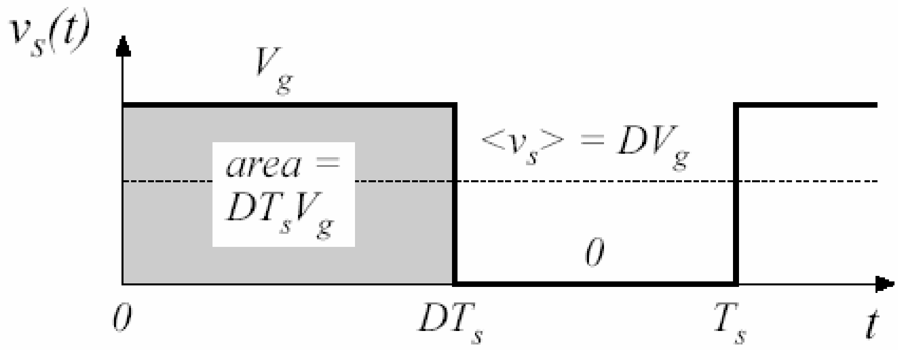


Switch output voltage waveform

Duty cycle *D*:
$0 \le D \le 1$

I. INTRODUCTION

The Buck Converter (DC component of output voltage)



Fourier analysis: Dc component = average value

DC component of $v_s(t)$ = average value:

$$V_s = \frac{1}{T_s}\int_0^{T_s} v_s(t)\,dt = DV_g$$

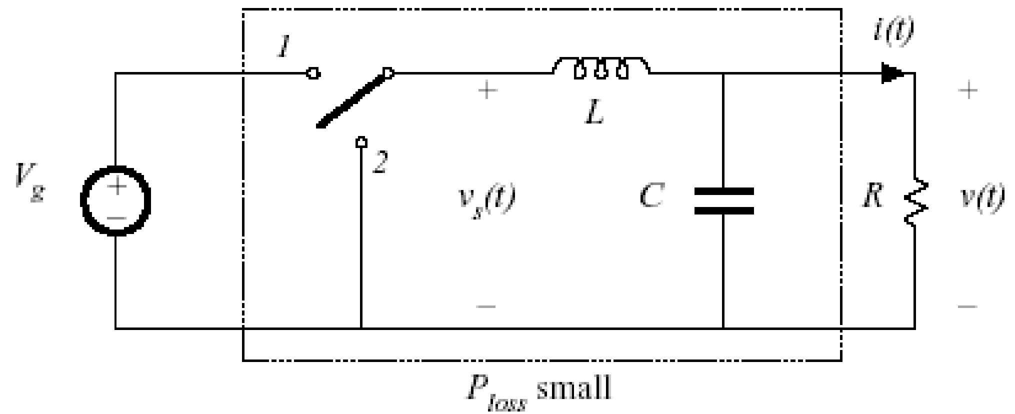
T_s = switching period

f_s = switching frequency
= $1 / T_s$

I. INTRODUCTION

Insertion of a low pass LC filter to remove switching frequency harmonics:

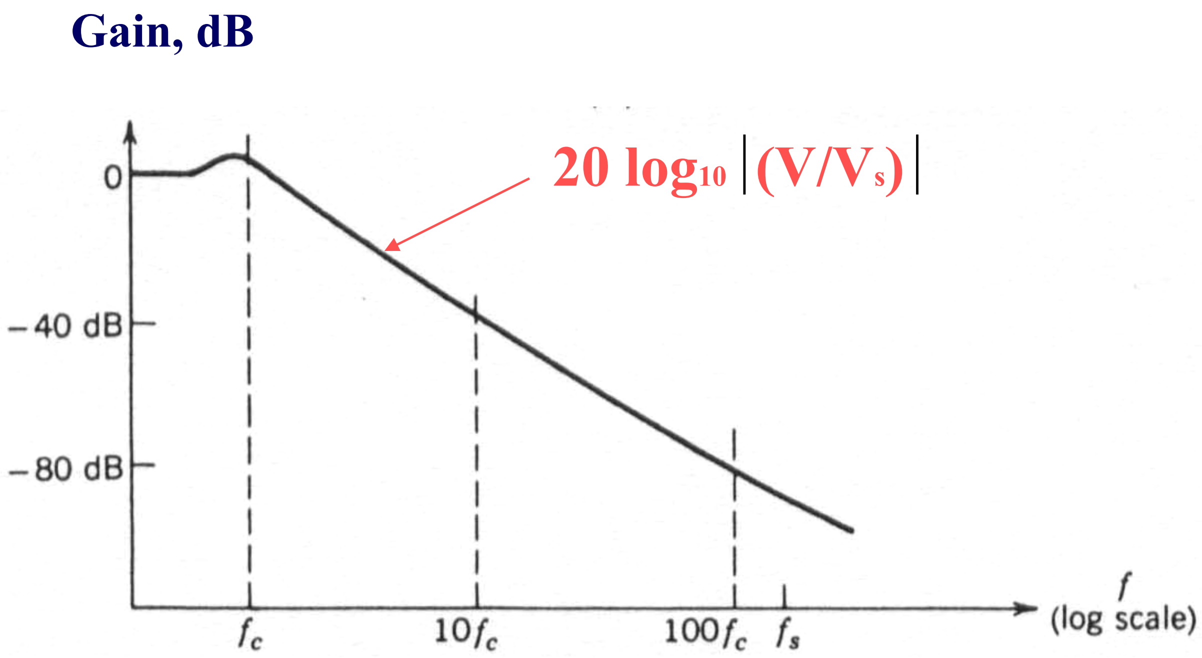
Addition of (ideally lossless) *L-C* low-pass filter, for removal of switching harmonics:



- Choose filter cutoff frequency f_0 much smaller than switching frequency f_s

I. INTRODUCTION

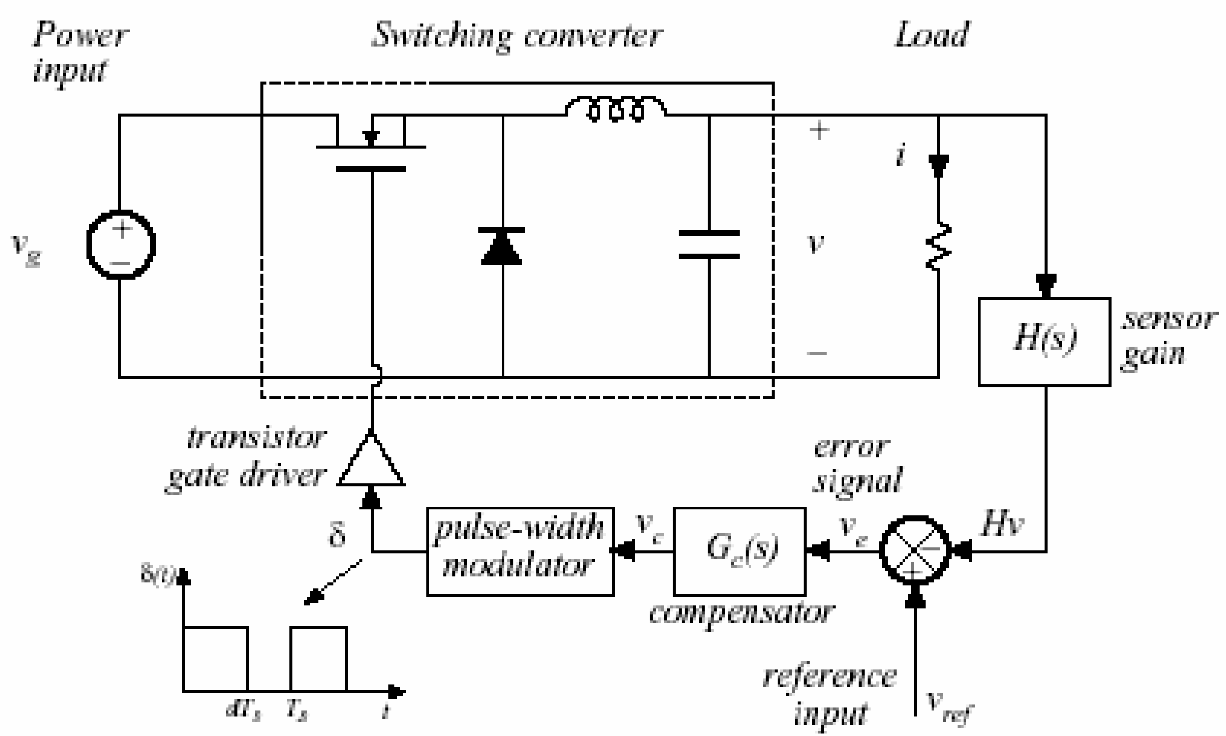
Low pass LC filter characteristics:



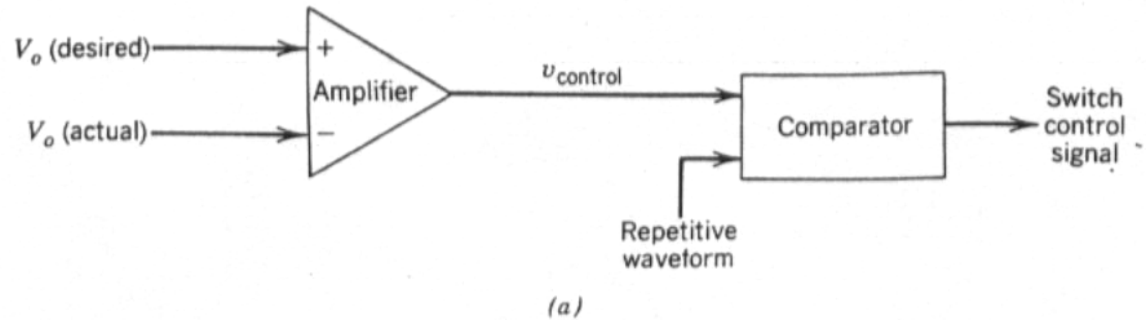
The cut-off frequency : $f_c = 1 / [2\pi\sqrt{(LC)}]$

I. INTRODUCTION

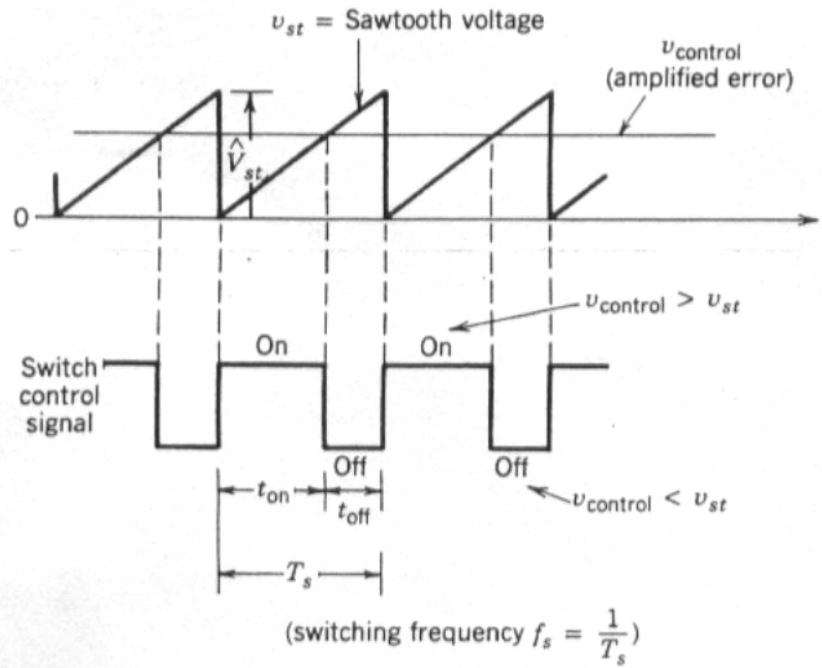
The Buck Converter (Power and control circuits)



I. INTRODUCTION

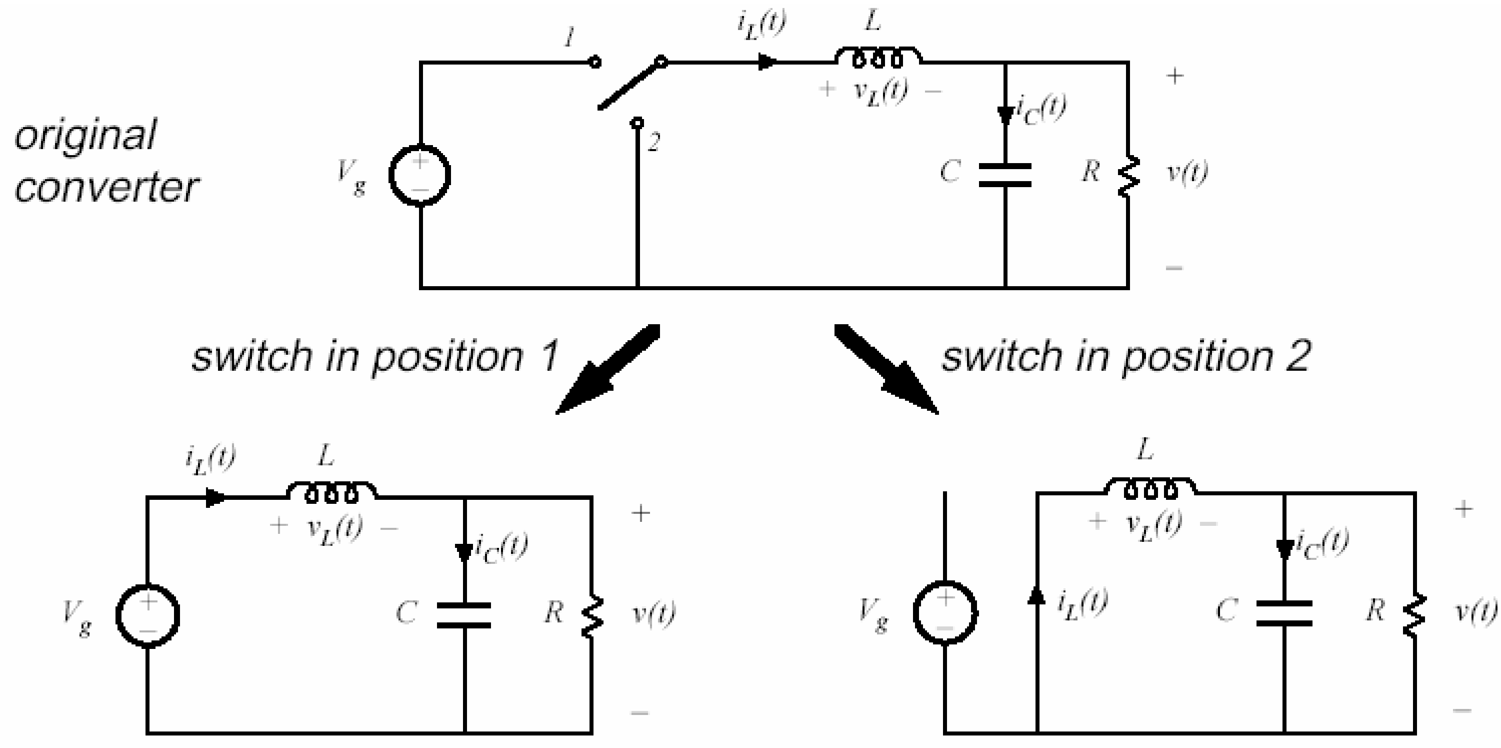


Pulse width modulator:



I. INTRODUCTION

Analysis of buck converter at steady-state: (continuous conduction)

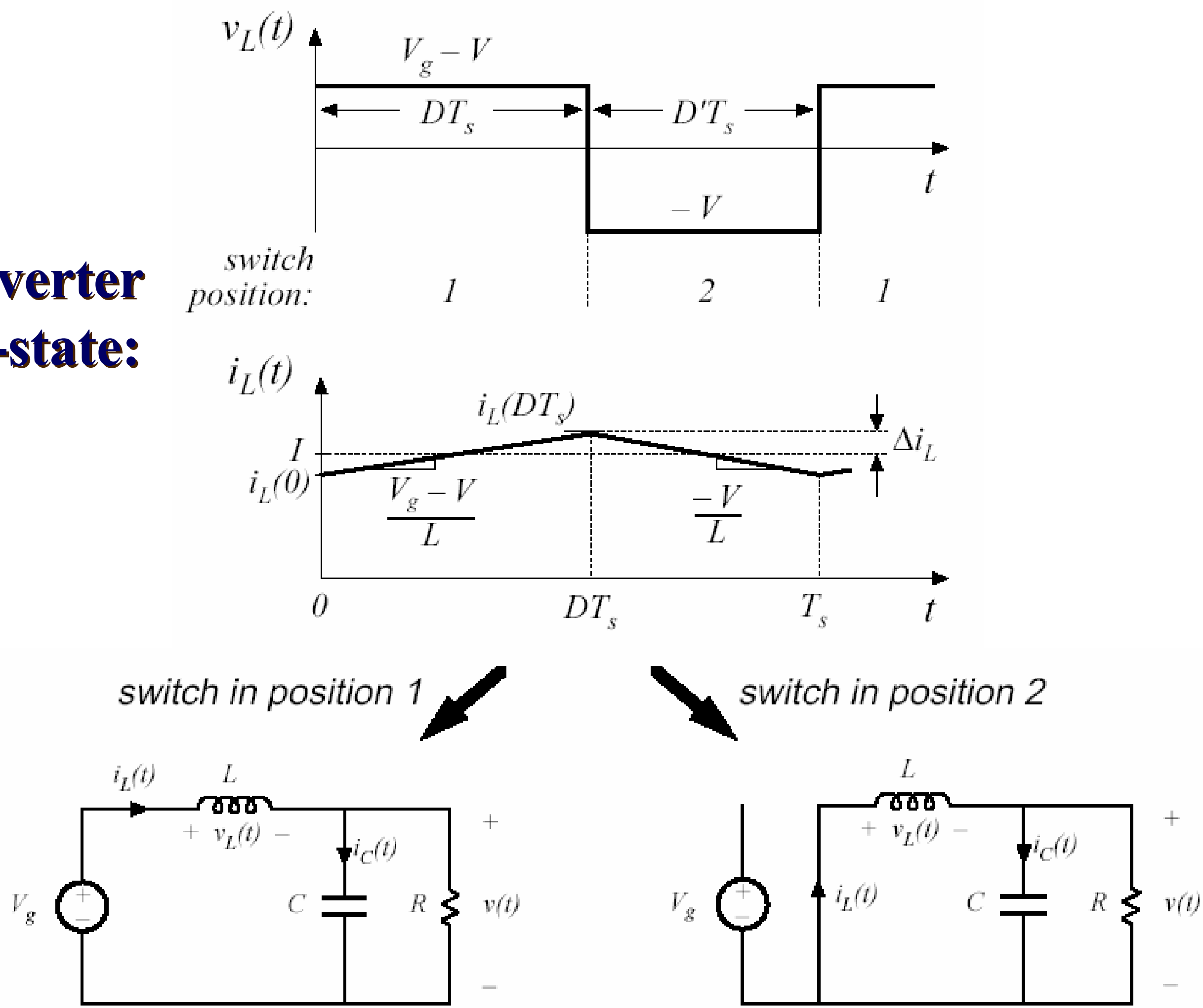


Q1 ON, D1 OFF

Q1 OFF, D1 ON

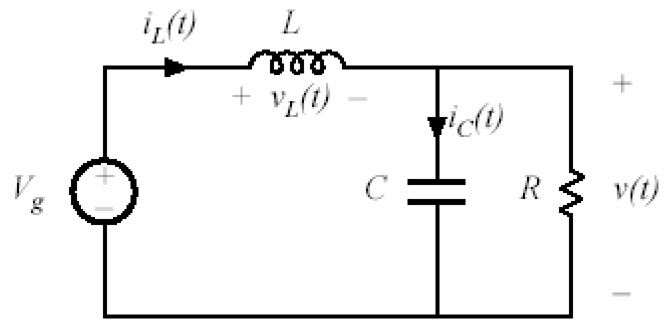
I. INTRODUCTION

Buck converter at steady-state:



I. INTRODUCTION

Interval I: *Switch in position 1*



Inductor voltage

$$v_L = V_g - v(t)$$

Small ripple approximation:

$$v_L \approx V_g - V$$

Knowing the inductor voltage, we can now find the inductor current via

$$v_L(t) = L\frac{di_L(t)}{dt}$$

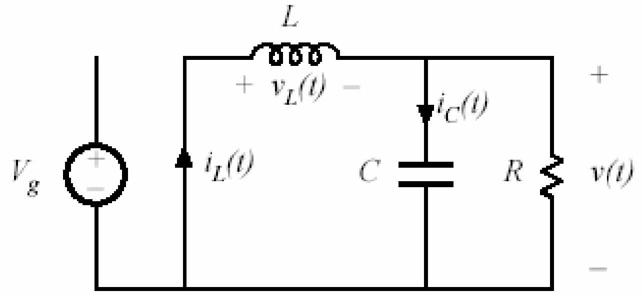
Solve for the slope:

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} \approx \frac{V_g - V}{L}$$

$\Rightarrow$ *The inductor current changes with an essentially constant slope*

I. INTRODUCTION

Interval II: *Switch in position 2*



Inductor voltage

$$v_L(t) = -\,v(t)$$

Small ripple approximation:

$$v_L(t) \approx -\,V$$

Knowing the inductor voltage, we can again find the inductor current via

$$v_L(t) = L\,\frac{di_L(t)}{dt}$$

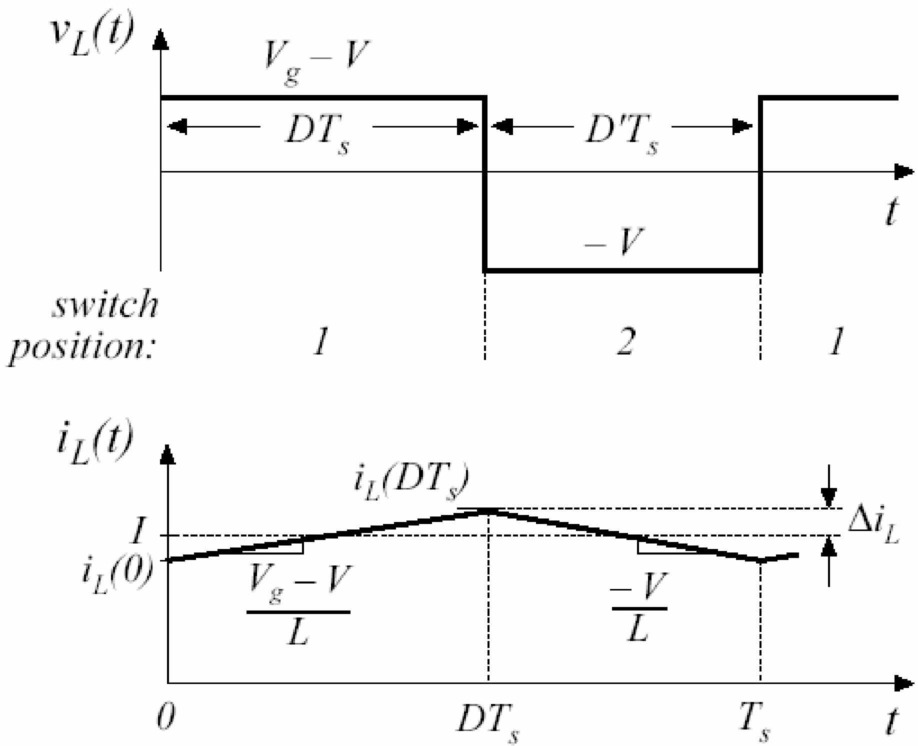
Solve for the slope:

$$\frac{di_L(t)}{dt} \approx -\,\frac{V}{L}$$

⇒ *The inductor current changes with an essentially constant slope*

I. INTRODUCTION

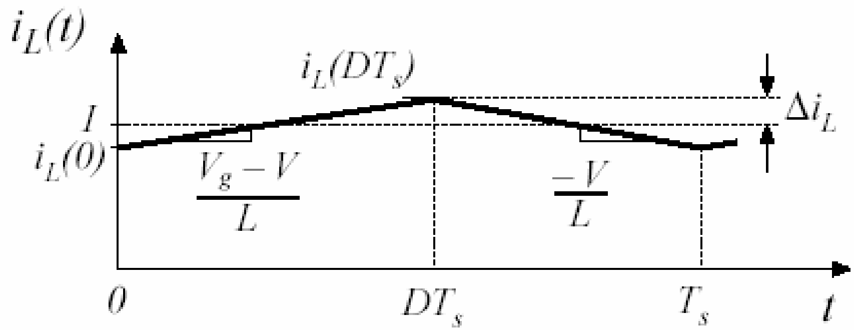
Inductor voltage and current waveforms



$$v_L(t) = L\,\frac{di_L(t)}{dt}$$

I. INTRODUCTION

Inductor current ripple magnitude:



$$(\text{change in } i_L) = (\text{slope})(\text{length of subinterval})$$

$$(2\Delta i_L) = \left(\frac{V_g - V}{L}\right)(DT_s)$$

$$\Rightarrow \qquad \Delta i_L = \frac{V_g - V}{2L} DT_s \qquad\qquad L = \frac{V_g - V}{2\Delta i_L} DT_s$$

I. INTRODUCTION

Inductor volt-second balance:

Inductor defining relation:

$$v_L(t) = L\,\frac{di_L(t)}{dt}$$

Integrate over one complete switching period:

$$i_L(T_s) - i_L(0) = \frac{1}{L}\int_0^{T_s} v_L(t)\,dt$$

In periodic steady state, the net change in inductor current is zero:

$$0 = \int_0^{T_s} v_L(t)\,dt$$

Hence, the total area (or volt-seconds) under the inductor voltage waveform is zero whenever the converter operates in steady state.

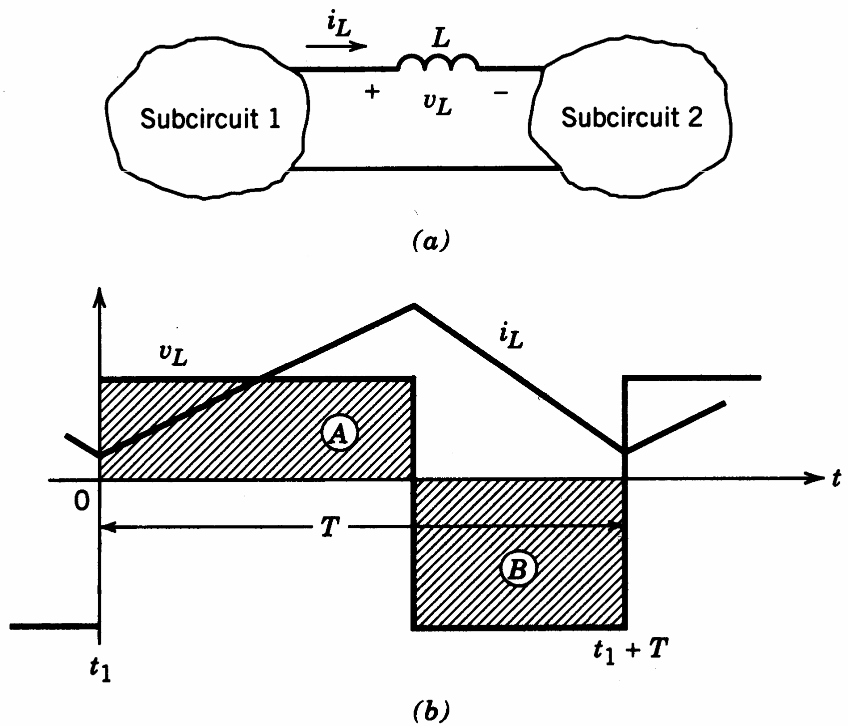
An equivalent form:

$$0 = \frac{1}{T_s}\int_0^{T_s} v_L(t)\,dt = \left\langle v_L \right\rangle$$

The average inductor voltage is zero in steady state.

I. INTRODUCTION

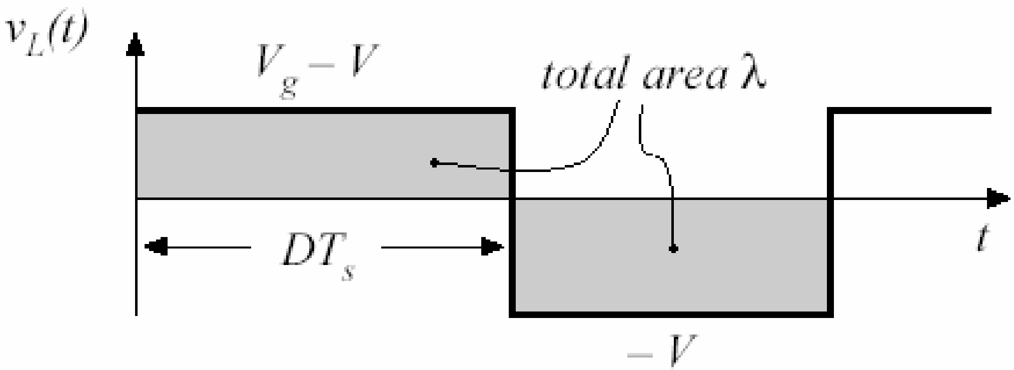
Inductor Voltage and Current in Steady State



- Volt-seconds over *T* equal zero.

I. INTRODUCTION

Inductor volt-second balance in the buck converter:



Integral of voltage waveform is area of rectangles:

$$\lambda = \int_0^{T_s} v_L(t)\,dt = (V_g - V)(DT_s) + (-V)(D'T_s)$$

Average voltage is

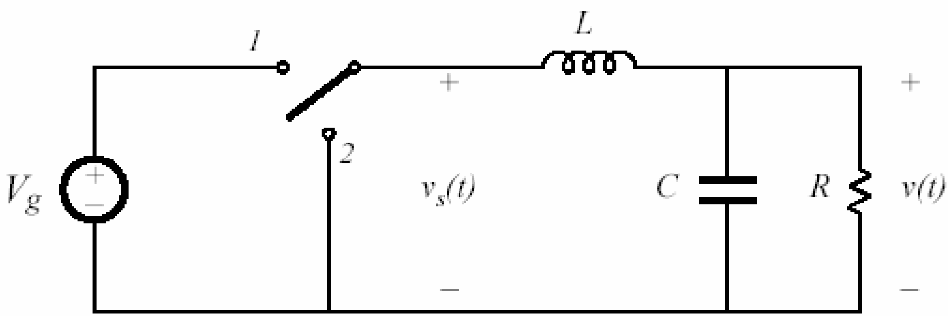
$$\langle v_L \rangle = \frac{\lambda}{T_s} = D(V_g - V) + D'(-V)$$

Equate to zero and solve for *V*:

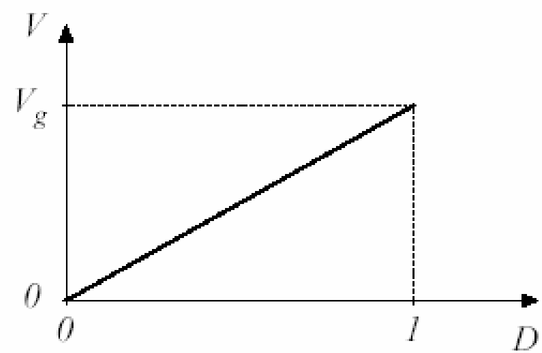
$$0 = DV_g - (D + D')V = DV_g - V \qquad \Rightarrow \qquad V = DV_g$$

I. INTRODUCTION

The Buck Converter (DC component of output voltage)



$$v \approx \langle v_s \rangle = DV_g$$



I. INTRODUCTION

Capacitor charge-balance:

Capacitor defining relation:

$$i_C(t) = C\,\frac{dv_C(t)}{dt}$$

Integrate over one complete switching period:

$$v_C(T_s) - v_C(0) = \frac{1}{C}\int_0^{T_s} i_C(t)\,dt$$

In periodic steady state, the net change in capacitor voltage is zero:

$$0 = \frac{1}{T_s}\int_0^{T_s} i_C(t)\,dt = \langle i_C \rangle$$

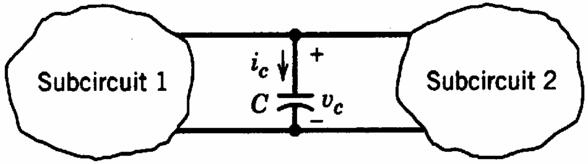
Hence, the total area (or charge) under the capacitor current waveform is zero whenever the converter operates in steady state. The average capacitor current is then zero.

I. INTRODUCTION

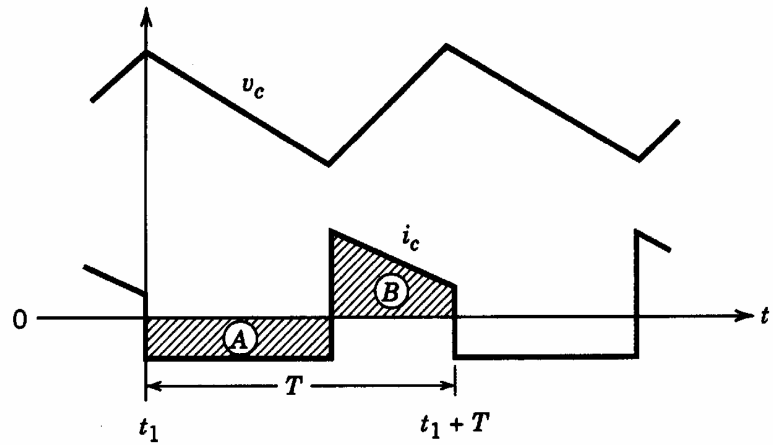
Capacitor Voltage and Current

in Steady State

- Amp-seconds over *T* equal zero.



(a)



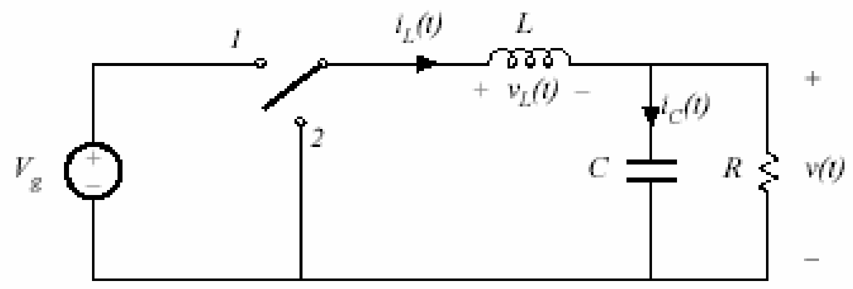
(b)

I. INTRODUCTION

The Buck Converter (Actual output voltage)

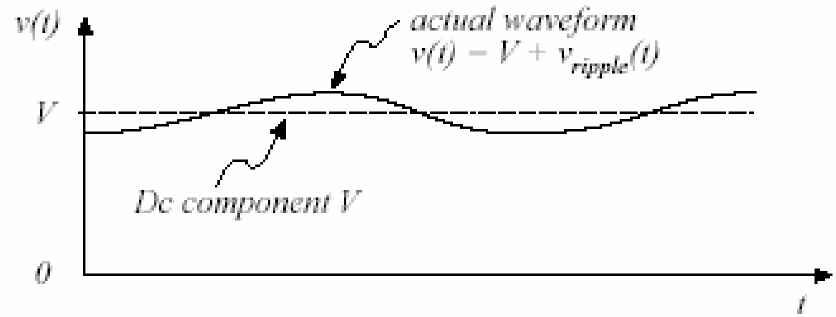
Actual output voltage waveform, buck converter

Buck converter containing practical low-pass filter



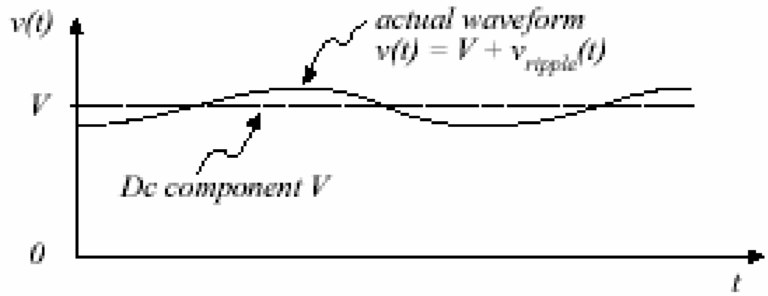
Actual output voltage waveform

$$v(t) = V + v_{ripple}(t)$$



I. INTRODUCTION

$$v(t) = V + v_{ripple}(t)$$



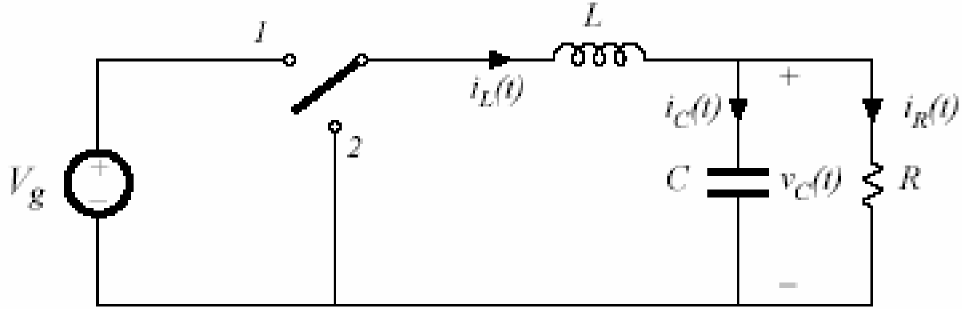
In a well-designed converter, the output voltage ripple is small. Hence, the waveforms can be easily determined by ignoring the ripple:

$$\left| v_{ripple} \right| << V$$

$$v(t) \approx V$$

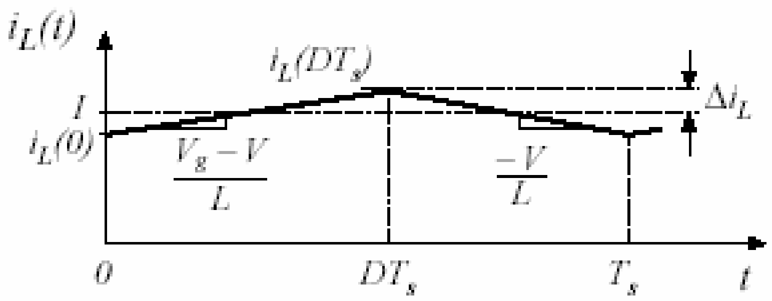
I. INTRODUCTION

Buck converter example: Determine output voltage ripple



Inductor current waveform.

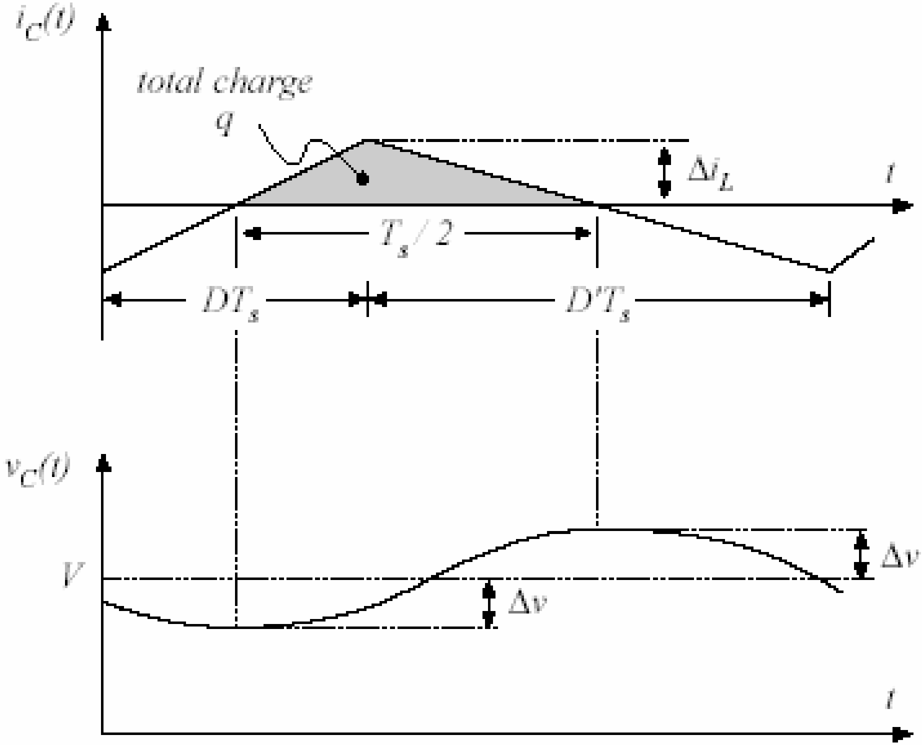
What is the capacitor current?



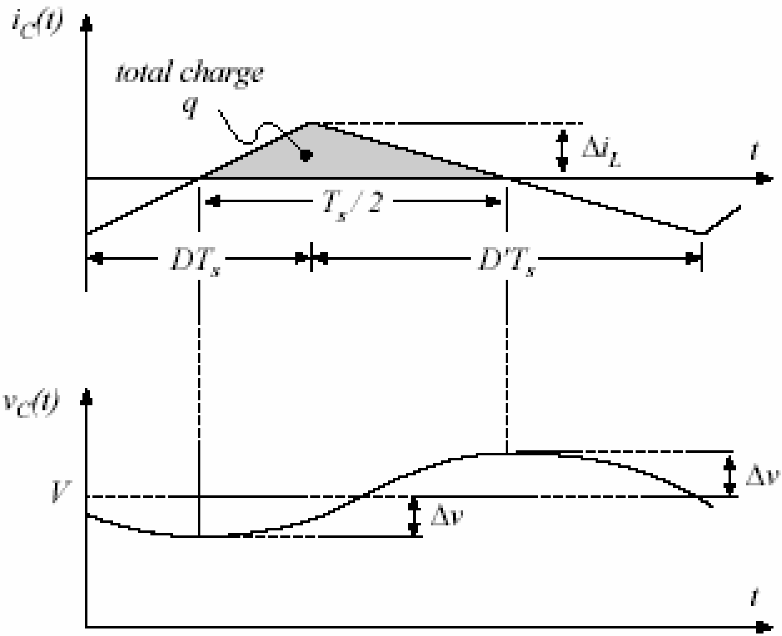
I. INTRODUCTION

Must not neglect inductor current ripple!

If the capacitor voltage ripple is small, then essentially all of the ac component of inductor current flows through the capacitor.



I. INTRODUCTION



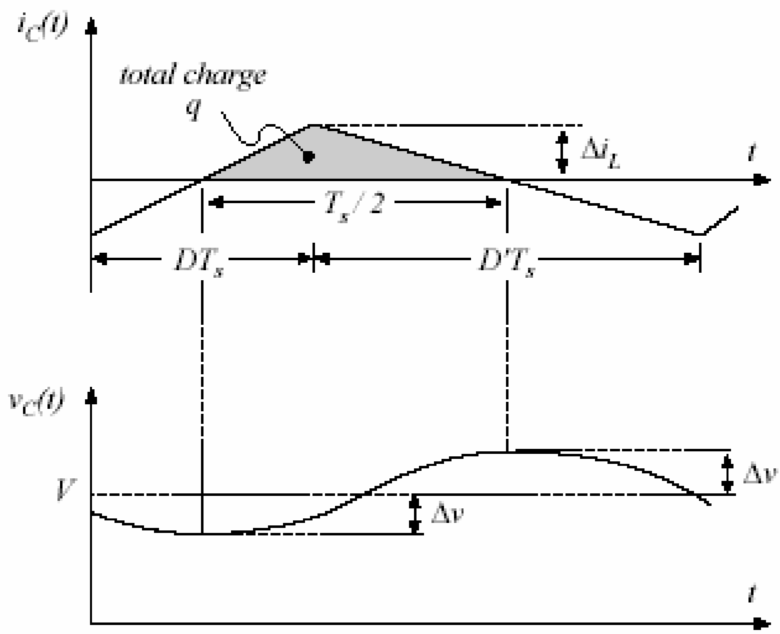
Current $i_C(t)$ is positive for half of the switching period. This positive current causes the capacitor voltage $v_C(t)$ to increase between its minimum and maximum extrema. During this time, the total charge q is deposited on the capacitor plates, where

$$q = C\,(2\Delta v)$$

$$(change\ in\ charge) = C\,(change\ in\ voltage)$$

I. INTRODUCTION

Estimating capacitor voltage ripple Δv



The total charge q is the area of the triangle, as shown:

$$q = \frac{1}{2}\Delta i_L \frac{T_s}{2}$$

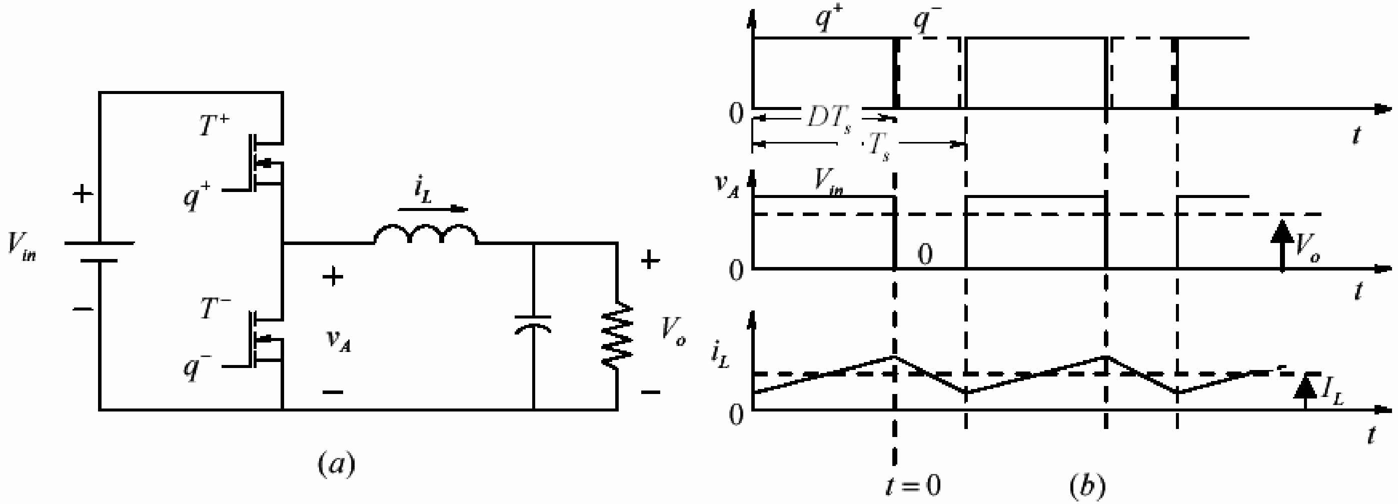
Eliminate q and solve for Δv:

$$\Delta v = \frac{\Delta i_L T_s}{8\,C}$$

Note: in practice, capacitor equivalent series resistance (esr) further increases Δv.

I. INTRODUCTION

SYNCHRONOUS-RECTIFIED BUCK CONVERTER FOR VERY LOW OUTPUT VOLTAGES



Synchronous rectification is a technique to reduce conduction loss by using a MOSFET switch in place of a diode.

I. INTRODUCTION

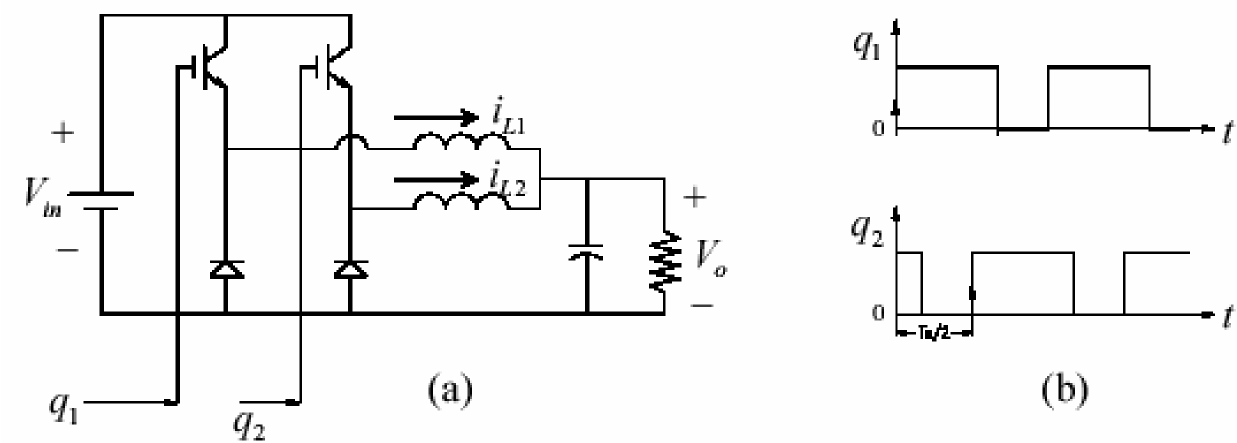
INTERLEAVING OF CONVERTERS

Interleaved Multiphase Converters

One method of increasing the output power of any topology and reducing the stresses upon the semiconductors, is a technique called interleaving. Any topology can be interleaved. An *interleaved multiphase* converter has two or more identical converters placed in parallel which share key components. For an n–phase converter, each converter is driven at a phase difference of $360/n$ degrees from the next. The output current from all the phases sum together at the output, requiring only I_{out}/n amperes from each phase.

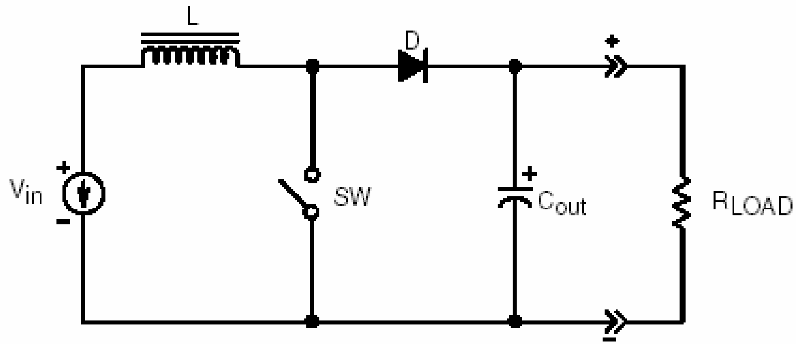
The input and output capacitors are shared among the phases. The input capacitor sees less RMS ripple current because the peak currents are less and the combined duty cycle of the phases is greater than it would experience with a single phase converter. The output capacitor can be made smaller because the frequency of current waveform is n–times higher and its combined duty cycle is greater. The semiconductors also see less current stress.

A block diagram of an interleaved multiphase buck converter is shown in Figure . This is a 2–phase topology that is useful in providing power to a high performance microprocessor.

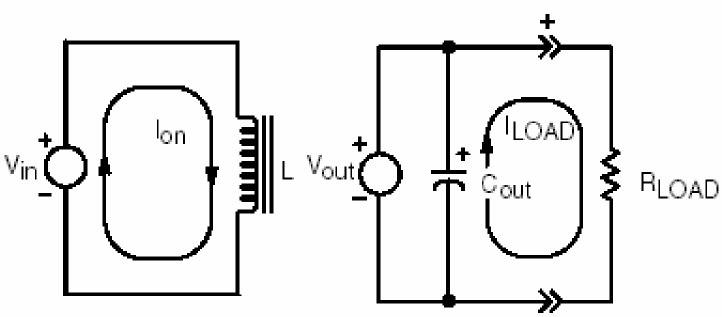


I. INTRODUCTION

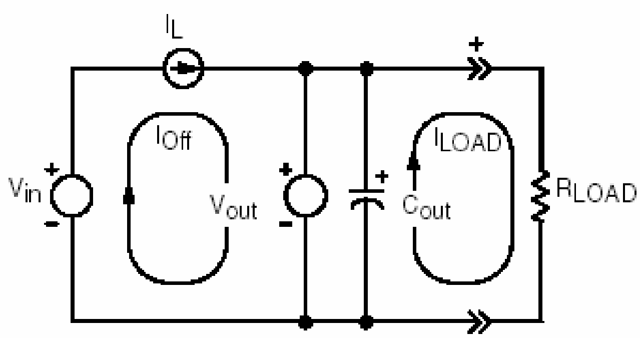
1.4.2. BOOST CONVERTER



A Basic Flyback-Mode Converter
(Boost Converter Shown)



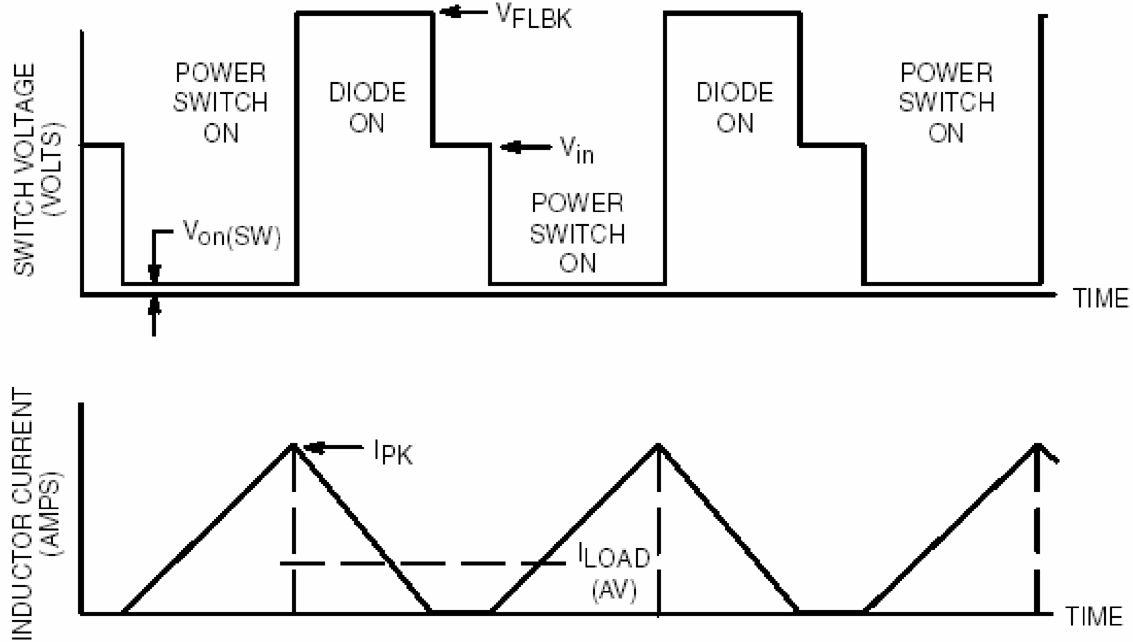
Power Switch ON



Power Switch OFF

I. INTRODUCTION

BOOST CONVERTER

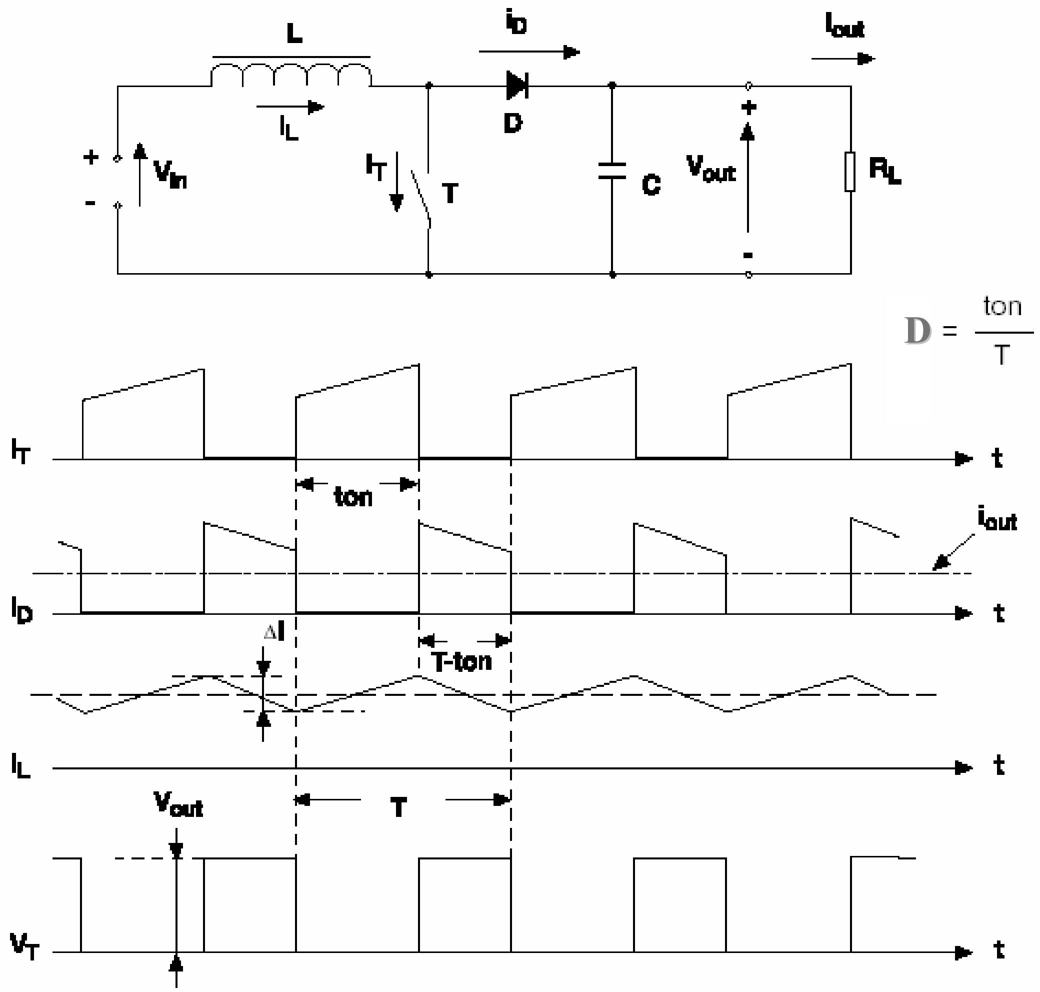


Waveforms of a boost converter in discontinuous conduction

I. INTRODUCTION

Boost Converter Waveforms:

(continuous conduction)



I. INTRODUCTION

Boost Converter

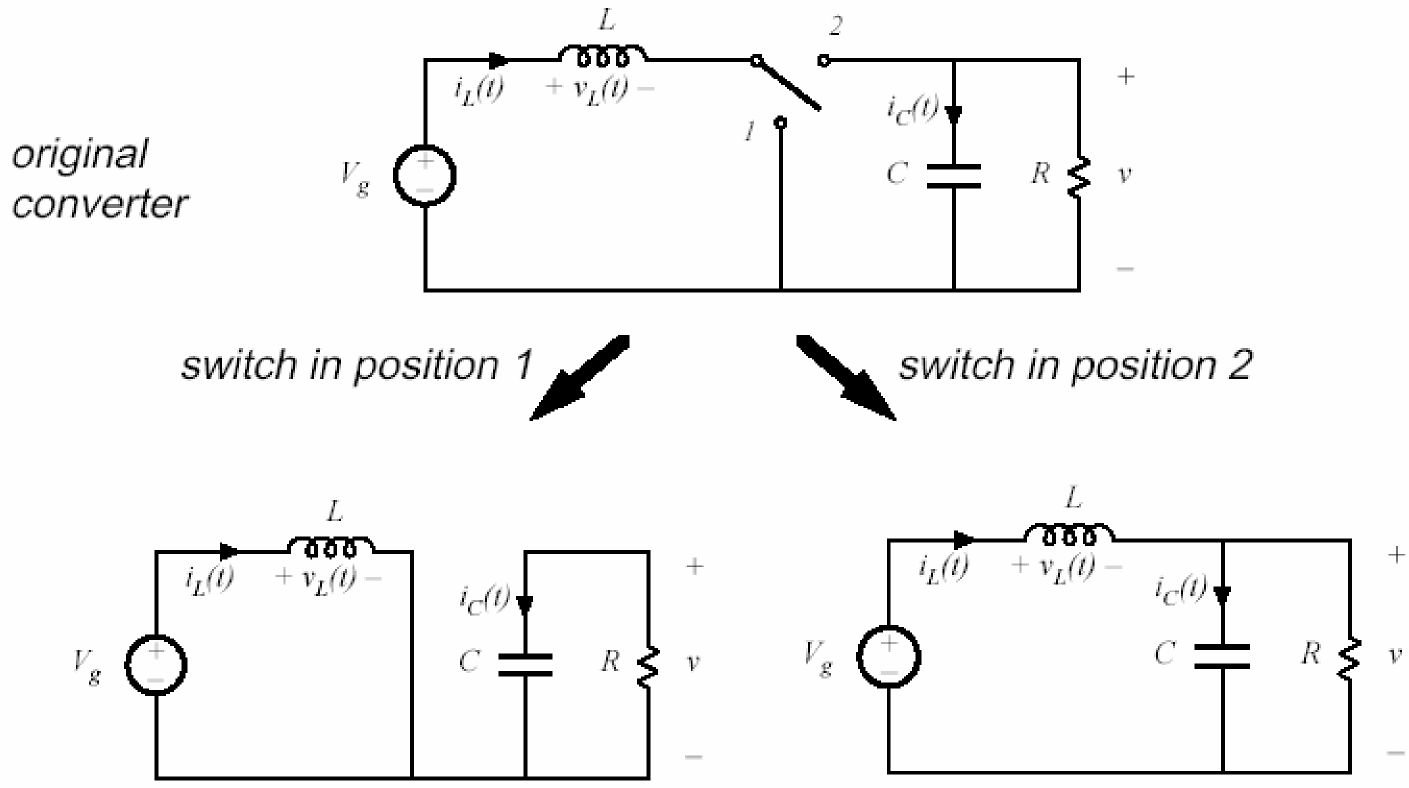
In normal operation, the energy is fed from the inductor to the load, and then stored in the output capacitor. For this reason, the output capacitor is stressed a lot more than in the Buck converter. $V_{out} = V_{in} / (1-D)$

Device selection:

- *Power Switch:* V_{ce} or $V_{dss} > V_{out}$
- I_{cmax} or $I_{Dmax} > I_{out} /(1- D) + \Delta I/2$
- *Rectifier:* $V_{RRM} > V_{out}$; $I_{fav} > I_{out}$

I. INTRODUCTION

Boost converter analysis at steady-state: (continuous conduction)

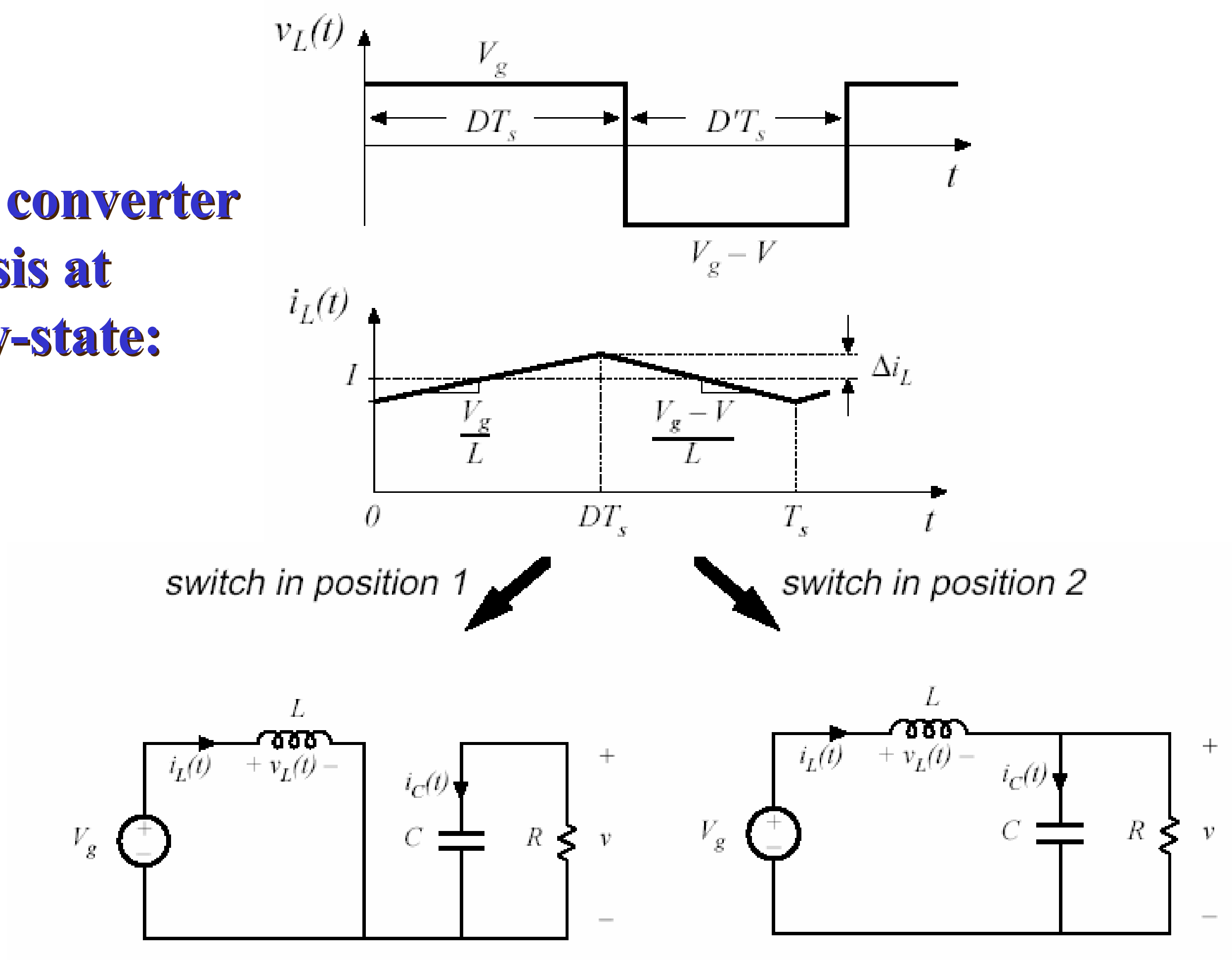


Q1 ON, D1 OFF

Q1 OFF, D1 ON

I. INTRODUCTION

Boost converter analysis at steady-state:

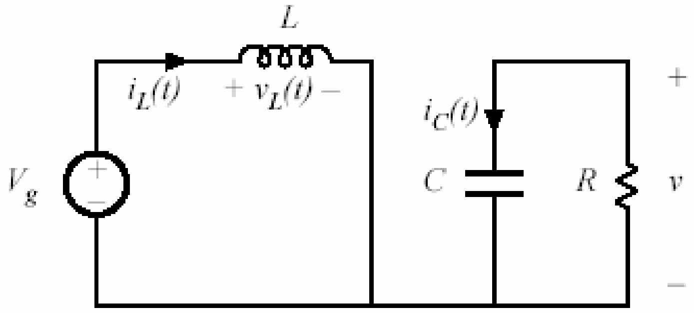


I. INTRODUCTION

Interval I: *Switch 1 in position 1*

Inductor voltage and capacitor current

$$v_L = V_g$$
$$i_C = -v / R$$



Small ripple approximation:

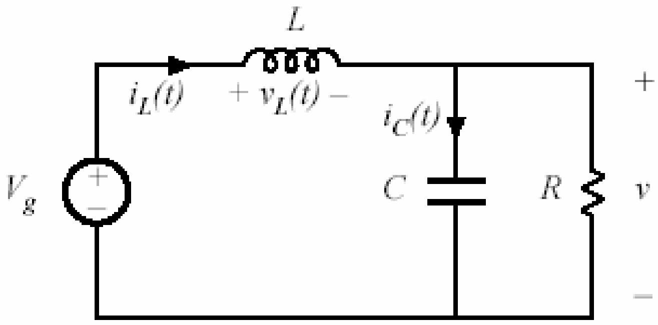
$$v_L = V_g$$
$$i_C = -V / R$$

I. INTRODUCTION

Interval II: *Switch 1 in position 2*

Inductor voltage and capacitor current

$$v_L = V_g - v$$
$$i_C = i_L - v / R$$

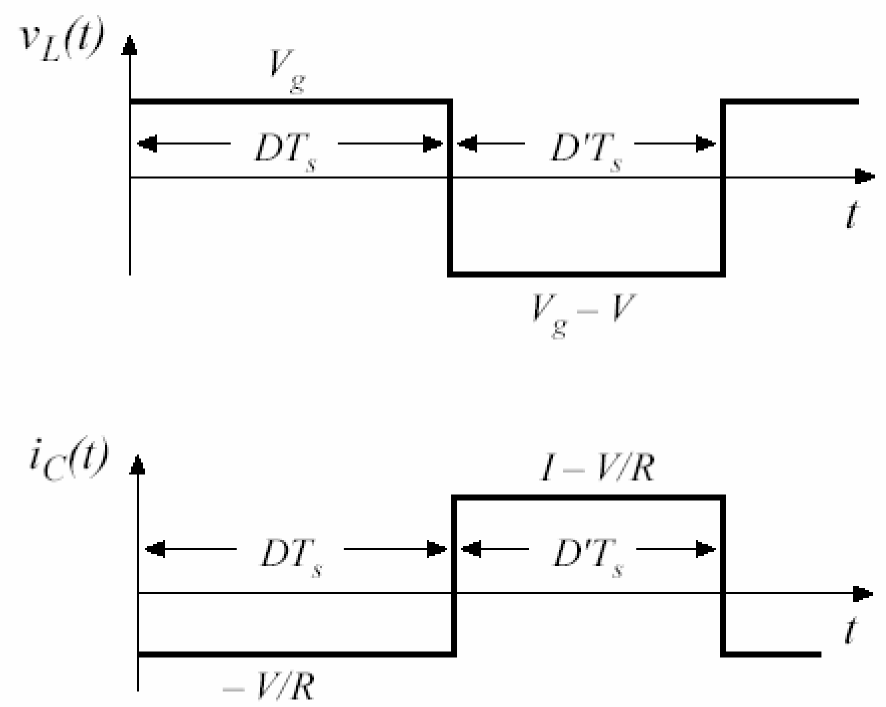


Small ripple approximation:

$$v_L = V_g - V$$
$$i_C = I - V / R$$

I. INTRODUCTION

Inductor current and capacitor voltage waveforms

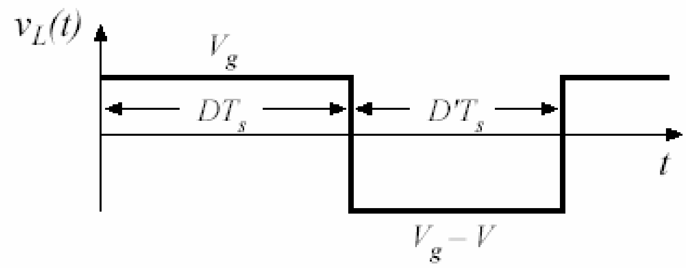


I. INTRODUCTION

Inductor volt-second balance:

Net volt-seconds applied to inductor over one switching period:

$$\int_0^{T_s} v_L(t)\,dt = (V_g)\,DT_s + (V_g - V)\,D'T_s$$



Equate to zero and collect terms:

$$V_g\,(D + D') - V\,D' = 0$$

Solve for V:

$$V = \frac{V_g}{D'}$$

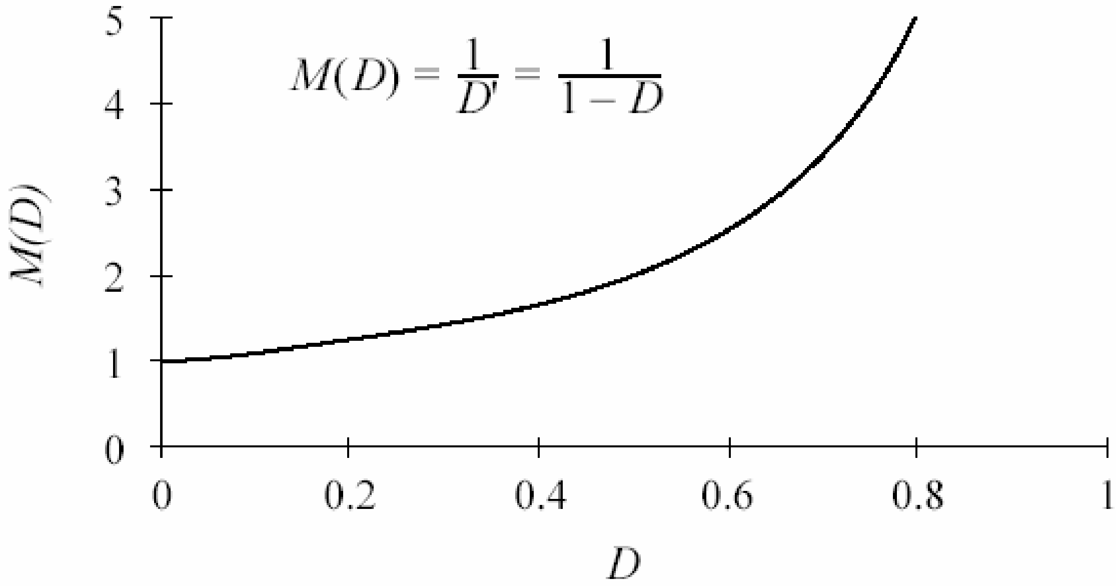
The voltage conversion ratio is therefore

$$M(D) = \frac{V}{V_g} = \frac{1}{D'} = \frac{1}{1-D}$$

I. INTRODUCTION

Conversion ratio of the boost converter

$$M(D) = V_{out}/V_{in}$$

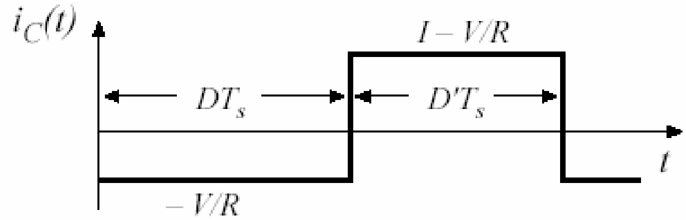


I. INTRODUCTION

Capacitor charge balance

Capacitor charge balance:

$$\int_0^{T_s} i_C(t)\, dt = (-\frac{V}{R})\, DT_s + (I - \frac{V}{R})\, D'T_s$$



Collect terms and equate to zero:

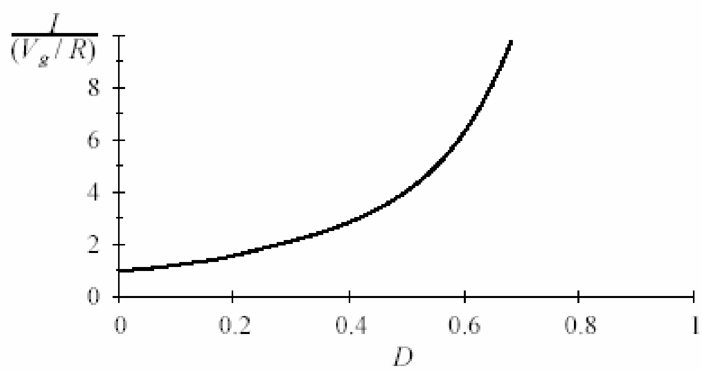
$$-\frac{V}{R}(D + D') + I\,D' = 0$$

Solve for I:

$$I = \frac{V}{D'\,R}$$

Eliminate V to express in terms of V_g:

$$I = \frac{V_g}{D'^2\,R}$$



I. INTRODUCTION

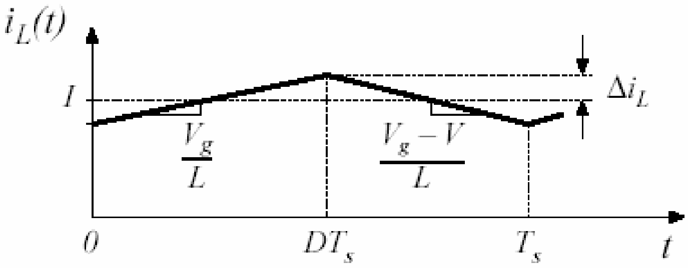
Inductor current ripple component

Inductor current slope during subinterval 1:

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g}{L}$$

Inductor current slope during subinterval 2:

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g - V}{L}$$



Change in inductor current during subinterval 1 is *(slope) (length of subinterval)*:

$$2\Delta i_L = \frac{V_g}{L} DT_s$$

Solve for peak ripple:

$$\Delta i_L = \frac{V_g}{2L} DT_s$$

- Choose L such that desired ripple magnitude is obtained

I. INTRODUCTION

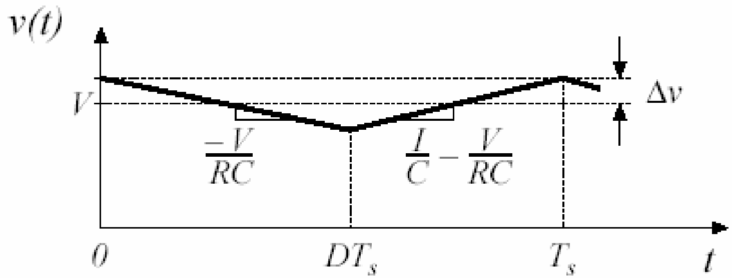
Capacitor voltage ripple

Capacitor voltage slope during subinterval 1:

$$\frac{dv_C(t)}{dt} = \frac{i_C(t)}{C} = \frac{-V}{RC}$$

Capacitor voltage slope during subinterval 2:

$$\frac{dv_C(t)}{dt} = \frac{i_C(t)}{C} = \frac{I}{C} - \frac{V}{RC}$$



Change in capacitor voltage during subinterval 1 is *(slope) (length of subinterval)*:

$$-2\Delta v = \frac{-V}{RC} DT_s$$

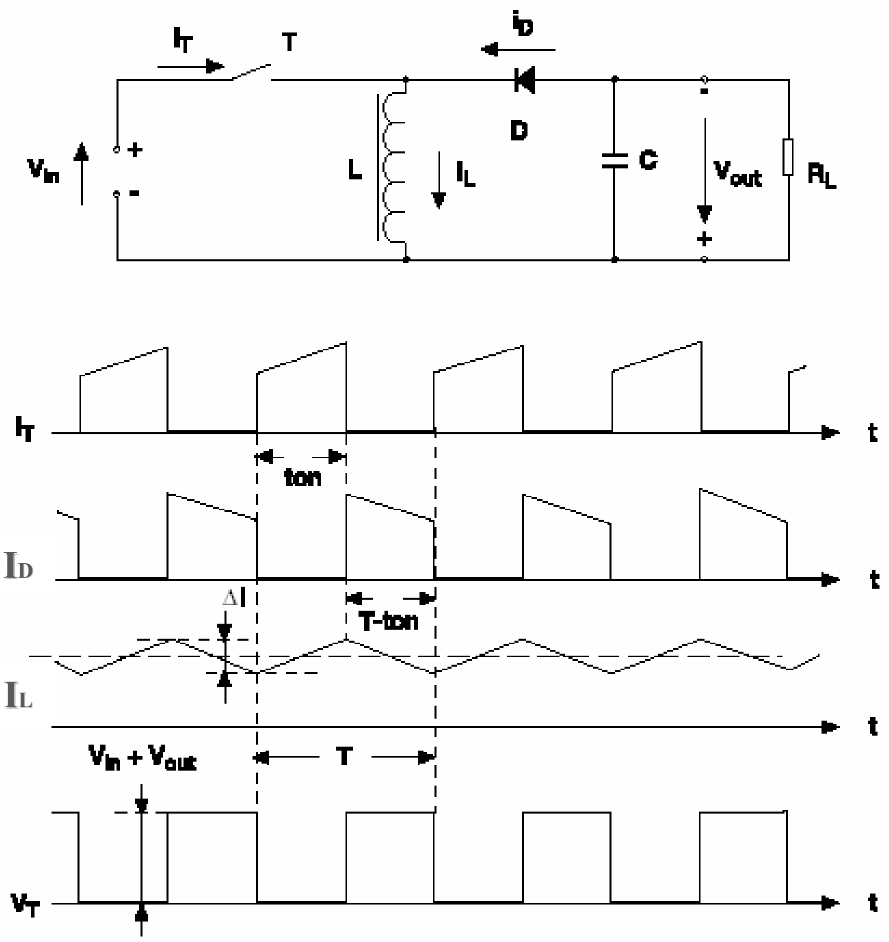
Solve for peak ripple:

$$\Delta v = \frac{V}{2RC} DT_s$$

- Choose *C* such that desired voltage ripple magnitude is obtained
- In practice, capacitor *equivalent series resistance* (esr) leads to increased voltage ripple

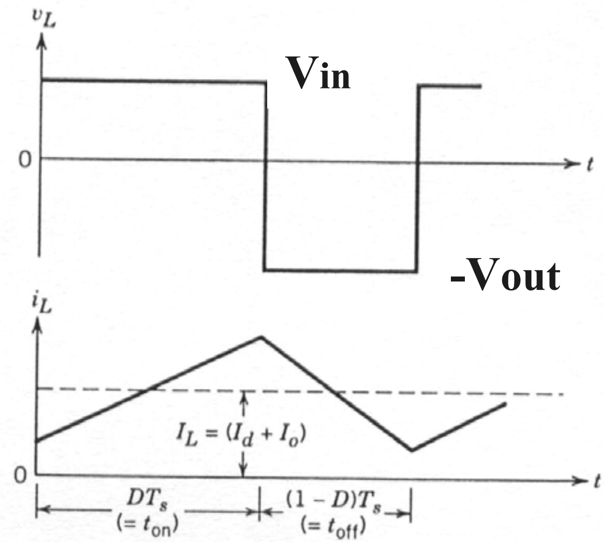
I. INTRODUCTION

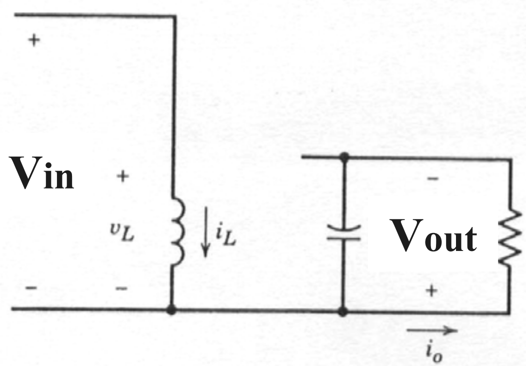
BUCK-BOOST CONVERTER

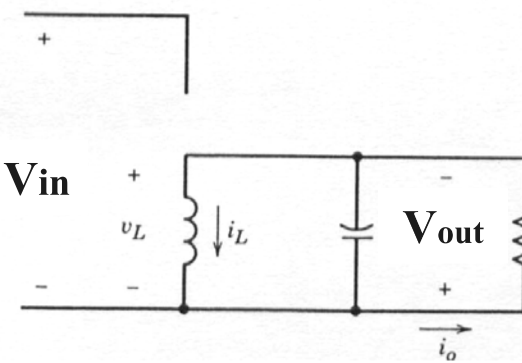


I. INTRODUCTION

Buck-boost converter operation:

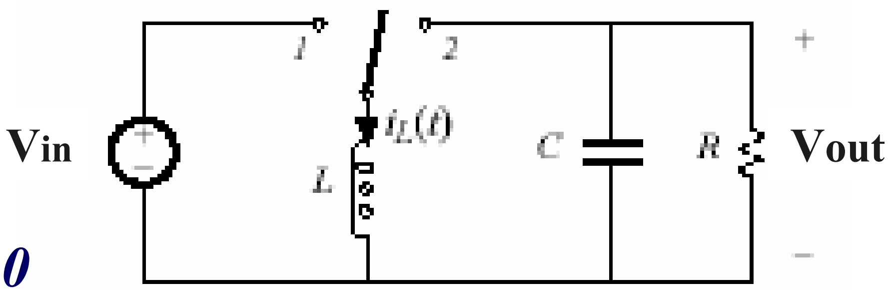






I. INTRODUCTION

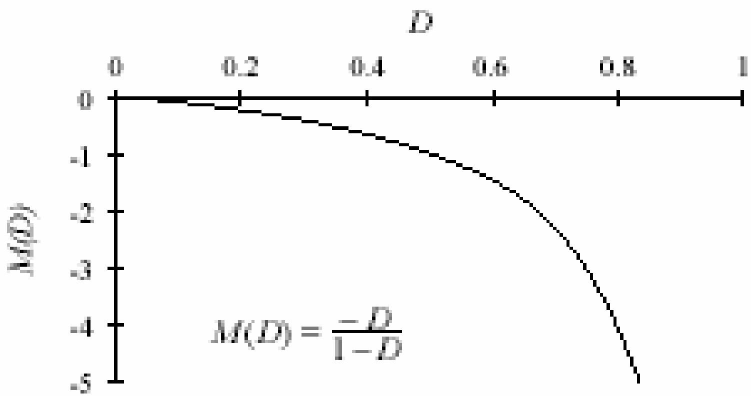
Buck-boost converter:



$$V_{in}\, D\, T_s + V_{out}(1-D)\, T_s = 0$$

$$\Rightarrow V_{out} / V_{in} = M(D)$$

$$= -D / (1-D)$$



The converter steps-up or down the input voltage depending on duty cycle D

I. INTRODUCTION

BUCK-BOOST CONVERTER

For a duty cycle under 0.5, the conversion works in step down mode, for a duty cycle over 0.5, the converter then operates in step-up mode. $V_{out} = -V_{in} D / (1-D)$

Device selection:

❖ **Power Switch:** V_{cemax} or $V_{dss} > V_{in\,max} + V_{out}$
I_{cmax} or $I_{dmax} > I_{out} / (1- D) + \Delta I/2$

❖ ***Rectifier:*** $V_{RRM} > V_{in\,max} + V_{out}$
$I_{fav} > I_{out}$

I. INTRODUCTION

Basic DC-DC Converters:

	STEP DOWN	STEP UP	STEP UP/DOWN
V_{out}	$V_{in} . \delta$	$V_{in}/1- \delta$	$[-V_{in} .\delta] / [1- \delta]$
RMS current in C_{out}	low	high	high
Supplied input current	discontinuous	continuous	discontinuous
Gate drive	floating	grounded	floating

δ: duty cycle

I. INTRODUCTION

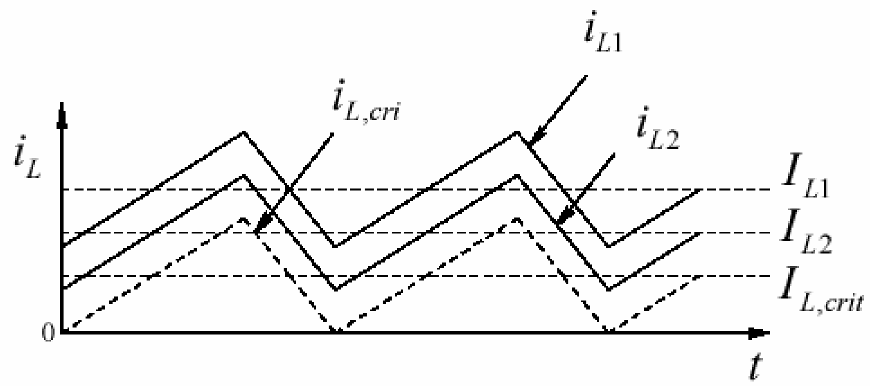
Device Voltages and Currents

Criterion		Buck	Boost	Buck-Boost
Transistor $\hat{V}$		V_{in}	V_o	$(V_{in}+V_o)$
Transistor $\hat{I}$		I_o	I_{in}	$I_{in}+I_o$
I_{rms}	Transistor	$\sqrt{D}I_o$	$\sqrt{D}I_{in}$	$\sqrt{D}\left(I_{in}+I_o\right)$
I_{avg}	Transistor	DI_o	DI_{in}	$D\left(I_{in}+I_o\right)$
	Diode	$(1-D)I_o$	$(1-D)I_{in}$	$(1-D)\left(I_{in}+I_o\right)$
I_L		I_o	I_{in}	$I_{in}+I_o$
Effect of L on C		significant	little	little
Pulsating Current		input	output	both

D: duty cycle

I. INTRODUCTION

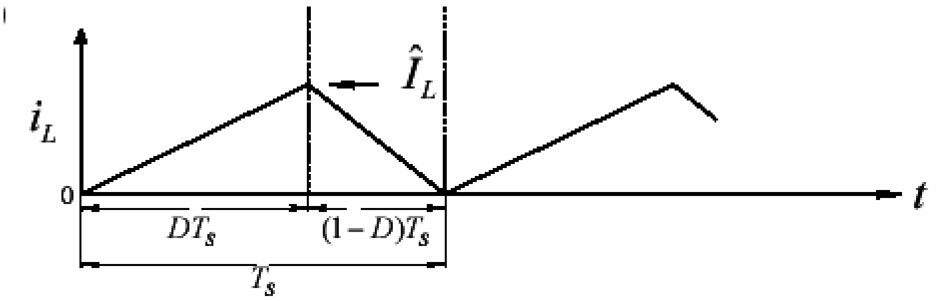
DISCONTINUOUS-CONDUCTION MODE (DCM)



Inductor current at various loads, duty ratio kept constant

I. INTRODUCTION

Critical inductor currents

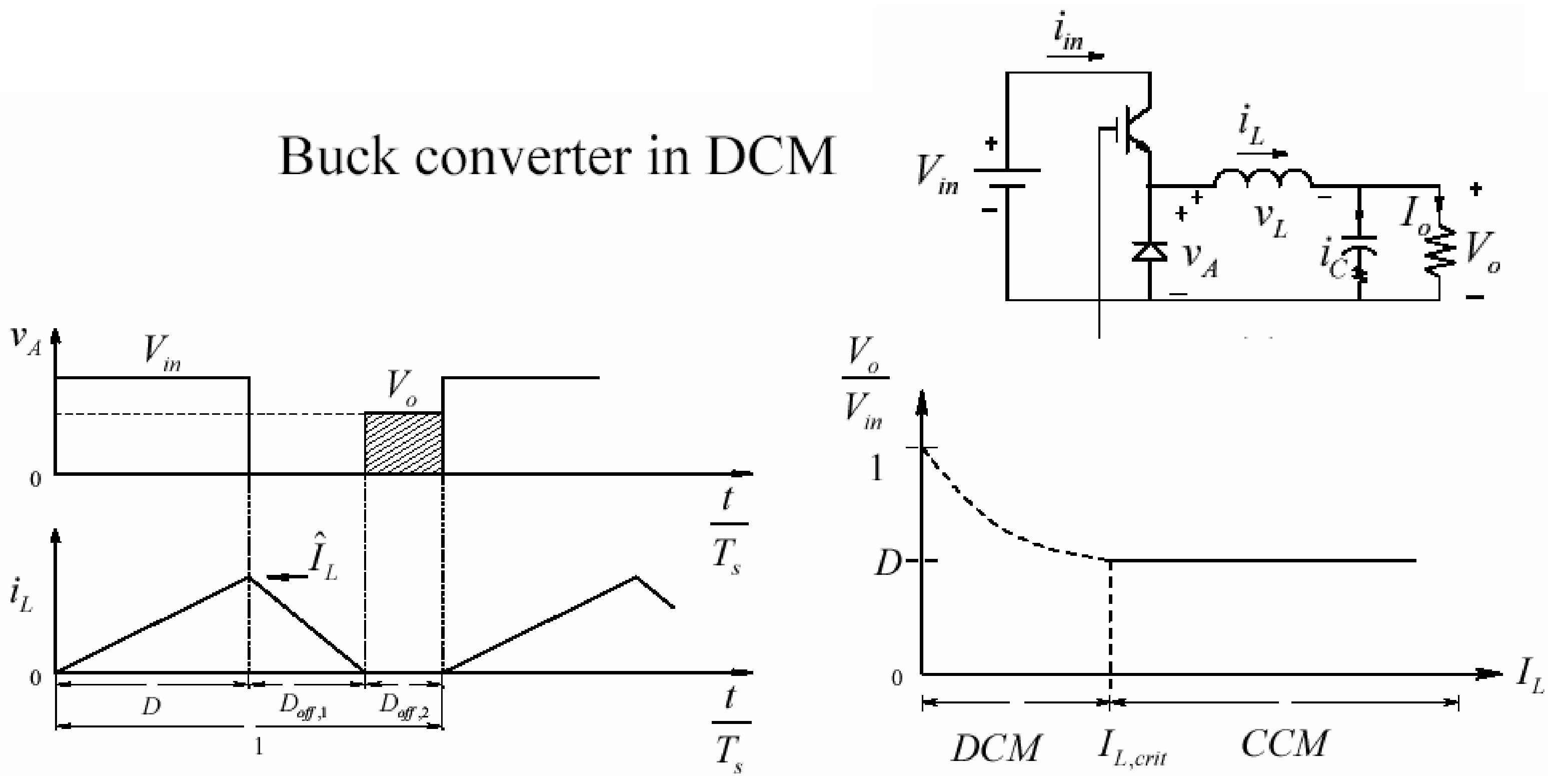


$$I_{L,crit,Buck} = \frac{V_{in}}{2Lf_s} D(1-D)$$

$$I_{L,crit,Boost} = I_{L,crit,Buck\text{-}Boost} = \frac{V_{in}}{2Lf_s} D$$

I. INTRODUCTION

Buck converter in DCM

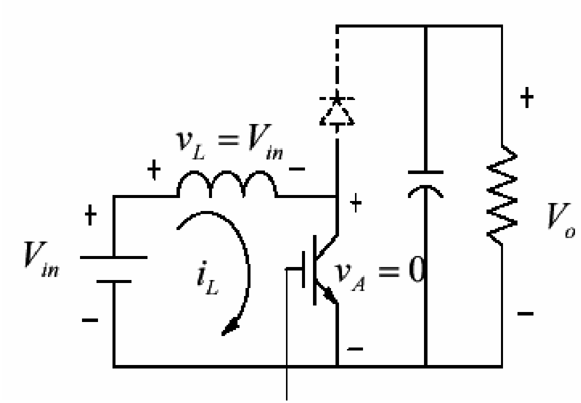


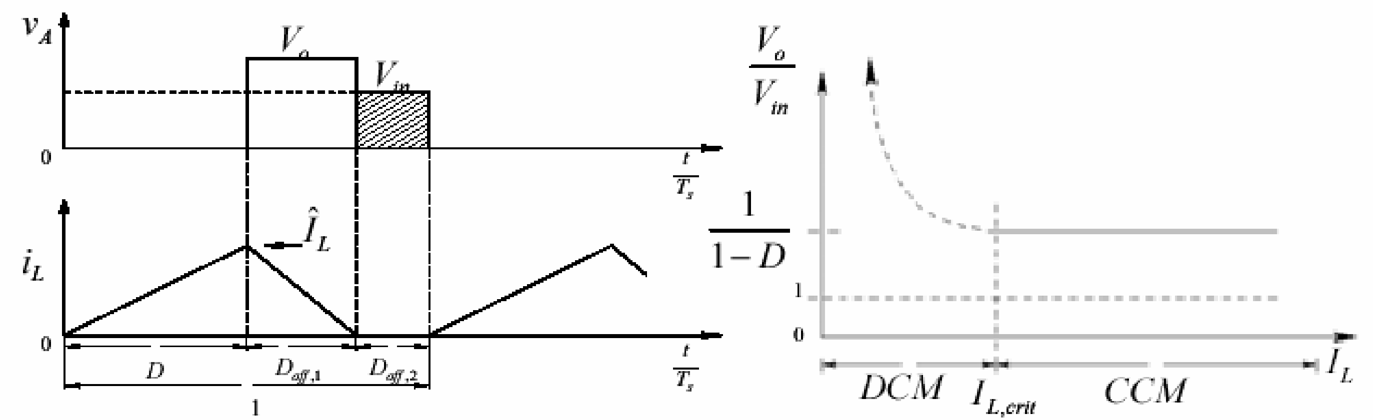
(a)

(b)

I. INTRODUCTION

Boost Converters in DCM

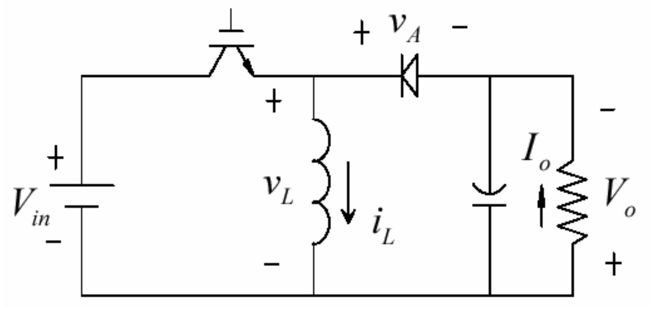


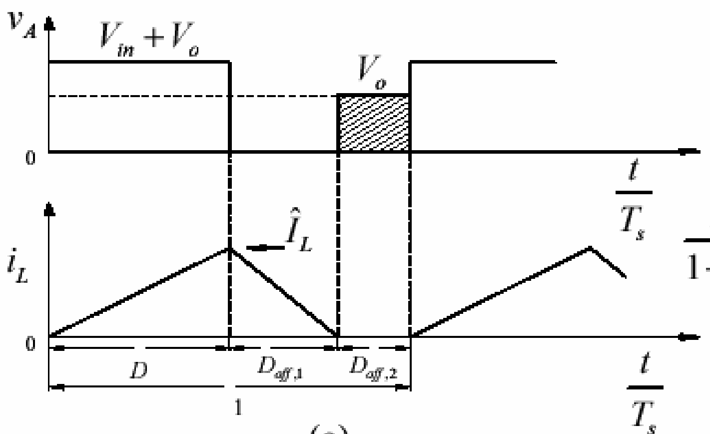


(a) (b)

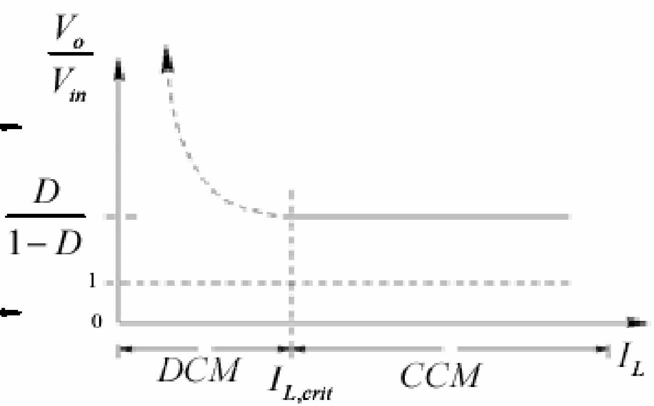
I. INTRODUCTION

Buck-Boost converter in DCM





(a)



(b)

I. INTRODUCTION

Summary

1. The dc component of a converter waveform is given by its average value, or the integral over one switching period, divided by the switching period. Solution of a dc-dc converter to find its dc, or steady-state, voltages and currents therefore involves averaging the waveforms.
2. The linear ripple approximation greatly simplifies the analysis. In a well-designed converter, the switching ripples in the inductor currents and capacitor voltages are small compared to the respective dc components, and can be neglected.
3. The principle of inductor volt-second balance allows determination of the dc voltage components in any switching converter. In steady-state, the average voltage applied to an inductor must be zero.

I. INTRODUCTION

Summary

4. The principle of capacitor charge balance allows determination of the dc components of the inductor currents in a switching converter. In steady-state, the average current applied to a capacitor must be zero.
5. By knowledge of the slopes of the inductor current and capacitor voltage waveforms, the ac switching ripple magnitudes may be computed. Inductance and capacitance values can then be chosen to obtain desired ripple magnitudes.
6. In converters containing multiple-pole filters, continuous (nonpulsating) voltages and currents are applied to one or more of the inductors or capacitors. Computation of the ac switching ripple in these elements can be done using capacitor charge and/or inductor flux-linkage arguments, without use of the small-ripple approximation.