Hacettepe University
Electrical and Electronics Engineering Department

ELE 764
Special Topics in Electrical and Electronics Engineering

Lecture Notes
Chapter VII

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Electromagnetic Interference (EMI)

- **7.1. EMI Considerations**

  Conducted and Radiated EMI, EMI Sources, Circuit Layouts to Mitigate EMI Problems

- **7.2. EMC Standards**
- **7.3. EMI Filters and Shielding** *(Ref: B. Mammano and B. Carsten, 'Understanding and Optimizing Electromagnetic Compatibility in SMPS)*
- **7.4. PCB Layout Considerations**

Electromagnetic Interference (EMI)

7.1. EMI Considerations

EMI (Electromagnetic Interference) is the unwanted coupling of signals from one circuit or system to another

Conducted EMI: unwanted coupling of signals via conduction through parasitic impedances, power and ground connections

Radiated EMI: unwanted coupling of signals via radio transmission

These effects usually arise from poor circuit layout and unmodeled parasitic impedances

Analog circuits rarely work correctly unless engineering effort is expended to solve EMI and layout problems

Sooner or later (or now!), the engineer needs to learn to deal with EMI

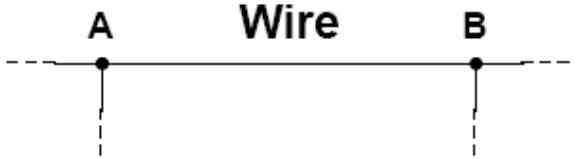
The ideal engineering approach:

- figure out what are the significant EMI sources
- figure out where the EMI is going
- engineer the circuit layout to mitigate EMI problems

Build a layout that can be understood and analyzed

Assumptions made in Circuits

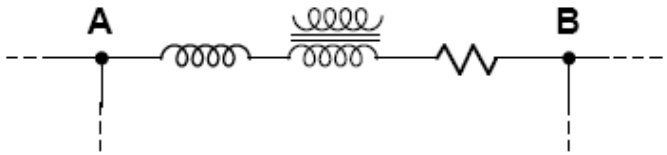
1. Wires are perfect (equipotential) conductors



$V_A = V_B$

This assumption ignores

- wire resistance
- wire inductance
- mutual inductance with other conductors

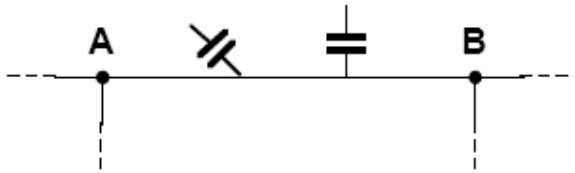


EMI CONSIDERATIONS

A related assumption:

1a. The space surrounding a wire is a perfect insulator (dielectric constant = 0)

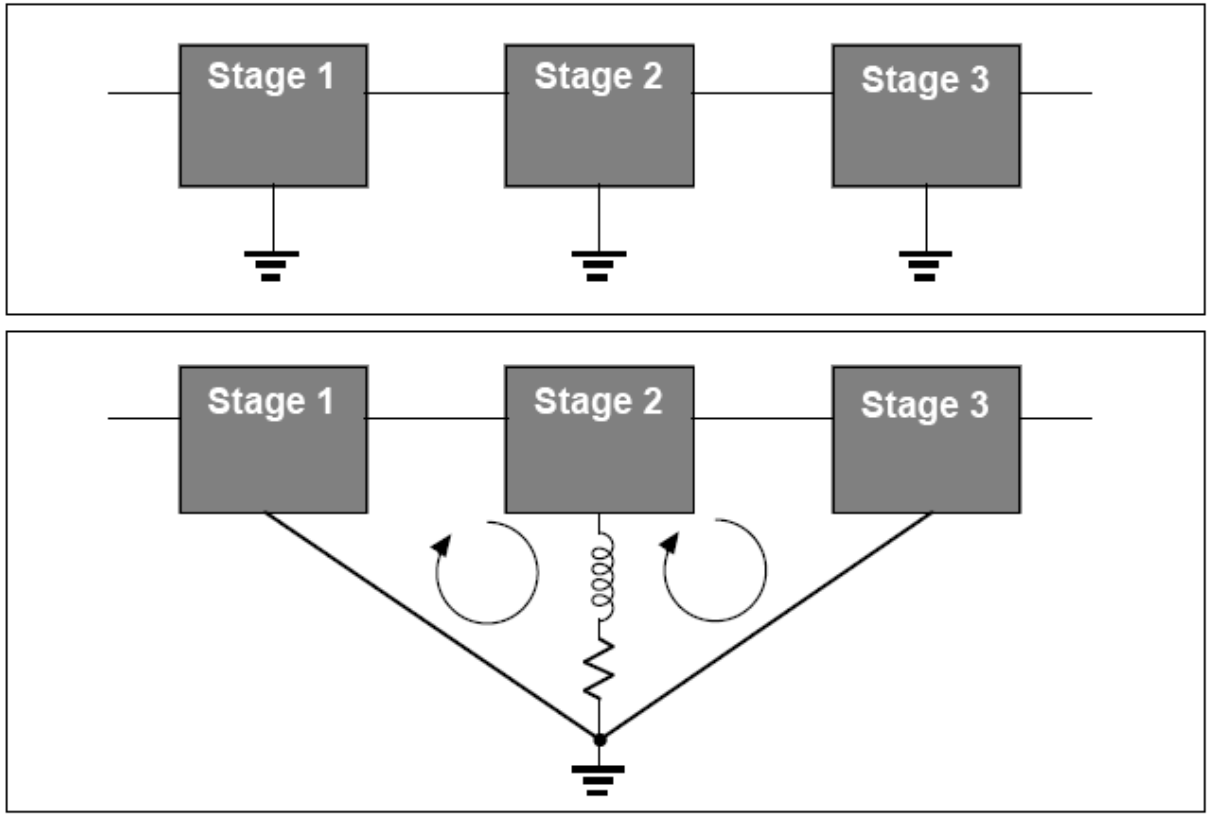
This assumption ignores capacitance between conductors



EMI CONSIDERATIONS

2. The ground (reference) node is at zero potential

Formally, this is a definition. But there is an implicit assumption that all parts of the system can be connected via ideal conductors to a common ground node. In practice, it is often quite difficult to ensure that each stage of a system operates with the same zero potential reference.



EMI CONSIDERATIONS

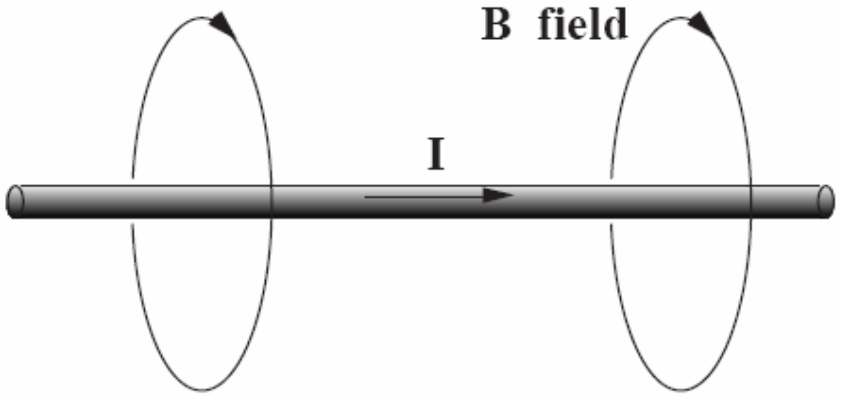
We reinforce the problem by freely using the ground symbol

By use of this symbol, we avoid indicating how the actual wiring connection is made. In consequence, the possibility of conducted EMI via nonideal ground conductors is ignored

EMI CONSIDERATIONS

About inductance of wires

Single wire in space



Self inductance

$$L = \frac{\lambda}{i}$$

$$L = 0.00508\, l \left(2.303 \log_{10}\left(\frac{4l}{d}\right) - 0.75\right) \mu H$$

Terman, *Radio Engineer's Handbook*, p. 48ff, 1943

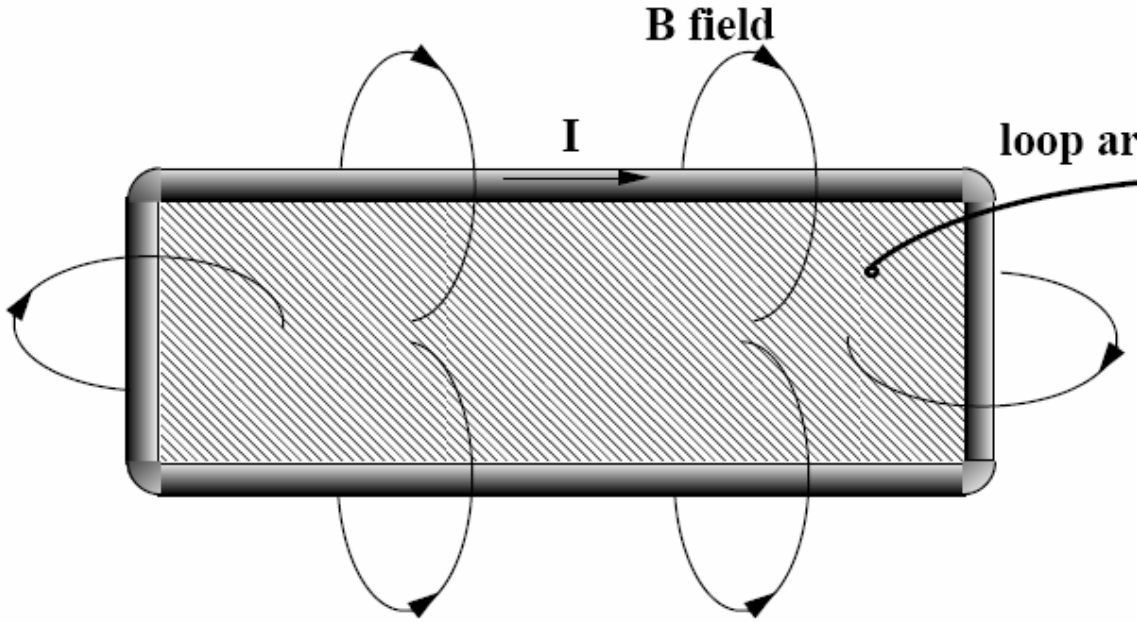
l = wire length
d = wire diameter
dimensions in inches

- Larger wire has lower inductance, because B-field must take longer path length around wire
- But how does the charge get back from end to beginning ? There is no closed loop, and so formula ignores area of loop
- Formula ignores effects of nearby conductors

EMI CONSIDERATIONS

A more realistic scenario:

current flows around a closed loop



single-turn air-core inductor

Simple-minded inductance formula:

$$L = \frac{\mu_o A_C}{l_m}$$

$\mu_o = 4\pi \cdot 10^{-7}$ H/m

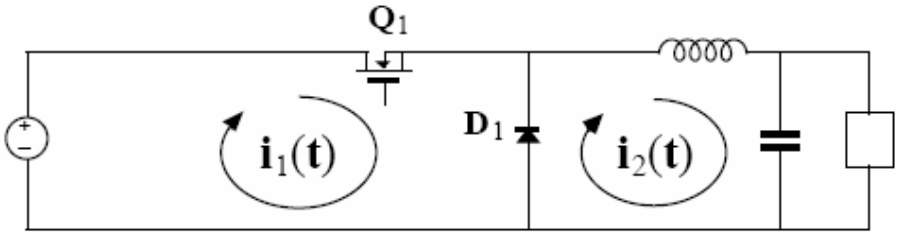
l_m = effective magnetic path length

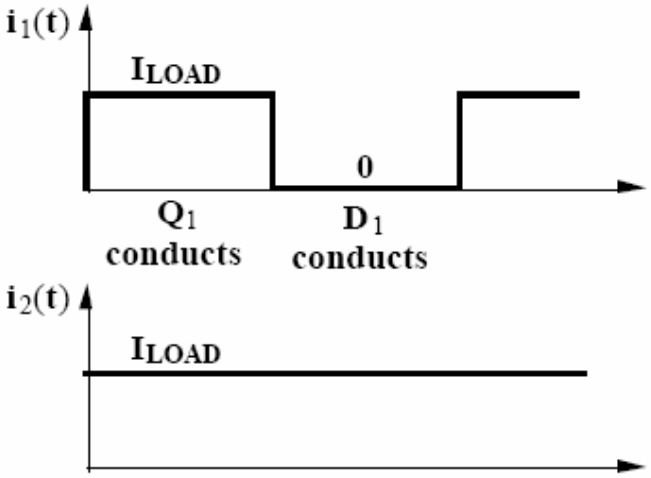
To reduce inductance: reduce loop cross-sectional area (by routing of wires), or increase path length (use larger wire).

EMI CONSIDERATIONS

Example: Buck converter

Use loop analysis





switched input current $i_1(t)$ contains large high frequency harmonics

—hence inductance of input loop is critical

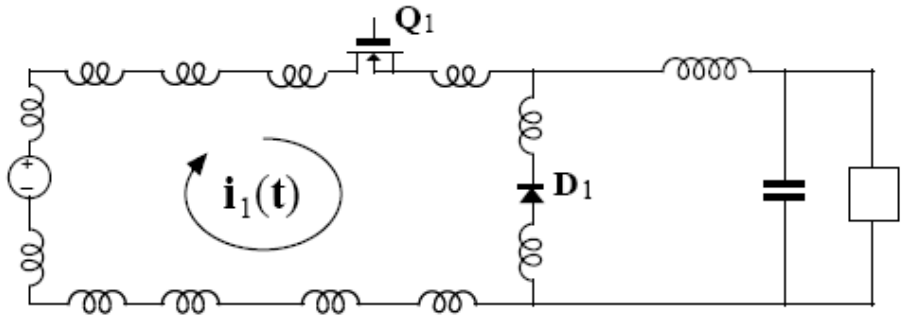
inductance causes ringing, voltage spikes, switching loss, generation of B- and E-fields, radiated EMI

the second loop contains a filter inductor, and hence its current $i_2(t)$ is nearly dc

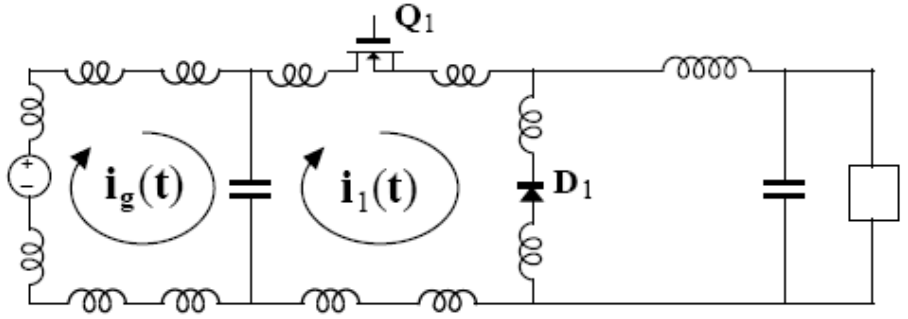
—hence additional inductance is not a significant problem in the second loop

EMI CONSIDERATIONS

Parasitic inductances of input loop explicitly shown:



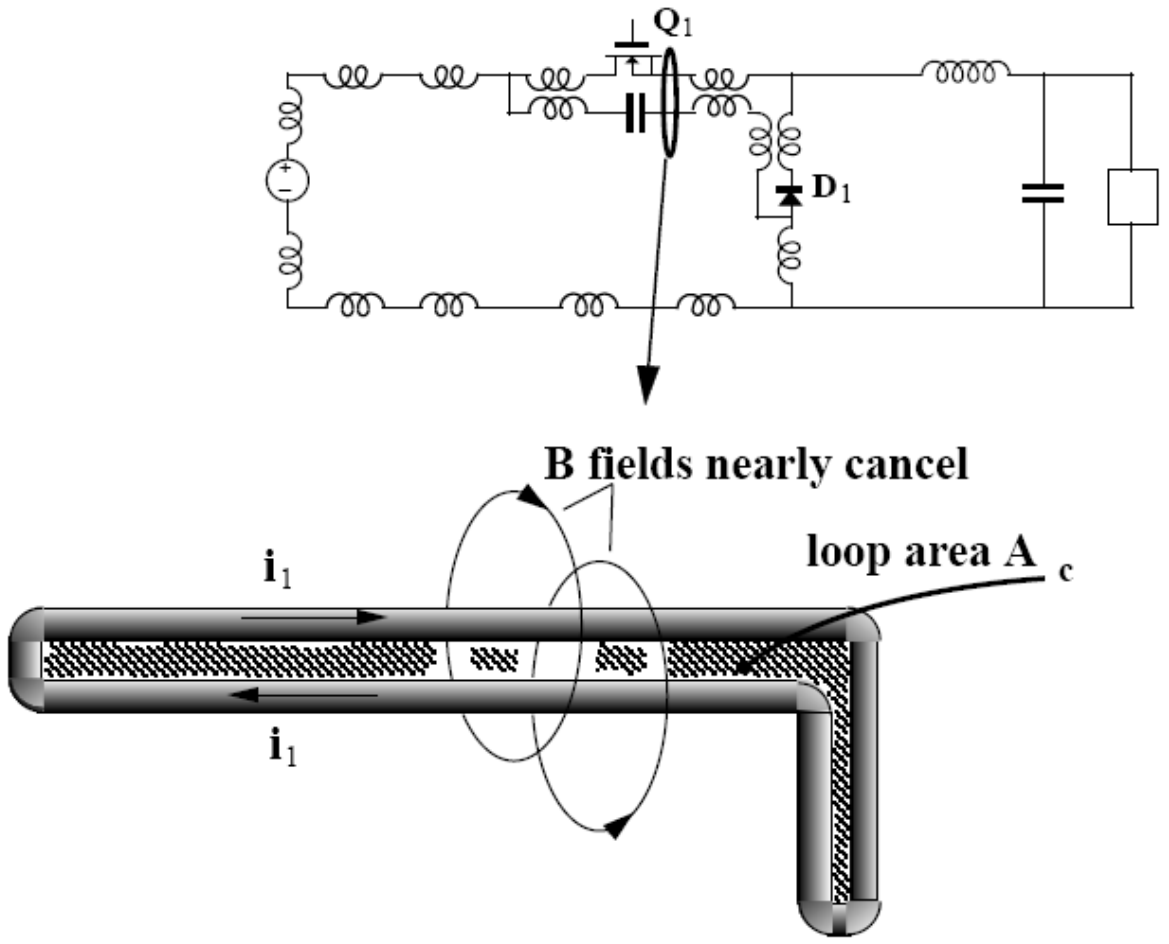
Addition of bypass capacitor confines the pulsating current to a smaller loop:



high frequency currents are shunted through capacitor instead of input source

EMI CONSIDERATIONS

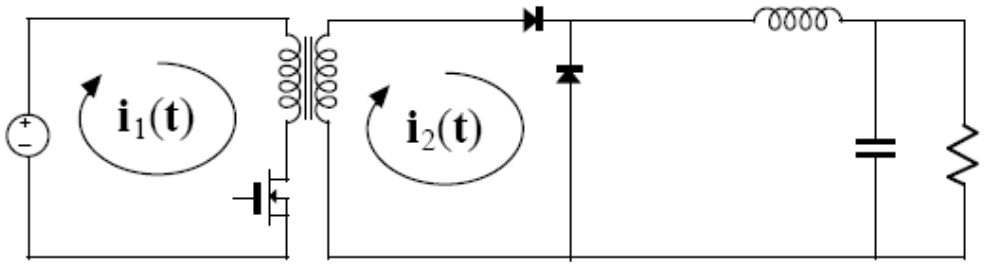
Even better: minimize area of the high frequency loop, thereby minimizing its inductance



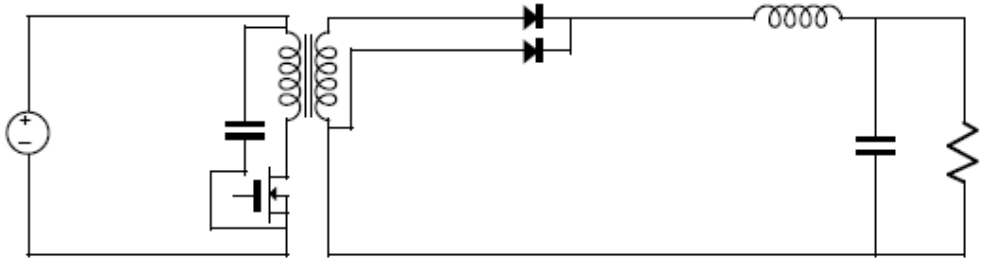
EMI CONSIDERATIONS

Forward converter

Two critical loops:

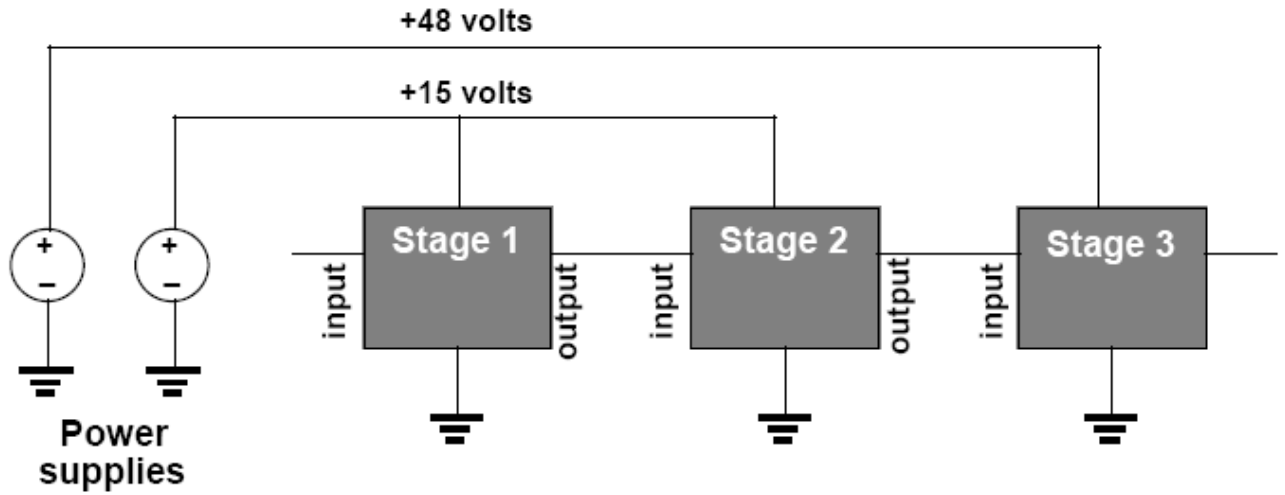


Solution:



EMI CONSIDERATIONS

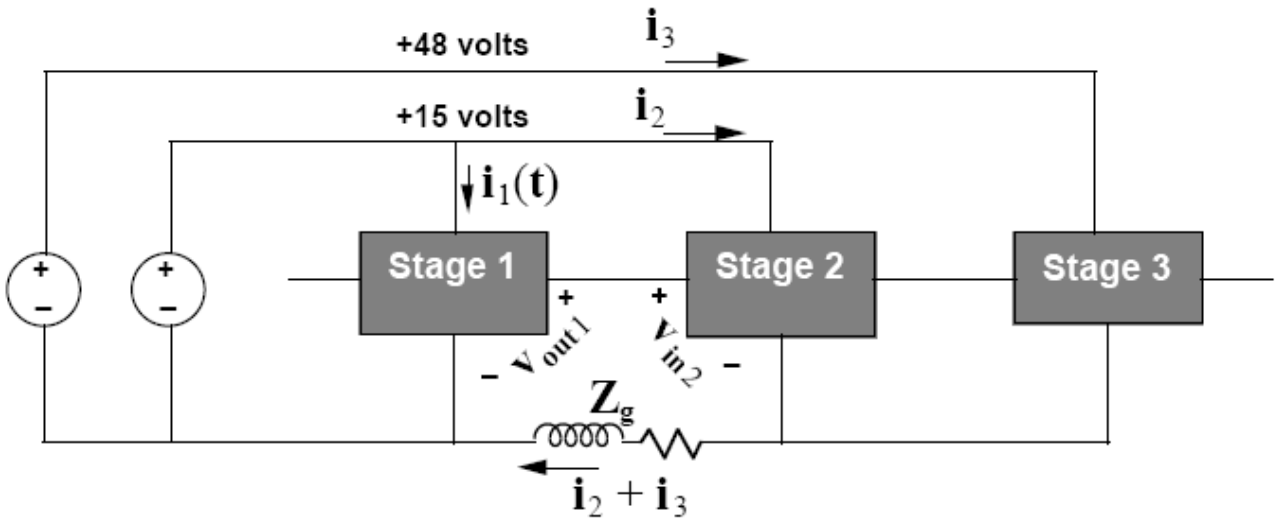
Unwanted coupling of signals via impedance of ground connections



- All currents must flow in closed paths: determine the entire loop in which large currents flow, including the return connections
- Ground (zero potential) references may not be the same for every portion of the system

EMI CONSIDERATIONS

Example: suppose the ground connections are



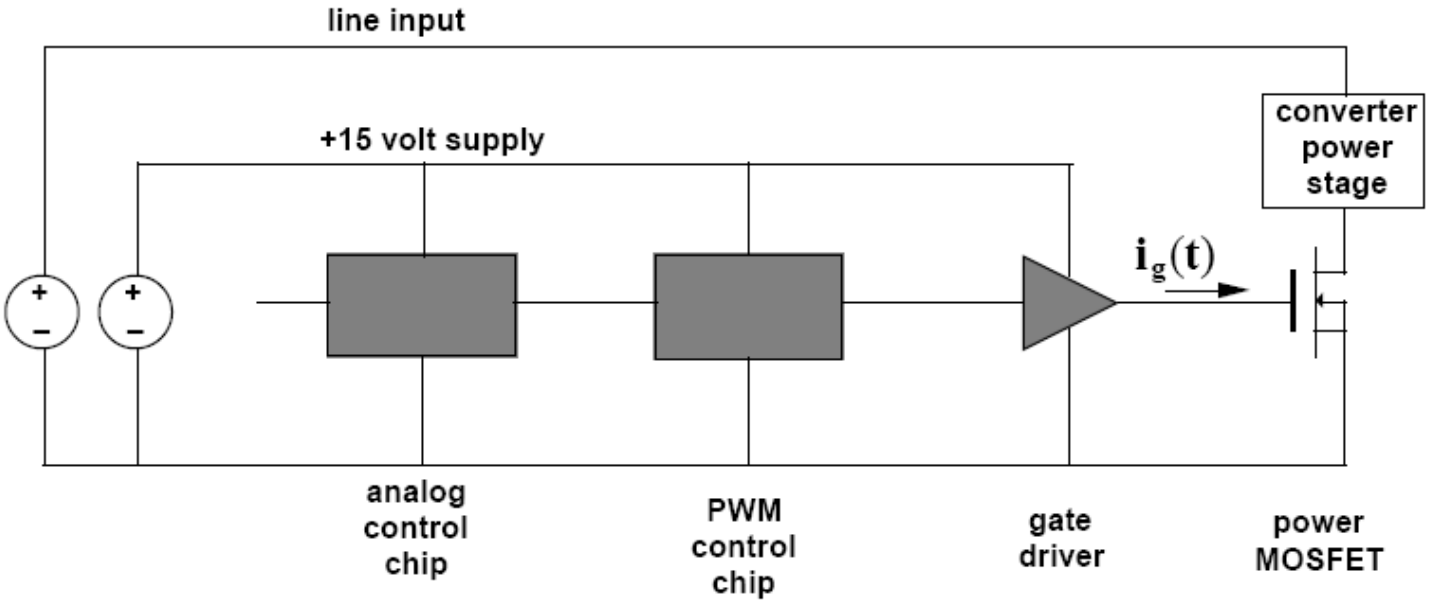
$$v_{in2} = v_{out1} - Z_g (i_2 + i_3)$$

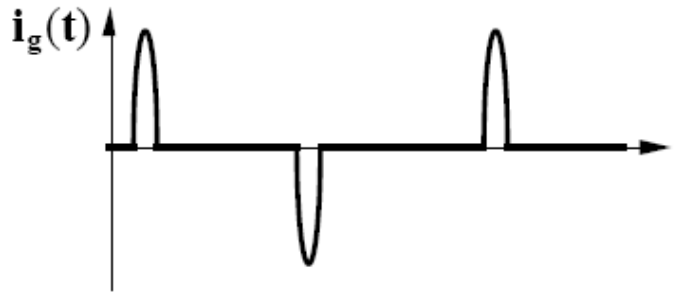
"Noise" from stages 2 and 3 couples into the input to stage 2

This represents conducted EMI, or specifically corruption of the ground reference by system currents

EMI CONSIDERATIONS

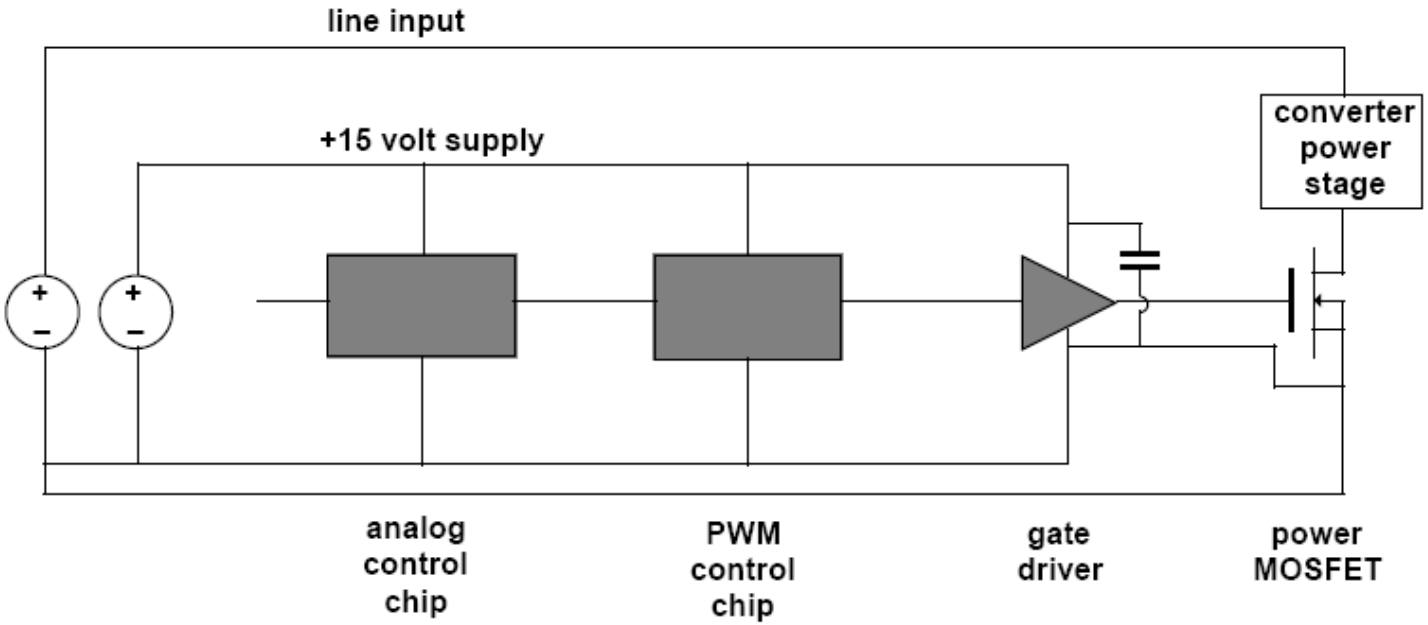
Example: gate driver





EMI CONSIDERATIONS

Solution: bypass capacitor and close coupling of gate and return leads

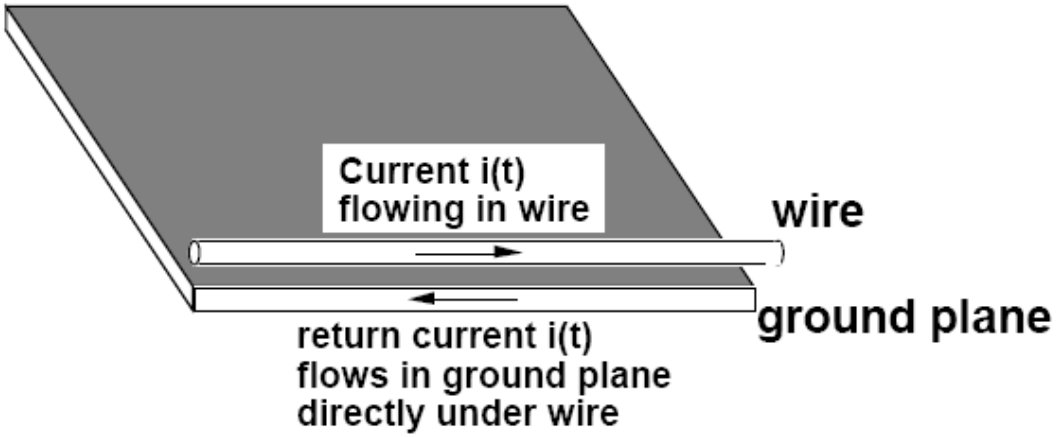


High frequency components of gate drive current are confined to a small loop

A dc component of current is still drawn output of 15V supply, and flows past the control chips. Hence, return conductor size must be sufficiently large

EMI CONSIDERATIONS

About ground planes



Inductance of return connections is minimized

Hence ground planes tend to exhibit lower impedance ground connections, and more nearly equipotential ground references

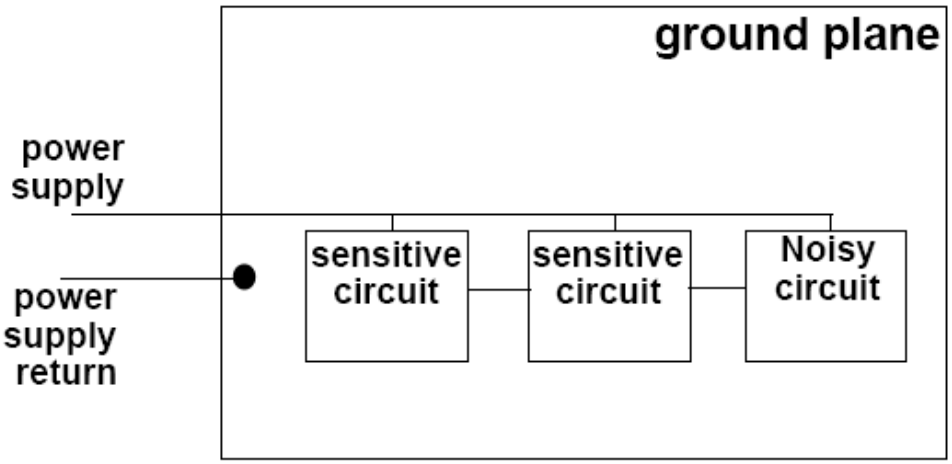
Ground planes are especially effective in the analog control portions of switching regulator circuits

But it is still possible to observe significant coupling of noise in ground, by

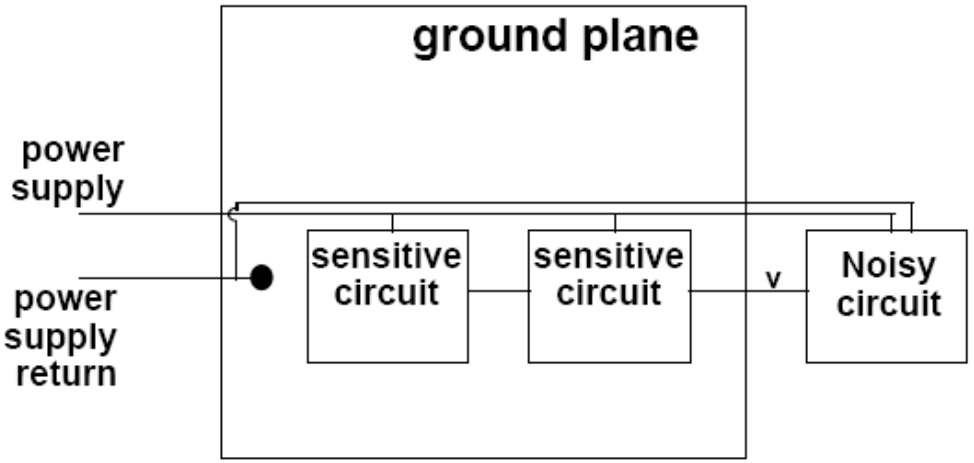
- poor layout of ground plane, or
- high resistance of ground plane

EMI CONSIDERATIONS

A poor ground plane layout



Return current of noisy circuit runs underneath sensitive circuits, and can still corrupt their ground references



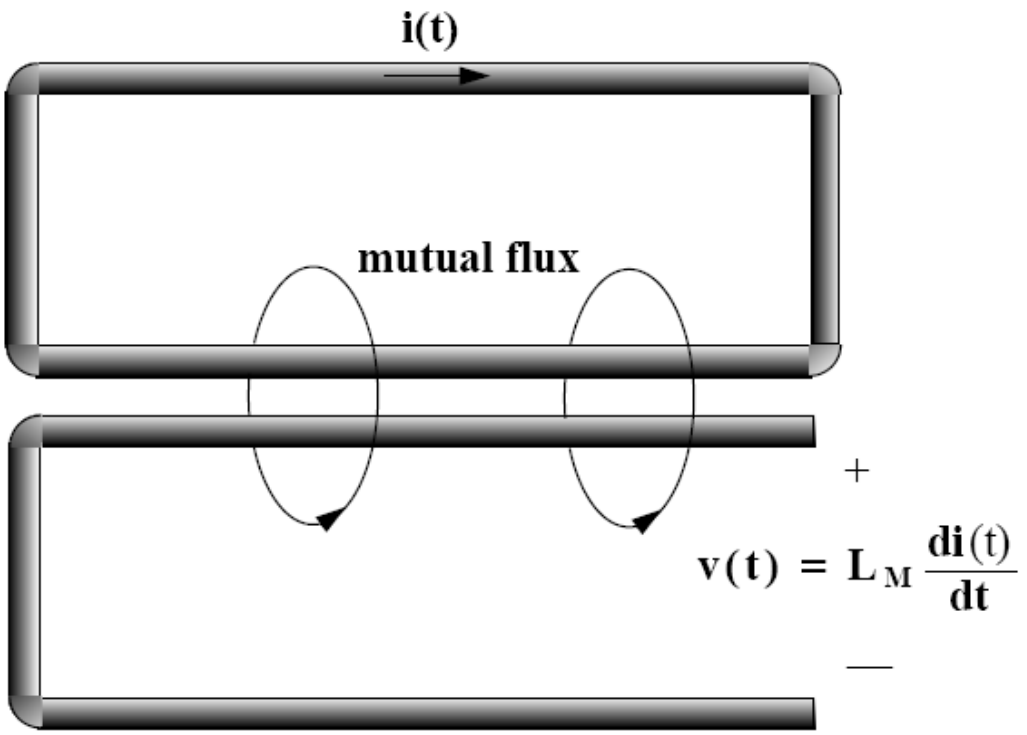
A solution is to remove the noisy circuit from the ground plane. One could then run a separate ground wire for the noisy circuit. The only drawback is that noise can be coupled into the input signal v.

EMI CONSIDERATIONS

Coupling of signals via magnetic fields

Loop containing ac current i(t) generates B field

which links another conductor, inducing an unwanted voltage v(t)



This phenomenon can sometimes be a problem when ground loops are present. Circulating ground currents are then induced, which lead to variations in the ground reference potential

EMI CONSIDERATIONS

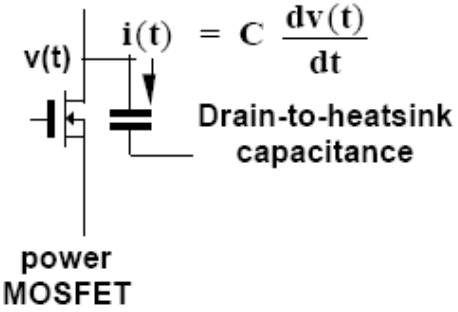
Stray capacitances

Most significant at high voltage points in circuit

Two major sources of EMI:

- Transformer interwinding capacitance
- MOSFET drain-to-heatsink capacitance

Drain-to-heatsink capacitance



When the switched drain voltage is applied to this capacitance, current spikes must flow.

The currents must flow in a closed path (a loop). What is the loop in your circuit?

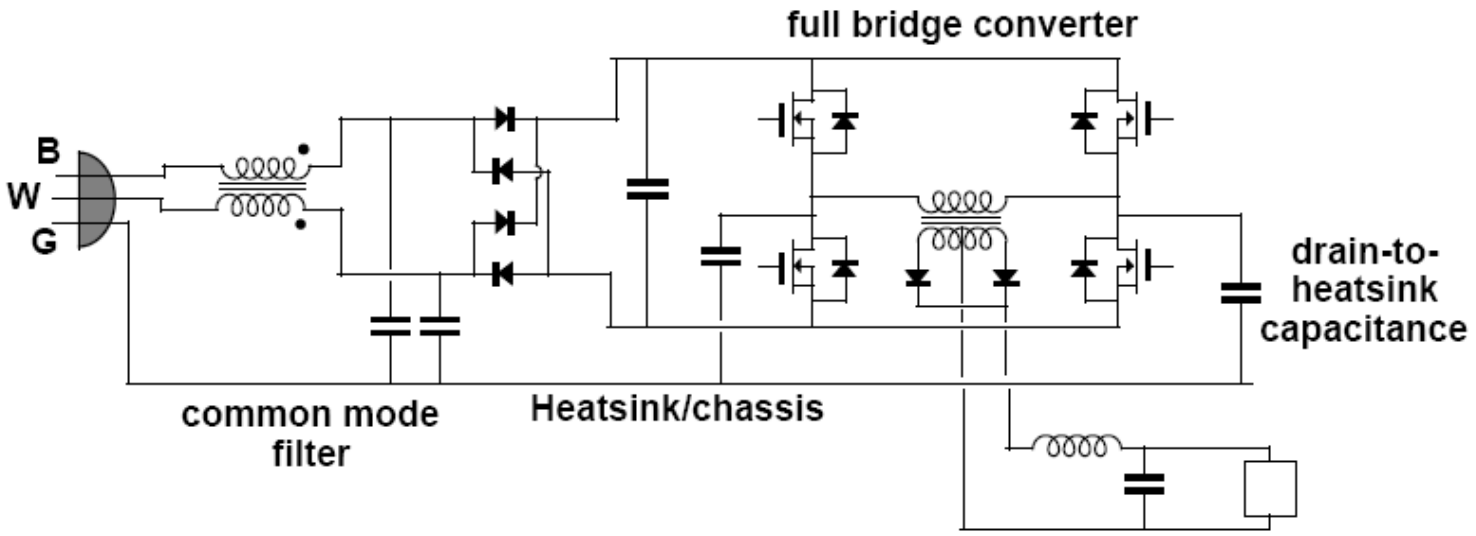
To control the effects of these currents,

- provide a short path for them to return to their origin
- add common-mode filters
- slow down switching times

EMI CONSIDERATIONS

Common mode noise generation

by drain-to-heatsink capacitance

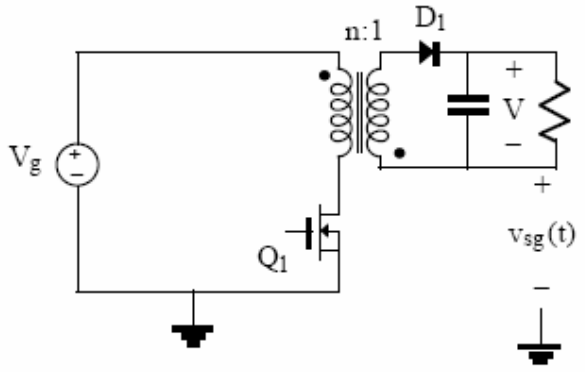


EMI CONSIDERATIONS

Common mode noise generation

by transformer interwinding capacitance

Flyback converter example

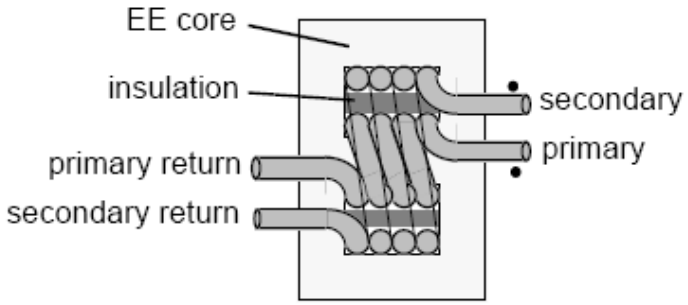


Transformer interwinding capacitance causes currents to flow between the isolated (primary and secondary) sides of the transformer, and can cause the secondary-side ground voltage to switch at high frequency: $v_{sg}(t)$ contains a high-frequency component.

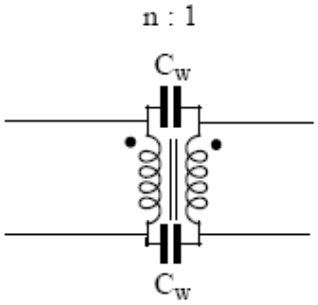
EMI CONSIDERATIONS

Modeling transformer interwinding capacitance

Suppose the transformer is wound as follows:

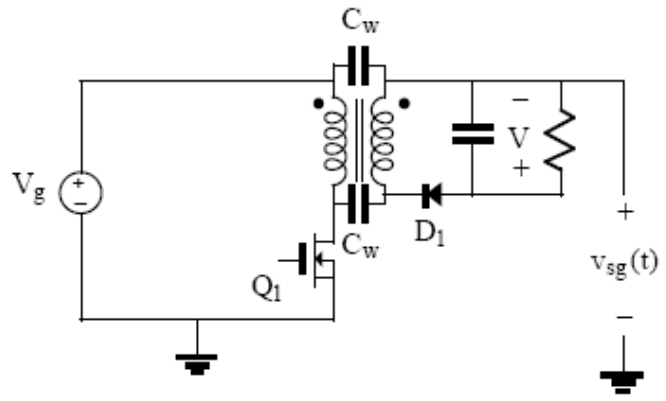


A simple lumped element model, including interwinding capacitance:



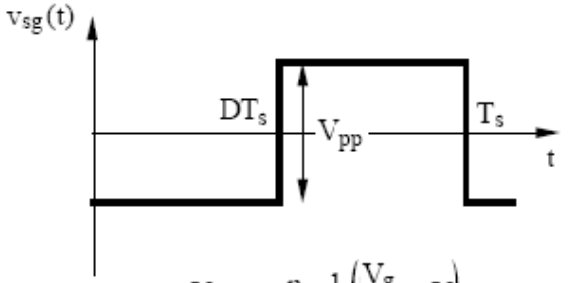
EMI CONSIDERATIONS

Flyback converter ground potentials



Flyback converter circuit, with interwinding capacitance modeled

One can solve the circuit to find the high-frequency ac component of $v_{sg}(t)$. The result is



$$V_{pp} = \frac{n-1}{2}\left(\frac{V_g}{n} + V\right)$$

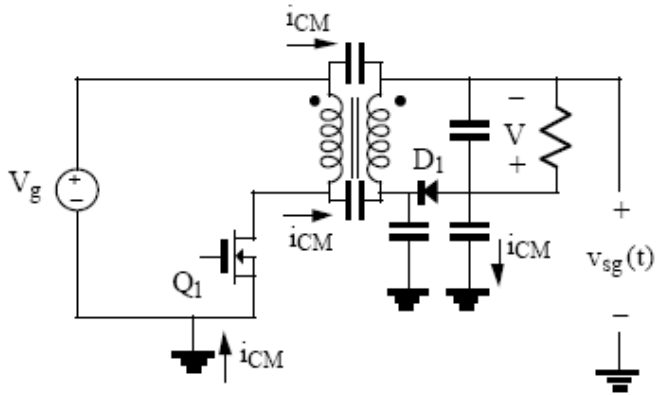
The secondary ground potential switches at high frequency with respect to the primary ground.

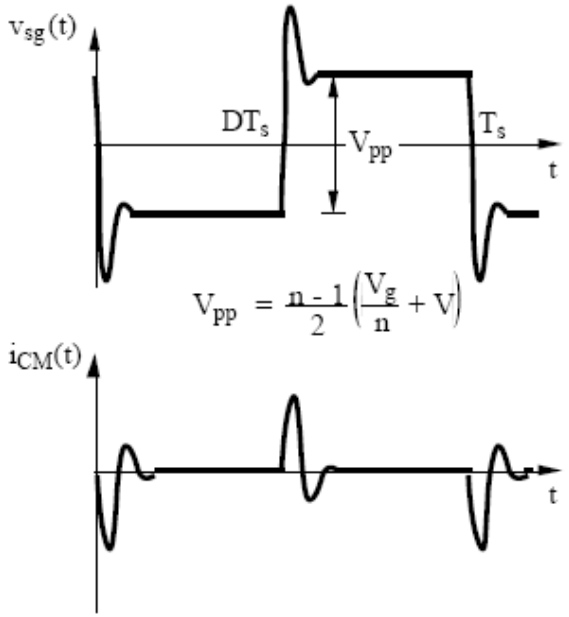
The peak-peak voltage V_{pp} is typically approximately equal to V_g. $v_{sg}(t)$ can also have a dc component, not predicted by the circuit model.

EMI CONSIDERATIONS

Secondary-side stray capacitances now lead to common-mode currents

Example: diode case-to-heatsink capacitance





These currents usually corrupt the ground reference voltage

EMI CONSIDERATIONS

Discussion

- Transformers can successfully provide dc and low-frequency ac isolation
- Transformer interwinding capacitances couple the primary and secondary voltages, greatly reducing the high-frequency ac isolation and leading to common-mode currents and conducted EMI

Some possible solutions:

- Redesign the transformer to reduce the interwinding capacitance. This usually leads to increased leakage inductance
- Add common-mode filters:

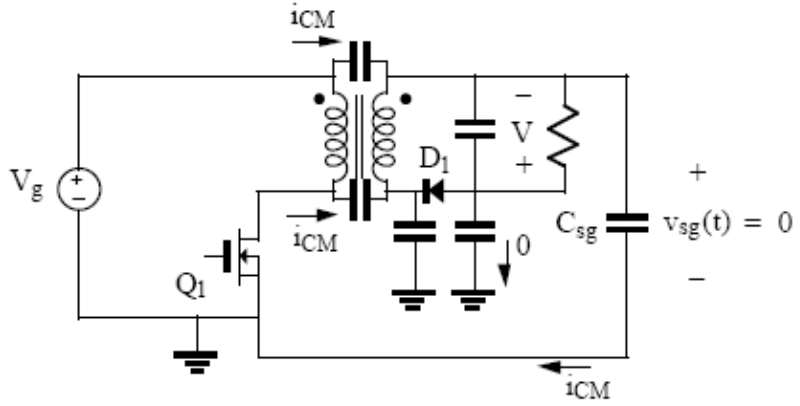
  Capacitors which connect the primary- and secondary-side grounds

  Common-mode filter inductors

  This greatly reduces conducted EMI, and can also reduce radiated EMI. But the capacitors do not allow the secondary ground potential to switch at high frequency.

EMI CONSIDERATIONS

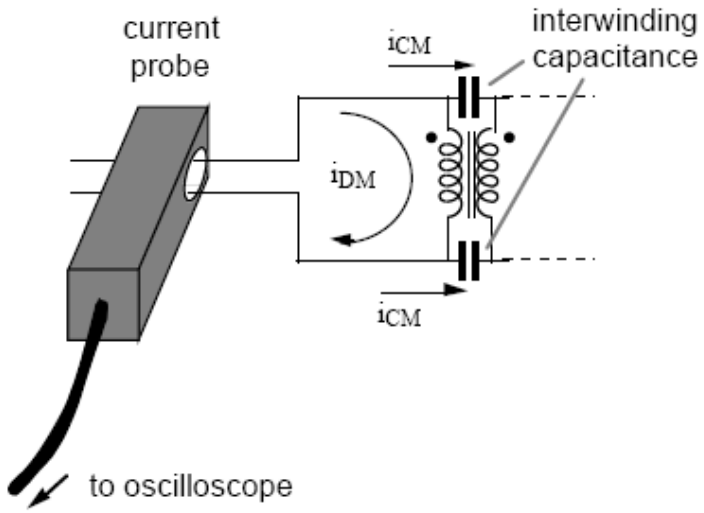
Addition of capacitance between primary and secondary grounds



Capacitor C_{sg} is much larger than the stray capacitances, and so nearly all of the common-mode current flows through C_{sg}. If C_{sg} is sufficiently large, then it will have negligible voltage ripple, and $v_{sg}(t)$ will no longer contain a high-frequency component.

EMI CONSIDERATIONS

Measurement of common mode current

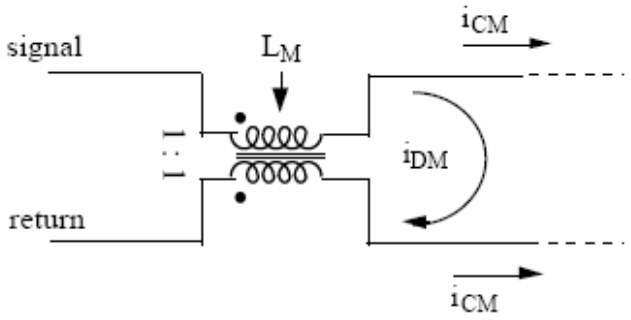


The common mode current due to transformer interwinding capacitance can be easily measured using a current probe

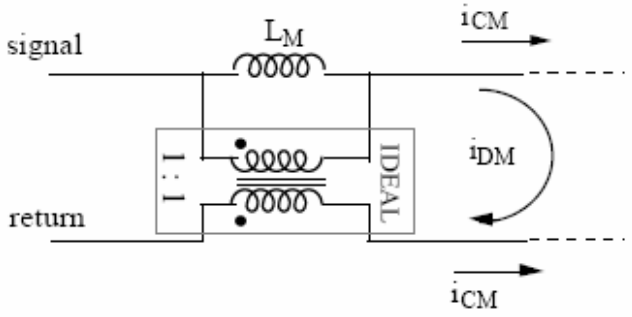
The differential-mode current $i_{DM}(t)$ cancels out, and the oscilloscope will display $2i_{CM}(t)$.

EMI CONSIDERATIONS

A Common-Mode Choke



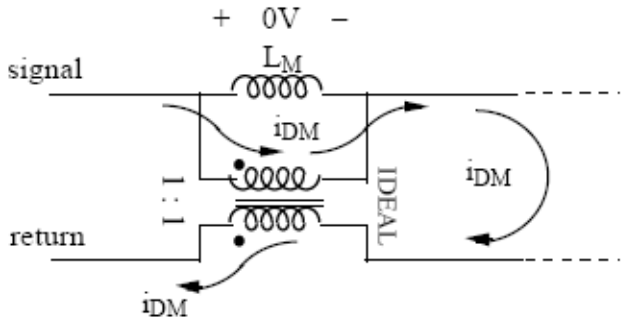
Equivalent circuit, including magnetizing inductance:



EMI CONSIDERATIONS

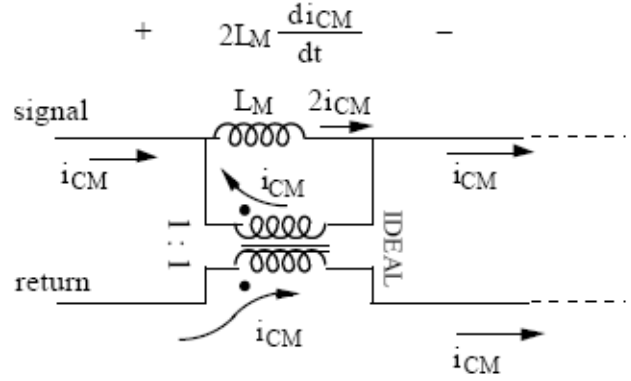
Operation of Common-Mode Choke

Differential mode



i_{DM} cancels out in windings, with no net magnetization of core. To the extent that the leakage inductance can be neglected, the common-mode choke has no effect on the differential-mode currents.

Common mode

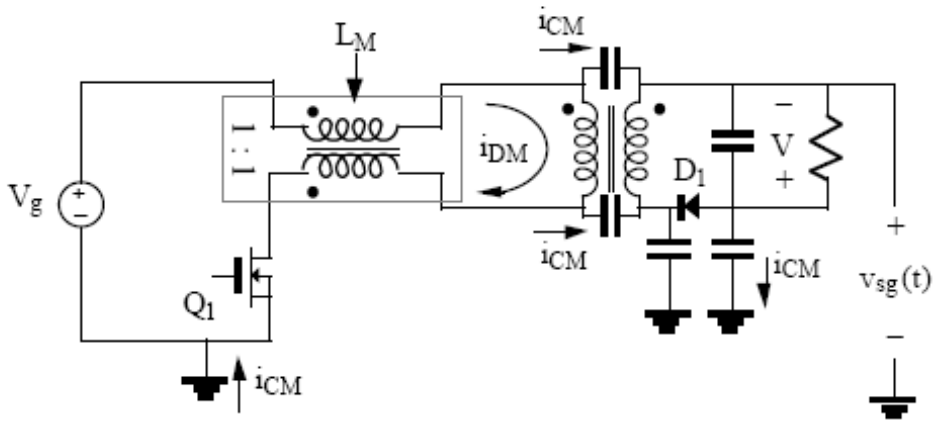


The common-mode currents effectively add, magnetizing the core. The common-mode choke presents inductance L_M to filter these currents.

EMI CONSIDERATIONS

Use of a common-mode choke

to reduce the magnitude of currents
in transformer interwinding capacitances

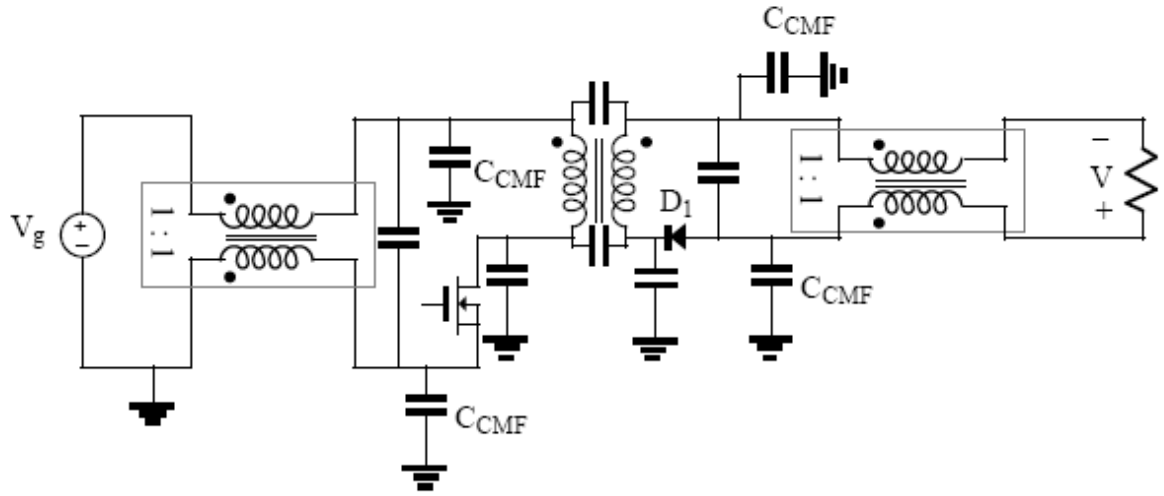


Common-mode choke inserts inductance L_M to oppose flow of high-frequency common-mode currents

EMI CONSIDERATIONS

Use of common-mode chokes

to filter the power supply input and output



The common-mode chokes, along with the capacitors C_{CMF}, form two-pole low pass filters which oppose the flow of high-frequency common-mode currents

EMI CONSIDERATIONS

Summary

EMI ("Noise") is caused by the violation of idealizing assumptions:
- Imperfect conductors
- Corruption of zero-potential ground reference
- Stray capacitances

Inductance of wires
- Keep areas of high frequency loops as small as possible

Coupling of signals via impedance of ground connections
- Steer ground currents away from sensitive circuits
- Examples: power return, gate drive return, coupling of signals from one stage to the next
- Use ground planes in sensitive analog portions of system

Coupling of signals via magnetic fields
- Ground loops and circulating ground currents
- Example: audiosusceptibility measurement

EMI CONSIDERATIONS

Coupling of signals via electric fields
- Stray capacitances
- Example: drain-to-heatsink capacitance
- Example: transformer interwinding capacitances

Common mode noise
- Usually caused by stray capacitances
- Can be filtered using common-mode chokes and common-mode filter capacitors

It is possible to figure out where the EMI is being generated, and to engineer the circuit to mitigate its effects

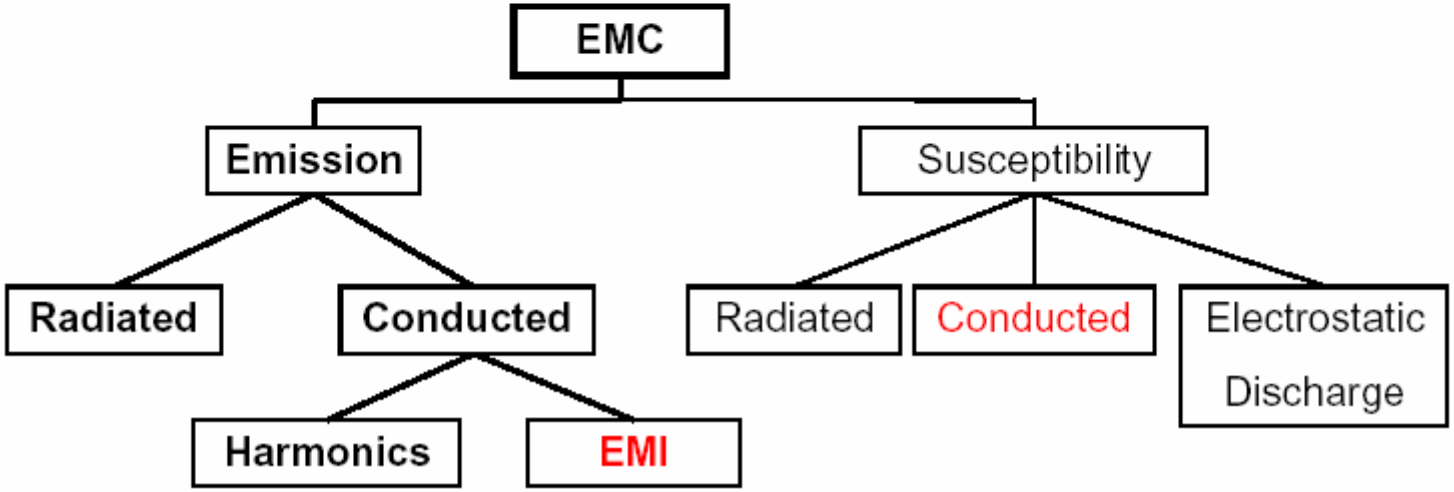
EMC CONSIDERATIONS

Electromagnetic Compatibility

Ability of the device (e.g. power supply) to:

function satisfactorily in its electromagnetic environment (susceptibility or immunity aspect)

without introducing intolerable electromagnetic disturbances (**emission** aspect)



EMC CONSIDERATIONS

7.2. EMC Testing Standards

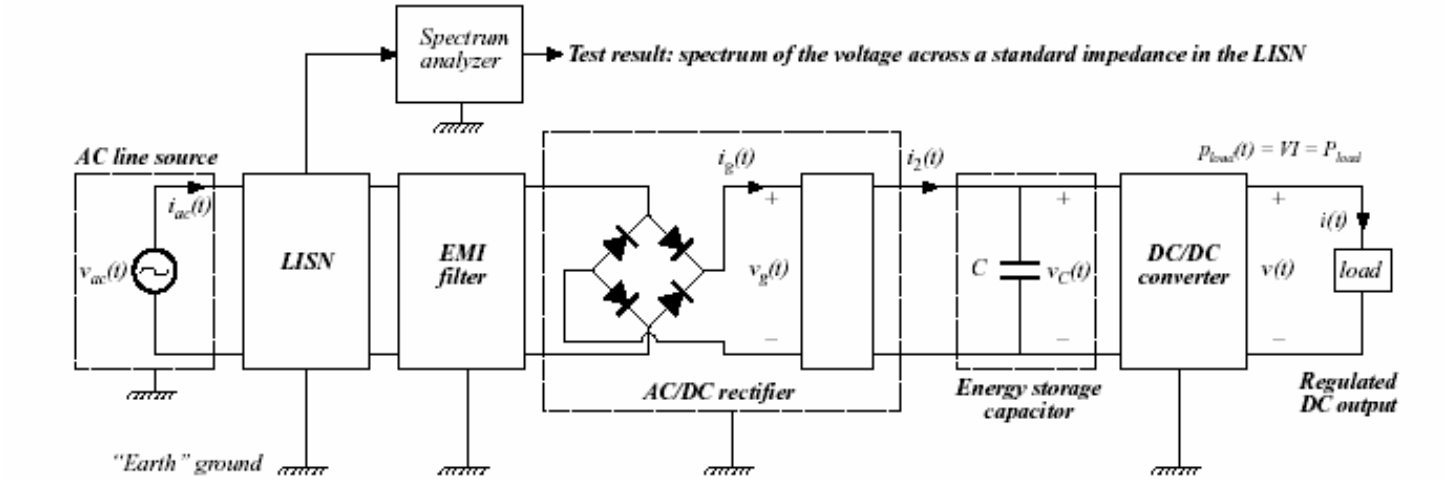
SMPSs and electrical devices containing SELCs are required to be in conformance with the EMC Directive 89/336/EEC and the implementing UK regulations SI 2372 1992. Therefore EMC testing is required and the following tests were applied to the SMPSs and SELCs purchased for this project:

- Harmonic Emission Testing (EN61000-3-2:2000 [11])
- Conducted Emission Testing (EN55022:1998 [2])
- Radiated Magnetic Field Emission Testing (EN55011:1998 [12] and EN55015:2001 [13])
- Radiated Electric Field Emission Testing (EN55022:1998 [2]).

The conducted emission measurements were performed in accordance with EN55022 Class B [2] (0.15MHz to 30 MHz) with additional measurements being performed between 9kHz and 150kHz for this project

EMC CONSIDERATIONS

Conducted EMI



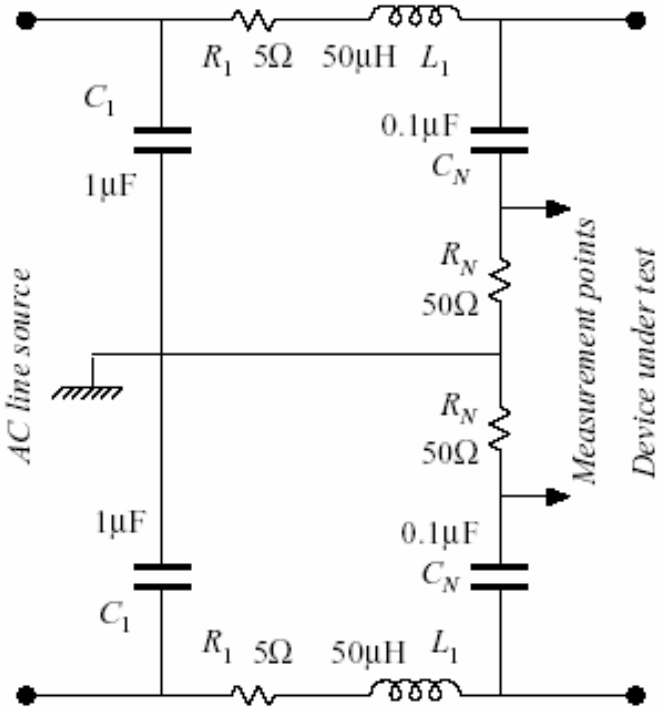
Sample of EMC regulations that include limits on radio-frequency emissions:

European Community Directive on EMC: Euro-Norm EN 55022 or 55081, earlier known as CISPR 22

National standards: VDE (German), FCC (US)

EMC CONSIDERATIONS

LISN

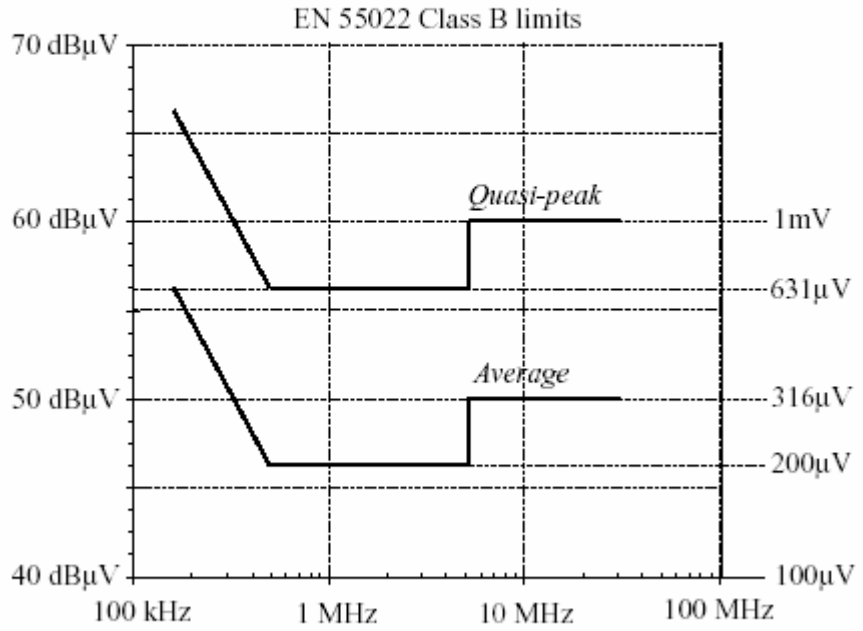


LISN example

- **LISN:** "Line Impedance Stabilization Network," or "artificial mains network"
- **Purpose:** to standardize impedance of the power source used to supply the device under test
- Spectrum of conducted emissions is measured across the standard impedance (50Ω above 150kHz)

EMC CONSIDERATIONS

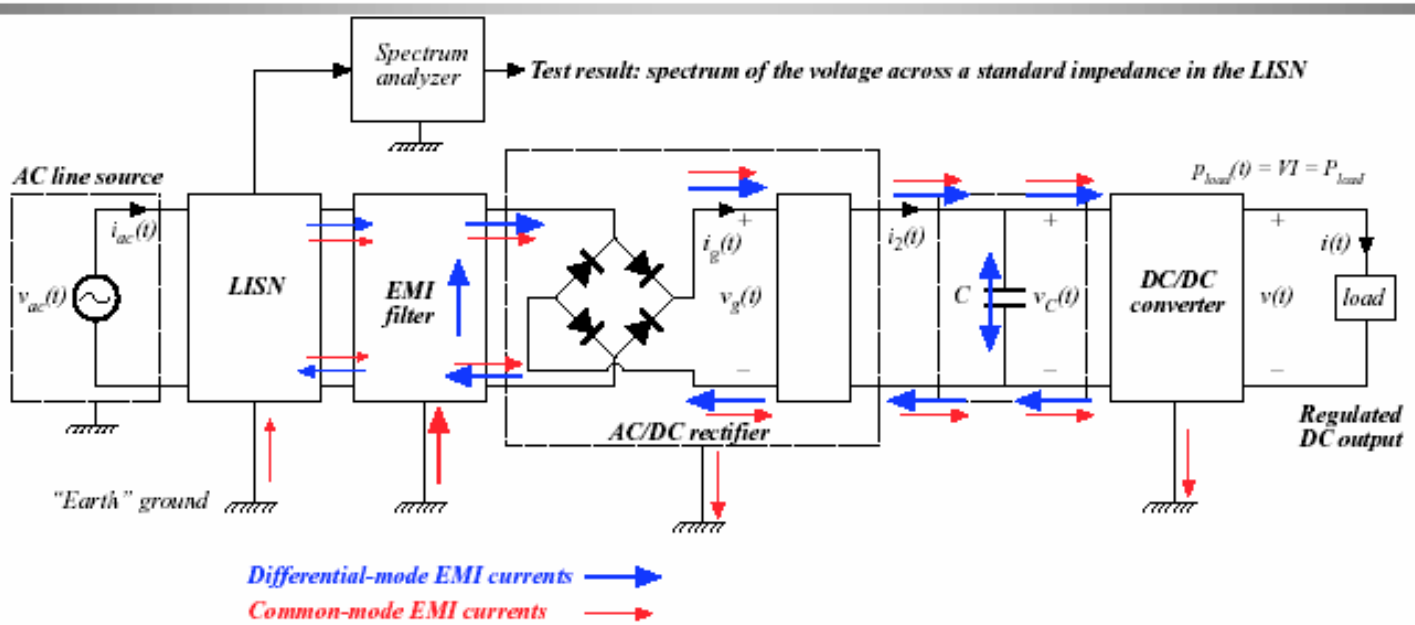
An Example of EMI Limits



- Frequency range: 150kHz-30MHz
- Class B: residential environment
- Quasi-peak/Average: two different setups of the measurement device (such as narrow-band voltmeter or spectrum analyzer)
- Measurement bandwidth: 9kHz

EMC CONSIDERATIONS

Differential and Common-Mode EMI



- **Differential mode EMI**: input current waveform of the PFC. Differential-mode noise depends on the PFC realization and circuit parameters.
- **Common-mode EMI**: currents through parasitic capacitances between high *dv/dt* points and earth ground (such as from transistor drain to transistor heat sink). Common-mode noise depends on: *dv/dt*, circuit and mechanical layout.

EMC CONSIDERATIONS

7.4. PCB Layout Considerations

In addition to basic design, and magnetics design, PCB layout is critical. Improper layout can adversely affect RFI radiation, component reliability, efficiency, and stability.

- All PCB traces exhibit inductance and resistance. These can cause high voltage transitions whenever there is a rate of change in current flowing through the trace.

- For traces that are too narrow for the current flowing through them, a voltage drop occurs from one end of trace to the other, which can be an antenna for RFI. In addition, capacitive coupling between adjacent traces can interfere with proper circuit operation.

EMC CONSIDERATIONS

PCB Layout Considerations

There are 2 rules of thumb for PCB layout: 'short and fat' for all power carrying traces, and 'one point grounding' for the various ground systems.

-Traces that are short and fat minimize the inductive and resistive aspects of the trace, thus reducing the noise within the circuits, and RFI.

- Single point grounding keeps the noise sources separated from the sensitive control circuits.

EMC CONSIDERATIONS

PCB Layout Considerations

Within all SMPS, there are four major current loops:

- Two of the loops conduct high level ac currents: the power switch AC current loop, and the output rectifier ac current loop. The currents are typical trapezoidal current pulses with very high peaks, and very rapid di/dt s.

-The two other current loops are the input source and output load current loops, which carry low frequency current being supplied from the voltage source, and to the load, respectively.

EMC CONSIDERATIONS

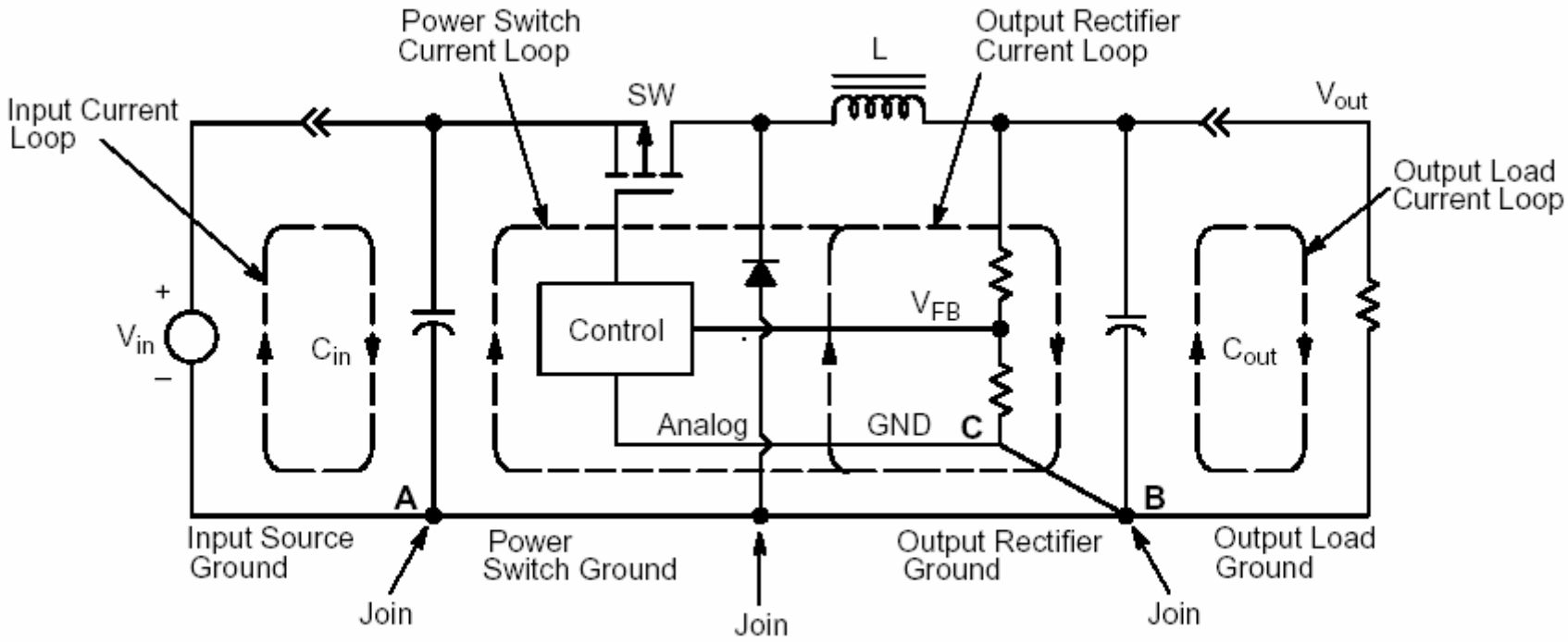
- For the power switch ac current loop, current flows from input filter capacitor through inductor or transformer winding, through the power switch back to negative pin of capacitor.

- Similarly, the output rectifier current loop's current flows from the inductor or sec. transformer winding through the rectifier to output filter capacitor, and back to the winding.

- Filter C's can source or sink large AC currents, these PCB traces should be made as wide and as short as possible, to minimize r,l's. These traces should be the first to be laid out.

EMC CONSIDERATIONS

The Current Loops and Grounds for the Major Converter Topologies



(a) The Non–Isolated DC/DC Converter

Fig.21

EMC CONSIDERATIONS

- Both input source and output load current loops must be connected directly to their respective filter C terminals, otherwise switching noise could bypass the filtering action of C, this is called conducted interference.

- These loops can be seen in Fig.21 for two major forms of SMPS (non-isolated, and isolated).

EMC CONSIDERATIONS

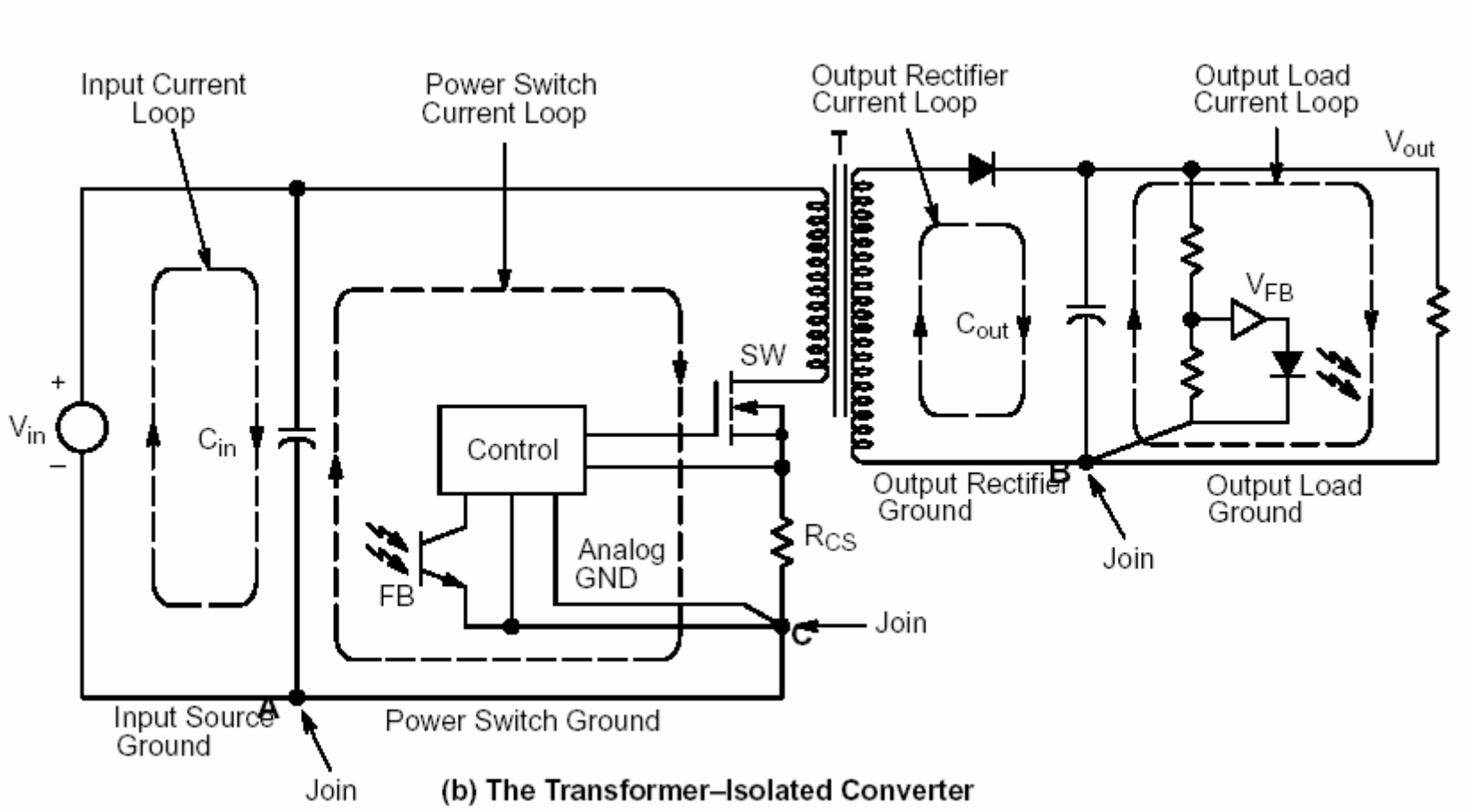


Fig.21

EMC CONSIDERATIONS

The grounds are extremely important for proper operation since they form the reference connections for the entire supply, each ground has its own set of signals which can adversely affect the supply operation, if connected improperly.

- There are five distinct grounds within a typical SMPS: 4 of them form the return paths for the above current loops, the remaining one is the low-level analog control ground.

- The grounds which are part of major current loops must be connected as shown in Fig.21. Here again, the connecting point between high level AC grounds and input or output grounds is at the negative terminal of the appropriate filter capacitor (pts A and B in Figs.21 a and b).

EMC CONSIDERATIONS

- Noise on the AC grounds can very easily escape into the environment if the grounds ar not directly connected to the negative terminal of filter capacitors.

- The analog ground must be connected to the point where the control IC must measure key power parameters such as AC or DC current and the output voltage (pt. C in Fig.21). Here any noise introduced by large AC signals within the AC grounds will sum directly onto the low-level control parameters, and affect the operation of the supply.

- The last important factor in PCB design is the layout surrounding the AC voltage nodes (drain of power Mosfet, and anodes of output rectifiers). These nodes can capacitively couple into any trace on different layers of the PCB that run under the AC pad.

EMC CONSIDERATIONS

- Many times, it is necessary to parallel filter capacitors to reduce the amount of rms ripple current of each capacitor. Close attention should be paid to the layout. If paralleled capacitors are in a line, C closest to the source of ripple current will operate hotter than the others, shortening its operating life.

- To ensure even sharing of ripple currrent, any paralleled C should be laid out in a radially symmetric manner around the current source (typically a rectifier or power switch)

EMC CONSIDERATIONS

PCB LAYOUT

BASIC PRINTED CIRCUIT BOARD DESIGN GUIDELINES FOR SMPS SWITCHING POWER SUPPLIES

1. Keep PCB creepage and clearance between primary circuits, secondary circuits and safety ground according to the requirements of applicable standards. For example, in a typical commercial application with 120-230 VAC input, creepage between primary and secondary circuitry per UL 60950 or IEC 60950 should be 6.4 mm min.

2. High frequency pcb design requires carefull grounding. Use ground plane for control circuit. Try to make most of control ground connections through vias to this ground plane rather then through PC traces.

3. For each power supply stage, keep power ground and control ground separately. If they are electrically connected, connect them in only point near DC output of this stage.

4. Minimize areas and lengths of loops which contain high frequency switching currents.

5. Locate capacitors that bypass supply voltage and reference pins of all ICs close to these pins.

6. Place filter capacitors so that their terminals physically go right into the PWB traces that carry mainstream of the current to be filtered.

7. Use symmetrical routing for paralleled power devices.

8. Choose the width of PCB traces based on the abnormal current (such as short circuit current) that could develop in the circuit, rather then on rated current.