Hacettepe University
Electrical and Electronics Engineering Department

ELE 789
Special Topics in Electrical and Electronics Engineering

Lecture Notes

Chapter IV

Instructor: Dr. Işık Çadırcı

IV. CONTROL METHODS IN SMPS

4.0. Introduction - Testing the Power Supply Units

4.1. Voltage Mode Control

4.2. Current Mode Control

Peak Current Mode Control, Average Current Mode Control

4.3. Closing the feedback loop – Stability

4.4. Examples

IV. CONTROL METHODS IN SMPS

OBJECTIVES OF FEEDBACK CONTROL

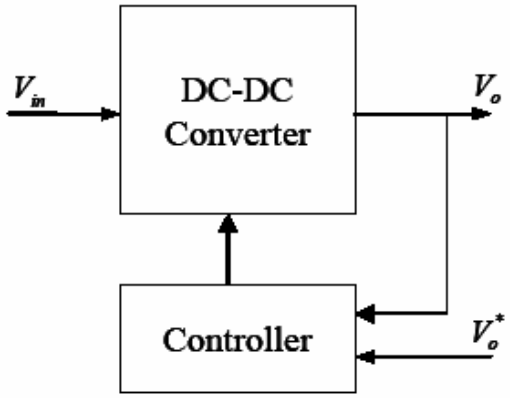


Figure 4-1 Regulated dc power supply.

- zero steady state error
- fast response
- low overshoot
- low noise susceptibility.

IV. CONTROL METHODS IN SMPS

4.0. Testing Power Supply Units:

Does the SMPS meet the design specs? The power supply industry has evolved a set of tests and parameters that form the basis of SMPS technical specs:

- *Line Regulation*
- *Load Regulation*
- *Dynamic Load Response*
- *Dielectric Withstand Voltage*
- *Hold Up Time*
- *Over current Limit Tests*

IV. CONTROL METHODS IN SMPS

Line Regulation: *The amount of change in the output voltage in response to a change in the input voltage. The test is conducted with the power supply delivering its rated output power. The output voltage is measured at three input voltage levels: minimum, nominal, and maximum specified input voltages.*

$$\text{Line Regulation} = \frac{V_{out(high)} - V_{out(low)}}{V_{out(nominal)}} \times 100\ \%$$

Steady-State Load Regulation: *The change in the steady-state output voltage in response to a change in the mean load current for each output. The set is conducted at the nominal input voltage. Output voltage is then measured usually at 10% of rated load, and at rated load.*

IV. CONTROL METHODS IN SMPS

$$\text{Load Regulation} = \frac{V_{out(high)} - V_{out(low)}}{V_{out(nominal)}} \times 100\ \%$$

Dynamic Load Response: This parameter basically tests for the time it takes for the regulation feedback loop to react to a step change in the output load current and return the output to the specified steady-state voltage. This is one parameter that is worse than the linear regulator. Usually it takes four or more switching cycles to replace the energy taken from the output storage elements and to provide the increased or decreased amount of energy needed by the load at its new load current. The response time and the shape of the response gives the designer an indication of the error amplifier's DC gain and the frequency compensation.

IV. CONTROL METHODS IN SMPS

Dynamic load response time:

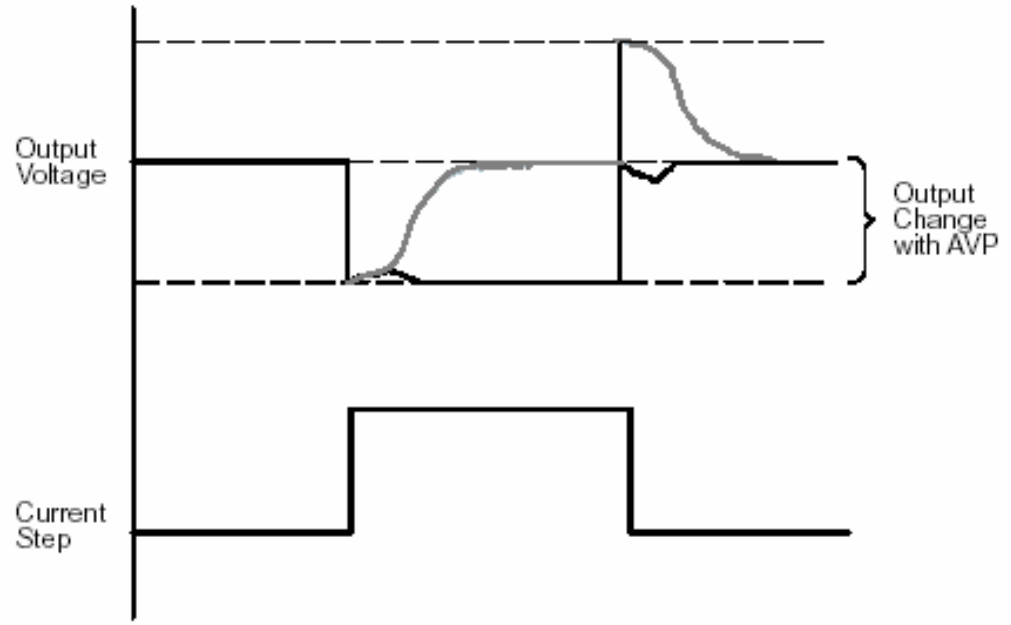
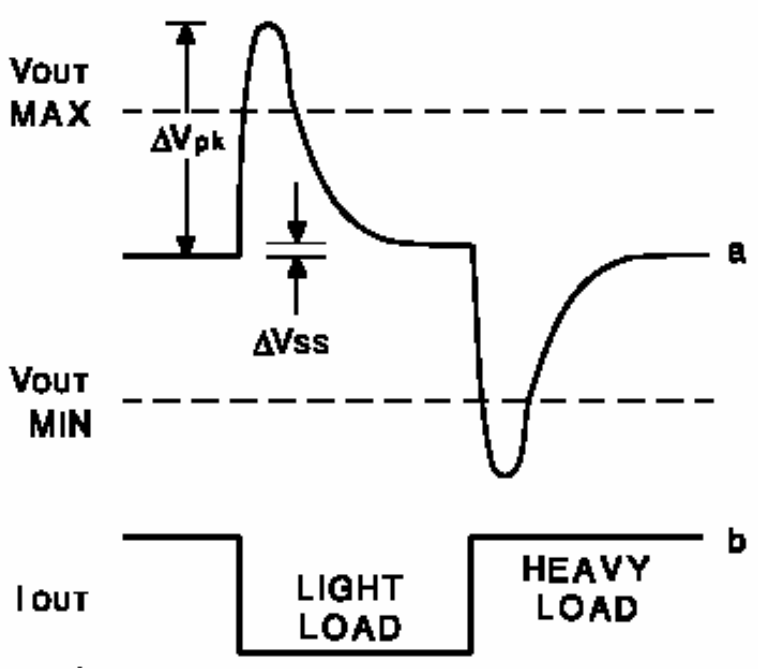


Figure 1. Output Change for Change in Output Current

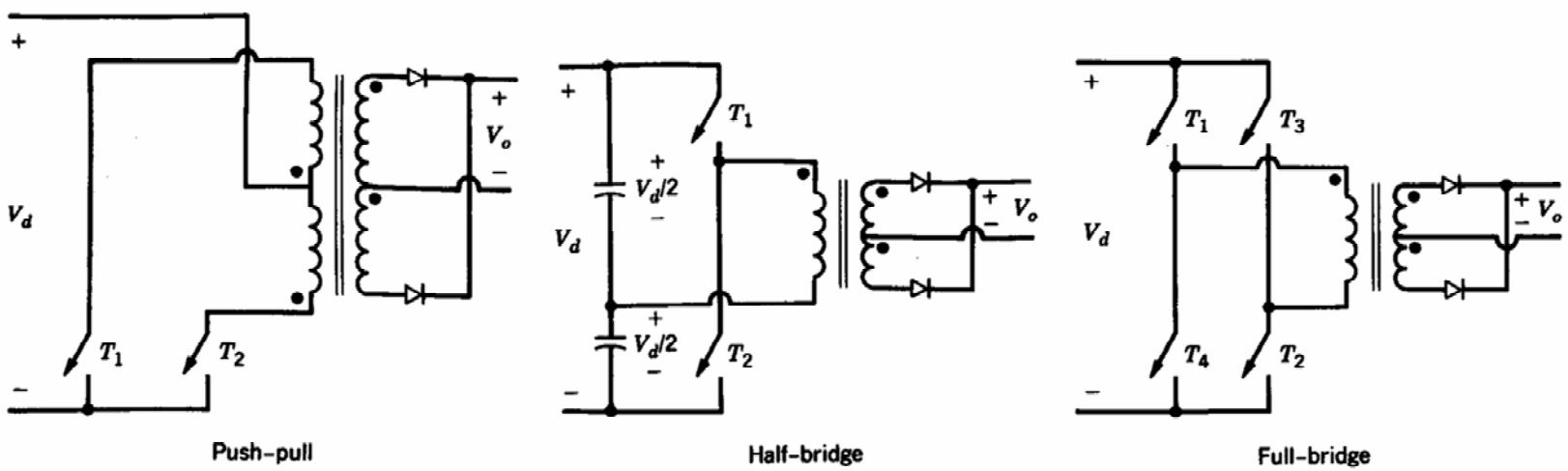


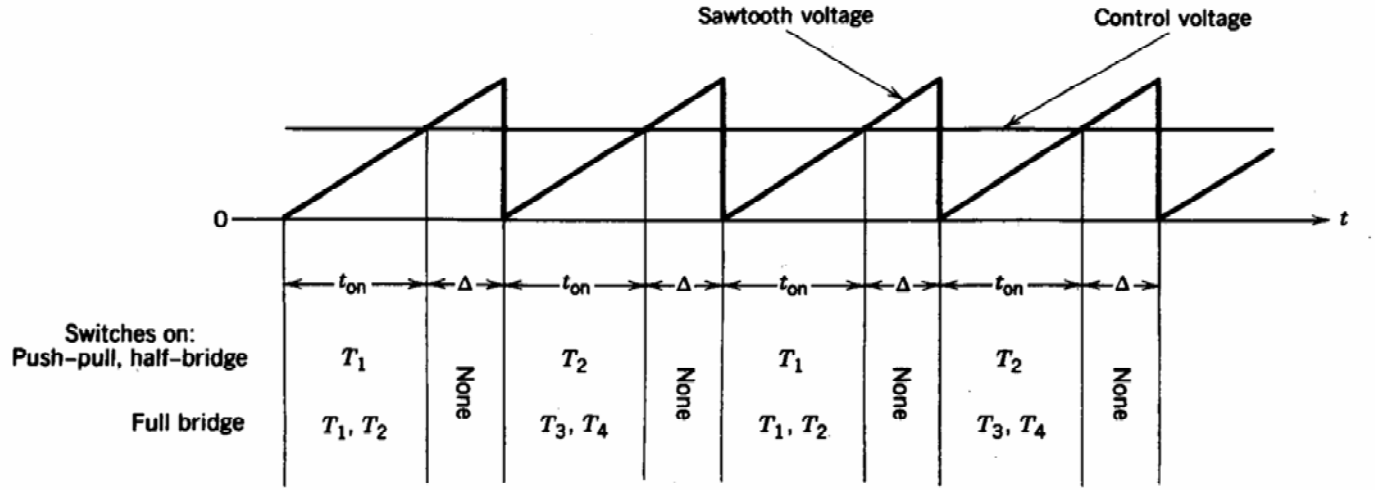
IV. CONTROL METHODS IN SMPS

Dielectric Withstand Voltage: *A test that checks whether the dielectric isolation between the input, chassis, and output(s) exceeds a specified minimum voltage. The overall purpose of this test is to ensure that there is no possibility that potentially lethal voltages from the input line or within the product can reach the end user of the equipment. The test failure is determined by exceeding a specified current limit during the period when the test voltage is applied to the unit.*

Hold-Up Time: *The length of time that the output can provide rated power after removal of the input power. The requirements of this test dictate the amount of energy that has to be stored in the input filter – storage capacitor within the SMPS.*

IV. CONTROL METHODS IN SMPS





PWM Scheme used in dc–dc converters, where the converter output is rectified to produce a dc output.

IV. CONTROL METHODS IN SMPS

There are basically the single-loop and the multi-loop control methods in SMPS: **Voltage mode control and current mode control**

4.1. Voltage mode control

Single-loop control is commonly called the 'voltage mode control'. This is the traditional method where only the output voltage is sensed and compared to the reference in order to control the duty cycle of the power switches.

Voltage mode control provides adequate control for the SMPS but can introduce problems in its dynamic load response time and line regulation. The controller compares the error with the ramp waveform created by the oscillator to determine the PWM for the power switch. This performs quite well when loads are constant.

IV. CONTROL METHODS IN SMPS

VOLTAGE MODE CONTROL

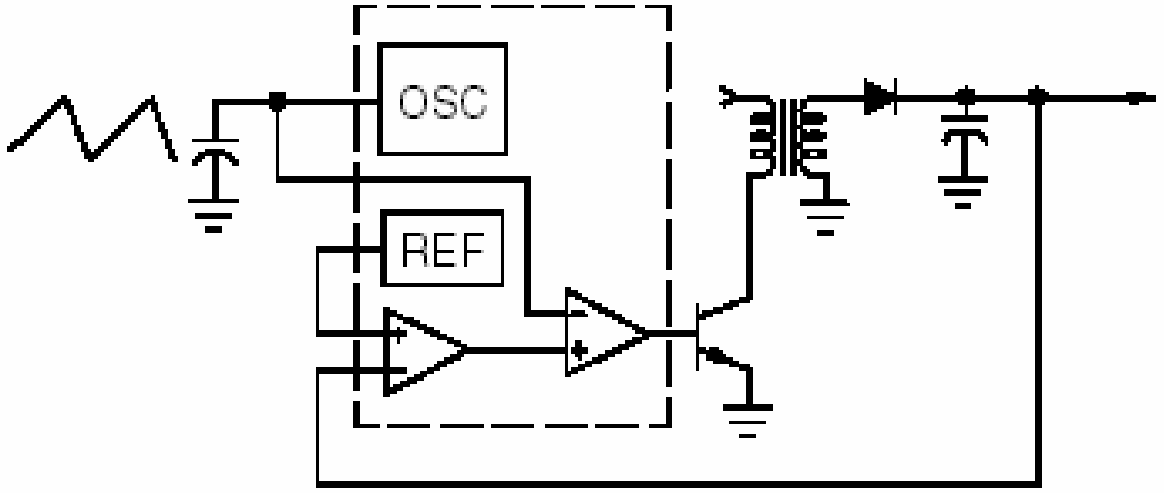
This was the approach used for the first switching regulator designs and served the industry well for many years
There is a single voltage feedback path, with pulse-width-modulation (PWM) performed by comparing the voltage error signal with a constant ramp waveform. Current limiting must be done separately.

The advantages of the voltage mode control are :

- **A single feedback loop is easier to design and analyse**
- **A large amplitude ramp waveform provides good noise margin**
- **A low impedance power output provides better cross regulation for multiple output power supplies**
- **Voltage mode's disadvantages can be listed as :**
- **Any change in line or load must first be sensed as an output change and the corrected by the feedback loop (slow response)**
- **Feedback compensation is further complicated by the fact that the loop gain varies with input voltage.**

IV. CONTROL METHODS IN SMPS

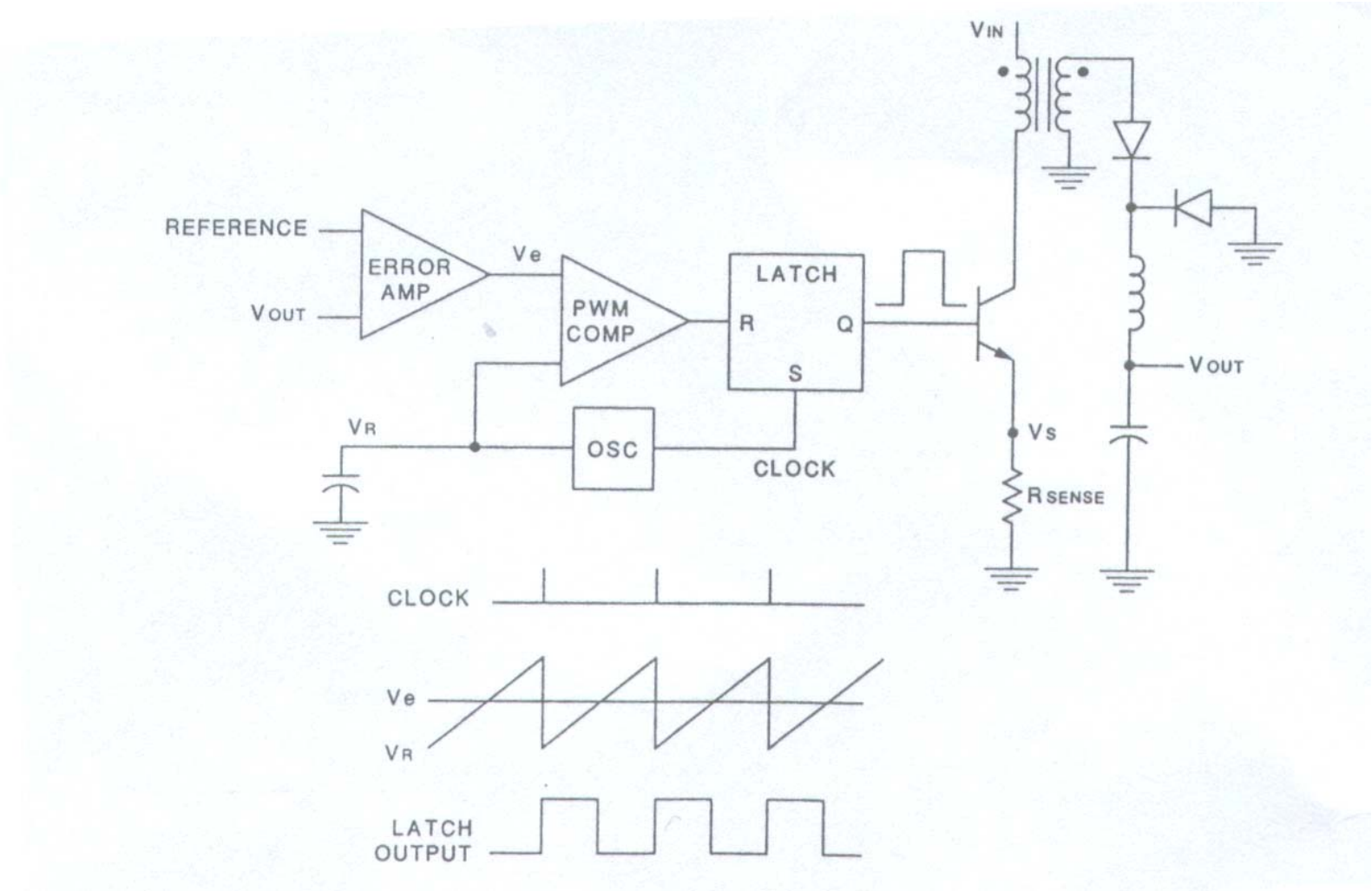
The PWM comparator converts the error voltage into a PWM waveform in order to drive the power switches in a pulsewidth modulated on/off fashion. The most common voltage mode control is a fixed frequency method of control:



Voltage mode control

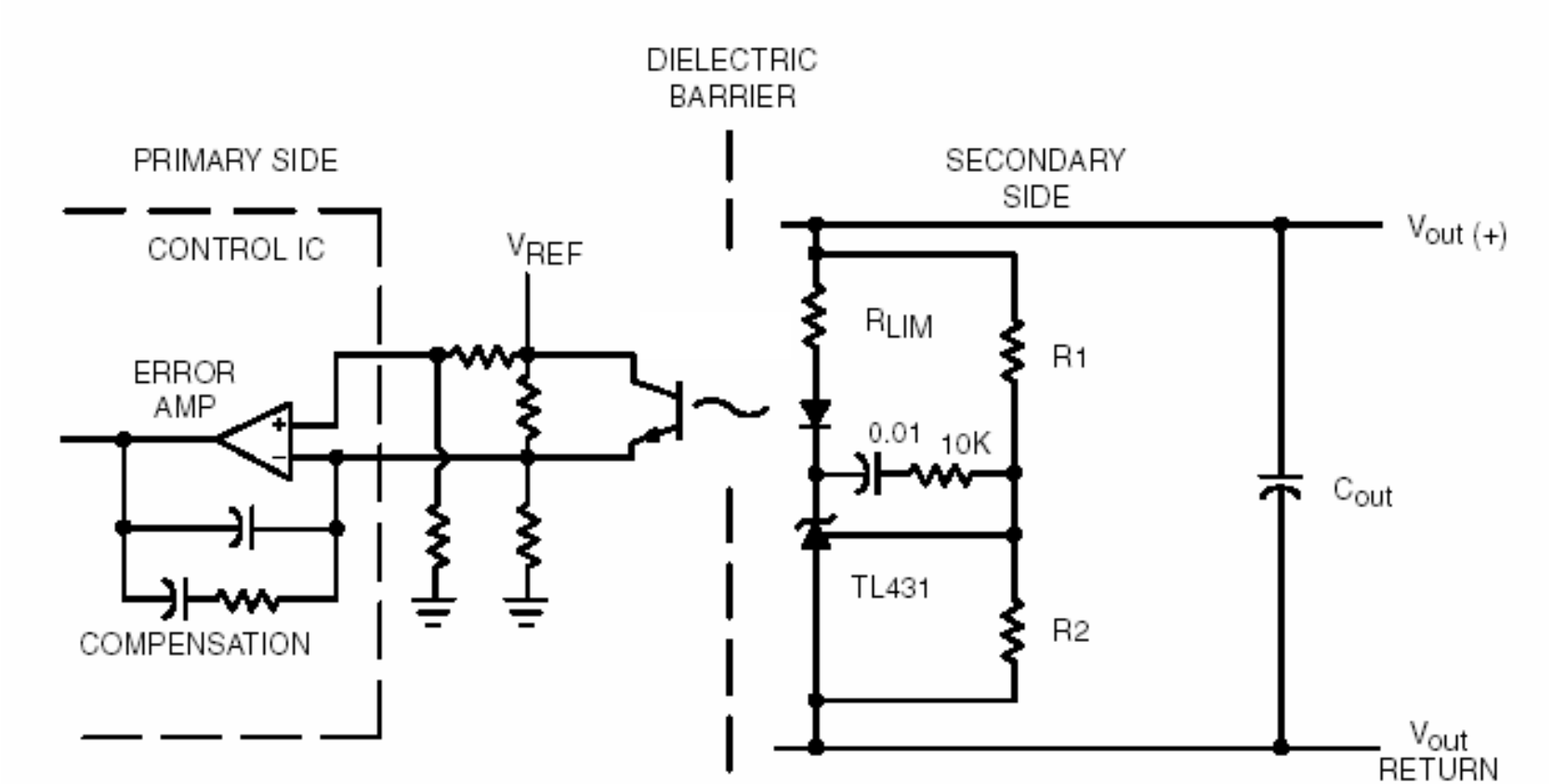
IV. CONTROL METHODS IN SMPS

Voltage Mode Control



IV. CONTROL METHODS IN SMPS

Control Methods: Opto-isolated voltage feedback for Off-line SMPS



IV. CONTROL METHODS IN SMPS

In this method, only the output voltage is sensed at the rear of the supply. If the load or the line changes quickly, the magnetic elements and filters provide a severe time delay before the overall supply can respond to these changes. For this reason, multiloop control was invented.

4.2. Current Mode Control:

Current mode control now adds a second control loop to the voltage feedback loop. In place of the ramp from the oscillator, as in voltage mode control, the current ramp from the magnetic elements is used for the error voltage-to-PWM process. The oscillator now only serves to fix the frequency of operation. The level of error voltage dictates the maximum level of peak current allowed.

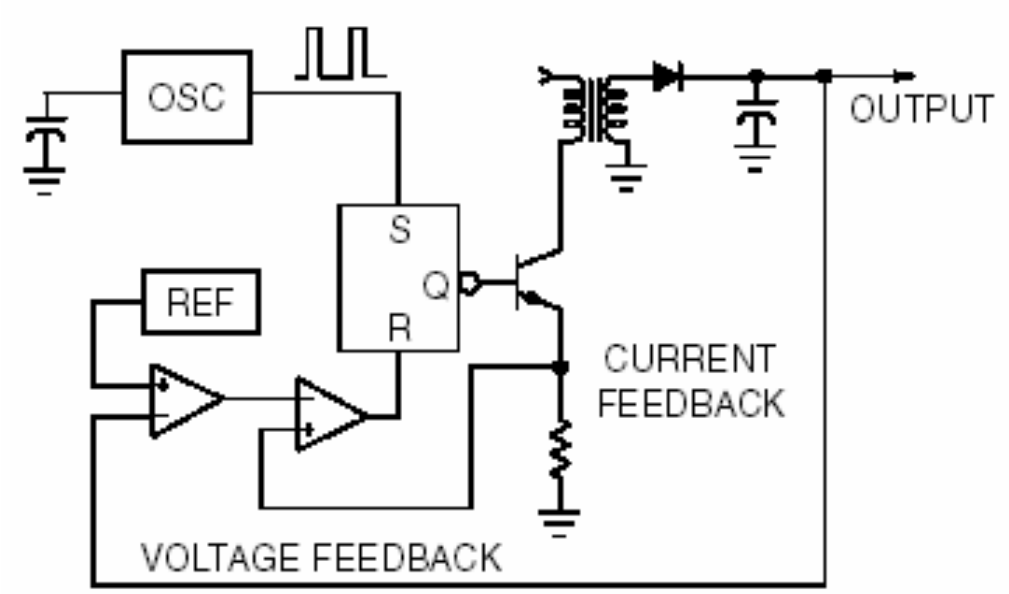
IV. CONTROL METHODS IN SMPS

If the input line changes, it is sensed immediately in the change in peak current within the magnetics, and output voltage is held constant. If the load changes, voltage error amplifier allows higher peak currents to enter the output filter. Also, the level of valley current I_{min} changes. This is immediately compensated for by the current feedback loop. So, the internal states of the magnetic portions of the supply are sensed and quickly compensated for.

One major problem with this method is that for duty cycles greater than 50%, the system becomes unstable. This can be corrected by 'slope compensation'. This requires two other signals to be summed into the feedback current ramp. The circuitry needed for slope compensation is not provided within the current mode controller IC, so it must be added externally.

IV. CONTROL METHODS IN SMPS

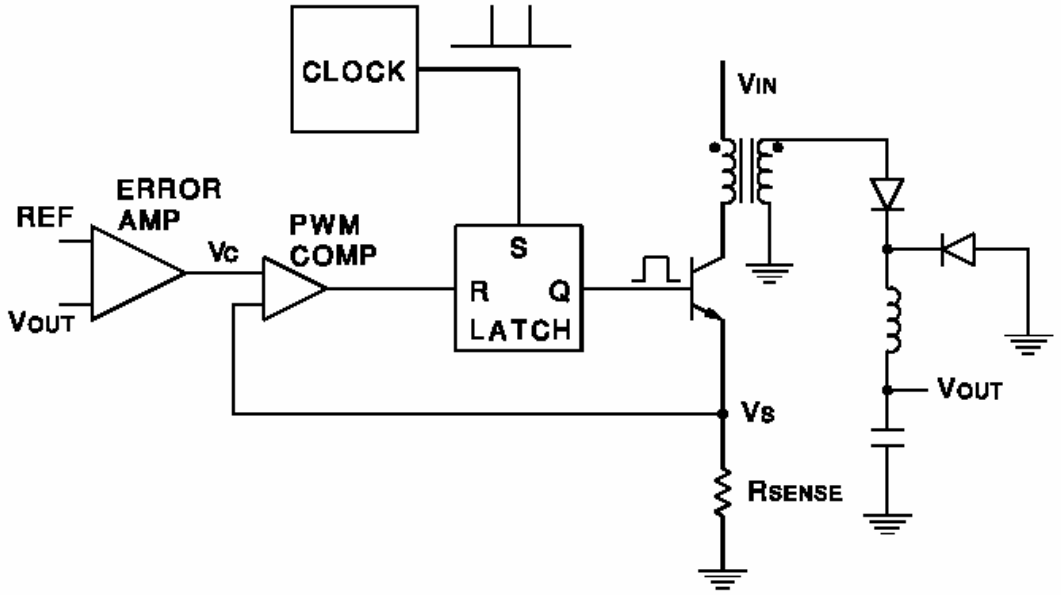
In current mode control, not only the output voltage, but also the amount of current that flows through the inductor or transformer are sensed. *Current mode controllers can be identified by the output of the error amplifier being placed into a comparator, where the level of the current ramp is sensed . The frequency of operation is determined by an oscillator whose only purpose is to start each 'on' cycle.*

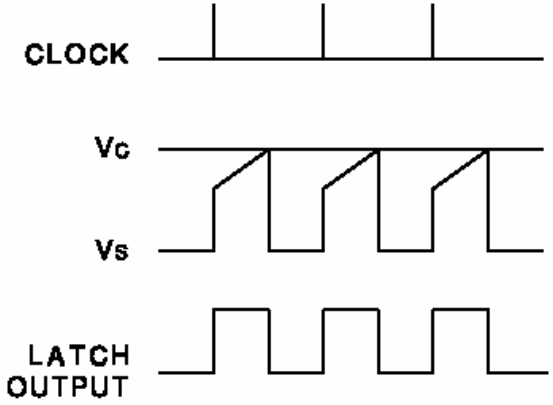


Current mode control

IV. CONTROL METHODS IN SMPS

Peak Current Mode Control





IV. CONTROL METHODS IN SMPS

CURRENT MODE CONTROL

- **Basic current mode control uses oscillator only as a fixed frequency clock**
- **The ramp waveform is replaced with a signal derived from output inductor/transformer current.**

The advantages of the current mode control are :

- **No delayed response to line voltage changes**
- **Simpler compensation and a higher gain bandwidth**
- **Inherent pulse by pulse current current limiting**
- **Some of the problems of the current mode control are :**
  2 feedback loops (circuit analysis more difficult)
- **The control loop becomes unstable at duty cycles above 50%**
  (slope compensation is required)

IV. CONTROL METHODS IN SMPS

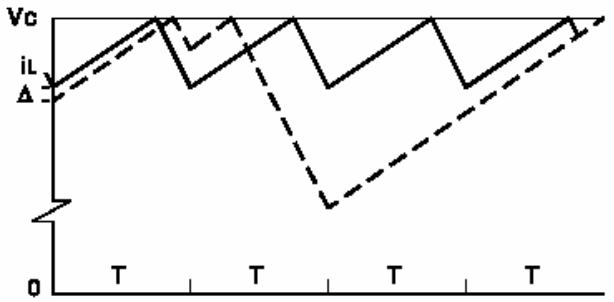
Peak Current Mode Control (CMC)

Peak current mode control does have its own set of problems: Average current is what should be controlled, but peak is controlled instead. The peak-to-average error is quite large, especially at light loads, and the voltage loop must correct for this, which hurts response time. Open loop gain of the CMC loop is already quite low (5 - 10) in the continuous current mode, but when the load diminishes to the point where inductor current becomes discontinuous, the CMC loop gain plummets and the peak-to-average error becomes huge. Operation becomes unsatisfactory in the discontinuous mode.

Subharmonic Instability:

Switching power supply control loops are all subject to subharmonic instability *if the waveforms applied to the two inputs of the PWM comparator do not cross over each other at their points of intersection.* This instability is observed as a tendency to oscillate (or a full-blown oscillation) at frequency $f_S/2$.

Figure shows the subharmonic instability in a peak CMC loop. Normal operation is shown by the solid triangular waveform labeled i_L. This voltage, representing the inductor current, is applied to one side of the comparator. The switch is turned on by a clock pulse, and i_L rises until it reaches control voltage V_C at the other comparator input. The switch turns off, and the current decreases until the next clock pulse occurs. (It does not matter of the current *downslope* is observed through the current sense resistor—referring to Fig. —because switch turn-on is by the clock, and not dependent on the current level.)



IV. CONTROL METHODS IN SMPS

Peak Current Mode Control

Slope Compensation:

Subharmonic instability is eliminated simply by forcing the waveforms at the two inputs of the comparator to cross over each other at their points of intersection. This can be accomplished by adding an artificial ramp to one of the comparator inputs. Figure shows an optimum slope compensation ramp added to the control voltage comparator input, labeled "$V_C + V_S$". The optimum ramp, as shown, causes the two waveforms at the comparator inputs to *coincide* during the interval when the switch is off and the inductor current is decreasing, rather than actually cross over. This is ideal, because, as shown, a perturbation is erased in the very first switching period after its occurrence!!

The compensation ramp reduces the current loop gain. If the ramp slope is increased further so that the waveforms actually cross over, the system is stable but the gain is reduced below optimum (and it actually takes longer for the perturbation to be erased). Optimum is when slopes coincide,

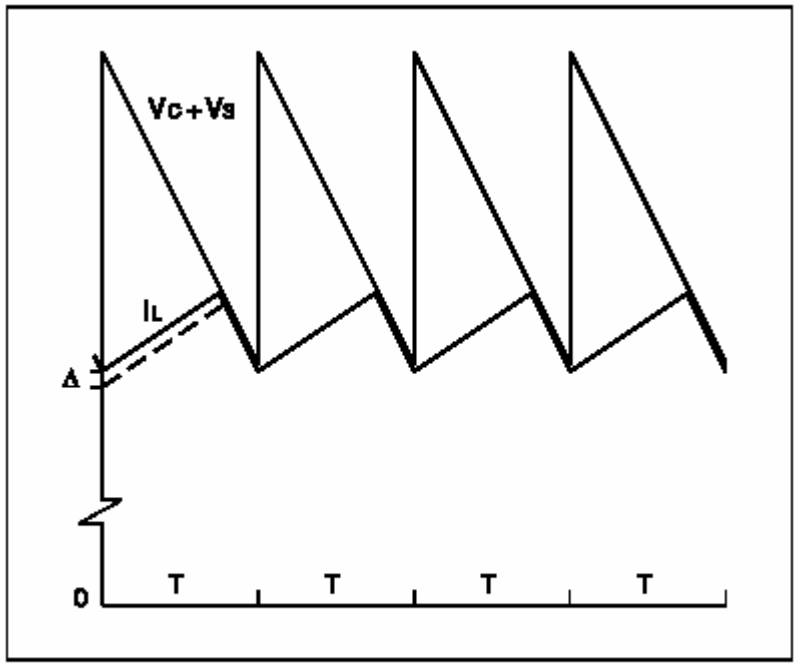
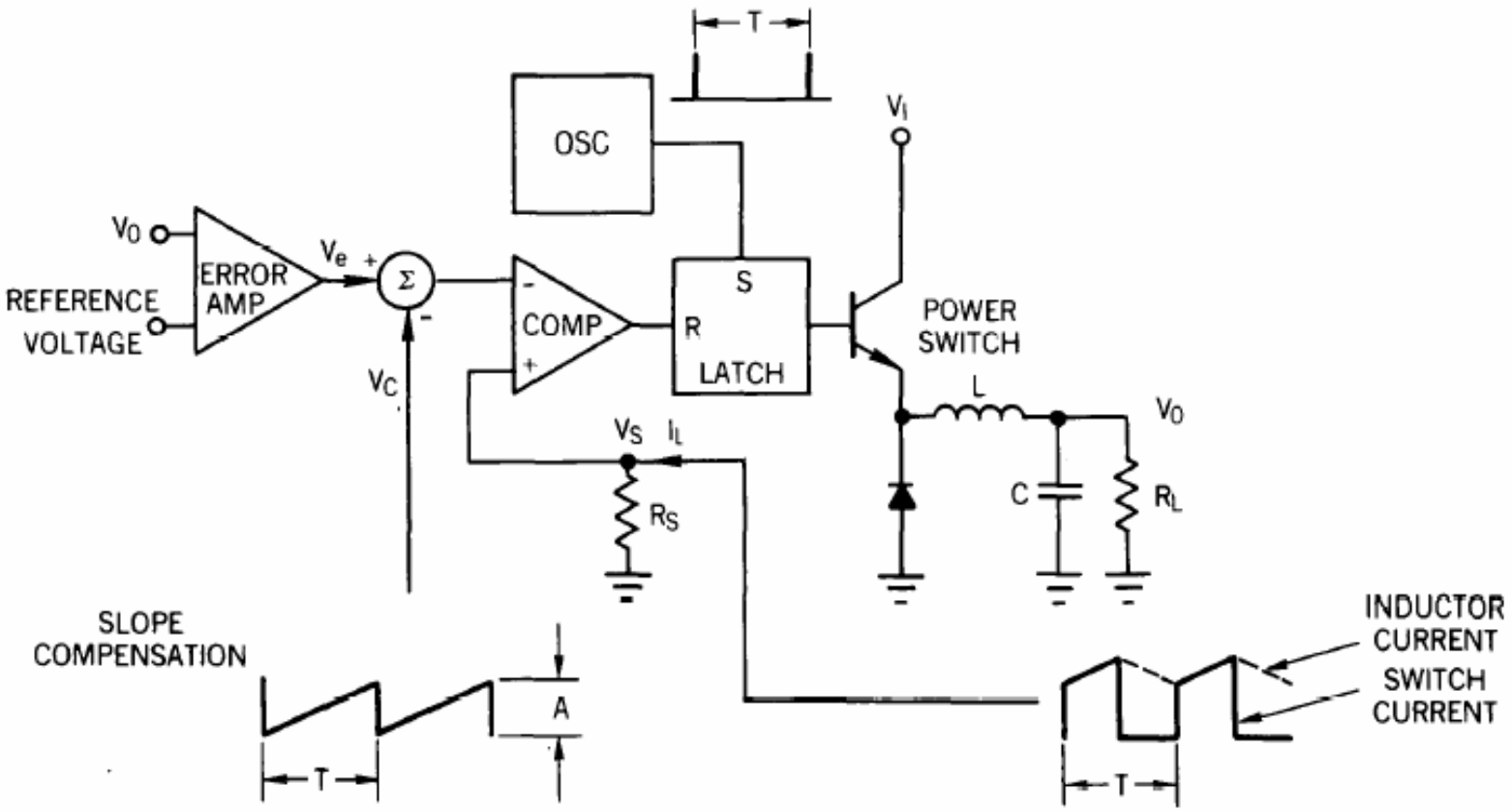


Figure . - Peak CMC with Slope Compensation

IV. CONTROL METHODS IN SMPS



A CURRENT-MODE CONTROLLED BUCK REGULATOR WITH SLOPE COMPENSATION.

Fig.1.

IV. CONTROL METHODS IN SMPS

Instability of the inner current loop occurs for any fixed frequency current-mode converter operating above 50% duty cycle, regardless of the state of the voltage feedback loop. By injecting a small amount of slope compensation into the inner loop, stability will result for all values of duty cycle.

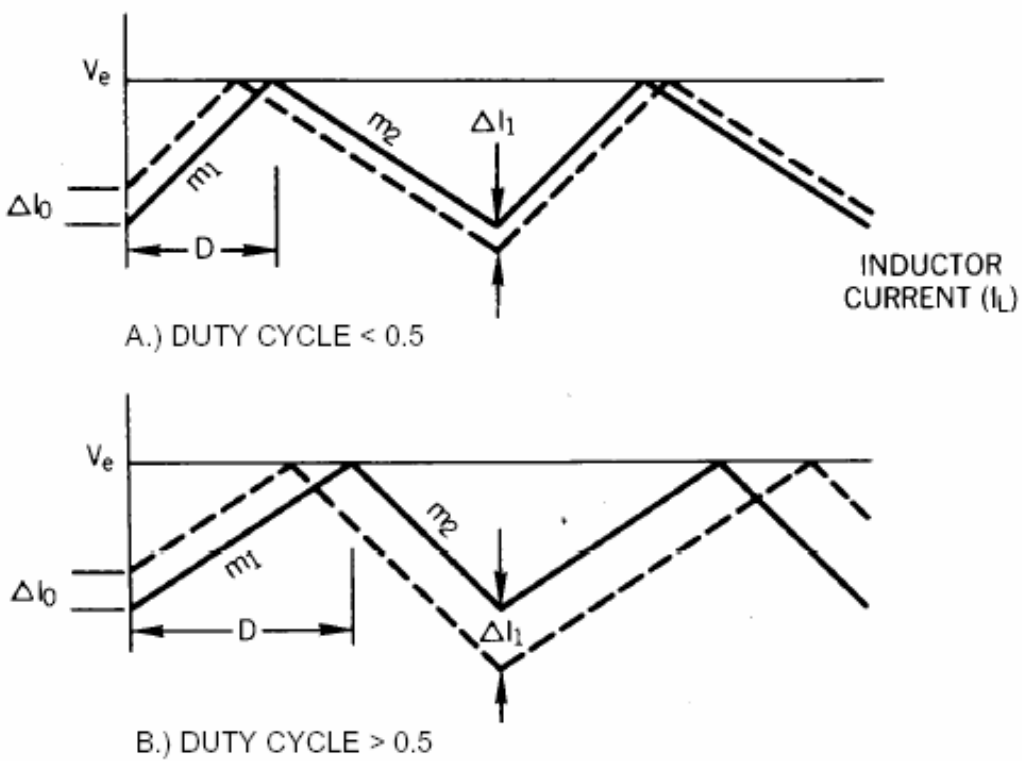


Fig.2. Open-loop instability with current mode converter

IV. CONTROL METHODS IN SMPS

Figure 2 depicts the inductor current waveform, I_L, of a current-mode converter being controlled by an error voltage V_e. By perturbing the current I_L by an amount ΔI, it may be seen graphically that ΔI will decrease with time for D < 0.5 (Figure 2A), and increase with time for D > 0.5 (Figure 2B). Mathematically this can be stated as

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2}{m_1}\right) \qquad (1)$$

Carrying this a step further, we can introduce a linear ramp of slope -m as shown in Figure 2C. Note that this slope may either be added to the current waveform, or subtracted from the error voltage. This then gives

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2 + m}{m_1 + m}\right) \qquad (2)$$

Solving for m at 100% duty cycle gives

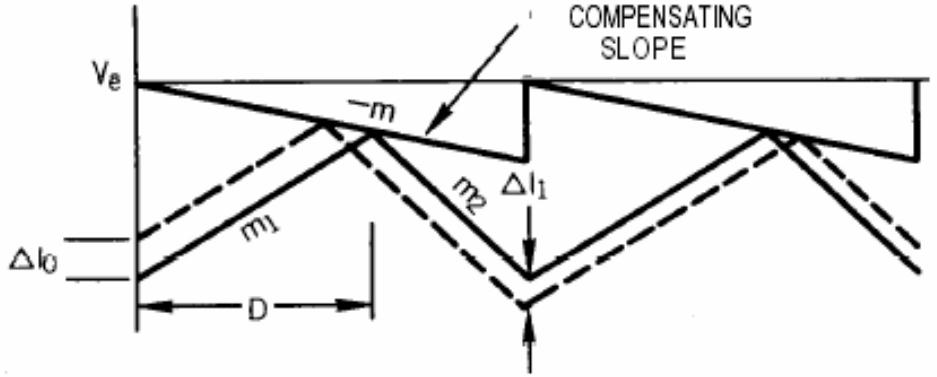
$$m > -\tfrac{1}{2} m_2 \qquad (3)$$

IV. CONTROL METHODS IN SMPS

Therefore, to guarantee current loop stability, the slope of the compensation ramp must be greater than one-half of the down slope of the current waveform. For the buck regulator of Figure 1, m_2 is a constant equal to $\frac{V_0}{L} R_S$, therefore, the amplitude A of the compensating waveform should be chosen such that

$$A > T R_S \frac{V_0}{L} \qquad (4)$$

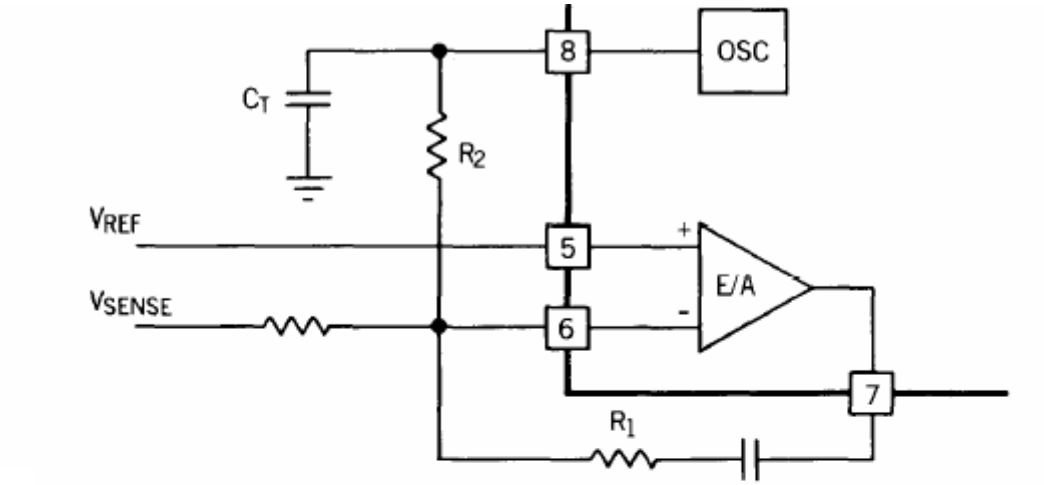
to guarantee stability above 50% duty cycle.



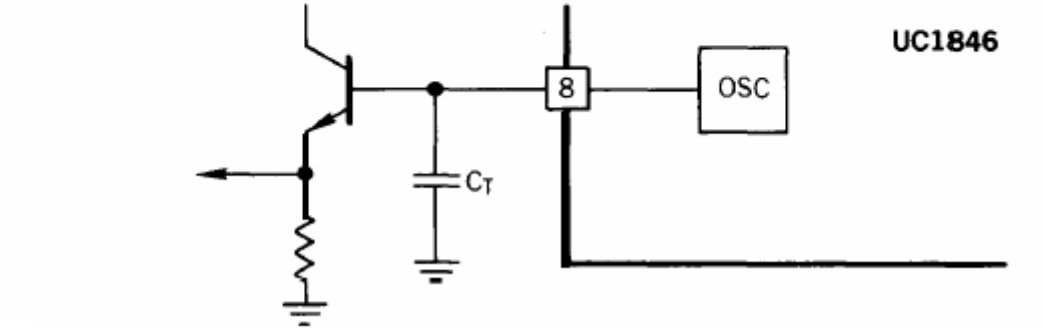
C.) DUTY CYCLE > 0.5 WITH SLOPE COMPENSATION

IV. CONTROL METHODS IN SMPS

Alternative methods of implementing slope compensation with current mode controllers



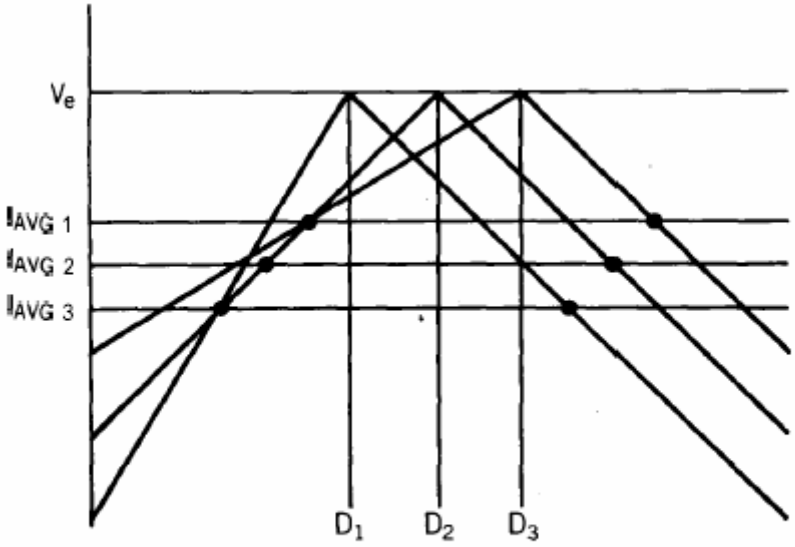
SUMMING OF SLOPE COMPENSATION WITH ERROR SIGNAL



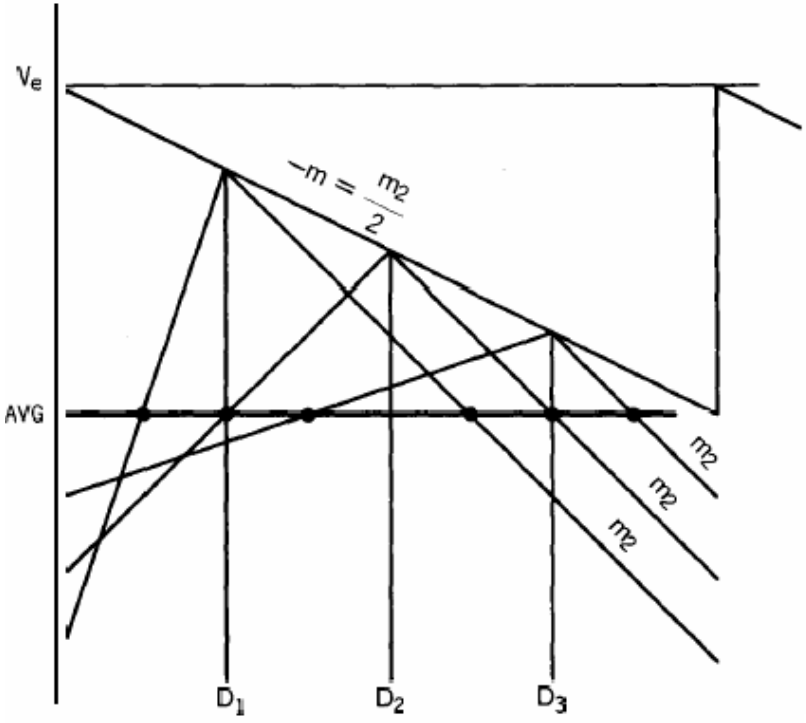
EMITTER FOLLOWER USED TO LOWER OUTPUT IMPEDANCE OF OSCILLATOR.

IV. CONTROL METHODS IN SMPS

Peak current sensing vs average current sensing



- PEAK CURRENT SENSING WITHOUT SLOPE COMPENSATION ALLOWS AVERAGE INDUCTOR CURRENT TO VARY WITH DUTY CYCLE



- AVERAGE INDUCTOR CURRENT IS INDEPENDENT OF D CYCLE AND INPUT VOLTAGE VARIATION FOR A SLOPE COMPENSATION OF m = -½ m_2.

IV. CONTROL METHODS IN SMPS

Average Current Mode Control

Peak current mode problems such as poor noise immunity, need for slope compensation, and peak-to-average current errors cannot be corrected by the inherently low current loop gain. Average current mode control eliminates these problems.

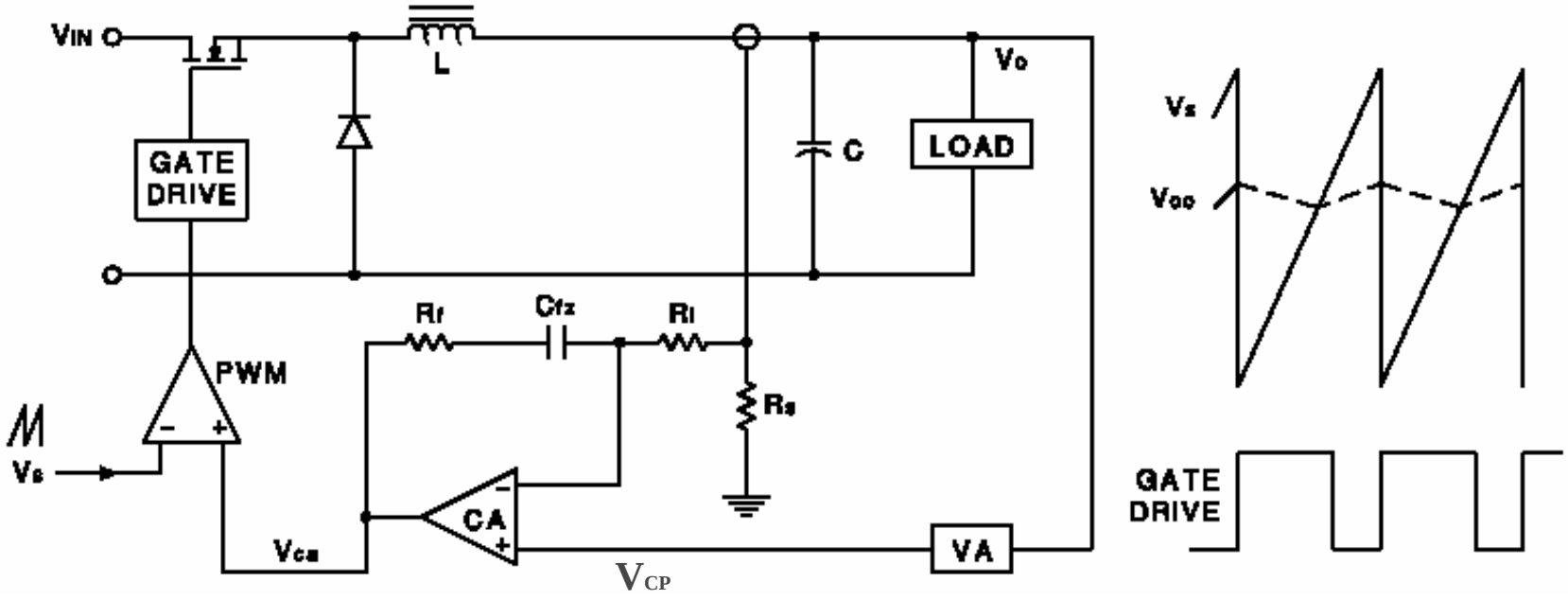


Figure A

IV. CONTROL METHODS IN SMPS

Average Current Mode Control

The deficiencies of the Peak CMC loop basically relate to its low internal loop gain. Average CMC, as shown in Figure A eliminates this problem by adding an error amplifier to the current loop (in addition to the amplifier in the outer voltage loop). Inductor current is sensed through a resistor. The resulting voltage is compared with voltage V_{CP} which sets the *desired* inductor current. The differential, representing the current error, is amplified by CA, the current error amplifier. The CA output is compared to a sawtooth ramp taken from the IC clock generator to determine the duty cycle

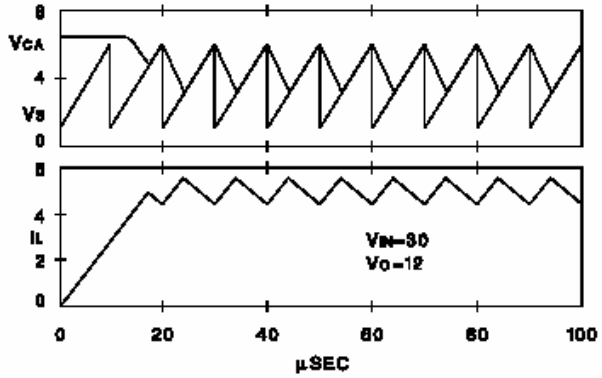


Figure B

Figure B shows the comparator voltage waveforms when the E/A gain is optimized using the slope matching criteria discussed below. Note that amplifier CA inverts the error signal, so the triangular waveform V_{CA} is an upside-down representation of the inductor ripple current. The rising portion of the V_{CA} waveform (coincident with sawtooth waveform V_S) represents *falling* inductor current, when the switch is OFF. As Figure B shows, where the waveforms intersect (near the midpoint of the sawtooth ramp) and the switch turns OFF is where the inductor current is at its *peak* (the waveform is inverted). Why is this called average CMC if it really functions at the peak??

IV. CONTROL METHODS IN SMPS

Average Current Mode Control

Actually, average CMC when optimized is identical in its behavior to peak CMC with *all* of its positive attributes – it has the same crossover frequency, the same instantaneous response to a current overload, etc. But at frequencies below f_C, where the peak CMC loop gain flattens out at a gain of only 5 or 10, the gain of the average CMC loop keeps rising, ultimately to a gain of more than 1000 if desired. This much higher loop gain at lower frequencies eliminates the peak-to-average error and enables the average CMC loop to function well at light loads when the inductor current becomes discontinuous.

Loop Design Procedure:

Normally, the power circuit topology is decided upon and the power circuit values are determined, based on the application requirements, before control loop design begins. Occasionally, problems encountered in the control loop design process may force a rethinking of these power circuit decisions. The steps in the control loop design process will generally proceed as follows:

(1) Define the control loop strategy and plot the tentative goal.

(2) Plot the known part of the loop.

(3) Define the crossover frequency, f_S.

(4) Try to meet the goal — Define and plot the error amplifier and overall loop characteristics.

V. CONTROL METHODS IN SMPS

Examples of Analog PWM Controller ICs

Unitrode Products from Texas Instruments

UC1825
UC2825
UC3825

High Speed PWM Controller

FEATURES

- Compatible with Voltage or Current Mode Topologies
- Practical Operation Switching Frequencies to 1MHz
- 50ns Propagation Delay to Output
- High Current Dual Totem Pole Outputs (1.5A Peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start / Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1mA)

DESCRIPTION

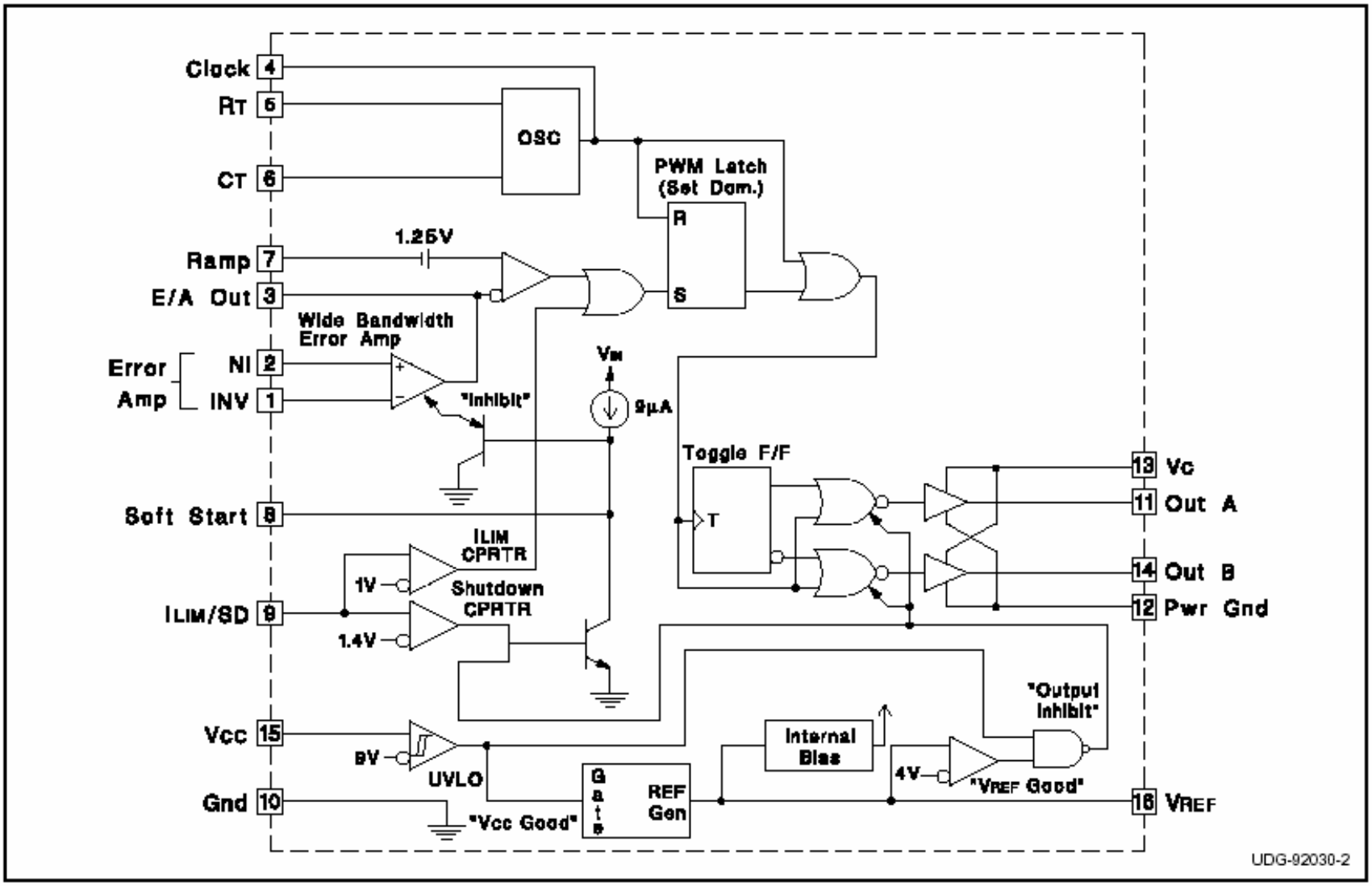
The UC1825 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1V threshold, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at an output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the outputs are high impedance.

These devices feature totem pole outputs designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is designed as a high level.

V. CONTROL METHODS IN SMPS

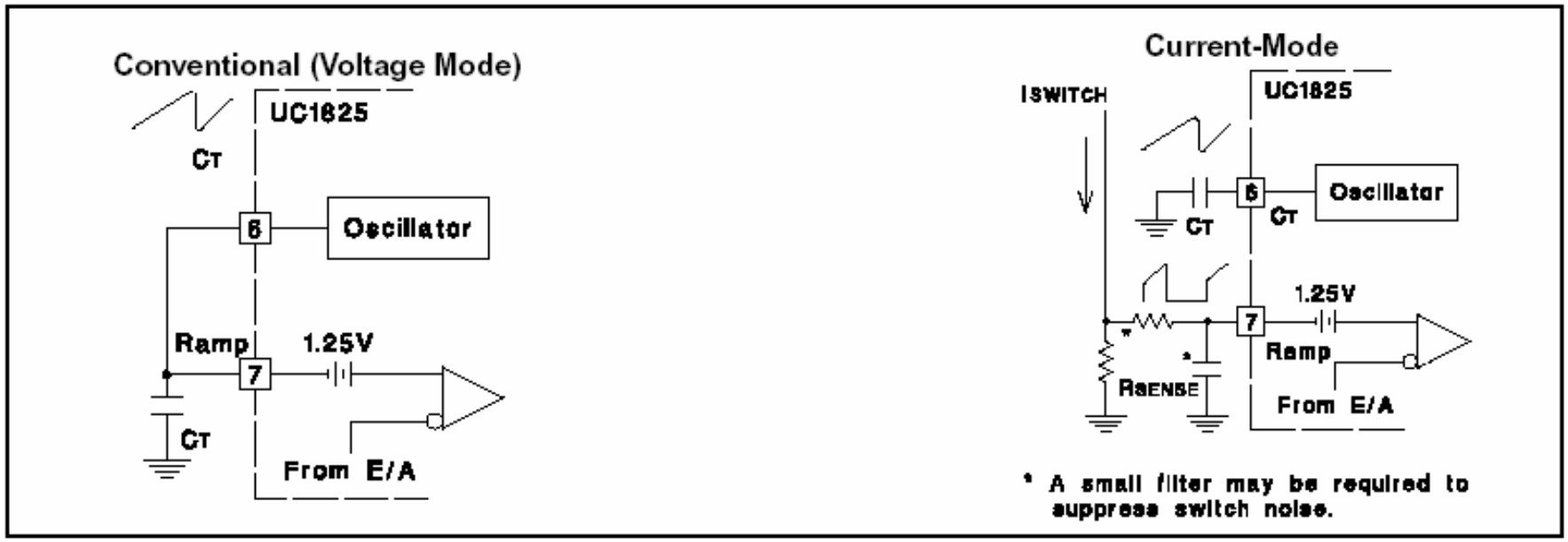
BLOCK DIAGRAM



V. CONTROL METHODS IN SMPS

Voltage mode and current mode controls using PWM controller IC UC3825

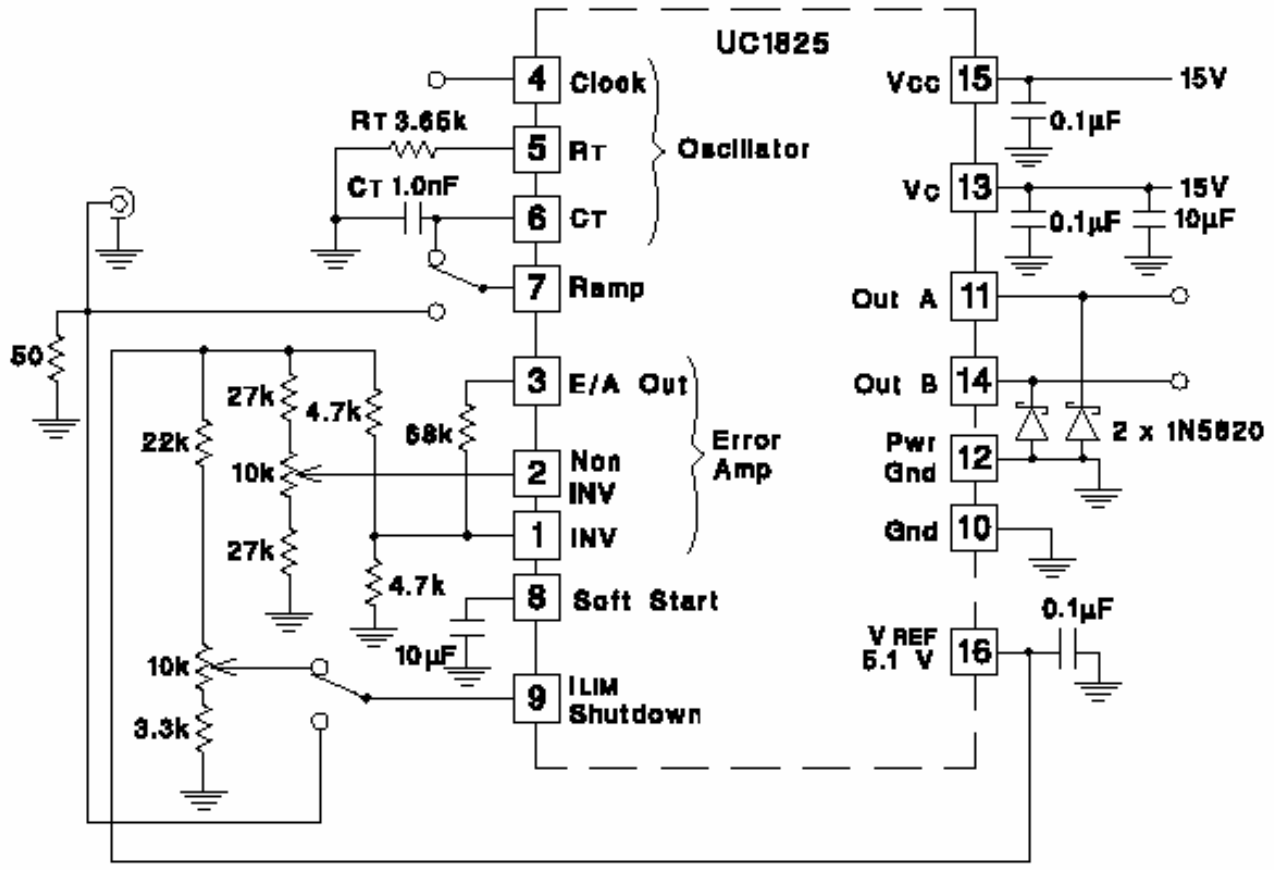
PWM Applications



V. CONTROL METHODS IN SMPS

Open Loop Laboratory Test Fixture

UC3825



This test fixture is useful for exercising many of the UC1825's functions and measuring their specifications.

As with any wideband circuit, careful grounding and by-pass procedures should be followed. The use of a ground plane is highly recommended.

V. CONTROL METHODS IN SMPS

INTEGRATED CIRCUITS
UNITRODE

UC1856
UC2856
UC3856

Improved Current Mode PWM Controller

FEATURES

- Pin-for-Pin Compatible With the UC3846
- 65ns Typical Delay From Shutdown to Outputs, and 50ns Typical Delay From Sync to Outputs
- Improved Current Sense Amplifier With Reduced Noise Sensitivity
- Differential Current Sense with 3V Common Mode Range
- Trimmed Oscillator Discharge Current for Accurate Deadband Control
- Accurate 1V Shutdown Threshold
- High Current Dual Totem Pole Outputs (1.5A peak)
- TTL Compatible Oscillator SYNC Pin Thresholds
- 4kV ESD Protection

DESCRIPTION

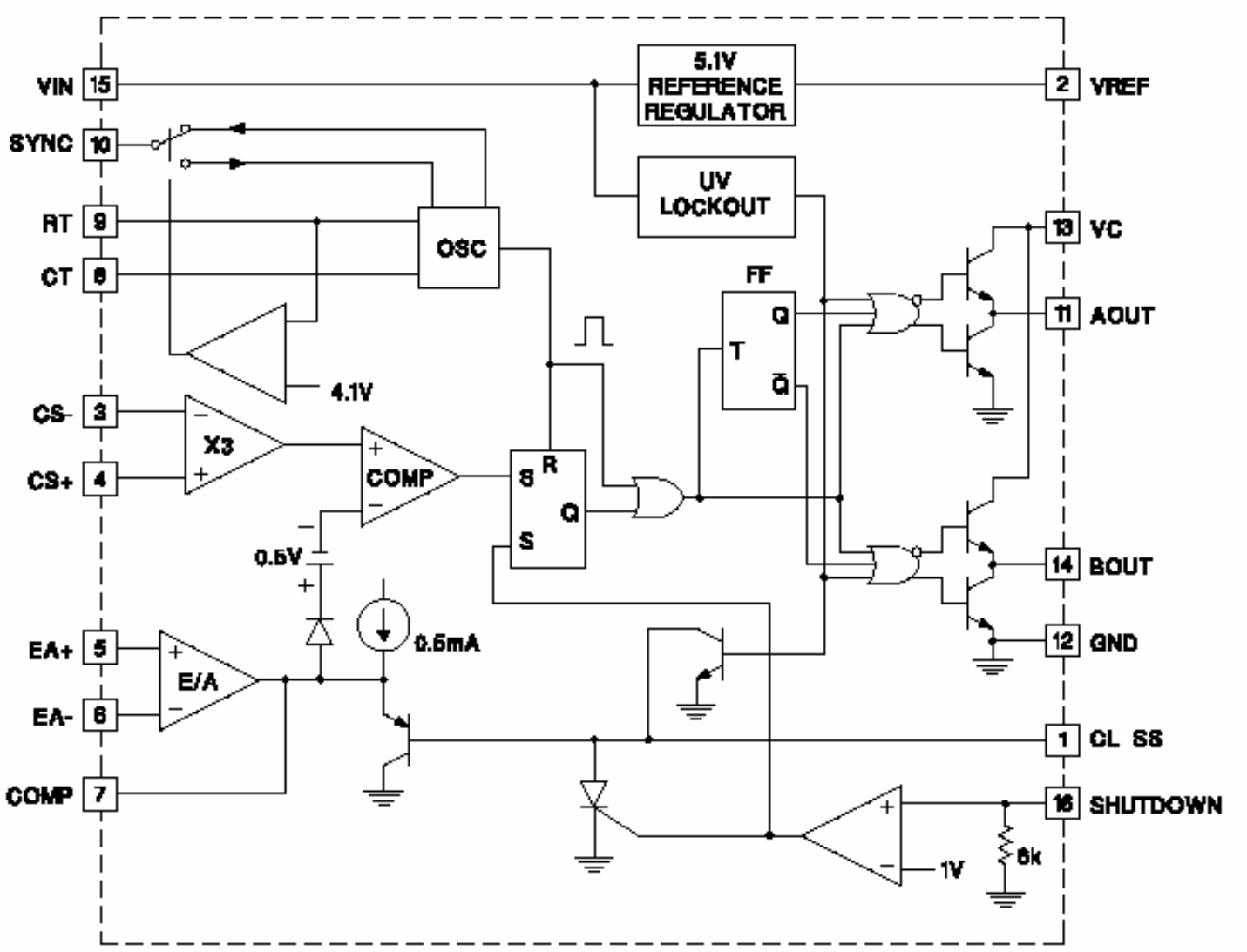
The UC3856 is a high performance version of the popular UC3846 series of current mode controllers, and is intended for both design upgrades and new applications where speed and accuracy are important. All input to output delays have been minimized, and the current sense output is slew rate limited to reduce noise sensitivity. Fast 1.5A peak output stages have been added to allow rapid switching of power FETs.

A low impedance TTL compatible sync output has been implemented with a tri-state function when used as a sync input.

Internal chip grounding has been improved to minimize internal "noise" caused when driving large capacitive loads. This, in conjunction with the improved differential current sense amplifier results in enhanced noise immunity.

Other features include a trimmed oscillator current (8%) for accurate frequency and dead time control; a 1V, 5% shutdown threshold; and 4kV minimum ESD protection on all pins.

V. CONTROL METHODS IN SMPS



IV. CONTROL METHODS IN SMPS

4.3. Closing the loop- Feedback and Stability

- *SMPS use closed loop feedback to achieve design objectives for line and load regulation, and dynamic response. Accurate and tight regulation of the output voltage requires a high dc gain. But, with high gain comes the possibility of instability.*

- *As in all real-world control applications with electronic negative feedback loops, the process to be controlled is much slower than the abilities of feedback path. So the gain and the 'responsiveness' of the feedback path must be tailored to the process it is controlling.*

- *Through the use of some simple tools, the designer can compensate the feedback path and ensure stability.*

IV. CONTROL METHODS IN SMPS

Bode Plots

Bode plot is a simple method to represent the response of a circuit over a range of frequencies. It consists of two parameters: the gain and phase plotted against frequency. Since the range values for the gain can be very large, and the gain function is non-linear, it is convenient to represent its function as a logarithm. The amplitude level is represented in decibels (dB)

$$\mathbf{dB = 20 \log_{10} (Gain)}$$

The frequency also is plotted in log scale to help condense the plot to a reasonable size. The gain and phase curves are reasonably approximated by replacing them with 'asymptotes'.

As an example, first consider an R-C filter:

IV. CONTROL METHODS IN SMPS

Bode Plots

Low Pass — Single Pole: Figure B-1

$$F(s) = \frac{1}{1+\frac{s}{\omega_p}} ; \quad \omega_p = \frac{1}{RC} \text{ or } \frac{L}{R}$$

Gain Slope: -20 dB/decade; Phase Lag: -90° total

First Order Filters (R-C or L-R):

Single pole or zero first order filters both have gain slopes of 20 dB/decade above the corner frequency. The phase shift asymptotes slope 45°/decade, extending 1 decade each side of the corner frequency for a total 90° phase shift (see Figure B-1).

Single Zero: Has the same gain and phase characteristic as the single pole shown in Figure B-1, except gain increases with frequency. Gain and phase slopes are both *positive*.

$$F(s) = 1+\frac{s}{\omega_z} ; \quad \omega_z = \frac{1}{RC} \text{ or } \frac{L}{R}$$

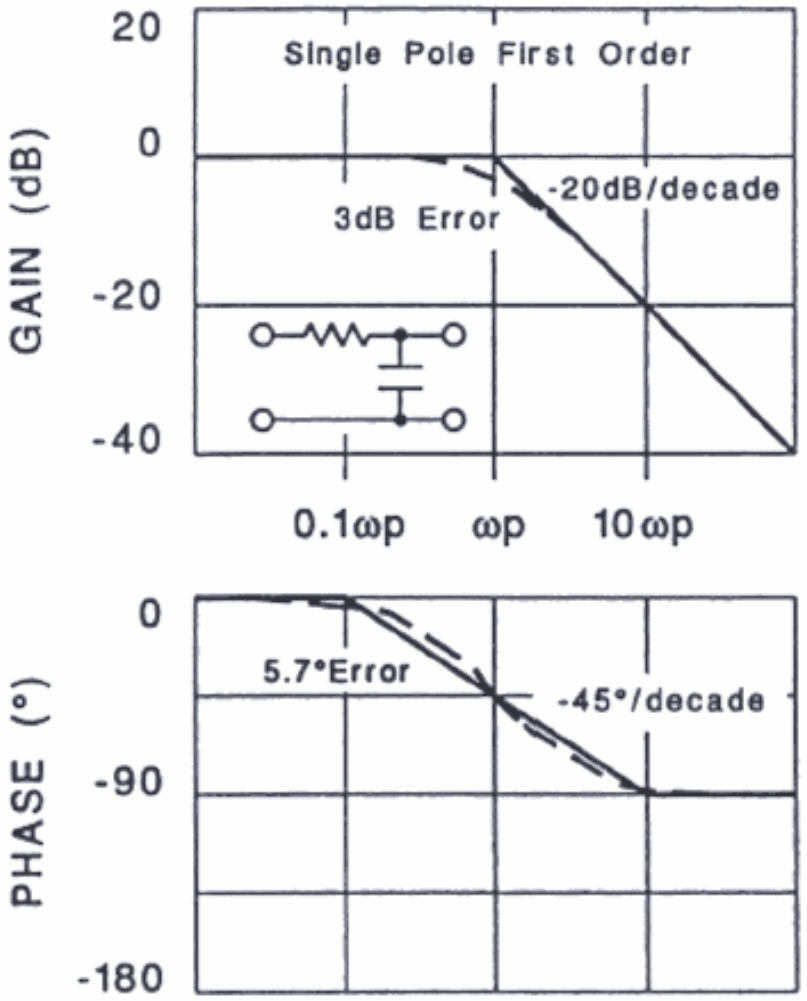


Figure B-1

IV. CONTROL METHODS IN SMPS

Bode Plots

- *The term 'pole' refers to any circuit that causes a decrease in the output voltage (-20dB/dec) with increasing frequency. These are frequency-dependent terms in the denominator of the transfer function. Each pole contributes a -90° phase shift (phase lag).*
- *'Zeros' are terms that are found in the numerator of the transfer function, and cause an increase in output voltage (+20 dB/dec) with increasing frequency. Each zero contributes a +90 ° phase shift (phase lead).*
- *When more than one pole or zero is in the circuit in a closed loop feedback system, the magnitude slope and phase of each is summed at each frequency.*

IV. CONTROL METHODS IN SMPS

Second Order Filters (Resonant LC):

The resonant LC filter of Figure B-2 has a 2 pole –40 dB/decade gain slope above its corner (resonant) frequency, and a total phase lag of 180°. The gain characteristic has a resonant peak which varies with Q, as shown in Figure .The resonant effect is suppressed in the closed-loop characteristic, although it can reduce gain margin and cause loop instability if the resonance is close to the crossover frequency.

$$F_s = \frac{1}{1 + (s/\omega_0)/Q + (s/\omega_0)^2}$$

$$\text{where } \omega_o = \frac{1}{\sqrt{LC}}, \quad Q = \omega_o \frac{L}{R_s}$$

Gain Slope: -40 dB/decade; Phase Lag: -180° total

Bode Plots

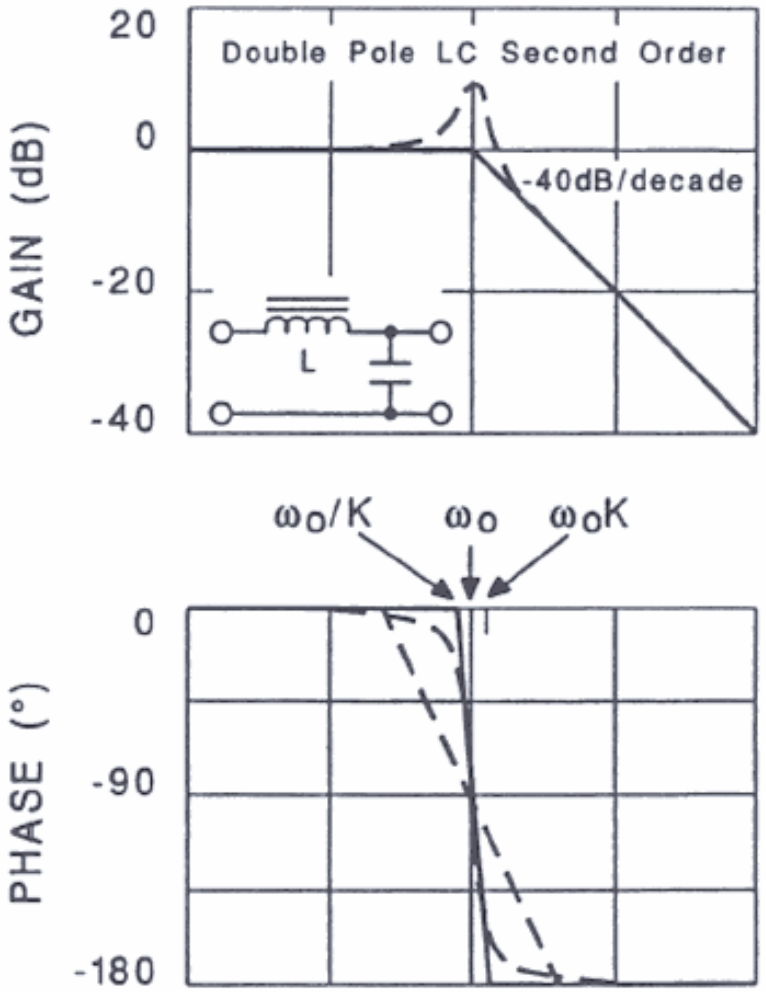


Figure B-2

IV. CONTROL METHODS IN SMPS

Closing the loop

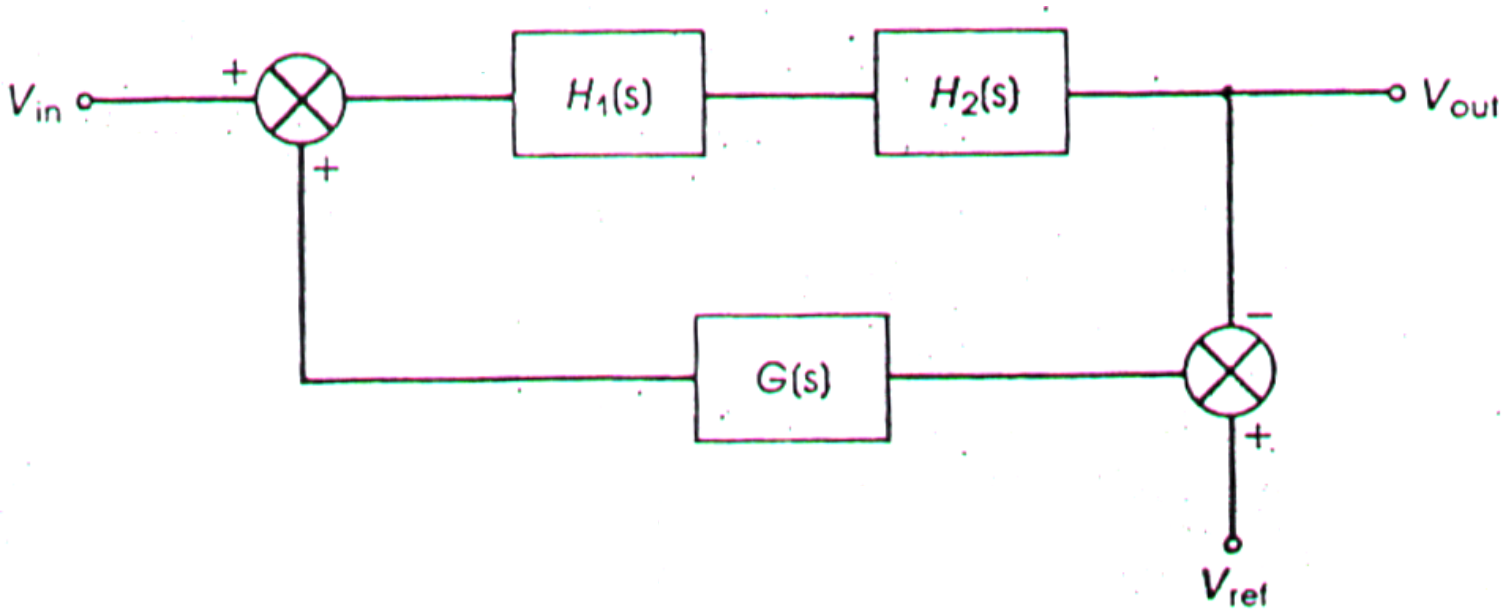
- *SMPS rely on negative feedback to maintain o/p voltages at their specified value. To accomplish this, an inverting differential amplifier (EA) is used to sense the difference between a reference voltage (V_{ref}), and the actual output voltage (V_{out}). The inverse of this difference multiplied by the gain of the EA results in what is called the 'error voltage', V_{err}. So, error between the reference and the actual output is minimized, as the demands of the load causes the output voltages to rise and fall.*

- *If the loads, and input voltage never changed, the gain of EA would have to be considered only at DC. But, in practice this is not true, loads increase and decrease, i/p voltage rises and falls. So, the EA must respond to these non DC effects by having gain at higher f's.*

IV. CONTROL METHODS IN SMPS

Closing the Loop

Closed loop block diagram of SMPS:



$H_1(s)$: AC transfer function of the modulator, including any transformer
$H_2(s)$: Transfer function of the output filter, and
G(s): Transfer function of EA and compensation network.

IV. CONTROL METHODS IN SMPS

Closing the Loop

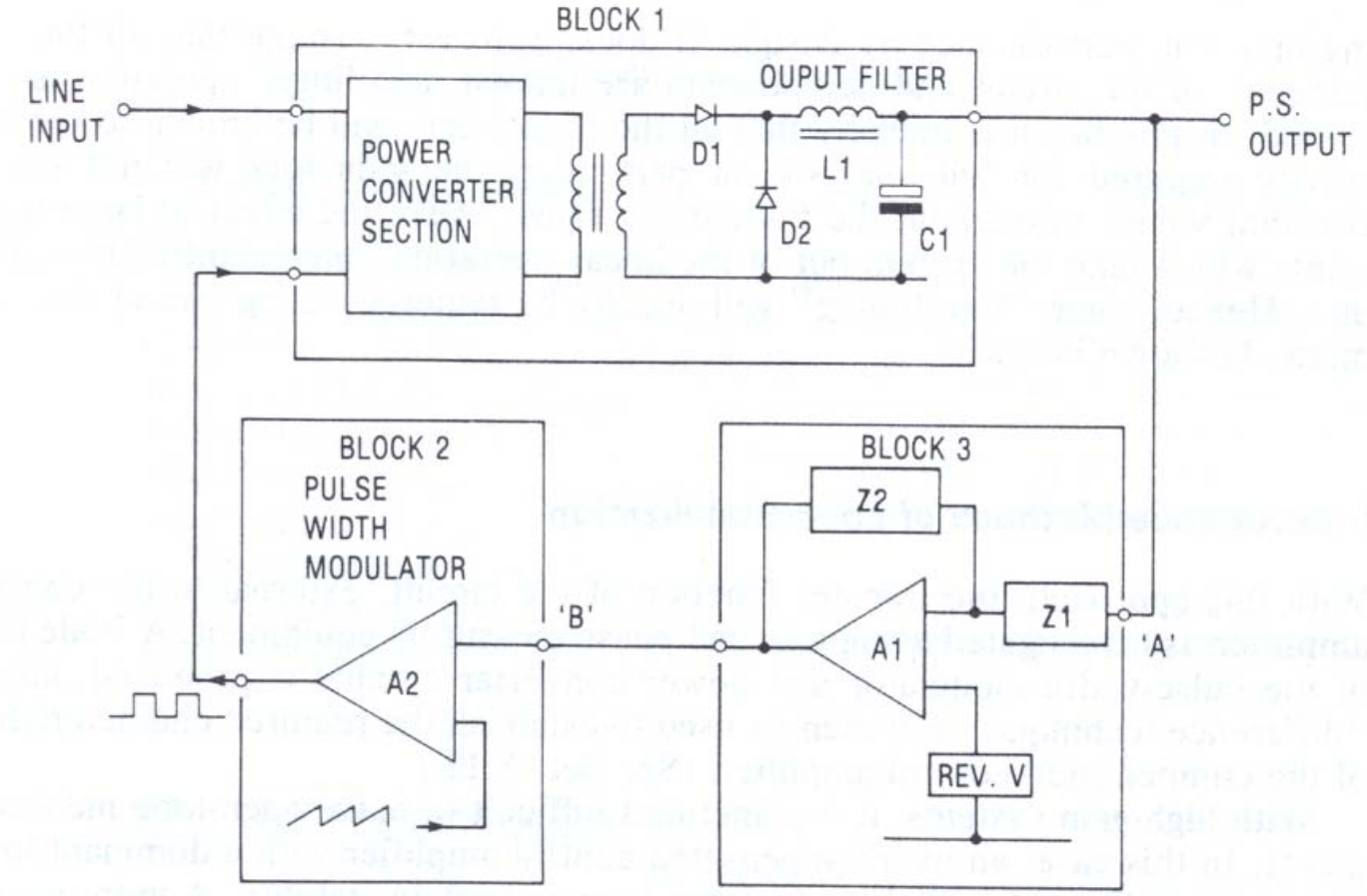
The closed loop transfer function is : $\dfrac{H_1(s)\,H_2(s)}{1+G(s)H_1(s)H_2(s)}$

The poles and zeros of the system can be determined from the actual constituents of the blocks.

As one proceeds around the loop, the gain and phase of each successive block are added to the sum. In SMPS, it is convenient to cut the EA out of closed loop (Block 3 in next slide), and see what the remaining elements in the loop contribute to loop gain and phase.

By this way, the EA can be used to compensate for some detrimental effects of the rest of the loop. This partial loop is called the 'control-to-output characteristics'.

IV. CONTROL METHODS IN SMPS



Block schematic diagram of the control loop, for a forward (buck-derived) switchmode power converter. Showing power section block 1, pulse-width modulator block 2, and control circuit block 3.

IV. CONTROL METHODS IN SMPS

Stability Criteria

The rule of stability, when applied to power supplies is simply:

'Whenever the closed loop gain is greater than or equal to 1, the closed-loop phase should never come to within 45 - 60 ° of 360 °, in practice !

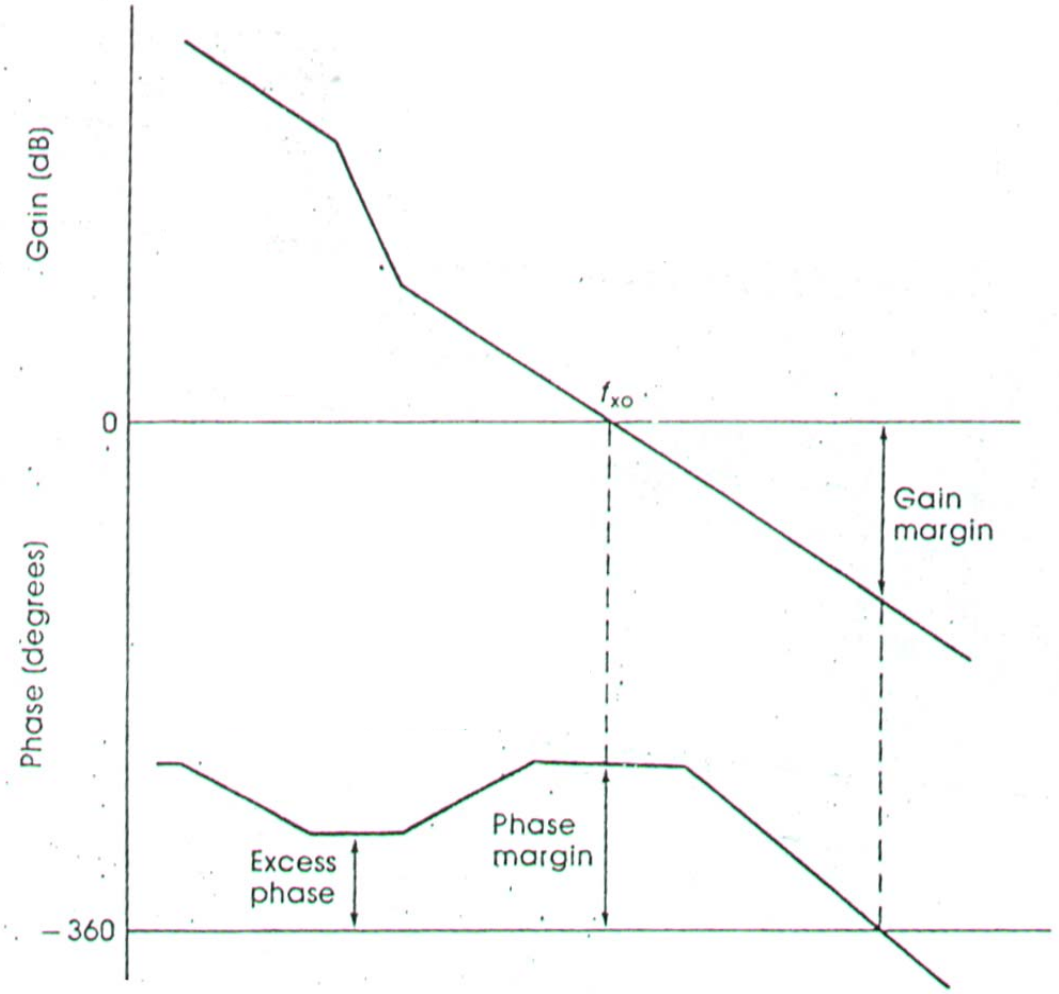
These are the max. boundaries of the gain and phase Bode Plots of the overall closed-loop system. Otherwise, systems will break out into oscillation under the effect of a small transient, or at least will ring in an underdamped fashion.

The definition of closed-loop Bode response and the design of compensation network are the main difficulties.

Next Fig. shows the meaning of some terms used in closed loop systems:

IV. CONTROL METHODS IN SMPS

Stability Criteria



IV. CONTROL METHODS IN SMPS

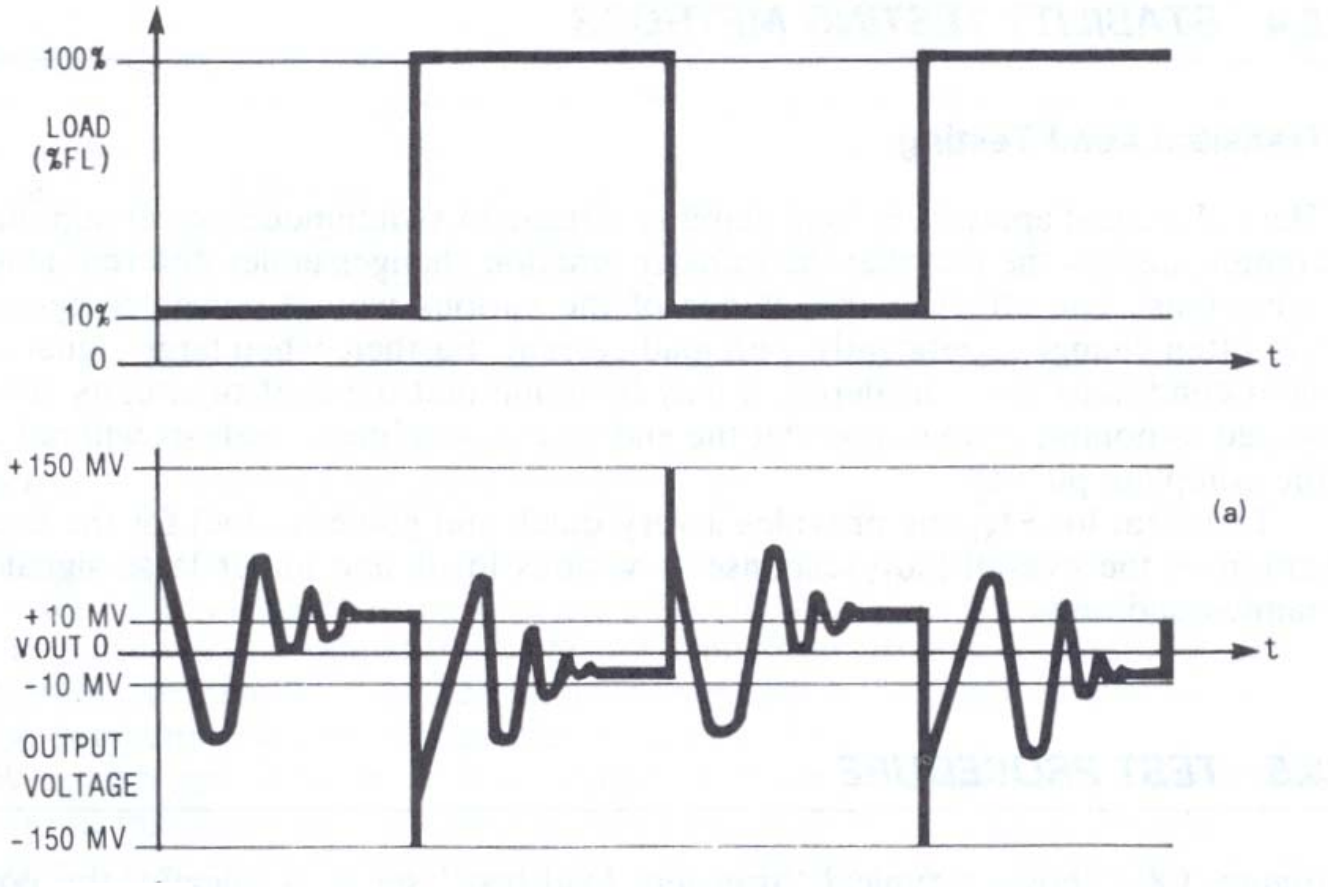
Stability Criteria

1. *Phase Margin:* **This is the value of the phase of the closed loop transfer function at the gain crossover frequency (0dB)**
2. *Gain Margin:* **This is the value of the gain when the phase of the closed loop system crosses 360°.**
3. *Excess phase:* **This is the value of the phase of the closed loop system at its closest point to 360° whenever the closed loop gain is greater than unity (phase margin anywhere within the system bandwidth).**

For system stability, it is important to always keep the phase of the closed loop system more than desired excess phase away from 360°.

IV. CONTROL METHODS IN SMPS

Typical transient current and voltage waveforms



a. Underdamped performance

IV. CONTROL METHODS IN SMPS

FIG. 3.8.3 Typical output current and voltage waveforms, for switchmode converters under pulse loading conditions: (*a*) underdamped performance, (*b*) overdamped performance, (*c*) optimum performance.

b. Overdamped performance, c. Optimum performance

IV. CONTROL METHODS IN SMPS

a. Underdamped performance:

A power supply showing this type of response will have poor gain and phase margins, and may be only conditionally stable.

With a performance of this type, oscillation may occur under some loading conditions, or as a result of additional phase change or increase in gain at higher temperatures.

Hence, this response is not recommended, and the compensation network should be adjusted to roll-off at a lower frequency.

IV. CONTROL METHODS IN SMPS

b. Overdamped performance:

Although this response type is very stable, it does not give the best transient recovery performance. The roll-off frequency should be increased.

c. Optimum performance

This response is closer to the optimum condition, giving good performance and stable transient response, with adequate gain and phase margins for most applications.

IV. CONTROL METHODS IN SMPS

The control-to-output transfer functions of common SMPS

The control-to-output transfer function is a partial model of the final closed loop power supply system. It removes the error amplifier from the loop, and determines the remaining circuit's inherent gain, poles, and zeros.

The method of compensation of the error amplifier is chosen in order to make the supply both stable and to meet the load regulation and transient response specs.

All common SMPS fall into three basic control-to-output categories:

IV. CONTROL METHODS IN SMPS

The control-to-output transfer functions of common SMPS

The three basic control-to-output categories:

i- Forward mode (buck converter or some form of transformer isolated foward mode converter) using voltage mode control

ii- Flyback mode converters using voltage-mode control,

and

Forward mode converters using current mode control.

IV. CONTROL METHODS IN SMPS

i- For forward mode converters using voltage mode control:

The control-to-output transfer function is as shown in next Fig. The lowest encountered corner frequency is that contributed by the output LC filter. The corner frequency can be calculated by:

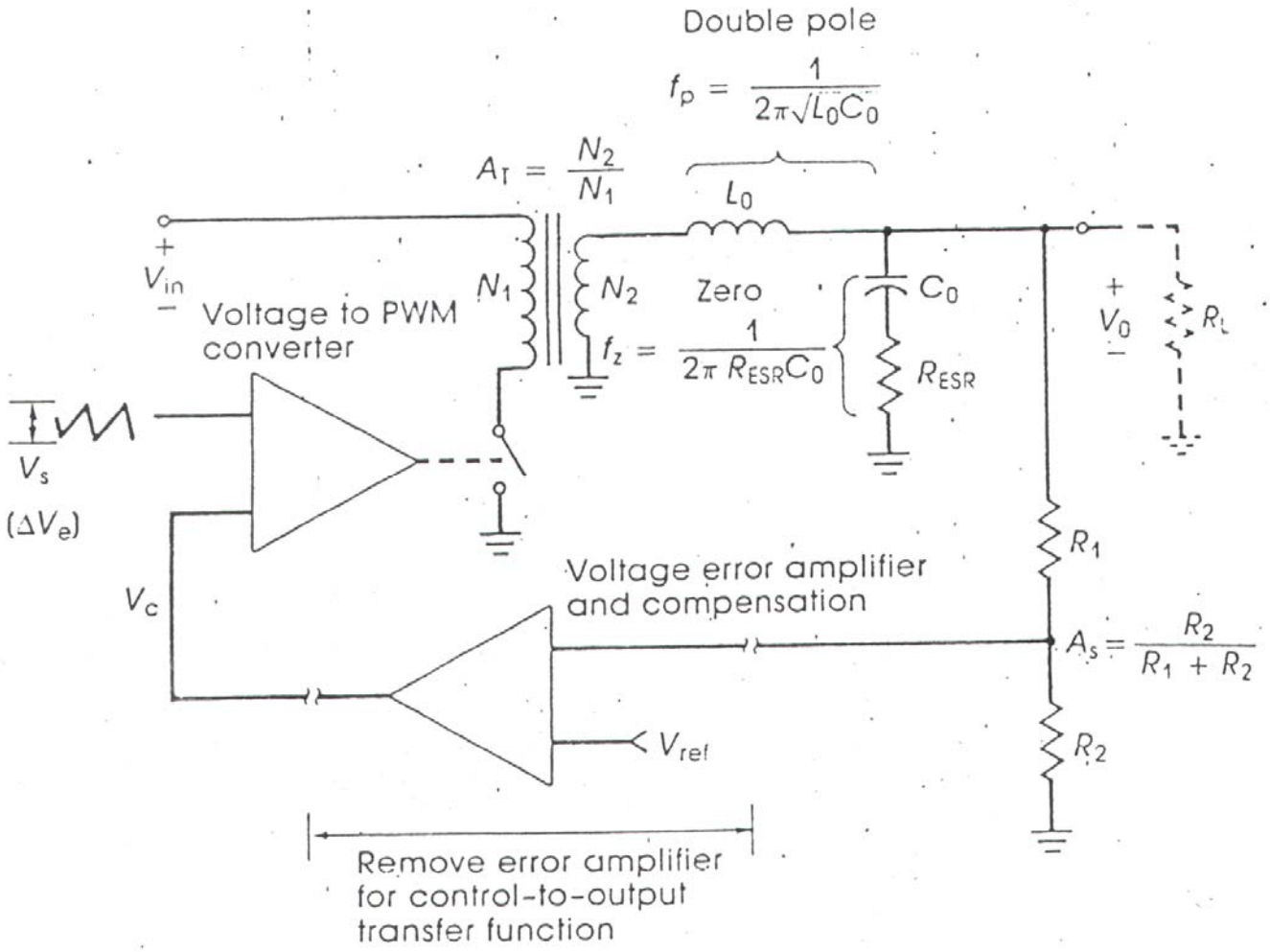
$$f_{LC} = 1 / (2\pi\sqrt{L_o C_o})$$

This represents a double pole and exhibits a -40 dB/decade roll-off and a -180° phase shift above its corner frequency.

The second major corner frequency is the zero contributed by the ESR of the output filter capacitor and output capacitance value itself. The corner frequency is: $f_z = 1 / (2\pi R_{esr} C_o)$

IV. CONTROL METHODS IN SMPS

Physical circuit elements within a forward mode converter that contribute to control-to-output characteristics:



IV. CONTROL METHODS IN SMPS

- To calculate the gain of the control-to-output transfer function at 0 Hz (or DC) for a forward mode converter, one simply adds the gain contributed by the step-up/step-down transformer to the gain of time averaged waveform presented to the LC filter.

- This can be obtained by:
$A_{DC} = (N_S/N_P).V_{in} / \Delta V_e$ where, ΔV_e is the max. change in voltage of error amplifier

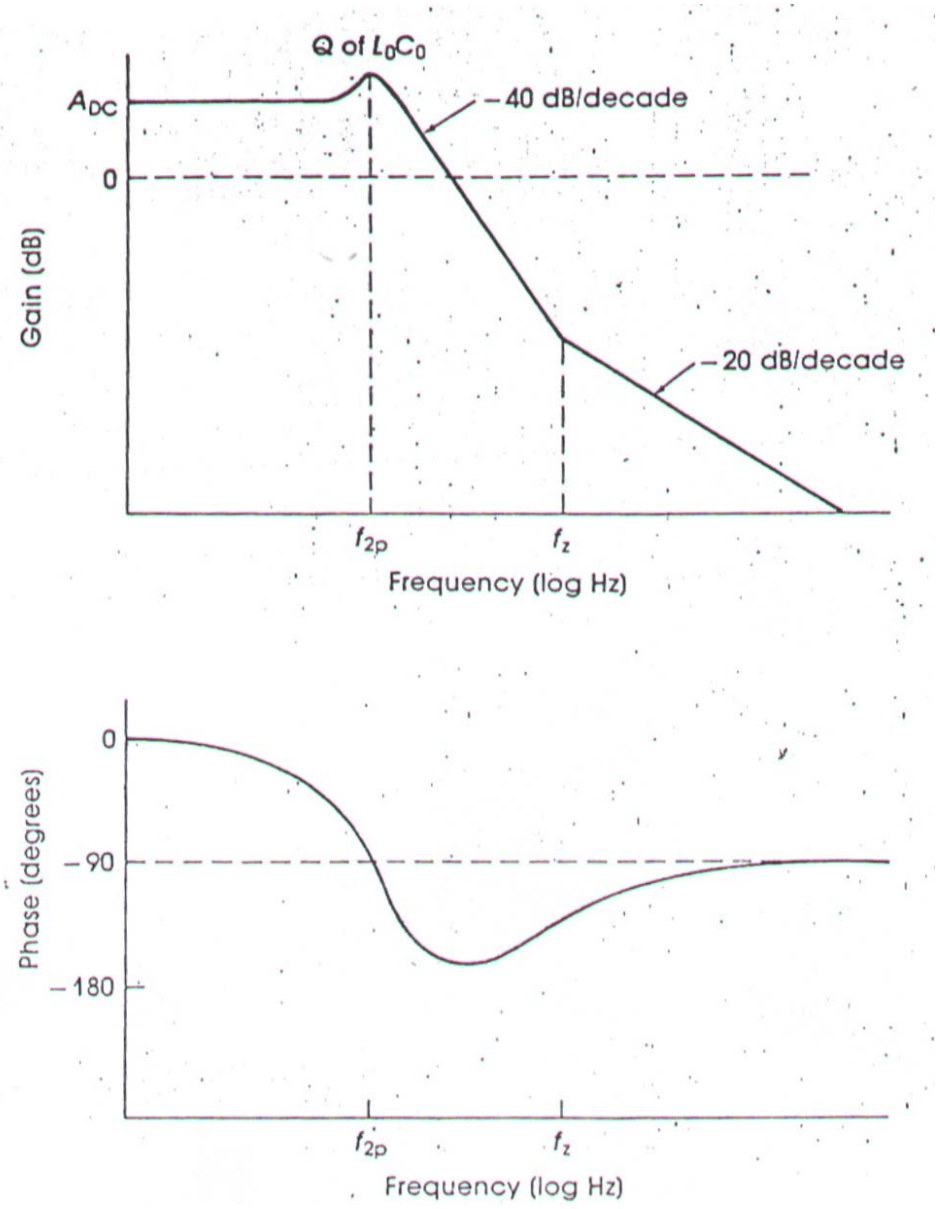
- This calculation should be done at the highest specified input voltage because, the system exhibits its highest DC gain at that point.

- Control-to-output characteristics of the forward mode converters is shown below.

IV. CONTROL METHODS IN SMPS

For forward mode converters, the process needed to develop the control-to-output Bode plot is straightforward:

The gain at DC,and the pole and zero corner frequencies should be determined.



IV. CONTROL METHODS IN SMPS

ii- For flyback mode converters using voltage mode control, and for forward-mode converters using current mode control:

In that case, the main filter pole in the transfer function is heavily dependent on the equivalent resistance of the output load. In that case, it is recommended to consider both Bode Plots at high and low input line, and at light and heavy loads.

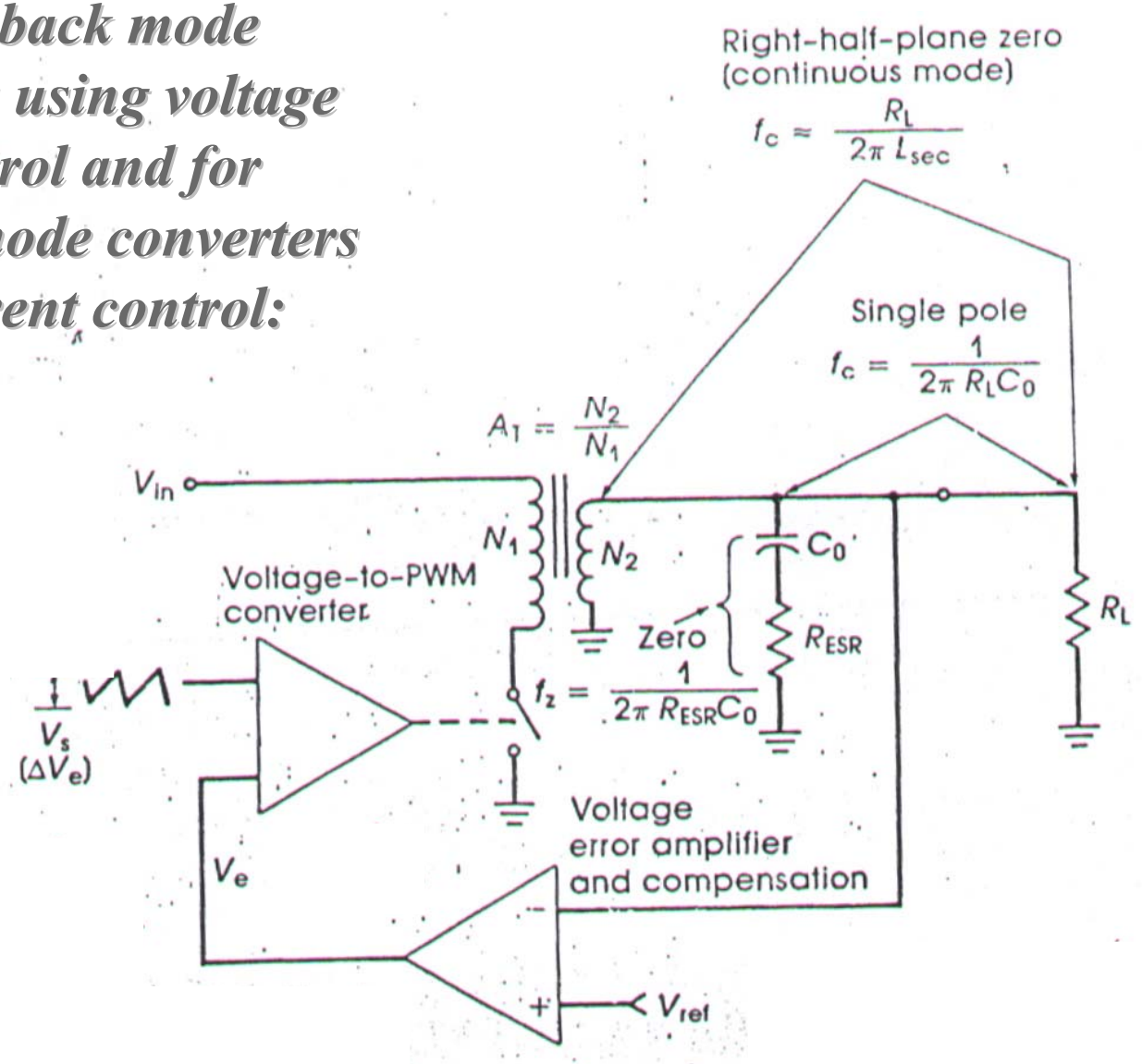
A single pole is created by the output filter capacitor and the output load resistance, and a zero is contributed by the esr of Co.

$f_p = 1 / (2\pi R_L C_o)$, it depends highly on R_L.

Also, if the load is highly inductive, it adds another zero to the transfer function.

IV. CONTROL METHODS IN SMPS

ii- For flyback mode converters using voltage mode control and for forward-mode converters using current control:



IV. CONTROL METHODS IN SMPS

ii- For flyback mode converters using voltage mode control and for forward-mode converters using current control:

The zero contributed by the esr of output filter capacitor is:

$$f_z = 1 / (2\pi R_{esr} C_o)$$

The DC gain of the transfer function is calculated by:

$$A_{DC} = [N_s/N_p] \ (V_{in} + V_{out})^2 / (V_{in} \Delta V_e)$$

This should also be calculated for highest and lowest input voltage.

IV. CONTROL METHODS IN SMPS

ii- *For flyback mode converters using voltage mode control and for forward-mode converters using current control:*

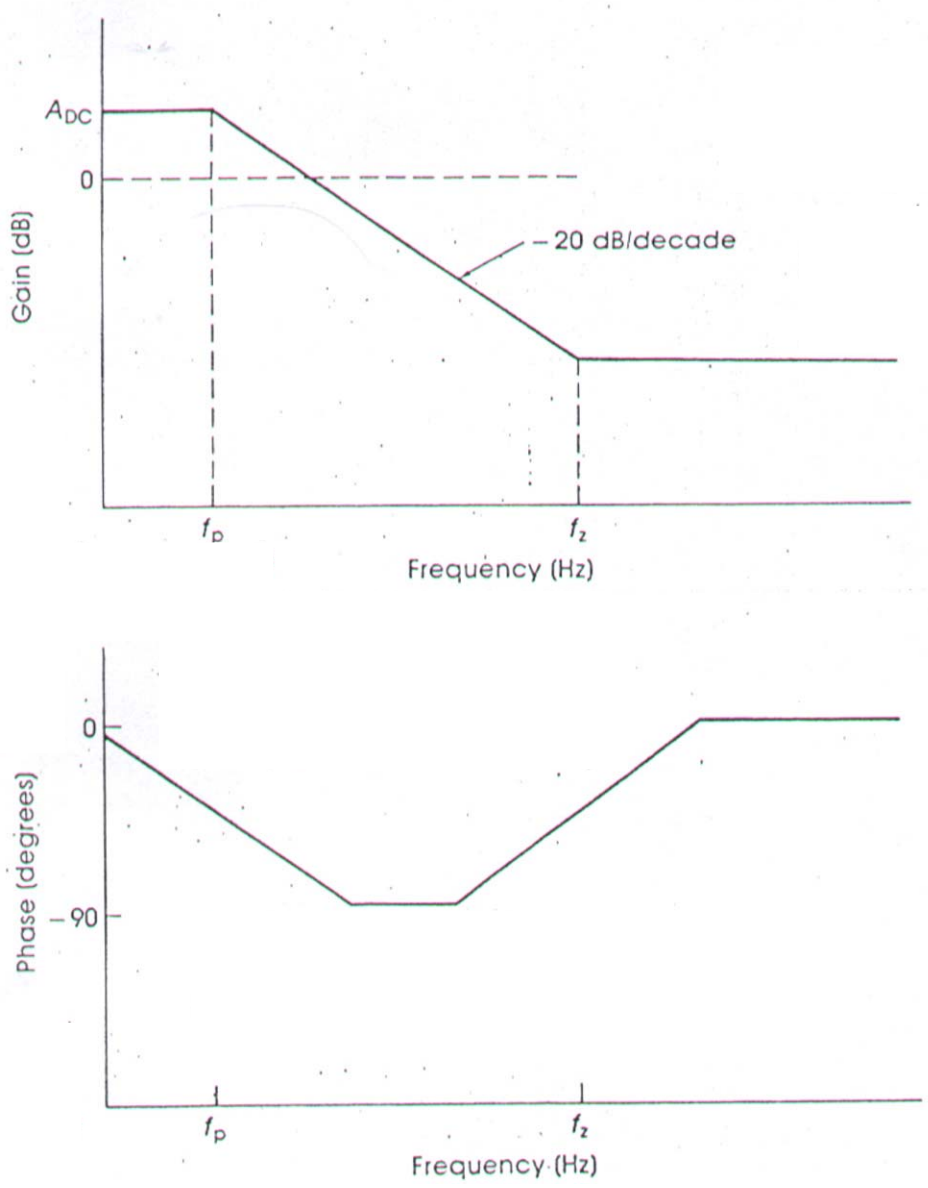
- *The representative control-to-output transfer function of a discontinous flyback mode converter is shown in Fig. This is applicable to flyback, boost, and buck-boost topologies operating in discontinuous mode, also applicable to forward mode converters with a current control method.*

- *Continous mode flyback converters can be extremely difficult to compensate (due to appearance of a RHP zero in the transfer function) within EA in a voltage-mode control system.*

Next Fig. shows the control-to-output ch. of continuous flyback-mode converters

IV. CONTROL METHODS IN SMPS

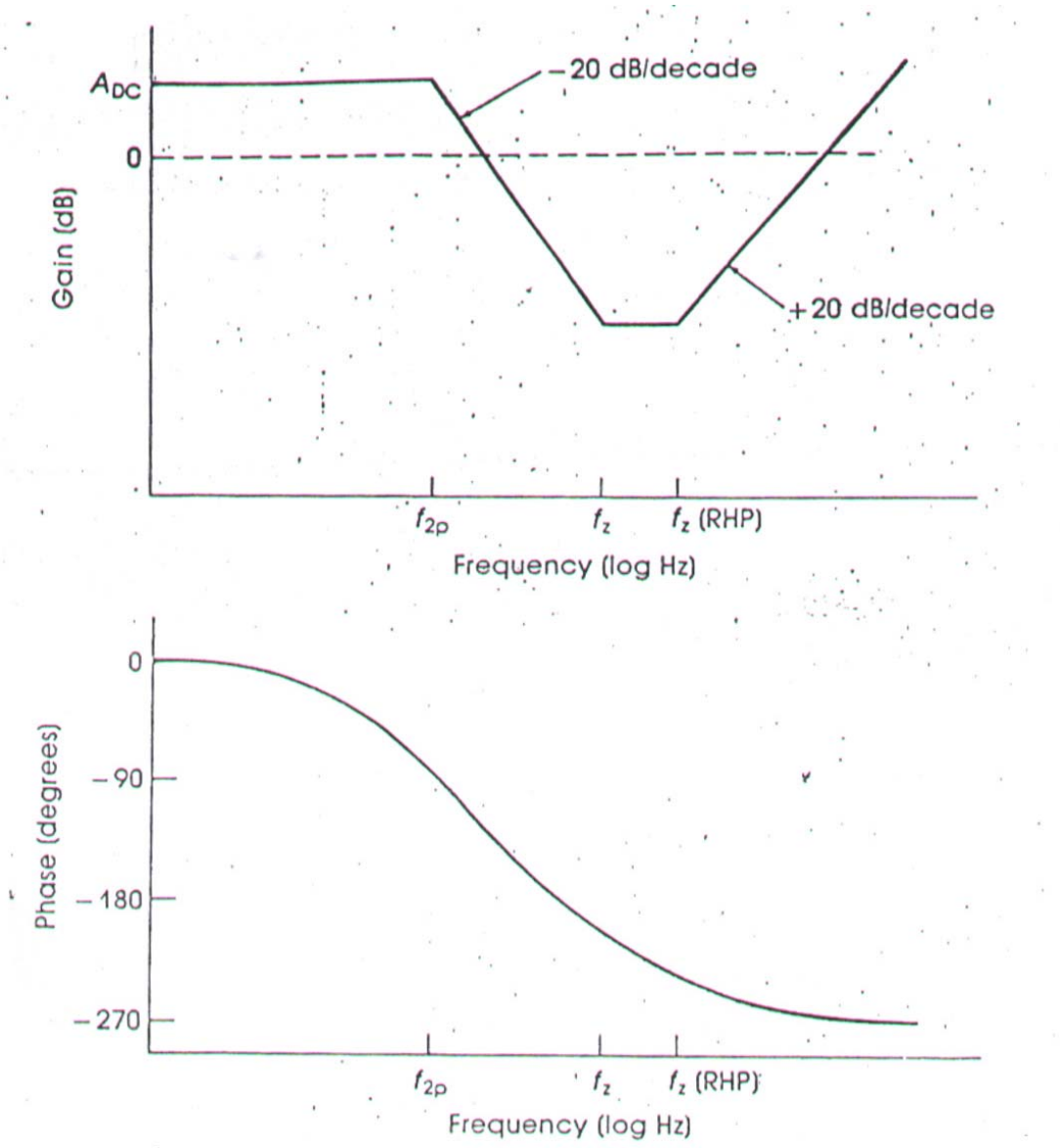
ii- The representative control-to-output transfer function of a discontinuous flyback mode converter:



IV. CONTROL METHODS IN SMPS

ii- *The representative control-to-output transfer function of continuous flyback mode converters:*

RHP zero causes the phase to lag an additional 90° at high f's. This severe phase lag cannot be compensated by a typical error amplifier. Current mode control can help in this case.



IV. CONTROL METHODS IN SMPS

Attempting to compensate for a RHP zero: ***continuous mode flyback SMPS exhibit an additional difficulty to stabilize the system:***

-Difficulty of obtaining a good stability margin, and high frequency transient performance from the continuous mode flyback and boost converters.

-For stable operation of such converters, it is in general necessary to roll off the gain of the control circuits at much lower frequency than in the case of buck-derived topologies.

-A Bode plot of the RHP zero has the characteristic of rising 20 dB/dec gain and a 90 deg. phase lag., instead of phase lead.

-It is considered impossible to compensate this effect by normal loop compensation methods, and the designer is obliged to roll off the gain at a lower frequency, giving a poor transient response.

IV. CONTROL METHODS IN SMPS

Attempting to compensate for a RHP zero: ***continuous mode flyback SMPS exhibit an additional difficulty to stabilize the system:***

- The RHP zero is best explained by considering the transient action of continuous mode flyback converters.

-In this type of circuit, the transformer secondary current is not continuous, it flows only during flyback period, when the power switch is off .

-When a transient load is applied to the output, the first action of the control circuit will be to increase the on-period of the switch so as to increase the input current in the primary inductance.

-However, the large primary inductance will prevent any rapid increase in primary current, and several cycles are needed to reach the final value.

IV. CONTROL METHODS IN SMPS

Attempting to compensate for a RHP zero: ***continuous mode flyback SMPS exhibit an additional difficulty to stabilize the system:***

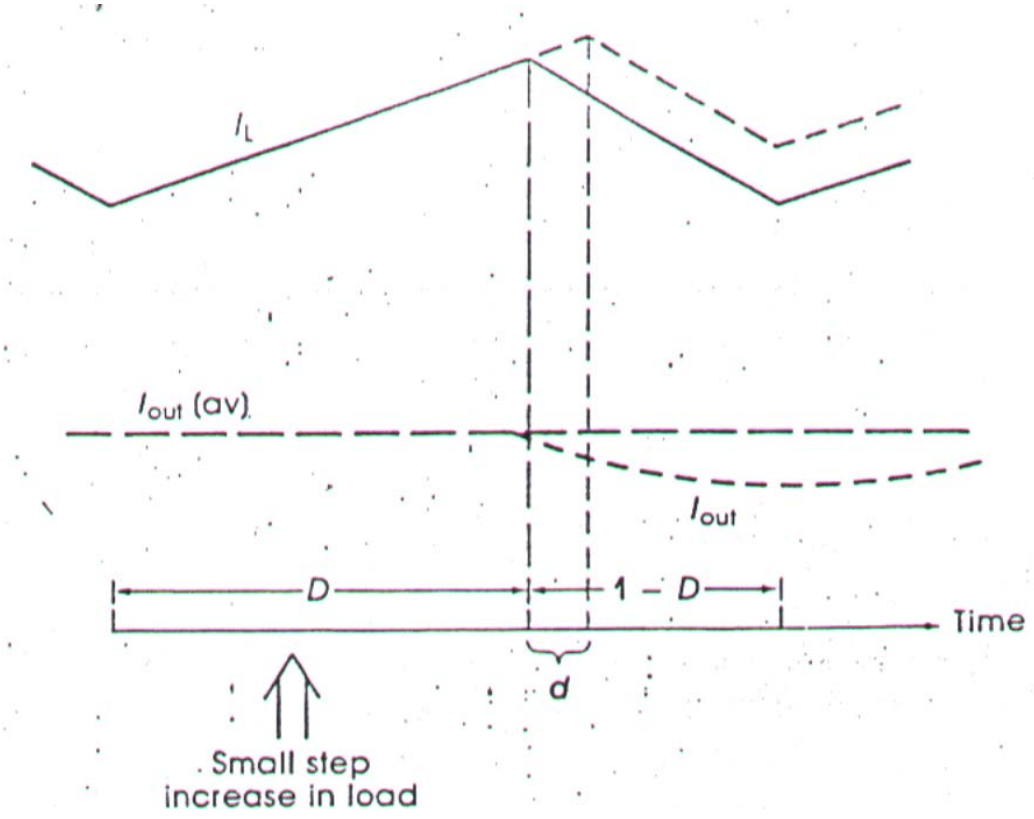
- The first effect of increasing the 'on' period is to reduce the flyback period. Since the primary current, and hence flyback current will not change much in the first few cycles, the mean output current will immediately decrease (rather than increasing as required).

-This reverses the normal control action during the transient, giving an additional 180 deg. of phase shift (this is the cause of RHP zero).

-The only cure for this effect is to change the pulse width slowly, over a large number of cycles so that the inductor current can follow the change. Under these conditions, the transient response will be poor.

IV. CONTROL METHODS IN SMPS

Attempting to compensate for a RHP zero: ***continuous mode flyback SMPS exhibit an additional difficulty to stabilize the system:***



Physical manifestation of a RHP in continuous mode flyback converters

IV. CONTROL METHODS IN SMPS

Common error amplifier compensation techniques:

- The purpose of adding compensation to the error amplifier is to counteract some of the gains and phases contained in the control-to-output transfer function that could adversely affect the stability of the SMPS. The ultimate goal is to make the overall closed loop transfer function satisfy the stability criteria.

- This is to avoid having the closed loop phase any closer to 360° than the desired phase margin anywhere where the gain is greater than unity. It is also desirable to have the slope of the gain at cross over point with a value of –20dB/dec. Phase margins of 45 to 60° are considered safe values, that yield well-damped transient load responses.

IV. CONTROL METHODS IN SMPS

Three other considerations that affect the final SMPS performance are:

-The overall gain crossover frequency should be as high as possible in order to minimize the dynamic transient load response time.

- The gain of the error amplifier at DC (0 Hz) should be as high as possible to ensure that the SMPS exhibits good load regulation.

- A good practice is to make the average slope of the compensated closed loop gain function close to –20 dB/dec.

Real world opamps exhibit a dc gain of 80 – 110 dB. They also have a single pole with fc: 10 – 100 Hz, and a gain roll-off of –20 dB/ dec.

IV. CONTROL METHODS IN SMPS

Common error amplifier compensation techniques:

1. Single-pole compensation ***(used for converter topologies that exhibit a minimal phase shift prior to anticipated gain crossover point). This includes forward mode regulators such as buck, push-pull, half- and full-bridge using either voltage or current mode control techniques.***

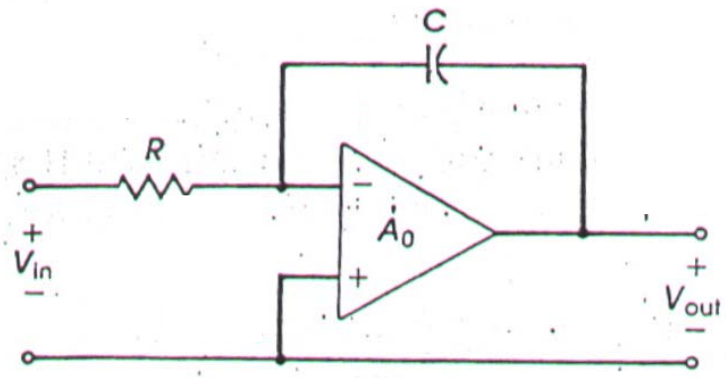
2. Zero pole-pair compensation ***(used for converters that exhibit a single filter pole at low f, and a max. phase shift of 90°: e.g. boost, buck-boost, flyback in the discontinuous mode of operation; and forward mode converters with current mode control)***

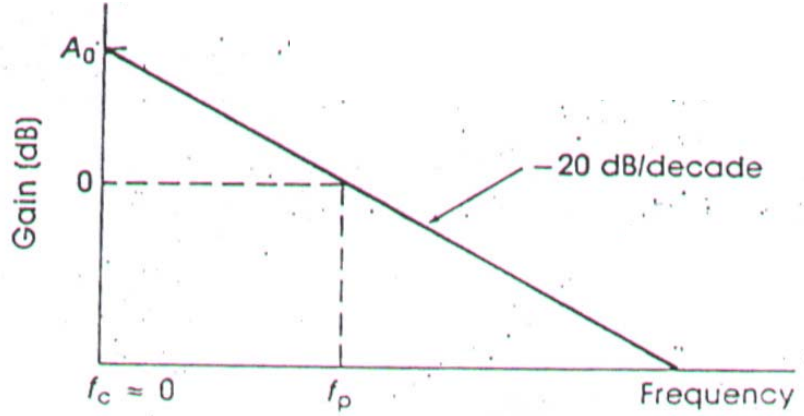
3. Two-pole, two-zero compensation ***(for SMPS that exhibit –40dB/dec roll-off above the poles of output filter and -180° phase lag., in forward mode converters using voltage–mode control).***

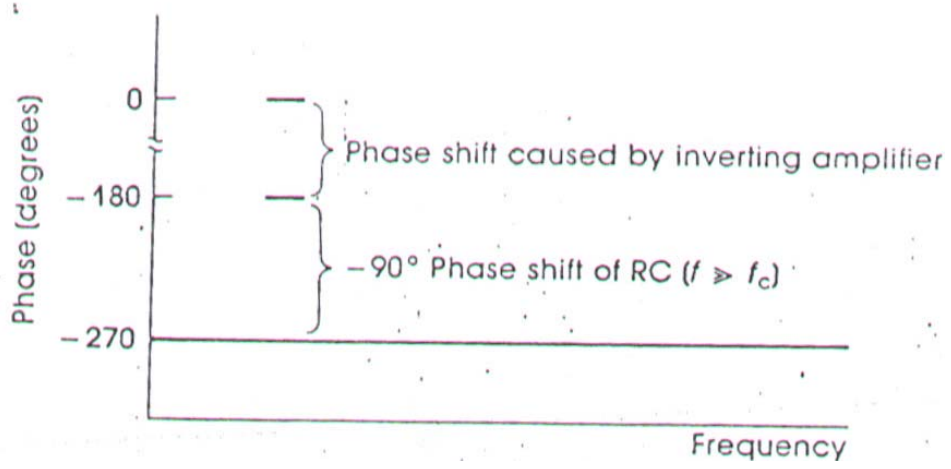
IV. CONTROL METHODS IN SMPS

Common error amplifier compensation techniques:

1. Single-pole compensation (Type 1):



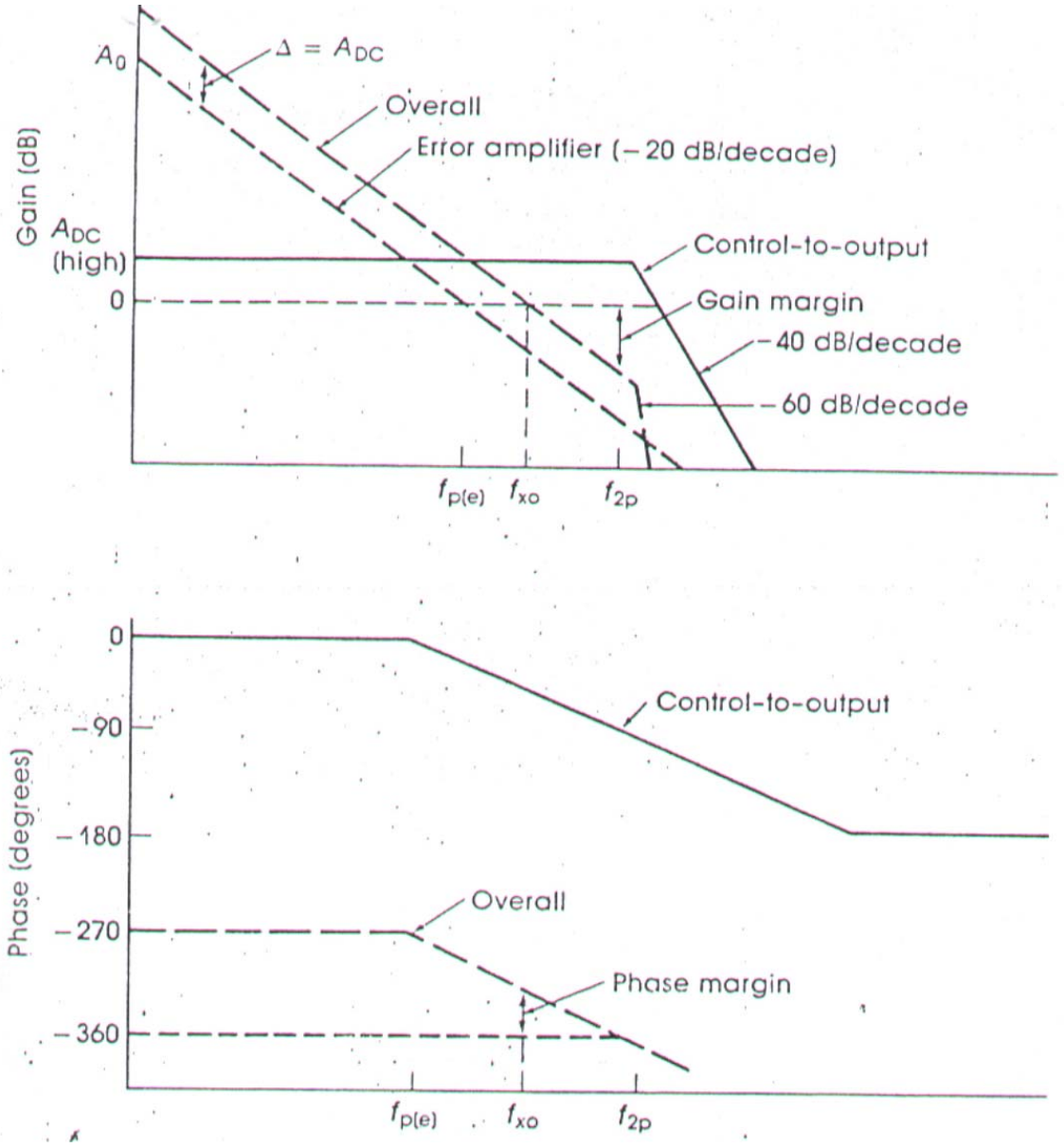




IV. CONTROL METHODS IN SMPS

Forward mode regulator using single-pole compensated error amplifier:

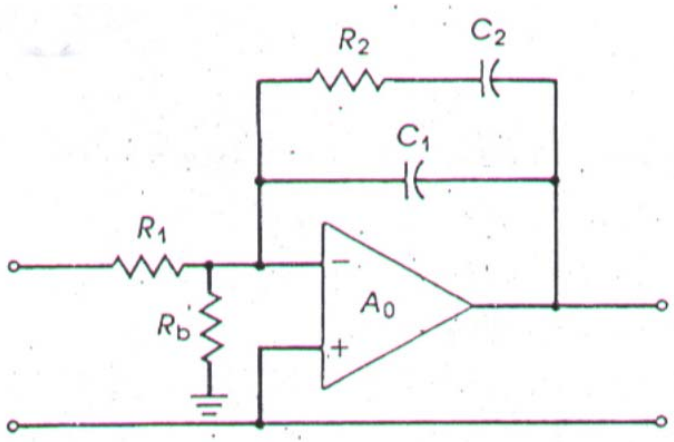
$f_{xo} = 1/(2\pi RC)$

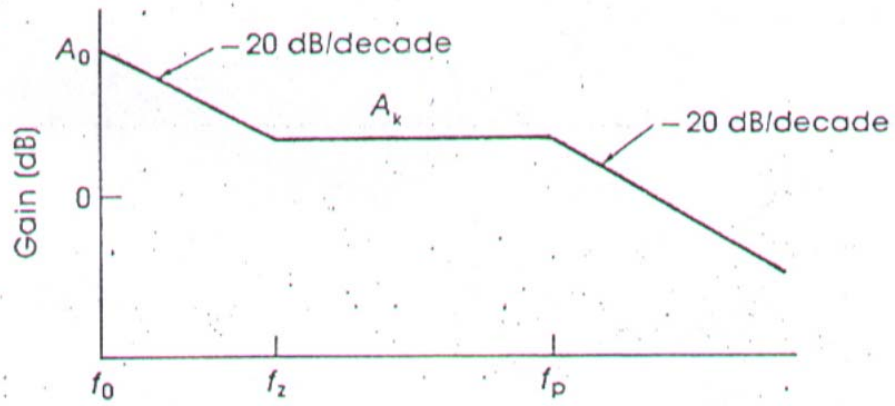


IV. CONTROL METHODS IN SMPS

Common error amplifier compensation techniques:

2. Zero pole-pair compensation (Type 2) :

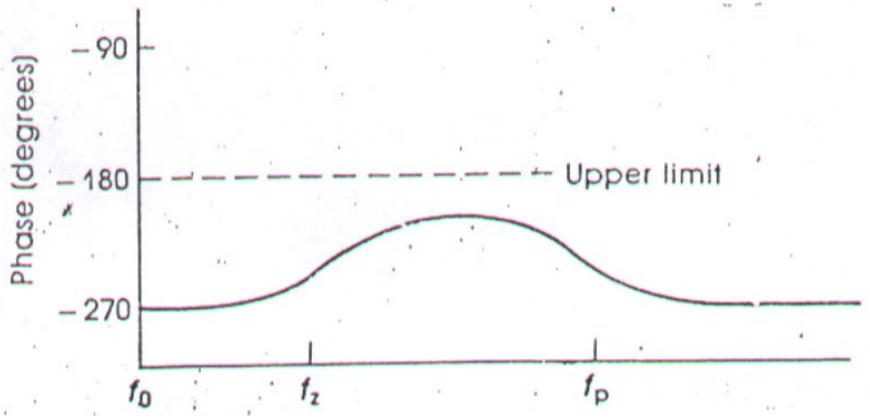




$$A_k = R_2 / R_1$$

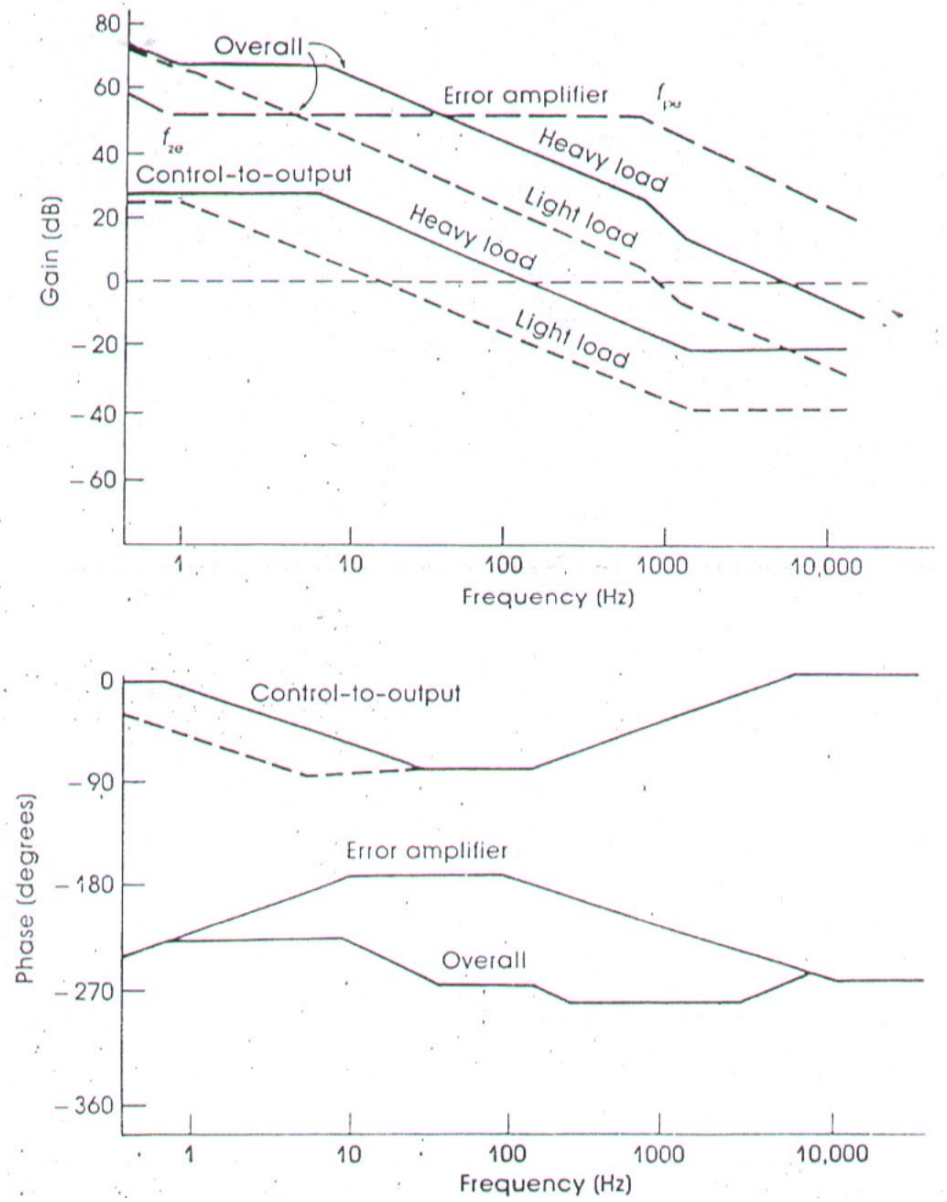
$$f_z = 1 / 2\pi R_2 C_2$$

$$f_p = 1 / 2\pi R_2 C_1$$



IV. CONTROL METHODS IN SMPS

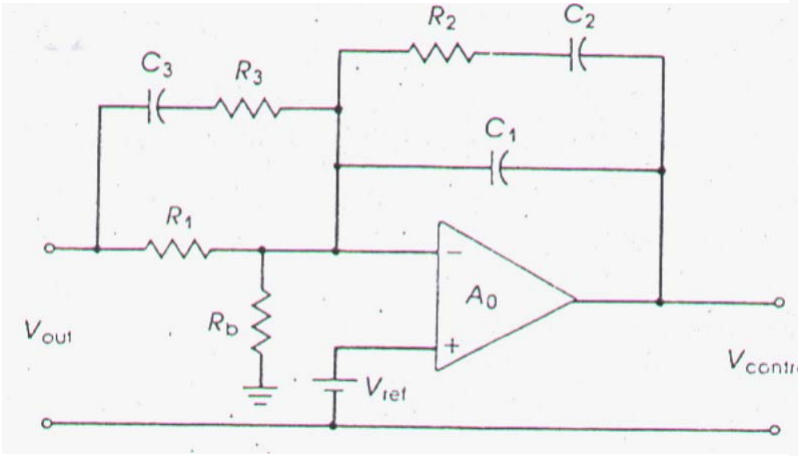
2. Zero pole-pair compensation:

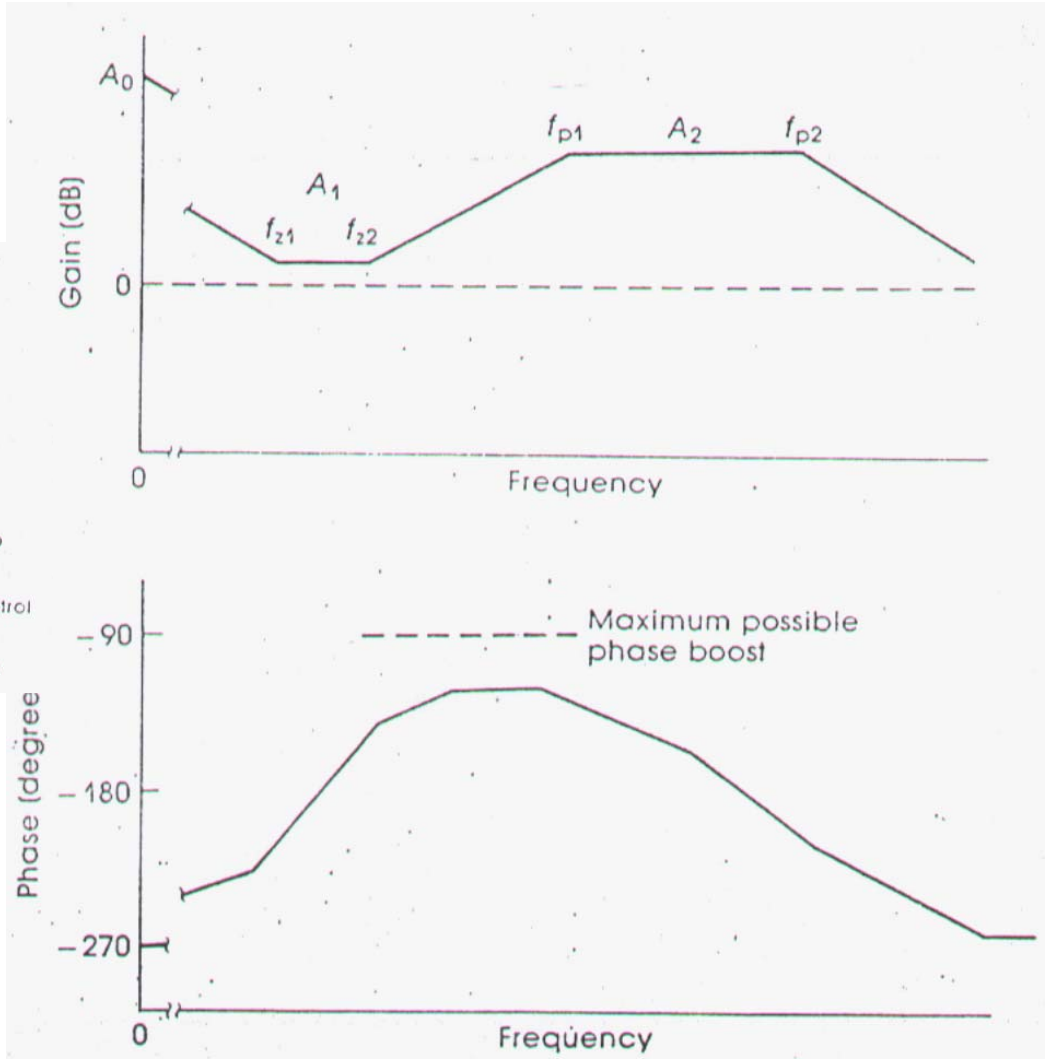


IV. CONTROL METHODS IN SMPS

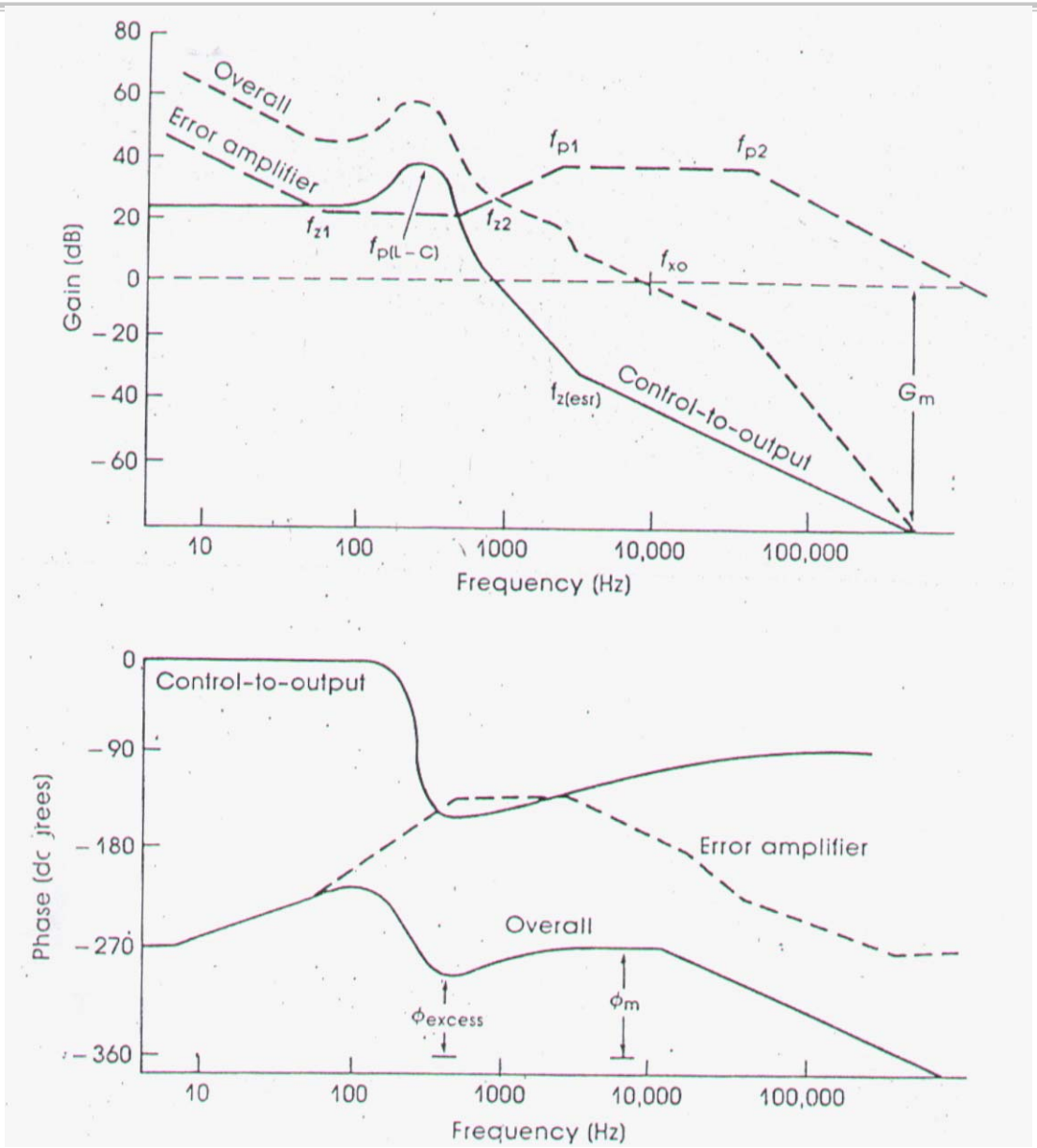
Common error amplifier compensation techniques:

3. Two-pole, two-zero compensation (Type 3) :





IV. CONTROL METHODS IN SMPS



IV. CONTROL METHODS IN SMPS

1. Determine the crossover frequency by $f_{xo} = f_s / 5$

2. Determine the gain needed to bring the control-to-output transfer function up to 0 dB at the desired crossover frequency.

3. If both zeros are placed at the same frequency, then they should be placed at: $f_{z1} = f_{z2} = f_{p(L\text{-}C)} / 2$. The resulting margin in excess phase is 45°.

To deemphasize the Q of L-C filter on overall gain function, the lower zeros can be separated: $f_{z1} = f_p/5$. The second zero is placed just above the LC poles such that: $f_p < f_{z2} < 1.2 f_p$.

4. Place f_{p1} at the lowest expected zero caused by the esr. $f_{p1} = f_{z(esr)}$

IV. CONTROL METHODS IN SMPS

5. Place f_{p2} above the overall crossover frequency at nearly:
$f_{p2} > 1.5\, f_{x0}$

Now, the component values of the compensation network can be determined.

The gain of the first zero f_{z1} is $A_1 = A_{x0} + 20 \log (f_{z2}/f_{p1})$, in dB

Other component values are:

$C_1 = 1 / (2\pi f_{xo} A_1 R_1)$, $R_2 = A_1 R_1$,

$C_3 = 1 / (2\pi f_{z2} R_1)$, $R_3 = R_2/A_2$, $C_2 = 1 / (2\pi f_{z1} R_2)$

IV. CONTROL METHODS IN SMPS

4.4. Examples

Ex-1: A 100 kHz, 50 W Off-Line Half-Bridge SMPS

Input voltage range: 90 V to 130 V at 50 Hz
Output voltage and current: +5V DC at 5 A
Output ripple voltage: 50 mV p-p
Transformer Core: Magnetics EC, F material
Turns ratio: $N_p / N_s = 32 / 2$
Output filter inductor, $L_o = 60\ \mu H$
Output filter capacitor, $C_o = 1000\ \mu F$
Control mode: Voltage mode control

IV. CONTROL METHODS IN SMPS

Error Amplifier Compensation

1. The dominant (lowest-frequency) output filter pole is caused by the +5-V-output L–C filter

$$f_p = 1 / (2\pi\sqrt{LoCo}) \Rightarrow \quad f_p(+5) = 719 \text{ Hz}$$

For tantalum capacitors, the zero caused by the ESR of the capacitor times the value of the capacitor itself can be expected to be about 10 kHz, but to play it safe, a frequency of 8 kHz will be used.

2. The gain exhibited by the power network at DC is

$$A_{DC} = 20 \log\left(\frac{V_{in}}{V_{ramp}} \cdot \frac{N_s}{N_p}\right); \qquad V_{ramp} = 2.4 \text{ V}$$

Low line: $A_{DC} = 17.1$ dB

High line: $A_{DC} = 20.6$ dB

3. For voltage-mode control, forward-mode regulators, a two-pole–two-zero type of compensation is recommended

IV. CONTROL METHODS IN SMPS

4. The overall gain crossover frequency is approximately

$$f_{xo} = \frac{f_s}{5} = \frac{100 \text{ kHz}}{5} = 20 \text{ kHz} \quad \text{(maximum)}$$

5. The gain needed to bring the control-to-output curve up to 0 dB at the overall crossover frequency is 29 dB (see Fig. X) (or a gain of 28.1).
6. The location of the two low-frequency zeros (f_z) will be at one-half the pole frequency of the output filter (the poles will coincide):

$$f_z = \frac{f_{L-C}}{2} = \frac{719 \text{ Hz}}{2} \approx 360 \text{ Hz}$$

IV. CONTROL METHODS IN SMPS

7. The location of the first high-frequency pole is at the worst-case ESR zero frequency, which is approximately 8 kHz.
8. The location of the second high-frequency pole should be

$$f_{p2} = 1.5f_{xo} = 1.5(20\text{ kHz}) = 30\text{ kHz}$$

9. The gain needed at the location of the two compensating zeros is

$$A_1 = A_2 + 20\log\left(\frac{f_{z2}}{f_{p1}}\right)$$

$$= 29.2\text{ dB} + 20\log\left(\frac{360\text{ Hz}}{8{,}000\text{ Hz}}\right)$$

$$= 2.3\text{ dB} \quad \text{(or a gain of 1.3)}$$

10. Find C_1 (R_{in} or $R_1 = 1.2\text{ k}\Omega$):

$$C_1 = \frac{1}{2\pi A_1 \cdot f_{xo} \cdot R_1}$$

$$= \frac{1}{2\pi(2)(2 \times 10^4\text{ Hz})(1.2\text{ k}\Omega)}$$

$$= 3300\text{ pF (rounded)}$$

IV. CONTROL METHODS IN SMPS

11. Find R_2:

$$R_2 = A_1(R_1) = 1.3(1.2\ \text{k}\Omega) = 1.5\ \text{k}\Omega$$

12. Find R_3:

$$R_3 = \frac{R_2}{A_2} = \frac{1.5\ \text{k}\Omega}{28.1} = 51\ \Omega$$

13. Find C_2:

$$C_2 = \frac{1}{2\pi f_{z2} \cdot R_2}$$

$$= \frac{1}{2\pi(360\ \text{Hz})(1.5\ \text{k}\Omega)}$$

$$= 0.29\ \mu\text{F} \rightarrow 0.27\ \mu\text{F}$$

14. Find C_3:

$$C_3 = \frac{1}{2\pi f_z \cdot R_1}$$

$$= \frac{1}{2\pi(360\ \text{Hz})(1.2\ \text{k}\Omega)}$$

$$= 0.36\ \mu\text{F}$$

IV. CONTROL METHODS IN SMPS

Bode Plots

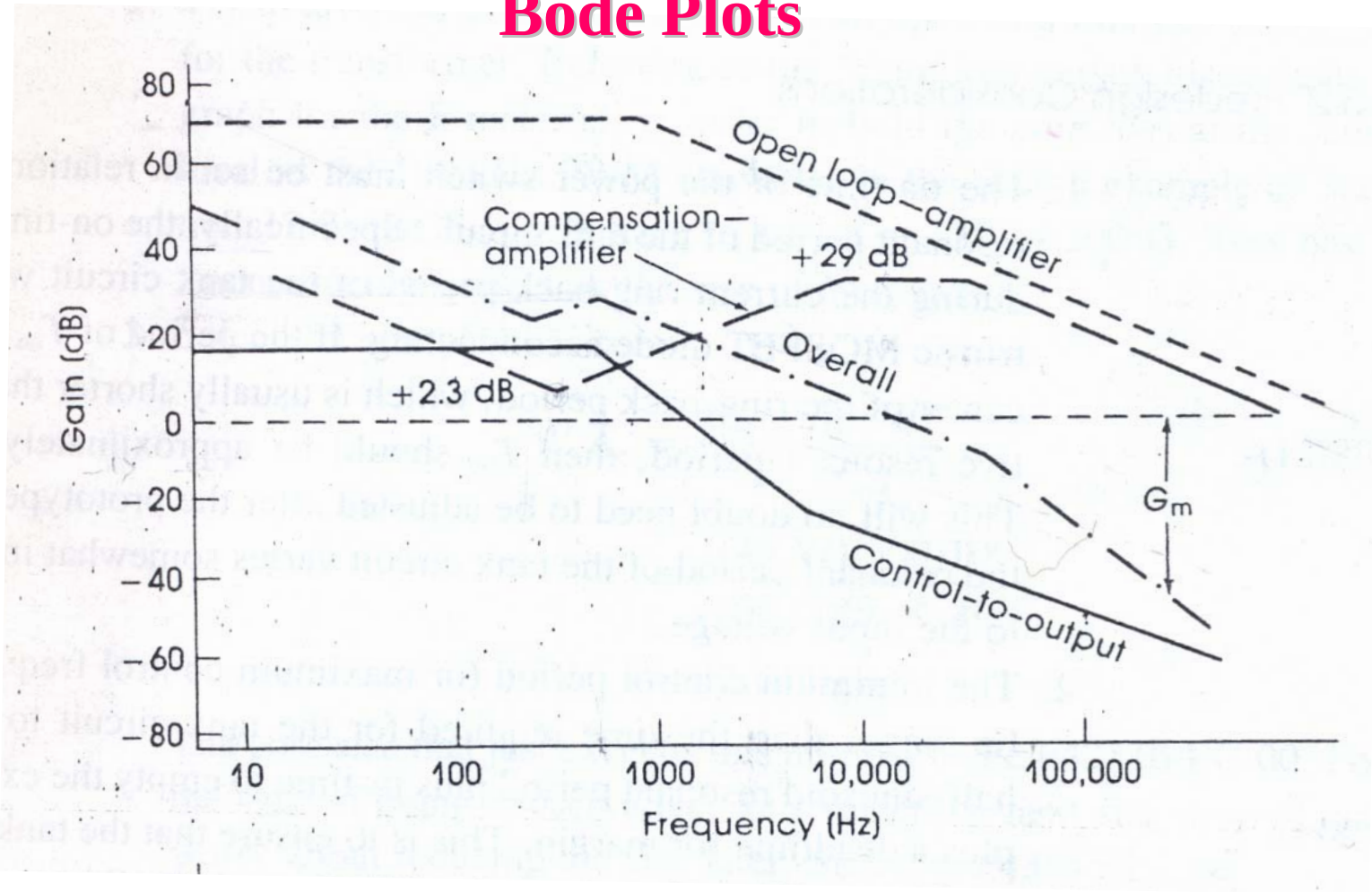
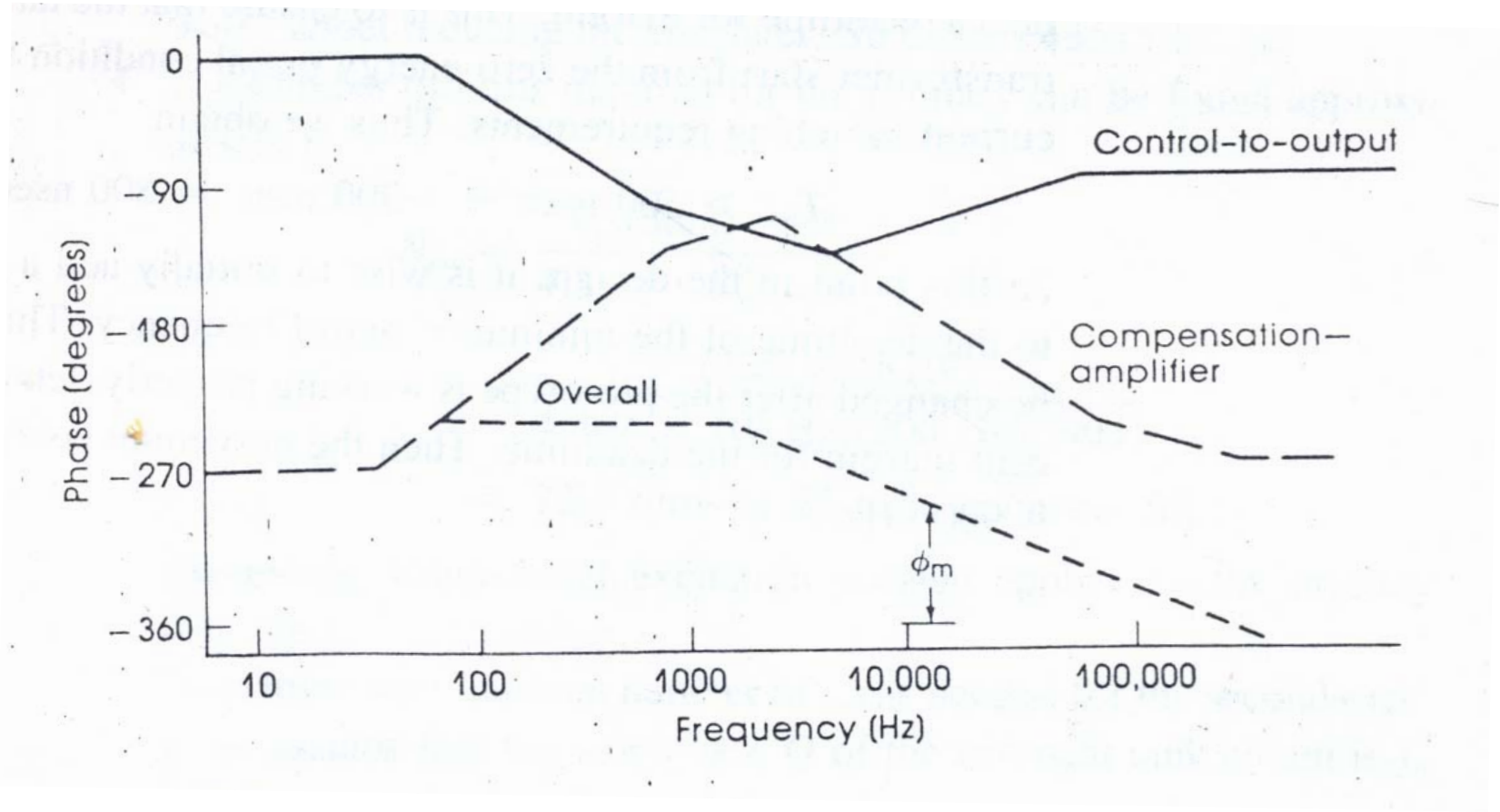


Fig. X.

IV. CONTROL METHODS IN SMPS



IV. CONTROL METHODS IN SMPS

Stability Analysis Using K-Factor

- In previous sections, practical mathematical tools were developed to design compensated error amplifiers to be used with various SMPS topologies.

- Another powerful mathematical tool, known as K-factor makes the analysis and design of error amplifiers easier.

-The K-factor is a tool for defining the shape and characteristics of a transfer function.

IV. CONTROL METHODS IN SMPS

Stability Analysis Using K-Factor

- K-factor is a measure of the reduction of the gain at low f, and increase at high f, by controlling the location of the poles and zeros of the feedback amplifier Bode Plot, in relationship to crossover frequency.

- For Type 1 compensation, K = 1. This is due to a total lack of phase boost, or corresponding increase or decrease in gain.

IV. CONTROL METHODS IN SMPS

-For compensation types 2 and 3, the zero is placed a factor of K below the loop crossover frequency, and the pole a factor of K above.

-Since f is the geometric mean, $f = (f_z f_p)^{1/2}$, of the zero and pole locations, peak phase boost will occur at the crossover frequency. For either case, as K is increasing so is the phase boost.

-The phase boost due to a zero-pole pair is the inverse tangent ratio of meaurement frequency to zero or pole f.

IV. CONTROL METHODS IN SMPS

- The total phase shift is then the sum of all individual zero and pole phase shifts.

For type 2 amplifiers, the boost at frequency f is:

$$\text{Boost} = \tan^{-1}(K) - \tan^{-1}(K)\tan^{-1}(1/K)$$

$$\Rightarrow K = \tan\left(\left(\text{Boost}/2\right) + 45\right) \qquad (*)$$

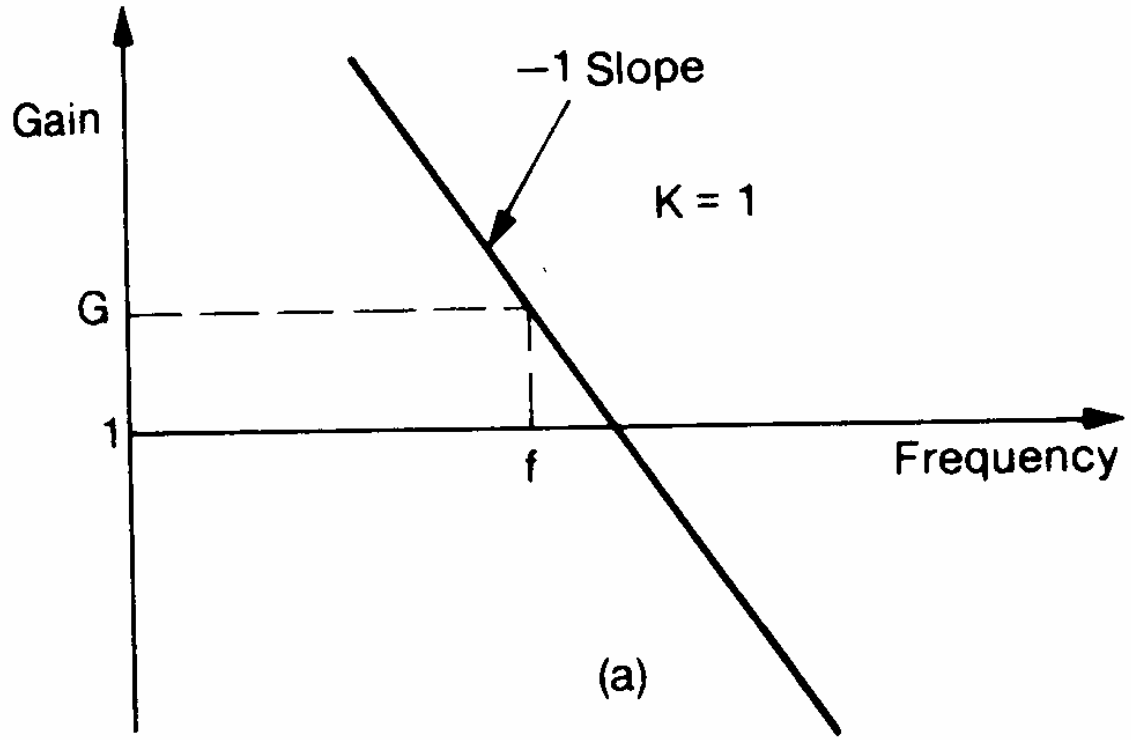
For type 3 amplifiers, the boost at frequency f is:

$$\text{Boost} = \tan^{-1}(K) - \tan^{-1}(1/K)$$

$$\Rightarrow K = \left(\tan\left(\text{Boost}/4\right) + 45\right)^2 \qquad (**)$$

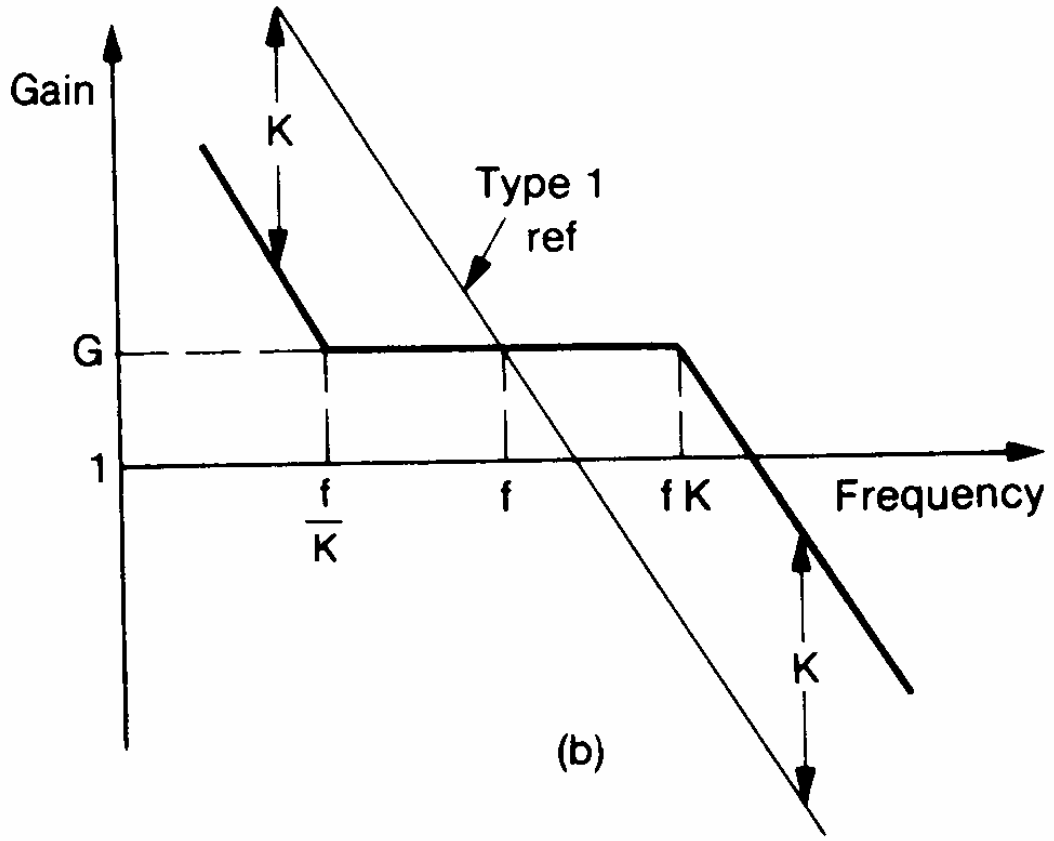
(See Fig. below)

IV. CONTROL METHODS IN SMPS



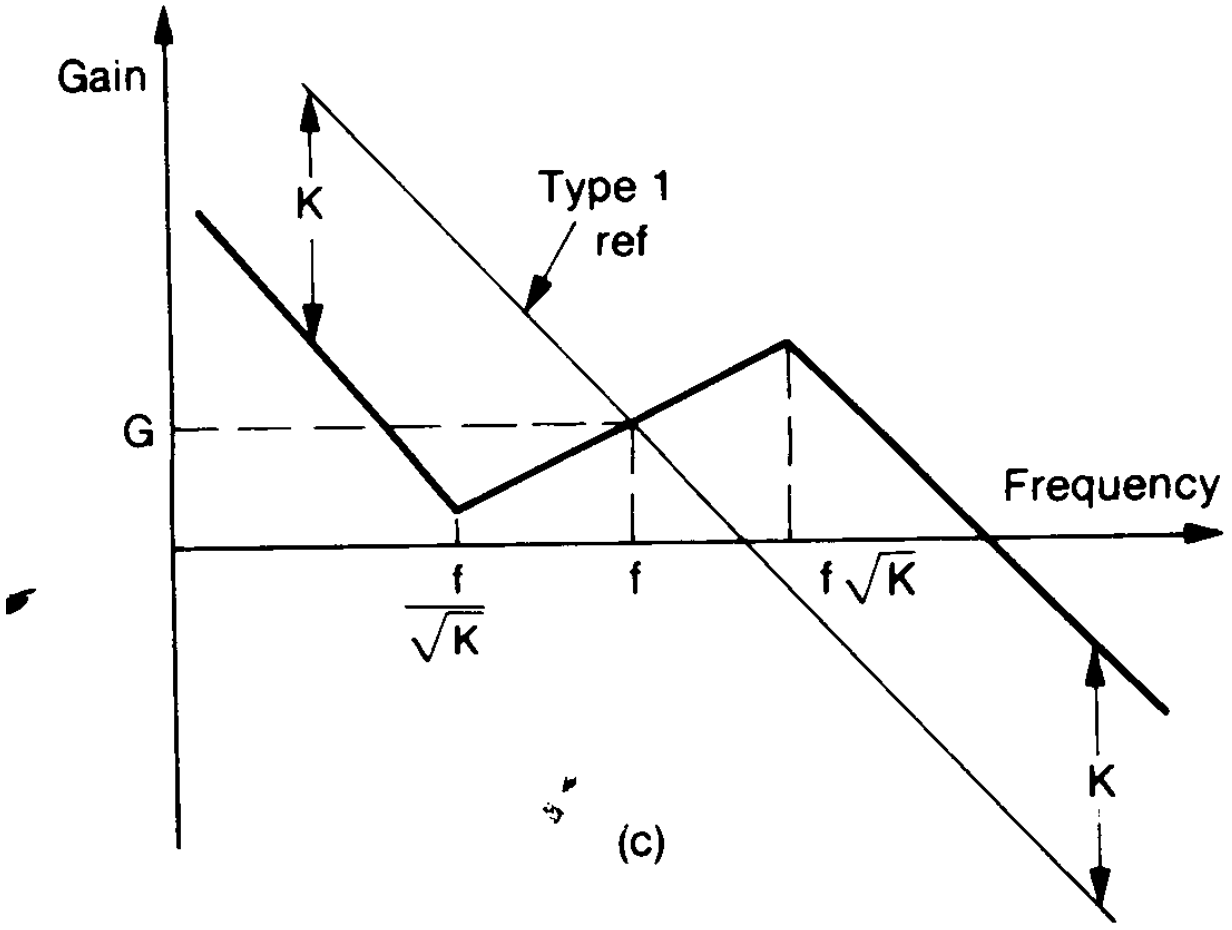
Bode plot characteristics of Type 1 compensation

IV. CONTROL METHODS IN SMPS



Bode plot characteristics of Type 2 compensation

IV. CONTROL METHODS IN SMPS



Bode plot characteristics of Type 3 compensation

IV. CONTROL METHODS IN SMPS

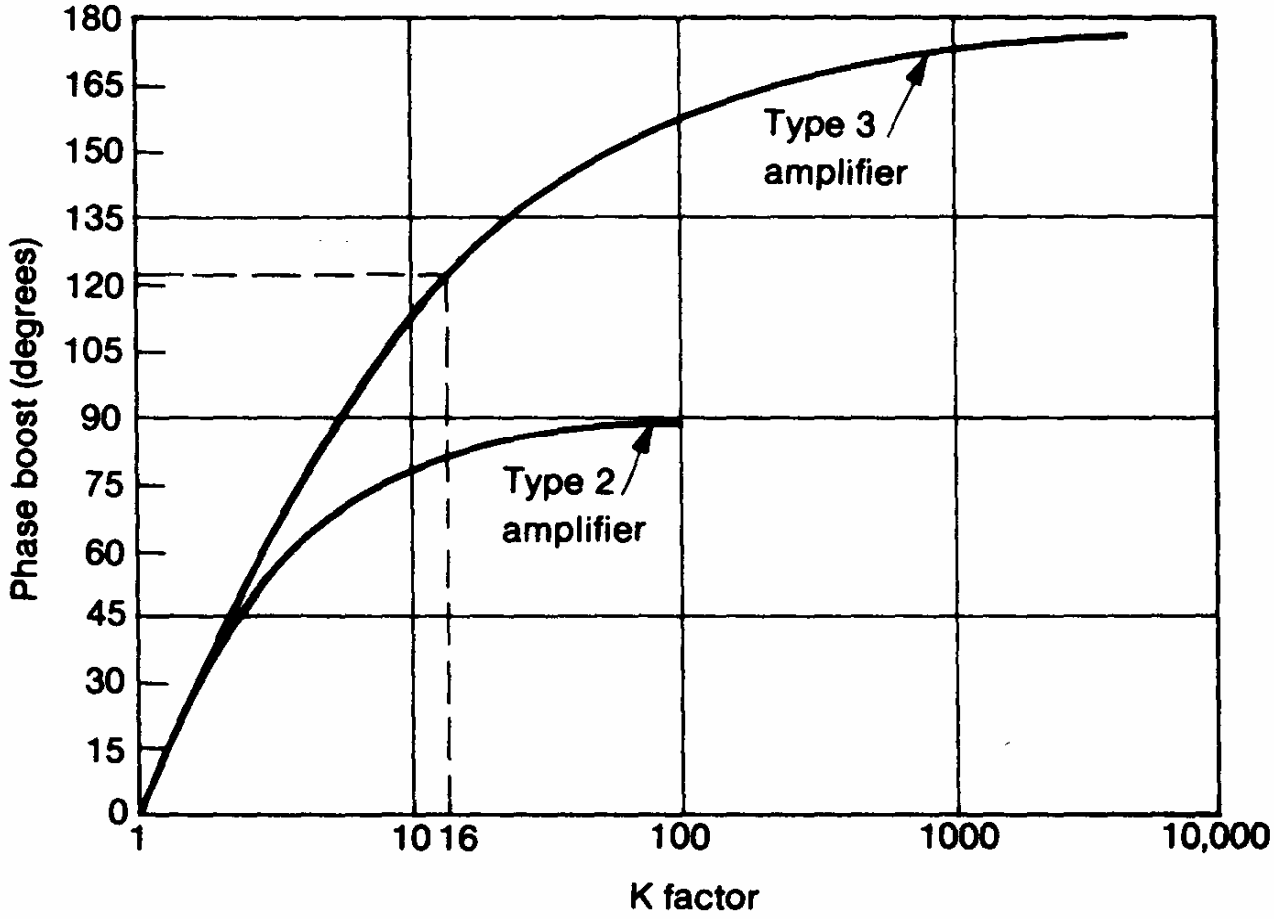


Fig.A. Phase boost vs K factor for Type 2 and Type 3 compensation

IV. CONTROL METHODS IN SMPS

Step 1: *Make a Bode plot of the modulator.* A typical modulator Bode plot showing both gain and phase characteristics is depicted in Fig. **(Control-to-output transfer function)**

Step 2: *Choose a crossover frequency.* The crossover frequency is the point where you want the overall loop gain to be unity. Remember that the higher the crossover frequency, the better the transient response of the power supply. However, practical limitations restrict the range of the crossover frequency. The theoretical limit is half the switching frequency, but practical considerations have proven that a crossover frequency figure of less than one-fifth of the clock frequency is a good choice.

Step 3: *Choose the desired phase margin.* This margin is the amount of phase desired at unity gain, as shown in Fig. **(Slide 47).** Phase margin may have a range of 30 to 90°, with 60° being a good compromise.

IV. CONTROL METHODS IN SMPS

Step 4: *Determine required amplifier gain.* This gain G is the required amplifier gain at crossover and must equal the modulator loss. When expressed in decibels, the amplifier gain is simply the negative of the modulator gain; otherwise, amplifier gain = 1/modulator gain.

Step 5: *Calculate the required phase boost.* The amount of phase boost required from the zero-pole pair in the amplifier is given by the formula

$$\text{Boost} = M - P - 90°$$

where M = desired phase margin, degrees
P = modulator phase shift, degrees

Step 6: *Choose the amplifier type.* Choose amplifier type 1 when no boost is required, amplifier type 2 when the required boost is less than 90°, and amplifier type 3 when the required phase boost is less than 180°.

IV. CONTROL METHODS IN SMPS

Step 7: *Calculate the K factor*. The K factor may be calculated using either Eq. (*) and (**) or directly from the curves of Fig. A. For amplifier type 1, $K = 1$. Location of the transfer function poles and zeros will determine the circuit values. The pole at the origin causes the initial -1 gain slope, and the frequency where this line crosses or would have crossed the 0-dB line (unity gain), is the unity gain frequency, UGF.

The following equations provide the component values of each amplifier type.

Type 1

$$C = \frac{1}{2\pi fGR}$$

IV. CONTROL METHODS IN SMPS

Type 2

$$\text{UGF} = \frac{1}{2\pi R_1(C_1 + C_2)}$$

$$C_2 = \frac{1}{2\pi f G K R_1}$$

$$C_1 = C_2(K^2 - 1)$$

$$R_2 = \frac{K}{2\pi f C_1}$$

Type 3

$$\text{UGF} = \frac{1}{2\pi R_1(C_1 + C_2)}$$

$$C_2 = \frac{1}{2\pi f G R_1}$$

$$C_1 = C_2(K - 1)$$

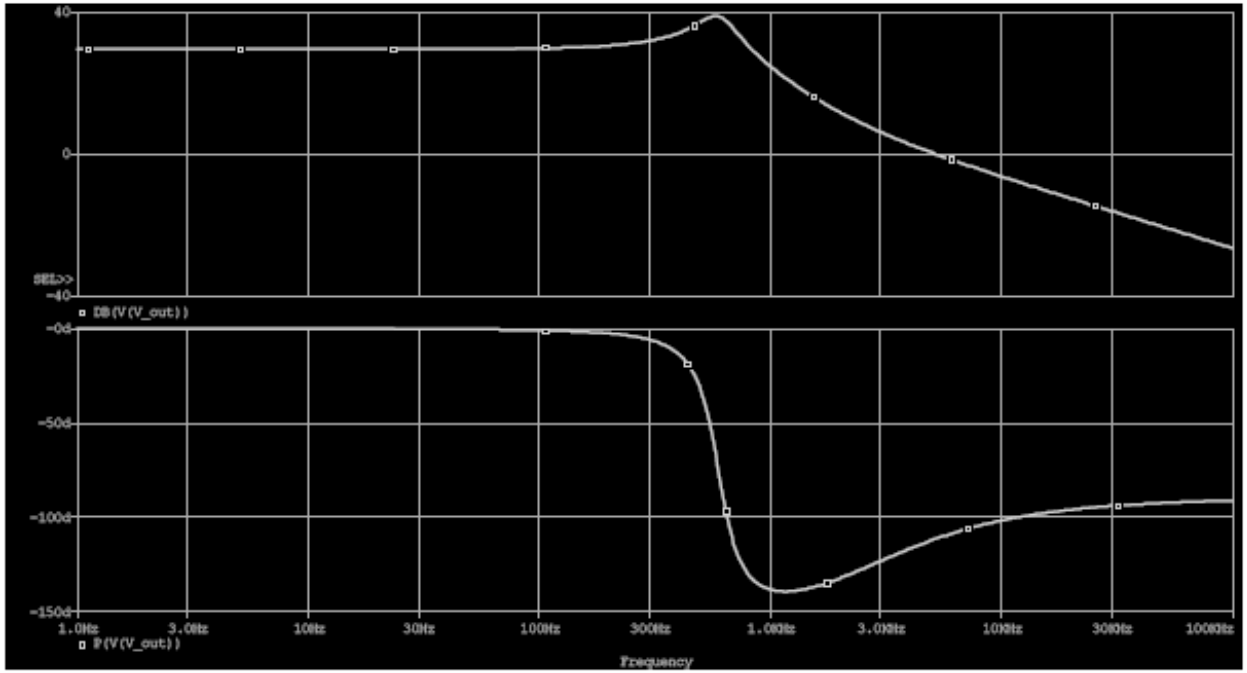
$$R_2 = \frac{\sqrt{K}}{2\pi f C_1}$$

$$R_3 = \frac{R_1}{K - 1}$$

$$C_3 = \frac{1}{2\pi f \sqrt{K} R_3}$$

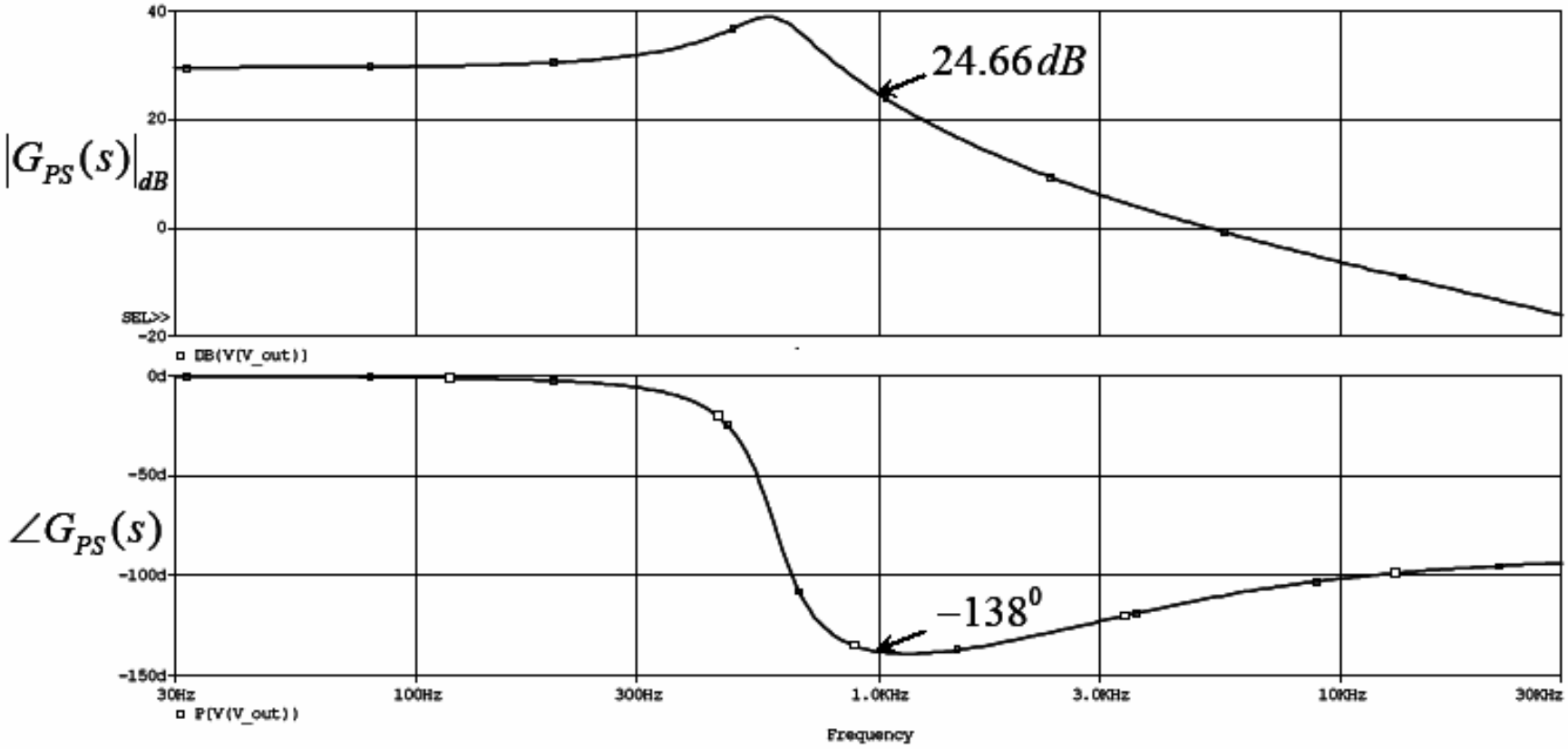
IV. CONTROL METHODS IN SMPS

▲ **Example 4-2** A Buck converter has the following parameters and is operating in CCM: $L = 100\,\mu H$, $C = 697\,\mu F$, $r = 0.1\Omega$, $f_s = 100\,kHz$, $V_{in} = 30V$, and $P_o = 36W$. The duty-ratio D is adjusted to regulate the output voltage $V_o = 12V$. Obtain both the gain and the phase of the power stage $G_{PS}(s)$ for the frequencies ranging from 1 Hz to 100 kHz.



IV. CONTROL METHODS IN SMPS

The gain and phase of the power stage



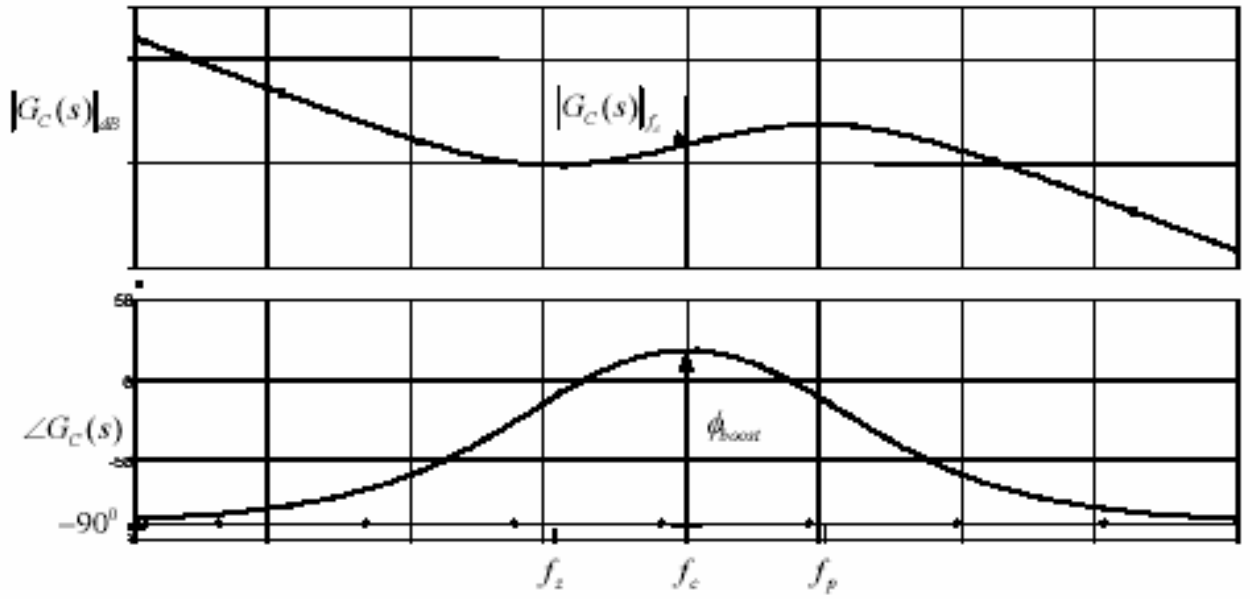
IV. CONTROL METHODS IN SMPS

▲ **Example 4-3** Design the feedback controller for the Buck converter described in Example 4-2. The PWM-IC is as described in Example 4-1. The output voltage-sensing network in the feedback path has a gain $k_{FB} = 0.2$. The steady state error is required to be zero and the phase margin of the loop transfer function should be 60^0 at as high a crossover frequency as possible.

1. The crossover frequency f_c of the open-loop gain is as high as possible to result in a fast response of the closed-loop system.
2. The phase angle of the open-loop transfer function has the specified phase margin, typically 60^0 at the crossover frequency so that the response in the closed-loop system settles quickly without oscillations.
3. The phase angle of the open-loop transfer function should not drop below -180^0 at frequencies below the crossover frequency.

IV. CONTROL METHODS IN SMPS

$$G_c(s) = \frac{k_c}{s} \underbrace{\frac{(1+s/\omega_z)^2}{(1+s/\omega_p)^2}}_{phase-boost}$$



Bode plot of $G_C(s)$

IV. CONTROL METHODS IN SMPS

Step 1: Choose the Crossover Frequency. Choose f_c to be *slightly* beyond the L-C resonance frequency $1/(2\pi\sqrt{LC})$, which in this example is approximately 600 Hz. Therefore, we will choose $f_c = 1\,\text{kHz}$. This ensures that the phase angle of the loop remains greater than -180^0 at all frequencies.

Step 2: Calculate the needed Phase Boost. The desired phase margin is specified as $\phi_{PM} = 60^0$. The required phase boost ϕ_{boost} at the crossover frequency is calculated as follows, noting that G_{PWM} and k_{FB} produce zero phase shift:

$$\angle G_L(s)\big|_{f_c} = \angle G_{PS}(s)\big|_{f_c} + \angle G_C(s)\big|_{f_c} \qquad \text{(from Eq. 4-2)} \qquad (4\text{-}19)$$

$$\angle G_L(s)\big|_{f_c} = -180^o + \phi_{PM} \qquad \text{(from Eq. 4-3)} \qquad (4\text{-}20)$$

$$\angle G_C(s)\big|_{f_c} = -90^o + \phi_{boost} \qquad \text{(from Fig. 4-11)} \qquad (4\text{-}21)$$

Substituting Eqs. 4-20 and 4-21 into Eq. 4-19,

$$\phi_{boost} = -90^o + \phi_{PM} - \angle G_{PS}(s)\big|_{f_c} \qquad (4\text{-}22)$$

In Fig. 4-10, $\angle G_{PS}(s)\big|_{f_c} \simeq -138^0$, substituting which in Eq. 4-22 yields the required phase boost $\phi_{boost} = 108^o$.

IV. CONTROL METHODS IN SMPS

Step 3: Calculate the Controller Gain at the Crossover Frequency. From Eq. 4-2 at the crossover frequency f_c

$$\left|G_L(s)\right|_{f_c} = \left|G_C(s)\right|_{f_c} \times \left|G_{PWM}(s)\right|_{f_c} \times \left|G_{PS}(s)\right|_{f_c} \times k_{FB} = 1 \qquad (4\text{-}23)$$

In Fig. 4-10, at $f_c = 1kHz$, $\left|G_{PS}(s)\right|_{f_c=1kHz} = 24.66\,dB = 17.1$. Therefore in Eq. 4-23, using the gain of the PWM block given as 0.556,

$$\left|G_C(s)\right|_{f_c} \times \underbrace{0.556}_{\left|G_{PWM}(s)\right|_{f_c}} \times \underbrace{17.1}_{\left|G_{PS}(s)\right|_{f_c}} \times \underbrace{0.2}_{k_{FB}} = 1 \qquad (4\text{-}24)$$

or

$$\left|G_C(s)\right|_{f_c} = 0.5263 \qquad (4\text{-}25)$$

IV. CONTROL METHODS IN SMPS

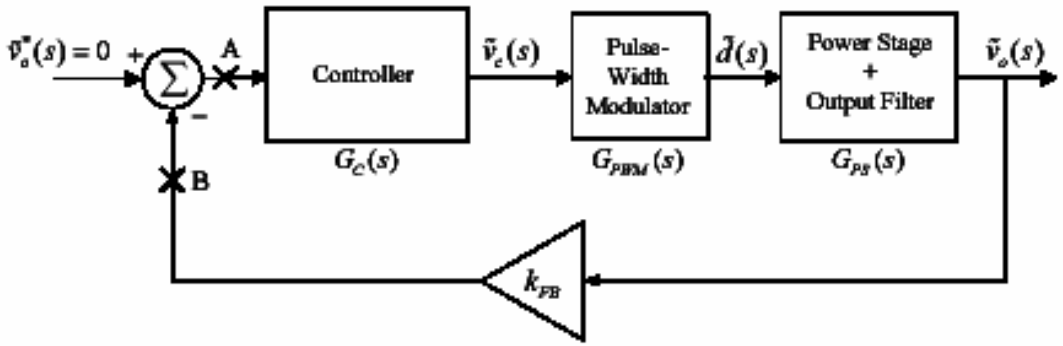


Figure 4-3 Small signal control system representation.

$$G_c(s) = \frac{k_c}{s} \underbrace{\frac{(1+s/\omega_z)^2}{(1+s/\omega_p)^2}}_{phase-boost}$$

$$\sqrt{K} = K_{boost} = \sqrt{\frac{\omega_p}{\omega_z}} \qquad K_{boost} = \tan\left(45^o + \frac{\phi_{boost}}{4}\right)$$

$$f_z = \frac{f_c}{K_{boost}} \qquad f_p = K_{boost} f_c$$

$$k_c = \left|G_C(s)\right|_{f_c} \frac{\omega_z}{K_{boost}}$$

IV. CONTROL METHODS IN SMPS

Implementation of the controller by an op-amp

$$G_c(s) = \frac{k_c}{s} \underbrace{\frac{(1+s/\omega_z)^2}{(1+s/\omega_p)^2}}_{phase-boost}$$

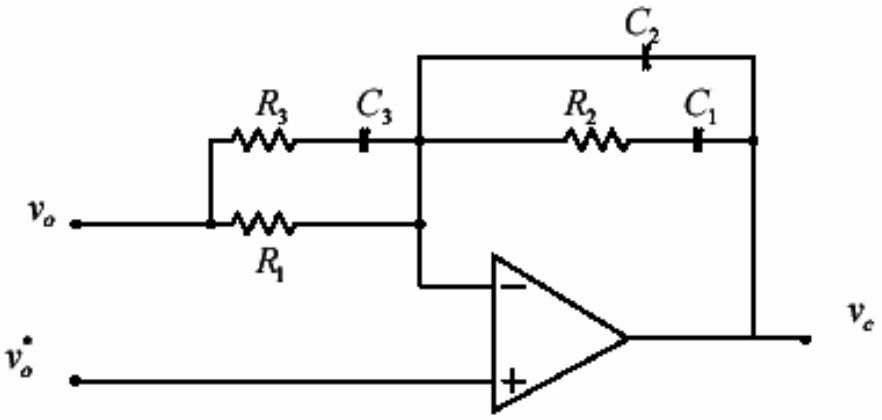


Figure 4-12 Implementation of the controller by an op-amp.

$$C_2 = \omega_z / (k_c \omega_p R_1)$$

$$C_1 = C_2 \left(\omega_p / \omega_z - 1 \right)$$

$$R_2 = 1/(\omega_z C_1)$$

$$R_3 = R_1 / (\omega_p / \omega_z - 1)$$

$$C_3 = 1/(\omega_p R_3)$$

IV. CONTROL METHODS IN SMPS

In this numerical example with $f_c = 1$ kHz, $\phi_{boost} = 108^o$, and $\left|G_C(s)\right|_{f_c} = 0.5263$, we can calculate $K_{boost} = 3.078$ in Eq. 4-27. Using Eqs. 4-27 through 4-30, $f_z = 324.9\,Hz$, $f_p = 3078\,Hz$, and $k_c = 349.1$. For the op-amp implementation, we will select $R_1 = 100\,k\Omega$. From Eq. 4-30, $C_2 = 3.0\,nF$, $C_1 = 25.6\,nF$, $R_2 = 19.1\,k\Omega$, $R_3 = 11.8\,k\Omega$, and $C_3 = 4.4\,nF$.

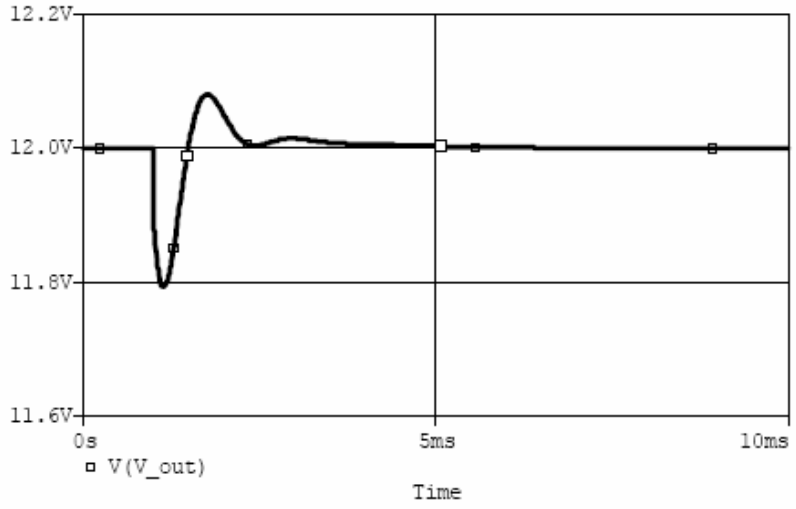
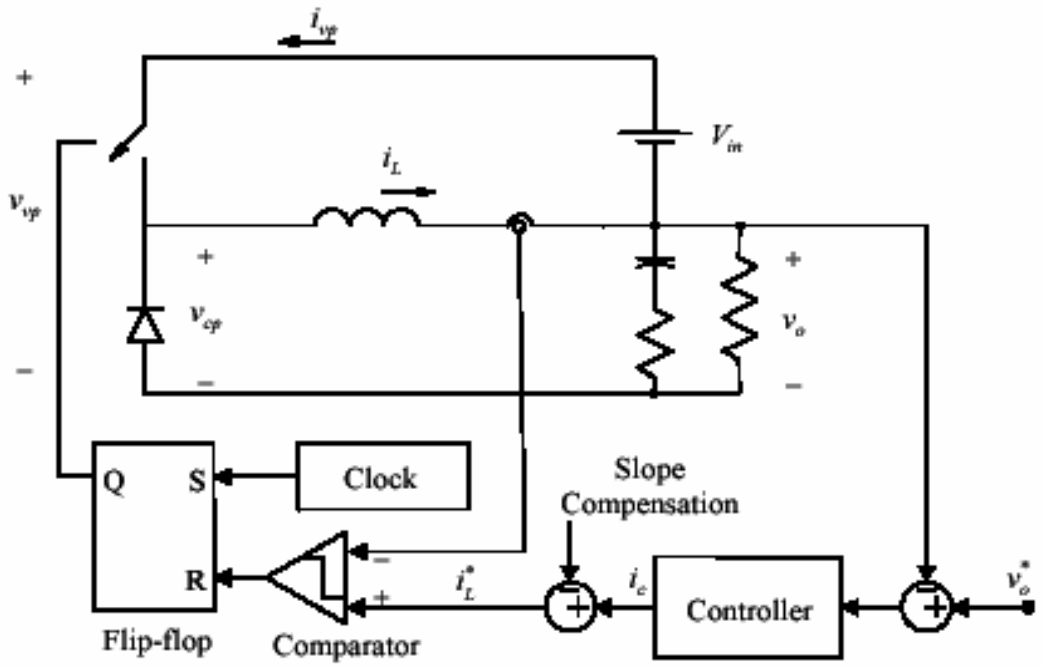


Figure 4-14 Response to a step-change in load.

IV. CONTROL METHODS IN SMPS

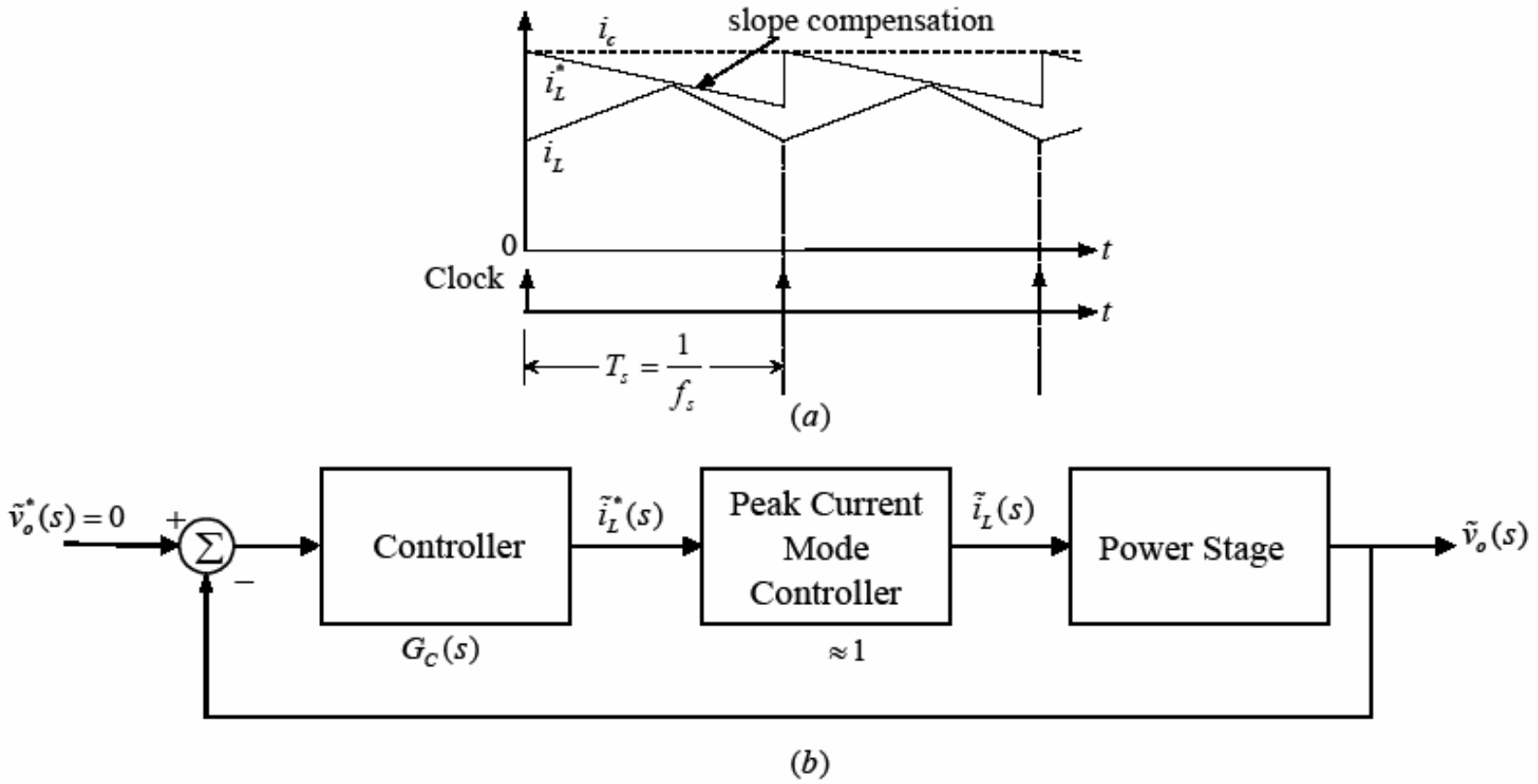
PEAK-CURRENT MODE CONTROL

- Peak-Current-Mode Control, and
- Average-Current-Mode Control.



Peak current mode control.

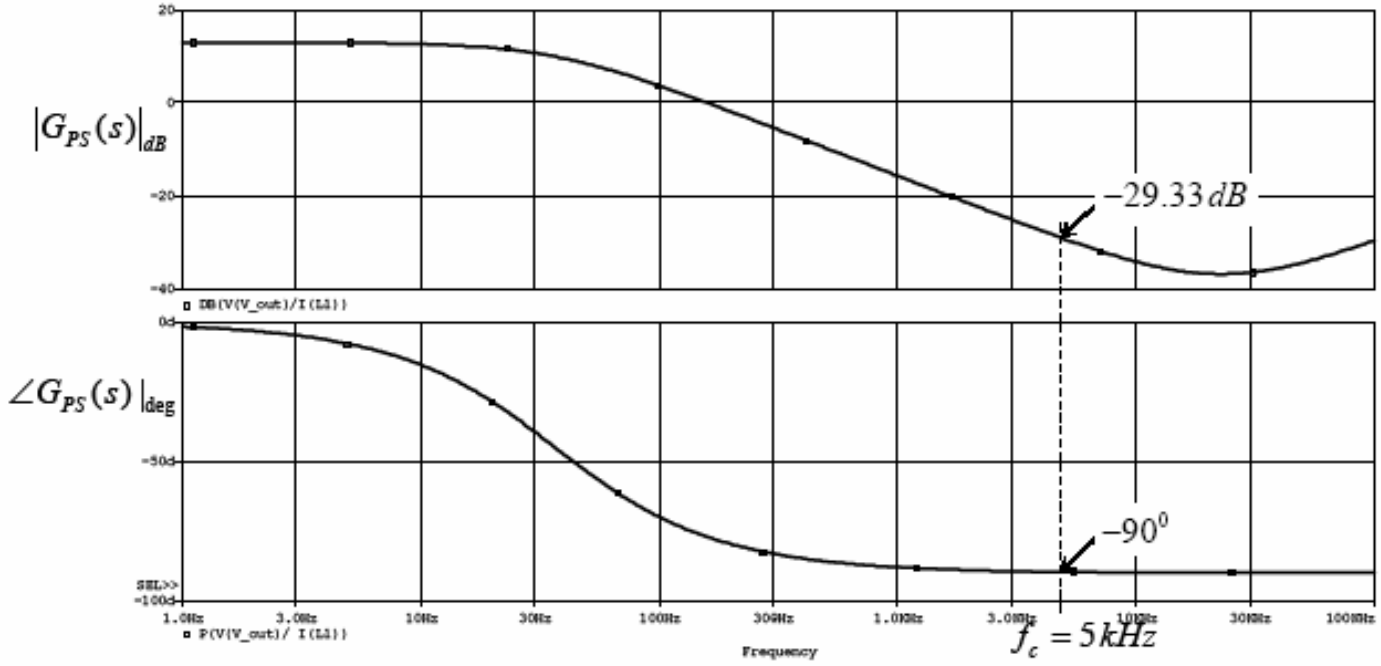
IV. CONTROL METHODS IN SMPS



Peak-current-mode control with slope compensation.

IV. CONTROL METHODS IN SMPS

▲ **Example 4-4** In this example, we will design a peak-current-mode controller for a Buck-Boost converter that has the following parameters and operating conditions: $L = 100\,\mu\text{H}$, $C = 697\,\mu\text{F}$, $r = 0.01\Omega$, $f_s = 100\,\text{kHz}$, $V_{in} = 30\,\text{V}$. The output power $P_o = 18\,\text{W}$ in CCM and the duty-ratio D is adjusted to regulate the output voltage $V_o = 12\,\text{V}$. The phase margin required for the voltage loop is 60^0. Assume that in the voltage feedback network, $k_{FB} = 1$.



IV. CONTROL METHODS IN SMPS

$$G_c(s) = \frac{k_c}{s} \underbrace{\frac{(1+s/\omega_z)}{(1+s/\omega_p)}}_{phase-boost} \qquad K_{boost} = \tan\left(45^o + \frac{\phi_{boost}}{2}\right)$$

$$f_z = \frac{f_c}{K_{boost}} \qquad f_p = K_{boost} f_c$$

$$k_c = \omega_z \left|G_C(s)\right|_{f_c}$$

At the crossover frequency, as shown in Fig. 4-18, the power stage transfer function has a gain $\left|G_{PS}(s)\right|_{f_c} = -29.33\,dB$. Therefore, at the crossover frequency, by definition, in Fig. 4-16b

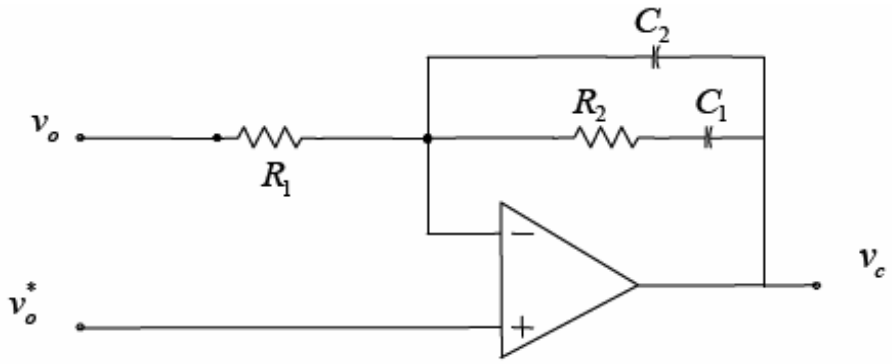
$$\left|G_C(s)\right|_{f_c} \times \left|G_{PS}(s)\right|_{f_c} = 1 \qquad (4\text{-}37)$$

Hence,

$$\left|G_C(s)\right|_{f_c} = 29.33\,dB = 29.27 \qquad (4\text{-}38)$$

Using the equations above for $f_c = 5\,kHz$, $\phi_{boost} \simeq 60^0$, and $\left|G_C(s)\right|_{f_c} = 29.27$, $K_{boost} = 3.732$ in Eq. 4-32. Therefore, the parameters in the controller transfer function of Eq. 4-31 are calculated as $f_z = 1340\,Hz$, $f_p = 18660\,Hz$, and $k_c = 246.4 \times 10^3$.

IV. CONTROL METHODS IN SMPS



Implementation of controller

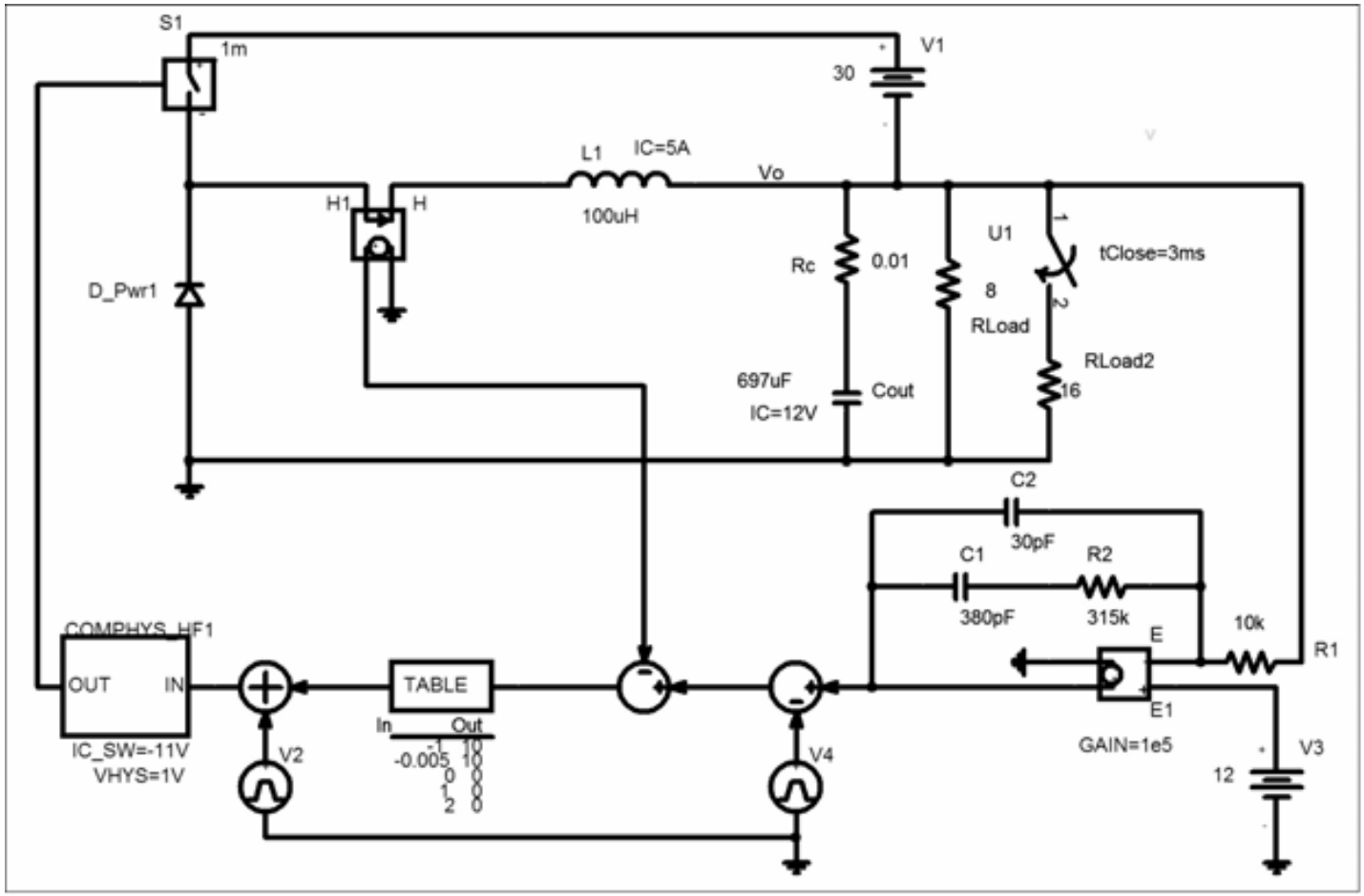
$$R_1 = 10\,k\Omega$$

$$C_2 = \frac{\omega_z}{\omega_p R_1 k_c} = 30\ pF$$

$$C_1 = C_2\left(\omega_p / \omega_z - 1\right) = 380\,pF$$

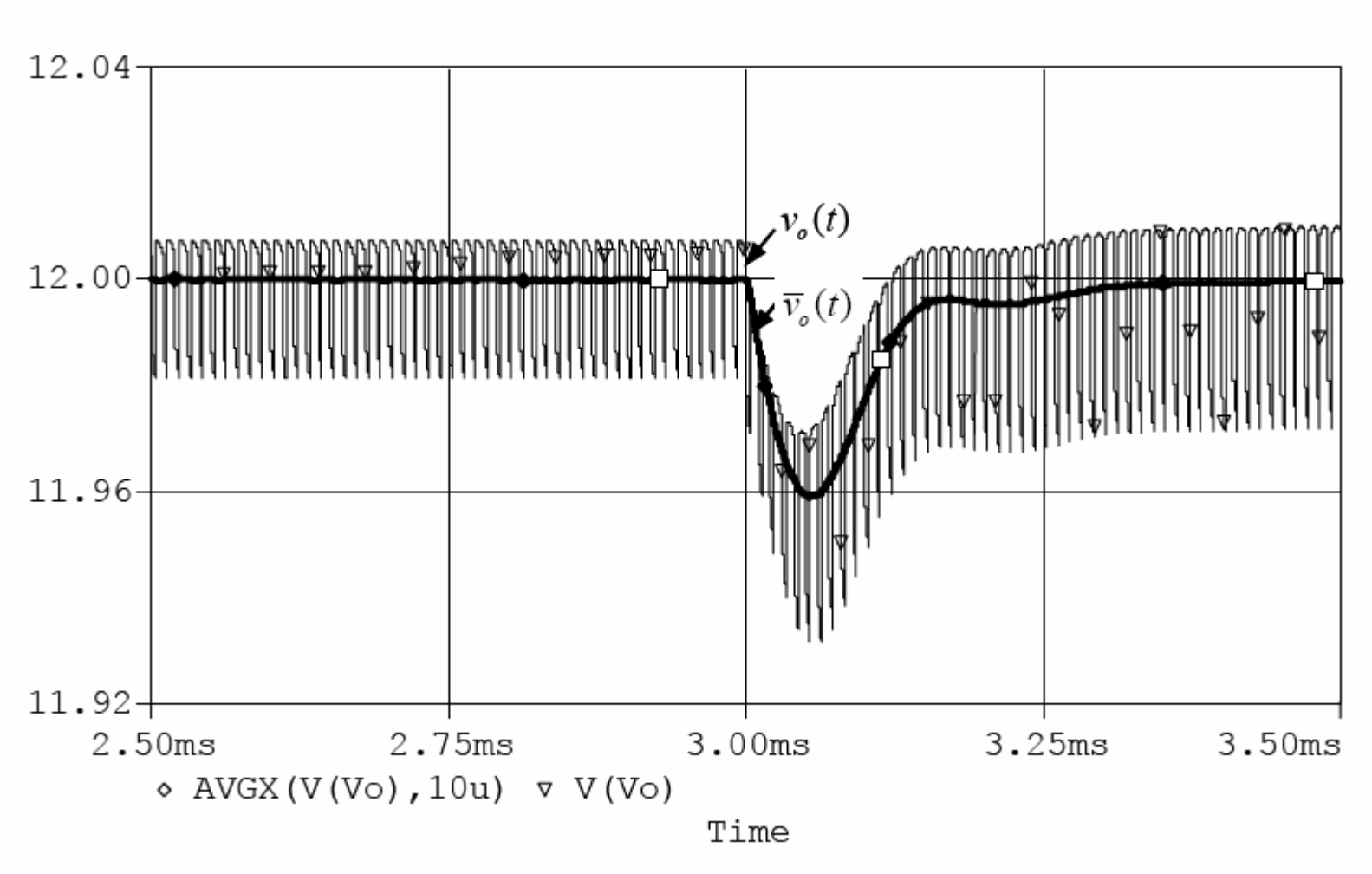
$$R_2 = 1/(\omega_z C_1) = 315\,k\Omega$$

IV. CONTROL METHODS IN SMPS



Simulation of peak current mode control

IV. CONTROL METHODS IN SMPS



IV. CONTROL METHODS IN SMPS

Summary

CLOSED LOOP DESIGN PROCEDURE

(1) Define the Goal: Make a Bode plot of the desired closed-loop characteristic that will achieve the best possible gain-bandwidth for good dynamic response, line and load regulation and stability.

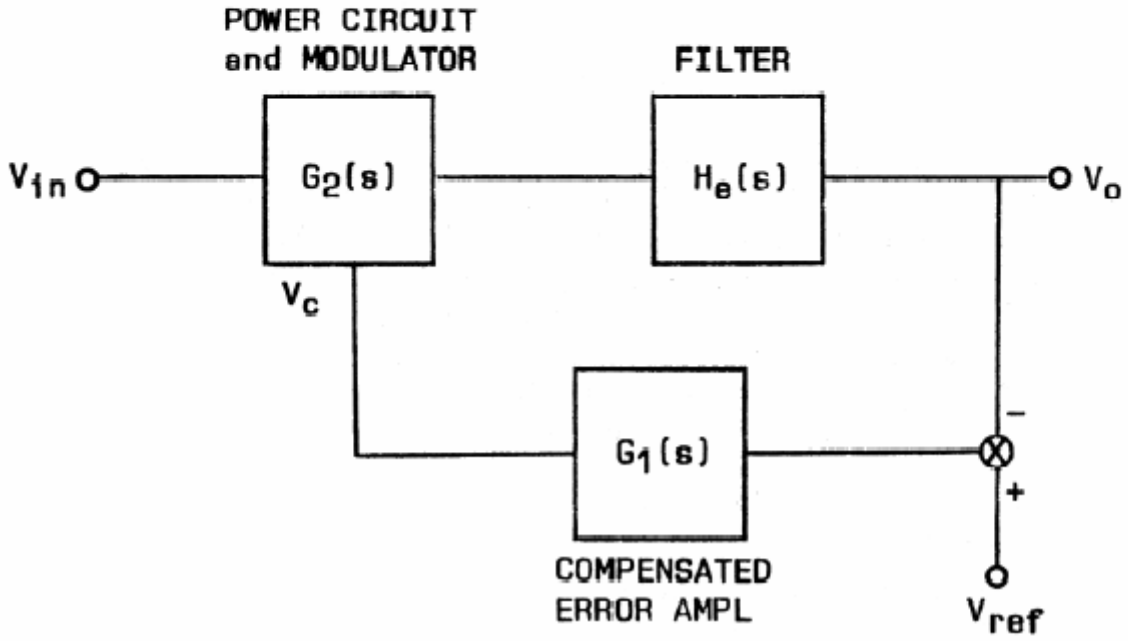
(2) Define the Control to Output Gain: Decide upon the control method. Make a Bode plot of G2(s), the gain characteristic of the pulse width modulator and power switch, and $H_e(s)$, the filter.

(3) Design the Compensation Network: Subtract the gain(dB) and phase plotted in (2) above from (1). The result is the G1(s) characteristic necessary to attain the closed loop objective.

V. CONTROL METHODS IN SMPS

Switching power supplies almost always use closed-loop negative feedback systems in order to achieve design objectives for line and load regulation and dynamic response. As shown in Figure 1, the closed loop can be described in terms of these major elements:

Reference and comparator
$G1(s)$: Error amplifier and compensation networks
$G2(s)$: Pulse width modulator and power switching circuit
$H_e(s)$: Output power filter



Closed loop control system

IV. CONTROL METHODS IN SMPS

DEFINE THE GOAL

Stability Criterion: Referring to Figure 2, if the gain magnitude crosses unity (0 dB) only once, the system is stable if the phase lag at the crossover frequency, f_c, is less than 180 degrees (in addition to the normal 180 degree phase shift of the negative feedback system). At other frequencies, the phase lag may exceed 180 degrees and the system will still be stable.

The 'phase margin' is the amount by which the phase lag at the crossover frequency, f_c, is less than 180 degrees. The 'gain margin' is the factor by which the gain is less than unity (0 dB) at the frequency where the phase lag is 180 degrees. If the phase lag at f_c is only slightly less than 180 degrees (small phase margin), the system will be stable, but will exhibit condsiderable overshoot and ringing. A phase margin of 45 degrees provides for good response with very little overshoot.

IV. CONTROL METHODS IN SMPS

DEFINE THE CONTROL TO OUTPUT GAIN

The control to output gain, or transfer characteristic, is the combined gain and phase vs. frequency characteristics of the PWM and switching circuit, G2(s), plus the output filter, He(s). The PWM, switching circuit and filter are fundamental to the design of the switching power supply. These elements are usually designed well before the process of closing the loop is started.

Because the control to output gain is part of the total loop, it is necessary to make a Bode plot of the control to output gain in order to know how to design the remainder of the loop -- the error amplifier and compensation network.

IV. CONTROL METHODS IN SMPS

DESIGN THE COMPENSATION NETWORK

The control to output gain characteristic subtracted from the overall closed loop objective roughly defines the characteristic sought in the error amplifier with its compensation network. In general, the procedure involves:

(1) Put zeros in the compensation network near the frequencies where excess poles occur in the control to output gain so that phase shift has an adequate margin (45 degrees) up to the cross-over frequency.

(2) Put poles in the compensation network near the frequencies where ESR zeros and right-half-plane zeros occur in the control to output gain. Otherwise these zeros will flatten the gain characteristic and prevent it from falling off as desired.

(3) If low frequency gain is too low to obtain desired DC regulation because of zeros added in step (1), add a pole-zero pair at low frequency to boost gain.

(4) In complex situations, a certain amount of juggling with trial solutions is inevitable.

IV. CONTROL METHODS IN SMPS

MISCELLANEOUS POINTS

EMI Filter Resonance: When an input EMI filter is used, make sure its resonance is well damped and its resonant frequency is not near the resonant frequency of the output filter, or severe interaction will result.

Modulator Phase Lag: The vast majority of PWM control chips use a simple comparator method of determining pulse width, wherein the output pulse is terminated according to the instantaneous value of the feedback control voltage at the moment of pulse termination. This "naturally sampled" method of pulse width modulation ideally results in zero phase lag in the modulator and in the converter power switching stage.[2] In practice, however, comparator delays and storage time delays in the power switch will cause a phase lag directly proportional to the delay time, t_d, and signal frequency, f, according to the relationship:

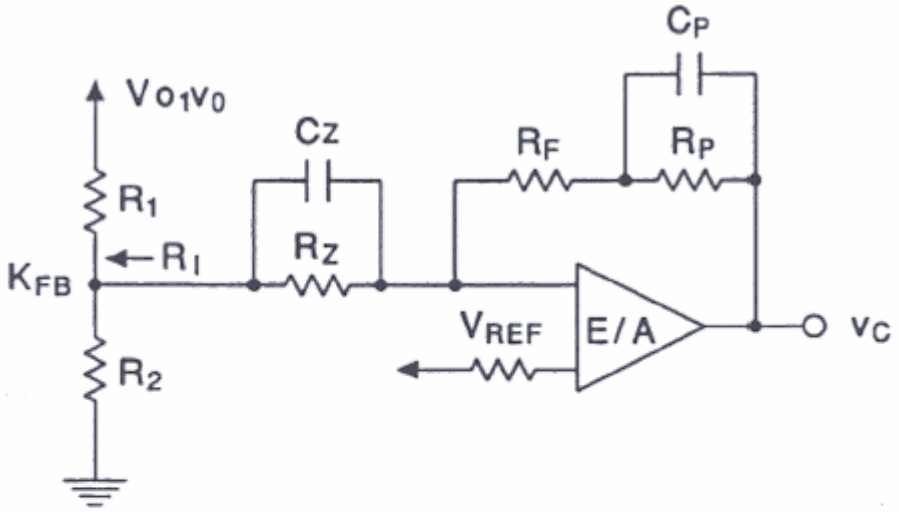
$$\phi_m = 360\, t_d/T = 360\, t_d\, f$$

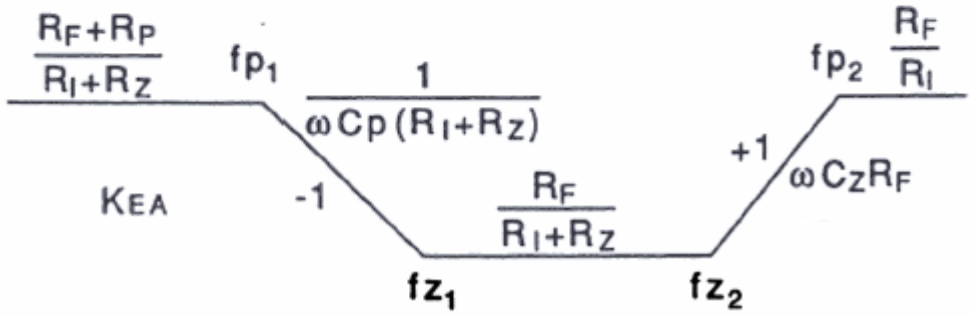
This additional phase lag reduces the phase margin at the unity gain crossover frequency and may therefore contribute to control loop instability. For example, at a crossover frequency of 25 kHz, consistent with a switching frequency greater than 50kHz, a storage time of 1 microsecond in the power switch will cause an additional phase lag of 9 degrees, reducing phase margin by that amount.

IV. CONTROL METHODS IN SMPS

Appendix: Error amplifier design

i- Voltage error amplifier





$$K_{FB} = \frac{V_{REF}}{V_O} = \frac{R_2}{R_1+R_2}$$

$$R_1 = \frac{R_I}{K_{FB}}$$

$$R_2 = \frac{R_I}{1-K_{FB}}$$

$$\omega_{PI} = \frac{1}{C_P(R_F+R_P)}$$

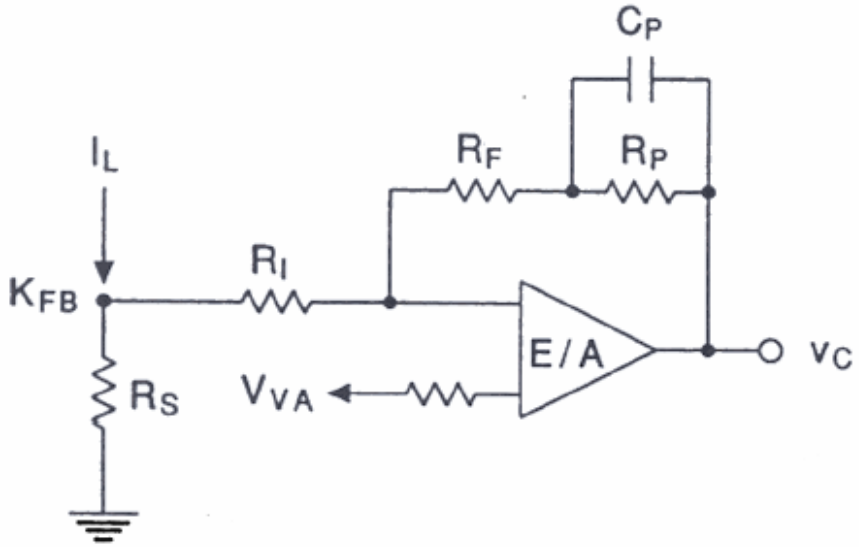
$$\omega_{Z1} = \frac{1}{C_P R_F}$$

$$\omega_{Z2} = \frac{1}{C_Z(R_I+R_Z)}$$

$$\omega_{P2} = \frac{1}{C_Z R_I}$$

IV. CONTROL METHODS IN SMPS

Error amplifier design: ii- Current error amplifier



$$K_{FB} = \frac{1}{R_S}$$

$$\omega_{P1} = \frac{1}{C_P(R_F + R_P)}$$

$$\omega_{Z1} = \frac{1}{C_P R_F}$$