Hacettepe University
Electrical and Electronics Engineering Department

ELE 764
Switch Mode Power Supplies

Lecture Notes
Chapter II

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II. SMPS TOPOLOGIES

Outline:

2.1 Introduction on SMPS Converter Circuit Topologies

Topology Selection, Application Areas

2.2. Comparison of Various SMPS Topologies

2.3. Asymmetrical Converters

Flyback Converter, Forward Converter

2.4. Symmetrical Converters

Push-Pull Converter, Half-bridge Converter,

Full-bridge Converter

2.5. Front-end Rectifiers

2.6. Examples

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2.1. SMPS Converter Circuit Topologies

There are several circuit topologies that have evolved, and used in SMPS. The major SMPS are classified as follows:

- *The buck converter*
- *The forward converter (buck-derived)*
- *The boost converter*
- *The flyback converter (buck-boost derived)*
- *The push-pull converter (buck-derived)*
- *The half-bridge converter (buck-derived)*
- *The full-bridge converter (buck-derived)*

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Some of the factors which determine the suitability of a particular topology to an application are:

Electrical isolation between input-output

The input voltage level across the inductor or transformer

Peak current flowing through the power semiconductors

Are multiple outputs required

How much voltage appears across the power semiconductors

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One or more of the factors listed below will help to select the best topology for a given application:

1) *Efficiency*
2) *Single vs multiple output*
3) *Power output*
4) *Input voltage source*
5) *Maximum output current from each output*
6) *Performance: RFI, transient response, output ripple, line and load regulation etc...*
7) *Size, weight and volume*
8) *Cost*
9) *Reliability*

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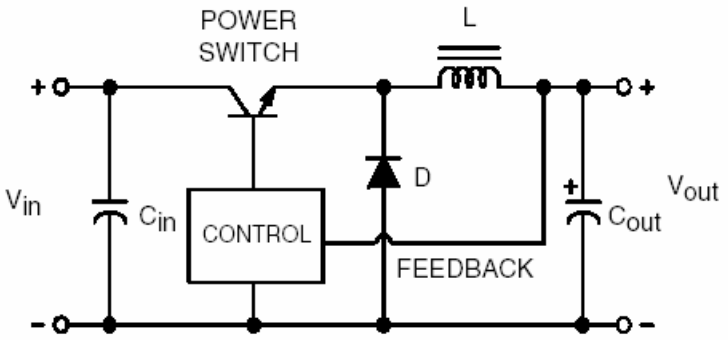
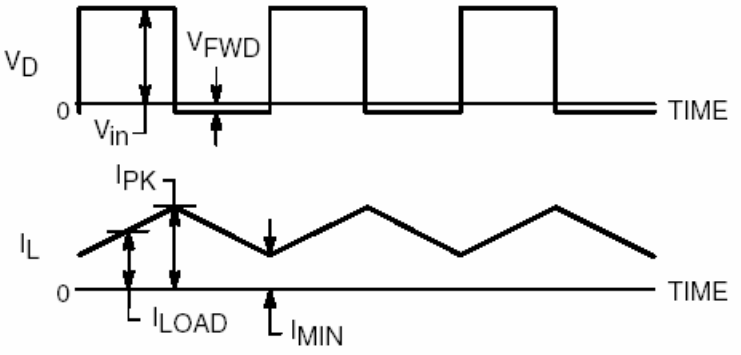
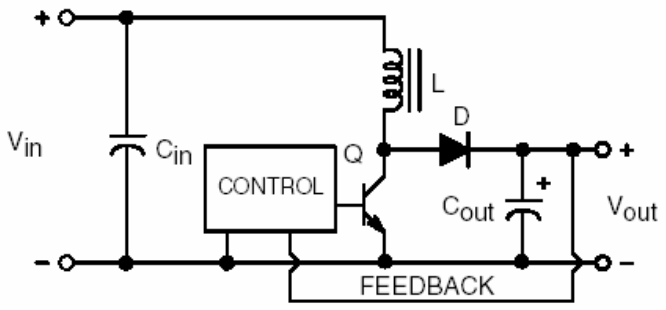
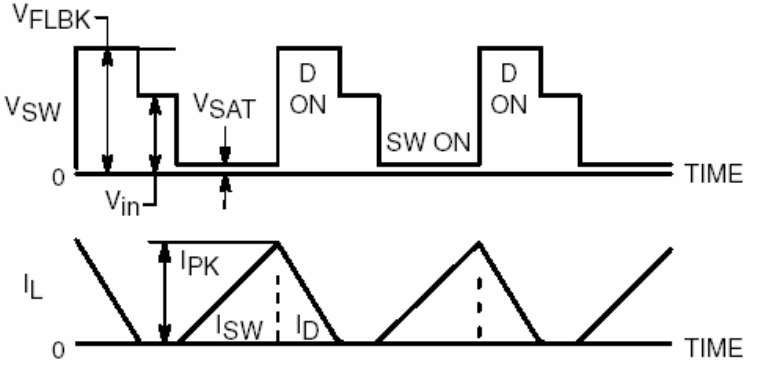
The Buck Regulator Topology





The Boost Regulator Topology





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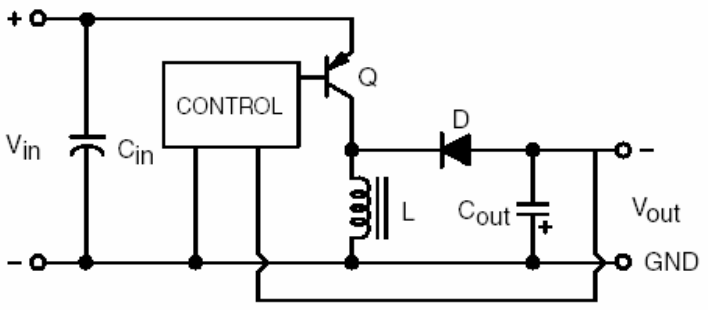
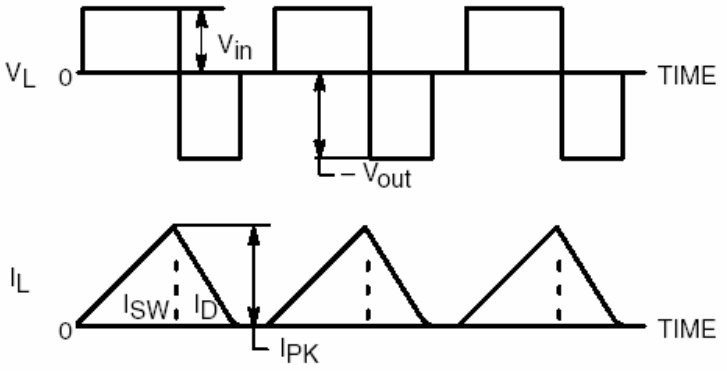
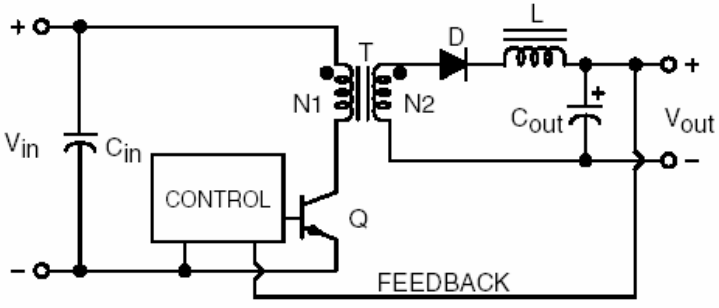
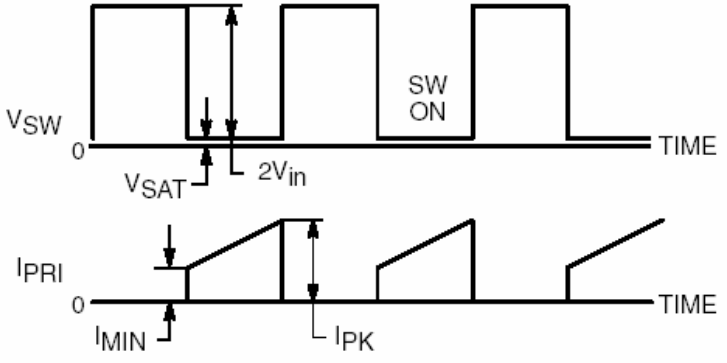
The Buck/Boost Regulator Topology





The Forward Regulator Topology





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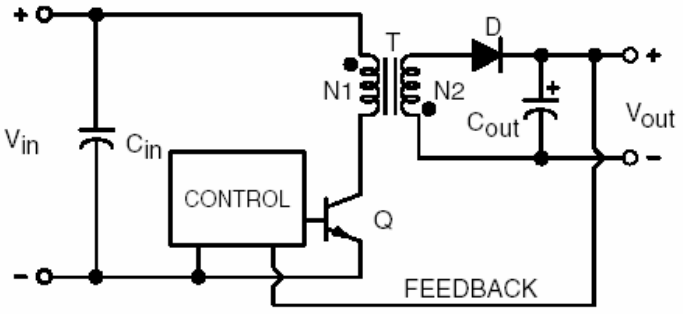
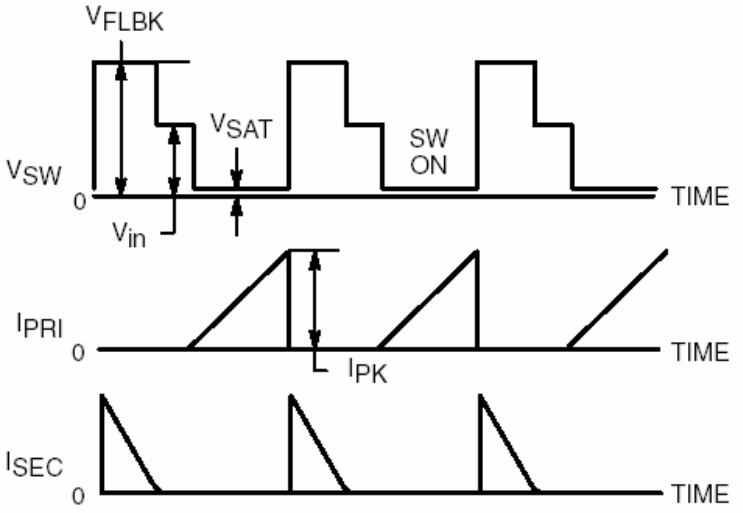
The Flyback Topology





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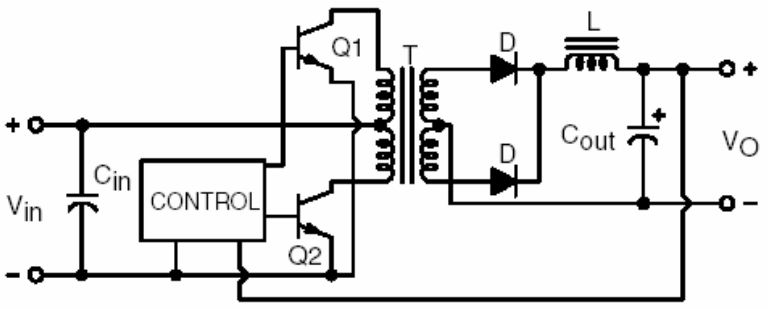
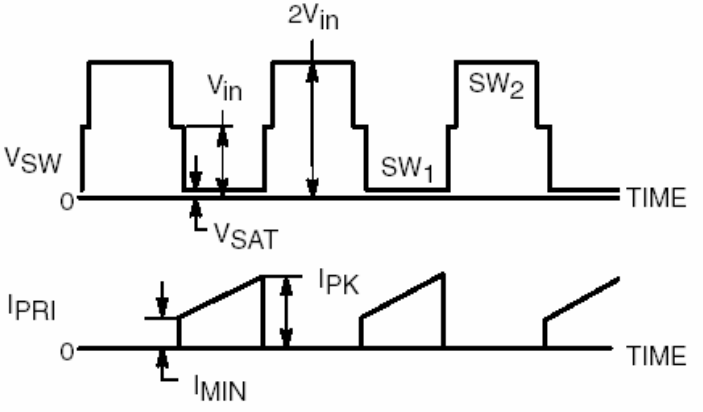
The Push-Pull Topology





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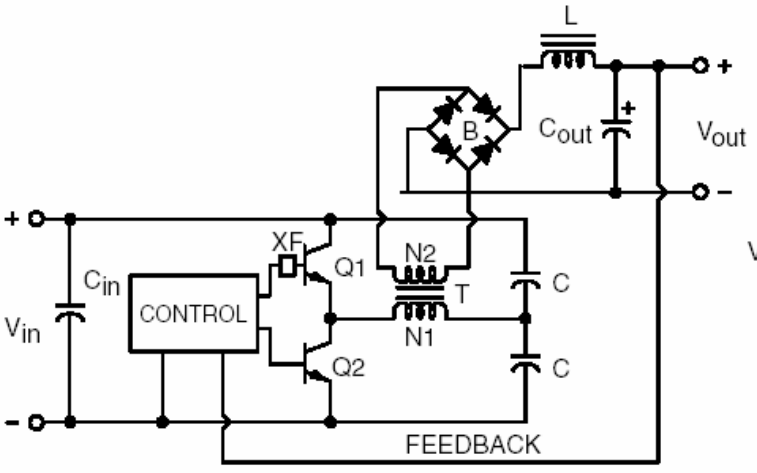
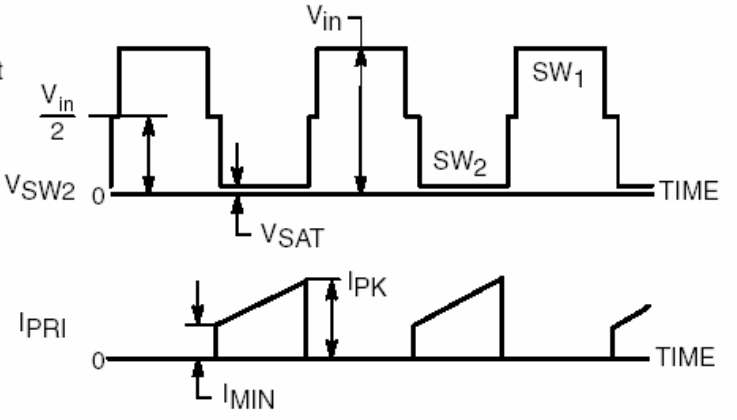
The Half-Bridge Topology





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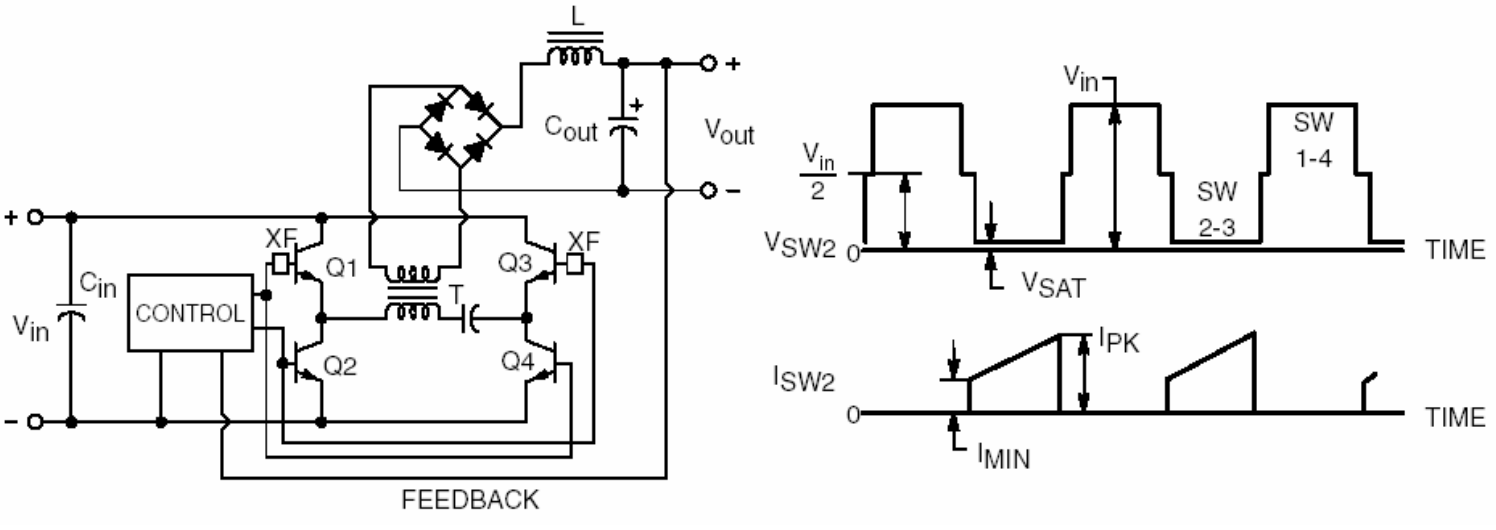
The Full-Bridge Topology



To make the best choice of a topology it is essential to be familiar with the merits, drawbacks and areas of usage of all topologies.

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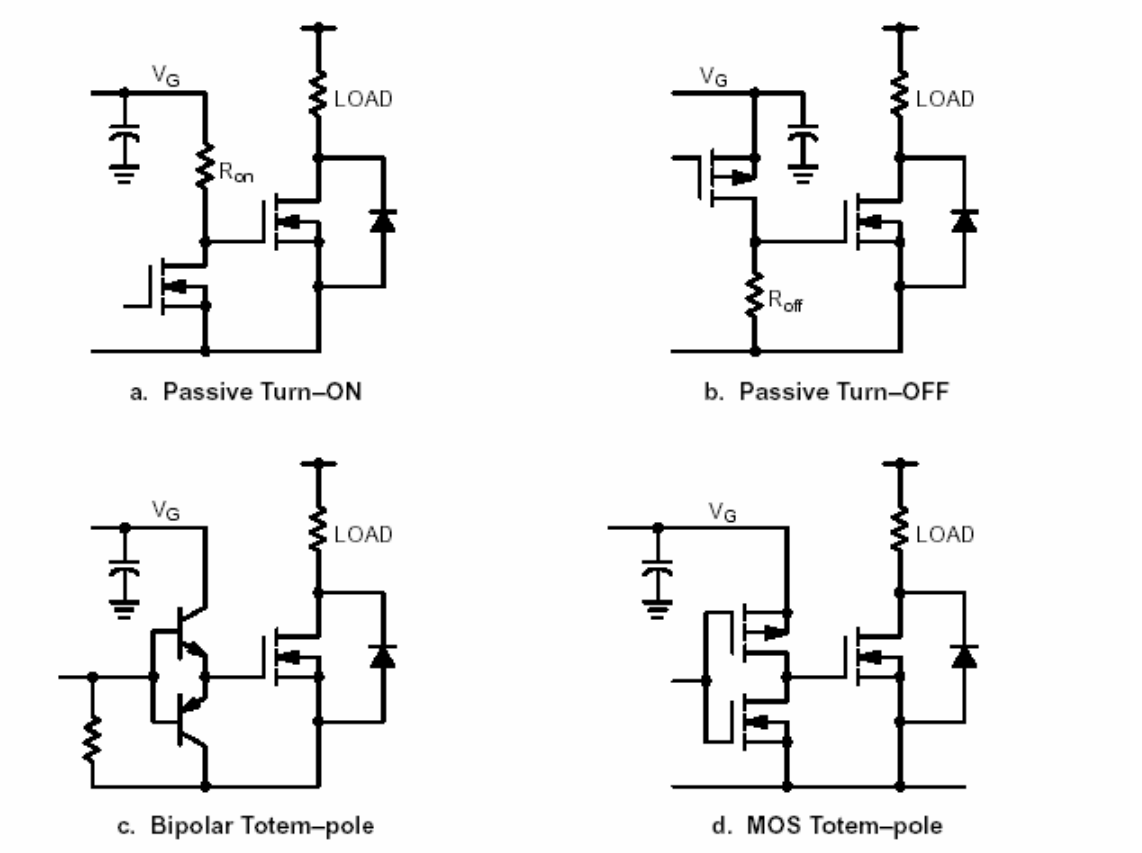
Bipolar and FET-Based Drive Circuits for MOSFETs in SMPS



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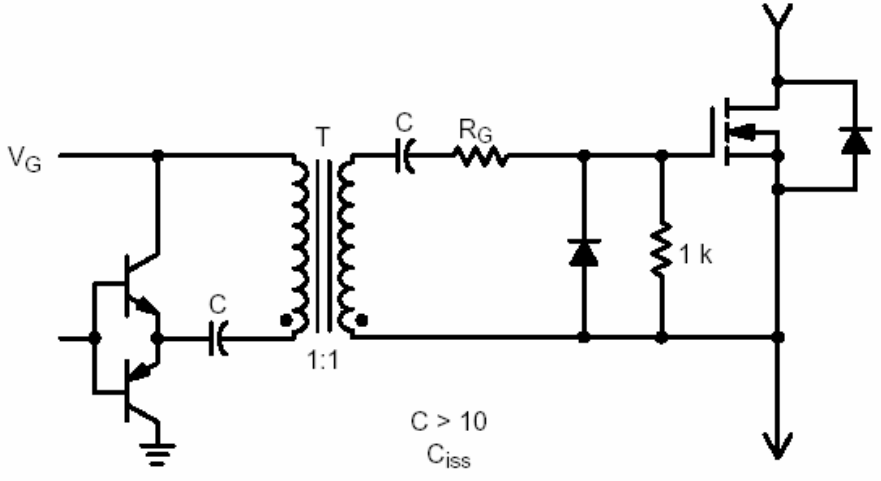
Transformer-isolated gate drive

Sometimes it is necessary to provide a dielectrically–isolated drive to a MOSFET. This is provided by a drive transformer. Transformers driven from a DC source must be capacitively coupled from the totem–pole driver circuit. The secondary winding must be capacitively coupled to the gate with a DC restoration circuit. Both of the series capacitors must be more than 10 times the value of the C_{iss} of the MOSFET so that the capacitive voltage divider that is formed by the series capacitors does not cause an excessive attenuation.



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From the gate terminal, there are 2 capacitances the designer encounters:

The gate input capacitance, C_{iss}, and the drain-gate reverse capacitance C_{rss}.

C_{iss} is a fixed value caused by the capacitance formed between gate metallization and substrate. Its value is in the range 800 – 3200 pF, depending upon MOSFET physical construction. C_{rss} is the capacitance between drain and gate, and is in the range 60-150 pF.

Although C_{rss} is smaller, it has much more pronounced effect upon the gate drive. It couples the drain voltage to the gate, thus dumping its stored charge into C_{iss}.

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Typical gate drive waveforms are shown below.

- *Time period t1 is only the C_{iss} being charged or discharged by the impedance of the external gate drive circuit.*

- *Period t2 shows the effect of changing the drain voltage being coupled into the gate through C_{rss}. One can observe the 'flattening' of the gate drive voltage during this period, both at turn-on and turn-off of the MOSFET.*

- *Time period t3 is the amount of overdrive voltage provided by the drive circuit but not really needed by the MOSFET.*

- *The time needed to switch the MOSFET depends upon the gate drive impedance, the drive crt. is bypasses with 0.1 μF keeping drive voltage constant over the drive period.*

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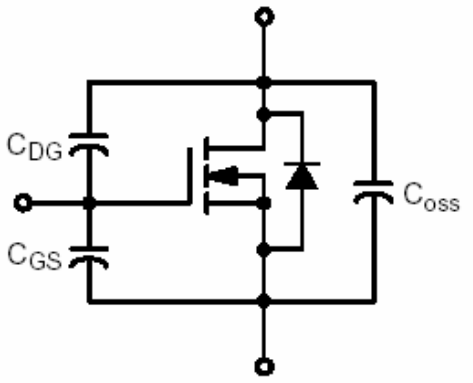
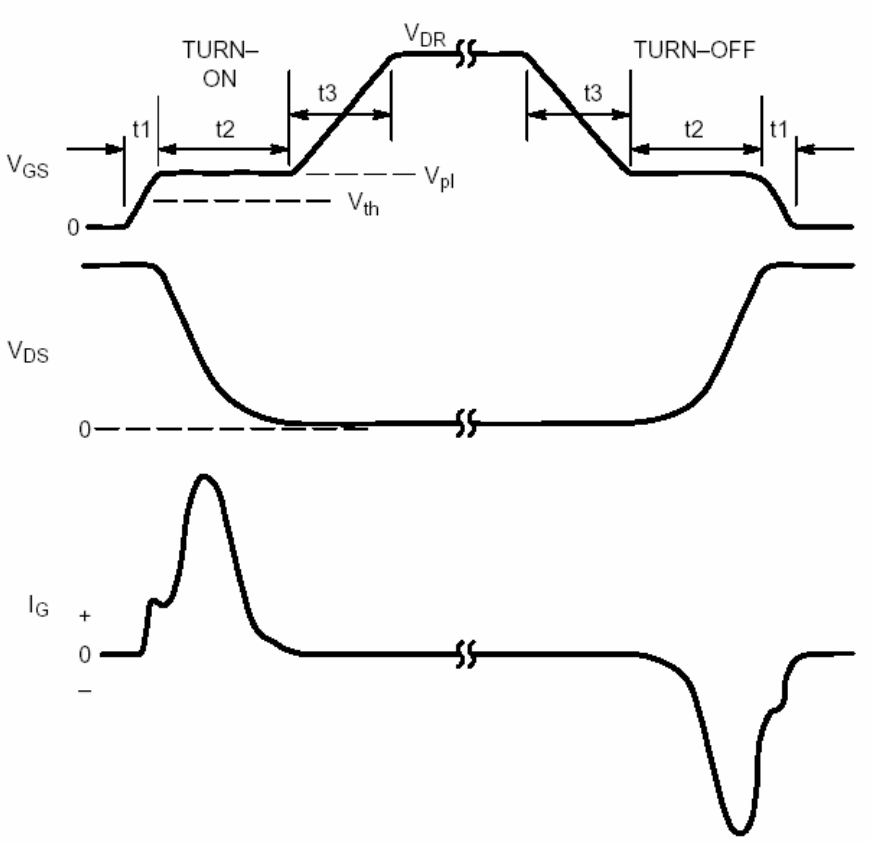
Typical MOSFET Drive Waveforms



The MOSFET model



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Types of Rectifier Technologies

Rectifier Type	Average V_f	Reverse Recovery Time	Typical Applications
Standard Recovery	0.7–1.0 V	1,000 ns	50–60 Hz Rectification
Fast Recovery	1.0–1.2 V	150–200 ns	Output Rectification
UltraFast Recovery	0.9–1.4 V	25–75 ns	Output Rectification (Vo > 12 V)
Schottky	0.3–0.8 V	< 10 ns	Output Rectification (Vo < 12 V)

A **standard recovery diode** is only suitable for 50–60 Hz rectification due to its slow turn–off characteristics. These include common families such as the 1N4000 series diodes. **Fast–recovery diodes** were first used in switching power supplies, but their turn–off time is considered too slow for most modern applications. They may find application where low cost is paramount, however. **Ultra–fast recovery diodes** turn off quickly and have a forward voltage drop of 0.8 to 1.3 V, together with a high reverse voltage capability of up to 1000 V. A **Schottky rectifier** turns off very quickly and has an average forward voltage drop of between 0.35 and 0.8 V, but has a low reverse breakdown voltage and a high reverse leakage current. For a typical switching power supply application, the best choice is usually a Schottky rectifier for output voltages less than 12 V, and an ultra–fast recovery diode for all other output voltages.

The major losses within output rectifiers are conduction losses and switching losses. The conduction loss is the forward voltage drop times the current flowing through it during its conduction period. This can be significant if its voltage drop and current are high. The switching losses are determined by how fast a diode turns off (t_{rr}) times the reverse voltage across the rectifier. This can be significant for high output voltages and currents.

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Types of Rectifier Technologies – Techniques to Improve Efficiency

The reduction of losses is important to the efficient operation of a switching power supply, and a great deal of time is spent during the design phase to minimize these losses. Some common techniques are described below.

The Synchronous Rectifier

As output voltages decrease, the losses due to the output rectifier become increasingly significant. For $V_{out} = 3.3$ V, a typical Schottky diode forward voltage of 0.4 V leads to a 12% loss of efficiency. Synchronous rectification is a technique to reduce this conduction loss by using a switch in place of the diode. The synchronous rectifier switch is open when the power switch is closed, and closed when the power switch is open, and is typically a MOSFET inserted in place of the output rectifier. To prevent "crowbar" current that would flow if both switches were closed at the same time, the switching scheme must be break–before–make. Because of this, a diode is still required to conduct the initial current during the interval between the opening of the main switch and the closing of the synchronous rectifier switch. A Schottky rectifier with a current rating of 30 percent of the MOSFET should be placed in parallel with the synchronous MOSFET. The MOSFET does contain a parasitic body diode that could conduct current, but it is lossy, slow to turn off, and can lower efficiency by 1% to 2%. The lower turn–on voltage of the Schottky prevents the parasitic diode from ever conducting and exhibiting its poor reverse recovery characteristic.

Using synchronous rectification, the conduction voltage can be reduced from 400 mV to 100 mV or less. An improvement of 1–5 percent can be expected for the typical switching power supply.

The synchronous rectifier can be driven either actively, that is directly controlled from the control IC, or passively, driven from other signals within the power circuit. It is very important to provide a non–overlapping drive between the power switch(es) and the synchronous rectifier(s) to prevent any shoot–through currents. This dead time is usually between 50 to 100 ns. Some typical circuits can be seen in Figure

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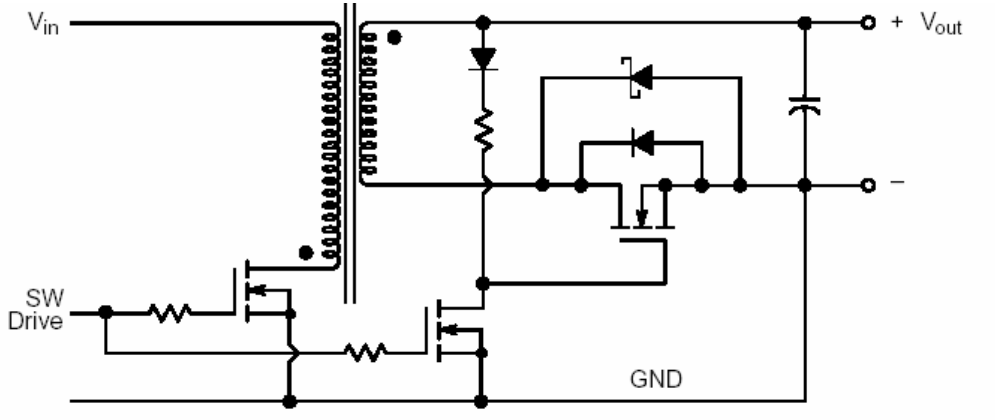
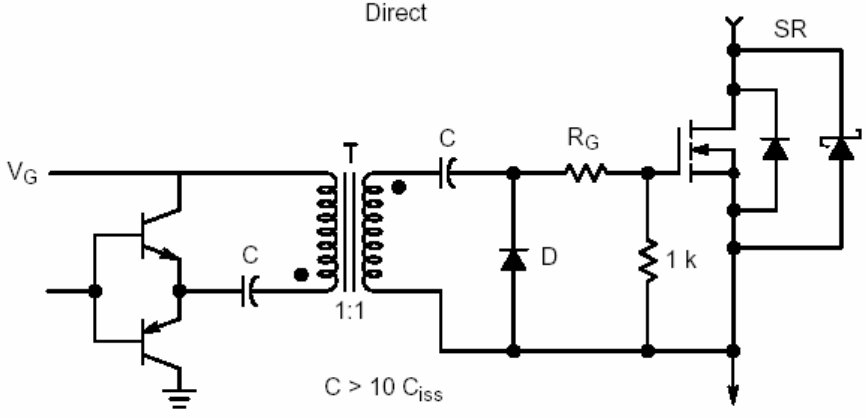
Types of Synchronous Rectifiers



Direct



Transformer–Isolated

(a) Actively Driven Synchronous Rectifiers

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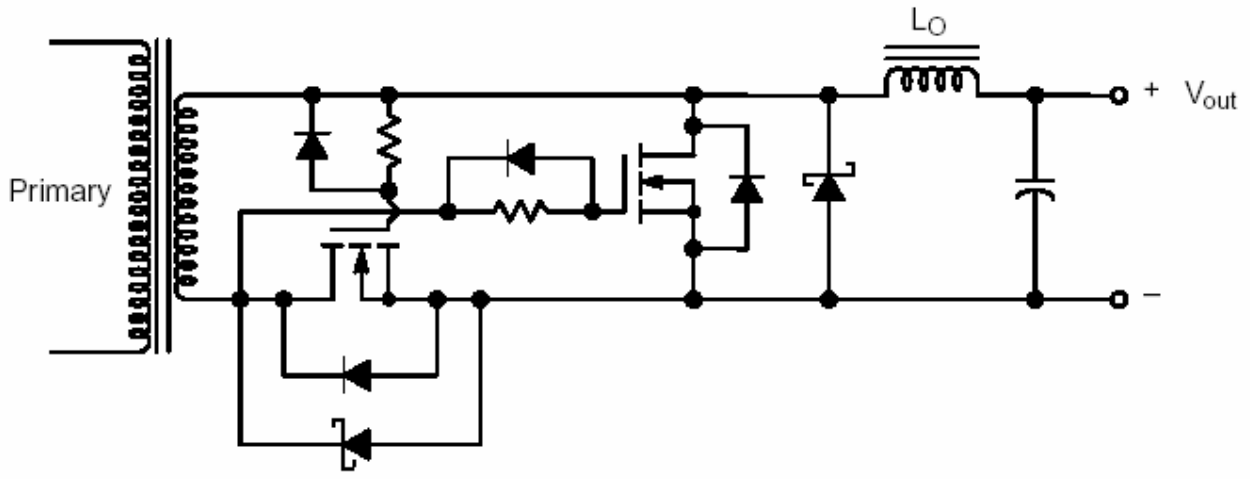
Types of Synchronous Rectifiers



(b) Passively Driven Synchronous Rectifiers

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2.2. Comparison of Various SMPS Circuit Topologies

Isolated or non-isolated topologies?

- *The first choice that faces the designer is whether to have input to output transformer isolation. Non-isolated SMPS are typically used for board level regulation where a dielectric barrier is provided elsewhere in the system. Non-isolated topologies are also used where a failure does not connect the input power source to the sensitive load. Transformer isolation should be used in all other circuitry.*

- *Transformer turns ratio can be selected to provide outputs widely different from the input, whereas non-isolated versions are limited to a range of nearly 5 times. By selecting a correct turns ratio, the duty cycle of the converter can be optimized, and the peak currents minimized.*

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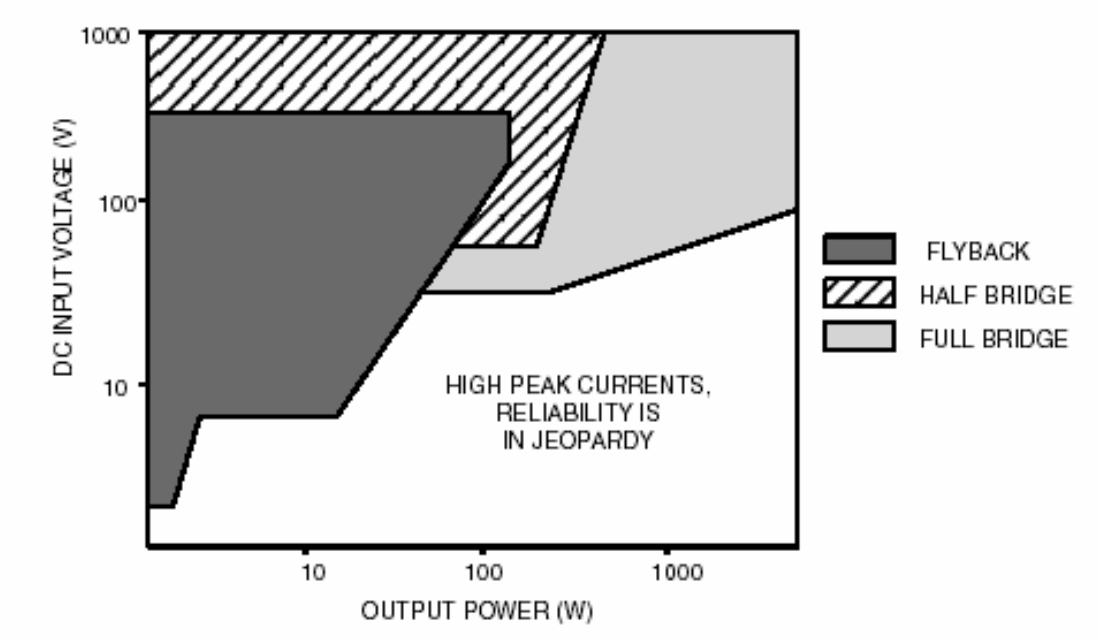
Application Areas of Transformer Isolated Topologies

➢ *The various areas show which topology best fits within that range of input voltage and output power that exhibits the least amount of stress on power semiconductors.*



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- *Transformers also provide additional output voltages to the power supply.*
- *Lesser input or output ripple and noise is another factor in a topology selection.*
- *Another factor is how much stress the power semiconductors are subjected to.*
- *At reduced dc input voltages, and at high powers, the peak currents that must be sustained by the power switch grow higher, which then affects the stress they must endure.*

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Comparison of the PWM Switching Regulator Topologies

Topology	Pwr Range (Watts)	$V_{in(DC)}$ Range	In/Out Isolation	Relative Cost
Buck	0 – 1000	5.0 – 1000*	No	1.0
Boost	0 – 150	5.0 – 600*	No	1.0
Buck-Boost	0 – 150	5.0 – 600*	No	1.0
Half-Forward	0 – 250	5.0 – 500	Yes	1.4
Flyback	0 – 150	5.0 – 600	Yes	1.2
Push-Pull	100 – 1000	50 – 1000	Yes	2.0
Half-Bridge	100 – 500	50 – 1000	Yes	2.2
Full-Bridge	400 – 2000+	50 – 1000	Yes	2.5

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Estimating Significant Parameters of Power Semiconductors (Min. Values)

Table shows the differences between various topologies used within the SMPS.

Parameters such as breakdown voltages should have a margin for the voltage spikes!

Topology	MOSFET Power Switch		Rectifier(s)	
	V_{DSS}	I_D	V_R	I_F
Buck	V_{in}	I_{out}	V_{in}	I_{out}
Boost	V_{out}	$\frac{2.0 P_{out}}{V_{in(min)}}$	V_{out}	I_{out}
Buck/Boost	$V_{in} - V_{out}$	$\frac{2.0 P_{out}}{V_{in(min)}}$	$V_{in} - V_{out}$	I_{out}
Flyback	$1.5\ V_{in(max)}$	$\frac{2.0 P_{out}}{V_{in(min)}}$	$10\ V_{out}$	I_{out}
1 Transistor Forward	$2.0\ V_{in}$	$\frac{1.5 P_{out}}{V_{in(min)}}$	$3.0\ V_{out}$	I_{out}
Push-Pull	$2.0\ V_{in}$	$\frac{1.2 P_{out}}{V_{in(min)}}$	$2.0\ V_{out}$	I_{out}
Half-Bridge	V_{in}	$\frac{2.0 P_{out}}{V_{in(min)}}$	$2.0\ V_{out}$	I_{out}
Full-Bridge	V_{in}	$\frac{1.2 P_{out}}{V_{in(min)}}$	$2.0\ V_{out}$	I_{out}

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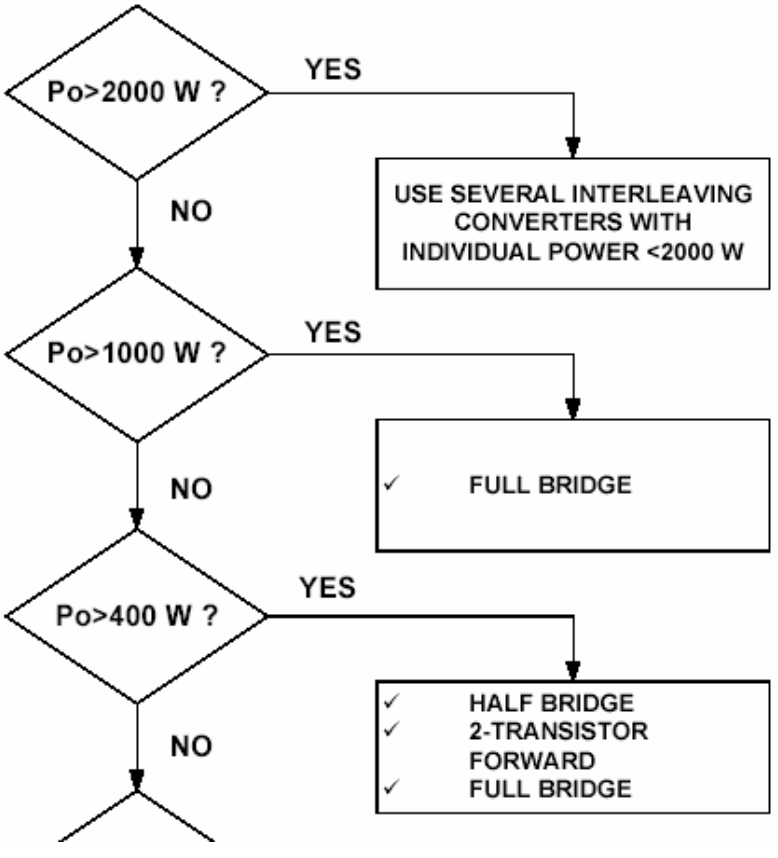
HOW TO SELECT TOPOLOGY OF THE OUTPUT CONVERTER IN OFFLINE SWITCHING POWER SUPPLY



ASSUMPTIONS:

1. Input voltage: 120 to 400 VDC (which is typical for rectified AC line voltage or an output of PFC boost)

2. Output voltages <48V

NOTE: This is just basic guidance in selecting the proper smps topology which is based on the author's personal view. The right topology will be selected depending on specific requirements for the power supply (including cost and time factors) and personal experience of the designer.

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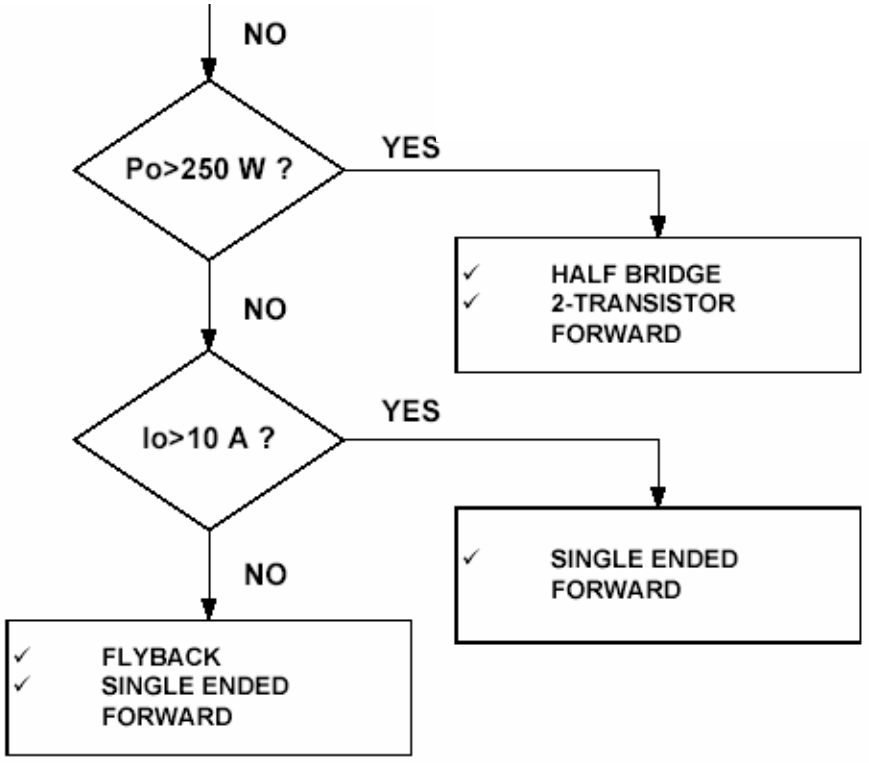

Po- output power
Io- maximum current of any output

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Most commonly used topologies in various applications:

A. Computer Main Frames
- full-bridge switching regulator
- current fed followed with a full-bridge
- step-down or linears in secondary outputs

B. Personal computer, Word processor, Point of sale terminals
- flyback switching regulator
- half-bridge switching regulator
- single transistor or two transistor forward converter
- step-down or linears in secondary outputs

C. Home computer
- linear regulator
- low cost flyback regulator

D. Printer
- linear regulator
- step-down regulator
- flyback regulator

E. PBX systems (switching station)
- two transistor forward converter
- half and full bridge regulator
- step-down or linears in secondary outputs

F. CATV
- step-down
- linear regulator
- flyback regulator

G. Video games
- linear regulator
- step-down regulator
- flyback regulator
- half-bridge regulator

H. Portable equipment (medical)
- buck regulator
- linear regulator

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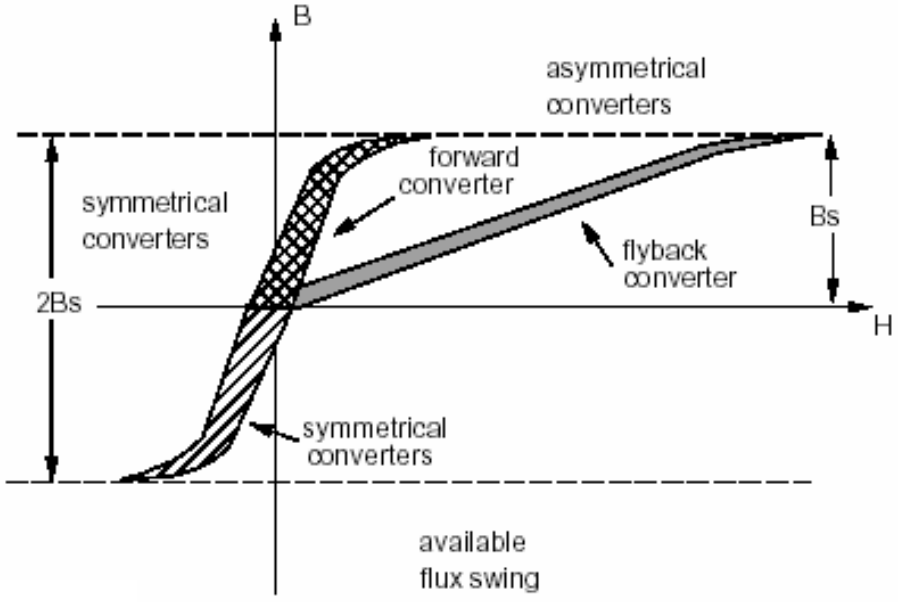
Isolated converters to be covered are split into two main categories:

Asymmetrical and symmetrical converters, depending upon how the transformer is operated.



Comparative core usage of asymmetrical and symmetrical converters.

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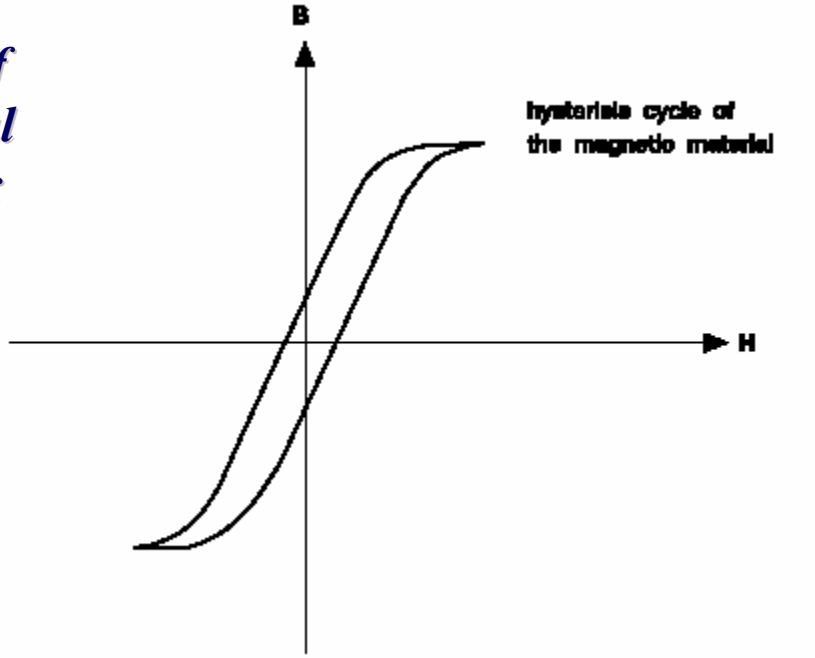
Isolated converters can be classified according to their magnetic cycle swing in the B-H plot. An isolated converter is asymmetrical if the magnetic operating point of the transformer remains in the same quadrant. Otherwise, it is called symmetrical.

B-H plot of symmetrical converters:



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2.3. Asymmetrical Converters

- *In asymmetrical converters, the magnetic operating point of the transformer is always in 1-Q, i.e. the flux and the magnetic field never change sign. The core has to be reset in each cycle to avoid saturation, meaning that only half of the usable flux is exploited.*

- *The flyback and forward converter are both asymmetrical types.*

- *The flyback is operated at a lower permeability (B/H), and lower inductance than the others. This is because the flyback transformer actually stores all of the energy before dumping into the load.*

- *Hence, an airgap is required to store this energy and avoid core saturation. The airgap has the effect of reducing the overall permeability of the core.*

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- One of the isolated converters, the single-ended flyback is shown in the following Figure. The use of a single transistor means that the transformer is used asymmetrically. The flyback is an isolated version of the buck-boost, and does not in truth contain a transformer, but a coupled inductor arrangement. When the transistor is turned on, current builds up in the primary, and energy is stored in the core. This energy is then released to the output circuit through the secondary when the switch is turned off.

- A normal transformer, such as the types used in buck derived topologies, couples the energy directly during the transistor on-time, ideally storing no energy.

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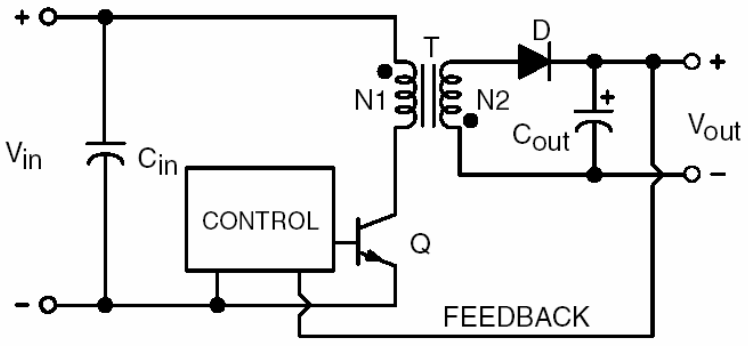
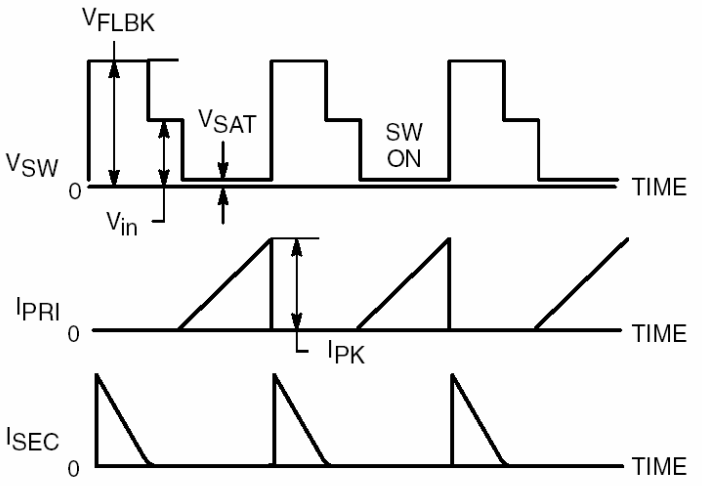
2.3.1 FLYBACK CONVERTER



In discontinuous conduction:



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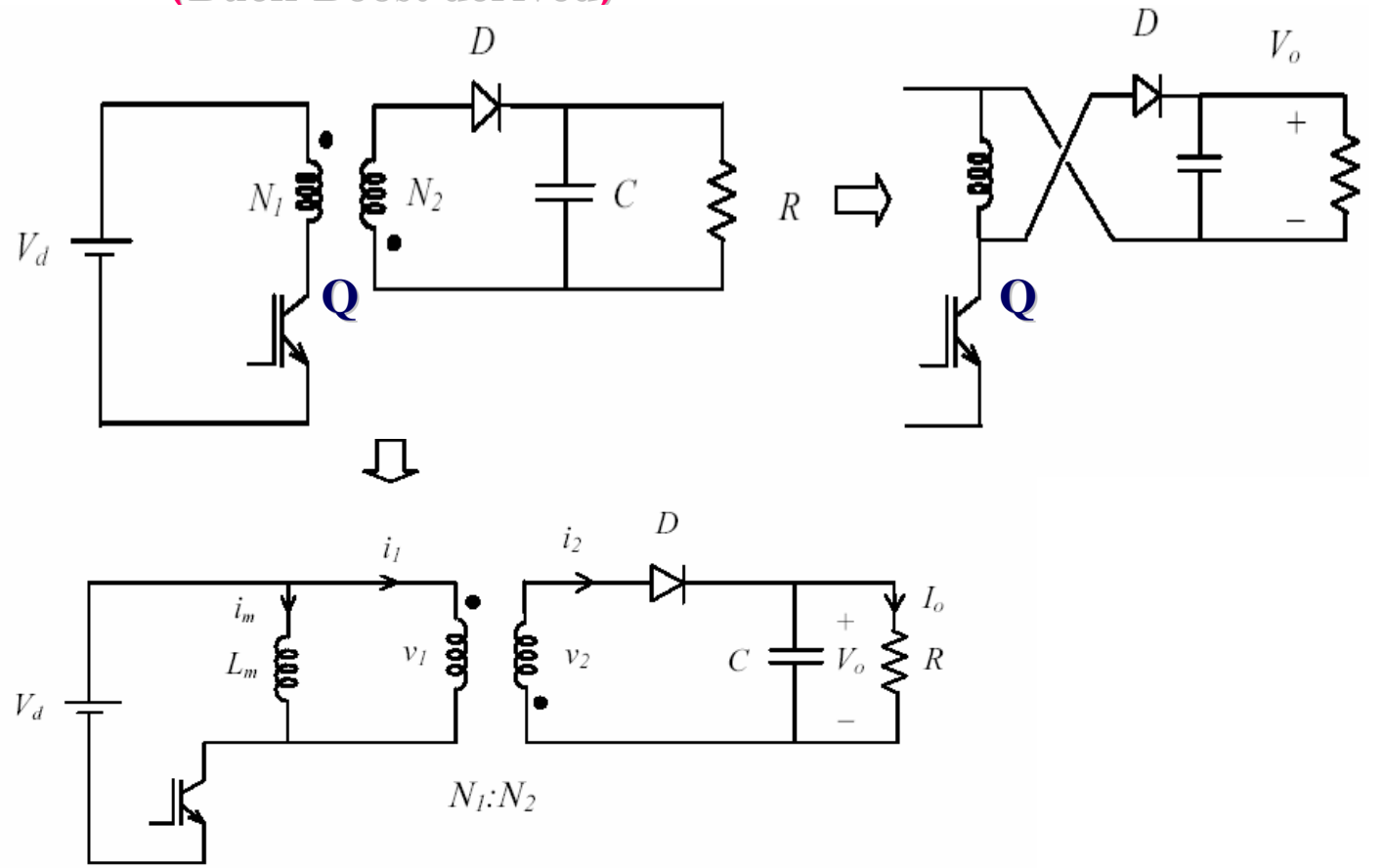
Flyback Converter (Buck-Boost derived)

Buck-Boost Converter



II. SMPS TOPOLOGIES

FLYBACK CONVERTER

- *The Flyback converter is widely used for output powers from 150 down to under 5W*
- *It has no secondary output inductor unlike the other topologies. The consequent savings in cost and volume of the output inductors is a significant advantage*
- *It is widely used for high output voltages at relatively low power (< 5kV, and at < 15 W)*
- *It is a frequent choice for multiple output power supplies in the region of 50 to 150 W*
- *It is attractive for a multiple output supply because the output voltages track one another with line and load changes far better than the other topologies due to the absence of output inductors*
- *It can be used from DC input voltages as low as 5V up to the usual rectified 320V DC form of 220V AC*

II. SMPS TOPOLOGIES

FLYBACK CONVERTER

- **Basic Operation :**

When the switch Q is **on** :

- Dot ends are positive so diode D on the secondary side is reverse biased
- There is a fixed voltage across the primary winding N1 and current in that winding ramps up linearly
- Energy is stored in the transformer
- The load current is supplied from the large storage filter capacitor C

II. SMPS TOPOLOGIES

FLYBACK CONVERTER

- **Basic Operation :**

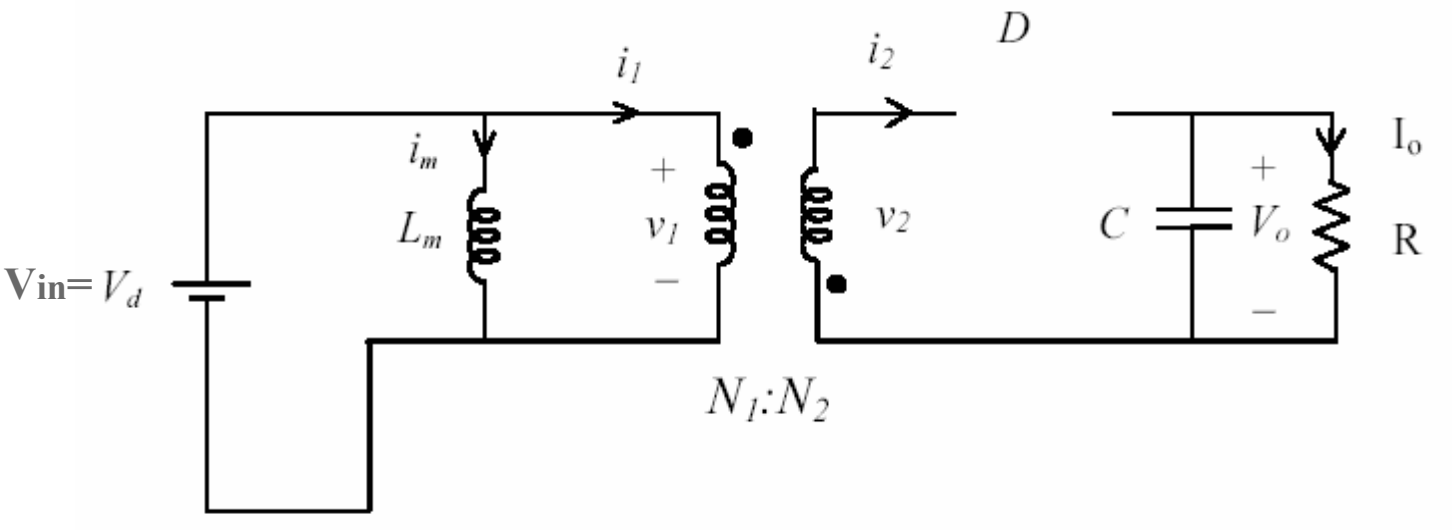
When the switch Q is **off** :

- Current in the magnetizing inductance forces the reversal of polarity on the secondary winding
- Diode D is forward biased
- The primary current is transferred to the secondary (Energy is transferred)
- The current in the secondary winding ramps down linearly

II. SMPS TOPOLOGIES

FLYBACK CONVERTER

When the switch Q is on :

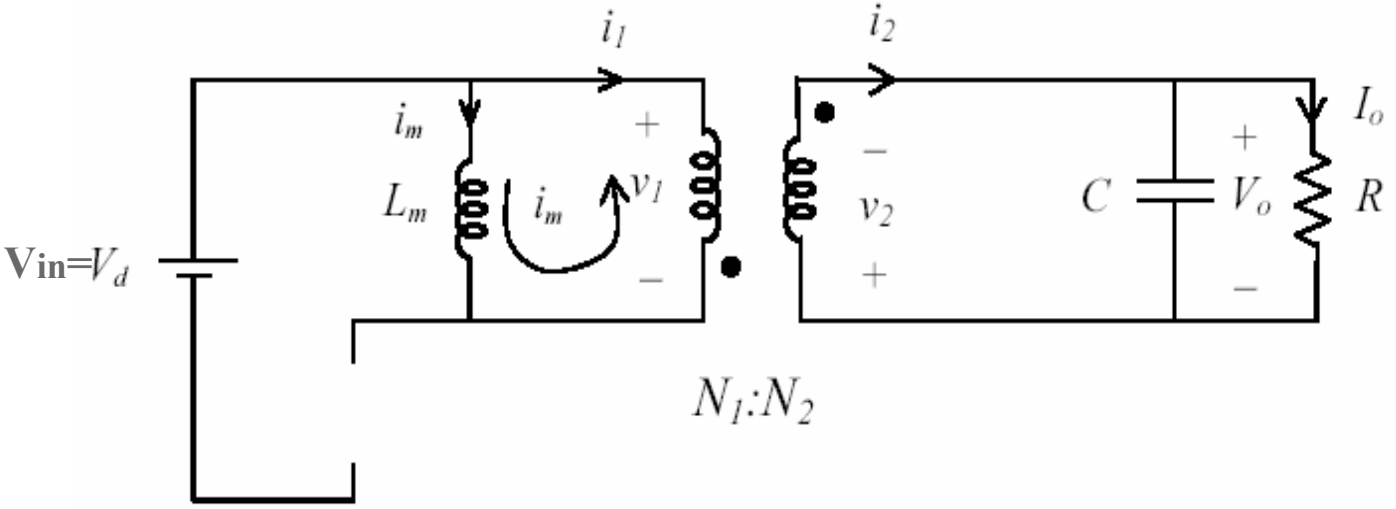


Circuit during t_{on} ; $v_1 = V_d$

II. SMPS TOPOLOGIES

FLYBACK CONVERTER

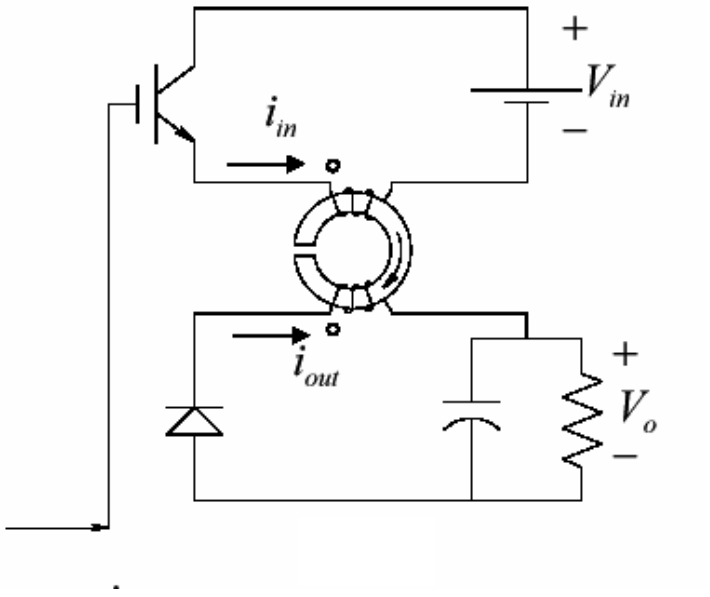
When the switch Q is off:

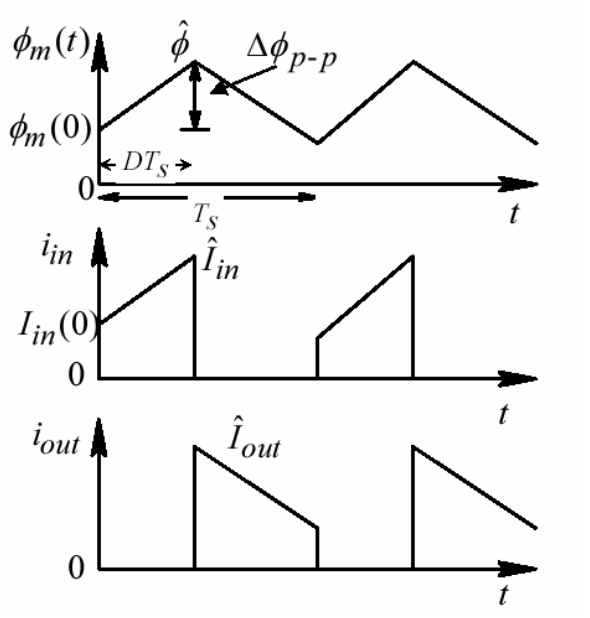


Circuit during t_{off} ; $i_2 = i_D$

II. SMPS TOPOLOGIES

Single switch flyback – Vo / Vin for continuous operation

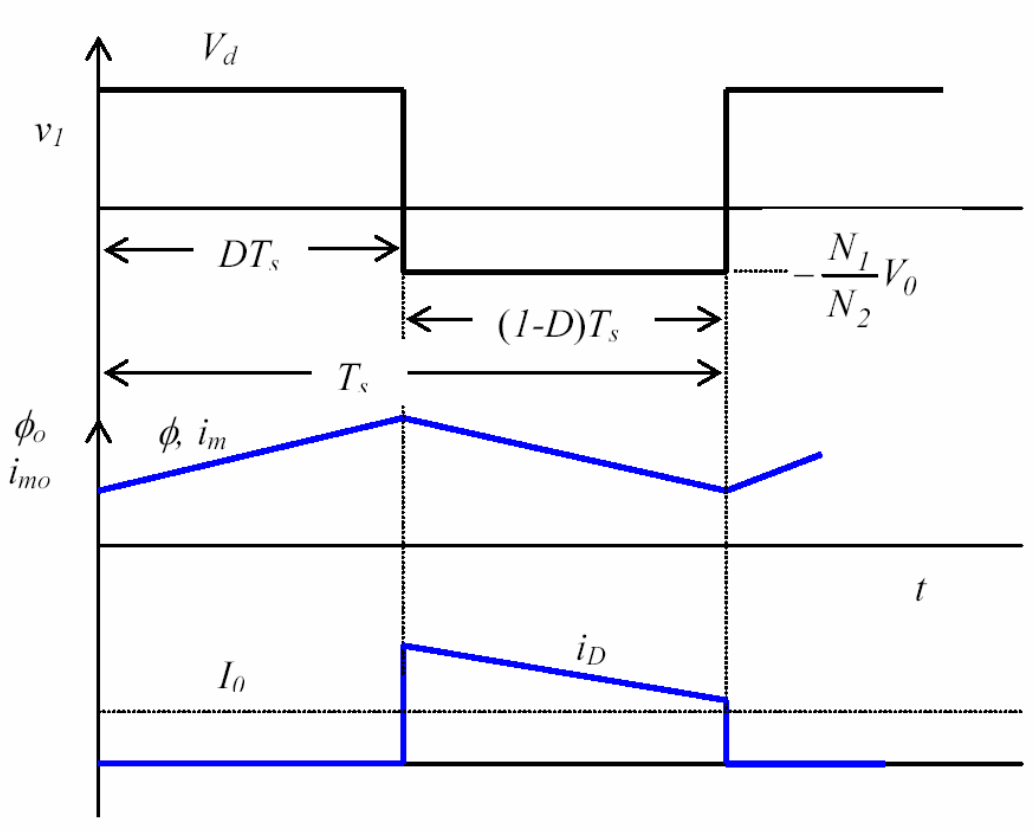




$$\Delta\phi_{p-p} = \frac{V_{in}}{N_1} DT_s = \frac{V_o}{N_2}(1-D)T_s \quad \Rightarrow \quad \frac{V_o}{V_{in}} = \left(\frac{N_2}{N_1}\right)\frac{D}{1-D}$$

II. SMPS TOPOLOGIES

Analysis of the Flyback Converter Under Continuous Conduction



II. SMPS TOPOLOGIES

Analysis of the Flyback Converter Under Continuous Conduction

$$v = N\frac{d\phi}{dt} \quad \text{or} \quad \frac{v}{N} = \frac{d\phi}{dt}$$

During $0 < t < t_{on}$, for the primary side,

$$\phi = \phi_0 + \frac{1}{N_1}\int_0^t V_d dt$$

$$\phi(t_{on}) = \phi_0 + \frac{V_d}{N_1}t_{on} = \phi_0 + \frac{V_d}{N_1}DT_s = \phi_{max}$$

During $t_{on} < t < T_s$ for the secondary side,

$$-V_o = N_2\frac{d\phi}{dt}$$

II. SMPS TOPOLOGIES

Analysis of the Flyback Converter Under Continuous Conduction

$$\therefore -\frac{1}{N_2}\int_{t_{on}}^{t} V_o\,dt = \phi_{max} - \frac{V_o}{N_2}(t - t_{on})$$

$$\phi(T_s) = \phi_{max} - \frac{V_o}{N_2}(T_s - t_{on}) = \phi_o + \frac{V_d}{N_1}DT_s - \frac{V_o}{N_2}(T_s - t_{on})$$

If the core flux is completely reset in each cycle, i.e., $\phi(0) = \phi(T_s) = 0$

$$\therefore \frac{V_o}{V_d} = \frac{N_2}{N_1}\frac{D}{1-D}$$

From power balance, $\frac{I_d}{I_0} = \frac{N_2}{N_1}\frac{D}{1-D}$

II. SMPS TOPOLOGIES

Operation Principles:

The polarity of the windings is such that the output diode blocks during the transistor on time. When the transistor turns off, the secondary voltage reverses, maintaining a constant flux in the core and forcing secondary current to flow through the diode to the output load. The magnitude of the peak secondary current is the peak primary current reached at transistor turn-off reflected through the turns ratio, thus maintaining a constant Ampere-turn balance.

The fact that all of the output power of the flyback has to be stored in the core as $1/2LI^2$ energy means that the core size and cost will be much greater than in the other topologies, where only the core excitation (magnetisation) energy, which is normally small, is stored. This, in addition to the initial poor unipolar core utilisation, means that the transformer bulk is one of the major drawbacks of the flyback converter.

In order to obtain sufficiently high stored energy, the flyback primary inductance has to be significantly lower than required for a true transformer, since high peak currents are needed. This is normally achieved by gapping the core. The gap reduces the inductance, and most of the high peak energy is then stored in the gap, thus avoiding transformer saturation.

When the transistor turns off, the output voltage is back reflected through the transformer to the primary and in many cases this can be nearly as high as the supply voltage. There is also a voltage spike at turn-off due to the stored energy in the transformer leakage inductance. This means that the transistor must be capable of blocking approximately twice the supply voltage plus the leakage spike. Hence, for a 220V ac application where the dc link can be up to 385V, the transistor voltage limiting value must lie between 800 and 1000V.

II. SMPS TOPOLOGIES

Advantages.

The action of the flyback means that the secondary inductance is in series with the output diode when current is delivered to the load; i.e driven from a current source. This means that no filter inductor is needed in the output circuit. Hence, each output requires only one diode and output filter capacitor. This means the flyback is the ideal choice for generating low cost, multiple output supplies. The cross regulation obtained using multiple outputs is also very good (load changes on one output have little effect on the others) because of the absence of the output choke, which degrades this dynamic performance.

The flyback is also ideally suited for generating high voltage outputs. If a buck type LC filter was used to generate a high voltage, a very large inductance value would be needed to reduce the ripple current levels sufficiently to achieve the continuous mode operation required. This restriction does not apply to the flyback, since it does not require an output inductance for successful operation.

Disadvantages.

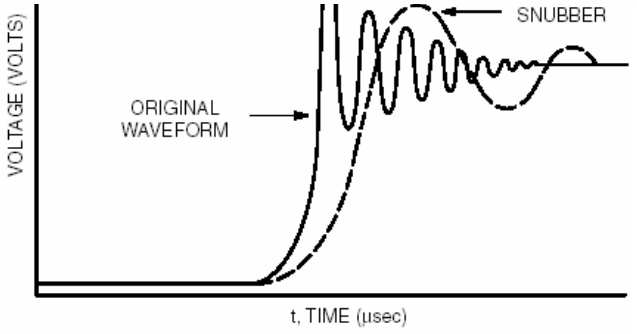
From the flyback waveforms in Fig. it is clear that the output capacitor is only supplied during the transistor off time. This means that the capacitor has to smooth a pulsating output current which has higher peak values than the continuous output current that would be produced in a forward converter, for example. In order to achieve low output ripple, very large output capacitors are needed, with very low equivalent series resistance (e.s.r). It can be shown that at the same frequency, an LC filter is approximately 8 times more effective at ripple reduction than a capacitor alone. Hence, flybacks have inherently much higher output ripples than other topologies. This, together with the higher peak currents, large capacitors and transformers, limits the flyback to lower output power applications in the 20 to 200W range. (It should be noted that at higher voltages, the required output voltage ripple magnitudes are not normally as stringent, and this means that the e.s.r requirement and hence capacitor size will not be as large as expected.)

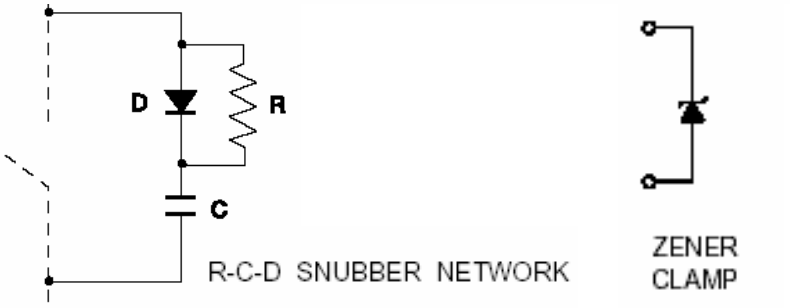
II. SMPS TOPOLOGIES

a. Single switch versus double switch flyback

In the single switch flyback, an overvoltage spike is applied across the power switch at each turn off. The peak value of this overvoltage depends upon the switching time, the circuit capacitance and the primary to secondary transformer leakage inductance. So, a single switch flyback nearly always requires a snubber circuit limiting this voltage spike (see figure 5).

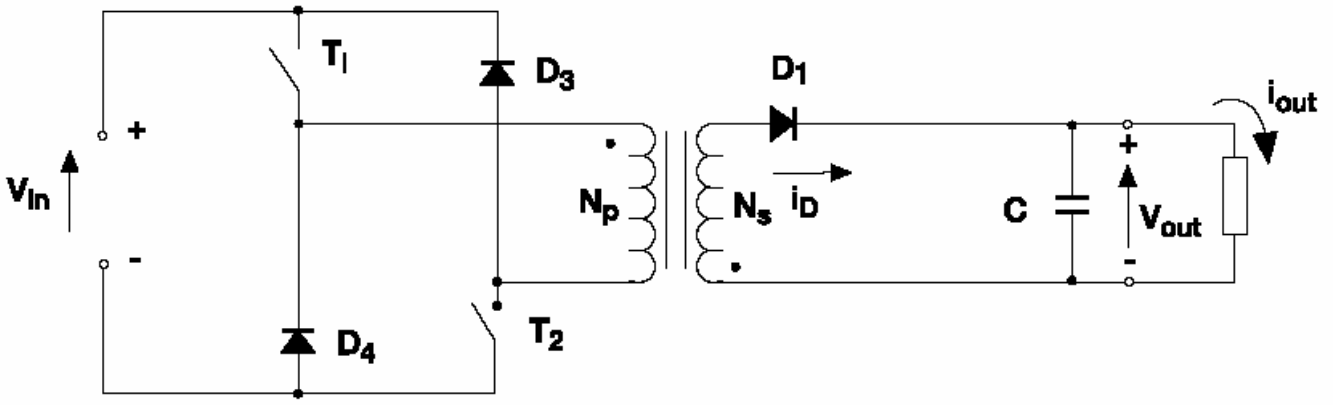
In a double switch flyback, the leakage inductance of the power transformer is much less critical (see figure). The two demagnetization diodes (D_1 and D_2) provide a single non dissipative way to systematically clamp the voltage across the switches to the input DC voltage V_{in}. This energy recovery system allows us to work at higher switching frequencies and with a better efficiency than that of the single switch structure. However, the double switch structure requires driving a high side switch. This double switch flyback is also known as asymmetrical half bridge flyback.





II. SMPS TOPOLOGIES

Isolated double switch flyback



* *Power switch:*

$$V_{CEV} \text{ or } V_{DSS} \geq V_{inmax}$$

* *Primary Rectifiers: D_3 and D_4*

$$V_{RRM} \geq V_{inmax}$$

II. SMPS TOPOLOGIES

b. Discontinuous versus continuous mode flyback

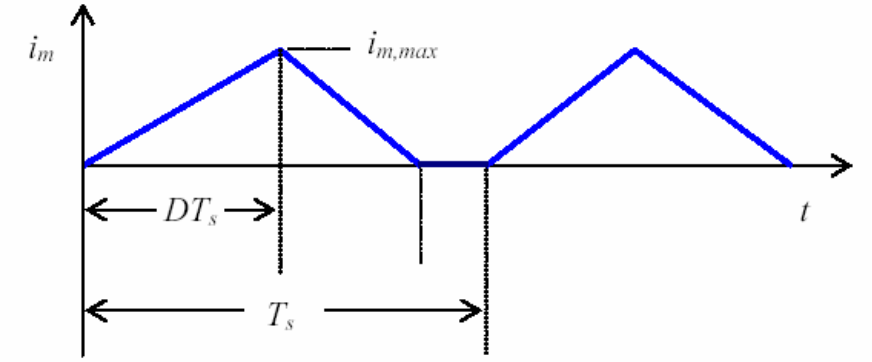
The flyback converter has two operating modes depending whether the primary inductance of the transformer is completely demagnetized or not.

Discontinuous mode

ADVANTAGES	DISADVANTAGES
- Zero turn-on losses for the power switch	- High peak currents in rectifiers and power switches
- Good transient line/load response	- Large output ripple: C_{out} (disc.) $\approx$ 2 $\cdot$ C_{out} (cont.)
- Feedback loop (single pole) easy to stabilize	
- Recovery time rectifier not critical: current is zero well before reverse voltage is applied	

II. SMPS TOPOLOGIES

Single switch flyback – input-output relationship for discontinuous operation



$$i_{m\,max} = \frac{V_d D T_s}{L_m}$$

$$V_d I_d = \frac{V_0^2}{R}$$

$$I_d = \frac{1}{2}\frac{V_d D T_s}{L_m} DT_s / T_s = \frac{V_d D^2 T_s}{2L_m}$$

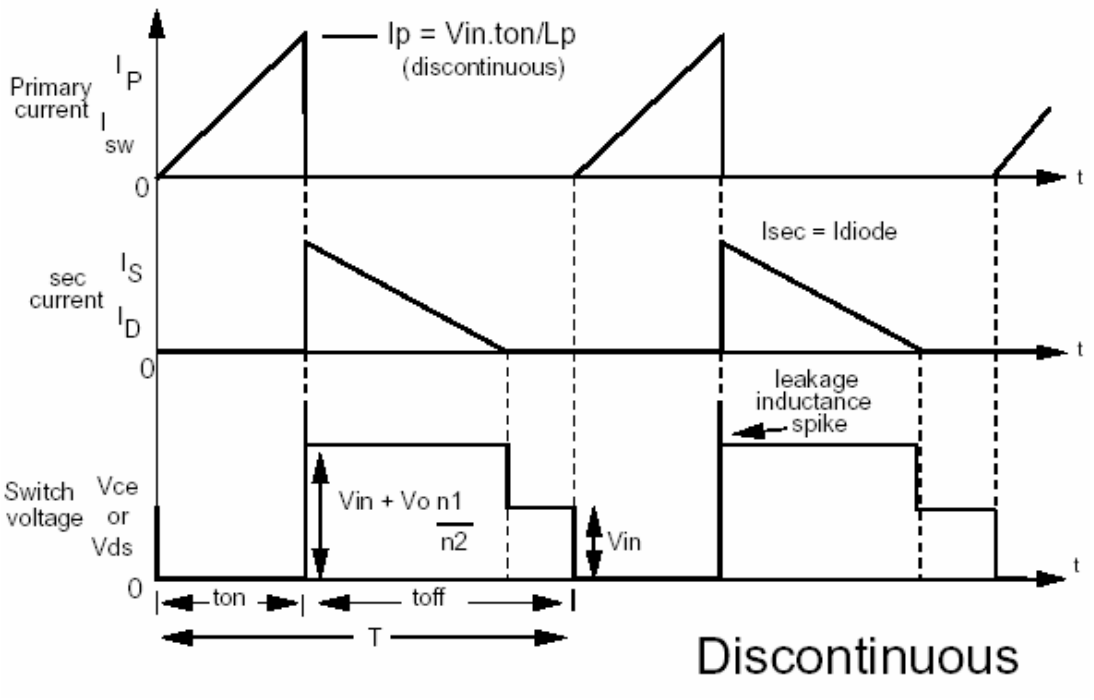
$$\therefore V_d I_d = \frac{V_d^2 D^2 T_s}{2L_m} = \frac{V_0^2}{R}$$

$$\therefore \frac{V_o}{V_d} = D\sqrt{\frac{T_s R}{2L_m}}$$

$$= D\sqrt{\frac{R}{2 f_s L_m}}$$

II. SMPS TOPOLOGIES

Discontinuous mode flyback waveforms



II. SMPS TOPOLOGIES

Semiconductor ratings (n = N_1/N_2, and η: efficiency)

*Power switch:

$$V_{CEV} \text{ or } V_{DSS} \geq V_{inmax} + nV_{out} + \text{leakage inductance spike}$$

* Secondary Rectifier:

$$V_{RRM} \geq V_{out} + \frac{V_{inmax}}{n}$$

* Power switch:

$$I_{Cpeak} \geq \frac{2P_{out}}{\eta V_{inmin}\,\delta_{max}}$$

$$I_{Drms} \geq \frac{2P_{out}}{\eta V_{inmin}\sqrt{(3\delta_{max})}}$$

* Rectifier:

$$I_{Fpeak} \geq \frac{2P_{out}}{V_{out}\ (1-\delta_{max})}$$

$$I_{F(AV)} \geq \frac{P_{out}}{V_{out}}$$

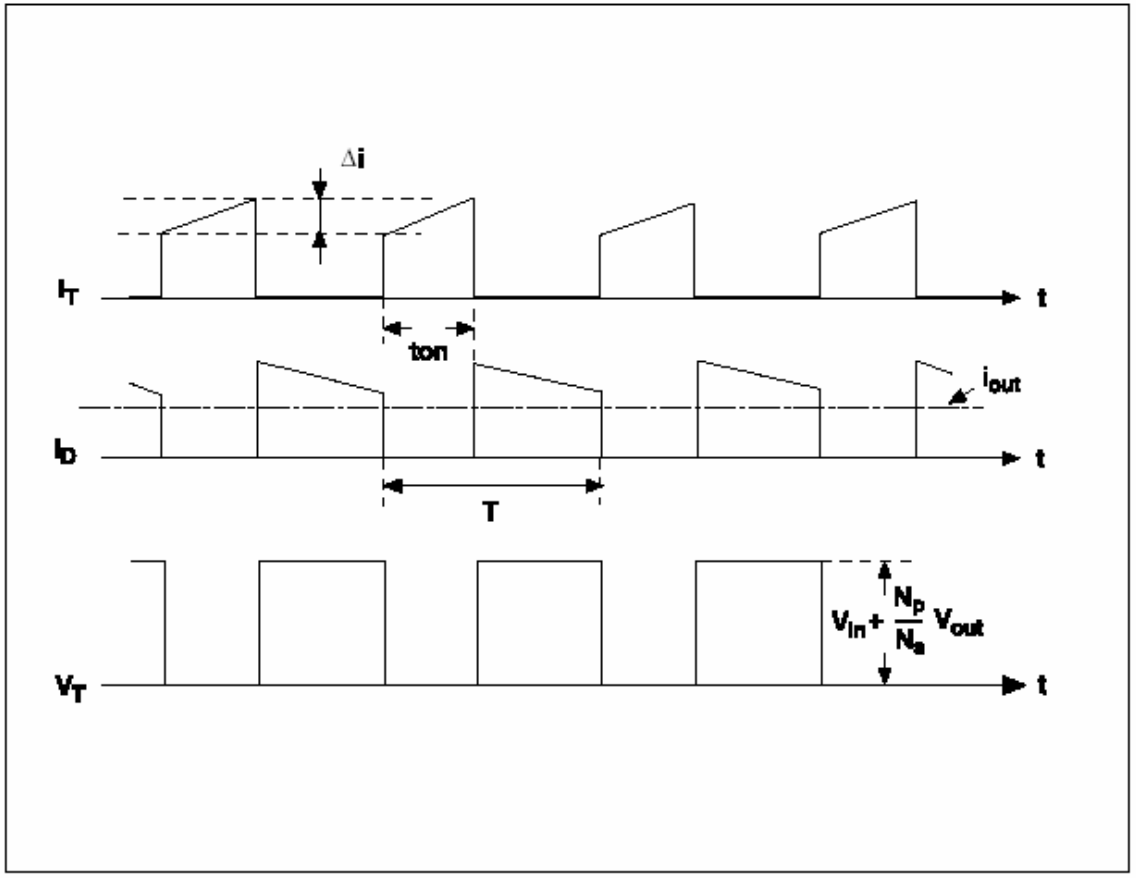
II. SMPS TOPOLOGIES

Continuous mode

ADVANTAGES	DISADVANTAGES
- Peak current of rectifier and switch is half the value of discontinuous mode	- Recovery time rectifier losses
- Low output ripple: C_{out} (cont.) $\approx$ 0.5 C_{out} (disc.)	-Feedback loop difficult to stabilize (2 poles and right half plane zero)

II. SMPS TOPOLOGIES

Continuous mode flyback waveforms



II. SMPS TOPOLOGIES

* *Power switch:*

$$I_{Cpeak} \geq \frac{2P_{outmax}}{\eta\, \delta_{max}\, V_{inmin}\, (1+A)}$$

$$I_{Drms} \geq \frac{2P_{out}}{\eta V_{inmin}} \sqrt{\frac{(1 + A + A^2)}{3\delta_{max}}}$$

* *Rectifier:*

$$I_{Fpeak} \geq \frac{2P_{out}}{V_{out}\,(1 - \delta_{max})(1+A)}$$

$$I_F(AV) \geq \frac{P_{out}}{V_{out}}$$

$$\text{with } A \geq = \frac{I_{peak} - \Delta I}{I_{peak}}$$

II. SMPS TOPOLOGIES

Flyback:

Max. Duty Cycle: Dmax or δmax = 0.45

*Power switch:

$$V_{CEV} \text{ or } V_{DSS} \geq V_{inmax} + nV_{out} + \text{leakage inductance spike}$$

* Secondary Rectifier:

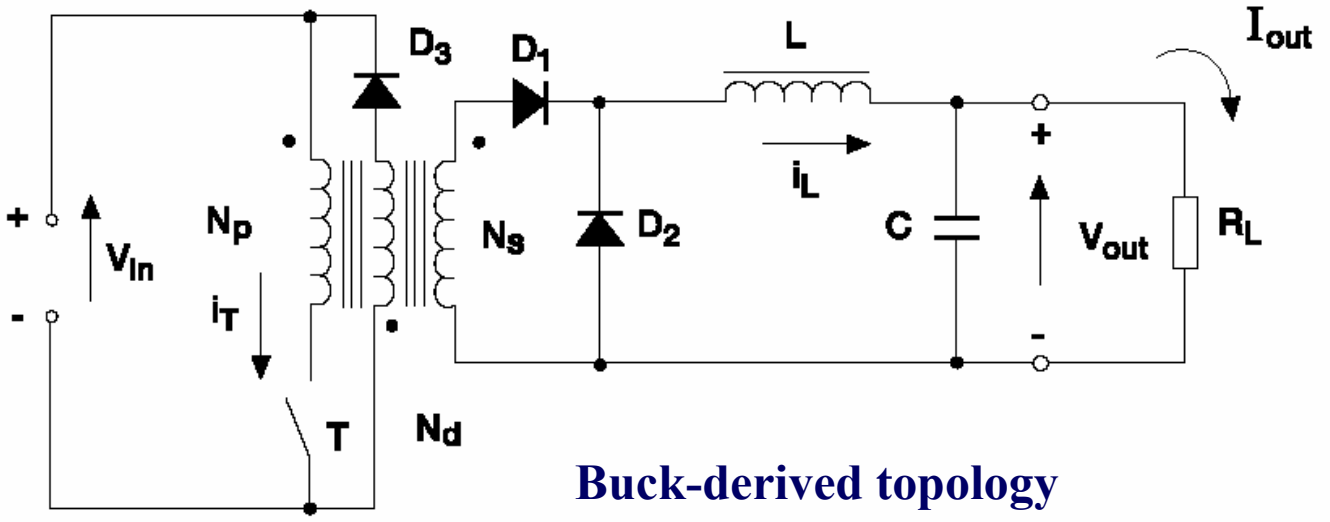
$$V_{RRM} \geq V_{out} + \frac{V_{inmax}}{n}$$

dc voltage gain:- (a) continuous $\frac{Vo}{Vin} = \frac{D}{1-D} \Big/ n$ (b) Discontinuous $\frac{Vo}{Vin} = D\sqrt{\frac{R_L}{2}\frac{T}{L_p}}$

Applications:- Lowest cost, multiple output supplies in the 20 to 200W range. E.g. mains input T.V. supplies, small computer supplies, E.H.T. supplies.

II. SMPS TOPOLOGIES

2.3.2. FORWARD CONVERTER
(Single-switch)



Buck-derived topology

II. SMPS TOPOLOGIES

FORWARD CONVERTER

- *It is one of the most widely used topologies for output powers under 200 W when the maximum input voltage is between 60-200 V_{DC}*

- *Above a maximum input voltage of 250 V_{DC} the maximum off stress on the transistor becomes too large*

- *It has one power transistor so it is economical*

- *Power is transferred when the power transistor is on. The transformer is reset after power transistor on time via reset diode and reset winding*

II. SMPS TOPOLOGIES

FORWARD CONVERTER

Basic Operation :

When the switch T is on :

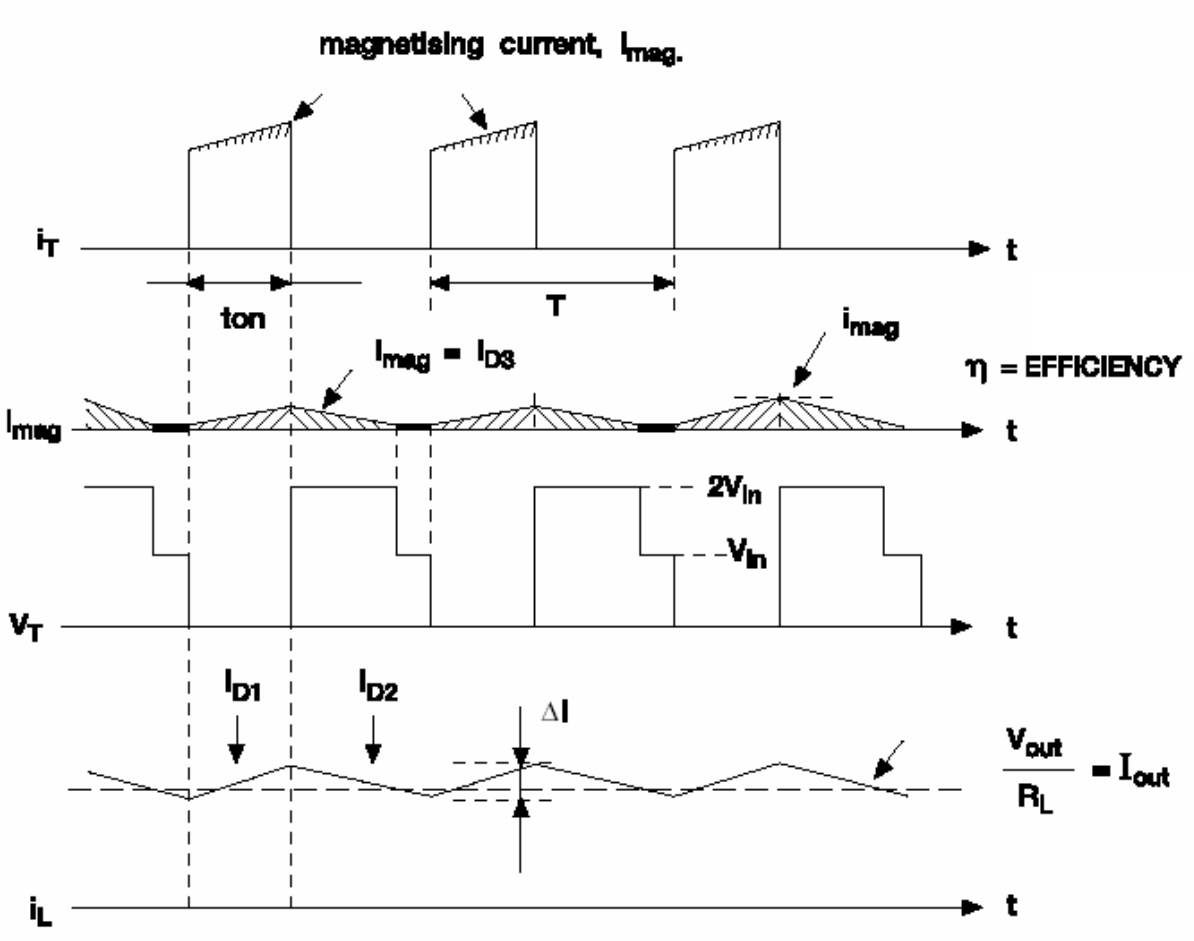
- **The dot end of the windings of the transformer go positive**
- **The primary voltage is reflected to the secondary by the turns ratio of the transformer**
- **The rectifier diode D1 is forward biased, the freewheeling diode D2 is reverse biased**
- **The inductor current starts to rise linearly (ramp on a step waveform)**
- **The load current reflected to the primary flows through the power transistor T**
- **Energy is transferred to the load**
- **The magnetizing current of the transformer ramps up linearly from zero**

II. SMPS TOPOLOGIES

When the switch T is off :

- The magnetizing current stored in the magnetizing inductance reverses the polarity of the voltage across the primary winding
- All the dot ends of the primary and secondary windings go negative
- The voltage across the power transistor equals 2 V_{in} (for $N_p=N_d$)
- Diode D1 is off, freewheeling diode D2 is on,clamp diode is on
- The inductor current starts to decrease linearly
- The transformer is reset via the clamp diode D3, and the reset winding
- The core has moved to in one direction on its hysteresis loop and now it returns to its original position on the loop
- Magnetizing current falls linearly to zero

II. SMPS TOPOLOGIES



II. SMPS TOPOLOGIES

* *Power switch:*

$$V_{CEV} \text{ or } V_{DSS} \geq V_{inmax}\left[1 + \frac{N_p}{N_d}\right] + \text{leakage inductance spike}$$

$$I_{cpeak} \geq \frac{1.2.P_{out}}{\eta V_{inmin} \cdot \delta_{max}}$$

$$I_{Drms} \geq \frac{1.2.P_{out}}{\eta V_{inmin} \cdot \sqrt{\delta_{max}}}$$

II. SMPS TOPOLOGIES

**Rectifiers:*

FORWARD D1:

$$V_{RRM} \geq V_{inmax} \cdot \frac{N_s}{N_d} + \text{leakage inductance spike}$$

$$I_{F(av)} \geq I_{out} \cdot \delta_{max}$$

FREEWHEELING D2:

$$V_{RRM} \geq \frac{V_{inmax} \cdot (V_{out} + V_F)}{V_{inmin} \cdot \delta_{max}}$$

$$I_{F(av)} \geq I_{out}$$

DEMAGNETIZATION D3:

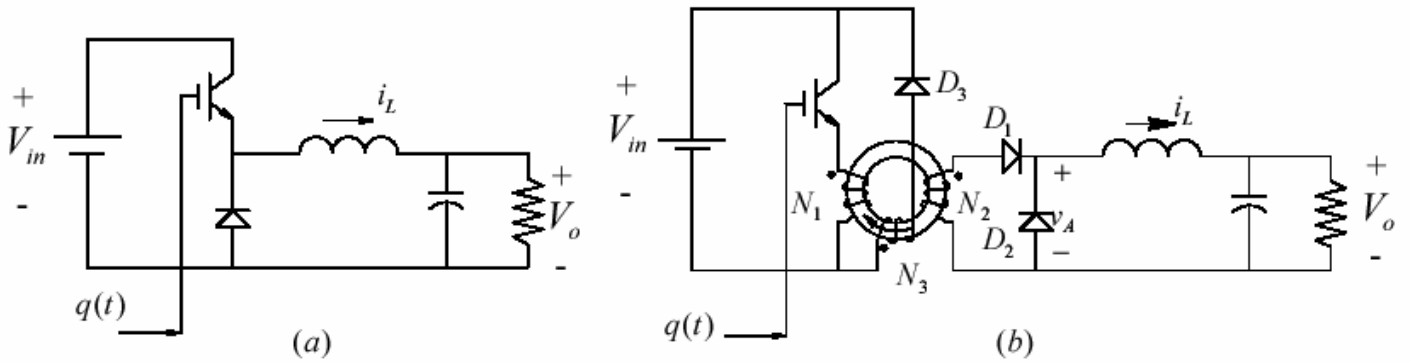
$$V_{RRM} \geq \left[1 + \frac{N_d}{N_p}\right] V_{inmax}$$

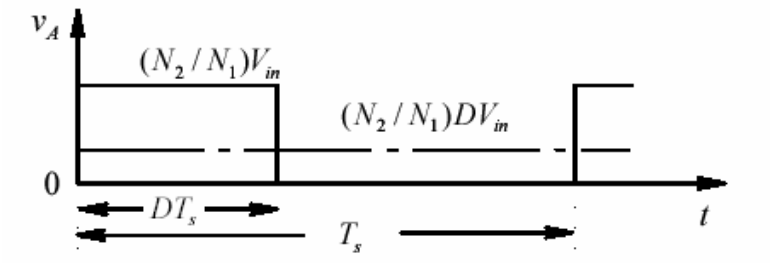
$$I_{F(av)} \geq \frac{I_{magnpeak}}{2} \cdot \delta_{max}$$

II. SMPS TOPOLOGIES

FORWARD CONVERTER

Buck converter ⇒ **Forward Converter (Buck derived)**





$$V_o = \left(\frac{N_2}{N_1}\right) D V_{in}$$

II. SMPS TOPOLOGIES

Forward Converter

Operation Principles

The forward converter is also a single switch isolated topology, and is shown in Fig. This is based on the buck converter described earlier, with the addition of a transformer and another diode in the output circuit. The characteristic LC output filter is clearly present.

In contrast to the flyback, the forward converter has a true transformer action, where energy is transferred directly to the output through the inductor during the transistor on-time. It can be seen that the polarity of the secondary winding is opposite to that of the flyback, hence allowing direct current flow through blocking diode D1. During the on-time, the current flowing causes energy to be built up in the output inductor L1. When the transistor turns off, the secondary voltage reverses, D1 goes from conducting to blocking mode and the freewheel diode D2 then becomes forward biased and provides a path for the inductor current to continue to flow. This allows the energy stored in L1 to be released into the load during the transistor off time.

The forward converter is always operated in continuous mode (in this case the output inductor current), since this produces very low peak input and output currents and small ripple components. Going into discontinuous mode would greatly increase these values, as well as increasing the amount of switching noise generated. No destabilising right hand plane zero occurs in the frequency response of the forward in continuous mode (as with the buck).
This means that the control problems that existed with the continuous flyback are not present here. So there are no real advantages to be gained by using discontinuous mode operation for the forward converter.

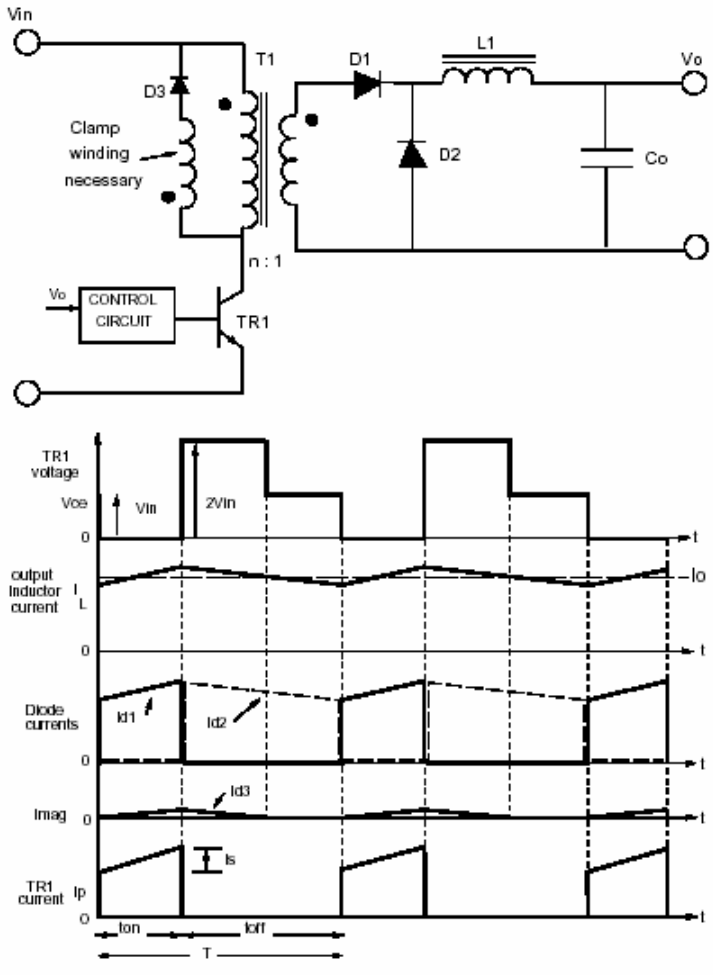
Advantages.

As can be seen from the waveforms in Fig. , the inductor current I_L, which is also the output current, is always continuous. The magnitude of the ripple component, and hence the peak secondary current, depends upon the size of the output inductor. Therefore, the ripple can be made relatively small compared to the output current, with the peak current minimised. This low ripple, continuous output current is very easy to smooth, and so the requirements for the output capacitor size, e.s.r and peak current handling are far smaller than they are for the flyback.

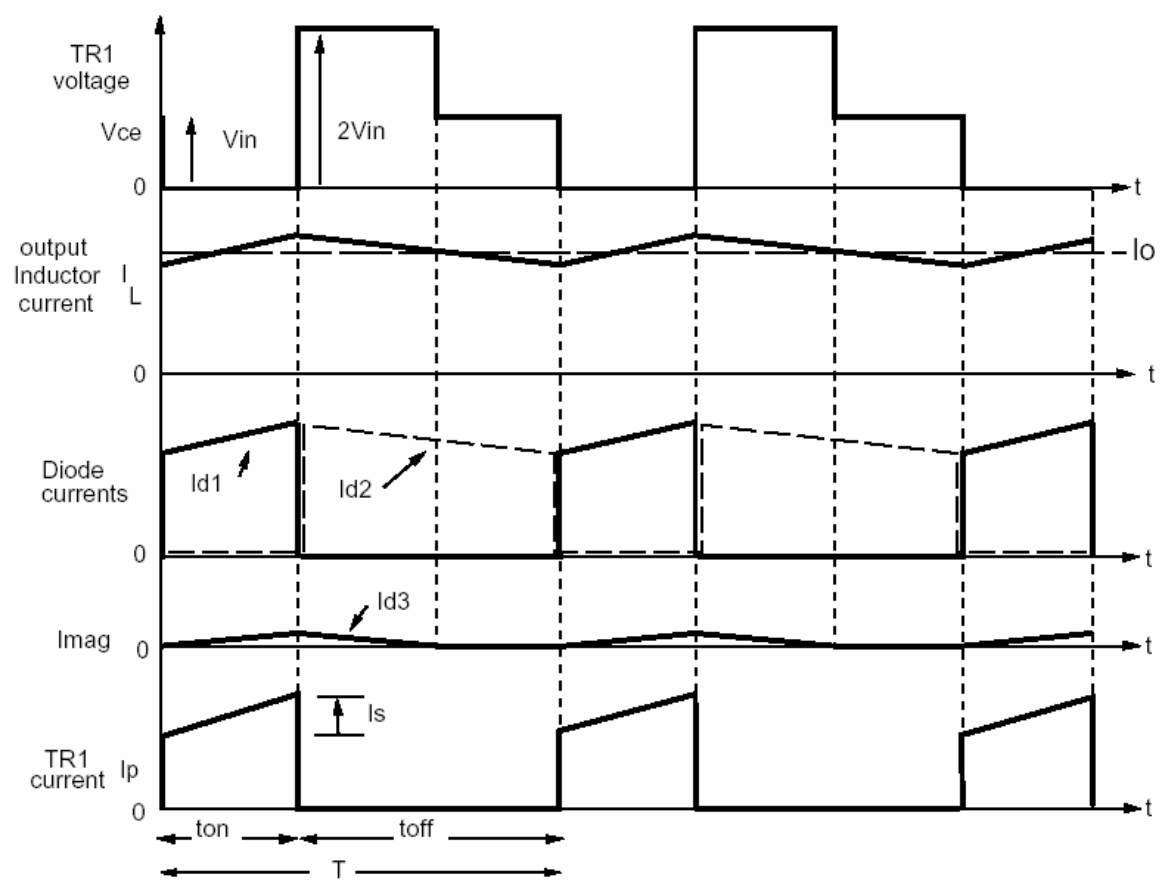
II. SMPS TOPOLOGIES

Since the transformer in this topology transfers energy directly there is negligible stored energy in the core compared to the flyback. However, there is a small magnetisation energy required to excite the core, allowing it to become an energy transfer medium. This energy is very small and only a very small primary magnetisation current is needed. This means that a high primary inductance is usually suitable, with no need for the core air gap required in the flyback. Standard un-gapped ferrite cores with high permeabilities (2000-3000) are ideal for providing the high inductance required. Negligible energy storage means that the forward converter transformer is considerably smaller than the flyback, and core loss is also much smaller for the same throughput power. However, the transformer is still operated asymmetrically, which means that power is only transferred during the switch on-time, and this poor utilisation means the transformer is still far bigger than in the symmetrical types.

The transistors have the same voltage rating as the discontinuous flyback (see disadvantages), but the peak current required for the same output power is halved, and this can be seen in the equations given for the forward converter. This, coupled with the smaller transformer and output filter capacitor requirements means that the forward converter is suitable for use at higher output powers than the flyback can attain.



II. SMPS TOPOLOGIES



Forward converter waveforms

II. SMPS TOPOLOGIES

Disadvantages.

Because of the unipolar switching action of the forward converter, there is a major problem in how to remove the core magnetisation energy by the end of each switching cycle. If this did not happen, there would be a net dc flux build-up, leading to core saturation, and possible transistor destruction. This magnetisation energy is removed automatically by the push-pull action of the symmetrical types. In the flyback this energy is dumped into the load at transistor turn-off. However, there is no such path in the forward circuit.

This path is provided by adding an additional reset winding of opposite polarity to the primary. A clamp diode is added, such that the magnetisation energy is returned to the input supply during the transistor off time. The reset winding is wound bifilar with the primary to ensure good coupling, and is normally made to have the same number of turns as the primary. (The reset winding wire gauge can be very small, since it only has to conduct the small magnetisation current.) The time for the magnetisation energy to fall to zero is thus the same duration as the transistor on-time. This means that the maximum theoretical duty ratio of the forward converter is 0.5 and after taking into account switching delays, this falls to 0.45. This limited control range is one of the drawbacks of using the forward converter. The waveform of the magnetisation current is also shown in Fig. The clamp winding in the flyback is optional, but is always needed in the forward for correct operation.

Due to the presence of the reset winding, in order to maintain volt-sec balance within the transformer, the input voltage is back reflected to the primary from the clamp winding at transistor turn-off for the duration of the flow of the magnetisation reset current through D3. (There is also a voltage reversal across the secondary winding, and this is why diode D1 is added to block this voltage from the output circuit.) This means that the transistor must block two times Vin during switch-off. The voltage returns to Vin after reset has finished, which means transistor turn-on losses will be smaller. The transistors must have the same added burden of the voltage rating of the flyback, i.e 400V for 110V mains and 800V for 220V mains applications.

Output diode selection.

The diodes in the output circuit both have to conduct the full magnitude of the output current. They are also subject to abrupt changes in current, causing a reverse recovery spike, particularly in the freewheel diode, D2. This spike can cause additional turn-on switching loss in the transistor, possibly causing device failure in the absence of snubbing. Thus, very high efficiency, fast trr diodes are required to minimise conduction losses and to reduce the reverse recovery spike. These requirements are met with Schottky diodes for outputs up to 20V, and fast recovery epitaxial diodes for higher voltage outputs. It is not normal for forward converter outputs to exceed 100V because of the need for a very large output choke, and flybacks are normally used.

II. SMPS TOPOLOGIES

The forward converter transfers directly the energy from the input source to the load during the on-time of the power switch. During off-time of the power switch, the energy is freewheeling through the output inductor and the rectifier D_2, like in a chopper

$$V_{out} = D \frac{V_{in}}{n}$$

A forward regulator can be realized with a single switch structure or with a double switch structure, according to the way the energy stored in the transformer primary inductance is demagnetized. Forward converters are commonly used for output power up to 250W in single switches, and up to 1kW in double switch structures.

Single switch vs. double switch forward

In the single switch forward, the magnetizing energy stored in the primary inductance is restored to the input source by a demagnetization winding N_d. Most commonly, the primary and the demagnetization windings have the same number of turns.

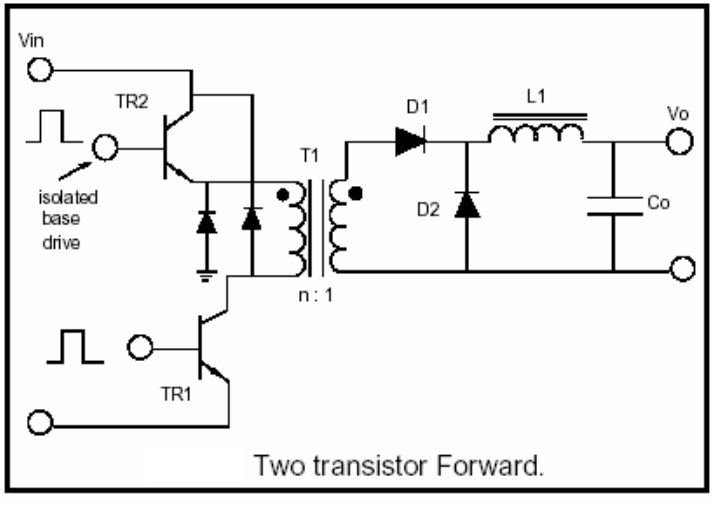
So, at turn-off, the power switch has to withstand twice the input voltage during the demagnetization time, and then, once the input voltage (see figure).

The demagnetization and primary windings have to be tightly coupled to reduce the voltage spike - more than the theoretical $2 V_{in}$ - occuring at turn-off across the power switch.

II. SMPS TOPOLOGIES

Double-switch forward converter:

In order to avoid the use of higher voltage transistors, the two transistor version of the forward can be used. This circuit, shown in Fig. _, is very similar to the two transistor flyback and has the same advantages. The voltage across the transistor is again clamped to V_{in}, allowing the use of faster more efficient 400 or 500V devices for 220V mains applications. The magnetisation reset is achieved through the two clamp diodes, permitting the removal of the clamp winding.



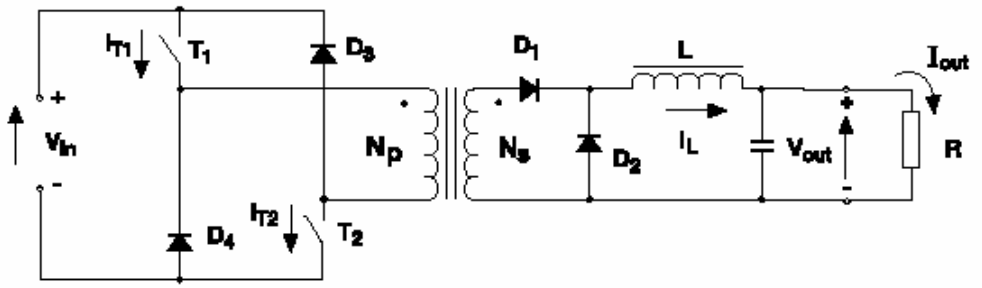
Two transistor Forward.

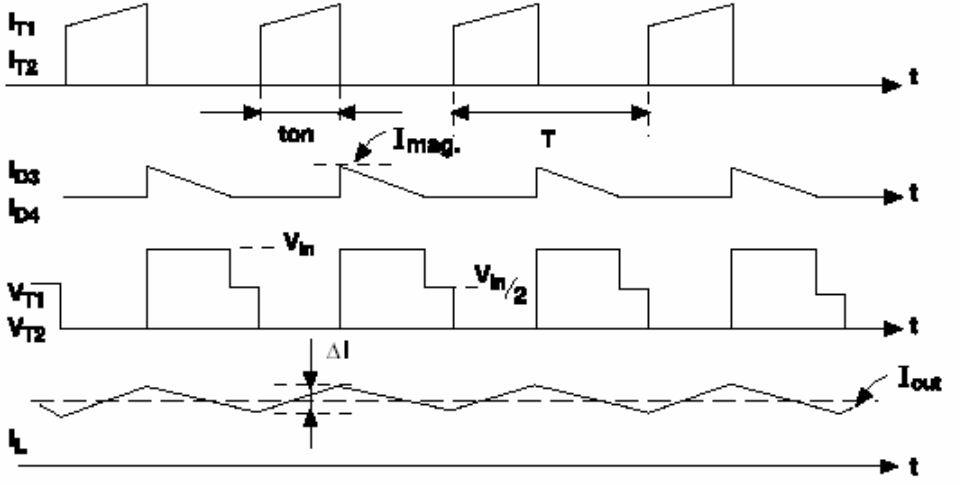
The two transistor version is popular for off-line applications. It provides higher output powers and faster switching frequencies. The disadvantages are again the extra cost of the higher component count, and the need for an isolated drive for the top transistor.

Although this converter has some drawbacks, and utilises the transformer poorly, it is a very popular selection for the power range mentioned above, and offers simple drive for the single switch and cheap component costs. Multiple output types are very common. The output inductors are normally wound on a single core, which has the effect of improving dynamic cross regulation, and if designed correctly also reduces the output ripple magnitudes even further. The major advantage of the forward converter is the very low output ripple that can be achieved for relatively small sized LC components. This means that forward converters are normally used to generate lower voltage, high current multiple outputs such as 5, 12, 15, 28V from mains off-line applications, where lower ripple specifications are normally specified for the outputs. The high peak currents that would occur if a flyback was used would place an impossible burden on the smoothing capacitor.

II. SMPS TOPOLOGIES

Double-switch forward converter waveforms





$\delta = \frac{ton}{T}$

η = EFFICIENCY

$f = \frac{1}{T}$

L_p = PRIMARY INDUCTANCE

II. SMPS TOPOLOGIES

In the "double switch forward", also called asymmetrical half bridge forward, the magnetizing energy stored in the primary inductance is automatically returned to the bulk capacitor by the two demagnetization diodes

The two power switches and demagnetisation diodes have to withstand only once the input voltage V_{in}. As for the double switch flyback, the asymmetrical half bridge needs a floating gate drive for the high side switch.

** Power switch:*

$$V_{CEV} \text{ or } V_{DSS} \geq V_{inmax}$$

$$I_{Drms} \geq \frac{1.2.P_{out}}{\eta V_{inmin} \cdot \sqrt{\delta_{max}}}$$

** Rectifiers:*

FORWARD D1:

$$V_{RRM} \geq \frac{V_{inmax}\ (V_{out} + V_F)}{V_{inmin}\ .\ \delta_{max}}$$

$$I_{F(av)} \geq I_{out}\ .\delta_{max}$$

FREEWHEELING D2:

$$V_{RRM} \geq V_{inmax}\ (V_{out} + V_F)$$

$$I_{F(av)} \geq I_{out}$$

II. SMPS TOPOLOGIES

Forward:

Max. Duty Cycle: Dmax or δmax = 0.45

Max transistor voltage, V_{ce} or $V_{ds} = 2V_{in(max)}$, **for Nd= Np**

Max *transistor current*, I_C ; $I_D = \dfrac{P_{out}}{\eta \quad D_{\max} \quad V_{\min}}$

dc voltage gain. $\dfrac{Vo}{Vin} = \quad D / n$

Applications:- Low cost, low output ripple, multiple output supplies in the 50 to 400W range. E.g. small computer supplies, DC/DC converters.

II. SMPS TOPOLOGIES

2.4. Symmetrical Converters

➢ *Symmetrical converters use an even number of switches. They better exploit the transformer's magnetic circuit than the asymmetrical converters. So, smaller size and weight can be achieved.*

The three most common structures among symmetrical converters are:

- *The Push Pull*
- *The Half Bridge*
- *The Full Bridge*

II. SMPS TOPOLOGIES

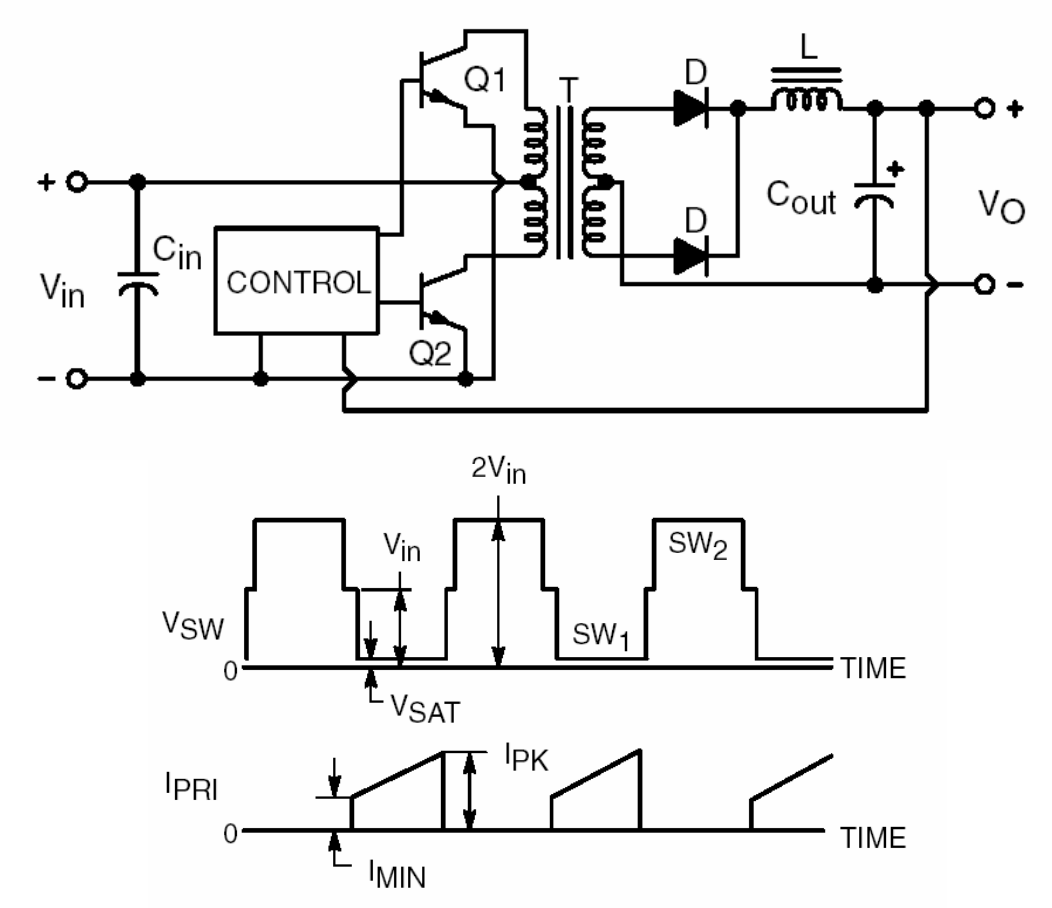
- *The push-pull, half-bridge, and full-bridge converters have true transformer action, and ideally store no energy, hence no air gap is needed.*

- *In the symmetrical converters, which always require an even number of transistor switches, the full available flux swing in both quadrants of the B-H loop is used, thus utilising the core much more effectively.*

- *Symmetrical converters can therefore produce more power than the asymmetrical ones. The 3 major symmetrical topologies used in practice are the push-pull, the half-bridge, and the full-bridge types.*

II. SMPS TOPOLOGIES

2.4.1. PUSH-PULL CONVERTER



II. SMPS TOPOLOGIES

PUSH-PULL CONVERTER

- **The push-pull converter is one of the oldest topologies**
- **It can be used up to power levels of several hundreds of Watts**
- **It consists of a power transformer, two power transistors, and two rectifier diode on the secondary side**
- **Compared to forward converter it can double the output power from the same core operating at the same peak flux density (but the core in the push-pull topology will be warmer since the core loss will be doubled)**
- **The copper losses, however, in both half primaries of the push-pull transformer equals the copper loss of the transformer of the forward converter having half output power**

II. SMPS TOPOLOGIES

Basic Operation :

When either of the switches (Q1 or Q2) is on:

- One of the diodes on the secondary side is forward biased
- The input voltage is applied to the upper half of the primary winding or to the lower half of the primary winding
- A square voltage pulse is applied to the input of the LC filter
- There are now 2 power pulses per period unlike the forward converter
- The inductor current ramps up linearly
- The core of the power transformer is excited bidirectionally
- (1. and 3. quadrant operation)

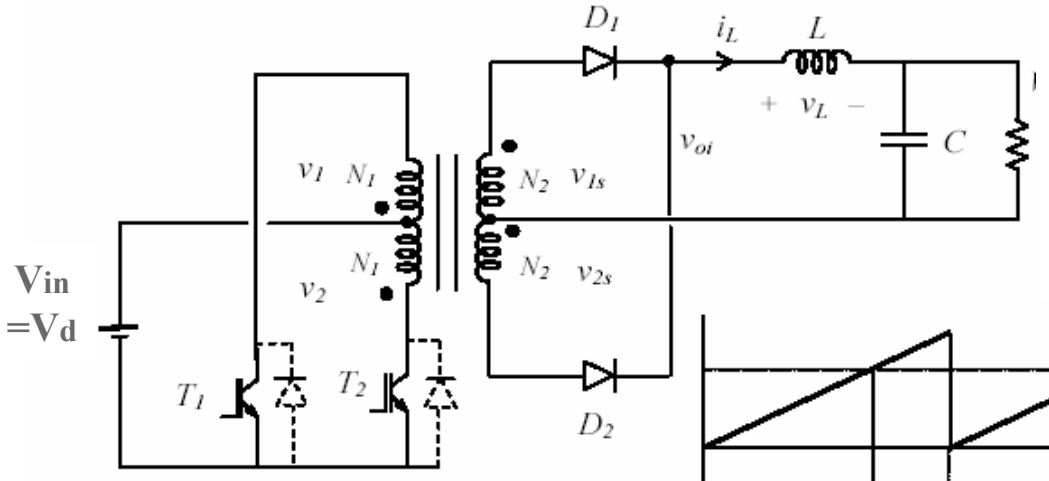
II. SMPS TOPOLOGIES

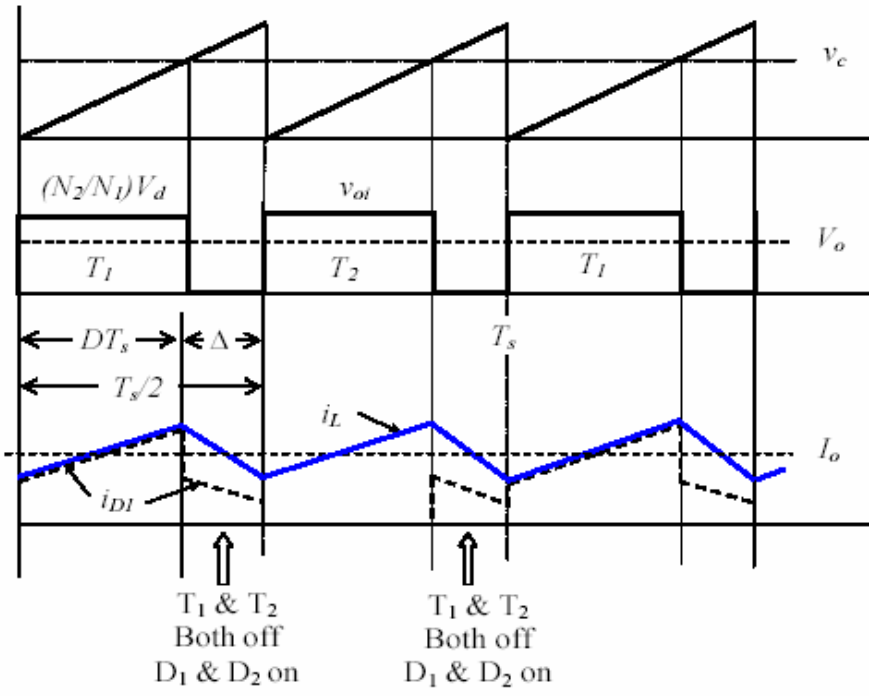
The power switch carries output inductor current reflected to the primary which has a ramp on a step waveform. The voltage stress of the power transistor which is off equals 2Vin

When the switches are off :

- The output inductor current freewheels through the rectifier diodes on the secondary side
- The voltage stress on the power switches equals V_{in} (disregarding the leakage spike)
- The output inductor current decreases linearly

II. SMPS TOPOLOGIES





Push-Pull Converter Operation:

II. SMPS TOPOLOGIES

Steady-state analysis:

When T_1 is ON, $v_1 = v_d$, $v_{1s} = \dfrac{N_2}{N_1} V_d$

and $v_L = \dfrac{N_2}{N_1} V_d - V_o$

$$\therefore \Delta i_L = \frac{\dfrac{N_2}{N_1} V_d - V_o}{L} DT_s$$

When T_2 is ON,

$$v_L = \frac{N_2}{N_1} V_d - V_o$$

and $$\therefore \Delta i_L = \frac{\dfrac{N_2}{N_1} V_d - V_o}{L} DT_s$$

When both T_1 and T_2 are off diodes D_1 and D_2 both conduct and share i_L equally. v_{oi} is then zero during this period.

II. SMPS TOPOLOGIES

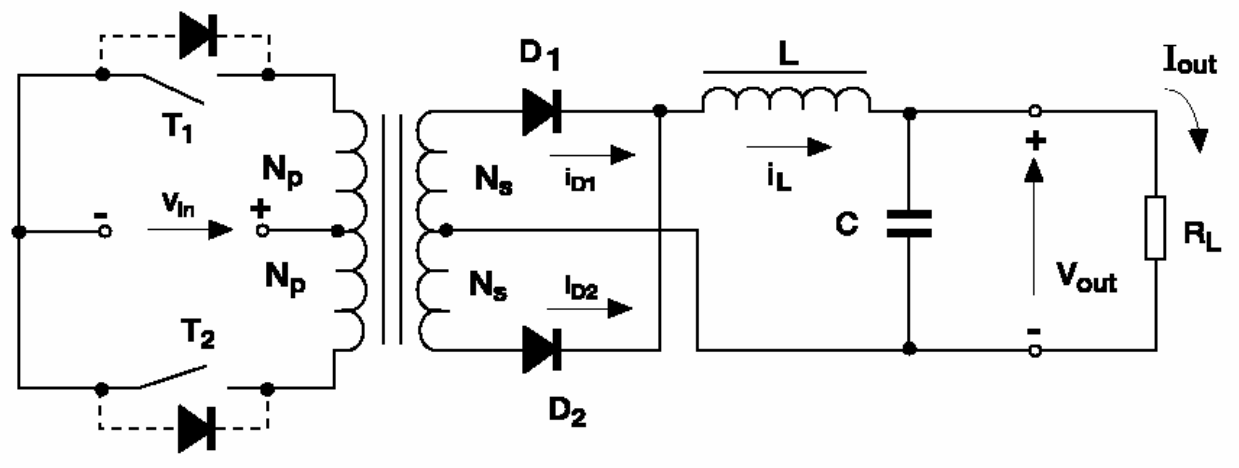
$$\therefore v_L = -v_0$$

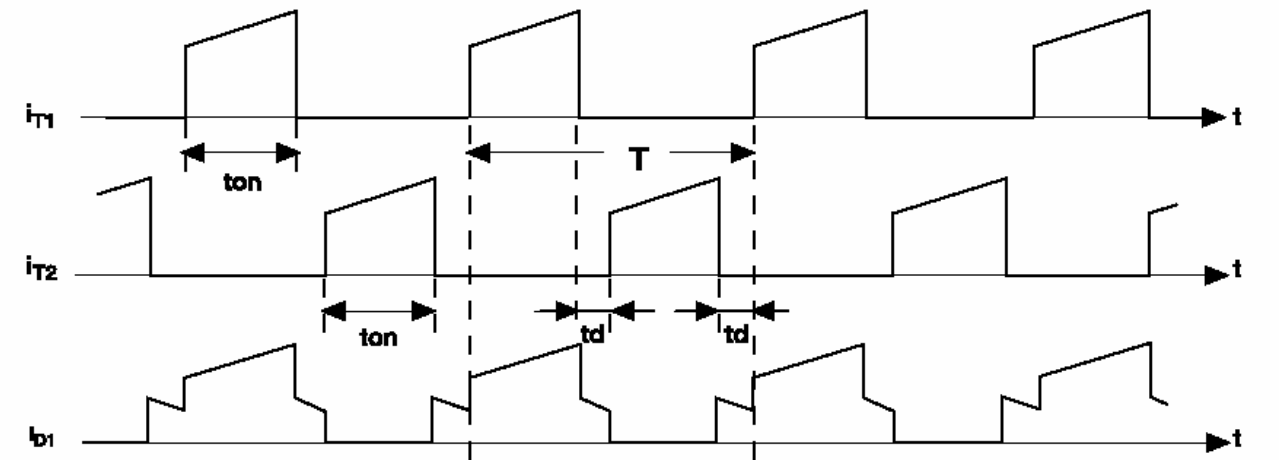
From $\frac{1}{2}\int v_L = 0$

$$\frac{\frac{N_2}{N_1}V_d - V_0}{L} DT_s - \frac{V_0}{L}\left(\frac{1}{2} - D\right)T_s = 0$$

$$\therefore \frac{V_0}{V_d} = 2\frac{N_2}{N_1}D$$

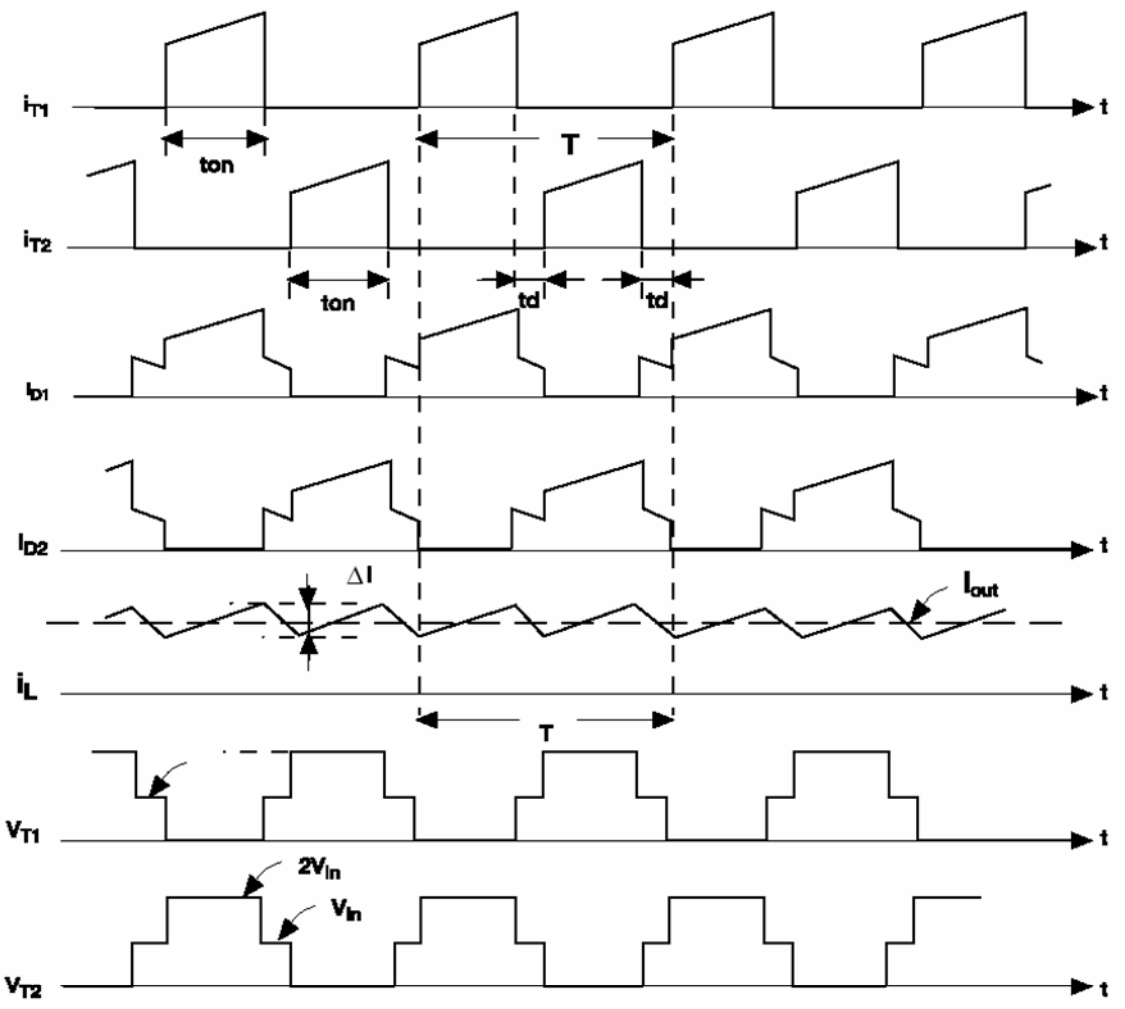
II. SMPS TOPOLOGIES





II. SMPS TOPOLOGIES

Push-Pull converter waveforms:



II. SMPS TOPOLOGIES

* *Power switch*

$$I_{Dpeak} \text{ or } I_{Cpeak} \geq \frac{P_{out}}{\eta V_{inmin}}$$

$$V_{CEV} \text{ or } V_{DSS} \geq 2V_{inmax} + \text{leakage inductance spike}$$

* *Rectifier*

$$V_{RRM} \geq \frac{(V_{out} + V_F)\, V_{inmax}}{\delta_{max}.V_{inmin}} + \text{Voltage spike}$$

$$I_{F(av)} \geq \frac{I_{outmax}}{2}$$

II. SMPS TOPOLOGIES

Push-Pull Converter Operation:

T_1 and T_2 switches (see figure) are alternately turned-on during a time t_{on}. The secondary circuit operates at twice the switching frequency.

A deadtime t_d between the end of conduction of one switch and the turn-on time of the other one is required in order to avoid simultaneous conduction of the two switches.

$$V_{out} = 2\frac{\delta V_{in}}{n}$$

Moreover, the snubber network in symmetrical converters must be carefully designed, since they inter-react with one another.

II. SMPS TOPOLOGIES

To utilise the transformer flux swing fully, it is necessary to operate the core symmetrically as described earlier. This permits much smaller transformer sizes and provides higher output powers than possible with the single ended types. The symmetrical types always require an even number of transistor switches. One of the best known of the symmetrical types is the push-pull converter shown in Fig.

The primary is a centre-tapped arrangement and each transistor switch is driven alternately, driving the transformer in both directions. The push-pull transformer is typically half the size of that for the single ended types, resulting in a more compact design. This push-pull action produces natural core resetting during each half cycle, hence no clamp winding is required. Power is transferred to the buck type output circuit during each transistor conduction period. The duty ratio of each switch is usually less than 0.45. This provides enough dead time to avoid transistor cross conduction. The power can now be transferred to the output for up to 90% of the switching period, hence allowing greater throughput power than with the single-ended types. The push-pull configuration is normally used for output powers in the 100 to 500W range.

The bipolar switching action also means that the output circuit is actually operated at twice the switching frequency of the power transistors, as can be seen from the waveforms in Fig. Therefore, the output inductor and capacitor can be even smaller for similar output ripple levels. Push-pull converters are thus excellent for high power density, low ripple outputs.

The centre-tap arrangement also means that extra copper is needed for the primary, and very good coupling between the two halves is necessary to minimise possible leakage spikes. It should also be noted that if snubbers are used to protect the transistors, the design must be very precise since each tends to interact with the other. This is true for all symmetrically driven converters.

These disadvantages usually dictate that the push-pull is normally operated at lower voltage inputs such as 12, 28 or 48V. DC-DC converters found in the automotive and telecommunication industries are often push-pull designs. At these voltage levels, transformer saturation is easier to avoid.

II. SMPS TOPOLOGIES

Advantages.

As stated, the push-pull offers very compact design of the transformer and output filter, while producing very low output ripple. So if space is a premium issue, the push-pull could be suitable. The control of the push-pull is similar to the forward, in that it is again based on the continuous mode buck. When closing the feedback control loop, compensation is relatively easy. For multiple outputs, the same recommendations given for the forward converter apply.

Clamp diodes are fitted across the transistors, as shown. This allows leakage and magnetisation energy to be simply channelled back to the supply, reducing stress on the switches and slightly improving efficiency.

The emitter or source of the power transistors are both at the same potential in the push-pull configuration, and are normally referenced to ground. This means that simple base drive can be used for both, and no costly isolating drive transformer is required. (This is not so for the bridge types which are discussed latter.)

Disadvantages.

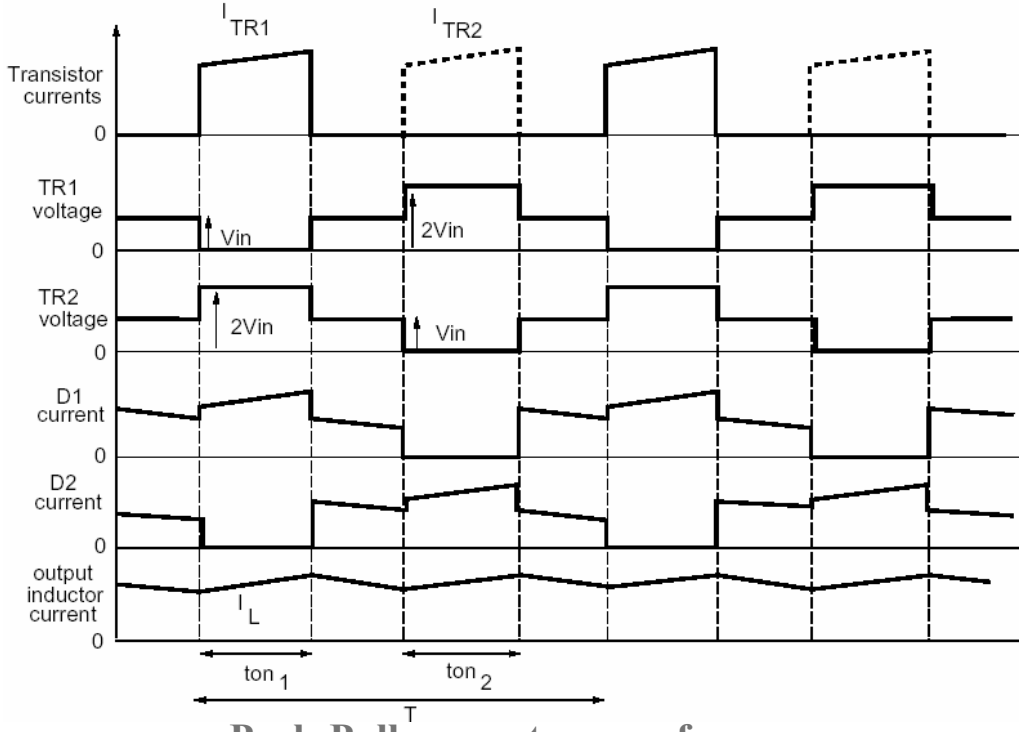
One of the main drawbacks of the push-pull converter is the fact that each transistor must block twice the input voltage due to the doubling effect of the centre-tapped primary, even though two transistors are used. This occurs when one transistor is off and the other is conducting. When both are off, each then blocks the supply voltage, this is shown in the waveforms in Fig. This means that TWO expensive, less efficient 800 to 1000V transistors would be required for a 220V off-line application.

A further major problem with the push-pull is that it is prone to flux symmetry imbalance. If the flux swing in each half cycle is not exactly symmetrical, the volt-sec will not balance and this will result in transformer saturation, particularly for high input voltages. Symmetry imbalance can be caused by different characteristics in the two transistors such as storage time in a bipolar and different on-state losses.

II. SMPS TOPOLOGIES

Current mode control.

The introduction of current mode control circuits has also benefited the push-pull type. In this type of control, the primary current is monitored, and any imbalance which occurs is corrected on a cycle by cycle basis by varying the duty cycle immediately. Current mode control completely removes the symmetry imbalance problem, and the possibilities of saturation are minimised. This has meant that push-pull designs have become more popular in recent years, with some designers even using them in off-line applications.



Push-Pull converter waveforms

II. SMPS TOPOLOGIES

Push-Pull converter

Max transistor voltage, V_{ce} or V_{ds} = $2V_{in(max)}$ + leakage spike.

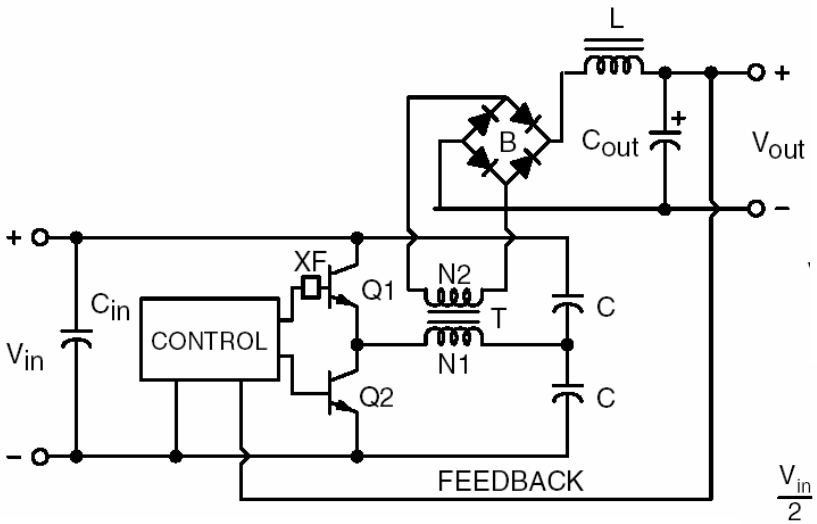
$$\text{Max } transistor current, I_C \quad ; \quad I_D = \frac{P_{out}}{\eta \quad D_{max} \quad V_{min}}$$

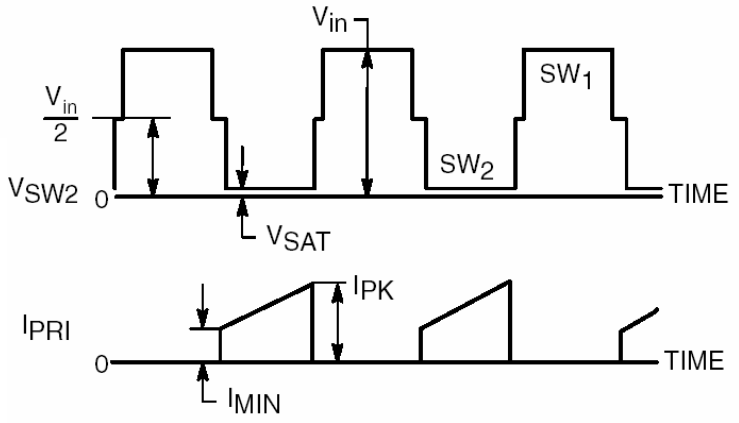
dc voltage gain:- $\frac{Vo}{Vin} = 2 \quad D/n$

Applications:- Compact design, very low output ripple supplies in the 100 to 500W range. More suited to low input applications. E.g. battery, 28, 40V inputs, high current outputs. Telecommunication supplies.

II. SMPS TOPOLOGIES

2.4.2. HALF BRIDGE CONVERTER





II. SMPS TOPOLOGIES

HALF BRIDGE CONVERTER

- **The bridge topologies are used mainly in off-line converters where twice the rectified DC would be quite high**
- An additional feature of bridge topologies is that the primary leakage inductance spikes are clamped to DC supply bus and any energy stored in the leakage inductance is returned to the input bus
- **Half bridge converter is widely used in equipment where the AC input voltage is 220 V**
- Peak primary current and maximum transistor off-voltage stress determine the practical maximum available output power
- **This limit is about 400-500 W**

II. SMPS TOPOLOGIES

Basic operation:

When either of the switches is (Q1,Q2) on:

- The primary of the transformer is connected across the capacitor whose voltage is half of the input DC voltage
- A square wave having amplitude half of the input DC voltage is generated
- This alternating waveform is rectified by the full wave rectifier on the secondary side and it is applied to the input of LC filter
- The output inductor current ramps up linearly
- The core of the power transformer is excited bidirectionally (1. and 3. quadrant operation)

II. SMPS TOPOLOGIES

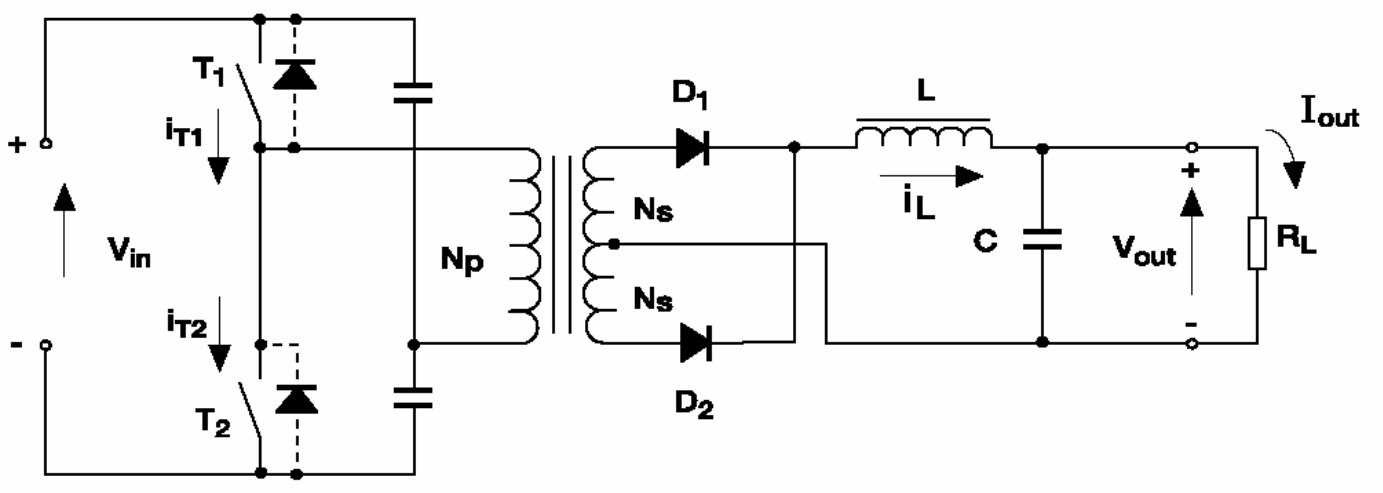
- The power switch carries output inductor current reflected to the primary which has a ramp on a step waveform
- The voltage stress of the power transistor which is off equals Vin

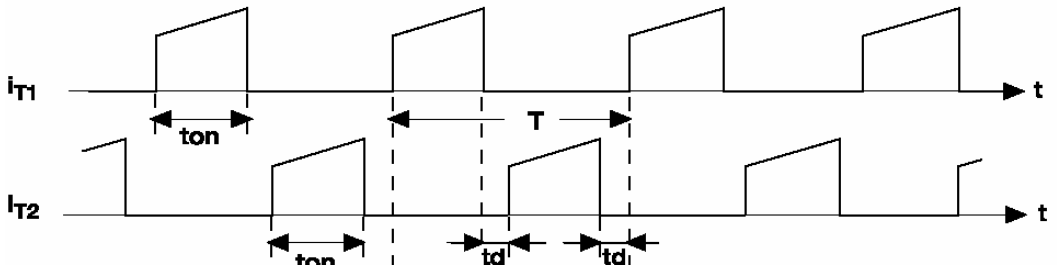
When the switches are off :

- The output inductor current freewheels through the rectifier diodes on the secondary side
- The voltage stress on the power switches equals Vin/2
- The output inductor current decreases linearly

II. SMPS TOPOLOGIES

Half Bridge Converter

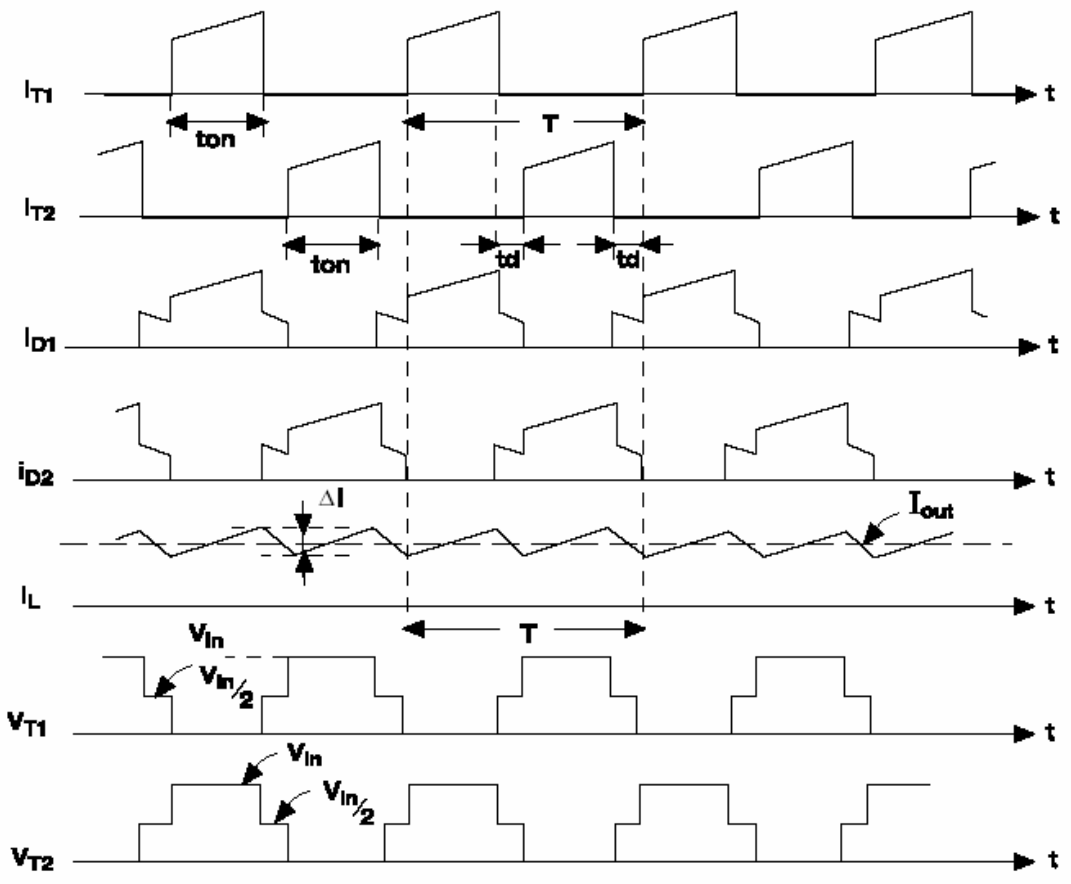




$$\delta = \frac{ton}{T}$$

η = EFFICIENCY

II. SMPS TOPOLOGIES

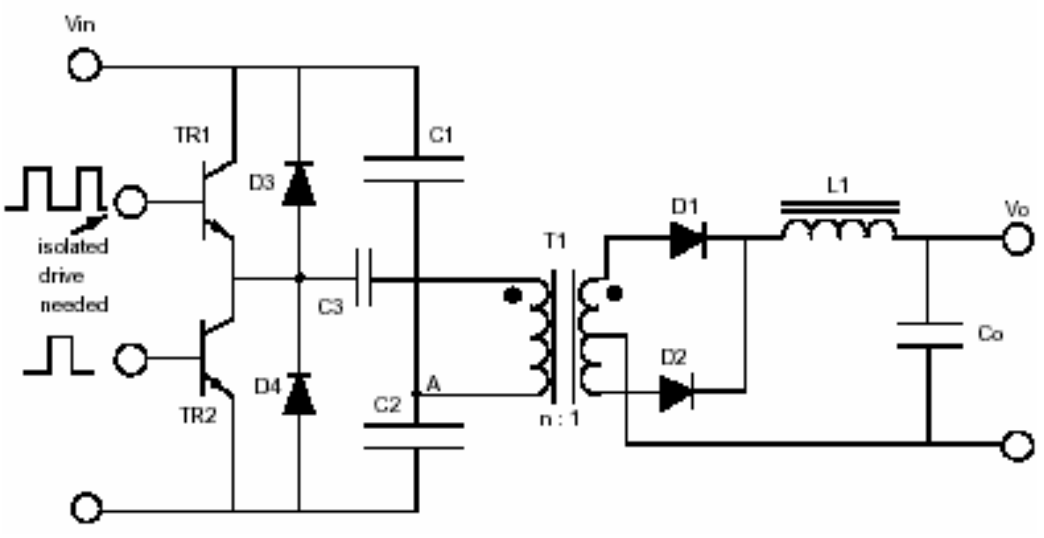


$$\delta = \frac{ton}{T}$$

η = EFFICIENCY

II. SMPS TOPOLOGIES

Half Bridge Converter (isolated drive required)



In push-pull: ***Switches were easy to drive since they are both referenced to ground.*** ***In half-bridge topology:*** ***an isolated high-side drive is required for the upper switch.***

II. SMPS TOPOLOGIES

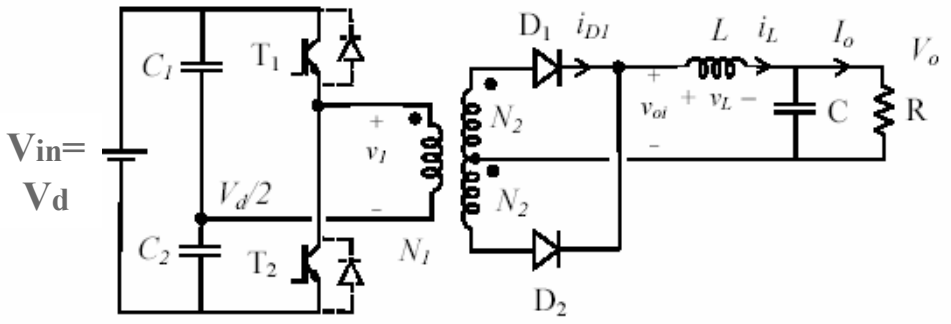
Half Bridge Converter Operation

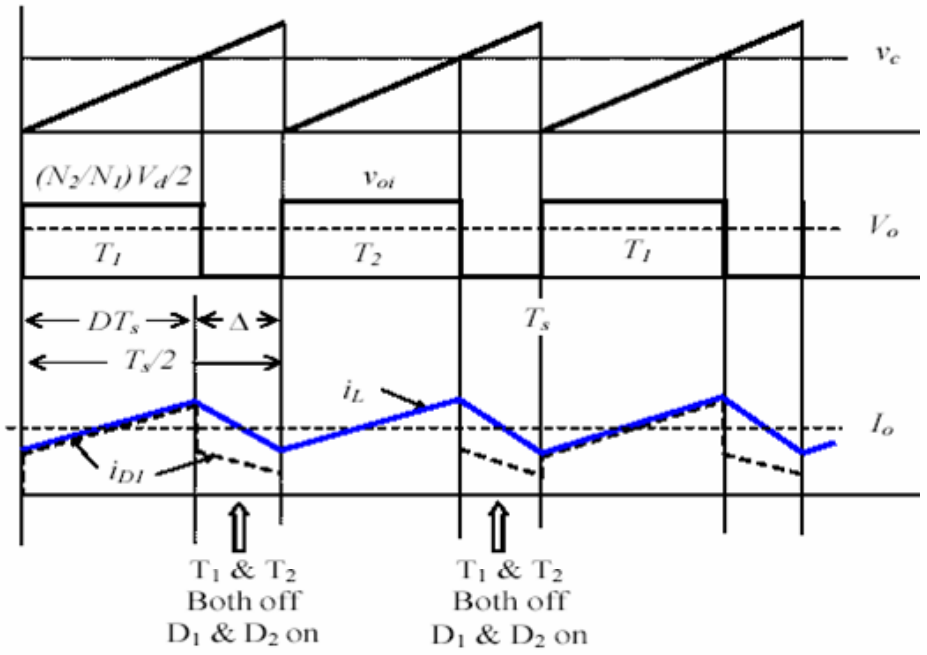
- *As for the push-pull converter, T1 and T2 switches are alternately turned-on during a time t_{on}. The capacitors in series across the supply fix a mid-point so that switches withstand only once the input voltage V_{in}.*

- *However, this topology requires driving a high-side switch. When using bipolar switches, transistor's storage time should have tight tolerances to avoid imbalance in operating flux level.*

- *The input – output relationship is:* $V_{out} = V_{in}\, D \,/\, n$

II. SMPS TOPOLOGIES





II. SMPS TOPOLOGIES

During t_{on},

$$v_L = \frac{N_2}{N_1}\frac{V_d}{2}$$

During $t_{on} < t < t_{on} + \Delta$,

$$v_L = -V_o$$

The waveforms repeat in $T_s/2$. By integrating v_L over $T_s/2$,

$$\frac{V_o}{V_d} = \frac{N_2}{N_1} D$$

where $D = t_{on}/T_s$

II. SMPS TOPOLOGIES

* *Power switch:*

$$I_{Cpeak} \text{ or } I_{Dpeak} \geq \frac{2P_{out}}{\eta V_{inmin}}$$

$$V_{CEV} \text{ or } V_{DSS} \geq V_{inmax}$$

* *Rectifier:*

$$V_{RRM} \geq \frac{(V_{out} + V_F) \cdot V_{inmax}}{\delta_{max} \cdot V_{inmin}} + \text{leakage inductance spike}$$

$$I_{F(av)} \geq \frac{I_{outmax}}{2}$$

Deadtimes (t_d in figure) between two consecutive switch conduction are absolutely mandatory to avoid bridge-leg short circuit.

Sometimes, power transformers are paralleled to provide higher output power.

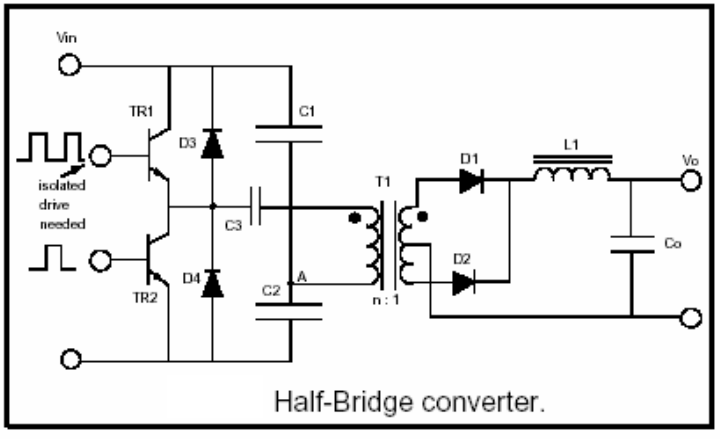
II. SMPS TOPOLOGIES

Half Bridge Converter

It is also referred to as the single ended push-pull, and in principle is a balanced version of the forward converter. Again it is a derivative of the buck. The Half-Bridge has some key advantages over the push-pull, which usually makes it first choice for higher power applications in the 500 to 1000W range.

Operation.

The two mains bulk capacitors C1 and C2 are connected in series, and an artificial input voltage mid-point is provided, shown as point A in the diagram. The two transistor switches are driven alternately, and this connects each capacitor across the single primary winding each half cycle. $V_{in}/2$ is superimposed symmetrically across the primary in a push-pull manner. Power is transferred directly to the output on each transistor conduction time and a maximum duty cycle of 90% is available (Some dead time is required to prevent transistor cross-conduction.) Since the primary is driven in both directions, (natural reset) a full wave buck output filter (operating at twice the switching frequency) rather than a half wave filter is implemented. This again results in very efficient core utilisation. As can be seen in Fig. , the waveforms are identical to the push-pull, except that the voltage across the transistors is halved. (The device current would be higher for the same output power.)



Half-Bridge converter.

Advantages.

Since both transistors are effectively in series, they never see greater than the supply voltage, V_{in}. When both are off, their voltages reach an equilibrium point of $V_{in}/2$. This is half the voltage rating of the push-pull (although double the current). This means that the half-bridge is particularly suited to high voltage inputs, such as off-line applications. For example, a 220V mains application can use two higher speed, higher efficiency 450V transistors instead of the 800V types needed for a push-pull. This allows higher frequency operation.

II. SMPS TOPOLOGIES

Advantages.

Another major advantage over the push-pull is that the transformer saturation problems due to flux symmetry imbalance are not a problem. By using a small capacitor (less than 10μF) any dc build-up of flux in the transformer is blocked, and only symmetrical ac is drawn from the input.

The configuration of the half-bridge allows clamp diodes to be added across the transistors, shown as D3 and D4 in Fig. The leakage inductance and magnetisation energies are dumped straight back into the two input capacitors, protecting the transistors from dangerous transients and improving overall efficiency.

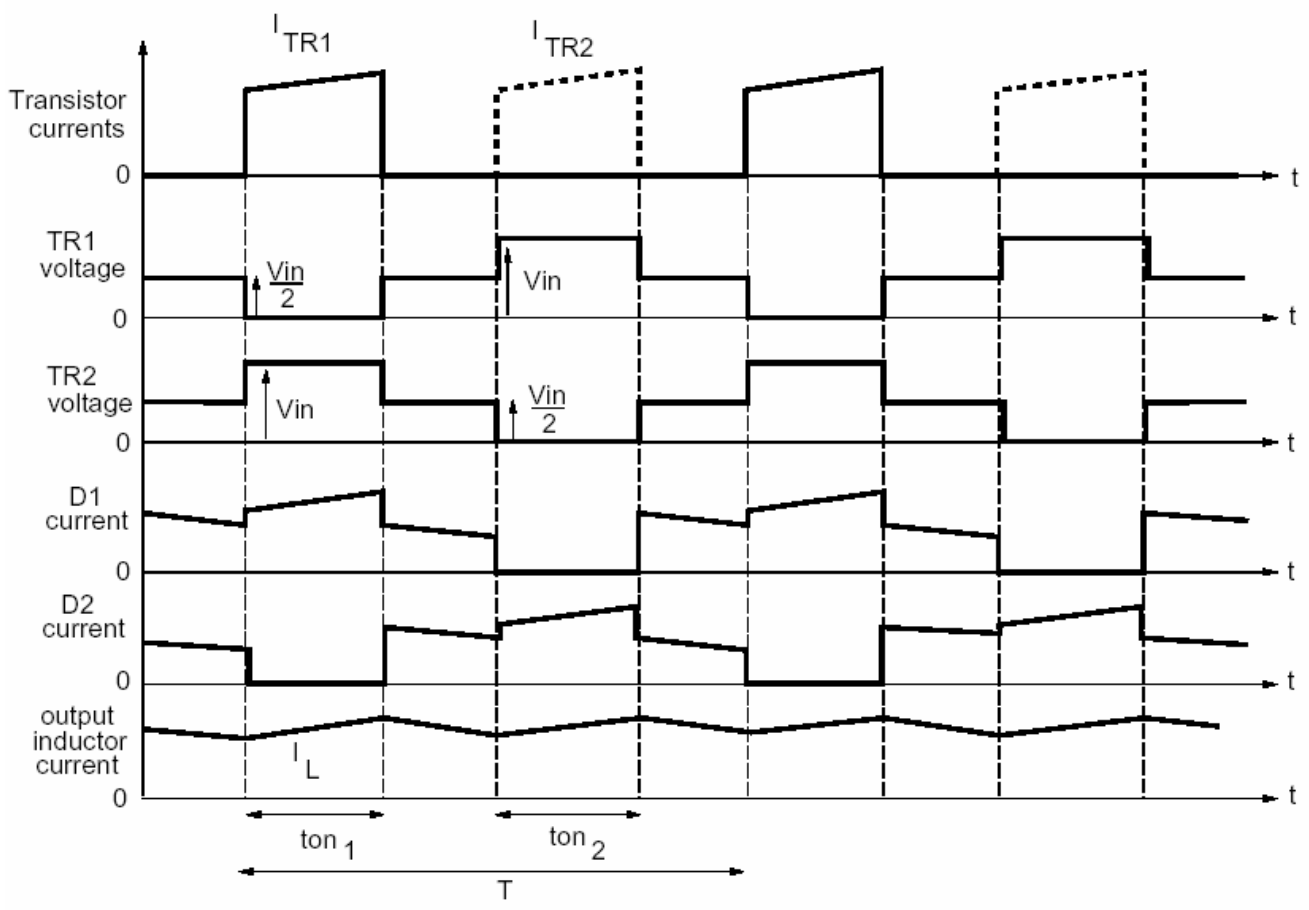
A less obvious exclusive advantage of the half-bridge is that the two series reservoir capacitors already exist, and this makes it ideal for implementing a voltage doubling circuit. This permits the use of either 110V /220V mains as selectable inputs to the supply.

The bridge circuits also have the same advantages over the single-ended types that the push-pull possesses, including excellent transformer utilisation, very low output ripple, and high output power capabilities. The limiting factor in the maximum output power available from the half-bridge is the peak current handling capabilities of present day transistors. 1000W is typically the upper power limit. For higher output powers the four switch full bridge is normally used.

Disadvantages.

The need for two 50/60 Hz input capacitors is a drawback because of their large size. The top transistor must also have isolated drive, since the gate / base is at a floating potential. Furthermore, if snubbers are used across the power transistors, great care must be taken in their design, since the symmetrical action means that they will interact with one another. The circuit cost and complexity have clearly increased, and this must be weighed up against the advantages gained. In many cases, this normally excludes the use of the half-bridge at output power levels below 500W.

II. SMPS TOPOLOGIES



Half Bridge converter waveforms

II. SMPS TOPOLOGIES

Half-bridge converter:

Max transistor voltage, V_{ce} or V_{ds} = $V_{in(max)}$ + leakage spike.

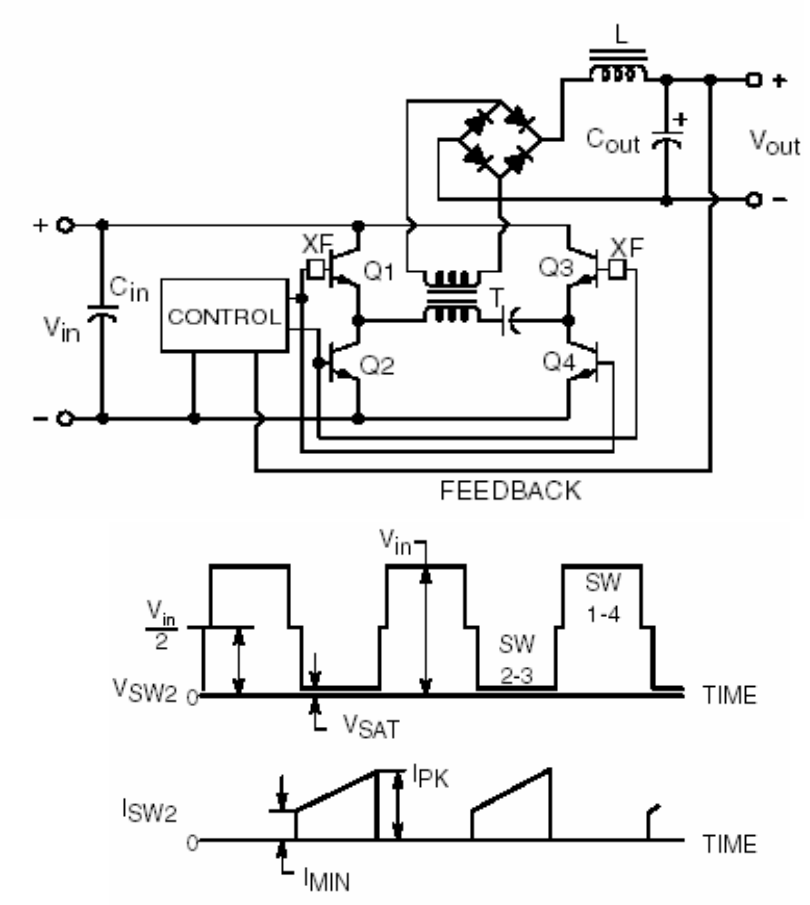
$$\text{Max } transistor\ current, I_C \quad ; \quad I_D = 2\frac{P_{out}}{\eta \quad D_{\max} \quad V_{\min}}$$

dc voltage gain:- $\frac{Vo}{Vin} = \quad D / n$

Applications:- High power, up to 1000W. High current, very low output ripple outputs. Well suited for high input voltage applications. E.g. 110, 220, 440V mains. E.g. Large computer supplies, Lab equipment supplies.

II. SMPS TOPOLOGIES

2.4.3. FULL BRIDGE CONVERTER



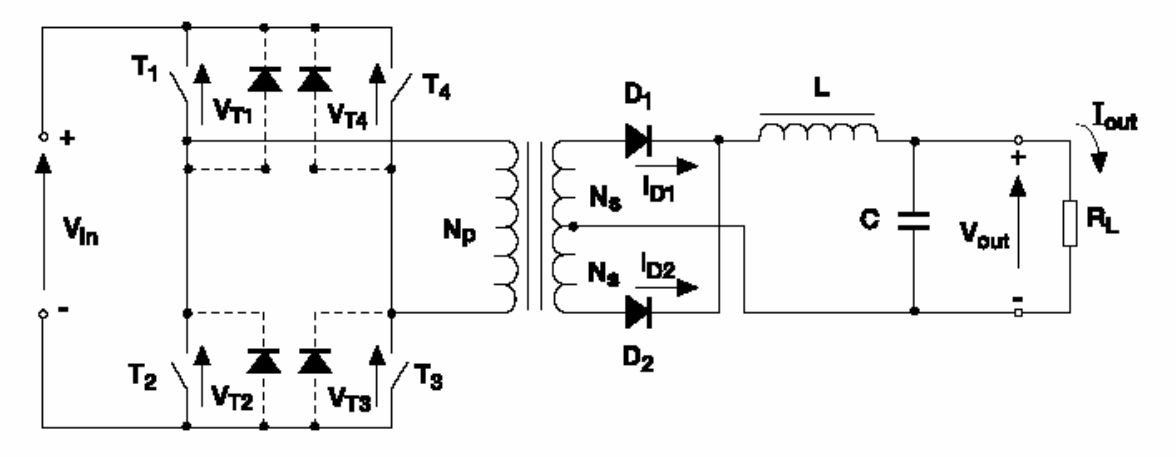
II. SMPS TOPOLOGIES

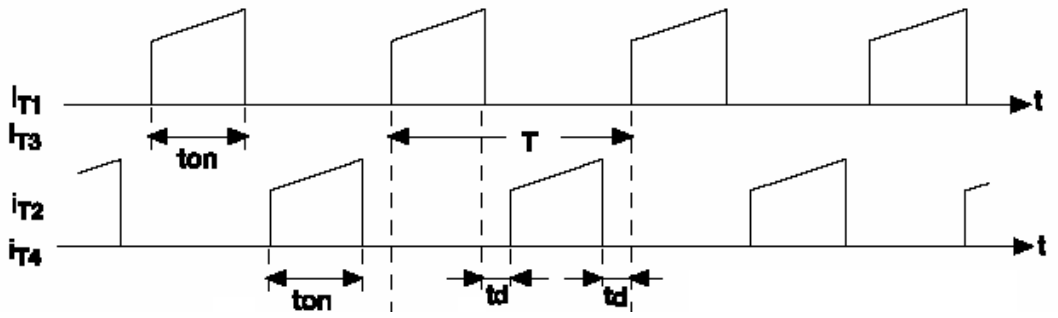
FULL BRIDGE CONVERTER

- The topology to consider above 500 W output is the full bridge converter
- It can deliver twice the output power of the half bridge converter with transistors of identical voltage and current ratings
- It uses 4 power transistors
- The voltage across the primary is a square wave of +/- Vin compared to +/- Vin/2 for the half bridge
- The voltage stress equals maximum DC input voltage (= Vin)

II. SMPS TOPOLOGIES

Full-bridge converter waveforms

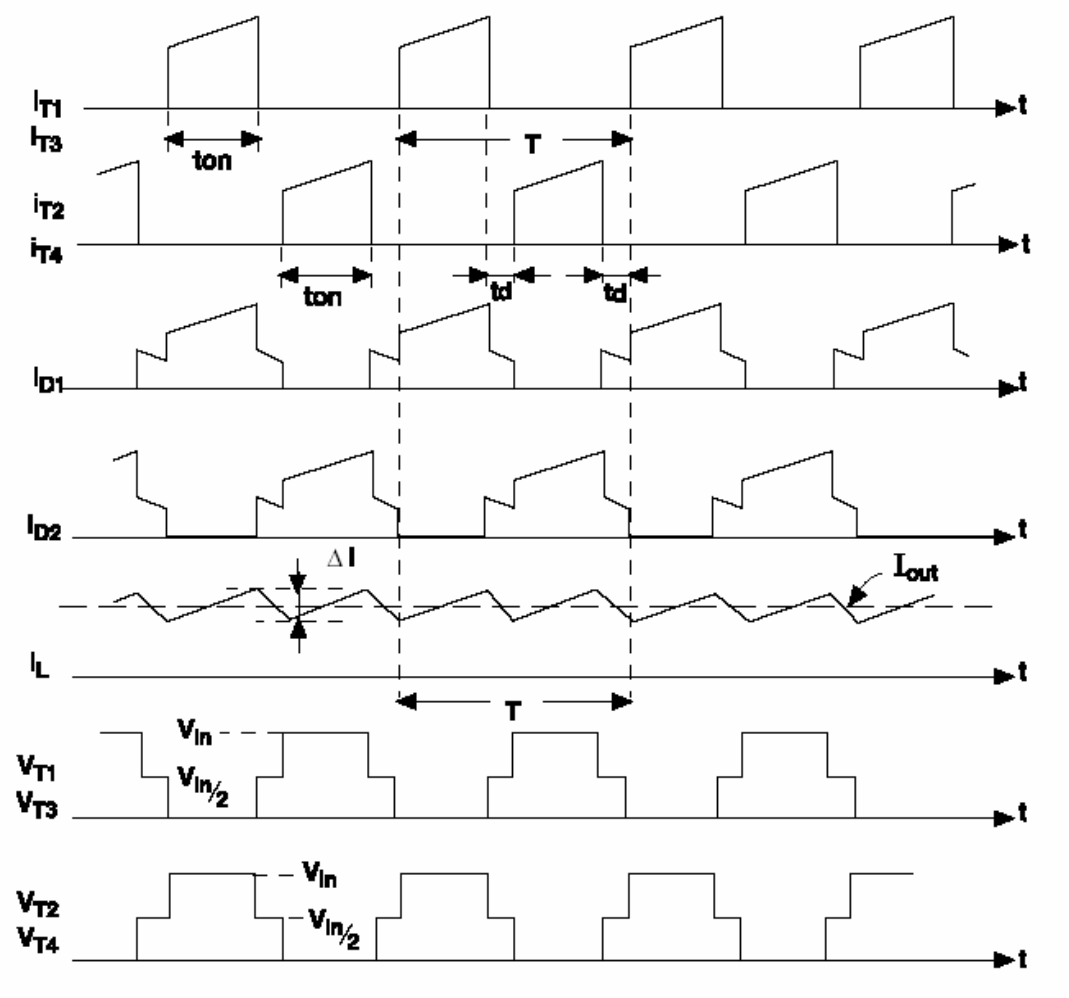




$$\delta = \frac{ton}{T}$$

η = EFFICIENCY

II. SMPS TOPOLOGIES



II. SMPS TOPOLOGIES

The full-bridge provides twice the output power of the half-bridge circuit withe the same switch ratings, but it requires 4 switches and clamping diodes.

** Power switch:*

$$I_{Cpeak} \text{ or } I_{Dpeak} \geq \frac{P_{out}}{\eta V_{inmin}}$$

$$V_{CEV} \text{ or } V_{DSS} \geq V_{inmax}$$

** Rectifier:*

$$V_{RRM} \geq \frac{(V_{out} + V_F)\ V_{inmax}}{\delta_{max}.V_{inmin}} + \text{leakage inductance spike}$$

$$I_F(av) \geq \frac{I_{outmax}}{2}$$

II. SMPS TOPOLOGIES

Outline.

The Full-Bridge converter shown in Fig. . . is a higher power version of the Half-Bridge, and provides the highest output power level of any of the converters discussed. The maximum current ratings of the power transistors will eventually determine the upper limit of the output power of the half-bridge. These levels can be doubled by using the Full-Bridge, which is obtained by adding another two transistors and clamp diodes to the Half-Bridge arrangement. The transistors are driven alternately in pairs, T1 and T3, then T2 and T4. The transformer primary is now subjected to the full input voltage. The current levels flowing are halved compared to the half-bridge for a given power level. Hence, the Full-Bridge will double the output power of the Half-Bridge using the same transistor types.

The secondary circuit operates in exactly the same manner as the push-pull and half-bridge, also producing very low ripple outputs at very high current levels. Therefore, the waveforms for the Full-Bridge are identical to the Half-Bridge waveforms shown in Fig. except for the voltage across the primary, which is effectively doubled (and switch currents halved). This is expressed in the dc gain and peak current equations, where the factor of two comes in, compared with the Half-Bridge.

Advantages.

As stated, the Full-Bridge is ideal for the generation of very high output power levels. The increased circuit complexity normally means that the Full-Bridge is reserved for applications with power output levels of 1kW and above. For such high power requirements, designers often select power Darlingtons, since their superior current ratings and switching characteristics provide additional performance and in many cases a more cost effective design.

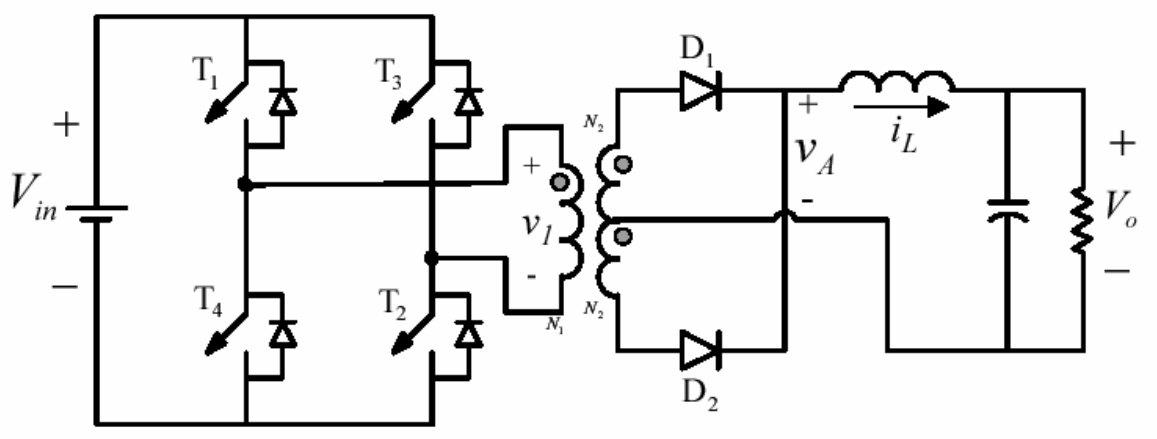
The Full-Bridge also has the advantage of only requiring one mains smoothing capacitor compared to two for the Half-Bridge, hence, saving space. Its other major advantages are the same as for the Half-Bridge.

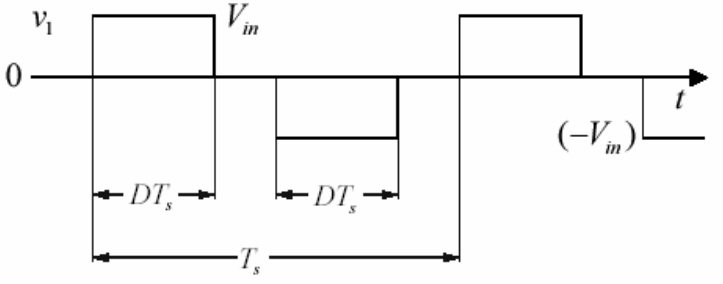
Disadvantages.

Four transistors and clamp diodes are needed instead of two for the other symmetrical types. Isolated drive for two floating potential transistors is now required. The Full-Bridge has the most complex and costly design of any of the converters discussed, and should only be used where other types do not meet the requirements. Again, the four transistor snubbers (if required) must be implemented carefully to prevent interactions occurring between them.

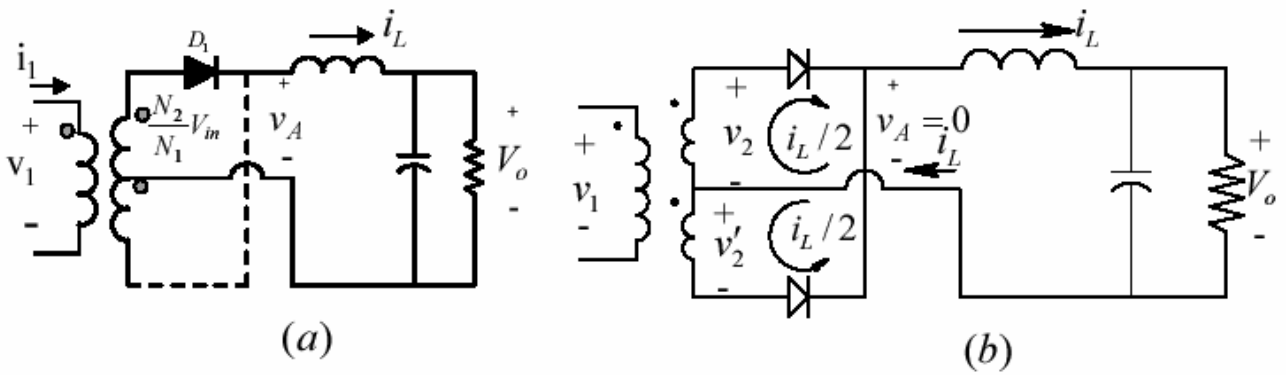
II. SMPS TOPOLOGIES

Full-bridge converter

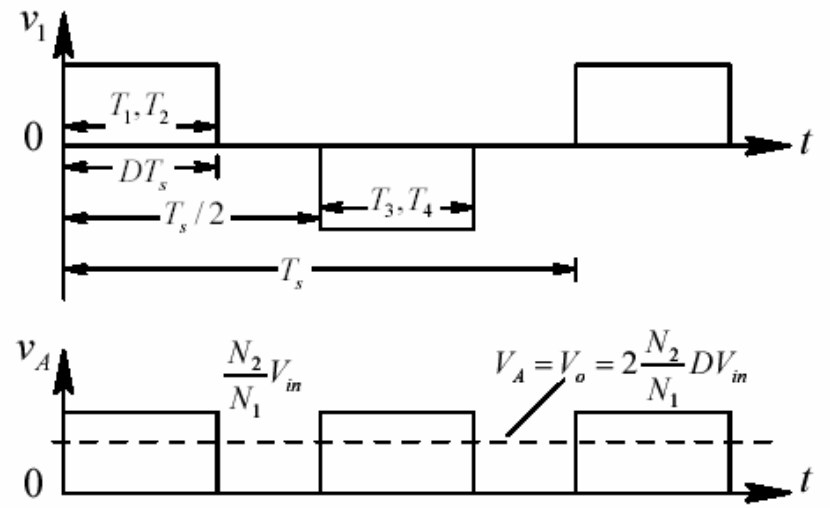




II. SMPS TOPOLOGIES



Full-Bridge: sub-circuits.



Input-output relationship:

$$\frac{V_o}{V_{in}} = 2\left(\frac{N_2}{N_1}\right)D$$

II. SMPS TOPOLOGIES

Full-bridge converter:

Max transistor voltage, V_{ce} or V_{ds} = $V_{in(max)}$ + leakage spike.

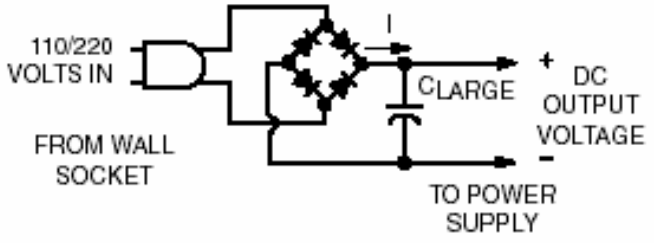
$$\text{Max } transistor current, I_C \quad ; \quad I_D = \frac{P_{out}}{\eta \quad D_{max} \quad V_{min}}$$

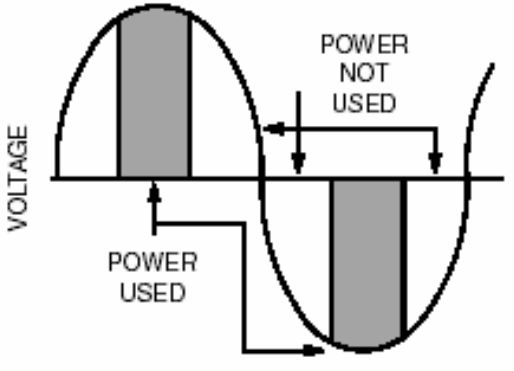
dc voltage gain: $\frac{Vo}{Vin} = 2D/n$

Applications:- Very high power, normally above 1000W. Very high current, very low ripple outputs. Well suited for high input voltage applications. E.g. 110, 220, 440V mains. E.g. Computer Mainframe supplies, Large lab equipment supplies, Telecomm systems.

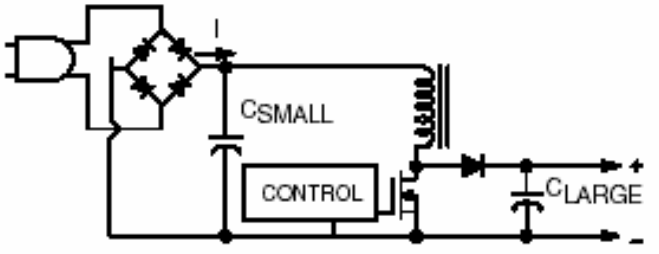
II. SMPS TOPOLOGIES

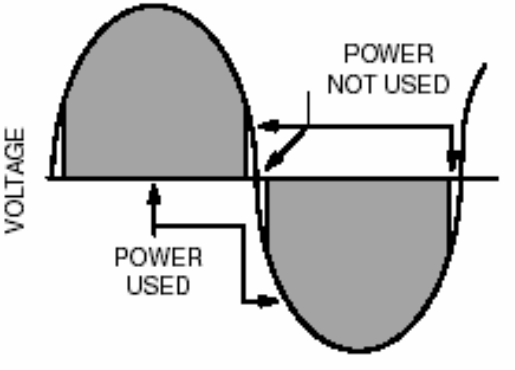
2.5. The Front End Rectifiers (Passive/Active)





Passive Front End Rectifier

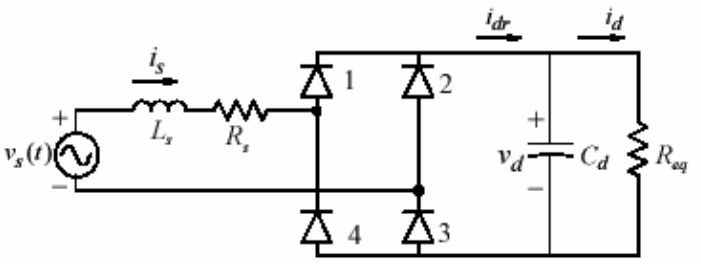


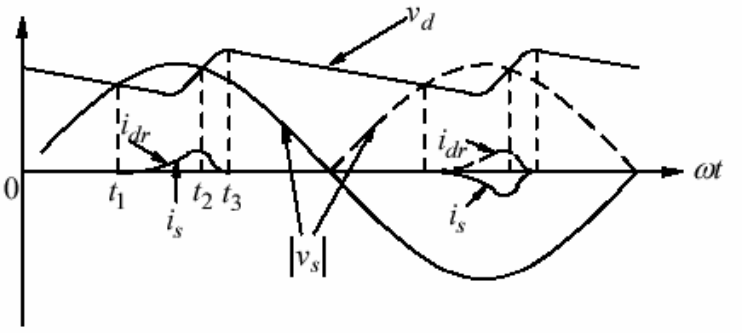


Active Front End Rectifier

II. SMPS TOPOLOGIES

The Passive Front End Rectifier
(Single-phase diode bridge rectifier)



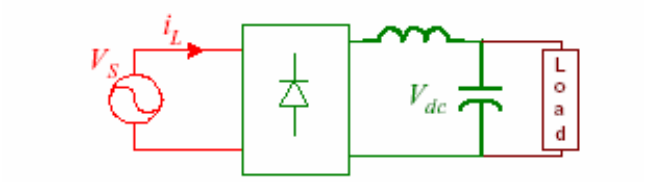


Total Harmonic Distortion: $\%THD = 100\ x\ \dfrac{I_{distortion}}{I_{s1}}$

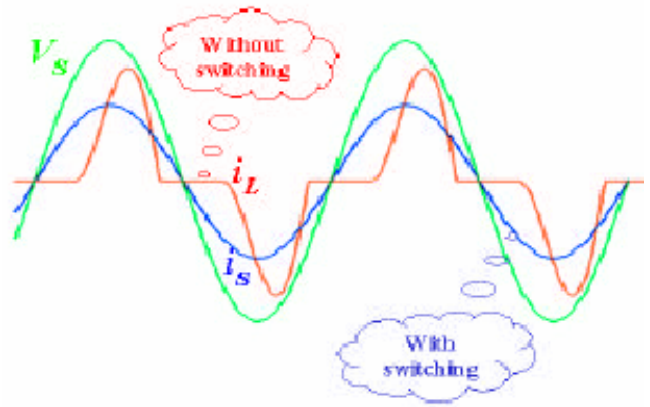
Displacement Power Factor: $DPF = \cos\ \phi_1$

$$PF = \frac{I_{s1}}{I_s}(DPF) = \frac{DPF}{\sqrt{1+THD^2}}$$ **(typically 0.5 – 0.6)**

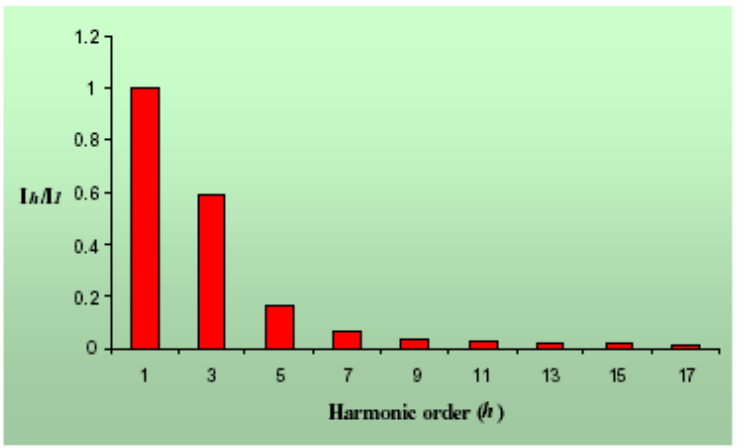
II. SMPS TOPOLOGIES



(a) Diode rectifier system



(b) Utility current and voltage



II. SMPS TOPOLOGIES

IEEE 519 Harmonic Guidelines

	Odd Harmonic Order h					Total Harmonic
I_{SC} / I_1	$h < 11$	$11 \le h \le 17$	$17 \le h \le 23$	$23 \le h \le 35$	$35 \le h$	Distortion(%)
< 20	4.0	2.0	1.5	0.6	0.3	5.0
$20 - 50$	7.0	3.5	2.5	1.0	0.5	8.0
$50 - 100$	10.0	4.5	4.0	1.5	0.7	12.0
$100 - 1000$	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0

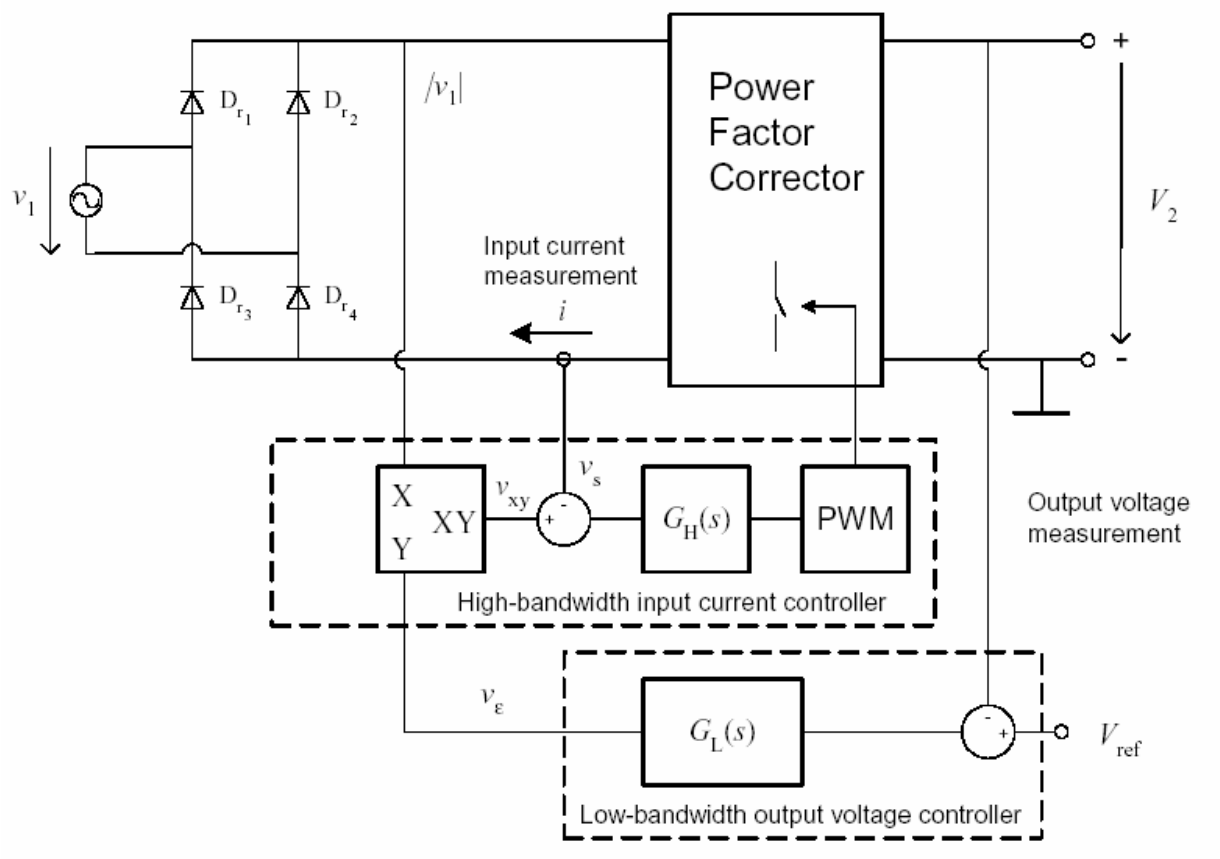
- IEEE – 519
- Limits on allowable harmonic currents drawn by loads of various relative magnitudes
- Relative magnitude of load currents is based on Short Circuit Ratio (SCR)

$$SCR = \frac{I_{sc}}{I_{s1}}$$

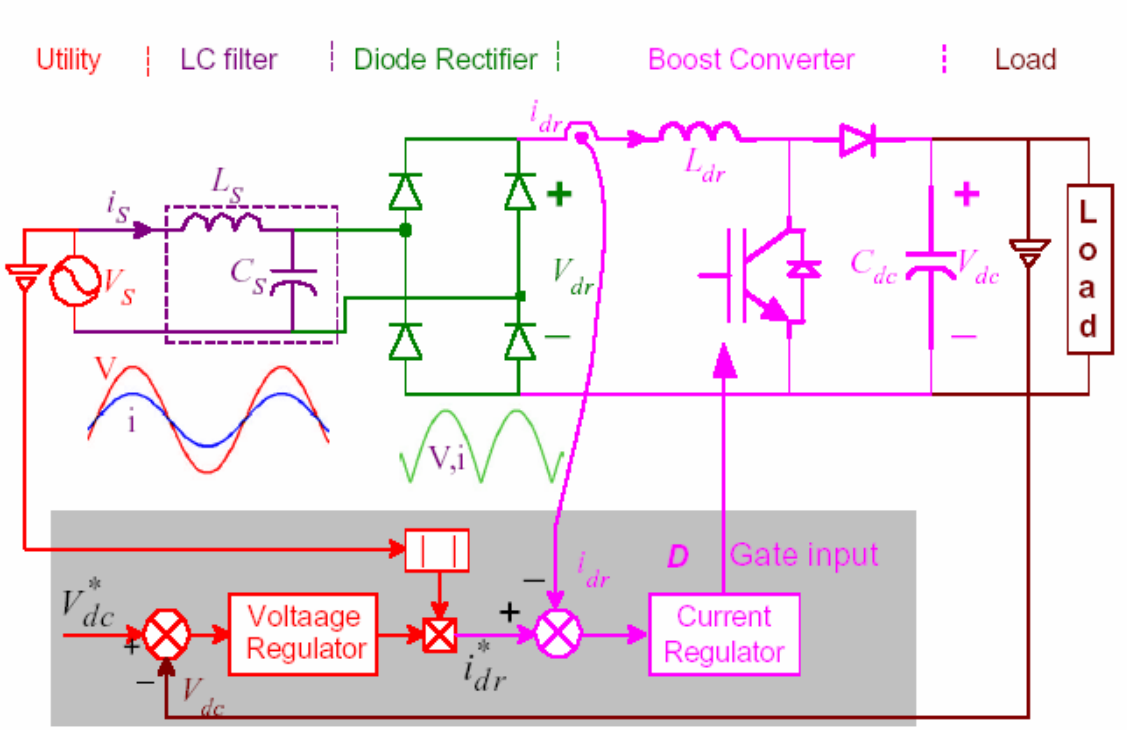
Where I_{sc} is the short circuit current and I_{s1} is the fundamental current of the load

II. SMPS TOPOLOGIES

The Active Front End Rectifier



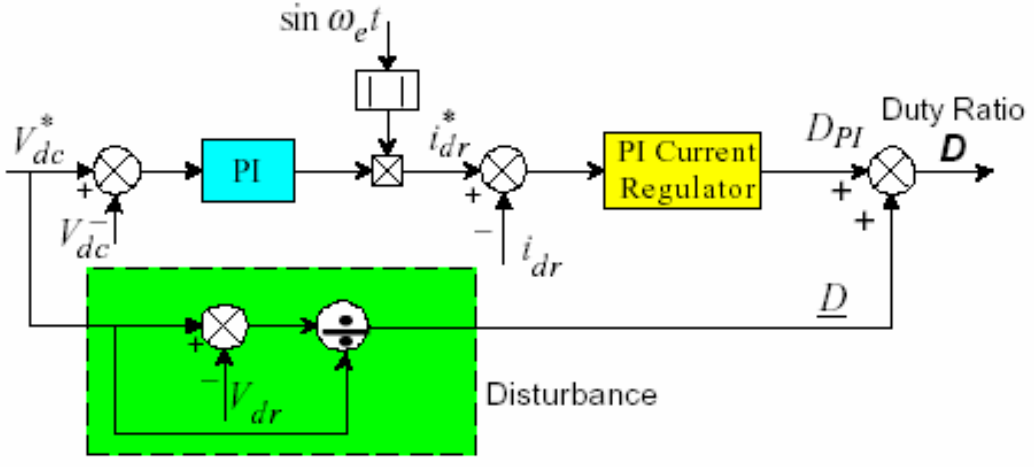
II. SMPS TOPOLOGIES



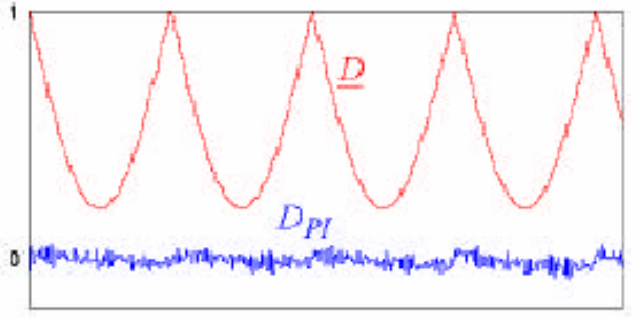
Analog IC : UC3854(TI/Unitrode), ML4812(Fairchild), L6561(STM)

Power factor corrected boost converter with analog control.

II. SMPS TOPOLOGIES

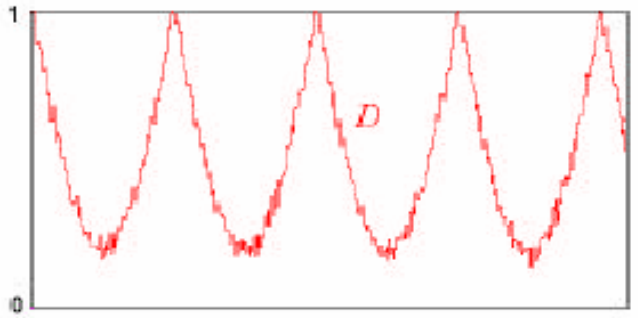


Control block diagram

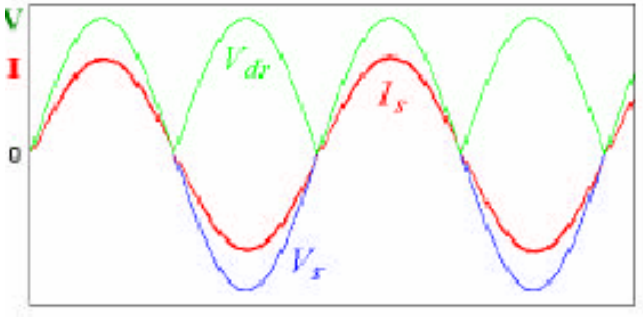


(a) $\underline{D}$ and D_{PI}

II. SMPS TOPOLOGIES

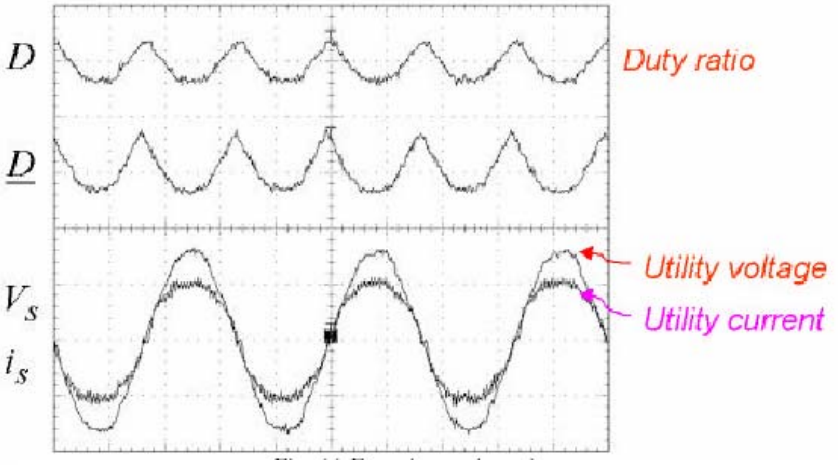


(b) Duty ratio D



(c) Utility voltage and current

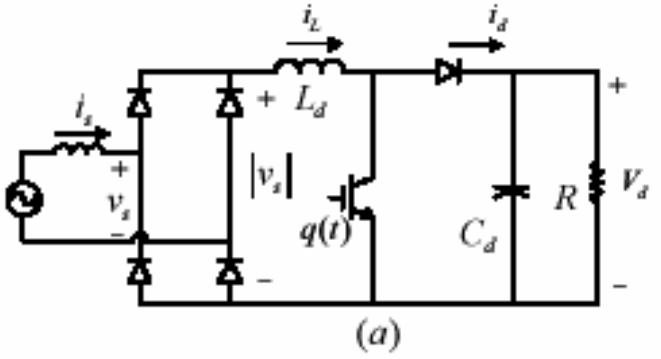
The waveforms of control system parameters.

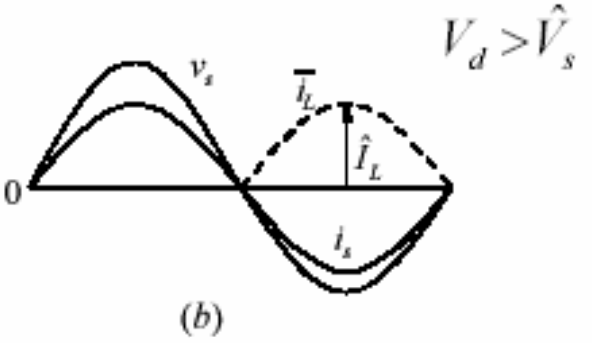


Experimental results

II. SMPS TOPOLOGIES

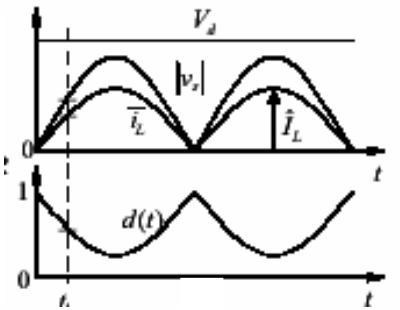
Power Factor Corrector
(continuous conduction mode)





$$d(t) = 1 - \frac{\hat{V}_s \left|\sin(\omega t)\right|}{V_o}$$

$$\frac{V_o}{|v_s|} = \frac{1}{1 - d(t)}$$



$$\bar{i}_d = \underbrace{\frac{1}{2}\frac{\hat{V}_s}{V_d}\hat{I}_L}_{I_d} - \underbrace{\frac{1}{2}\frac{\hat{V}_s}{V_d}\hat{I}_L \cos 2\omega t}_{i_{d2}(t)}$$

$$v_{d2} = -\frac{1}{\omega C}\frac{\hat{I}_L}{2}\frac{\hat{V}_s}{V_d}\int \cos 2\omega t \cdot d(\omega t) = -\underbrace{\left(\frac{\hat{I}_L \hat{V}_s}{4\omega C V_d}\right)}_{\hat{V}_{d2}} \sin 2\omega t$$

II. SMPS TOPOLOGIES

The Active Front End Rectifier Test Data

Power Factor Controller Test Data

AC Line Input									DC Output				
				Current Harmonic Distortion (% I_{fund})									
V_{rms}	P_{in}	PF	I_{fund}	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	η(%)
90	85.9	0.999	0.93	2.6	0.08	1.6	0.84	0.95	4.0	230.7	0.350	80.8	94.0
100	85.3	0.999	0.85	2.3	0.13	1.0	1.2	0.73	4.0	230.7	0.350	80.8	94.7
110	85.1	0.998	0.77	2.2	0.10	0.58	1.5	0.59	4.0	230.7	0.350	80.8	94.9
120	84.7	0.998	0.71	3.0	0.09	0.73	1.9	0.58	4.1	230.7	0.350	80.8	95.3
130	84.4	0.997	0.65	3.9	0.12	1.7	2.2	0.61	4.1	230.7	0.350	80.8	95.7
138	84.1	0.996	0.62	4.6	0.16	2.4	2.3	0.60	4.1	230.7	0.350	80.8	96.0

II. SMPS TOPOLOGIES

CONCLUSIONS

The five most common SMPS converter topologies, the flyback, forward, push-pull, half-bridge, and full-bridge types have been outlined. Each has its own particular operating characteristics and advantages, which makes it suited to particular applications.

The converter topology also defines the voltage and current requirements of the power transistors (either MOSFET or IGBT).

Simple calculations used to outline the requirements of the transistors for each topology have been presented.

II. SMPS TOPOLOGIES

Summary of key points

The steady-state behavior of transformer-isolated converters may be understood by first replacing the transformer with the magnetizing-inductance-plus-ideal-transformer equivalent circuit. The techniques developed in the previous chapters can then be applied, including use of inductor volt-second balance and capacitor charge balance to find dc currents and voltages, use of equivalent circuits to model losses and efficiency, and analysis of the discontinuous conduction mode.

In the full-bridge, half-bridge, and push-pull isolated versions of the buck and/or boost converters, the transformer frequency is twice the output ripple frequency. The transformer is reset while it transfers energy: the applied voltage polarity alternates on successive switching periods.

Summary of key points

In the conventional forward converter, the transformer is reset while the transistor is off. The transformer magnetizing inductance operates in the discontinuous conduction mode, and the maximum duty cycle is limited.

The flyback converter is based on the buck-boost converter. The flyback transformer is actually a two-winding inductor, which stores and transfers energy.

The transformer turns ratio is an extra degree-of-freedom which the designer can choose to optimize the converter design. Use of a computer spreadsheet is an effective way to determine how the choice of turns ratio affects the component voltage and current stresses.

Total active switch stress, and active switch utilization, are two simplified figures-of-merit which can be used to compare the various converter circuits.

II. SMPS TOPOLOGIES

2.6. Example

Specifications	
Maximum input voltage V_g	390 V
Minimum input voltage V_g	260 V
Output voltage V	15 V
Maximum load power P_{load}	200 W
Minimum load power P_{load}	20 W
Switching frequency f_s	100 kHz
Maximum output ripple Δv	0.1 V

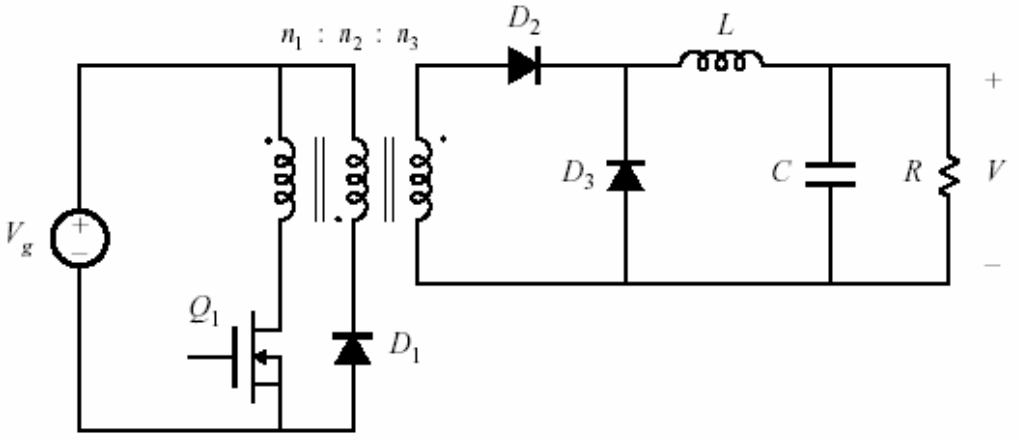
- Input voltage: rectified 230 Vrms ±20%
- Regulated output of 15 V
- Rated load power 200 W
- Must operate at 10% load
- Select switching frequency of 100 kHz
- Output voltage ripple ≤ 0.1V

Compare single-transistor forward and flyback converters in this application

Specifications are entered at top of spreadsheet

II. SMPS TOPOLOGIES

Forward converter design, CCM



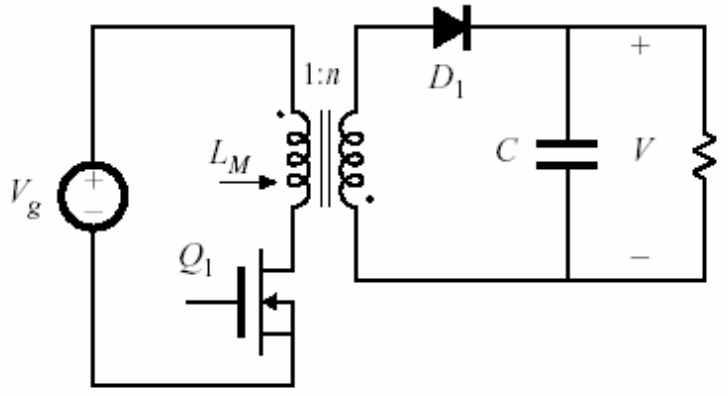
Design variables

Reset winding turns ratio n_2 / n_1	1
Turns ratio n_3 / n_1	0.125
Inductor current ripple Δi	2A ref to sec

- Design for CCM at full load; may operate in DCM at light load

II. SMPS TOPOLOGIES

Flyback converter design, CCM



Design variables

Turns ratio n_2/n_1	0.125
Inductor current ripple Δi	3 A ref to sec

- Design for CCM at full load; may operate in DCM at light load

II. SMPS TOPOLOGIES

Enter results of converter analysis into spreadsheet (Forward converter example)

Maximum duty cycle occurs at minimum V_g and maximum P_{load}. Converter then operates in CCM, with

$$D = \frac{n_1}{n_3}\frac{V}{V_g}$$

Inductor current ripple is

$$\Delta i = \frac{D'VT_s}{2L}$$

Solve for L:

$$L = \frac{D'VT_s}{2\Delta i}$$

Δi is a design variable. For a given Δi, the equation above can be used to determine L. To ensure CCM operation at full load, Δi should be less than the full-load output current. C can be found in a similar manner.

II. SMPS TOPOLOGIES

Forward converter example, continued

Check for DCM at light load. The solution of the buck converter operating in DCM is

$$V = \frac{n_3}{n_1} V_g \frac{2}{\sqrt{1 + \frac{4K}{D^2}}}$$

with $K = 2L / R T_s$, and $R = V^2 / P_{load}$

These equations apply equally well to the forward converter, provided that all quantities are referred to the transformer secondary side.

Solve for D:

$$D = \frac{2\sqrt{K}}{\sqrt{\left(\frac{2n_3 V_g}{n_1 V} - 1\right)^2 - 1}} \quad \textit{in DCM} \qquad D = \frac{n_1}{n_3}\frac{V}{V_g} \quad \textit{in CCM}$$

at a given operating point, the actual duty cycle is the small of the values calculated by the CCM and DCM equations above. Minimum D occurs at minimum P_{load} and maximum V_g.

II. SMPS TOPOLOGIES

More regarding forward converter example

Worst-case component stresses can now be evaluated.

Peak transistor voltage is

$$\max\left(v_{Q1}\right) = V_g\left(1 + \frac{n_1}{n_2}\right)$$

RMS transistor current is

$$I_{Q1,rms} = \frac{n_3}{n_1}\sqrt{D}\sqrt{I^2 + \frac{\left(\Delta i\right)^2}{3}} \approx \frac{n_3}{n_1}\sqrt{D}\,I$$

(this neglects transformer magnetizing current)

Other component stresses can be found in a similar manner.

II. SMPS TOPOLOGIES

Forward converter design, CCM		***Flyback converter design, CCM***	
Design variables		*Design variables*	
Reset winding turns ratio n_2/n_1	1	Turns ratio n_2/n_1	0.125
Turns ratio n_3/n_1	0.125	Inductor current ripple Δi	3 A ref to sec
Inductor current ripple Δi	2 A ref to sec		
Results		*Results*	
Maximum duty cycle D	0.462	Maximum duty cycle D	0.316
Minimum D, at full load	0.308	Minimum D, at full load	0.235
Minimum D, at minimum load	0.251	Minimum D, at minimum load	0.179
Worst-case stresses		*Worst-case stresses*	
Peak transistor voltage v_{Q1}	780 V	Peak transistor voltage v_{Q1}	510 V
Rms transistor current i_{Q1}	1.13 A	Rms transistor current i_{Q1}	1.38 A
Transistor utilization U	0.226	Transistor utilization U	0.284
Peak diode voltage v_{D2}	49 V	Peak diode voltage v_{D1}	64 V
Rms diode current i_{D2}	9.1 A	Rms diode current i_{D1}	16.3 A
Peak diode voltage v_{D3}	49 V	Peak diode current i_{D1}	22.2 A
Rms diode current i_{D3}	11.1 A		
Rms output capacitor current i_C	1.15 A	Rms output capacitor current i_C	9.1 A

II. SMPS TOPOLOGIES

Discussion: transistor voltage

Flyback converter

- Ideal peak transistor voltage: 510V
- Actual peak voltage will be higher, due to ringing causes by transformer leakage inductance
- An 800V or 1000V MOSFET would have an adequate design margin

Forward converter

- Ideal peak transistor voltage: 780V, 53% greater than flyback
- Few MOSFETs having voltage rating of over 1000 V are available —when ringing due to transformer leakage inductance is accounted for, this design will have an inadequate design margin
- Fix: use two-transistor forward converter, or change reset winding turns ratio

A conclusion: reset mechanism of flyback is superior to forward

II. SMPS TOPOLOGIES

Discussion: rms transistor current

Forward

1.13A worst-case

transistor utilization 0.226

Flyback

1.38A worst case, 22% higher than forward

transistor utilization 0.284

CCM flyback exhibits higher peak and rms currents. Currents in DCM flyback are even higher

II. SMPS TOPOLOGIES

Discussion: secondary-side diode and capacitor stresses

Forward

peak diode voltage 49V

rms diode current 9.1A / 11.1A

rms capacitor current 1.15A

Flyback

peak diode voltage 64V

rms diode current 16.3A

peak diode current 22.2A

rms capacitor current 9.1A

Secondary-side currents, especially capacitor currents, limit the practical application of the flyback converter to situations where the load current is not too great.