Hacettepe University
Electrical and Electronics Engineering Department

ELE 789
Special Topics in Electrical and Electronics Engineering

Lecture Notes
Chapter VI

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VI. MULTIPLE OUTPUT SMPS

MULTIPLE OUTPUT SMPS

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Cross Regulation is how the outputs of a multiple output SMPS respond to a change in the load on any one output.

Tight output regulation is more difficult in multiple output power supplies. The following are the most popular techniques.

1. The Linear Regulator, Figure 1, is the simplest and the most popular for low current (3.0 A) applications. The major disadvantage of the linear regulator is its poor efficiency.
2. A Step–Down Buck Regulator, Figure 2, can be used as a post regulator. Efficiencies up to 90% can be achieved by using this method. This solution looks very attractive in the low and medium power range (3.0 A to 8.0 A). However, several additional high cost components are required, including, a power switch, inductor and capacitors.

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3.A Magnetic Amplifier Post Regulator, Figure 3, offers high efficiency and tight regulation for output currents greater than 5.0 A .

Its drawbacks include: the difficulty in implementing overcurrent protection, poor regulation characteristics at light or no load conditions and the cost of the high frequency (200 kHz) magnetic amplifier inductor.

4.A Secondary Side Post Regulator (SSPR), Figure 4, uses a semiconductor switch with either leading edge (delayed turn–on) or trailing edge (delayed turn–off) modulation.

An SSPR provides excellent regulation, high efficiency, high frequency operation, lossless overcurrent protection and remote ON/OFF control.

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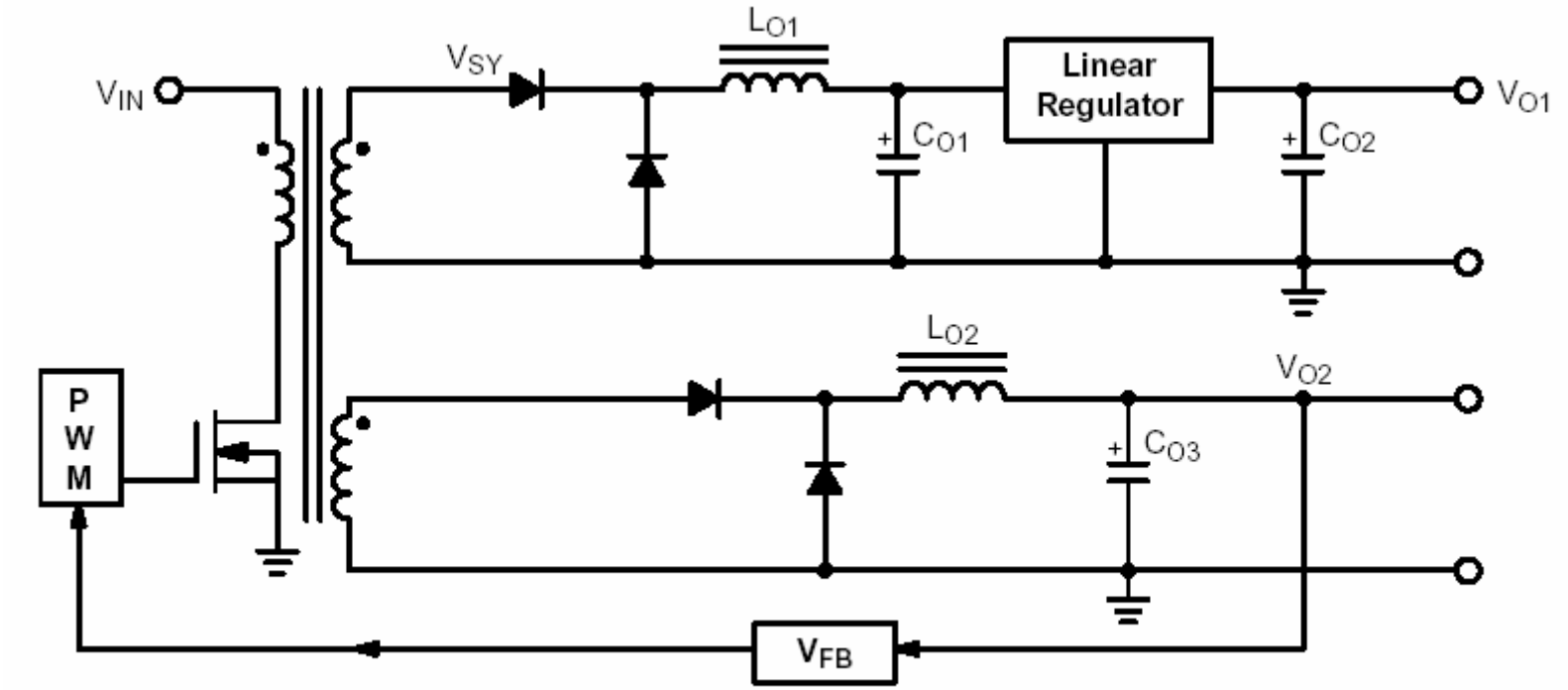

Figure 1. Linear Regulator

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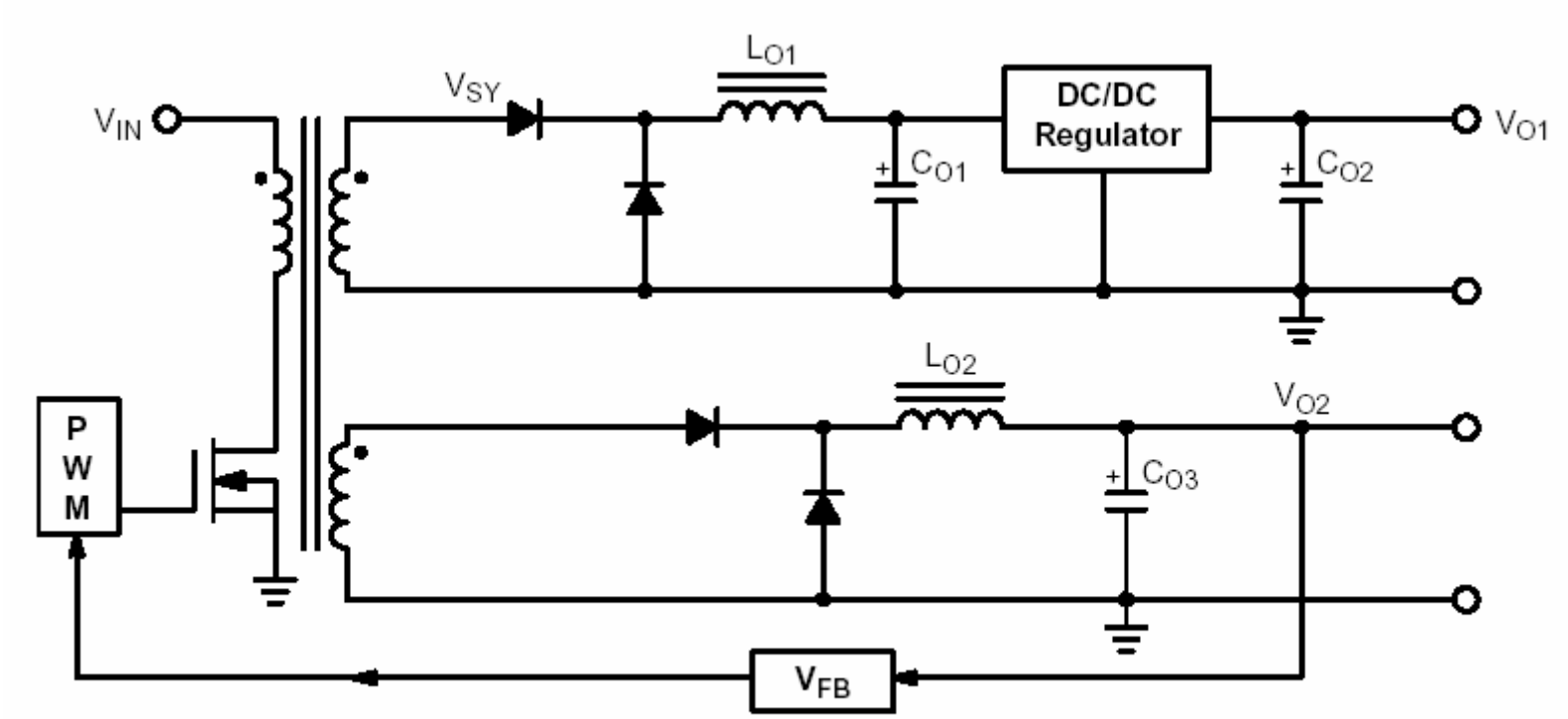

Figure 2. Switching Post Regulator

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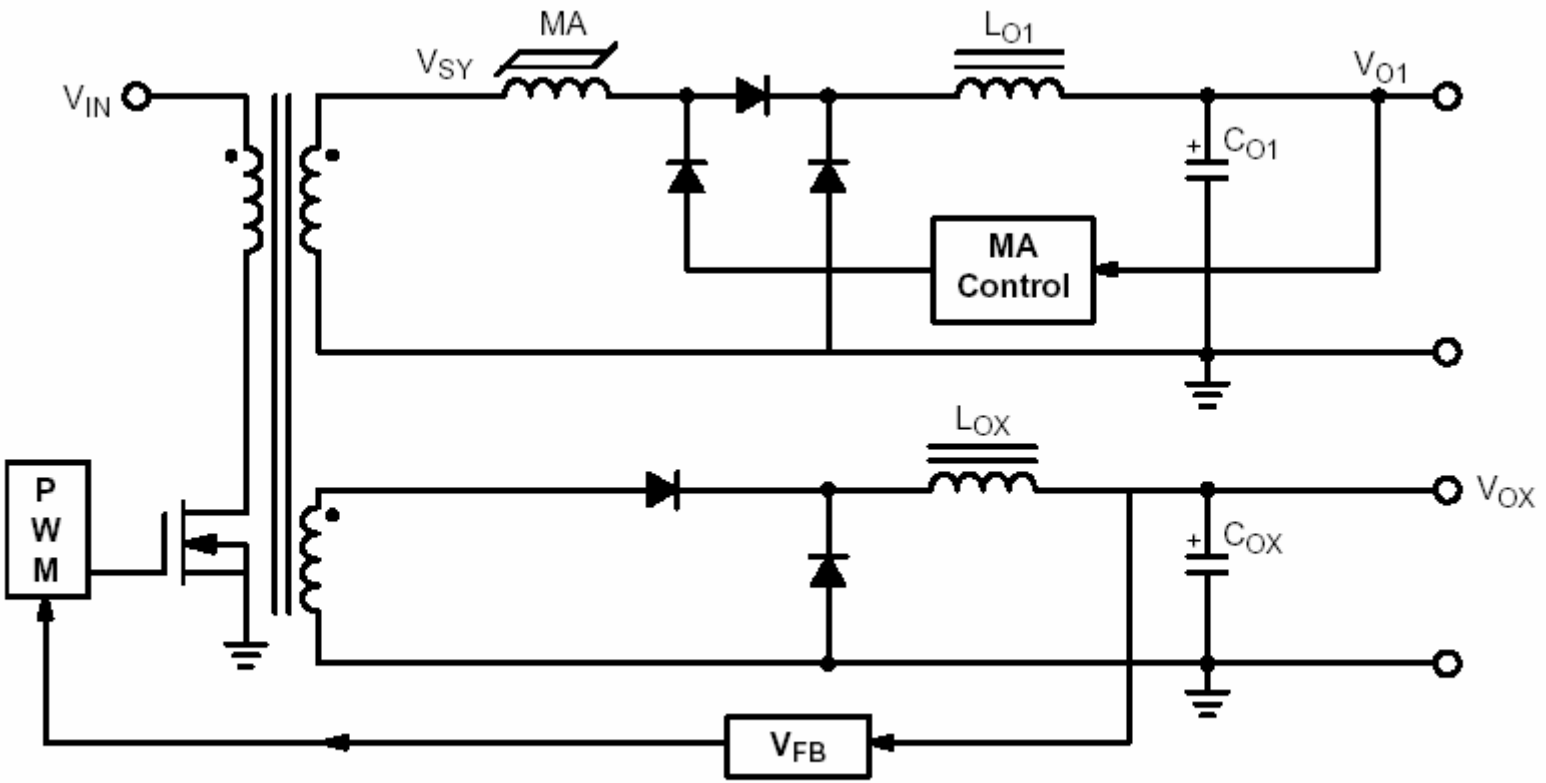

Figure 3. MAGAMP

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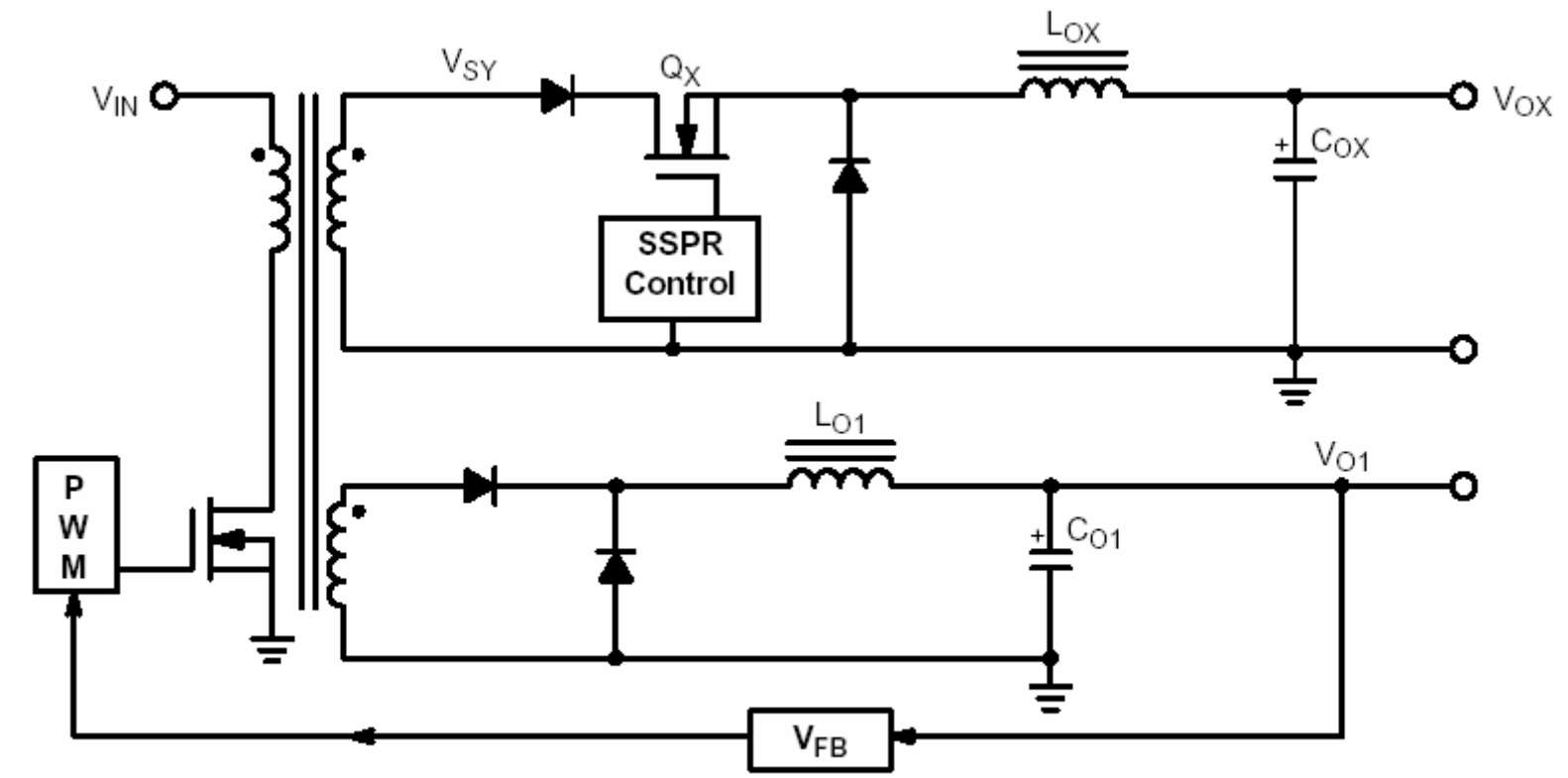

Figure 4. SSPR

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SSPR Operation

An SSPR regulator allows the designer to build multiple output power supplies with each output individually controlled without any feedback to the primary side.

The SSPR switch is connected in series with the secondary side rectifier and output inductor.

In a forward converter topology using current mode control, the primary controller maintains a constant volt–second product. The primary side current waveforms for both leading edge and trailing edge operation are shown in Figure 5. There is a step change in the primary current when the SSPR turns on, or turns off. Trailing edge modulation will cause loop instability in current mode control using peak current sensing. This is not a problem with voltage mode control regulators. Leading edge modulation does not have this limitation.

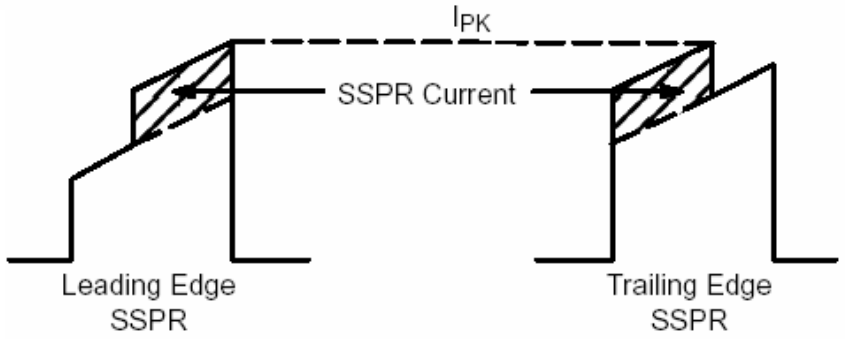

Figure 5. Primary Switch Current Waveforms

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Connecting the SSPR in a Circuit

The SSPR can be used in a variety of topologies including both single and dual ended buck or flyback converters operating with current or voltage mode control.

In each case, usually the N–FET power switch is connected in series with the forward diode as shown in Figure 7.

Since the N–FET is connected between two diodes it is impossible to use a single package center–tap rectifier. The source voltage of the N–FET changes from the secondary side peak voltage to approximately –0.7 V (the flyback diode forward drop) so the user must create a floating gate drive.

If it is not necessary to have a common ground connection between all outputs on the secondary side, the inductor can be connected on the ground side

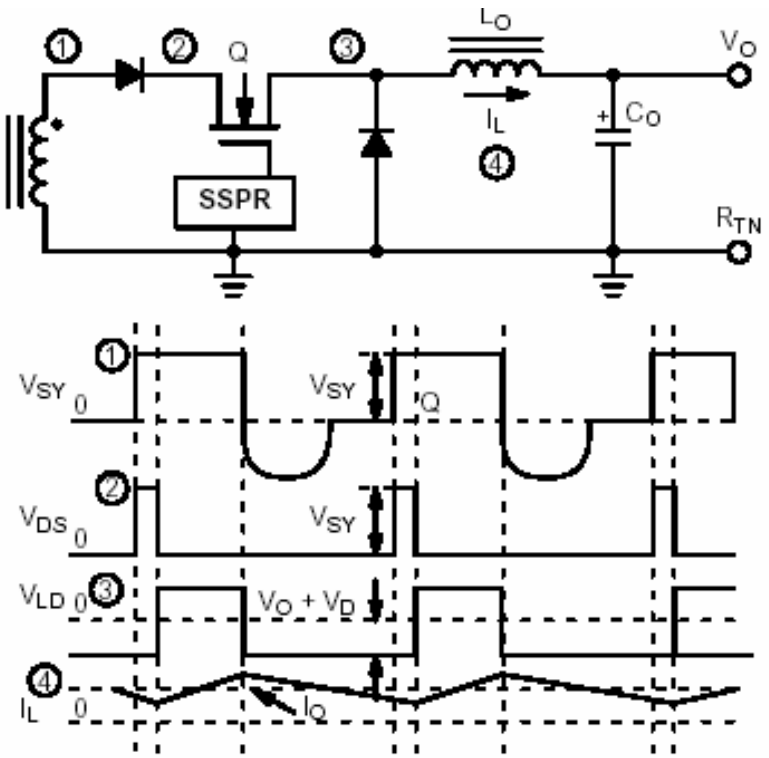

Figure 7. Primary Switch Current Waveforms

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There are two ways to generate a negative output voltage. One way is simply to reverse the ground and output connections as is shown in Figure 9. The SSPR circuit is referenced to the negative output.

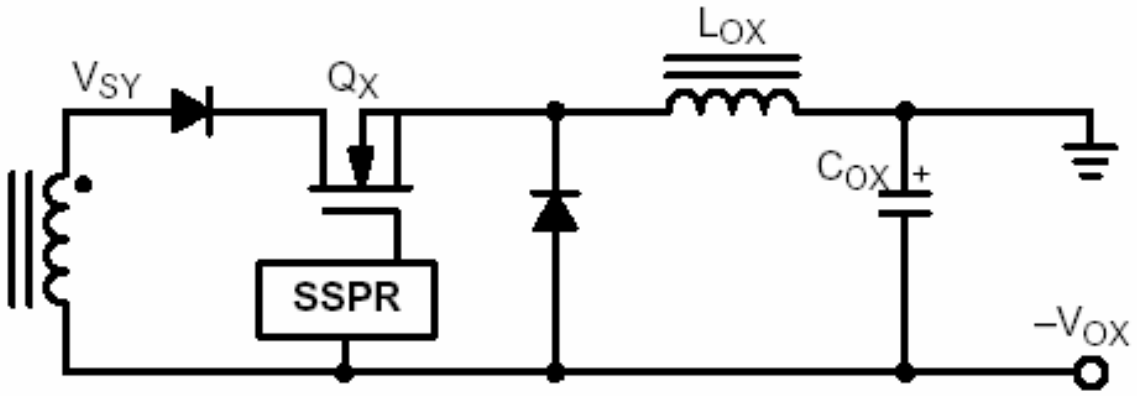

Figure 9. SSPR for Negative Output

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Another method is shown in Figure 10. The SSPR gate drive circuit is referenced to ground. An additional feedback signal inversion is required in this case.

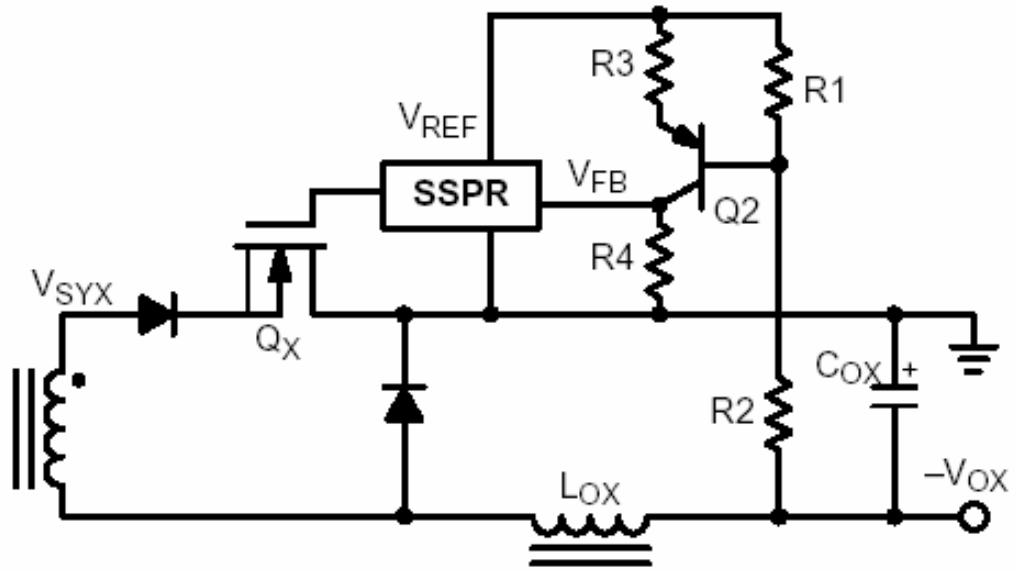

Figure 10. Ground Referenced Negative Output SSPR

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Design Example

As an example, we show the design of a dual output current mode control forward converter. The 5.0 V output is controlled by the main loop with feedback connected to the primary side PWM controller (CS3842A). The second 3.3 V output is controlled by the CS5101.

Design Specifications

Input Voltage Range	18 to 36 V_{DC}
Output Voltage, VO1	5.0 V_{DC}
Output Voltage, VO2	3.3 V_{DC}
Output Current, IO1	0.2 to 3.0 A_{DC}
Output Current, IO2	0.3 to 2.0 A_{DC}
Switching Frequency	100 kHz
Line/Load Regulation at all outputs	1.0%

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1. Power Transformer Design

To leave enough head room for SSPR operation at high line, assume the duty cycle at low line, D_{LL} is 0.6.

Voltage at the 5.0 V winding:

$$V_{SY5} = \frac{5.0 + 0.6}{0.6} = 9.33 \text{ V}$$

Transformer turns ratio:

$$n = \frac{V_{SY}}{V_{PY}} = \frac{9.33}{18} = 0.518$$

Use TDK core PC40EER25.5 – Z.

Minimum number of primary turns:

$$N_{PY} = \frac{V_{IN(MIN)} \times t_{ON}}{B_m \times A_e} 10^8$$

where:

B_m = Flux Density, in Gauss;

A_e = Effective core cross section area, in cm^2;

t_{ON} = Power switch on–time at low line;

$V_{IN(MIN)}$ = Minimum input voltage.

Rewriting this equation, in terms of duty cycle, D, and switching frequency, f_{SW},:

$$N_{PY} = \frac{V_{IN(MIN)} \times D_{MAX}}{f_{SW} \times B_m \times A_e} 10^8$$

$$N_{PY} = \frac{18 \times 0.6}{100 \text{ k} \times 1.2 \text{ k} \times 0.448} 10^8 = 20 \text{ turns}$$

Secondary turns for 5.0 V output:

$$N_{SY5} = 20 \times n = 20 \times 0.518 = 10.36 \text{ turns}$$

N_{SY5} = 11 T.

Use the same number of turns for both the 3.3 V and 5.0 V outputs. The turns ratio of the power transformer N_{PY}:N_{SY5}:N_{SY3}:N_{AUX} is equal to 20:11:11:8.

The transformer is reset with the clamp reset circuit comprising D8, R10, C18. At turn–off, the drain voltage of Q2 is clamped to a voltage equal to the input voltage plus the voltage across capacitor C18.

Actual duty cycle at low line:

$$D_{LL} = \frac{V_O + V_D}{V_{IN(MIN)} \times n}$$

$$D_{LL} = \frac{(5.0 + 0.8) \times 20}{18 \times 11} = 0.586$$

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Duty cycle at high line:

$$D_{HL} = D_{LL} \times \frac{V_{IN(MIN)}}{V_{IN(MAX)}}$$

$$D_{HL} = 0.586 \times \frac{18}{36} = 0.293$$

Output Inductor Design

We must maintain continuous mode operation at minimum load and maximum input voltage conditions.

5.0 V Output Inductor, L1

$I_{O5(MIN)} = 0.25$ A; $D_{MIN} = 0.293$; $f_{SW} = 100$ kHz;
$\Delta I = 2.0 \times I_{O(MIN)} = 0.5$ A.
Rectifier diode forward drop $V_D = 0.75$ @ 3.0 A. (MBR360)
The output inductor is calculated with the following equation:

$$L_{MIN} = \frac{(V_O + V_D) \times t_{OFF(MAX)}}{\Delta I}$$

$$L_{MIN} = \frac{(5.0 + 0.75) \times (1.0 - 0.293)}{100\ k \times 0.5} = 81\ \mu H$$

Allowing for a 20% tolerance in the inductor, L1 = 100 µH.
Use a T72–26 Powdered Iron Core from Micrometals.
Winding data: 34T, #24AWG.

3.3 V Output Inductor, L2

$I_{O3(MIN)} = 0.3$ A; $\Delta I = 0.6$ A.
Using the equation for output inductor, determine L2.

$$L_{O3(MIN)} = \frac{(3.3 + 0.75) \times (1.0 - 0.293)}{100\ k \times 0.6} = 48\ \mu H$$

L2 = 50 µH.
Use a T80–26 Powdered Iron Core from Micrometals.
Winding data: 42T, #24AWG.
Use a 330 µF, 15 V Aluminum Electrolytic Capacitor with ESR = 0.12 Ω on both outputs.
Ripple due to the ESR on the 5.0 V output:

$$\Delta V_{O5} = 0.12 \times 0.5 = 60\ mV_{P-P}$$

Ripple due to the ESR on the 3.3 V output:

$$\Delta V_{O3} = 0.12 \times 0.6 = 72\ mV_{P-P}$$

Because the regulator uses current mode control, the primary side peak current is sensed across the current sense resistor, R10. This primary side current is the combination of currents from both outputs. The effective slope of the current in the primary side is influenced by both output inductors. The outputs are reflected to the main output based on the turns ratio. The combined equivalent circuit is shown in Figure

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Inductance and capacitance reflected from the 3.3 V output to the main output is given by:

$$L'_{O3} = \frac{L_{O3}}{n^2}$$

$$C'_{O3} = C_{O3} \times n^2$$

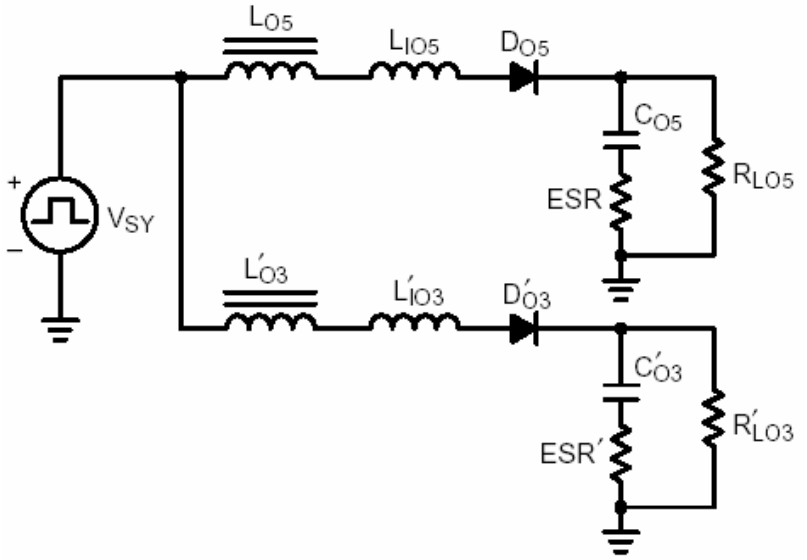
Voltage and current reflected from the 3.3 V output to the main output is given by:

$$V'_{O3} = \frac{V_{O3}}{n}$$

$$I'_{O3} = I_{O3} \times n$$

Reflected ESR is:

$$ESR'_{O3} = \frac{ESR_{O3}}{n^2}$$



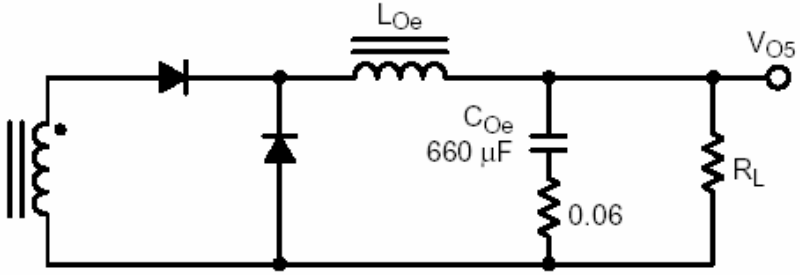


Figure 14. Main Output Equivalent Circuit

The turns ratio for the secondary windings is 1:1.
Then, effective inductance:

$$L_{Oe} = \frac{L_{O5} \times L'_{O3}}{L_{O5} + L'_{O3}}$$

$$L_{Oe} = \frac{100\,\mu \times 50\,\mu}{100\,\mu + 50\,\mu} = 33.3\,\mu H$$

Effective capacitance:

$$C_{Oe} = C'_{O3} + C_{O5} = 330 + 330 = 660\,\mu F$$

Slope Compensation

Because the duty cycle exceeds 50% at low input voltage, slope compensation is required to avoid instability.

Output inductor effective down slope, m_e is given by

$$m_e = \frac{I}{t} = \frac{V_L}{L_e} = \frac{5.0 + 0.75}{33.3\,\mu H} = 0.173\ V/\mu s$$

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The recommended slope compensation is one half of m_e. Due to the increased noise created by the SSPR at turn–on, the slope compensation should be increased to 0.6.

$$m_{COMP(SY)} = 0.7 \times m_e = 0.104\ V/\mu s$$

The compensation voltage, V_{COMP}, is given by:

$$V_{COMP} = \frac{m_{COMP(SY)} \times N_{SY}}{N_{PY}} \times R10$$

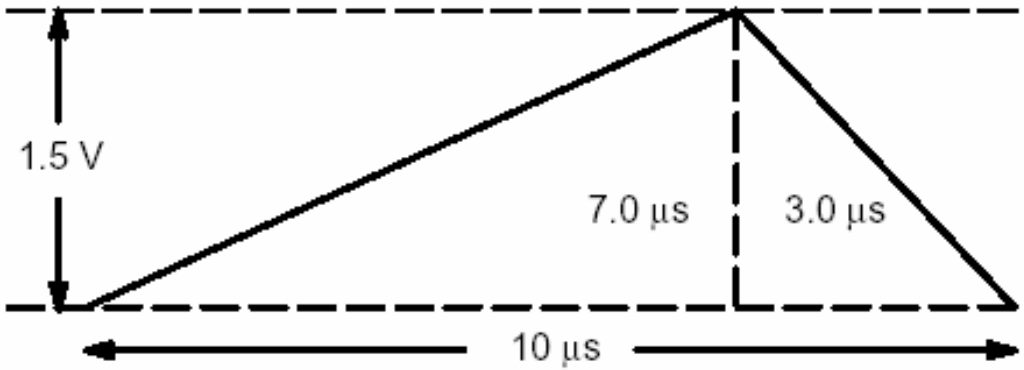

Figure 15. CS3842A Oscillator Voltage

$$V_{COMP} = \frac{0.104 \times 11}{20} \times 0.25 = 14.3 \times 10^{-3}\ V/\mu s$$

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PWM controller oscillator slope (see Figure 15), $\Delta V_{OSC} = 1.7$ V; $\Delta t_{OSC} = 7.0$ µs:

$$m_{OSC} = \frac{1.7}{7.0} = 0.243 \text{ V/µs}$$

$$R4 = \frac{R11 \times m_{OSC}}{m_{COMP}} = \frac{100 \times 0.243}{14.3 \times 10^{-3}} = 1.7 \text{ k}\Omega$$

Main Loop Compensation

Figure 16 shows the main components for loop compensation.

In general, for peak current mode control, the following expressions apply: $I_L = KV_C$ and $V_O = I_L R_L$, where $V_C = \Delta V_e$ (the error amplifier dynamic range).

For CS3842A, $V_C = 2.5$ V, and

$$V_O = K \times R_L \times \frac{V_C}{3.0}$$

From Figure 16,

$$K = \frac{N_{PY}}{N_{SY}} \times \frac{1.0}{R10}$$

Equivalent circuit for the output is shown in Figure 14.

$L_{Oe} = 37.5$ µH; $C_{Oe} = 660$ µF.

The output power range is:

$$P_{OMAX} = 5.0 \times 3.0 + 3.3 \times 2.0 = 21.6 \text{ W}$$

$$P_{OMIN} = 5.0 \times 0.25 = 1.25 \text{ W}$$

$R_{LMAX} = 20\ \Omega$; $R_{LMIN} = 1.16\ \Omega$

Sliding pole:

$$f_P = \frac{1.0}{2.0\pi R_L C_O}$$

$$f_{PMIN} = \frac{1.0}{2.0\pi \times 20\ \Omega \times 660\ \mu F} = 12 \text{ Hz}$$

$$f_{PMAX} = \frac{1.0}{2.0\pi \times 1.16\ \Omega \times 660\ \mu F} = 208 \text{ Hz}$$

Output capacitor ESR zero:

$$f_Z = \frac{1.0}{2.0\pi(ESR)C_O} = \frac{1.0}{2.0\pi \times 0.06 \times 660\ \mu F} = 4.02 \text{ kHz}$$

Control to output gain (see Figure 16):

$$G = \frac{dV_O}{dV_C} = \frac{N_{PY}}{N_{SY}} \times \frac{R_L}{3.0 \times R10}$$

Gain at high line:

$$G_{HL} = \frac{20}{11} \times \frac{20}{3.0 \times 0.25} = 48.5 \text{ (33.7 dB)}$$

Gain at low line:

$$G_{LL} = \frac{20}{11} \times \frac{1.16}{3.0 \times 0.25} = 2.81 \text{ (9.0 dB)}$$

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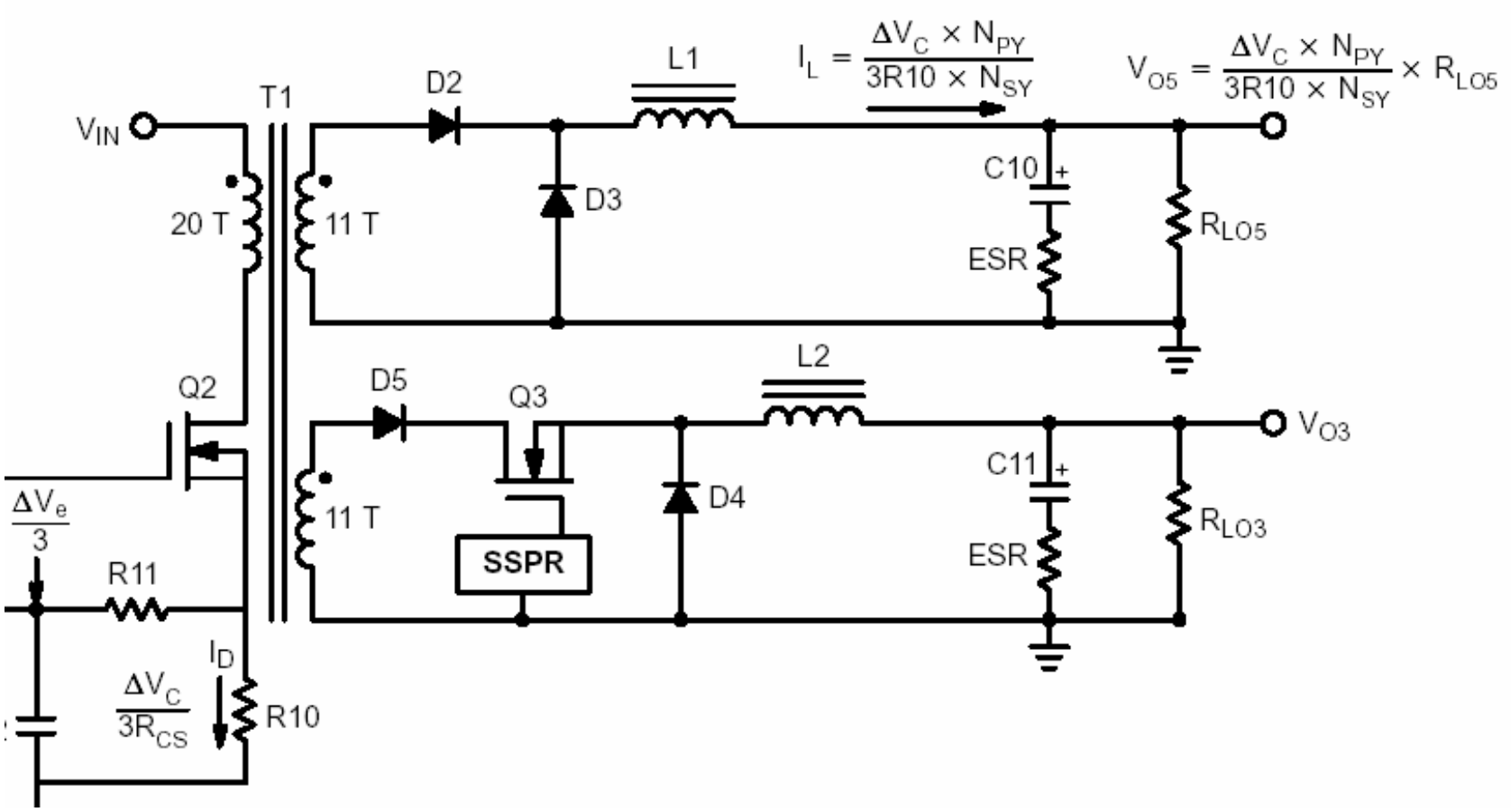

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It is good practice to make the crossover frequency between f_P (pole at high load) and f_{ZESR} (zero of output capacitor), i.e., $f_{CO} = 3.0$ kHz

Error amplifier gain needed to cross at 3.0 kHz:

$$G_{3.0\ kHz} = G_{HL} - 20 \log \frac{f_{CO}}{f_{PMIN}}$$

$$G_{3.0\ kHz} = 33.7 - 20 \log \frac{3.0\ K}{12} = 14.2\ dB\ (5.13\ times)$$

The error amplifier feedback resistor, R3, is equal to:

$$R3 = 5.13 \times R1 = 5.13 \times 4.99\ k\Omega = 25.5\ k\Omega$$

Pole to cancel the ESR zero: $f_{PESR} = f_{ZESR} = 4.02$ kHz, then

$$C1 = \frac{1.0}{2.0\pi \times 4.02\ kHz \times 25.5\ k\Omega} = 1.5\ nF$$

Another zero is placed at low frequency: $f_{Z1} = f_{PMIN} = 12$ Hz, then

$$C13 = \frac{1.0}{2.0\pi \times 12 \times 25.5\ k\Omega} = 520 \times 10^{-9} = 0.47\ \mu F$$

The frequency response diagram of the main loop is shown in Figure 17.

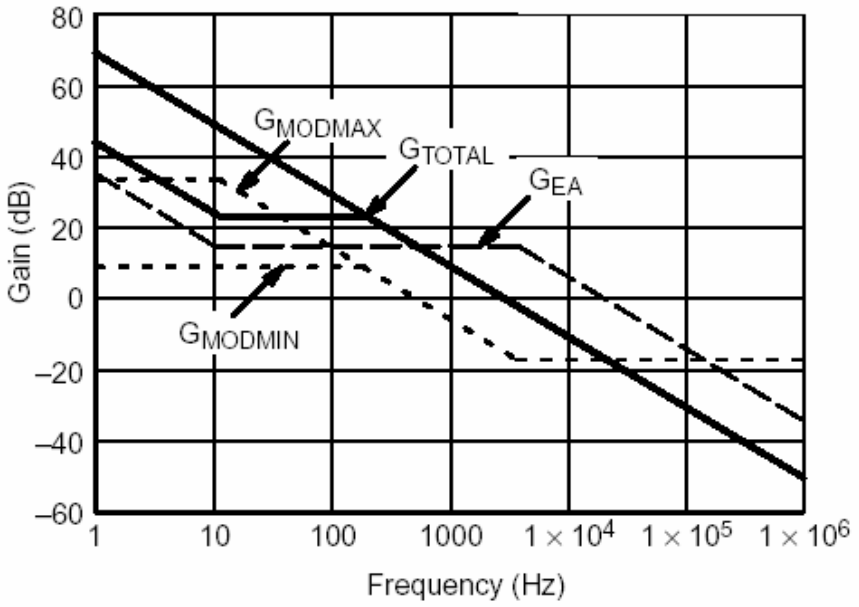

Figure 17. Main Loop Frequency Characteristics

The loop crossover frequency is 3.0 kHz with an adequate phase margin.

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SSPR Controlled Output Calculation

The following data from the specification and the previous calculations are important for the design.

Switching frequency: 100 kHz;

Transfer turns ratio: $N_{PY}:N_{O5}:N_{O3} = 20:11:11$;

Input voltage range: 18 to 36 V_{DC};

Duty cycle range determined by the 5.0 V output, $D_{MAX} = 0.586$, $D_{MIN} = 0.293$;

$L_{O3} = 50\ \mu H$;

$C_{O3} = 330\ \mu F$;

ESR = 0.12 Ω;

Voltage at the 3.3V winding at low line: $V_{SY3} = 18(11/20) = 9.90$ V.

Assuming the Schottky rectifier forward drop is 0.75 V and the DC voltage drop across the FET plus the winding resistance is 0.1 V at full load, the duty cycle required to maintain regulation:

$$D_{O3LL} = \frac{3.3 + 0.75 + 0.1}{9.9} = 0.419$$

$$D_{O3HL} = \frac{3.3 + 0.75 + 0.1}{19.8} = 0.209$$

The difference between the actual duty cycle and required, is calculated at high line;

$$\Delta D_{O3HL} = 0.293 - 0.209 = 0.084$$

For 100 kHz, switching frequency

$$\Delta t_{O3HL} = 10\ \mu s \times 0.084 = 840\ ns$$

The delay time through the SSPR is typically 300 ns, leaving enough head room for a good regulation within the specified voltage range.

Supply Voltage V_{CC} and V_C

The supply voltage is derived directly from the 3.3 V winding. V_{CC} varies with the input voltage, i.e., $V_{CC} = 9.0$ V to 19 V.

V_{CC} is referenced to ground while the gate drive voltage, V_C is bootstrapped and referenced to the source of Q3, i.e., $V_C = 8.0$ V to 18 V.

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SSPR Loop Compensation

The SSPR operates in voltage control mode. The control loop model is shown in Figure 18.

The modulator gain varies with input voltage, and from ref [3] is:

$$G_m = \frac{DV_O}{DV_C} = \frac{-V_{SY}}{\Delta V_C} He(s)$$

He(s) is represented by the double pole of the output filter and zero of the output capacitor's ESR, i.e.,

$$f_P = \frac{1}{2\pi\sqrt{L_2 C_{11}}}; \quad f_Z = \frac{1}{2\pi C_{11} ESR}$$

Modulator gain at input voltage extremes:

$$G_{O3(MAX)} = \frac{19.8}{2.5} = 7.92\ (17.97\ dB)$$

$$G_{O3(MIN)} = \frac{9.9}{2.5} = 3.96\ (11.95\ dB)$$

$$f_{PO3} = \frac{1}{2\pi\sqrt{50\ \mu H \times 330\ \mu F}} = 1.24\ kHz$$

$$f_{ZO3} = \frac{1}{2\pi \times 0.12\ \Omega \times 330\ \mu F} = 4.02\ kHz$$

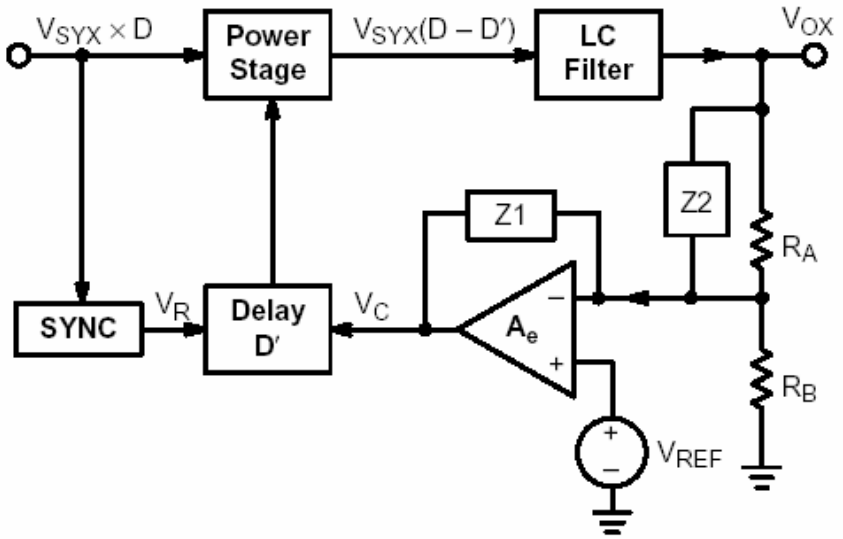

Figure 18. Modular Gain Block Diagram

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Performance Results and Waveforms

The complete schematic, component placement and PC board layout are shown in Figures 22 through 25.

The electrical performance characteristics of the demo board are shown in Table 1.

The load and line regulation of the 3.3 V output is better than 0.3%.

Actual waveforms of the demo board are shown in Figures 20 and 21.

Table 1. Demo Board Performance Measurements

V_{IN}	Main Output		SSPR Output	
	Current	Voltage	Current	Voltage
18 V	0.25 A	5.04	0 A	3.273
18 V	0.25 A	5.04	2.25 A	3.268
18 V	3.0 A	5.04	0 A	3.274
18 V	3.0 A	5.04	2.25 A	3.269
36 V	0.25 A	5.05	0 A	3.277
36 V	0.25 A	5.04	2.25 A	3.272
36 V	3.0 A	5.04	2.25 A	3.276
36 V	3.0 A	5.04	2.25 A	3.272

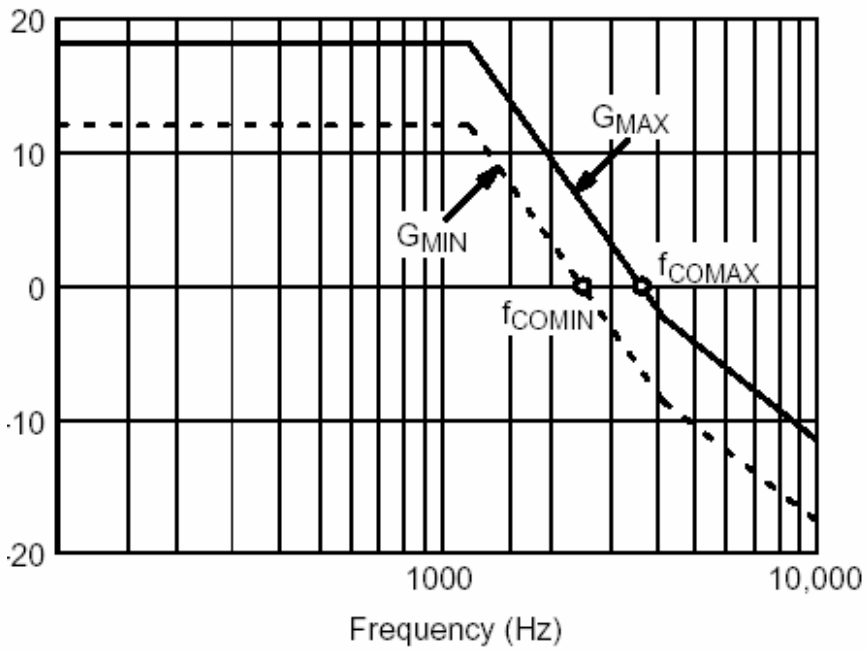

Figure 19. SSPR Loop Frequency Characteristics

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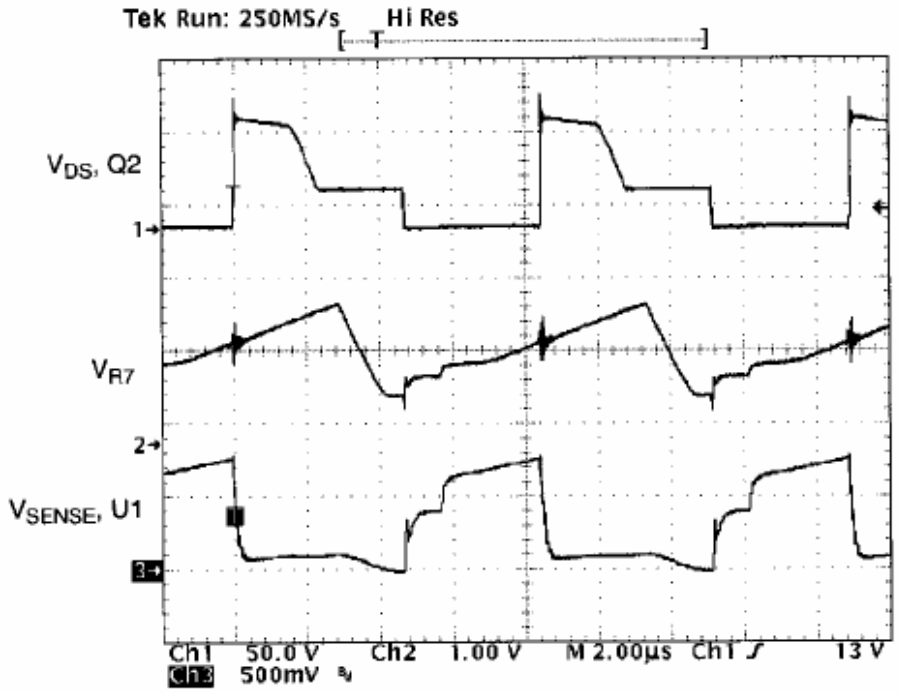

Figure 20. Primary Side Waveforms

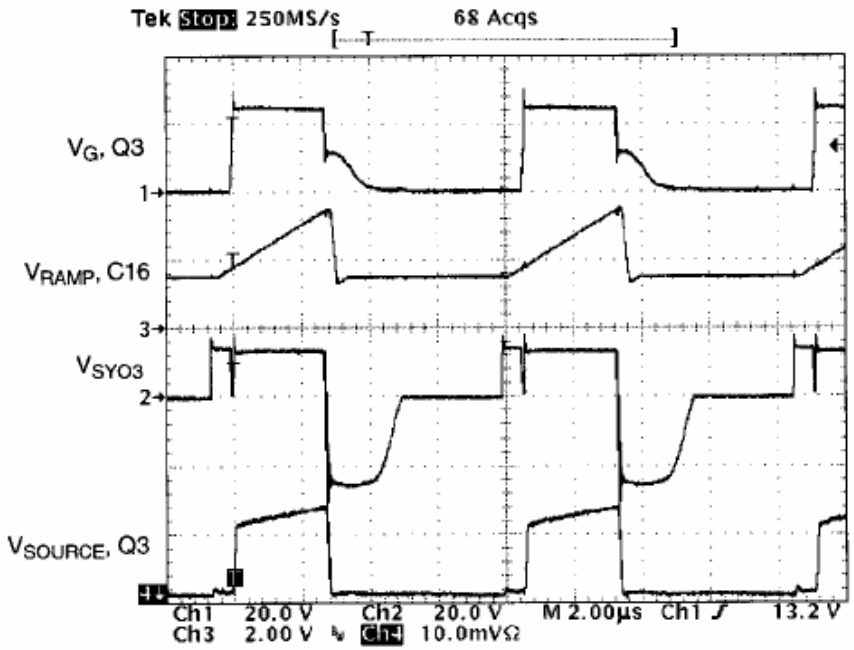

Figure 21. SSPR Waveforms