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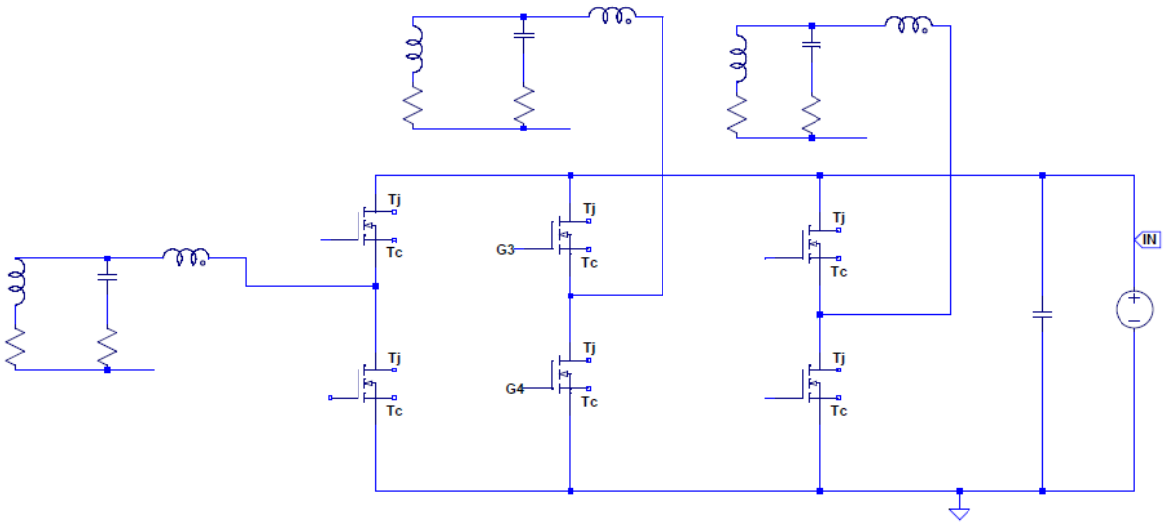
3PHASE 2 LEVEL 33KW PV INVERTER LTSPICE MODEL

REV 1



This document is prepared as a quick reference guide to perform simulations based on Wolfspeed SiC power MOSFET PSPICE library using LTSPICE simulation software.

DISCLAIMER

Models provided by Wolfspeed are not warranted by Wolfspeed as fully representing all of the specifications and operating characteristics of the semiconductor product to which the model relates. The model describes the characteristics of a typical device. In all cases, the current data sheet information for a given device is the final design guideline and the only actual performance specification. Although models can be a useful tool in evaluating device performance, they cannot model exact device performance under all conditions, nor are they intended to replace laboratory testing for final verification. This model is preliminary and subject to change without notice. Wolfspeed will not be responsible for any error or simulation issue arising due to the editing of the model library file.

MODEL SPECIFICATIONS
SPECIFICATION OF PV INVERTER:
Vin = 850Vdc
Vout = 480Vac L-L @ 60Hz
Pout = 33KW
Switching Frequency = 50 KHz

MODEL LIMITATIONS

- This inverter model is purely simulating the performance of the switching device of Wolfspeed products and without considering others parasitic from capacitor and transformer losses.
- No feedback control circuit has developed
- Refer to C2M LTSPICE User Guide for C2M0025120D component model limitation.

ABOUT 3 PHASE 2 LEVEL 33KW PV INVERTER LTSPICE MODEL
This LTspice model is created based on the PV inverter design requirement by incorporate six Wolfspeed C2M0025120D MOSFETs to the design. The intention of creating this inverter circuit is to provide customers a sample reference circuit and a quicker way to evaluate the performance of Wolfspeed SiC MOSFET. This model also enable user to modify some of the components value to achieve a different design requirement.

PREREQUISITE:
LTSPICE simulation software (http://www.linear.com/designtools/software/#LTspice)
MOSFET SPICE PACKAGE:

- SPICE Library Packaged Device Model (C2M0XXX120D - Packaged .lib) – Model includes the TO-247 package parasitic[1].
- LTSPICE Device Symbol (power_nmos_heat.asy)

SOFTWARE REQUIREMENT:
This model has been developed and optimized for LTSPICE. It is the responsibility of the user to be well-versed with the basic operation of LTSPICE simulation tool. Using this model on other PSPICE simulation tool may result in convergence error or incorrect simulation result. Please use the recommended software.

MODEL INSTALLATION GUIDELINES:
1. Extract the zip file.

2. Copy the 3phase 2 level PV inverter model file and paste it into the LTSPICE directory or any folder that user normally used. Typical path is given by (C:\Program Files (x86)\LTC\LTspiceIV\). This would make the model appear in the open window.

3. The model will be similar to the one shown in figure 1.
4. This model allows user to change the value of some components to meet their design requirement.

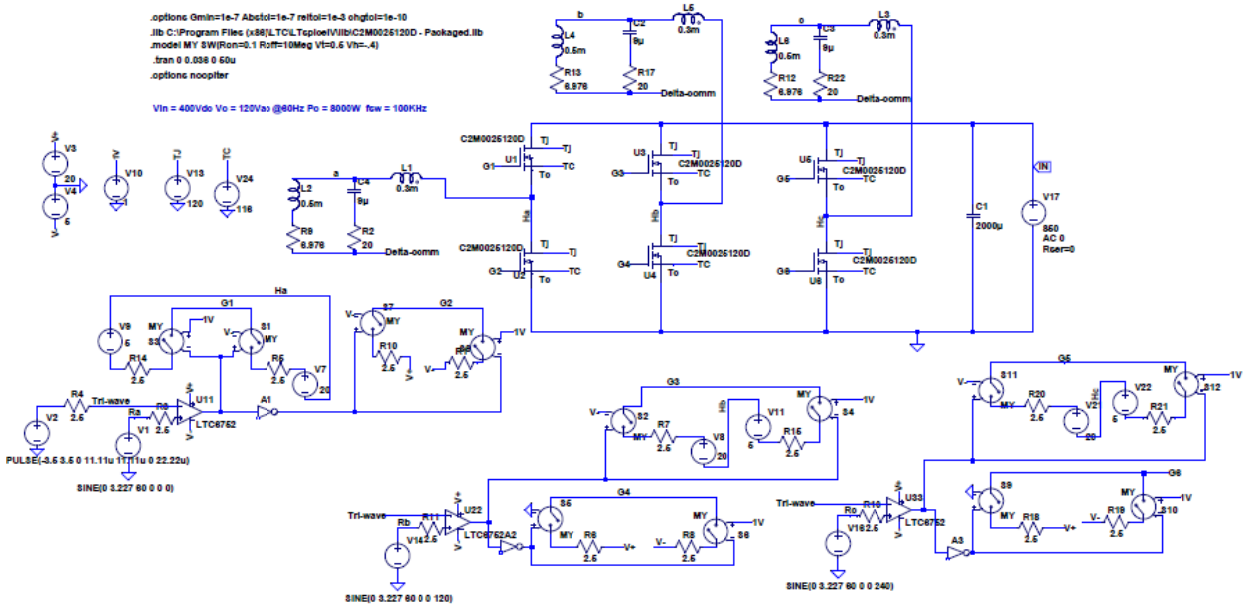


Figure 1: 3phase 2 level PV inverter model circuit

SIMULATION GUIDELINES:

In case user has difference design requirement, below are the component value at Inverter SPICE model that allows user to change in order to produce the desired output:

- Vin (V17)
- Vout (Va, Vb, Vc with respect to Delta-comm)
- Triangle source (V2)
- Phase A control source (V1)
- Phase B control source (V14)
- Phase C control source (V16)
- Tj source (V13)
- Tc source (V24)
- Output load (R9, R12, R13)

The terminals Tj and Tc are representing the temperature of the junction and case of the MOSFET. The temperature connections are working as voltage pins. Therefore a potential difference of 1V refers to a temperature difference of 1°C. User can vary these values base on your own cooling design and observe the performance of the MOSFET or inverter.

While performing simulations, it is not recommended to change simulation settings of the following SPICE directive which is already optimized base on the simulation speed and avoid any convergence error.

.options Gmin=1e-7 Abstol=1e-7 reltol=1e-3 chgtol=1e-10

RESULTS

Description	Design Requirement	LTspice Results	SpeedFit Results ***	Experimental Results
$V_{o\ rms}$ (V)	277	274.22	277	N.A.
$V_{o\ L\text{-}L}$ (V)	480	475	480	N.A.
Output Frequency (Hz)	60	60	60	N.A.
P_o (KW)	33	32.512	33.04	N.A.
Ploss**(W)		434.54	389.45	N.A.
Efficiency (%)*		98.68	98.82	N.A.

Table 1 LTspice result against design requirement

*** Efficiency is only based on semiconductor only.**

**** Ploss is the total semiconductor loss which is conduction and switching losses.**

***** SpeedFit is a Wolfspeed online simulation tool [2].**

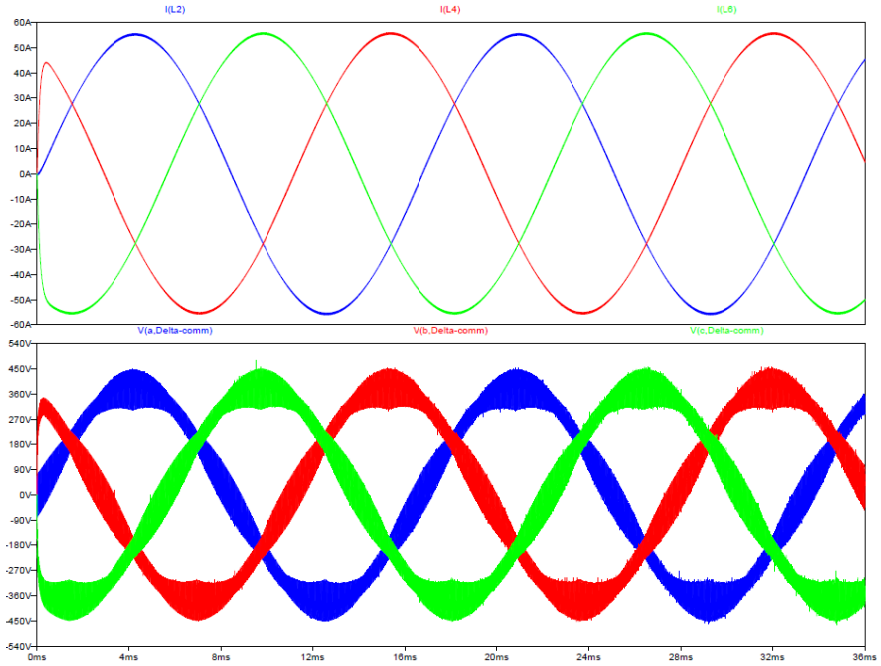


Figure 2: Inverter output voltage and current

REFERENCE

[1] Wolfspeed MOSFET LTspice models. Citing Websites. From http://go.wolfspeed.com/MOSFETModel

[2] SpeedFit, Wolfspeed online simulation tool. Citing Websites. From http://www.wolfspeed.com/speedfit/