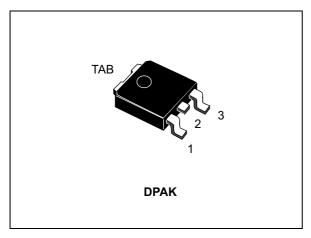
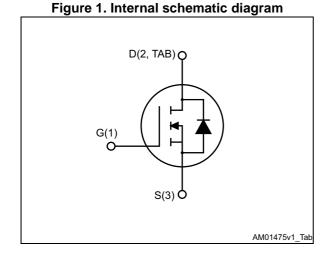
STD86N3LH5



Automotive-grade N-channel 30 V, 0.0045 Ω typ, 80 A STripFET H5 Power MOSFET in a DPAK package

Datasheet - production data





Features

Order code	V _{DSS}	R _{DS(on)} max	I _D
STD86N3LH5	30 V	< 0.005 Ω	80 A

- Designed for automotive applications and AEC-Q101 qualified
- Low on-resistance R_{DS(on)}
- · High avalanche ruggedness
- · Low gate drive power losses

Application

· Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™ H5 technology. The device has been optimized to achieve very low on-state resistance, contributing to a FoM that is among the best in its class.

Table 1. Device summary

Order code	Marking	Package	Packaging
STD86N3LH5	86N3LH5	DPAK	Tape and reel

Contents STD86N3LH5

Contents

1	Electrical ratings
2	Electrical characteristics
	2.1 Electrical characteristics (curves)
3	Test circuit
4	Package information
5	Packing information
6	Revision history

STD86N3LH5 Electrical ratings

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage (V _{GS} = 0 V)	30	V
V _{DS}	Drain-source voltage (V _{GS} = 0 V) @ T _{JMAX}	35	V
V _{GS}	Gate-source voltage	± 20	V
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25 °C	80	Α
I _D	Drain current (continuous) at T _C = 100 °C	55	Α
I _{DM} ⁽²⁾	Drain current (pulsed)	320	А
P _{TOT}	Total dissipation at T _C = 25 °C	70	W
	Derating factor	0.47	W/°C
E _{AS} (3)	Single pulse avalanche energy	165	mJ
T _{stg}	Storage temperature	-55 to 175	°C
T _j	Max. operating junction temperature	175	°C

^{1.} Limited by wire bonding

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case max	2.14	°C/W
R _{thj-pcb} (1)	Thermal resistance junction-pcb max	50	°C/W

^{1.} When mounted on 1 inch² FR-4 Oz Cu board

^{2.} Pulse width limited by safe operating area

^{3.} Starting Tj = 25°C, I_D = 40 A, V_{DD} = 25 V

Electrical characteristics STD86N3LH5

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	30	-	-	V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0 V)	V _{DS} = 20 V V _{DS} = 20 V,Tc = 125 °C	-	-	1 10	μA μA
I _{GSS}	Gate body leakage current (V _{DS} = 0 V)	V _{GS} = ± 20 V	ı	-	±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1	1.8	2.5	V
P-o/	Static drain-source on-	$V_{GS} = 10 \text{ V}, I_D = 40 \text{ A}$	ı	0.0045	0.005	Ω
R _{DS(on)}	resistance	$V_{GS} = 5 \text{ V}, I_D = 40 \text{ A}$	-	0.0055	0.0065	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		-	1850	-	pF
C _{oss}	Output capacitance	V _{DS} = 25 V, f=1 MHz,	-	380	-	pF
C _{rss}	Reverse transfer capacitance	$V_{GS} = 0 V$	-	58	-	pF
Qg	Total gate charge	V _{DD} = 15 V, I _D = 80 A	-	14	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 5 V	-	6.8	-	nC
Q _{gd}	Gate-drain charge	Figure 16	-	4.7	-	nC
Q _{gs1}	Pre V _{th} gate-to-source charge	$V_{DD} = 15 \text{ V}, I_{D} = 80 \text{ A}$ $V_{GS} = 5 \text{ V}$	-	2.3	-	nC
Q _{gs2}	Post V _{th} gate-to-source charge	Figure 16	-	4.5	-	nC
R _G	Gate input resistance	f = 1 MHz gate bias Bias = 0 test signal level = 20 mV, open drain	-	1.2	-	Ω



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Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time		-	6	-	ns
t _r	Rise time	$V_{DD} = 15 \text{ V}, I_D = 40 \text{ A},$ $R_G = 4.7 \Omega, V_{GS} = 5 \text{ V}$	-	14	-	ns
t _{d(off)}	Turn-off delay time	$R_G = 4.7 \Omega_S$, $V_{GS} = 5 V$ Figure 15	-	23.6	-	ns
t _f	Fall time		-	10.8	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		80	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)				320	Α
V _{SD} ⁽²⁾	Forward on voltage	$I_{SD} = 40 \text{ A}, V_{GS} = 0$	1		1.1	V
t _{rr}	Reverse recovery time	I _{SD} = 80 A,	1	31.8		ns
Q _{rr}	Reverse recovery charge	di/dt = 100 A/µs, V _{DD} = 20 V	ı	26.1		nC
I _{RRM}	Reverse recovery current	Figure 17	ı	1.6		Α

^{1.} Pulse width limited by safe operating area

^{2.} Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Electrical characteristics STD86N3LH5

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

Figure 3. Thermal impedance

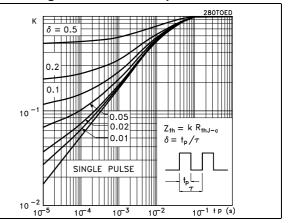


Figure 4. Output characteristics

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Figure 5. Transfer characteristics

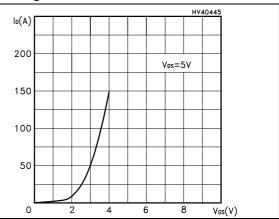


Figure 6. Normalized B_{VDSS} vs temperature

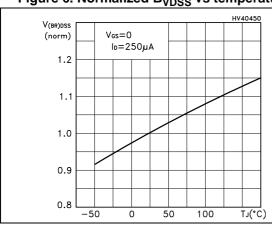
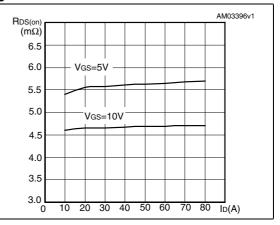


Figure 7. Static drain-source on resistance



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Figure 8. Gate charge vs gate-source voltage

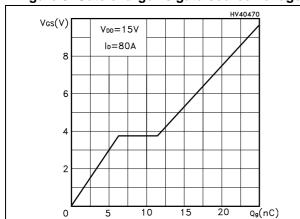


Figure 9. Capacitance variations

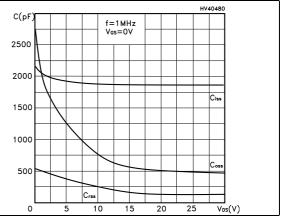
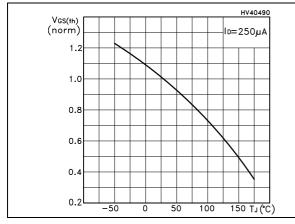


Figure 10. Normalized gate threshold voltage vs temperature

Figure 11. Normalized on resistance vs temperature



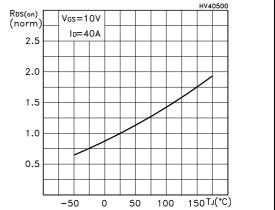
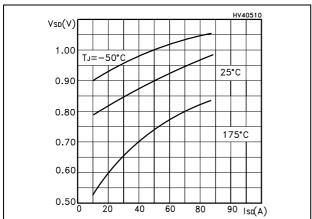


Figure 12. Source-drain diode forward characteristics



Test circuit STD86N3LH5

3 Test circuit

Figure 13. Switching times test circuit for resistive load

Figure 14. Gate charge test circuit

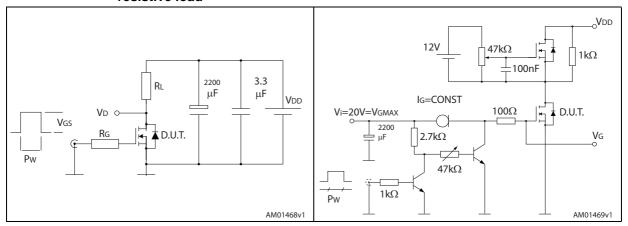


Figure 15. Test circuit for inductive load switching and diode recovery times

Figure 16. Unclamped inductive load test circuit

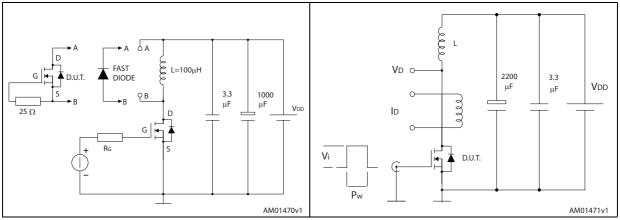
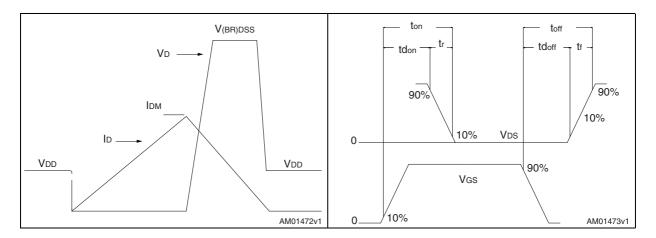


Figure 17. Unclamped inductive waveform

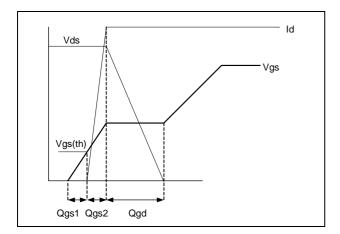
Figure 18. Switching time waveform



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STD86N3LH5 Test circuit

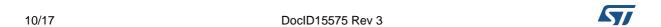
Figure 19. Gate charge waveform



Package information STD86N3LH5

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.



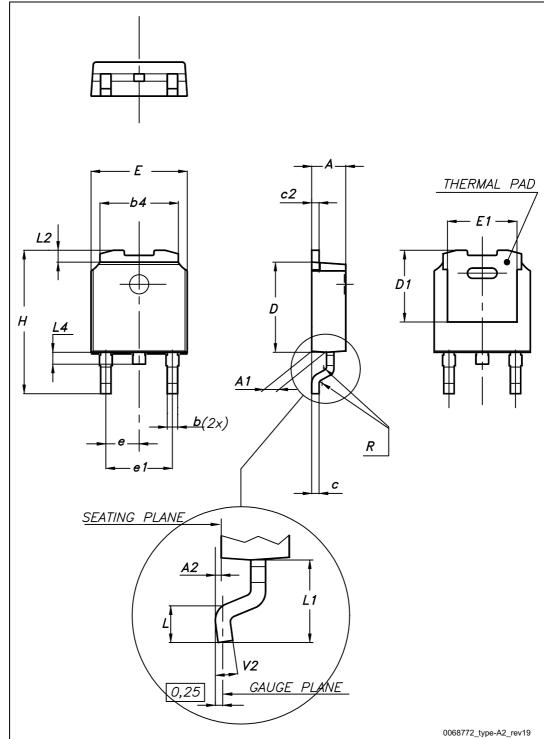


Figure 20. DPAK (TO-252) type A2 outline

Package information STD86N3LH5

Table 8. DPAK (TO-252) type A2 mechanical data

Dim		mm	
Dim.	Min.	Тур.	Max.
А	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
С	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
Е	6.40		6.60
E1	5.10	5.20	5.30
е	2.16	2.28	2.40
e1	4.40		4.60
Н	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

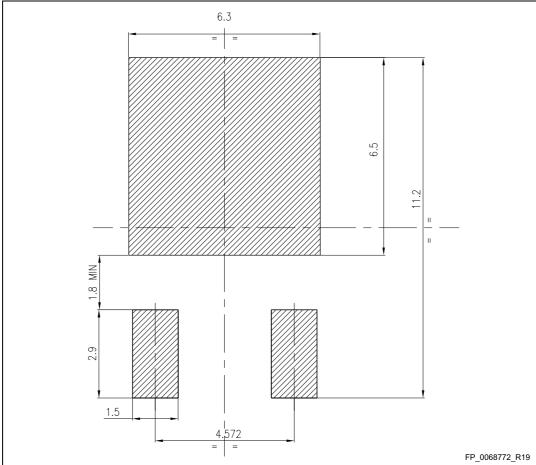


Figure 21. DPAK (TO-252) footprint ^(a)

a. All dimensions are in millimeters

Packing information STD86N3LH5

5 Packing information

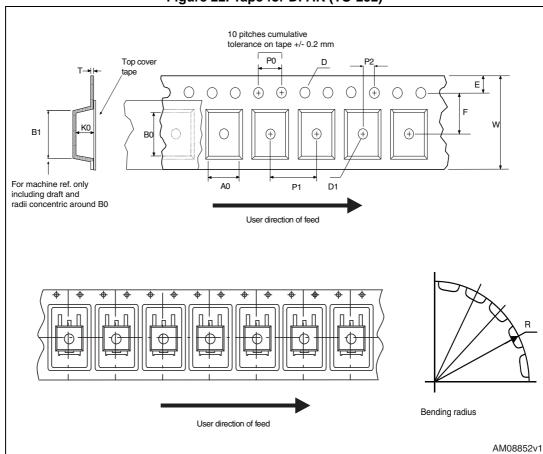


Figure 22. Tape for DPAK (TO-252)

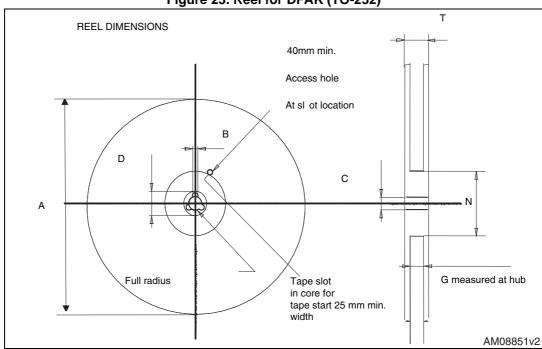


Figure 23. Reel for DPAK (TO-252)

Table 9. DPAK (TO-252) tape and reel mechanical data

	Таре			Reel	
Dim.	mm		Dim.	mm	
Dilli.	Min.	Max.		Min.	Max.
A0	6.8	7	А		330
В0	10.4	10.6	В	1.5	
B1		12.1	С	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
Е	1.65	1.85	N	50	
F	7.4	7.6	Т		22.4
K0	2.55	2.75			
P0	3.9	4.1		Base qty.	2500
P1	7.9	8.1		Bulk qty.	2500
P2	1.9	2.1			
R	40				
Т	0.25	0.35			
W	15.7	16.3			

Revision history STD86N3LH5

6 Revision history

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Table 10. Document revision history

Date	Revision	Changes
10-Apr-2009	1	First release.
22-Mar-2011	2	V _{GS} value has been corrected in <i>Table 2</i> and <i>Table 4</i> .
13-May-2015	3	Updated title, features and description in cover page. Updated Section 4: Package information.

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