Alexandria University
Faculty of Engineering
Computer and Systems
Engineering Dept.
First Year

CS131: Digital Computer
Fundamentals
Fall 2025/2026

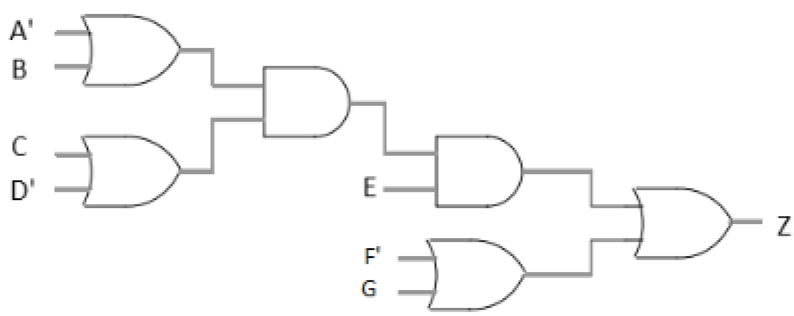
Sheet 6

1. **Using AND and OR gates, find a minimum circuit to realize f(a, b, c, d)= m4 + m6 + m7 + m8 + m9 + m10**
    a. **using two-level logic**
    b. **using three-level logic (12 gate inputs minimum)**

2. **Realize Z= A′D + A′C + AB′C′D′ using four NOR gates.**

3. **Realize Z= ABC + AD + C′D′ using only two-input NAND gates. Use as few gates as possible.**

4.
    a. **Convert the following circuit to all NAND gates, by adding bubbles and inverters where necessary.**
    b. **Convert to all NOR gates (an inverter at the output is allowed).**



5. **Find a minimum two-level NAND-NAND circuit to realize the function given in Equations f = Σ m(6, 7, 8, 9, 13, 14, 15)**

6. **f(a, b, c, d, e) = Σ m(2, 3, 6, 12, 13, 16, 17, 18, 19, 22, 24, 25, 27, 28, 29, 31)**
    a. **Find a minimum two-level NOR-gate circuit to realize f.**
    b. **Find a minimum three-level NOR-gate circuit to realize f.**

7.
    a. **Find a minimum two-level, multiple-output NAND-NAND circuit to realize f1 = Σ m(0, 2, 4, 6, 7, 10, 14) and f2 = Σ m(0, 1, 4, 5, 7, 10, 14).**
    b. **Repeat for a minimum two-level, multiple-output NOR-NOR circuit**

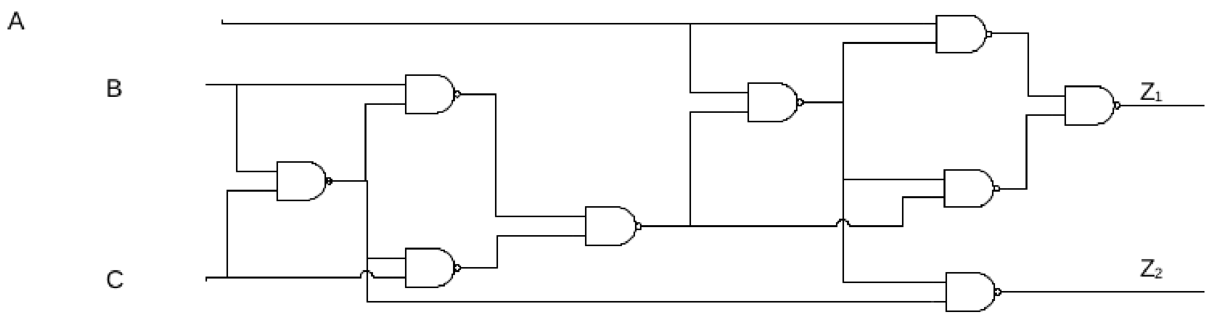
8. **Express the outputs of the following network as functions of the input variables using AND-OR-NOT functions. Check the circuit in the next page**

Policies:

- If 2 or more copies are discovered, both parties will receive serious submission penalties.
- No late submission is allowed.

Alexandria University
Faculty of Engineering
Computer and Systems
Engineering Dept.
First Year

CS131: Digital Computer
Fundamentals
Fall 2025/2026



Policies:

- If 2 or more copies are discovered, both parties will receive serious submission penalties.
- No late submission is allowed.