Appendix A

Design checklist

Many factors must be considered when looking at the EMC aspects of a design, and it is easy to overlook an important point. This generic checklist is provided for you to assess your design against as it proceeds. For particular classes of design, you will want to expand it with your own experience.

- Design for EMC from the beginning; know what performance you require
- Partition the system into critical and non-critical sections:
  - determine which circuits will be noisy or susceptible and which will not
  - lay them out in separate areas as far as possible
  - select internal and external interface locations to allow optimum common mode current control
- Select components and circuits with EMC in mind:
  - use slow and/or high-immunity logic; apply slew rate limiting to data transmission interfaces
  - use series R buffering on all high-speed clock and data lines
  - use good power decoupling techniques: small, low-inductance capacitors adjacent to the ICs they are decoupling
  - use series ferrite chips in the supplies to create power segments
  - reduce fan-out on clock circuits by liberal use of buffers
  - minimize analogue signal bandwidths
  - maximize dynamic range of analogue signal paths
  - check stability in wideband amplifiers
  - don't leave unused IC input pins floating: tie them to 0V or V_{CC}
  - include resistive, ferrite or capacitive filtering at all sensitive analogue inputs
  - incorporate a watchdog circuit on every microprocessor
  - avoid edge triggered digital inputs if possible, protect them if unavoidable
- PCB layout:
  - refer to separate checklist in section 11.2.4
- Cables:
  - segregate, and avoid parallel runs of, signal and power cables

- choose RF-screened cables if the wanted signal cannot be properly filtered
- avoid screened cable with the screen connected only at one end; if unavoidable, treat the cable as unscreened at RF
- use twisted pair both within and outside an enclosure, for balanced or high di/dt lines
- use properly designed looms, ribon or flexi for internal wiring – avoid loose wires or bundles
- run cables away from apertures in the shielding, tied close to conductive grounded structures
- apply ferrite suppressors to damp resonances and control common mode currents
- ensure that cable screens are properly terminated to the connector backshell; avoid pigtails
- terminate lines carrying high frequency signals with the correct transmission line impedance

- Grounding:
  - design and enforce the ground system at the product definition stage
  - consider the ground system as a return current path, not just as 0V reference
  - provide for parallel earth conductors at the system level
  - ensure metal-to-metal bonding of screens, connectors, filters, and enclosure panels
  - ensure that bonding methods will not deteriorate in adverse environments
  - mask paint from, and apply a conductive finish to, any intended contact surfaces
  - keep earth straps short and define their geometry
  - avoid common ground impedances for different circuits
  - provide an interface ground area for decoupling and filtering
- Filters:
  - assume that a supply filter is needed: design the filter for the application
  - filter all I/O lines, using either or both of three-terminal capacitors to interface ground, and common mode chokes
  - apply π filters at the DC power input to each board, in multi-board designs
  - ensure a defined ground return for each filter
  - apply filtering to interference sources, such as switches or motors, directly at their terminals
  - locate all filter components and associated wiring or tracks adjacent to the interface being filtered

- Shielding:
  - design all metallic structures as if they were electrical components: account for their stray capacitance and inductance
  - consider segregated enclosures: enclose particularly sensitive or noisy areas with extra internal shielding
  - avoid large or resonant apertures in a shield, or take measures to mitigate them
  - avoid dipole-like structures in a metallic enclosure
  - ensure that separate panels are well bonded along their seams using conductive gaskets: apply good bonding practice as in “grounding” above
  - design plastic enclosures to allow internal conductive coating if necessary
  - decide on and implement DC or RF tie points between circuit 0V and the shield
  - use multiple internal tie-points to minimize box resonances
- Test and evaluate for EMC continuously as the design progresses