



Home > emi filter pcb layout guidelines

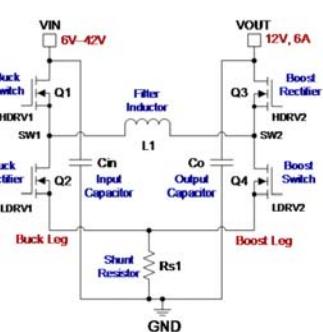
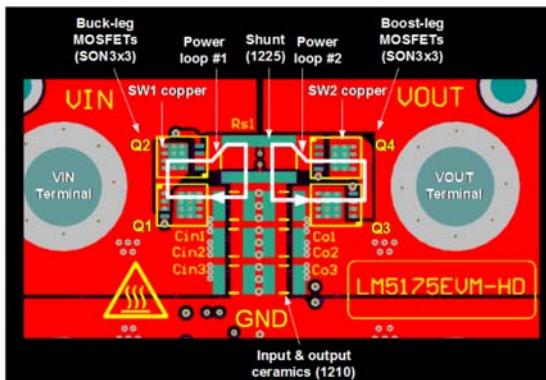
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Emi Filter Pcb Layout

Beranda

Written By voice — Thursday, January 1, 1970 — Add Comment

The bottom side of the board is a shielding reference ground area. Pcb via layout dimensions depend on pcb fabrication and assembly capabilities.



High Density Pcb Layout Of Dc Dc Converters Part 1 Power

More critical applications involving mil grade aerospace and healthcare will witness a higher failure rate.

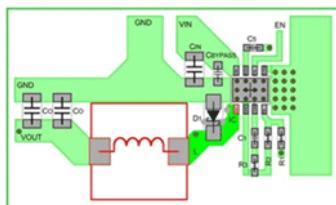
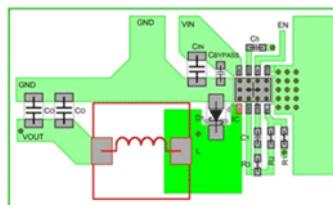


Figure 6-a. Desirable wiring to inductor

Figure 6-b. Undesirable wiring to inductor
Copper foil area broader than needed

Emi filter pcb layout. Couple that with the ever rising demand for higher clock speeds and you begin to realize why reducing emi is more important than ever before. Pcb design for emc can enable a circuit board to perform well in terms of its emc performance and to help there are a few basic guidelines that

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Location location location preventing emi coupling 1. Reduce emi in your next pcb design. Tle6365 pcb layout and emc filtering z8f52274259 dc dc converter application the circuit was developed in a way that all components are located on the top layer of a 2 layer pcb.

Your design needs to have some resistance to noise as well as emit low noise to be compatible with fcc and eu requirements. The evaluation boards provide more specialized solutions for certain emc problems and can be seen as addition to the design kit. Emi filter circuit design for your next pcb by zm peterson bullet.

Design your emc line filter step by step. Signals below 50 khz are not emi concerns 14 basic loops every edge transition that is sent from the microcomputer to another chip is a current pulse. Figure 4 shows that the electrical circuit c1 t.

Use of solder mask beneath component is not recommended. Noise suppression becomes even more important as operating frequencies rise and signal levels fall this becomes more manageable with an emi noise filter on a pcb design. Design your emc filter.

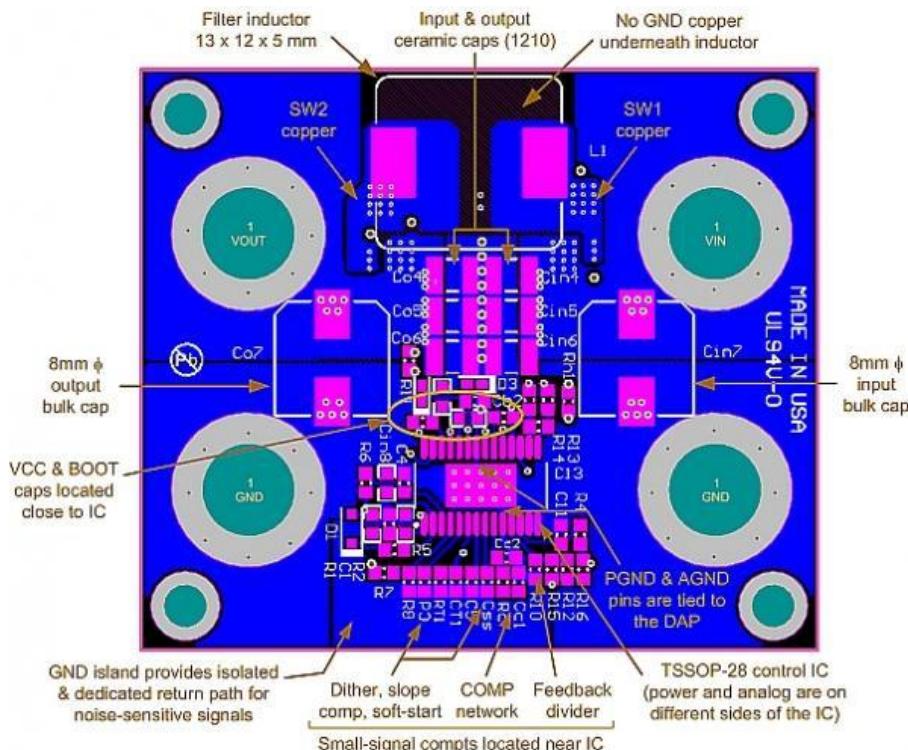
100 khz clock function may need to filter no need to filter 20 us figure 1. Its all too easy to accidentally create an antenna in the way you layout the traces and vias on your board. Pcb layout guidelines component specific terminal pad dimensions are listed in the jdi x2y datasheet.

Adding filtration to your pcb designs can enhance signal integrity in emi prone environments with large stray magnetic fields and in low power rf applications. The following table gives an overview on outstanding. This document provides

The topics covered include pcb design considerations regarding the routing of high speed signals selecting stack up of the pcb selecting decoupling components impedance controlled design of the traces and termination of high speed. One of the key areas of designing a circuit with good emc performance is that of the pcb design. 3222 emi filters.

On printed circuit board stiffeners making the. A poor design is the ultimate cause of unwanted em emission or susceptibility towards it which is why we combined our pcb design guidelines for emi and emc. The current pulse goes to the.

Emi has been the bane of many designs and will affect your products ability to pass emc certification tests.



Dc Dc Converter Pcb Layout Part 2

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Pcb Layout For Smps Part 2 Ti Com Video

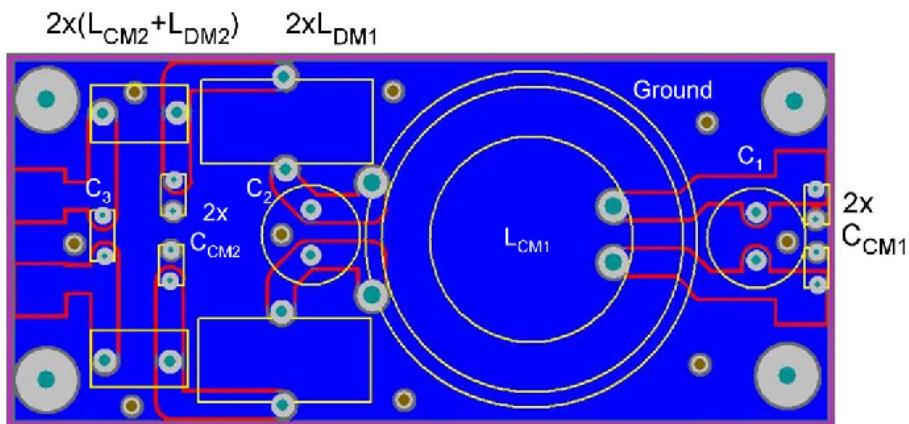
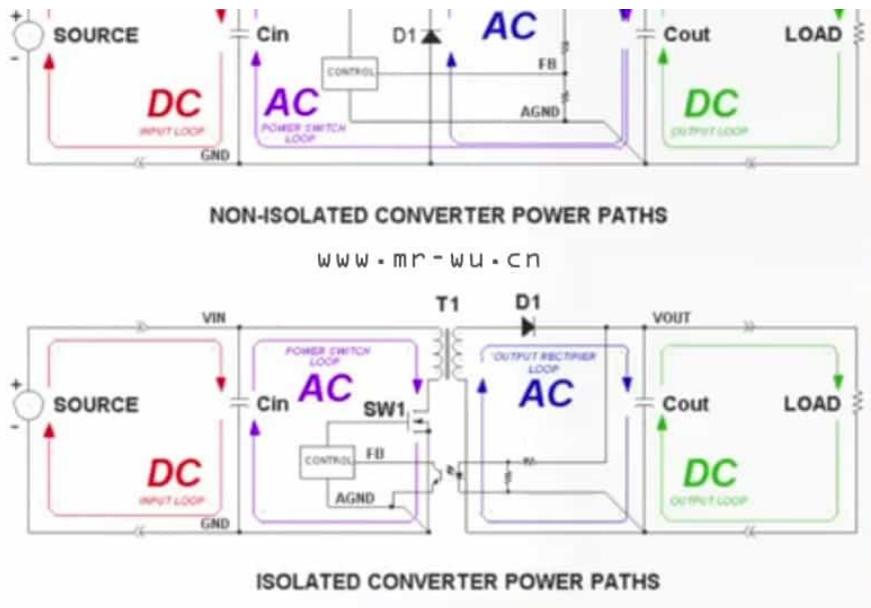


Figure 16 From Parasitic Effects Of Grounding Paths On Common Mode

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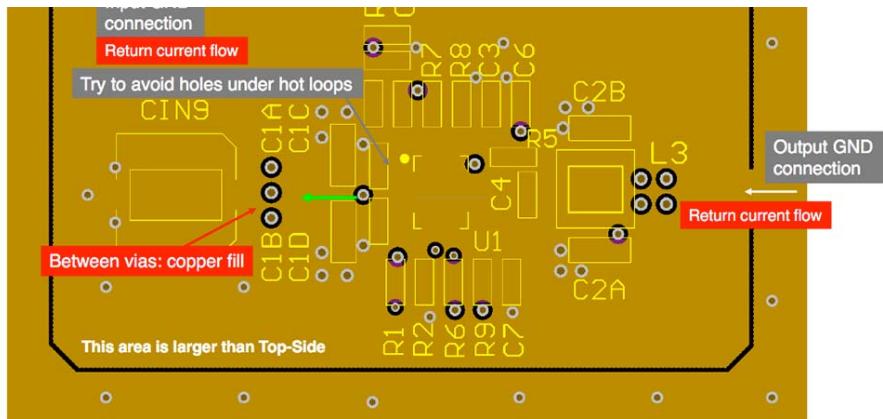
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Design Your Emc Filter Wurth Elektronik Electronic

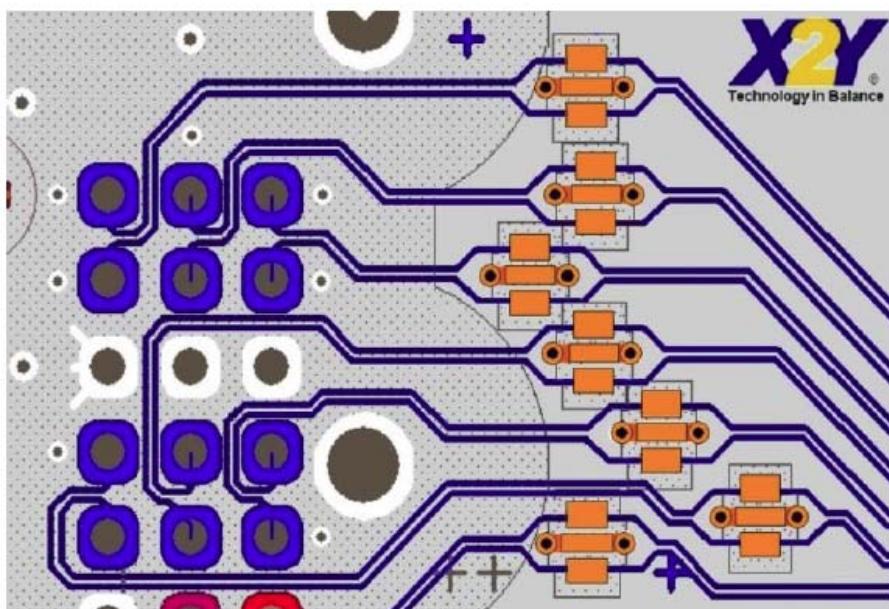


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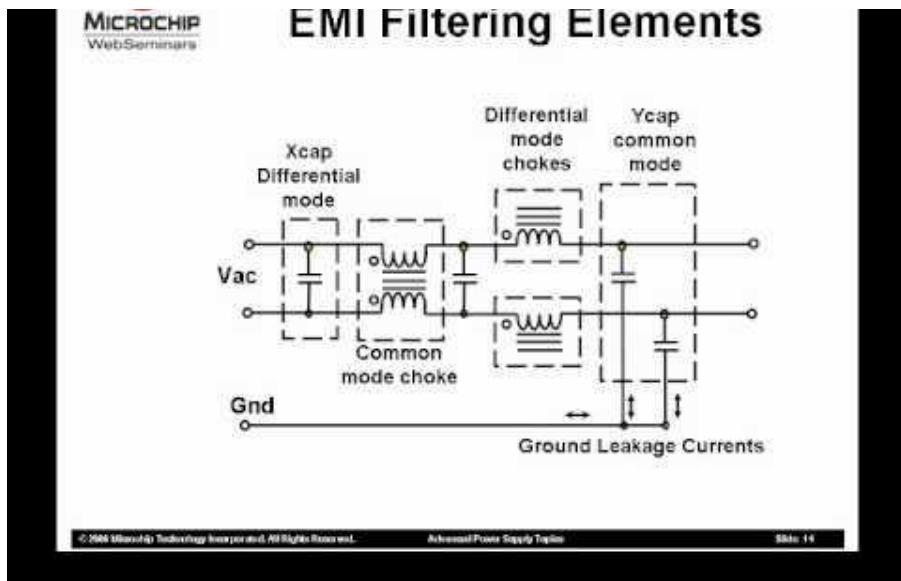
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High Voltage Capacitors And Power Resistors Johanson
Dielectrics

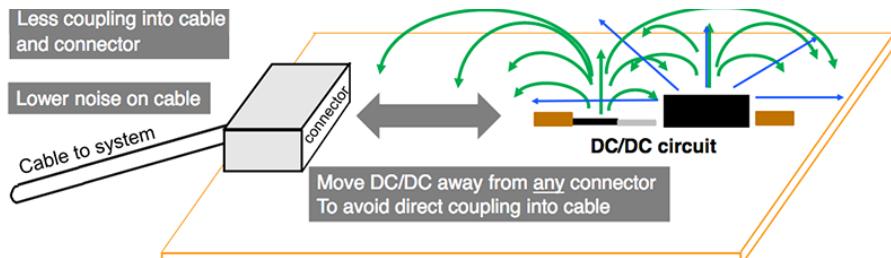


Advanced Smps Topics Emi Filtering Youtube



5uh Lsn For Spectrum Analyzer Emc Emi Work

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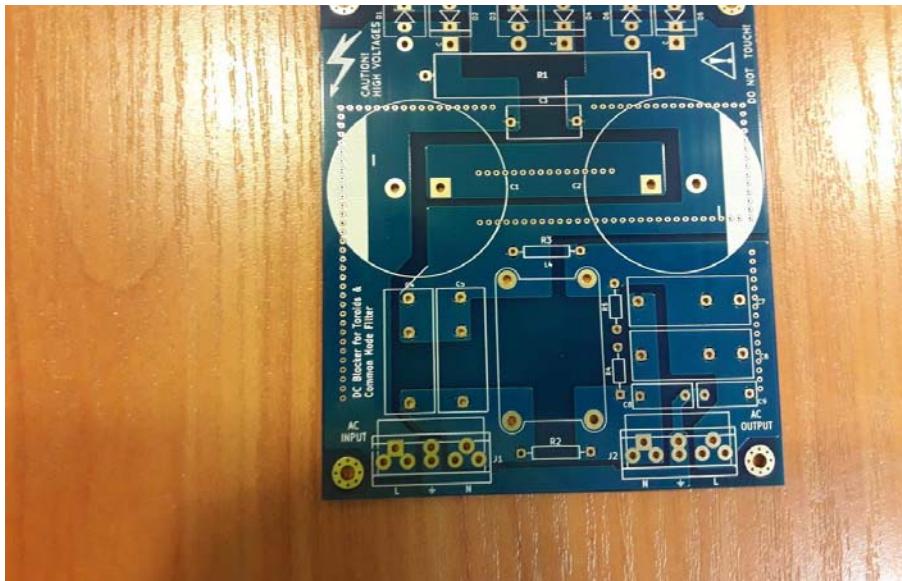
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- EMC filter components must be placed close to connector
- In case of two side assembly, EMC filter on opposite side with respect to DC/DC Converter gives best results

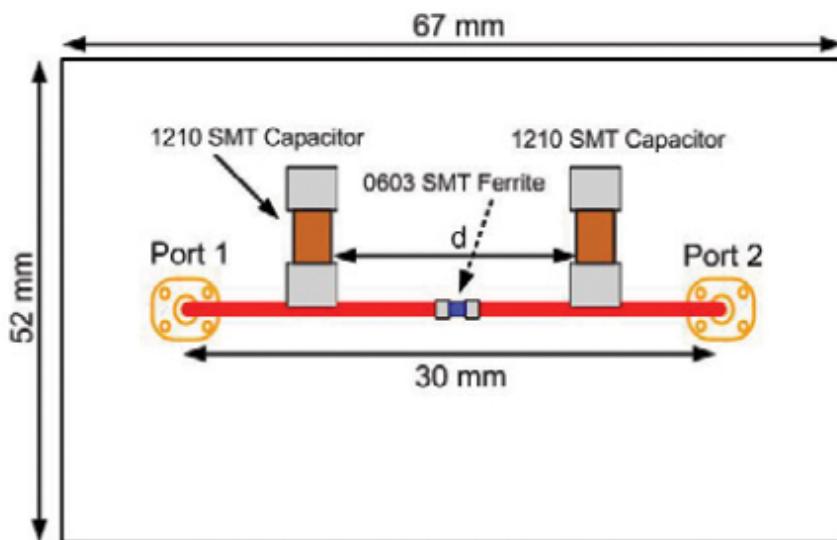
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Pcb Emi Filter Lumenis Lume One Pc6629010 Lume One Parts
Only



Pcb For Combined Dc Blocker Trap Filter Emi Rfi Common Mode



Noise Mitigation Analysis Of A P Filter For An Automotive Control

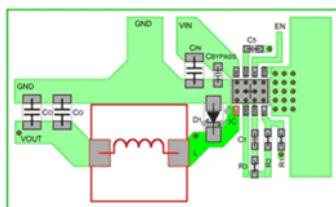


Figure 6-a. Desirable wiring to inductor

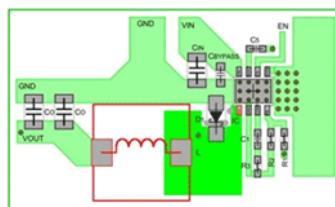
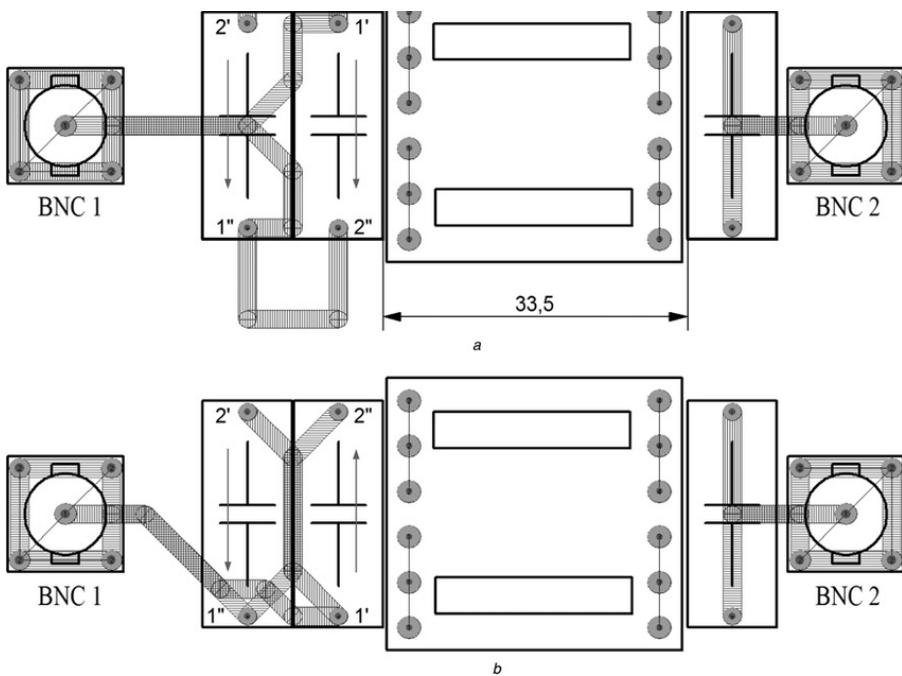


Figure 6-b. Undesirable wiring to inductor
Copper foil area broader than needed

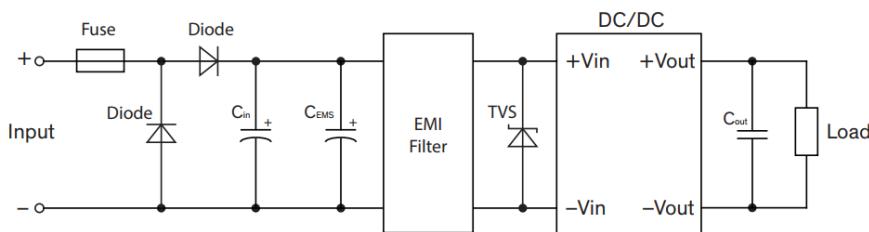
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Pcb Layout For Measuring The Coupling Between Two Capacitors

Suggested filter to comply with EN 50155 Immunity

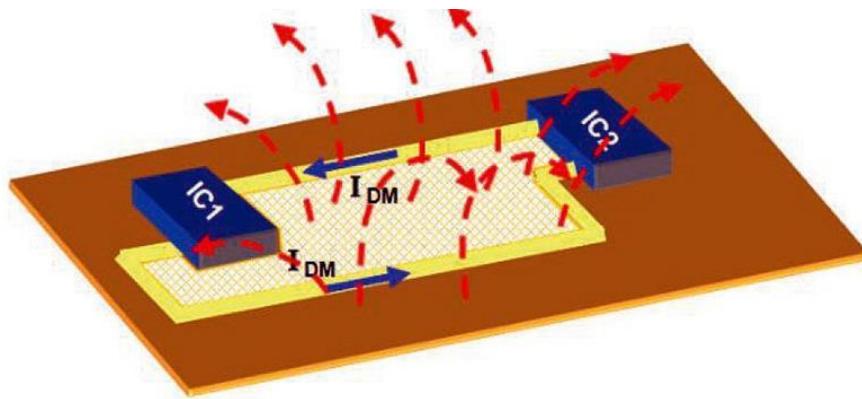


Suggested components to comply with EN 50155 Immunity

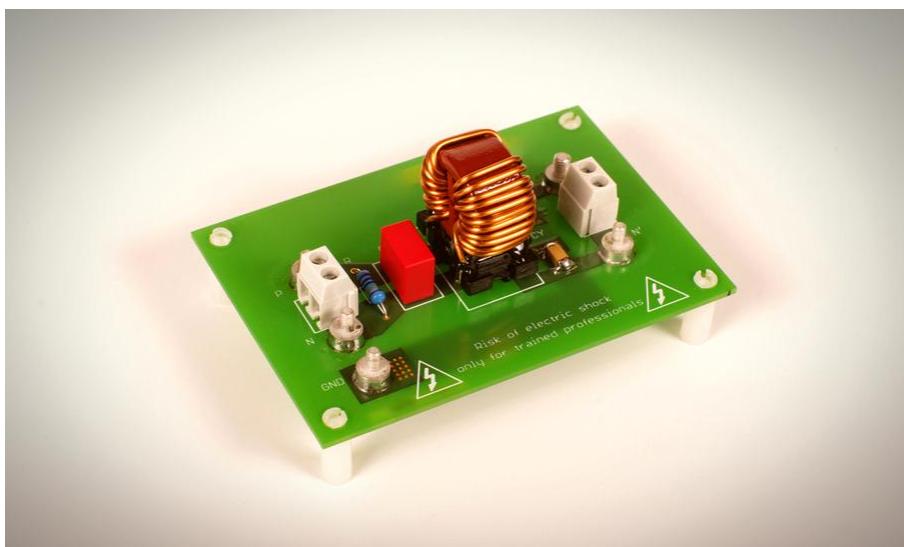
Model	Fuse	Diodes	C _{EMS}	TVS	C _{OUT}
TEN 40-24xxWIR	8 A Fast-Acting	200 V 1 - 1.5 × Fuse rating	Nippon chemi-con KY series 220 µF / 100 V	SMDJ58A 58 V / 3000 W peak pulse power	0.1 µF / 50 V X7R MLCC

Emi Filter Design With Tracopower Isolated Power Supply In Railway

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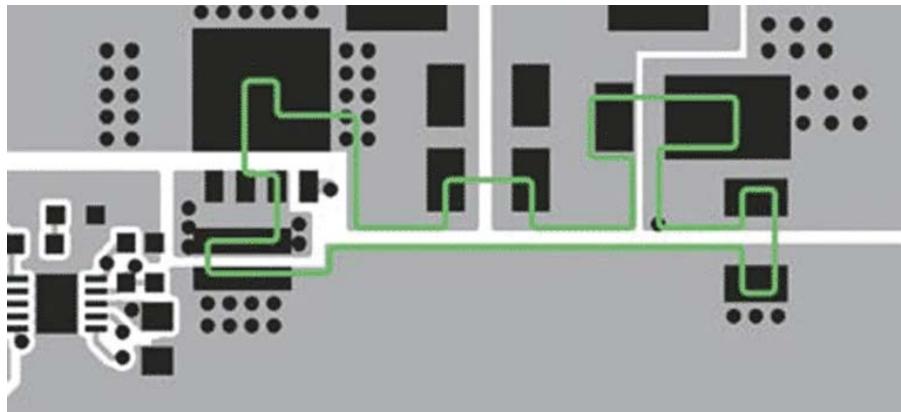
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Emc Basics And Practical Pcb Design Tips

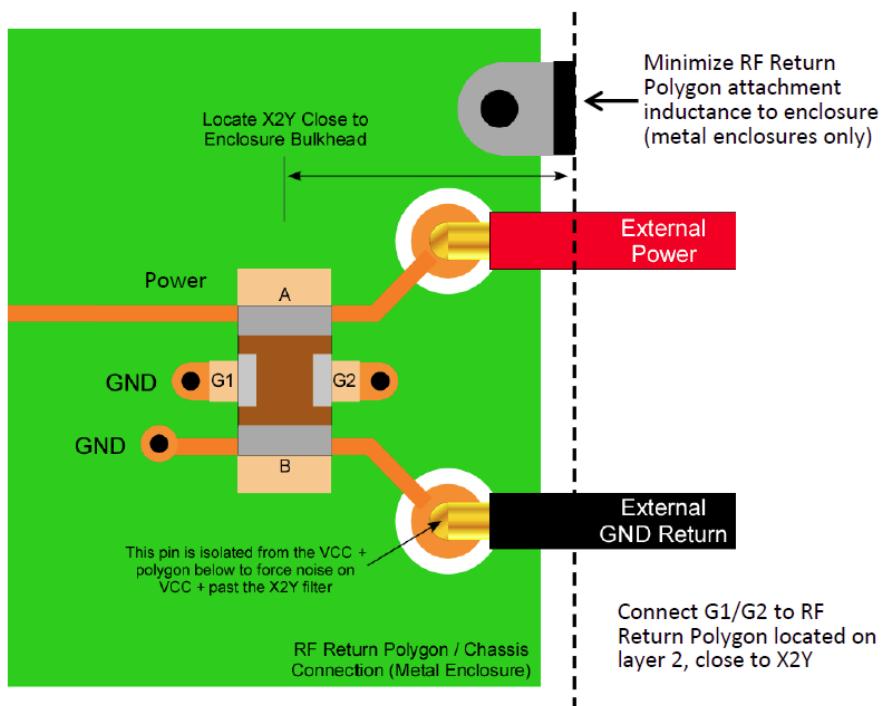


Suppress Noise And Emi In Your Pcb With The Right Analog Filter

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Layout Power Supply Boards To Minimize Emi Part 1 Power Electronics



1) Dual-Line EMI filtering of two conductor power feed.

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Emi Filter Basics

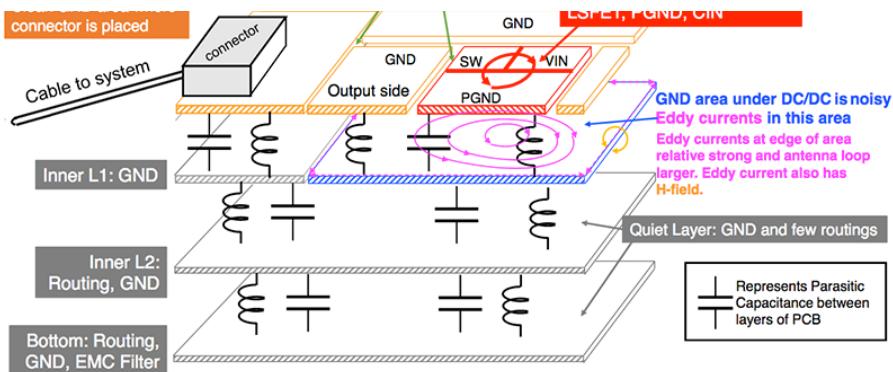
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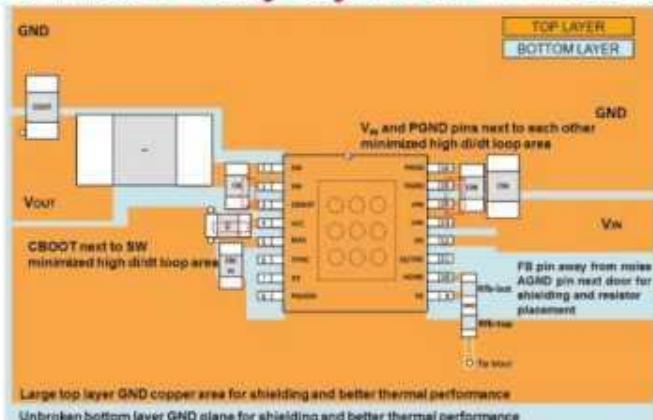
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LM43603 Pinout – Easy Layout for EMI Reduction

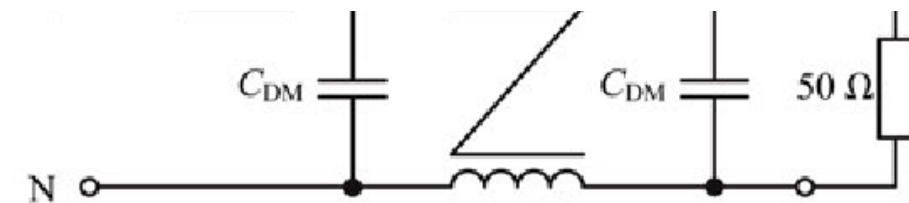


Layout Tips For Radiated Emi Reduction In Your Designs

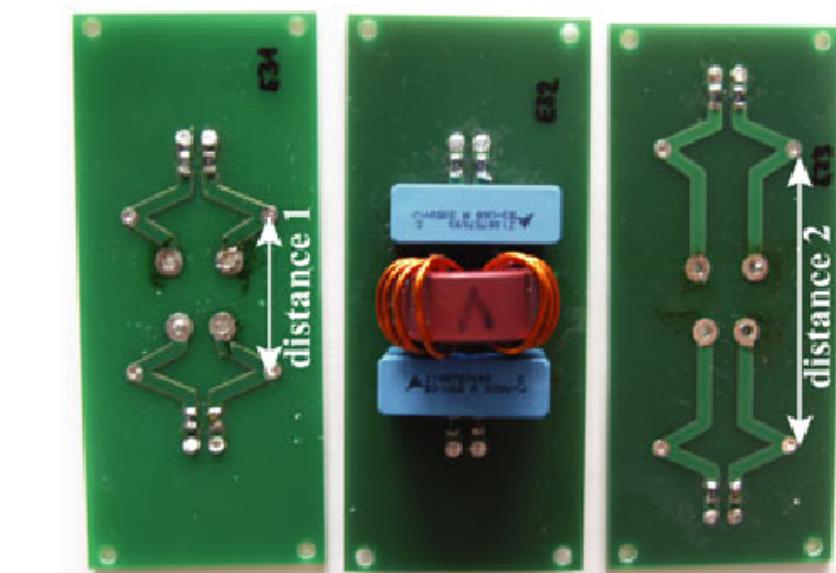
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<https://pcbways.blogspot.com/1970/01/emi-filter-pcb-layout.html>

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(a)



PCB layout I

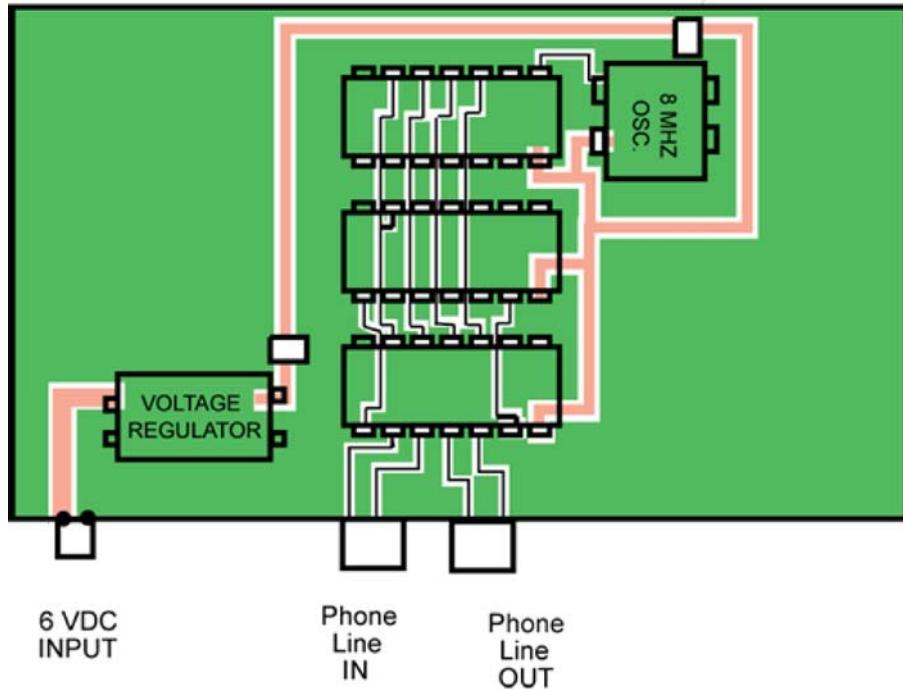
PCB layout II

(b)

PCB layout III

Figure 20 From 3 D Electromagnetic Modeling Of Parasitics
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Learnemc Pcb Layout

PCB Design for Real-World EMI Control

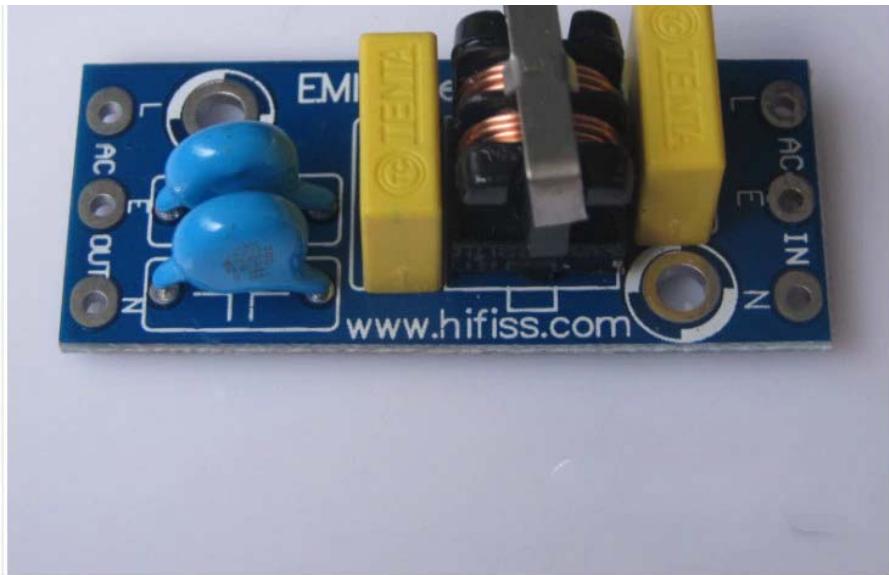
Bruce R. Archambeault



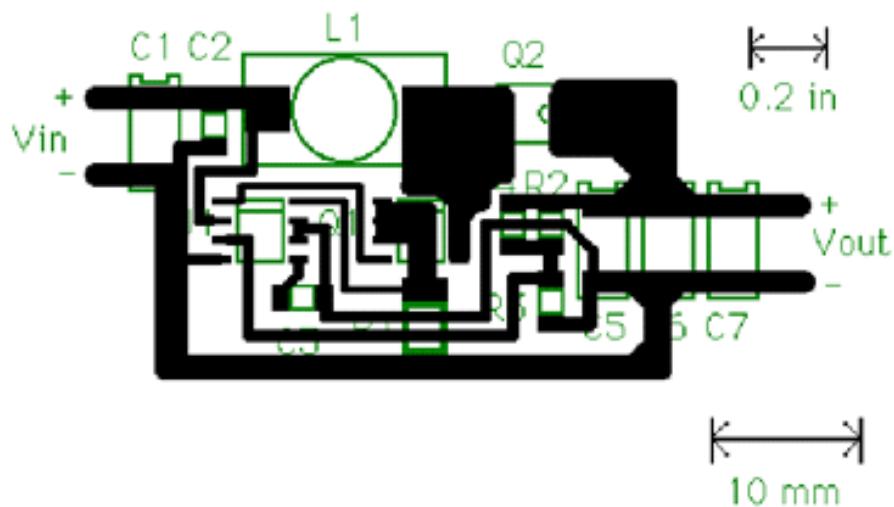
Contributions by James L. Browniak

Pcb Design For Real World Emi Control The Springer International

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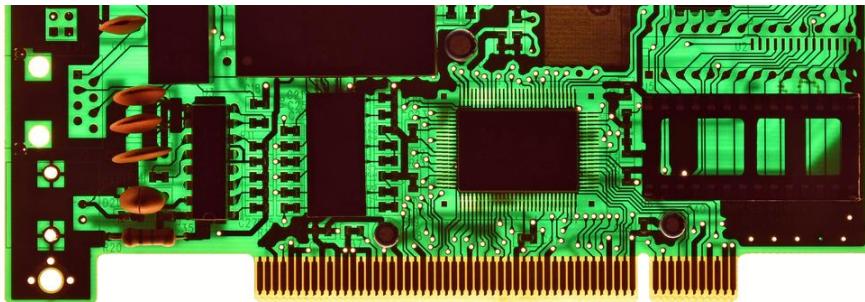
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Yimaker 5pcs Electromagnetic Interference Filters Emi Filter
Pcb

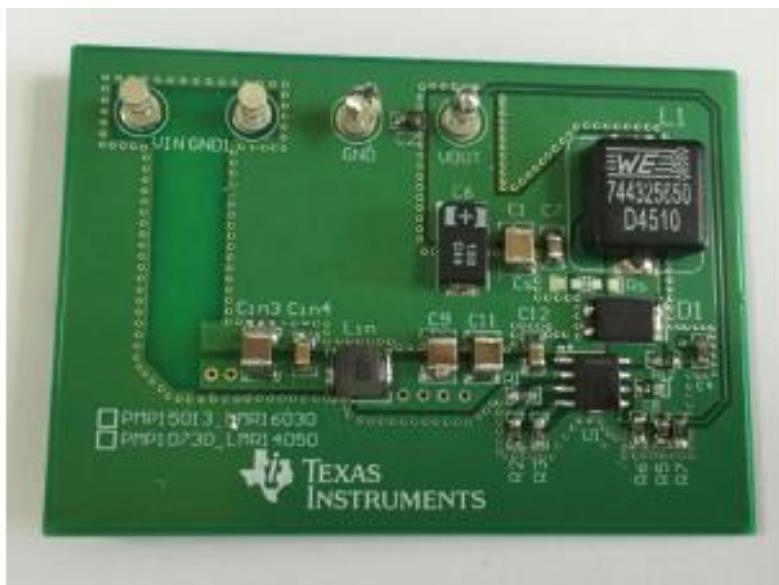


Good Physical Layout Takes Black Magic Out Of Power Supply
Design

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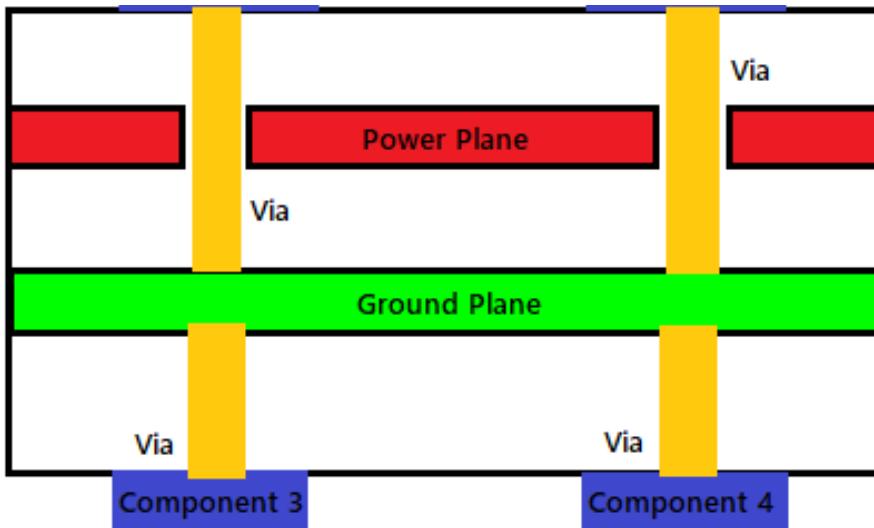
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7 Tips And Pcb Design Guidelines For Emi And Emc Sierra Circuits



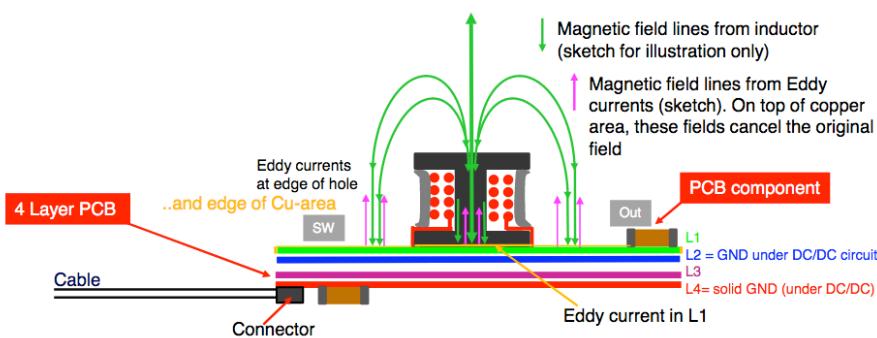
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Pcb Layout Design Tips Grounding Considerations

Onelectrontech



- + No AC magnetic field on bottom side of PCB
- + No magnetic coupling into bottom side components
- + Reduced Magnetic field coupling in cable
- + Reduced coupling in adjacent PCBs
- + AC Magnetic fields only on top side of PCB
- + inner layer should be clean

- Losses in Cu due to Eddy currents
- Increased parasitic capacity of coil
- Reduced effective inductance
- Eddy currents under coil in L1 and at edge of Cu-area

- Bottom side of PCB CLEAN
- EMC filter can be placed effectively here

Pcb For Low Emi Dc Dc Converters Working Design Ele Times

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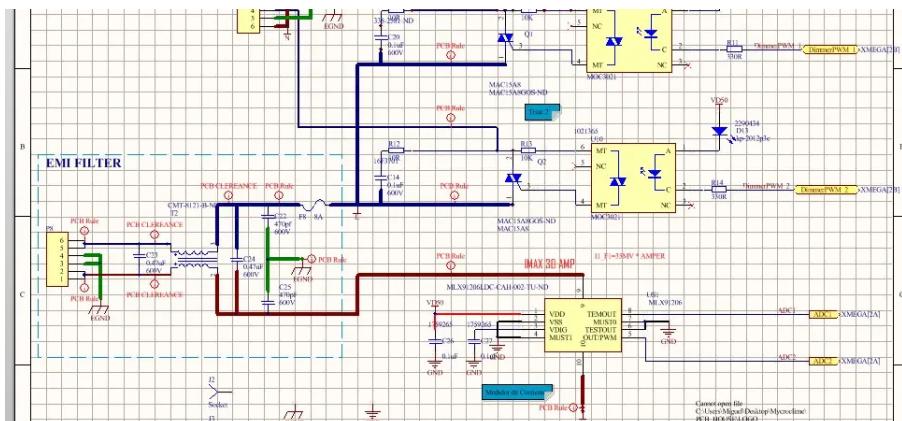
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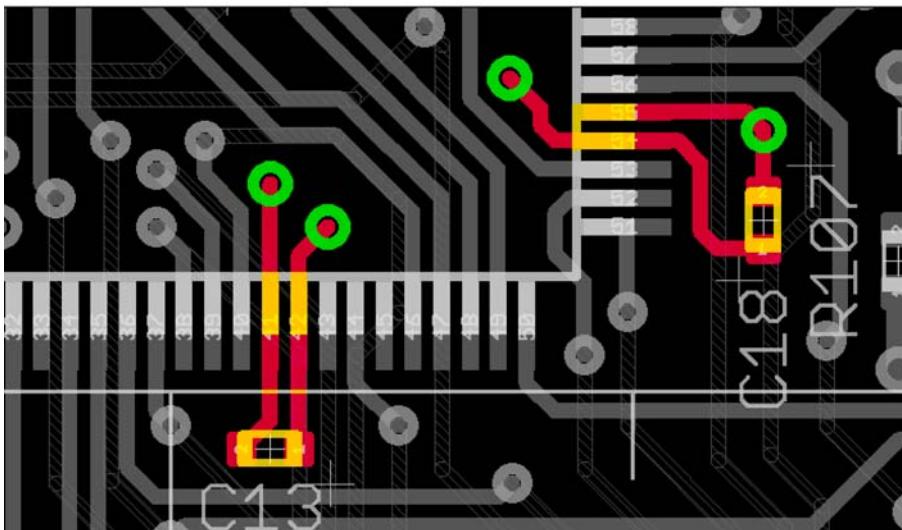
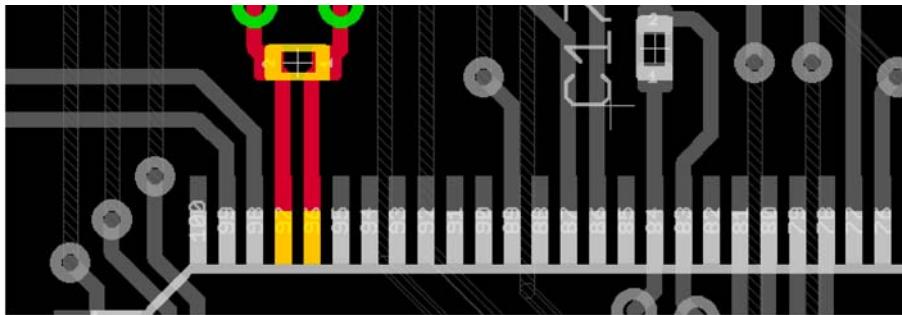
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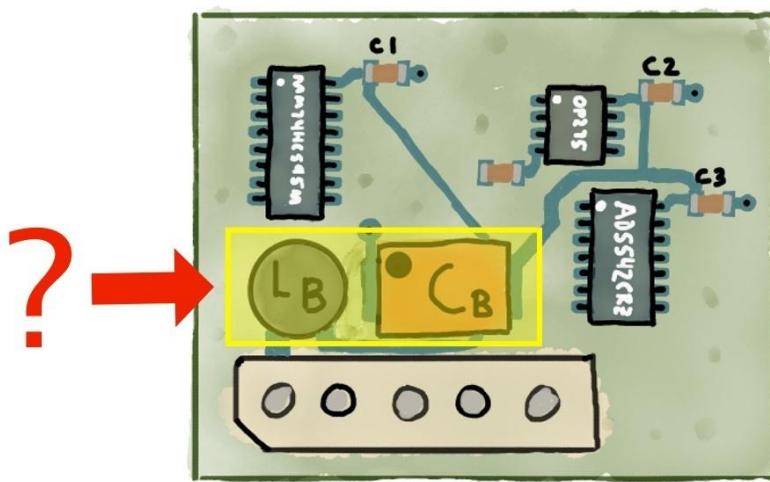


Pcb Layout For Emc Power Supply Design Tutorial Section 3 1

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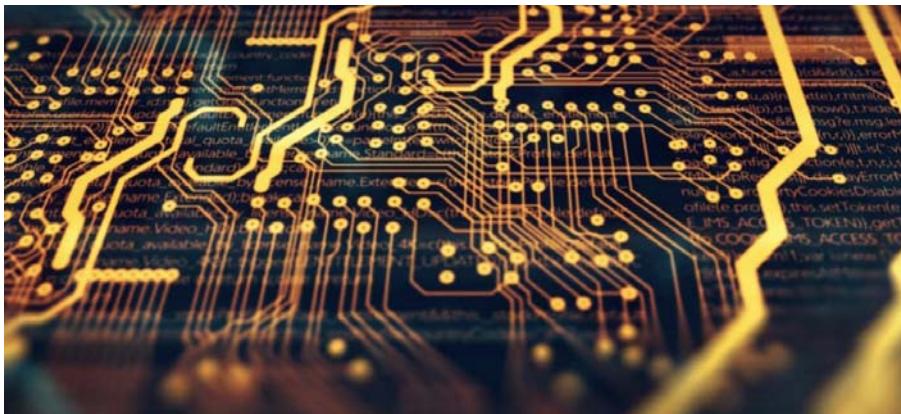
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Decoupling Caps Pcb Layout Electrical Engineering Stack Exchange



Power Supply Filter Design For Pcb Tempo Automation

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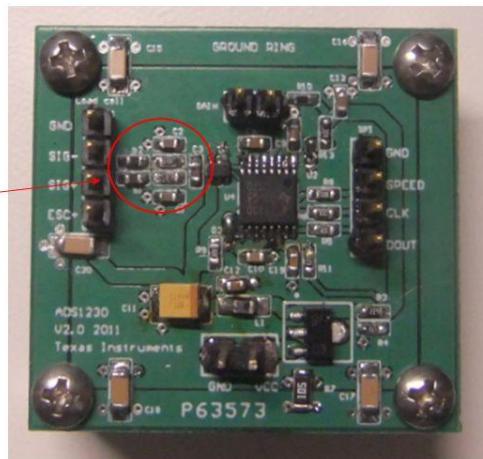
Cmos Is Different Pcb Design For Both Low Noise And Low
Emi



PCB Layout (SMD)

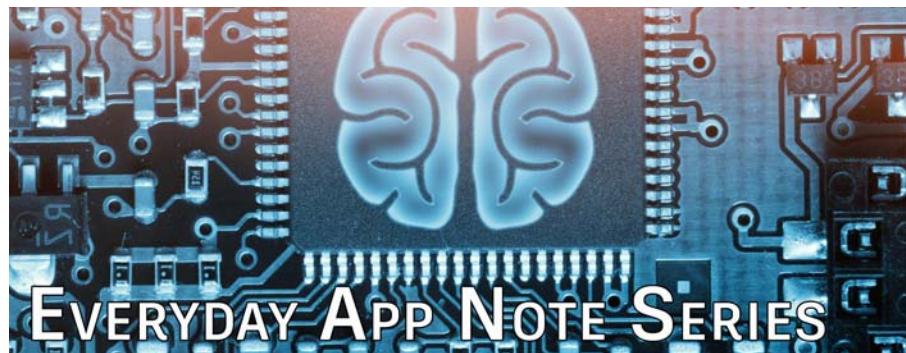
- Ground Plane on Bottom-side

Filter:
 $R=1\text{Kohm}$, $C_3=2.2\text{ uf}$, $C_1, C_2=0.22\text{uf}$,
2 Beads



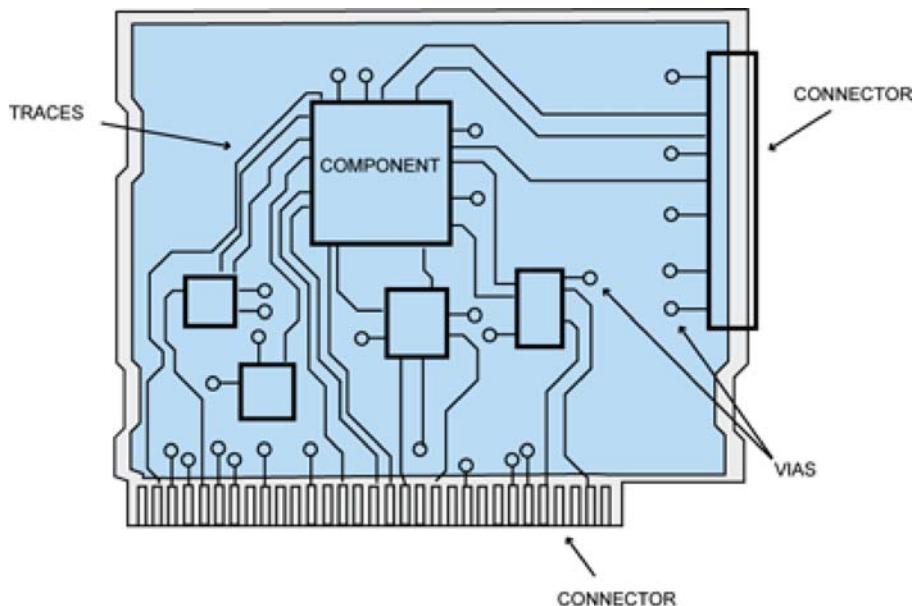
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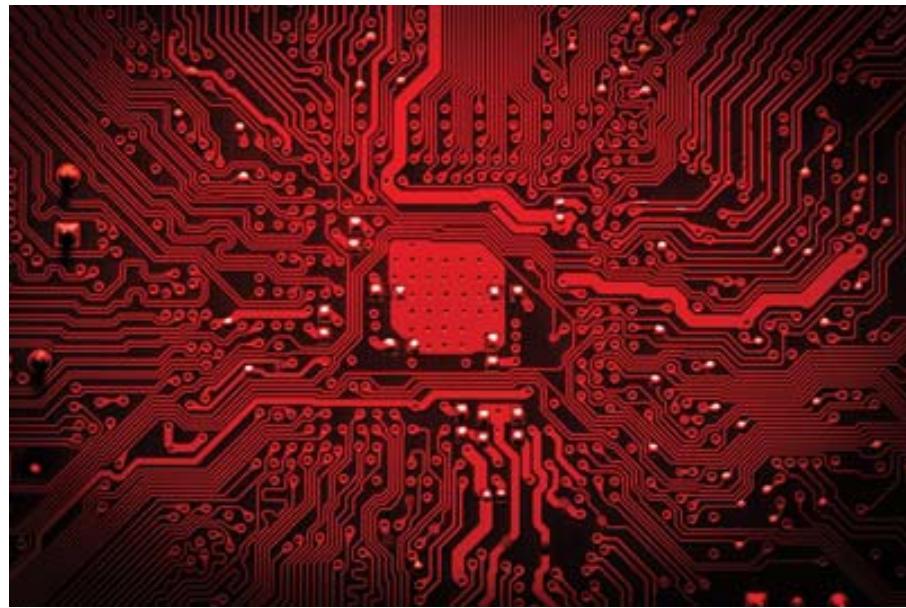
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Emi Filter Design



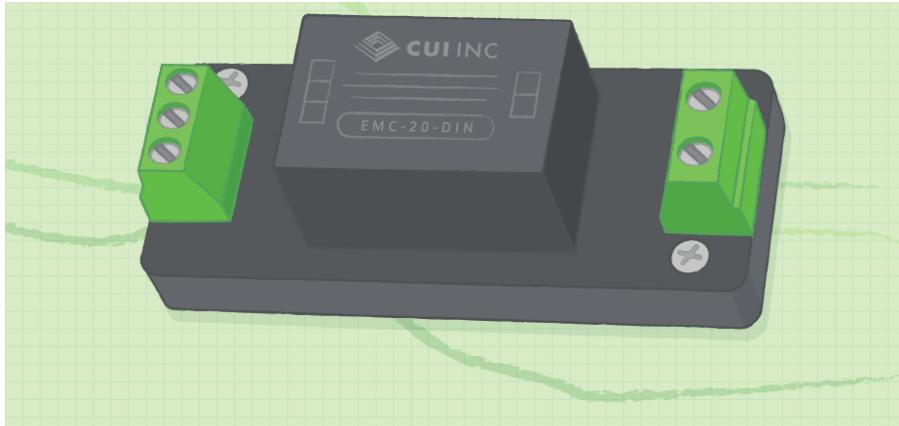
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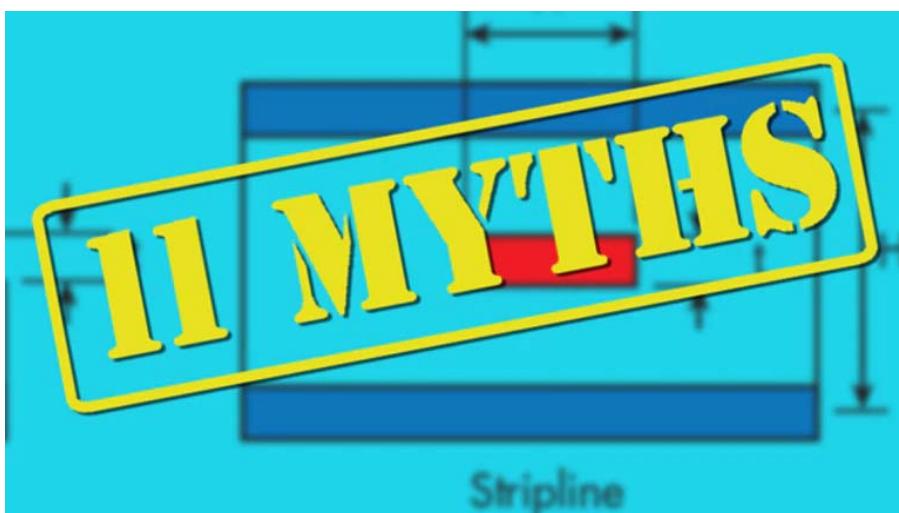


Emi And Signal Integrity How To Address Both In Pcb Design In

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How To Select An Emi Power Filter Cui Inc

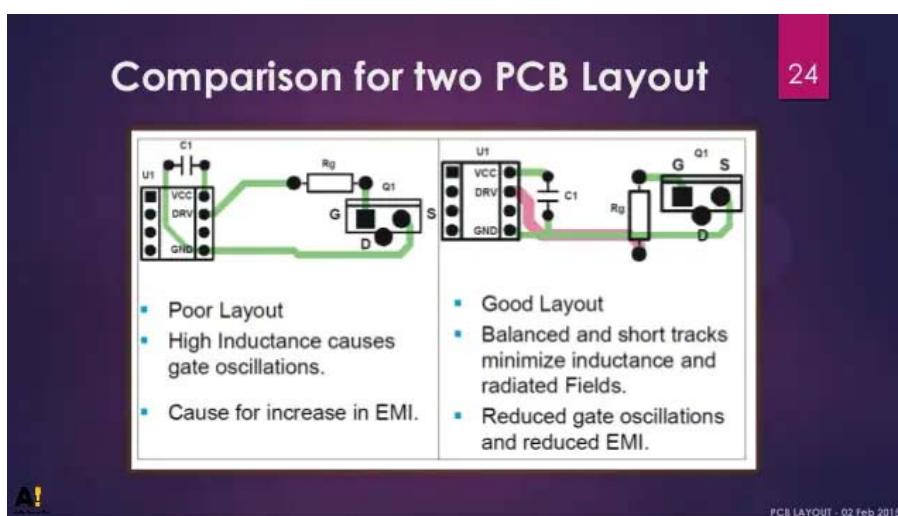


11 Myths About Emi Emc Electronic Design

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12v 1a Smps Power Supply Circuit Design On Pcb



Pcb Layout

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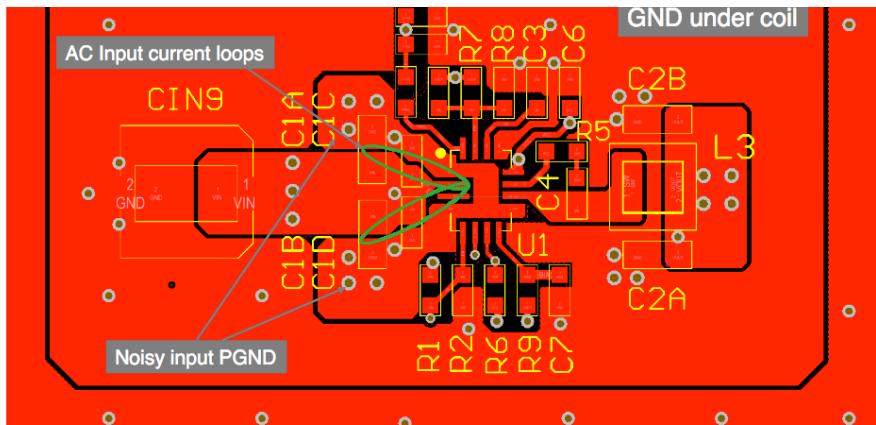
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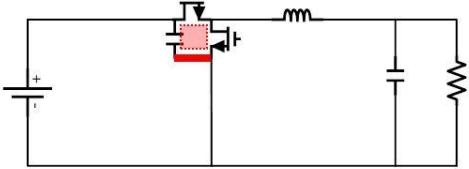
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EMI Mitigation by PCB Layout

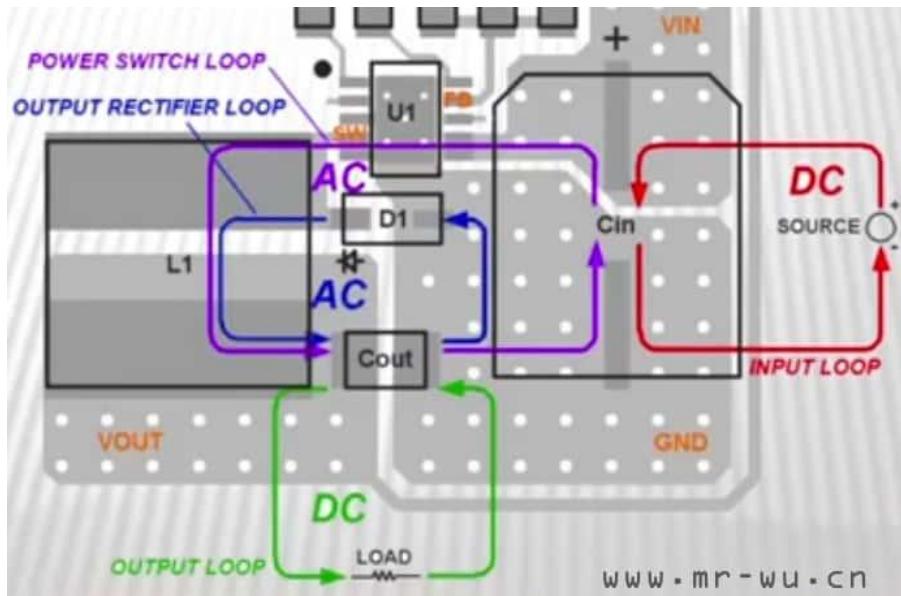
Critical Path Area Reduction		Grounding
High di/dt Caps	<ul style="list-style-type: none"> • BUCK Example 	
SW Node	<ul style="list-style-type: none"> • Bypass Caps in High di/dt loop should be placed as close as possible to the switching components 	
FETs & Driver	<ul style="list-style-type: none"> • Low side FET SOURCE should be connected as close as possible to the input capacitor • Apply to critical paths in other SMPS topologies 	

25


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Switching Power Supply Design Emi Reduction Ppt Download

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"X2Y® EMI Filter Evaluation & PCB Design Guidelines"

By Steve Cole – X2Y Product Manager
Johanson Dielectrics, Inc.

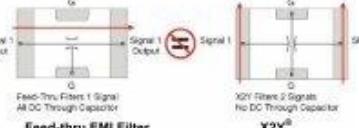
X2Y® Capacitors are capable of extraordinary EMI Filtering performance when effectively applied to the PCB. Understanding X2Y® primary advantages, different connection options, and following a few basic guidelines will help achieve successful lab evaluation and optimal production designs. This guide is focused on PCB EMI and RFI filtering however many of the same principals apply to DC Motor Filtering and IC Power Bypassing. For additional information on those topics please refer to "X2Y_DC_Motor_Filtering_Basics" and "X2Y_Power_Bypass_Mounting".

X2Y IN A NUTSHELL (Basic Theory)

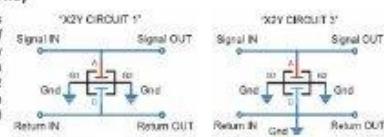
X2Y is an ultra-low inductance 3-node capacitor circuit consisting of two balanced Y capacitors of equal value. This configuration enables filtering of two signal lines (one positive AND negative power lines) simultaneously. A special electrode design provides broadband filtering characteristics for both differential and common-mode noise signals into the GHz band. EMI Immunity and Radiated Emissions performance far exceeds that of standard ceramic MLCs and multi-component filters. X2Y's low inductance maintains insertion loss over a wide frequency band, not just a narrow bandwidth around the capacitor SRF. This means that for a given capacitance value and corresponding pass band f_c , X2Y's deliver far better high frequency filtering than standard MLCs.

**IDENTITY CRISIS (X2Y vs. Feed-Thru Filter)**

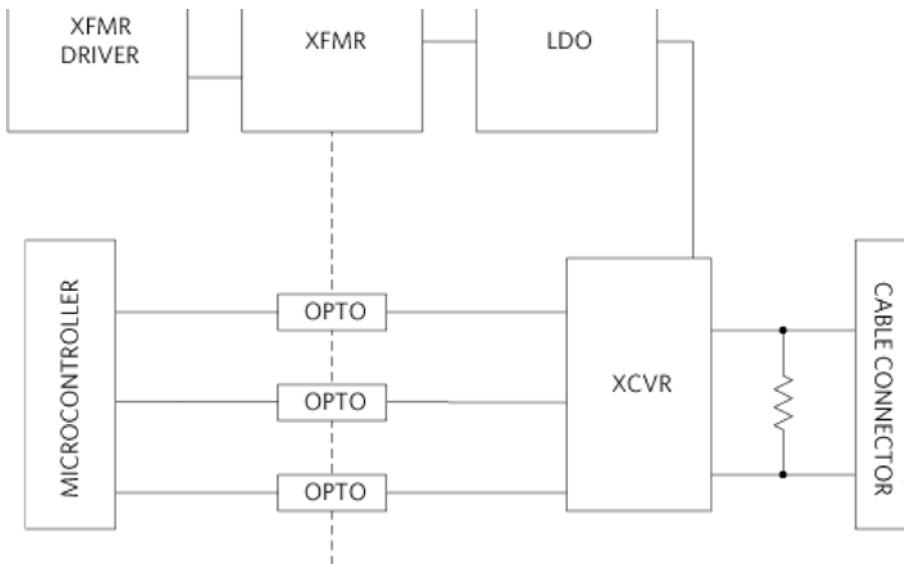
Externally an X2Y® closely resembles a chip feed-thru EMI filter but has major internal, schematic, and performance differences. A feed-thru capacitor drives one filtered signal through the capacitor along the long component axis and must handle both DC current and AC noise currents. X2Y® capacitors filter two signal lines simultaneously shunting only noise. Since no DC currents flow through the X2Y®, there is no DC current limitation. (In EMI applications AC noise currents are orders of magnitude smaller than DC currents.)

**HIT THE GROUND RUNNING (X2Y® Connection Options)**

X2Y® capacitors require a low inductance, dual ground connection as seen in "Circuit 1." Chassis or system ground is preferred, but if unavailable, an isolated or "floating" ground may be used very effectively. Because the filtered noise currents are small, adding a copper flood layer in the PCB and connecting it with vias to G1 & G2 create an image plane. Circuit 3 may be used in applications where a signal line is common with system ground. Comparative radiated emissions testing shows nearly the same level of effectiveness.

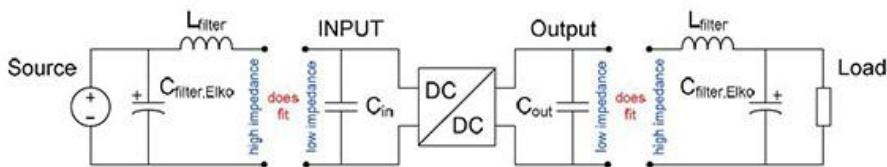


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How To Design And Layout An Emi Optimized Pcb For The
Maxm22511

$$L_{\text{filter}} = \frac{1}{(2 \cdot \pi \cdot 0,1 \cdot f_{\text{sw}})^2 \cdot C_{\text{filter}}}$$



Impact Of The Layout Components And Filters On The Emc Of
Modern

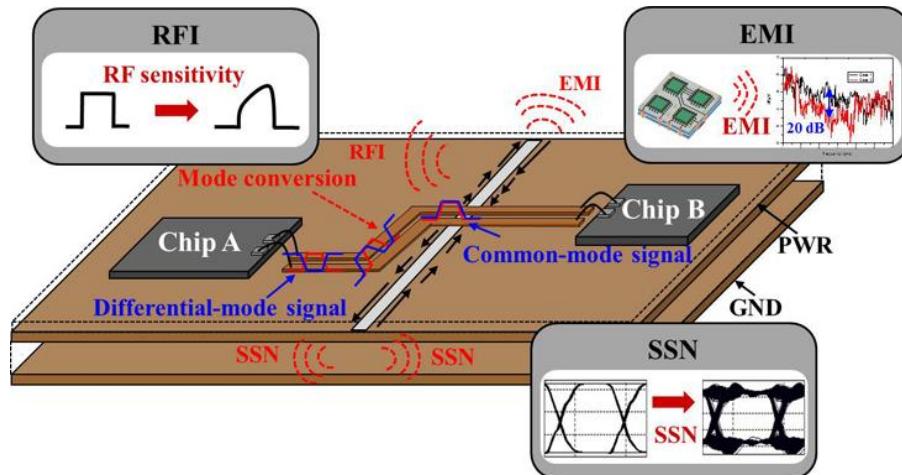


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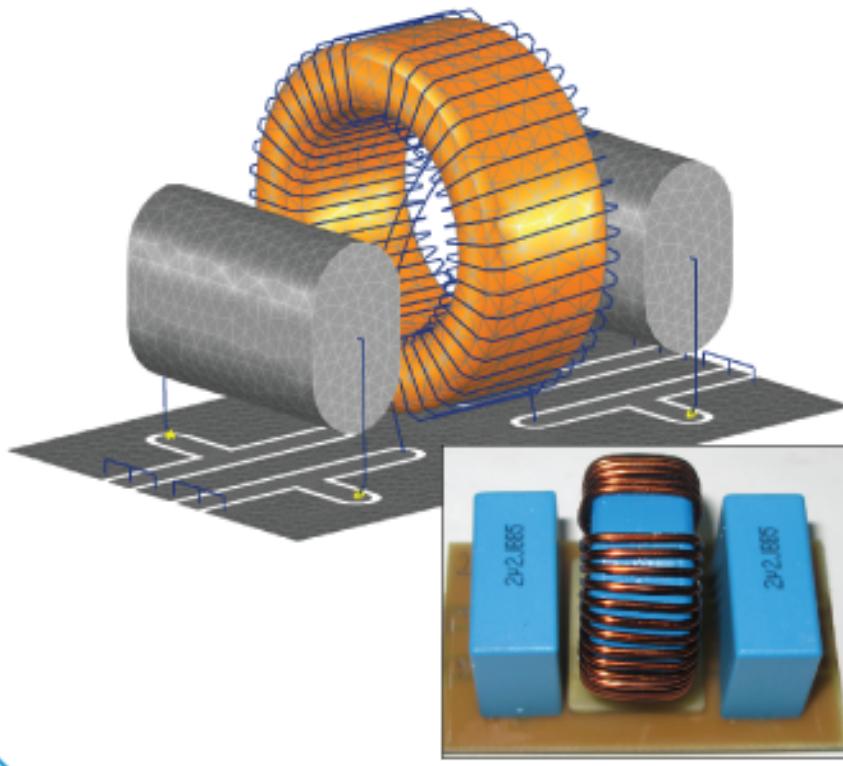
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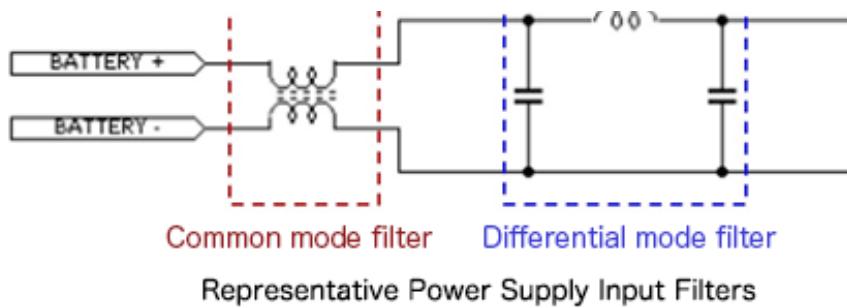
Simulation Model and Measurement Sample
of LC Filter with Vertical Alignment of CM Choke



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Input Filters For Switching Power Supplies Basic Knowledge



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Chip Common Mode Filter Array Emi Filter Manufacturers Emi

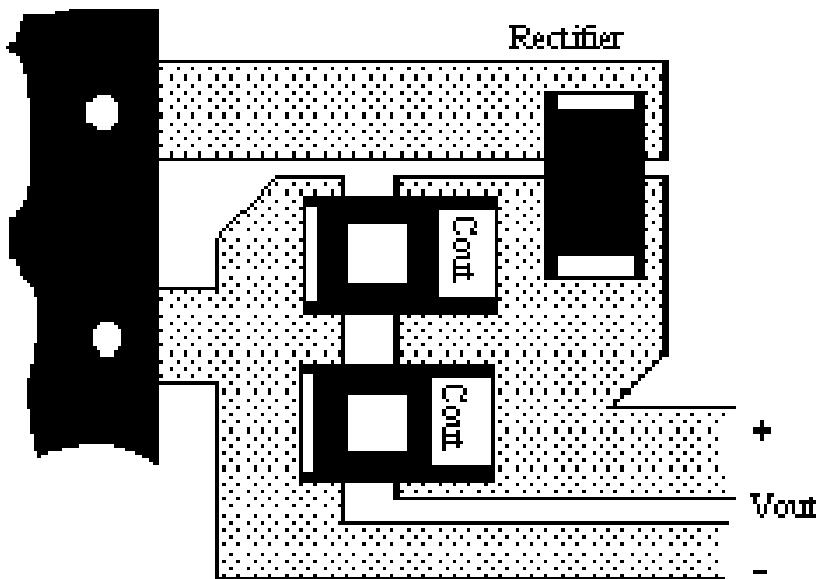
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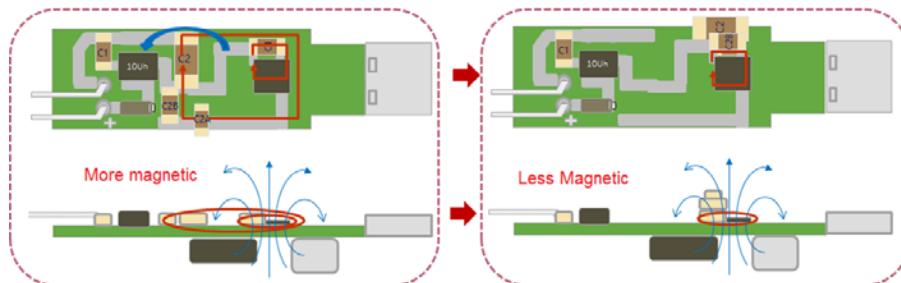
Step By Step Example For Practical Pcb Design Power Supply



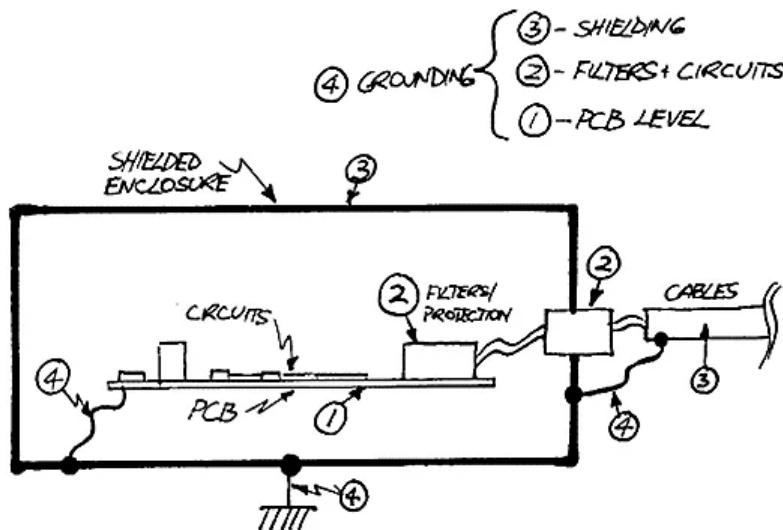
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Good Physical Layout Takes Black Magic Out Of Power Supply Design



Optimizing Emi In Switching Regulators For Consumer And Rf



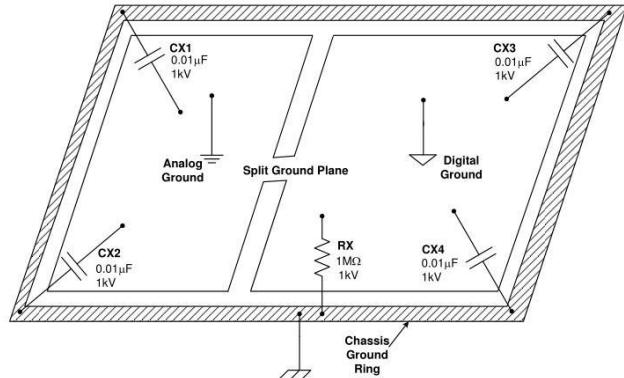
AREAS OR 'LEVELS' OF EMC ENGINEERING APPLICATION

Practical Shielding Emc EMI Noise Reduction Earthing And

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- A chassis “ground ring” --additional EMI/RFI Filter components



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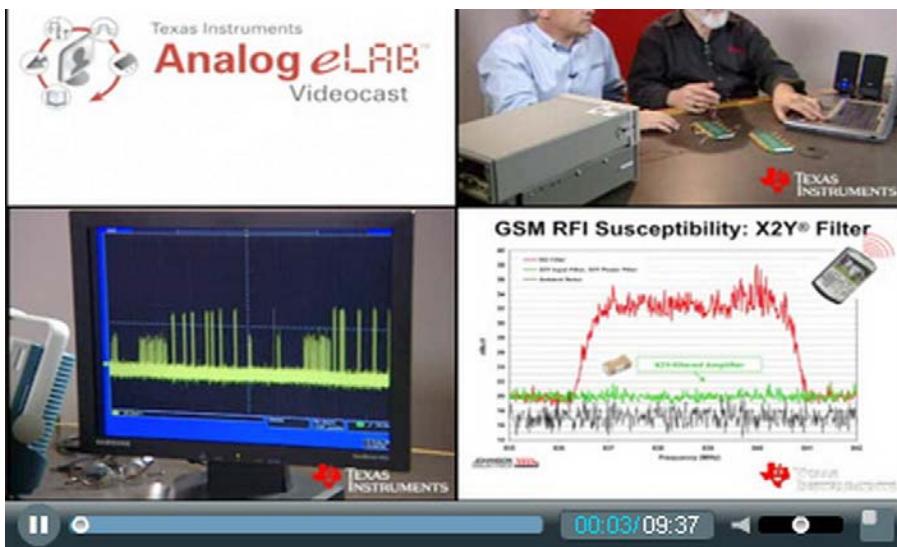


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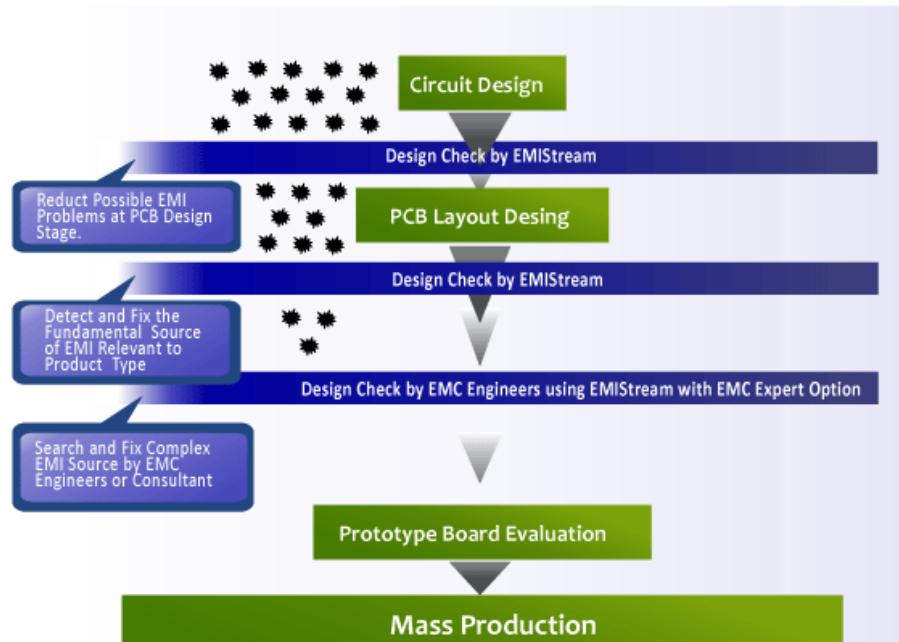
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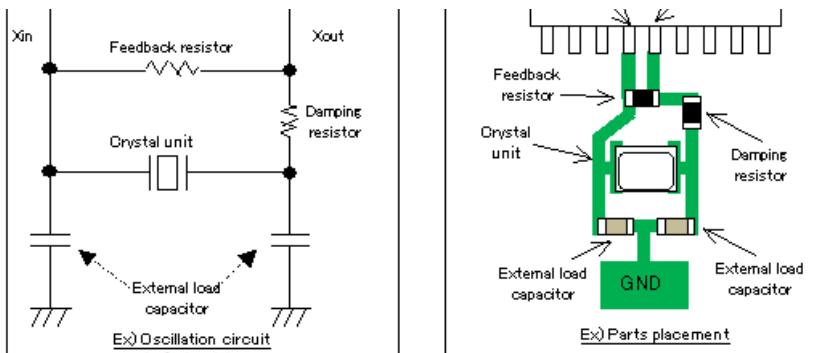
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X2y Attenuators Emi Filtering

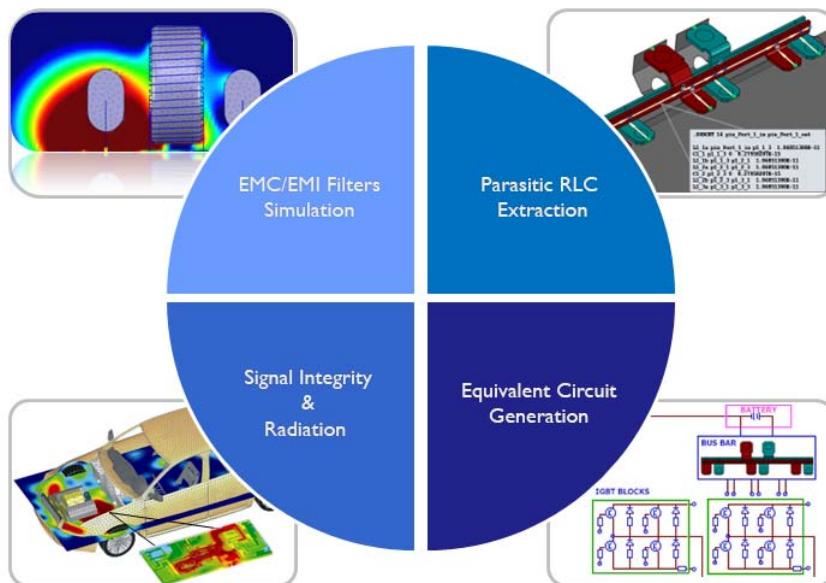


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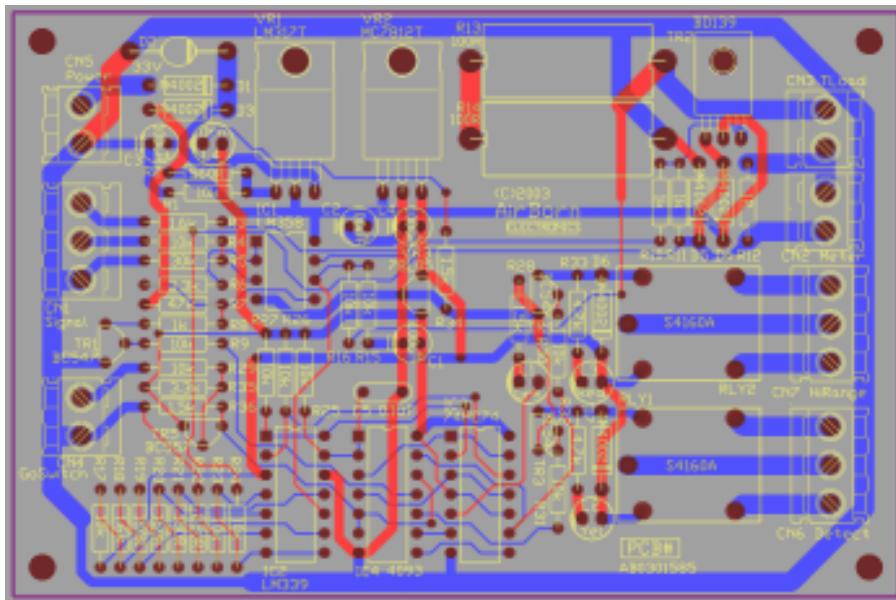
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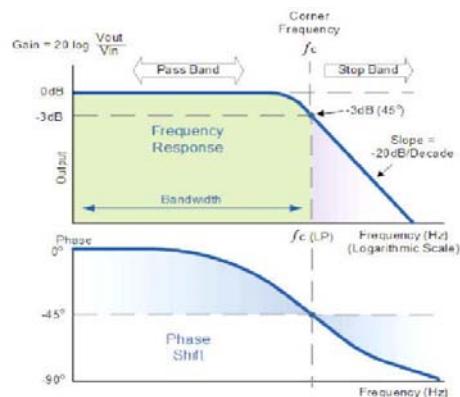


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M Fiam Filter Input Attenuator Module Mil Cots Vicor Corporation

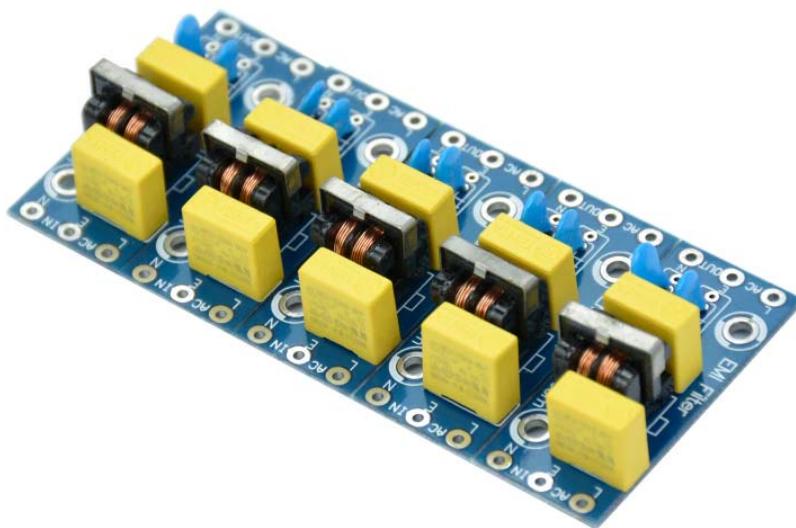


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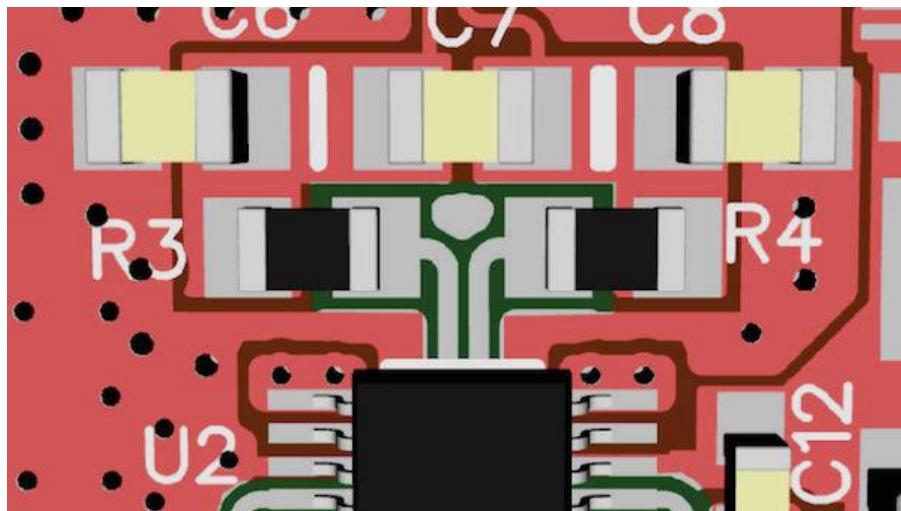
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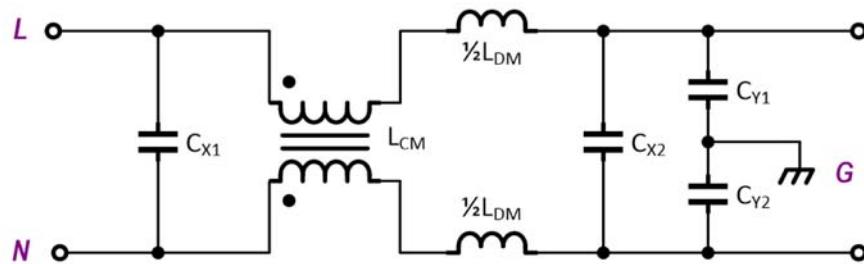
Be Careful With Input Output Feedback In Filters Passive



Yimaker 5pcs Electromagnetic Interference Filters Emi Filter
Pcb



How To Turn A Schematic Into A Pcb Layout Pcb Design For A Custom



Conducted Emi Reduction By Means Of Hybrid Common Chokes Richtek

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Schaffner PCB Filter FN 409



Schaffner IEC Inlet Filter FN 9222



Schaffner Chassis Mount Filter FN 2410

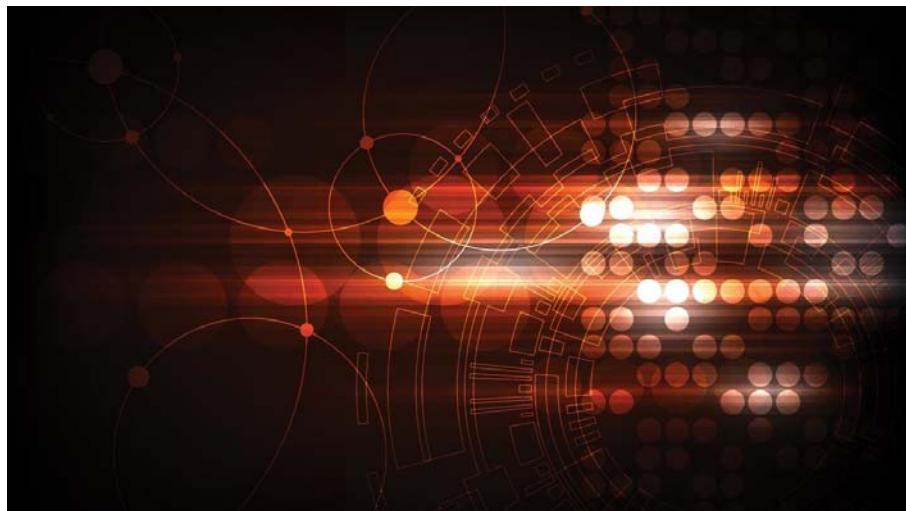


Schaffner Three-Phase Filter FN 3270



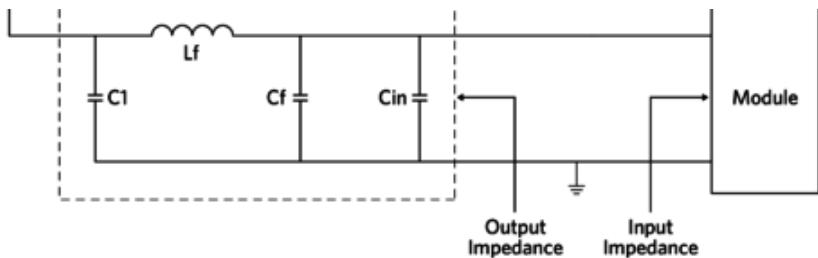
Schaffner Feedthrough Filter FN 7611

Emi Filter Design

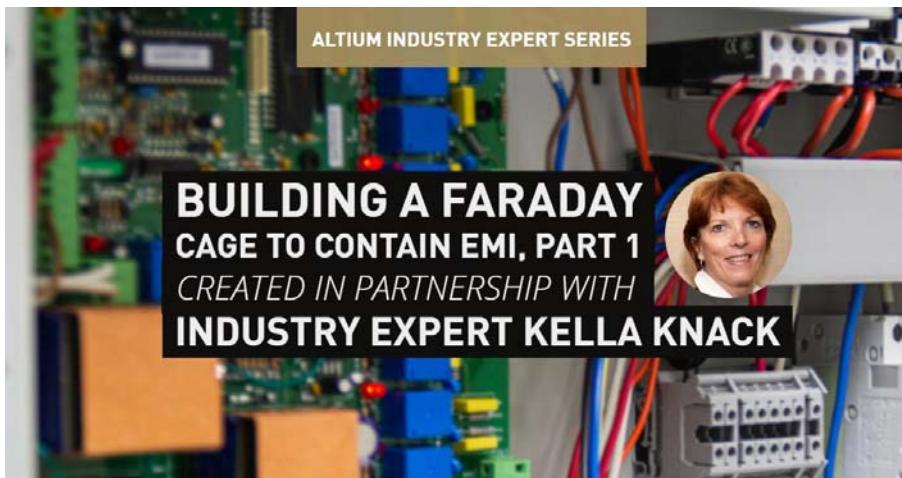


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Emi Achieving Cispr 22 Compliant Power Solution Maxim Integrated



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*Application Report*

SNVA755-June 2016

Simple Success with Conducted EMI and Radiated EMI for LMR160X0

Vincent Zhang

ABSTRACT

Electromagnetic Interference (EMI) is an unwanted effect between two electrical systems as a result of either electromagnetic radiation or electromagnetic conduction. EMI is the major adverse effect caused by the application of switch-mode power supplies (SMPS). In switching power supplies, EMI noise is unavoidable due to the switching actions of the semiconductor devices and resulting discontinuous currents. EMI control is one of the more difficult challenges in SMPS design, beyond functional issues, robustness, cost, thermal and space constraints.

First, this application note introduces the overview of LMR160X0 family products and conducted EMI knowledge. Second, step by step differential filter parameters design will be introduced to suppress conducted EMI noise. Third, a reference PCB layout based on LMR160X0 is presented. Finally, both conducted EMI and radiated EMI test with and without input filter were provided and compared to verify the theories. This approach also could be applied to the LMR140X0 family.

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Simple Success With Conducted Emi And

Conducted EMI Issues in a 600-W Single-Phase Boost PFC Design

Leopoldo Rossetto, *Member, IEEE*, Simone Buso, *Member, IEEE*, and Giorgio Spiazzoli, *Member, IEEE*

Abstract—This paper presents the results of experimental activity concerned with the development of a 600-W boost power-factor corrector (PFC) complying with the EMC standards for conducted EMI in the 150-kHz–30-MHz range. In order to accomplish this task, different circuit design and layout solutions are taken into account and their effect on the conducted EMI behavior of the converter is experimentally evaluated. Common-mode and differential-mode switching noise, together with input filters' design and topology and with the printed circuit board layout (in terms of track length and spacing, ground and shielding planes, etc.) are the key aspects which have been considered. In particular, the paper reports the conducted EMI measurements for different filter capacitor placements and values, for different power switch drive circuits, together with several other provisions which have turned out to be decisive in the reduction of the generated EMI.

Index Terms—Conducted EMI, power-factor-correction rectifier, printed circuit board layout.

I. INTRODUCTION

THE employment of boost power-factor correctors (PFCs) in order to comply with the IEC 1000-3-2 low-frequency EMC standard [1]–[3] is becoming more and more ordinary in a large variety of industrial applications of switch-mode power supplies (SMPSs). This solution, however, increases the conducted interference generation of the power supply in the high-frequency range. As a consequence, while the low-frequency harmonic content of the current driven from the utility grid is normally well controlled and compliant with the aforementioned IEC standard, the high-frequency currents generated by the converter on the grid may be beyond the corresponding standard limits [4]–[7]. To avoid this, it is very important to properly design the EMI filters and the circuit layout so as to minimize the effects of the switching converter on the line pollution. This paper discusses the design of a 600-W boost PFC complying with the EMC standards for conducted EMI in the 150-kHz–30-MHz range [8]. Different circuit design and layout solutions are taken into account and their effect on the conducted EMI behavior of the converter is experimentally evaluated. Common-mode and differential-mode switching noise, together with input filters' design and topology and with

the printed circuit board (PCB) layout (in terms of track length and spacing, ground and shielding planes, etc.) are the key aspects which have been considered. In particular, the paper reports the conducted EMI measurements for different filter capacitor placements and values, different power switch drive circuits, together with several other provisions, which have turned out to be decisive in reducing the conducted EMI level of the converter [9]. By means of this design example, which employs two-layer PCB technology, the paper also shows that the application of the theoretically derivable EMC basic design rules, which, in principle, should guarantee the limitation of the EMI in a switching power converter, may, in some cases, become partially ineffective because of second-order effects (e.g., resonances, component parasitics, connections). The experimental results illustrate these unexpected outcomes and the validity of the adopted provisions which allow one to design a fully compliant power supply.

II. BASIC SCHEME OF THE CONVERTER

Fig. 1 shows the basic scheme of the considered boost PFC. The ratings of the converter are reported in Table I. These represent the typical characteristics of a PFC designed for a large variety of applications (e.g., telecom applications). A conventional and simple design procedure can be adopted to derive the necessary passive components' values, required to guarantee the continuous conduction mode of operation for the converter practically during the whole line period and a suitable output voltage ripple level. Also, the selection of the required switch and diode is almost straightforward, given the current and voltage stresses, which are easily determined analyzing the converter's typical waveforms. The resulting list of adopted components is reported in Table II.

III. CONSIDERATIONS ON THE POWER STAGE DESIGN

The considered topology is simple and well known [10]–[13]. However, when it comes to EMI control, it is necessary to adopt particular care in the definition of the layout of the power stage [14]–[18].

Of course, the main sources of EM noise can be easily identified in the power switch and diode. The reduction of the wire lengths for the current return paths and for the high dV/dt circuit branches, together with the reduction of the areas embraced by high dI/dt loops, as shown in Fig. 2, appear to be fundamental provisions. It is, therefore, fundamental that the area between the power switch and the two high-frequency bypass capacitors, which are used to drain the current pulses generated during the

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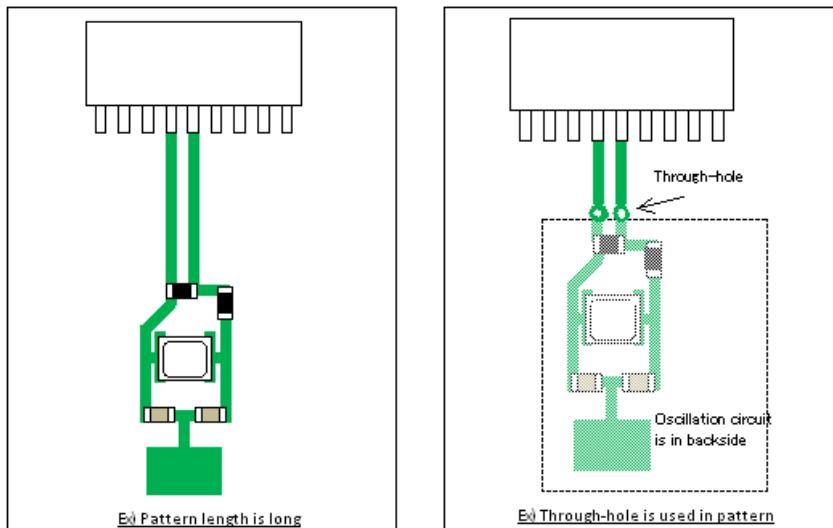
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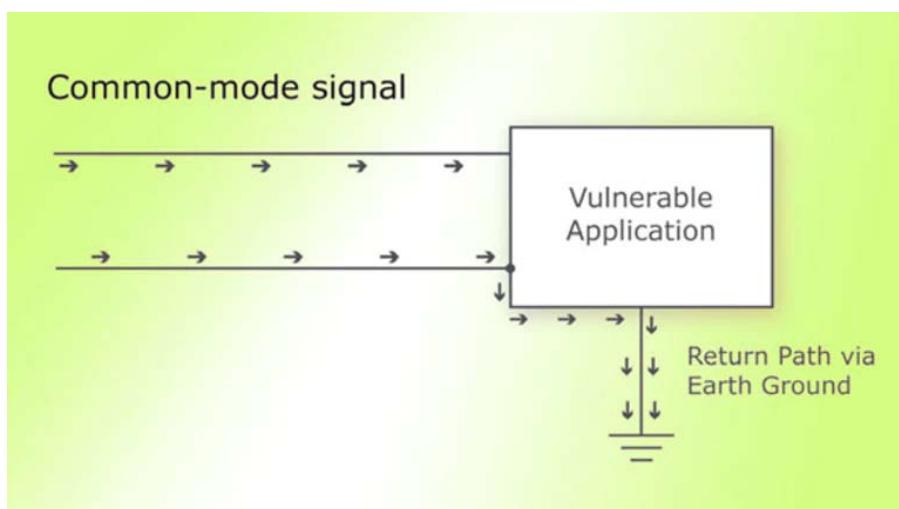
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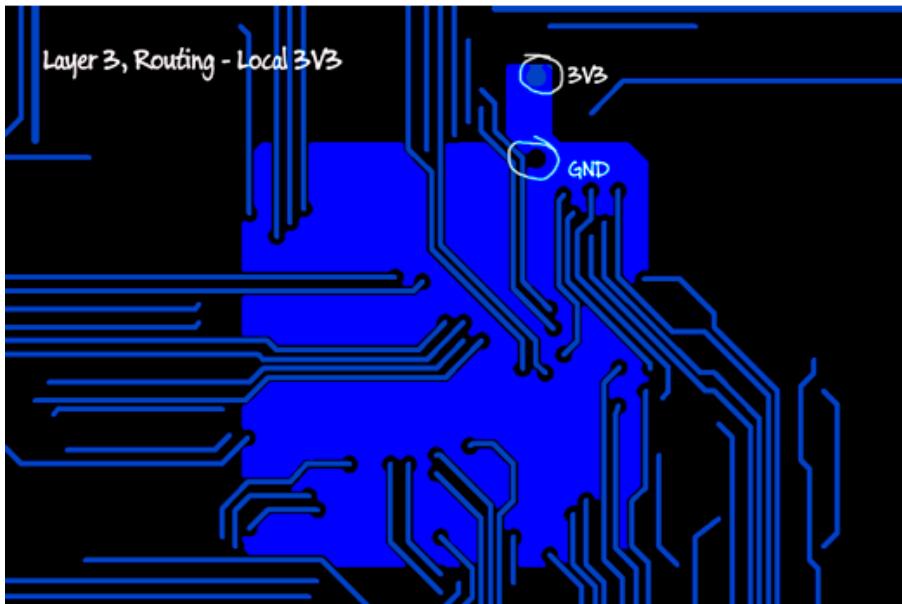
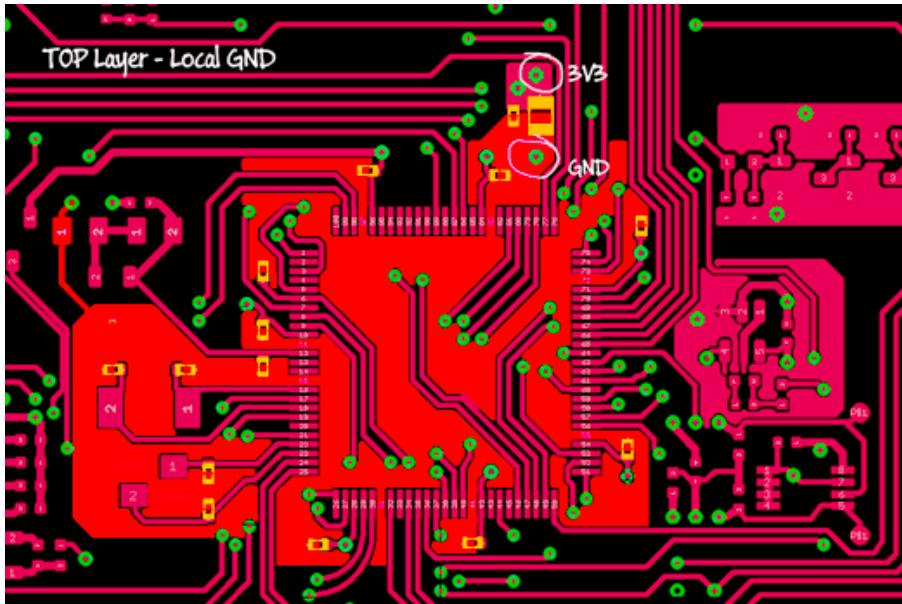


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