Appendix C

Case studies

This section discusses a few real-life case studies of electronic product design, each of which illustrates some aspects of the EMC design principles discussed earlier in this book. While based on real products, the details have, of course, been dis-identified.

C.1 Cockpit display

A common EMC problem arises with large (say, 10" or 12") LCD displays driven with standard VGA or high resolution video. The product featured here was cost limited and was required to be daylight visible, but also had to meet stringent radiated RF emission limits, not just the standard Class B ITE limits of EN 55022. Because of the first two requirements, the third couldn't be met by a shielded window – it would have been too expensive and would have attenuated the light transmission too much. So although a shielded enclosure was acceptable and necessary for the electronics, which included a 100MHz processor, the display had to be outside the shield. The challenge was to find a way of doing this without compromising the emissions limits.

Emissions from these displays tend to be dominated by the pixel clock and its harmonics, and come via two coupling routes: direct radiation from the glass face, and common mode radiation from the whole assembly. The face radiation is entirely controlled by the LCD manufacturer – it depends on the transition speed of the edges created by the transistor matrix drivers, and the physical configuration of the conductor pattern on the glass – so the first task was to evaluate the emissions from several manufacturers' samples in a standardized jig. From this exercise a couple of front-runners emerged, the final choice being made on other features.

The emissions limits in this application were not uniform across the frequency range – they were tighter in those frequency bands that included receivers in close proximity to the display unit. The second task then was to identify clock frequencies whose fundamental and harmonics would fall within these bands and try to eliminate them from the design. This eventually meant outlawing certain display modes, and subtly tweaking others to shift their pixel clocks slightly up or down. Choosing a display and a graphics controller with maximum flexibility in acceptable clock frequencies aids this process; it's not too difficult if the only display is the one on-board, but harder if you have to feed the video out in parallel to an external monitor so that it must meet the specified VESA standards. As well as the display frequencies, the processor clock frequencies had to be vetted and tweaked in the same way.

The major design work involved the creation of a structure that would minimize the common mode radiation. This radiation is due to noise voltages appearing on the metal case of the LCD relative to the shield, which then emits in much the same way as a patch, or transmission line, antenna. These voltages are amenable to control by careful design. This took a number of forms, referring to Figure C.1:

- the shielded enclosure for the rest of the electronics was maintained along the back of the module, behind the front face of the unit but enclosing the electronics;
- the separation distance between the back of the LCD module and the outside of the shield was kept to a minimum: radiating efficiency is directly proportional to this distance;
- the back of the LCD module was grounded at multiple points to the shield, using conductive gasket material (in some applications the LCD is at circuit 0V, and this has to be separate at DC from the shield. This means that capacitance has to be inserted in series with the grounding points, which is tricky but possible);
- most importantly, the signal cable to the LCD should not introduce common mode noise along its length, despite carrying the pixel clock and the video data, and despite the LCD connector being poorly specified for screening. Wire bundles are ruled out. The best solution is a flexi connection between the driver on the electronics PCB and an adapter to plug into the LCD module (see section 13.1.8.3). The double-sided flexi has one side devoted to a ground plane that is taken through multiple pins to the driver PCB 0V, which is locally grounded to the shield to minimize the noise voltage difference between the ground plane and the shield. The adapter converts the flexi to the LCD connector, and takes a separate low-inductance connection to the LCD case.

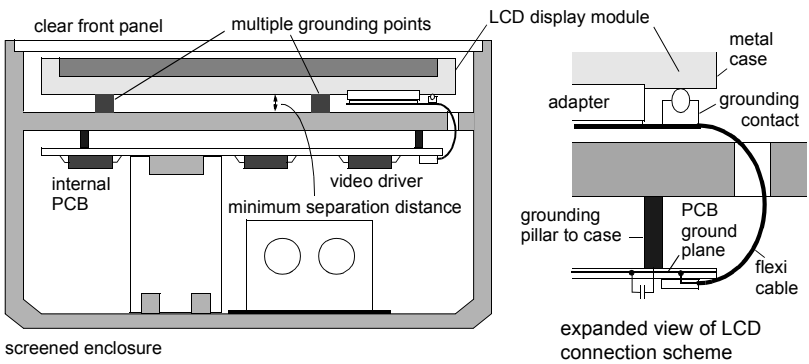

Figure C.1 General assembly of cockpit display

C.2 Liquid tank sensor

A manufacturer of instrumentation, which included temperature and liquid level sensing transmitters, discovered a market in the marine sector; but this entailed hardening the electronics against RF to a level of 20V/m whereas before it only needed 3V/m. The least possible and lowest cost change to the design was desired. The original unit had a remote thermistor and level sensing potentiometer, connected by unscreened wires to terminal blocks on the two-layer electronics PCB in a plastic box (Figure C.2).

The unit was connected to the system control by a long distance 4–20mA link, again over unscreened wires.

To improve the hardening, a classical interface filtering plus shielding approach was needed. The PCB design was expanded to four layers and a 0V plane was implemented. The terminal blocks remained on the upper side of the board and the circuit was enhanced with filter capacitors to the ground plane on all terminal pins, and capacitors applied for bandwidth limitation at selected points in the analogue circuit – generally at the inputs to the operational amplifiers. Finally, the interior of the box was specified to be sprayed with low-cost conductive paint (at the time, nickel), and the edge of the board was fitted with a series of surface mount spring fingers to make contact between the 0V plane and the conductive coating. After all this, there was no susceptibility discernible up to at least 30V/m. The manufacturer later found that he could omit the nickel shielding on the plastic box, and the unit was still adequately immune to 20V/m due solely to the PCB-level changes.

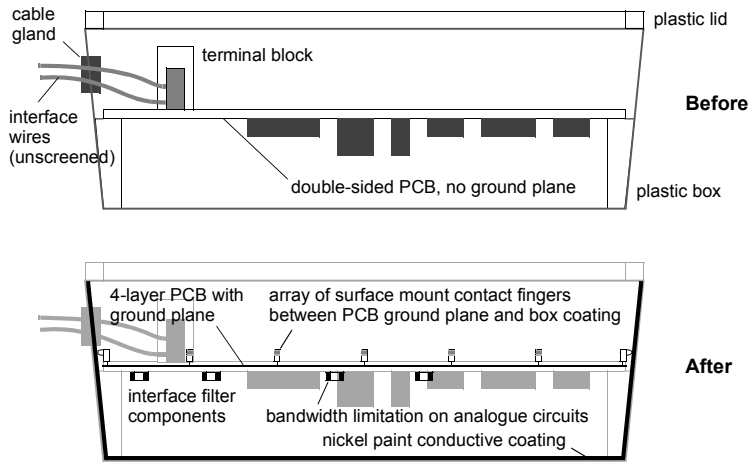

Figure C.2 Changes to the level/temperature transmitter

C.3 The problem with wall-warts

Because many small products – particularly IT and consumer products – use low levels of power at DC (typically 12V) but need to be supplied at mains voltage, a large market has grown up for external DC switchmode power supplies which plug directly into the mains outlet (hence, "wall-wart") and which supply power to the application unit via a short two-wire low-voltage cable. The product manufacturer normally buys these in from an external supplier, often in the Far East, and has no control over the design of the supply itself. The wall-wart supplier will typically offer a product which does in fact meet at least the conducted emissions requirements of the IT standard EN 55022, and this might appear to be enough for the product manufacturer who will package it with their own unit. But the supplier of such a "system" must ensure that the whole system complies when it is used in a typical configuration, and the connection of a DC load to the output of the wall-wart may change its emissions profile, as well as adding its own

emissions coupled back down the DC power lead.

This isn't the only problem. EN 55022 Edition 3 includes requirements for conducted emissions tests on telecom ports. In these tests, you again bump into the problem of conducted emissions generated by the wall-wart power supply. To understand the mechanism, we must delve more deeply into the equivalent circuit.

C.3.1 The conducted emissions equivalent circuit

The equivalent circuit of the conducted emissions test, both for mains port and telecom port emissions, can be drawn as shown in Figure C.3. For the sake of this discussion, emissions generated within the unit – for illustration, call it a LAN switch – itself are ignored. The wall-wart is Safety Class 2, i.e. it has no connection to its safety earth pin.

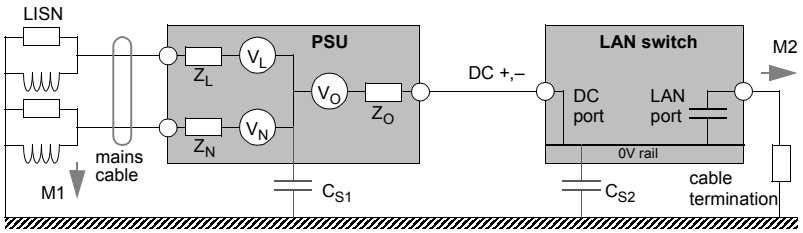

Figure C.3 Equivalent circuit for conducted emissions

The interference is generated within the wall-wart PSU due to its switching power supply and is represented by V_N and V_L, feeding the live and neutral mains connections, and V_O, feeding the DC output connection. Each has a source impedance Z_L, Z_N or Z_O, and each is referred to the enclosure and thence by stray coupling to the ground reference plane of the test. These impedances are likely to be predominantly capacitive and affected by layout aspects and transformer construction of the power supply. (If the enclosure is entirely plastic then the capacitive interconnections become more complicated, but do not vanish.)

It is vital to appreciate that the components at the output of the wall-wart form the *common mode* circuit; that is, neither the DC link voltage nor the LAN output signals are of any interest to us and are not shown, only the entire cable, considered as a whole, is shown. It doesn't actually matter whether or not the LAN switch itself is powered up and operating for this circuit and its effects to be valid.

V_O can only be referred to the case of the unit, to which V_N and V_L are also referred. This means that V_O will be added to the measurement M1 of both V_L and V_N, but its level will depend on the ratio of the various impedances in the power supply circuit (Z_O, Z_L, Z_N and the LISN impedance) as well as the impedance of whatever the output is connected to. In the circuit this is determined by the connection of the LAN switch's signal port. Clearly then, mains emissions in this case will be affected by the test set-up at the output of the wall-wart.

If there were no output connection, V_O would be irrelevant, and the levels measured at live and neutral would be entirely determined by V_L, V_N, their source impedances and the LISN impedance. But with the LAN switch connected, V_O is added to each of V_N and V_L from a source impedance determined at low frequency by the series combination of Z_O, the LAN port output impedance and the cable termination impedance. From this you can see that if the LAN cable termination is a high impedance

(say, a short unscreened cable to a laptop) the effect of adding V_O will be negligible; but if it is low, such as a desktop PC fed via a screened cable, V_O will be significant. So it would be quite reasonable for two different but equally valid test set-ups to produce markedly different results.

The situation is complicated at high frequencies by the presence of stray capacitances C_{S1} and C_{S2}, and also by the inductive impedance of the DC power cable and the signal cable. These can often combine with other strays into a series resonant circuit that gives a characteristic hump in switchmode emissions around 10–25MHz (see Figure 12.18 on page 311), but usually they are less significant below, say, 1MHz.

C.3.2 Telecom port emissions

The previous discussion has concerned mains conducted emissions, but Figure C.3 shows that similar issues apply to telecom port emissions, i.e. those measured in common mode on the LAN cable (M2). Although some such emissions will be generated within the LAN switch, particularly the common mode component of the LAN data, there will also be a significant component that is passed directly through the LAN switch from the wall-wart. Here, the worst case will be if the reference for V_O is in fact directly connected to earth (Safety Class 1 supplies). This allows the maximum current developed by V_O to flow through Z_O and out through the terminated LAN cable. Even if V_O is negligible, the mains sources V_L and V_N will also contribute to levels at the telecom port if the earth is removed.

C.3.3 Mitigation

Because all these emissions are propagated from the wall-wart to the LAN switch in common mode, any differential mode fixes such as capacitive filtering at the DC supply input of the LAN switch will be utterly useless. Indeed, this is a simple diagnostic technique: put a big capacitor, say 1μF, across + and – at the input to the LAN switch and check to see if it makes any difference. If it doesn't, and if you have confirmed that the emissions frequency spectrum implicates the wall-wart, this is conclusive evidence of the coupling path.

In this case, shielding of the LAN switch or providing a metal chassis or improving its PCB layout will also all be useless, since the interference is being passed directly from DC input to LAN output.

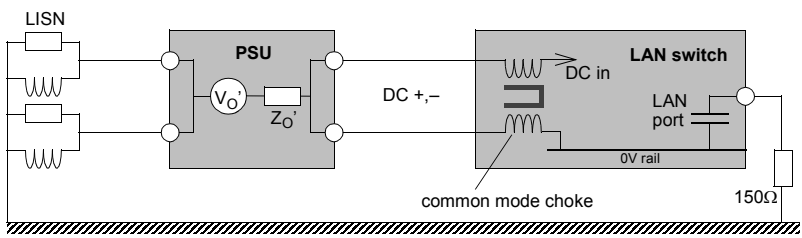

Figure C.4 Inserting a common mode choke

The first solution that will work is to put a common mode choke right at the DC input to the LAN switch (Figure C.4). The choke increases the impedance in series with Z_O' (the total common mode source impedance). This will reduce the disturbance currents flowing through the LAN cable in direct proportion to the difference in

impedances with and without the choke. Thus if the dominant impedances without the choke are (Z_O' + 150) ohms, and you need a 6dB improvement in emissions, the CM choke must also have an impedance of (Z_O' + 150) ohms at the appropriate frequency. This works well if Z_O' is relatively low and the frequencies are high; there are many small surface mount CM chokes for DC inputs that can give well over 1kΩ impedance. It also has the benefit of reducing the effect of any common mode emission sources within the LAN switch. If the frequency is down towards 150kHz though, and Z_O' is already high (implying that the wall-wart is acting more like a common mode current source), then you will need a potentially very large CM choke to have enough effect.

The next "solution" that will work is to reduce the impedance of the LAN switch itself to the measurement ground plane, by making a direct or indirect connection to it. If the unit were to have an earth point, then this would be directly connected to the ground plane and the majority of the power supply emissions would pass into the plane rather than through the LAN port. But how many such devices have an intentional earth connection?

You may, though, have the option of making additional connections to other ports. If these have a low-impedance connection to the LAN switch's 0V plane, and also a low impedance termination to the ground plane (or at least stabilized to 150 ohms, as with the LAN port) then they will also pass a proportion of the power supply emission currents to the plane (Figure C.5). The proportion will be directly related to the ratio of impedances at the various ports; if the impedance of one additional connected port is the same as that of the measured LAN port, then a reduction in the LAN port emissions of 6dB can be expected.

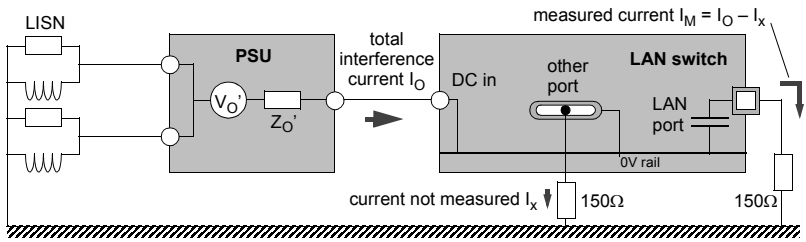

Figure C.5 Connections to other ports

Lastly, the best way of dealing with the whole problem is to specify the emissions of the wall-wart supply properly. Instead of leaving it to the wholly unsatisfactory and uncontrolled requirement that the wall-wart be CE Marked, place explicit specifications on both the input and output emissions levels. It will generally be sufficient to quote EN 55022 Class B levels for the mains conducted emissions, with the output terminated in a DC load equivalent to its maximum rated power and at the same time a common mode impedance of 150 ohms to the ground plane. The crucial extra requirement is that the DC output common mode voltage and/or current is also specified to EN 55022 Class B telecom port emission levels, under the same conditions. If the supplier can be contractually persuaded to meet these limits, then you have good confidence that any emission failures are due to your own product, not the wall-wart.

C.4 The dipole problem: a box in two halves

The example used here is a fingerprint analyser, but the principles apply to a wide range of products which are mechanically designed in the same way. The form of construction (Figure C.6) neatly illustrates a number of points.

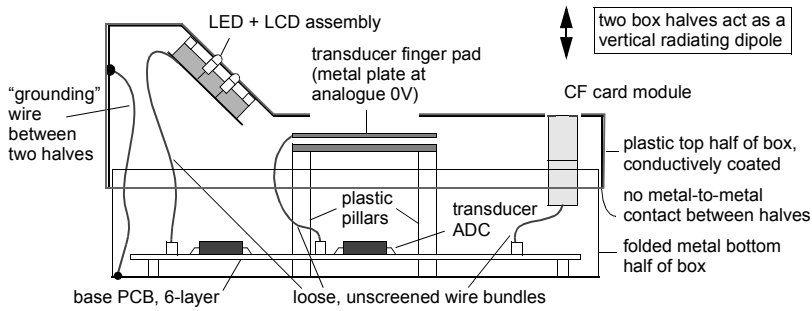

Figure C.6 Two half-boxes acting as a vertical dipole

This design had serious ESD susceptibilities as well as over-limit radiated emissions. It might also have suffered radiated RF susceptibilities, but nobody found this out because the test programme was stopped once the early problems were discovered.

The base (processor) board design was fundamentally sound, with both ground and power planes on a six-layer PCB. But the various peripherals, all mounted on the upper half of the box, fed down to several connectors on the base board through loose wire looms. Anticipating possible EMC problems, the manufacturer had elected to "shield" the box by conductively coating the inside of the top part, and had "grounded" the two halves together by a 15cm length of (admittedly green-and-yellow) wire.

The ESD susceptibilities manifested in three ways:

- air discharges to the LEDs and LCD bezel, both of which were accessible through the front panel, would immediately corrupt the LCD display and, after an indeterminate number, crash the processor;
- contact discharges to the finger pad would destroy the analogue-to-digital converter (ADC), sometimes immediately but always within a few discharges;
- air discharge to the edge of the Compact Flash (CF) card would corrupt the CF memory and crash the processor.

In addition, although the unit's radiated emissions were satisfactory under quiescent conditions, when the CF card was addressed (which happened frequently) they shot up above the limit. This problem was clearly due to the signals present on the card interface wires as it could be traced to the relevant clock frequencies, creating noise on the CF module which then coupled capacitively to the metallization on the top half of the box. Since the top and the bottom were only connected via a length of wire, the pair formed an effective radiating dipole antenna in the vertical plane. The wire's inductance merely re-tuned the antenna's worst-case resonance, it didn't reduce the radiating efficiency.

C.4.1 Mitigation

The various changes that were made to this design are shown in Figure C.7. To solve the radiated emissions problem, the most effective method was in fact to *eliminate* the top half of the shield, while "shielding" the cables to the CF module. The conductive coating was removed from the top plastic half of the case (which pleased the designer, since it was a noticeable cost reduction). The loose wire cable was enclosed in a metallized sheath bonded at one end to the 0V plane on the base board, and at the other to the case of the CF module; this reduced the common mode noise carried up to the CF module, and the lack of shielding on the top half meant that the radiating dipole effect was limited only to the module itself, not the whole case. It would have been possible to have left the top half shielded, with all the other measures to be described in place, and improved the bond between the top and bottom halves by using appropriate conductive fasteners and gaskets so as to reduce the dipole effect; but this would have been a lot more expensive and would have probably created further ESD problems.

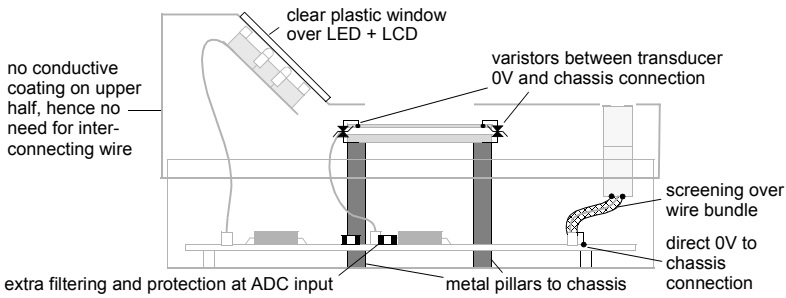

Figure C.7 Modifications to the box in two halves

A preferable way to have reduced the CF module noise would have been to redesign the cable connection to it for minimum transfer impedance, by using either multi-ground connections in a ribbon or a ground plane flexi. But this wasn't an option; shielding the cable assembly was. In other circumstances, the better options would be possible.

The effect of making this change to the cable was also to increase the ESD immunity of the CF module. It was important that the cable screen at the base board was taken to the 0V plane very close to a grounding connection to the chassis. Otherwise, the discharge current would have had to flow in a large area of the 0V plane, with greater stress to the processor operation.

The ESD susceptibility of the LED/LCD assembly was reduced to some extent by a ferrite sleeve on the wires coupling to the base board, but this was not enough. Rather than spend a lot of effort on improving the immunity of this connection, the easiest way around that problem was to prevent a discharge occurring in the first place: both the LEDs and the LCD were protected by a clear plastic window placed over the front of the enclosure, sufficiently large so that no short creepage path existed around its edge to any conductive parts of the components. This is invariably the preferred method of dealing with discharges to any similar parts.

The ESD susceptibility of the transducer ADC was dealt with in the opposite way. There was no way around the fact of a discharge occurring to the metal finger pad. But

the discharge current could be diverted to the base of the unit, simply by using metal instead of plastic pillars, and putting varistors between the analogue 0V of the contact pad and its now chassis-connected metal backing plate. At the same time, the protection of the ADC input was beefed up by series resistors and parallel steering diode pairs. Then, the discharge current was encouraged to flow through the pillars to chassis rather than through the high impedance of the ADC input, which in turn could cope with the remanent spike that did make it onto the base board.