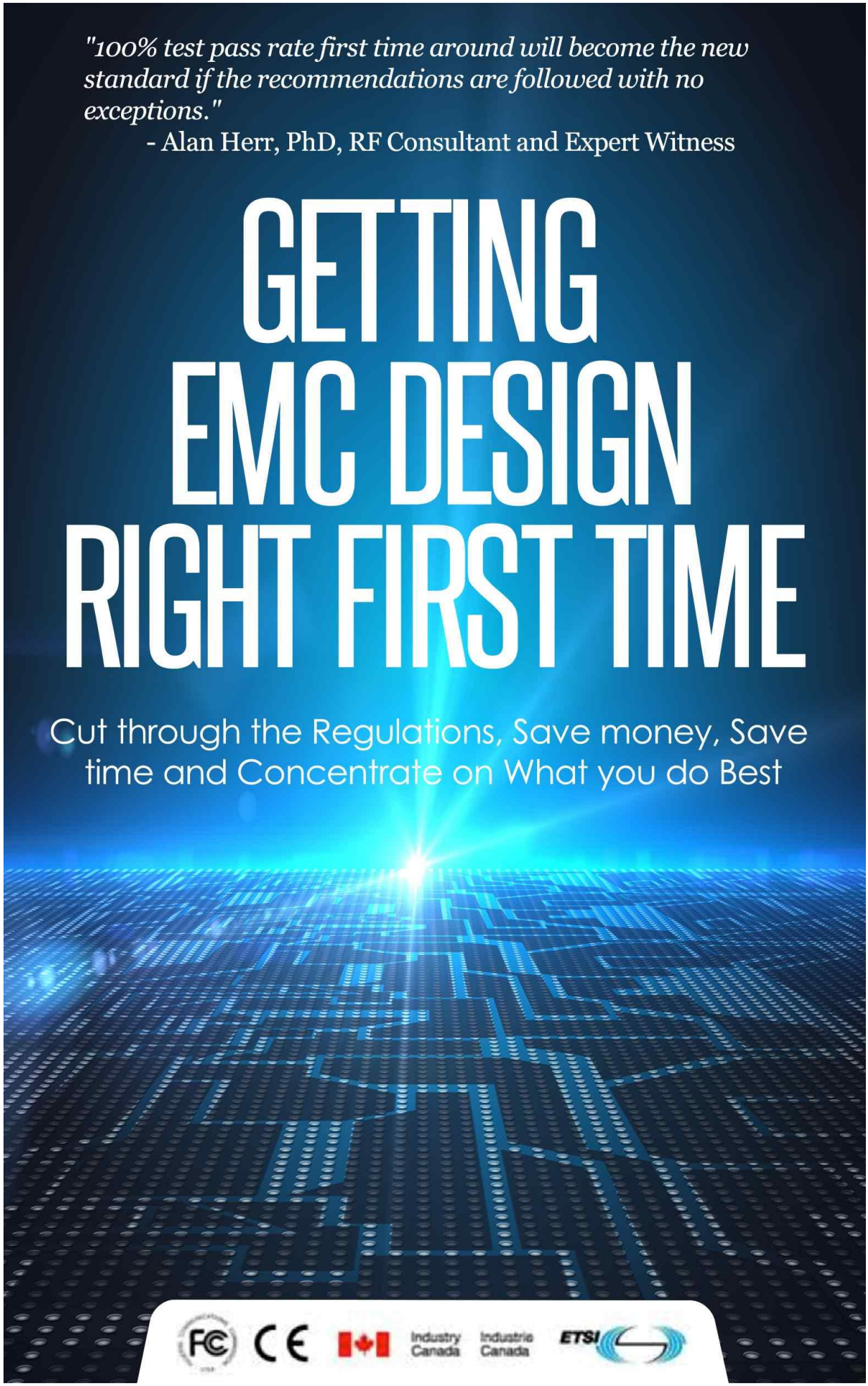
"100% test pass rate first time around will become the new standard if the recommendations are followed with no exceptions."

- Alan Herr, PhD, RF Consultant and Expert Witness

GETTING EMC DESIGN RIGHT FIRST TIME

Cut through the Regulations, Save money, Save time and Concentrate on What you do Best



Getting EMC Design Right First Time

Version 2.1

By

EMC FASTPASS

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Editor: A. Eadie (B.Eng)

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Foreword

I created EMC FastPass in 2014 with a specific goal in mind: to help hardware manufacturers to get a grip on the EMC problem.

According to a report from Intertek, one of the largest test lab groups, approximately 50% of hardware products fail EMC testing first time. That number lined up with the failure rate I saw at my own independent EMC/RF test lab. That's huge!

A failure could cost your company an extra ½ day at a test lab if you're extremely lucky, but more than likely it will cost you several days to several weeks of unaccounted for development and debug time. Project delays of months are not unheard of.

The short of it is that EMC failures cost the electronics industry billions of dollars in additional project costs and lost revenue.

I noticed that there were many heavy leather-bound books on the subject of EMC, as well as instructors who travelled the world delivering EMC seminars.

Yet the problem persists, and if anything, it's getting worse.

So, I started EMC FastPass to begin providing high-quality online education to any engineers who were interested in learning more about the subject.

As the website and company grows, we're excited to continue publishing case studies, blog posts, webinars, eBooks and online courses. The subject of EMC is so large that there's a lifetime of learning and exploring to do!

If you're just getting into EMC, this eBook is a great start, but I would encourage anyone looking to take their EMC knowledge and education further to enrol in our online training courses (details below).

Have fun and stay curious!

Enjoy,

Andy Eadie
Founder, EMC engineer and instructor.

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Table of Contents

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1. Grounding and Planes

1.1 Filters

Hint on filtering

- ***Use a global filter for each power supply. Use a local filter for each block sensitive to power supply noise.***

Each power supply must have a filter located in close proximity either to the voltage regulator if it is located on board, or near the PCB entry point if regulator is external. This filter should be designed in accordance with the ripple characteristics of the regulator and the power supply requirements of the integrated circuits, and should include at least two capacitors:

- One large capacitor (µF) for low-frequency filtering
- One small capacitor (nF) for high-frequency filtering

Integrated circuits that require a clean power supply should be provided with an additional L-C filter, to avoid noise coupling through from other blocks of the circuit. An example of appropriate filtering for such a case is illustrated by figure 3.1

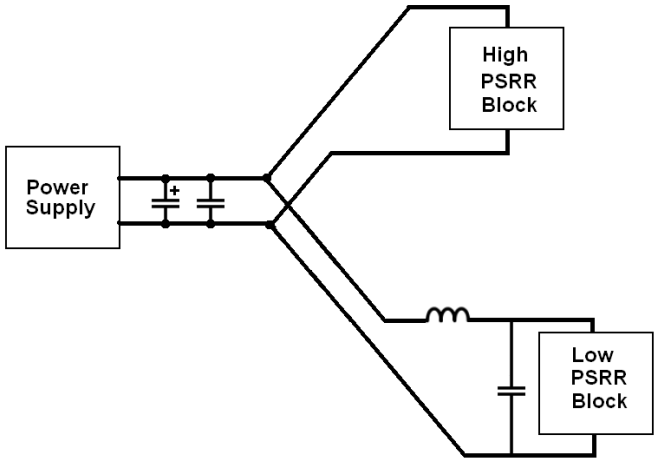

Fig. 3.1 Filtering of high and low PSRR blocks supply

Further details on the filter placement and routing are provided in the EMC chapter, paragraph 6.3.2

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1.2 Routing

An absolute MUST for routing power/ground traces

- ***Power/ground trace should be as wide as possible and close to each other.***

The power distribution network (PDN) should provide a low-impedance path between the voltage regulator and the integrated circuits. The best way to achieve this is by using power planes both for the supply voltage and ground, as planes provide an inter-plane capacitance and a low inductance. If multiple supply voltages and ground nets are used, they should not be placed on parallel planes as the capacitive coupling between them will allow high frequency currents to flow between planes. For such a case the plane layers should be split between multiple nets. Figure 3.2 illustrates an example of poor and proper separation of signal and RF ground.

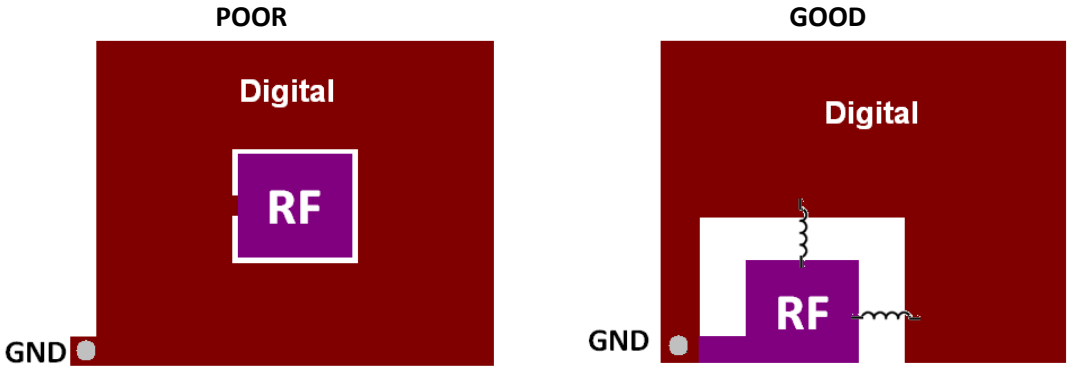

Fig. 3.2 Example of poor and good ground separation

The first solution is poor because:

- RF currents must travel to the digital ground in order to reach the GND point (at supply)
- The small clearance between digital and RF ground will generate capacitive coupling

The second solution is good because:

- RF return path does not overlap with the digital return path
- The large clearance between planes minimizes the coupling capacitance
- Additional inductors increase the coupling impedance, to prevent RF currents to flow from one plane to another

If planes cannot be used for each supply voltage, the routing should be done with respect to the following recommendations:

(i) Power and ground traces should be as wide as possible

(ii) Power and ground traces should not create large loops, as this will drastically increase the self inductance

(iii) Any available areas on PCB should be filled with ground island

(iv) If a layer is used for both routing and as a ground plane, caution should be taken when routing through the plane in order to avoid creating large return loops. If a trace must penetrate the plane then this should be bridged, as illustrated by fig 3.3.

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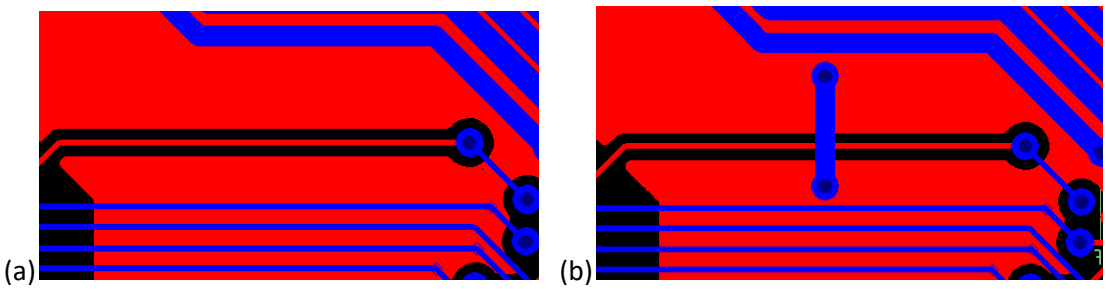

Fig. 3.3 Un-bridged (a) and bridged (b) ground plane

(v) If a star distribution topology is required for crosstalk or EMC considerations, such as the PDN illustrated in fig. 3.1, each supply trace must have its own return path in order to fulfill the "small loop area" requirement

(vi) If multiple isolated ground levels are used, such as a common ground and a RF ground, they should not be routed in proximity to avoid capacitive coupling.

1.3 Plane slots and boundaries

Hint on routing over plane slots and boundaries

- ***Don't !!!***

Plane slots are created when a plane is cut to accommodate routing traces. This should be avoided when possible, but sometimes must be done due to routing space restrictions. Plane slots are also created by THD components such as dual in-line ICs or row connectors. Figure 3.4 illustrates such examples of plane slots.

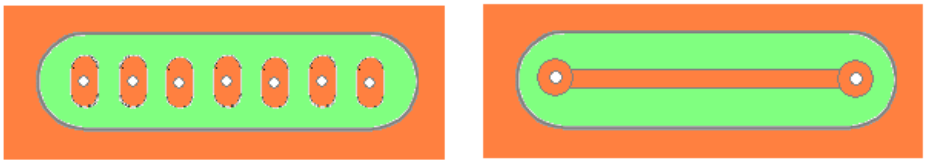

Fig. 3.4 Plane slots

When a signal trace passes over a plane slot, the return current will have to travel around the slot and so create a large loop which will add an impedance discontinuity, increase its self inductance and radiated emission. To prevent this, high speed signal traces should not pass over plane slots. If this cannot be avoided than another return path should be created, close to the signal path, either using a ground trace or a partial plane on another layer.

A similar thing happens when signals pass over the boundary between separated planes. This should also be avoided.

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1.4 Decoupling capacitors

Hint on decoupling

- ***Use multiple decoupling capacitors per pin pair for ICs expected to generate a lot of noise (high-speed bus drivers, DSPs, processors)***

Hint on routing decoupling capacitors

- ***Make sure the supply current goes to capacitor first, and only then to the IC***

Each integrated circuit should have at least a decoupling capacitor placed in close proximity to the supply pins. The decoupling capacitors are required to provide the transient currents the IC needs during switching, to counteract the effect of the power supply output inductance and supply-IC interconnection inductance. For the decoupling capacitors to be effective, their placement and routing should be done with respect to the following recommendations:

(i) The decoupling capacitors should be placed as closed as possible to the supply pins of the IC

(ii) If the IC has multiple VCC-GND pairs, each require its own decoupling capacitor. See manufacturer's datasheet and application notes for further details.

(iii) If the power and ground pins are far apart, it is better to place the capacitor closer to the ground pin, as signals are referenced to ground

(iv) The power and ground pins should not be connected directly to the power and ground nets but through the decoupling capacitor, otherwise its effectiveness will be limited

(v) The traces connecting the decoupling capacitor to the IC pins should be as wide and closely spaces as possible, to provide a low impedance between them

(vi) The traces connecting the decoupling capacitor to the power and supply nets should be narrow and loosely spaced, to provide a high impedance to the potential noisy power and ground nets.

Figure 3.5 illustrates the appropriate placement and routing of the decoupling capacitors.

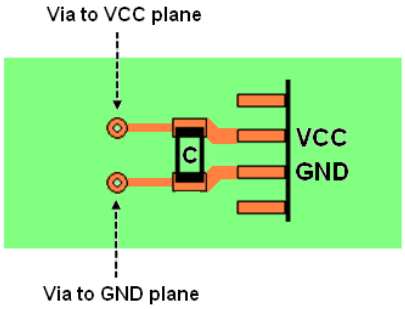

Fig. 3.5 Placement / routing of the decoupling capacitors

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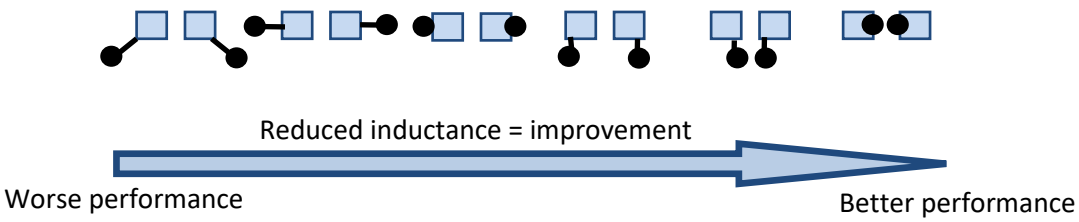

1.5 Power Distribution Network Impedance

Hint on PDN impedance

- ***Don't trust rules of thumb on this, as details matter. Run a thorough analysis to make sure the PDN impedance is low on the entire frequency range.***

The power distribution network (PDN) impedance is determined by several factors, illustrated by fig. 3.6:

- The power supply output impedance
- The PCB traces impedances
- The power supply filtering
- The decoupling capacitors
- The choice of filtering and decoupling capacitors (trough their equivalent series resistance – ESR – and equivalent series inductance – ESL)
- The inter-plane capacitance of the PCB
- The ICs input impedance.

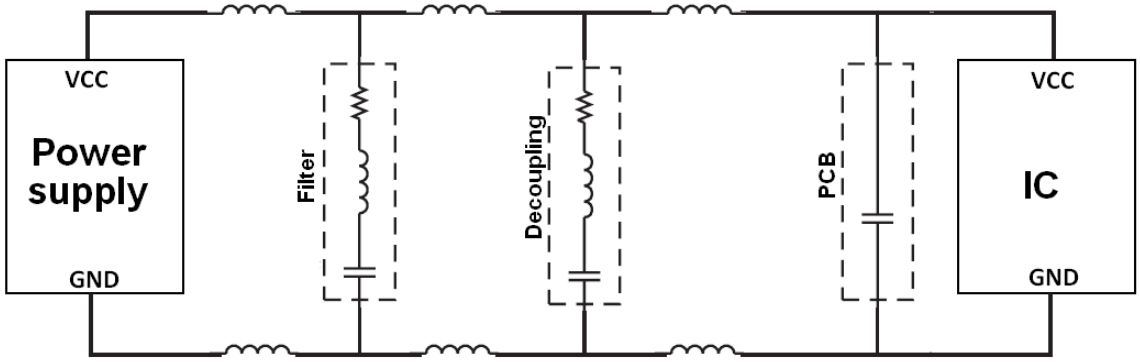

Fig. 3.6 PDN Equivalent circuit

The goal of analyzing the PDN impedance is to keep it as low as possible on the entire frequency range between DC and the effective frequency (see paragraph 4.2 for a definition of the effective frequency). The most critical aspect regarding the choice of decoupling capacitors is, besides the capacitance value, their ESL. As a general requirement, decoupling capacitors should have a low ESL, which is accomplished using small packages (0402, 0603).

As so many factors contribute to the PDN impedance, it is important to run a thorough analysis using a software tool. Figure 3.7 illustrates one situation where a single detail really makes

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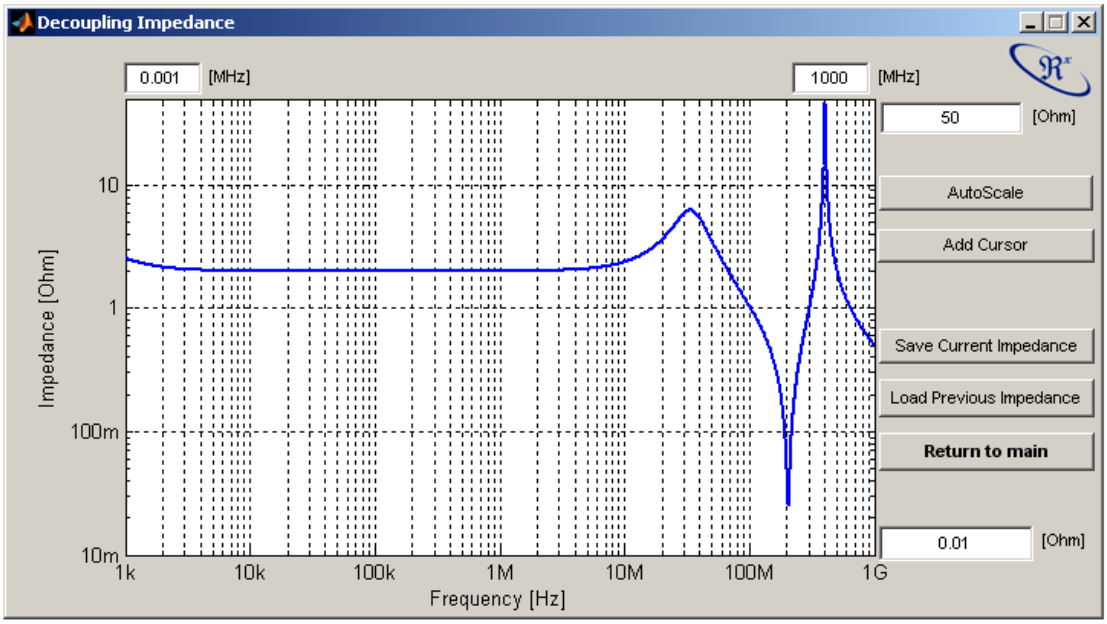
the difference: two identical decoupling solutions implemented on different stackups. Note that when the PCB provides an inter-plane capacitance the PDN will have a large impedance around 300 MHz, caused by the anti-resonance between the inter-plane capacitance and the 1 [nF] decoupling capacitor, which will likely generate higher supply noise at this frequency.

100 [µF] || 1 [nF] || PCB inter-plane capacitance



100 [µF] || 1 [nF], no PCB inter-plane capacitance

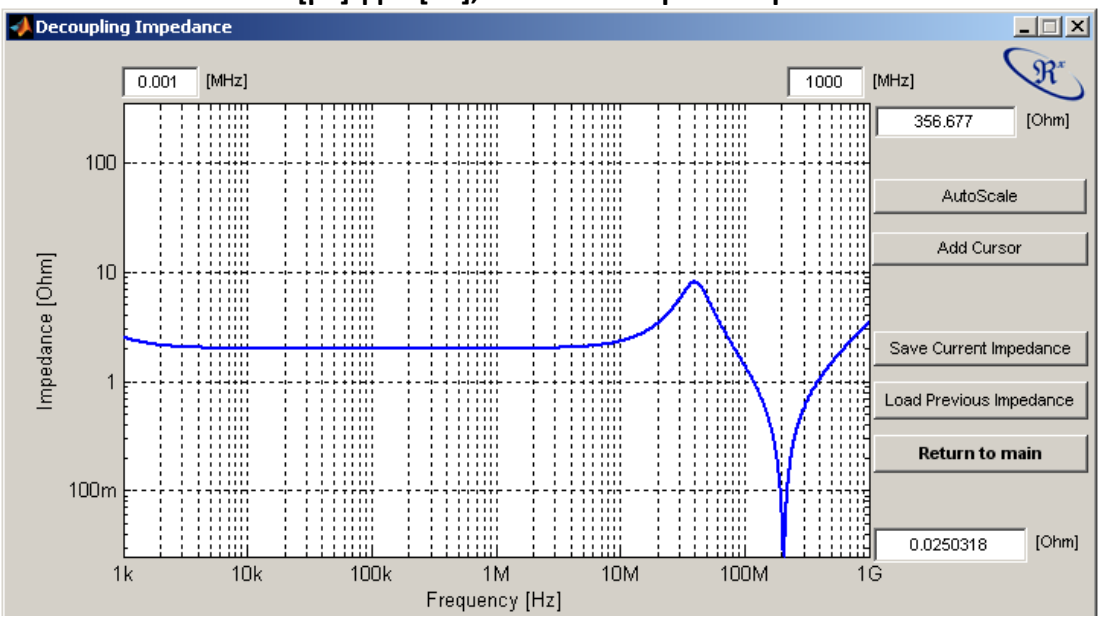


Fig. 3.5 PDN Impedance analysis

Free PDN analysis software such as Altera's PDN tool can provide a lumped-modeling analysis of the decoupling network to predict their impedance. If a more detailed analysis is required then a distributed-modeling simulation using a power integrity simulator such as Hyperlynx PI should be considered. See section 11.3 for software options.

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2. High Speed Considerations

2.1 Identifying High Speed Signals

Critical Length Rule

- ***Signals carried by PCB traces longer than 1/10 of the critical length should be regarded as high speed signals***

High speed signals are not necessary signals of high frequency, but rather signal with fast rise/fall time. Most of the energy of a digital signal is concentrated below the knee frequency, defined as:

$$f_{KNEE}[GHz] = \frac{0.35}{t_{rise}[ns]} \tag{4.1}$$

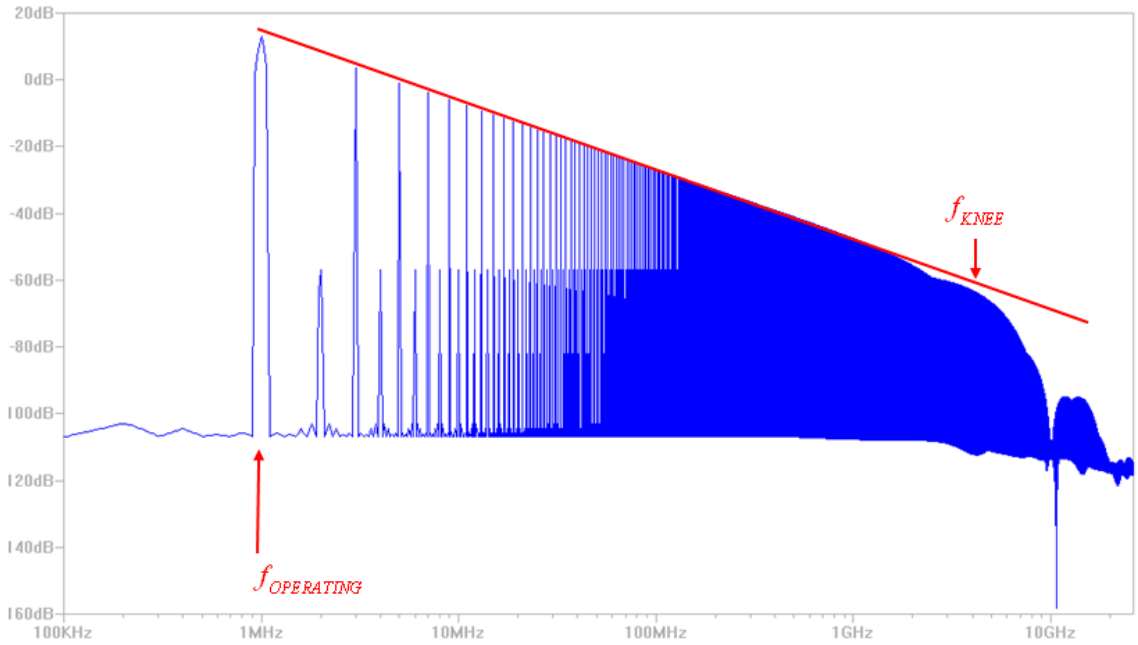

Fig. 4.1 Spectrum of a digital signal with $f_{OPERATING}$=1 [MHz] and t_r = 0.1 [ns]

In order to avoid distortion of digital signals, the PCB must be able to transport their entire spectrum not just the operating frequency.

High speed signals make the PCB traces act as transmission line, even if their physical length seems short. A good indicator of when a trace exhibits transmission line behavior is the critical length, defined as:

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$$l_{CR} = \frac{t_r}{2 \cdot TD} = \frac{t_r \cdot v}{2} \ [m] \tag{4.2}$$

, where TD is the characteristic time delay of the line:

$$TD = \frac{1}{v} \approx 3 \cdot 10^{-8} \cdot \sqrt{\varepsilon_r} \ \left[\frac{s}{m}\right] \tag{4.3}$$

Fig. 4.2 illustrates the critical length for various dielectric constants (ε_r) in the typical range 2-10.

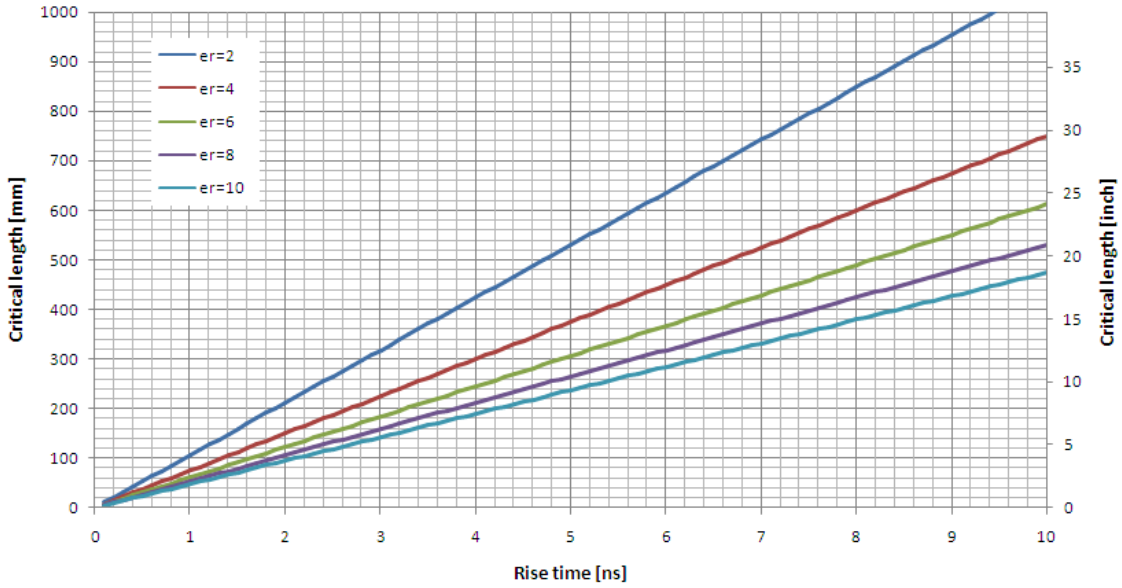

Fig. 4.2 The critical length for various dielectric constants

As the physical length of the trace approaches the critical length, signal reflection, crosstalk and electromagnetic radiation increase.

2.2 Impedance

Controlled Impedance Rule

- ***High speed signals should always be routed with controlled impedance, either in microstrip or stripline configuration. Furthermore, high speed signals require terminations (see paragraph 6.3)***

Note on differential impedance:

- ***The differential impedance of a differential pair is twice the odd-mode characteristic impedance of each trace and lower than the differential impedance of two un-coupled traces***

2.2.1 Single Ended Characteristic Impedance

The characteristic impedance of a PCB trace represents the ratio of the voltage and current waves propagating through a transmission line. It is characteristic in the sense that it

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characterizes signal propagation through any infinitesimally short segment of the transmission line, and it is a local parameter as it can vary along the trace.

Note that the characteristic impedance should not be mistaken as the self impedance (or self resistance) of the trace: a 1[m] long trace may have the same characteristic impedance as a 2[m] long trace, while their self resistances will be different. The typical range for PCB traces characteristic impedance is 20-100 [Ω] and please note that the self resistance of the same trace might be in the range of hundreds of [mΩ].

Each infinitesimally short segment of a transmission line can be regarded as an R-L-C-G circuit, as illustrated by fig. 4.3. Those characteristic parameters of the transmission line determine its characteristic impedance:

$$Z_0 = \sqrt{\frac{R_0 + j\omega L_0}{G_0 + j\omega C_0}} \approx \sqrt{\frac{L_0}{C_0}} \ [\Omega] \tag{4.4}$$

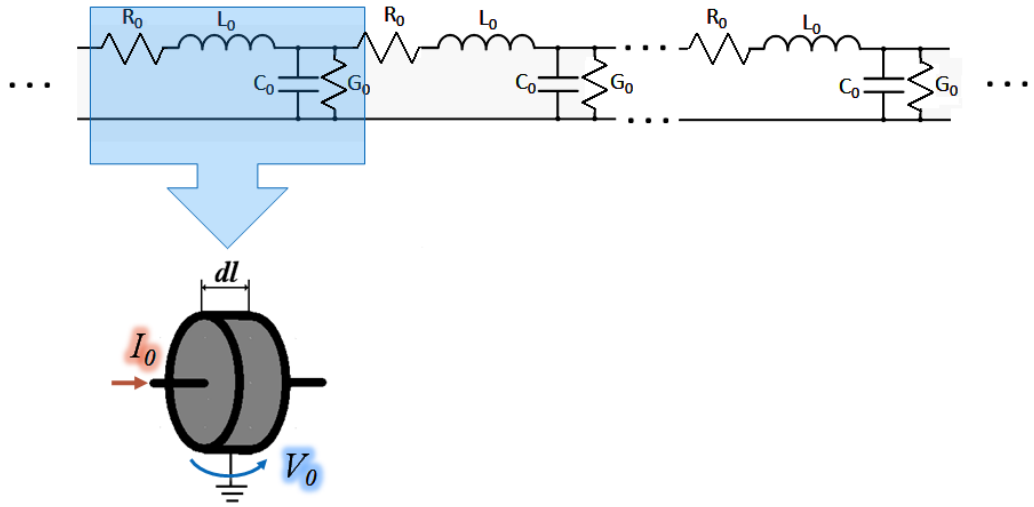
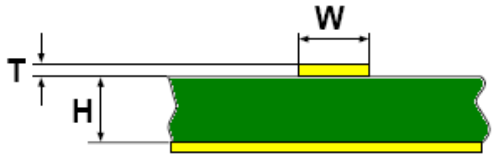
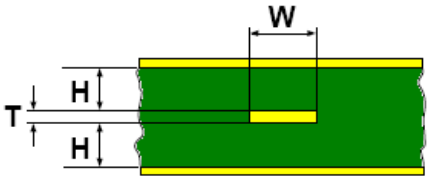


Fig. 4.3 The electrical model of a transmission line

The characteristic impedance is determined by the dielectric type, trace geometry and proximity to power and ground planes. In order to control the characteristic impedance of a trace, those parameters must be controlled. There are two basic PCB geometries that allow the control of the traces characteristic impedance: microstrip (signal trace text to a single reference plane) and stripline (signal trace between two reference planes). Either VCC or GND planes can be regarded as reference planes for impedance control.

Surface microstrip	Symmetric stripline
	
$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \cdot \ln\left(\frac{5.98 \cdot H}{0.8 \cdot W + T}\right)$ [Ω]	$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \cdot \ln\left(\frac{1.9 \cdot (2H + T)}{0.8 \cdot W + T}\right)$ [Ω]

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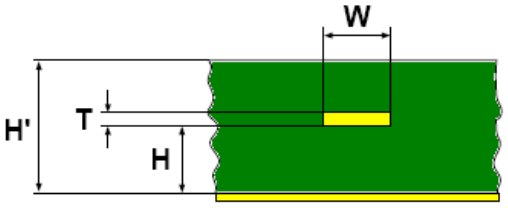
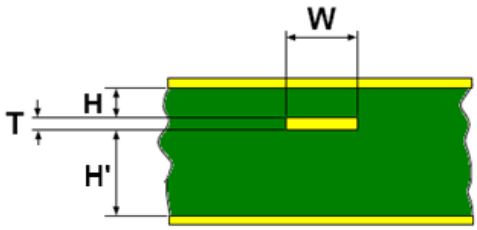
Embedded microstrip



$$Z_0 = \frac{60}{\sqrt{\varepsilon_r'}} \cdot \ln\left(\frac{5.98 \cdot H}{0.8 \cdot W + T}\right) \quad [\Omega]$$

$$\varepsilon_r' = \varepsilon_r \cdot \left(1 - e^{-\frac{1.55 \cdot H'}{H}}\right)$$

Asymmetric stripline



$$Z_0 = \frac{80}{\sqrt{\varepsilon_r}} \cdot \ln\left(\frac{1.9 \cdot (2H + T)}{0.8 \cdot W + T} \cdot \left(1 - \frac{H}{4H'}\right)\right) \quad [\Omega]$$

Fig. 4.4 Controlled impedance configurations

For an estimation of the characteristic impedance of PCB traces use an analytic calculator such as Zcalc, but with precaution regarding the accuracy range. Even in the specified range a ±5% calculation error should be expected. For a more precise evaluation of the characteristic impedance, use a field solver such as Polar SI8000.

2.2.2 Differential Impedance

Differential signals should always be routed in parallel and close to each other in order to avoid coupling of differential noise from various sources. This coupling between differential traces (also called "differential pair") introduces mutual inductances and capacitances, which affects their characteristic impedance. Since differential signals always travel in opposite direction, this coupling (also called "odd mode coupling") will decrease the characteristic impedance of each trace, according to the equations:

$$Z_{ODD\_1} = \sqrt{\frac{L_{10} - L_{12}}{C_{10} + C_{12}}} < \sqrt{\frac{L_{10}}{C_{10}}} \quad [\Omega]$$

$$Z_{ODD\_2} = \sqrt{\frac{L_{20} - L_{12}}{C_{20} + C_{12}}} < \sqrt{\frac{L_{20}}{C_{20}}} \quad [\Omega] \qquad (4.5)$$

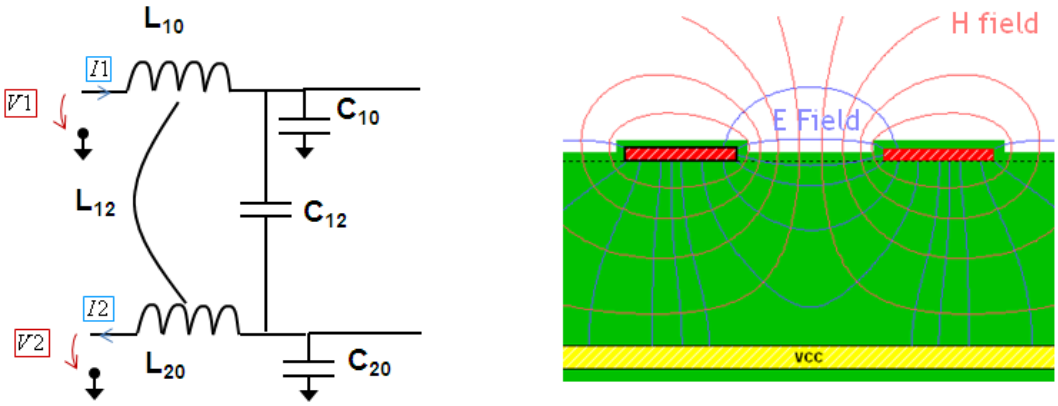


Fig. 4.5 Odd mode propagation of differential signals

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When differential signals propagate on differential pairs, the information is carried by the difference of the voltages on the two lines. This differential signal will "see" the characteristic impedance of the pair as twice the characteristic impedance of each individual trace.

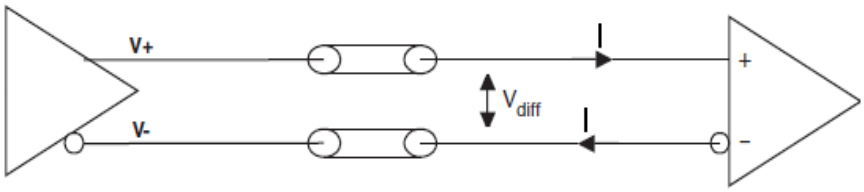

Fig. 4.6 Propagation of differential signals on differential pairs

$$Z_{diff} = \frac{V_{diff}}{I} = \frac{V_+ - V_-}{I} = \frac{V_+ - (-V_+)}{I} = \frac{2 \cdot V_+}{I} = 2 \cdot Z_0 \tag{4.6}$$

Since the characteristic impedance of each individual trace is the odd mode impedance, the differential impedance is defined as:

$$Z_{diff} = 2 \cdot Z_{0\_ODD} = 2 \cdot \sqrt{\frac{L_{10} - L_{12}}{C_{10} + C_{12}}} \tag{4.7}$$

For an estimation of the differential impedance an analytic calculator such as Zcalc may be used. However, please note that analytic calculators can provide as much as ±50% calculation error when it comes to evaluate odd and even mode propagation, so a field solver such as Polar SI8000 is highly recommended.

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2.3 Terminations

Termination Rule:

- ***High speed signals require termination either at the driver or the receiver end. Do not use termination at both ends, as it will reduce the voltage to half their driven values.***

Termination Hint:

- ***When high speed signals drive a chain of multiple receivers only the farthermost from driver should be terminated (see paragraph 6.4.3 on topology)***

Termination Hint:

- ***The easiest way to terminate a differential pair is using a single resistor equal to the differential impedance of the PCB traces***

2.3.1 Single Ended Terminations

When high speed signals arrive at an impedance discontinuity point, some of the energy of the signal will reflect and travel back to the generator. Signal reflections are a major cause of noise and radiation on PCBs, and should be avoided.

To avoid reflections, high speed signals should see a constant impedance from the driver to the receiver. This requires not just to keep the impedance of the PCB trace constant, which is achieved using microstrip or stripline configurations, but also to make the PCB trace characteristic impedance (Z_0) equal to the driver circuit output impedance (Z_{OUT}) and the receiver circuit input impedance (Z_{IN}). This condition is generally not met by default because driver circuits usually have low output impedances and receiver circuits usually have high input impedance. Fig. 4.7 shows a typical signal distortion caused by multiple reflections.

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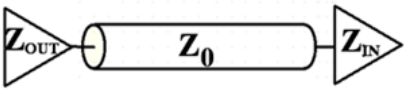


$$Z_{OUT} < Z_0 < Z_{IN}$$

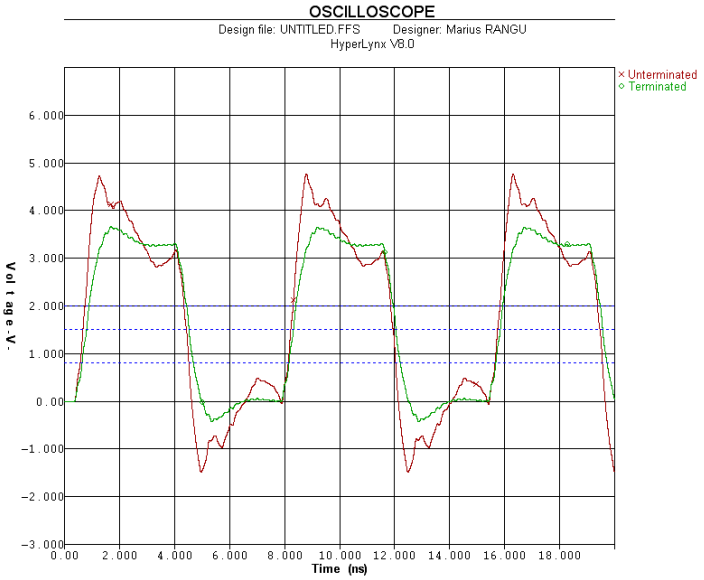
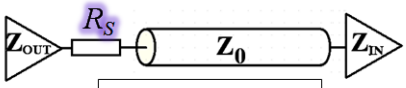


Fig. 4.7 Typical waveform at the receiver for terminated and un-terminated traces

In order to avoid reflections at the driver and receiver ends of a PCB trace, their impedance should match the characteristic impedance of the PCB trace. This technique is called "termination" and achieved using resistors connected at driver / receiver ends of the PCB trace. Fig. 4.8 presents the single ended termination techniques.

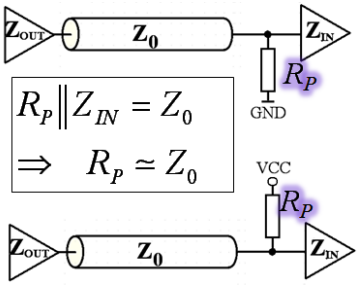
Series termination (at driver)



$$R_S = Z_0 - Z_{OUT}$$

- Avoids signal distortion at receiver
- Doesn't eliminate the first reflection at the receiver (potential radiation problems)
- Has no effect on the driver current and DC voltage levels

Parallel termination (at receiver)



$$R_P \| Z_{IN} = Z_0$$
$$\Rightarrow \quad R_P \simeq Z_0$$

- The termination resistor may be connected either to VCC or GND
- Eliminates all the reflections
- Increases the driver DC current (must drive a low-value resistor)
- Resistor to GND lowers the DC voltage level for *High* state
- Resistor to VCC rises the DC voltage level for *Low* state

Thevenin termination (at receiver)

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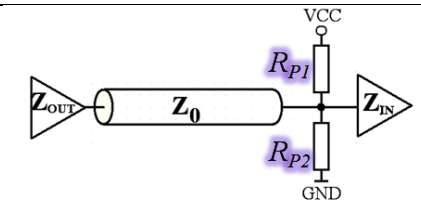
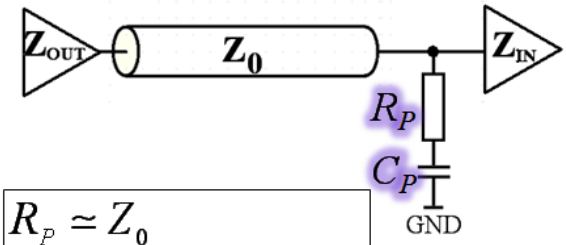


$$R_{P1} \| R_{P2} \| Z_{IN} = Z_0 \quad \Rightarrow \quad R_{P1} \| R_{P2} \simeq Z_0$$

- Eliminates all the reflections
- Increases the driver DC current (must drive low-value resistors)
- Lowers the DC voltage level for *High* state and rises the DC voltage level for *Low* state, half as much as parallel termination

AC termination (at receiver)



$$R_P \simeq Z_0$$

$$\tau_{RC} = R_P \cdot C_P < 2 \cdot t_P$$

- Eliminates all the reflections
- Has no effect on the driver current and DC voltage levels
- Increases the rise time at the receiver end (use with caution!)

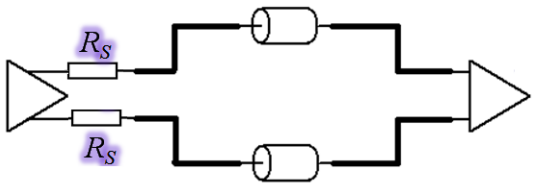
Fig. 4.8 Single ended termination techniques

Series terminations require the resistor to be connected physically as close as possible to the driver, and parallel terminations require the resistors / capacitor to be connected as close as possible to the receiver.

2.3.2 Differential Terminations

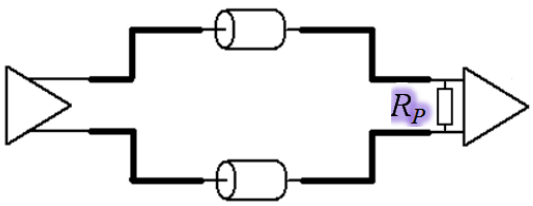
Just like single ended signals, differential signals must "see" a differential impedance constant along the transmission line, which means that driver output impedance should be equal to the differential pair impedance and to the receiver input impedance. The common termination techniques used for differential pairs are presented in fig. 4.9

Series termination (at driver)



$$R_S = \frac{Z_{OUT\_diff} - Z_{diff}}{2}$$

- Avoids signal distortion at receiver
- Doesn't eliminate the first reflection at the receiver (potential radiation problems)
- Has no effect on the driver current and DC voltage levels



- Most common receiver termination
- Eliminates all the reflections of the differential signal
- Does not eliminate the reflections of the common mode signal

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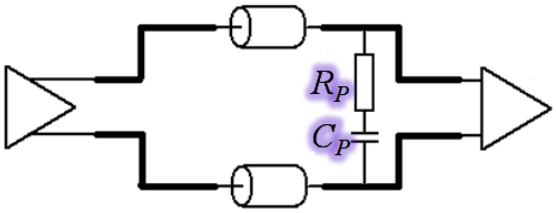
$R_P = Z_{diff}$

- (potential radiation problems)
- Increases the driver DC current (must drive a low-value resistor)

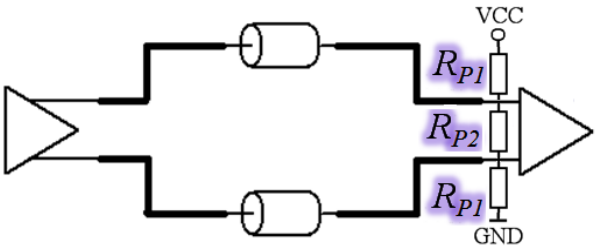
AC termination (at receiver)



$R_P = Z_{diff}$; $\tau_{RC} = R_P \cdot C_P < 2 \cdot t_P$

- Similar to parallel termination but without the additional driver DC current
- Increases the rise time at the receiver end (use with caution!)

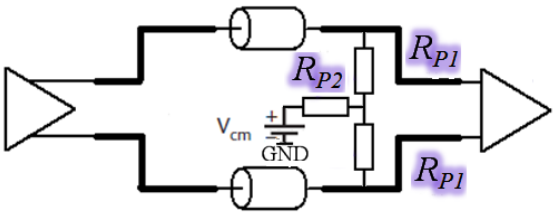
"PI" Termination (at receiver)



$R_{P1} = Z_{even}$; $R_{P2} = \frac{2 \cdot Z_{even} \cdot Z_{odd}}{Z_{even} - Z_{odd}}$

- Terminates both common end and differential signals
- Eliminates all the reflections
- Assures a valid input state at the receiver when driver is in HighZ

"T" Termination (at receiver)



$R_{P1} = Z_{odd}$; $R_{P2} = \frac{Z_{even} - Z_{odd}}{2}$

- Terminates both common end and differential signals
- Eliminates all the reflections
- Requires an additional voltage source for differential signals with common mode offset (some differential receivers might have an internal regulator to provide common mode voltage outside the chip, if this is the case then use it!)

Fig. 4.9 Differential termination techniques

Just like for single ended signals, series terminations require the resistors to be connected physically as close as possible to the driver, and parallel, PI and T terminations require the resistors / capacitor to be connected as close as possible to the receiver.

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2.4 Placement

Block placement rule

- ***The circuit should be partitioned into functional blocks and each block should have a restricted zone assigned on the PCB***

Block placement hint

- ***The most "aggressive" blocks should be placed closest to the supply***

2.4.1 Partitioning

The schematic of almost any electronic application is a concatenation of functional blocks. It is essential that those blocks are correctly identified and that the components within each block are grouped together on the PCB, in order to minimize crosstalk and reduce interconnections length. Most signal integrity problems associated with high speed signals can be addressed by propped component placement.

Prior to detailed placement and routing, the schematic should be partitioned into functional blocks. Furthermore, to ease the next step of zoning, the functional blocks should be classified according to the specificity of the signals contained.

Class	Description
Supply	Power supply circuitry (converters, regulators, filters). The decoupling capacitors should not be included in the supply blocks
Analog	Low level analog signal processing blocks
Digital	Digital processing blocks
Power	High voltage and / or high current blocks.
RF	Radio frequency communication blocks

2.4.2 Zoning

Once the system is partitioned into functional blocks, each should be assigned a distinct physical location on the PCB. This operation is called "zoning" or "floor-planning". A draft placement should be made in order to estimate the space necessary for each block.

The zoning should tend to minimize the length of the interconnections between blocks and also the electromagnetic coupling between them. Coupling can be caused either by electromagnetic fields interference, which can be minimized by physically placing the blocks as far apart as possible, either by common impedance, which is caused by return currents following the same physical path. Since all currents return to the power supply, the common return between each block class should be made as short as possible. This requires the most "aggressive" blocks (RF, Power, Digital) to be placed closer to the Supply and the most sensitive blocks (Analog) to be placed farther to the Supply. If possible, highly "aggressive" blocks (RF) should be isolated from the main circuitry in order to completely avoid a common return path.

Figure 4.10 presents a recommended zoning for an application with several functional blocks.

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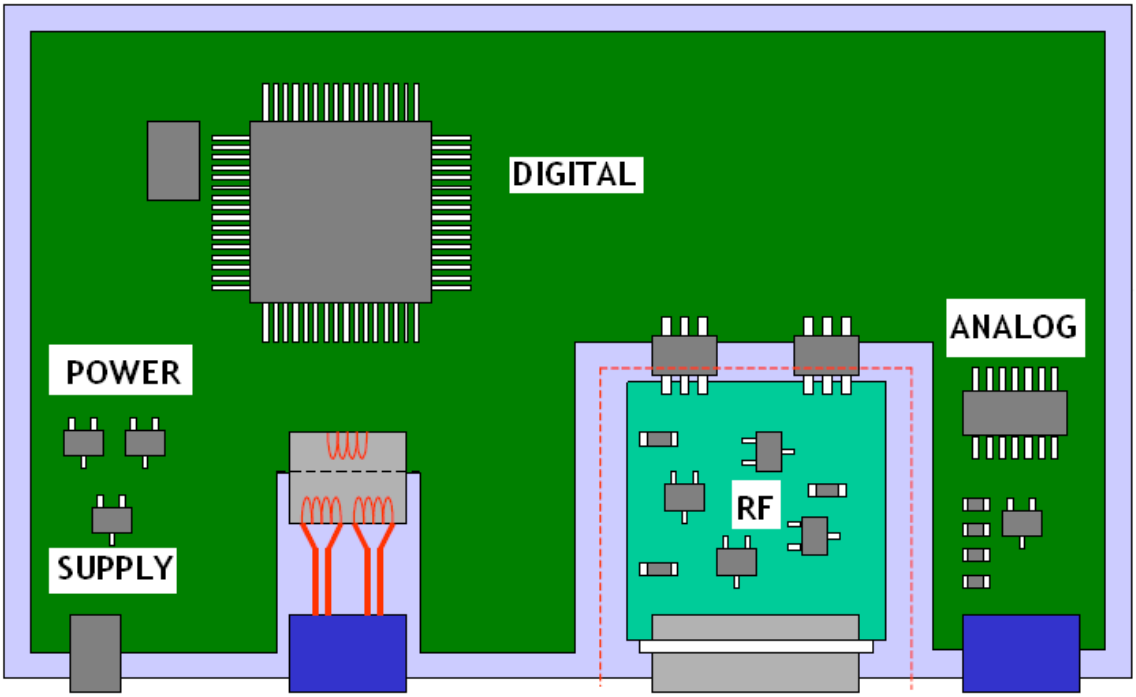

Fig. 4.10 Recommended zoning for various functional blocks

2.4.3 Analog Buffers

It is a common practice to carry the analog signals generated outside the application PCB, such as those coming from sensors, through analog buffers (repeaters). This can have beneficial effects on the integrity of the analog signals because the buffers will drive the PCB traces with a low impedance source, which will reduce their susceptibility to crosstalk noise caused by capacitive coupling. In order to benefit from this advantage, it is essential that analog buffers are placed as close as possible to the PCB entry point of the analog signals.

If possible, the analog blocks should be placed close to the analog signal connectors to minimize the interconnections length. However, since connector placement is usually determined by mechanical requirements, this might not be possible. If this is the case then the analog buffers should not be considered part of the analog processing block but associated with the signal connectors. Figure 4.11 presents the recommended placement of analog buffers for such a situation.

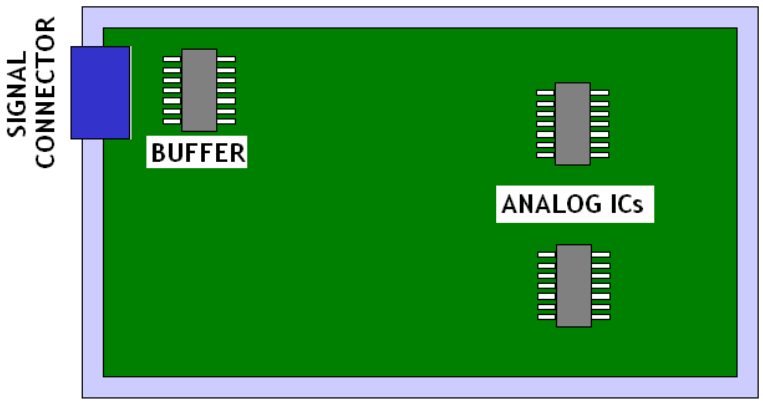

Fig. 4.11 Recommended placement of analog buffers

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2.5 Routing

Hint on routing topology

- ***Think twice before deciding on a bus topology and designing it. Use a transmission line simulator for a thorough investigation, as each routing detail is important***

Hint on routing buses

- ***Keep the buses as wide as practical and hidden from the rest of the world***

A rule of thumb for corners

- ***90° corners should be avoided for RF signals and digital signals with rise times smaller than 0.1 [ns]***

Hint on vias

- ***Avoid using PTH vias for high speed signals and keep their number to a minimum***

Rules of differential routing

Route differential pairs in this order:

1. ***With equalized propagation time***
2. ***Symmetrical***
3. ***Tightly coupled***
4. ***Homogeneous***

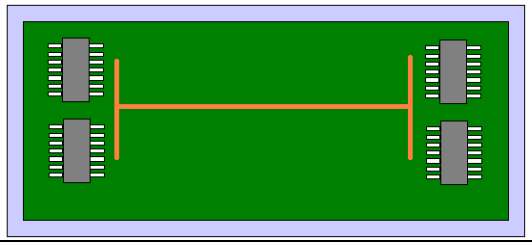
Rule of thumb for board edge

- ***Avoid routing high speed signals closer to 10·H to the edge of the board.***

2.5.1 Topology

High speed signals that must interconnect multiple ICs may be routed in one of the topologies illustrated by fig. 4.12. This is often the case for clock and control signals, but may also apply to data busses or analog signals. Each topology has advantages and disadvantages and must allow an optimal compromise between signal integrity and geometrical constraints. Note that for signals that don't qualify as "high speed", the topology is largely irrelevant.

Point to point



- This can only be applied if all ICs can be grouped into just two blocks and the connections between proximate ICs can be kept well below the critical length
- The interconnection behaves like a simple interconnection between two ICs

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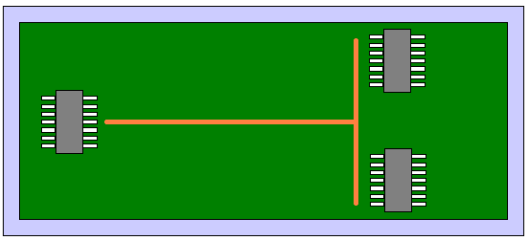
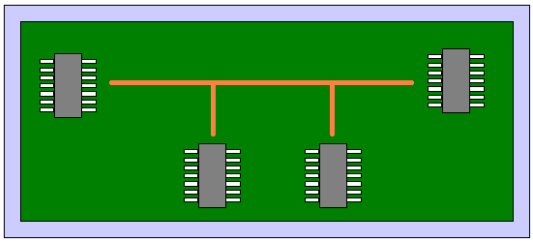
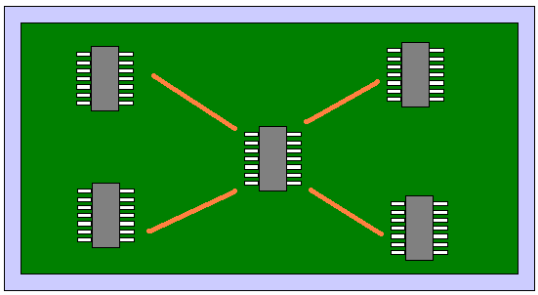
	• Provides best results from the signal integrity point of view but is very demanding in terms of routing
	**"T"** • This topology derives from the point-to-point topology if the connections between proximate ICs cannot be kept below 1/10 of the critical length • It provides good results for unidirectional signals, with the driver located at the left. • The interconnections length between the T junction and the receiver ICs should be closely matched, otherwise the junction point will introduce an impedance discontinuity • Can provide equalized propagation times • Each receiver needs termination • The arms of the "T" should have twice the characteristic impedance of the body
	**Daisy Chain** • This topology is common for the multi-drop data busses • The stubs should be much shorter than the critical length, otherwise they will introduce impedance discontinuities • The parasitic of each IC along the chain (package & pad capacitance) will introduce a small impedance discontinuity. Those effects cumulates, so the larger the number of ICs the worse signal degradation should be expected. • Only the first or last ICs in the chain require terminations
	**Star** • This topology should be considered for unidirectional signals when the propagation time matching is critical • The driver should be located in the middle and all the receivers interconnected with traces having exactly the same propagation time • Each receiver should be terminated identically • Use with caution as any unbalance between driver-receiver connections can have detrimental effects on the signal integrity

Fig. 4.12 Routing topologies

Upon deciding on a routing topology, a thorough investigation of the particularities of the ICs should be done. Useful information can be usually found in the IC's datasheet and application notes. If available, a transmission line simulator such as HyperLynx (and appropriate IBIS models) should be employed to provide a numerical prediction before deciding on a specific topology.

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2.5.2 Bus Routing

Buses pose special signal integrity problems because they require a large number of traces to be routed in parallel for a long distance and also because they usually switch at the same time. Expect the worst from buses, as multiple problems are likely to occur at the same time. Besides topology (covered in paragraph 4.5.1) and timing (covered in paragraph 4.7) issues, some of the signal integrity problems related to busses are:

- ***Impedance variations***: when two traces are routed in parallel for a long distance they will be electromagnetically coupled through a mutual inductance and a mutual capacitance. When two signals travel in the same direction through those lines (both signals switch from 0 to 1 or from 1 to 0), the coupling will modify the characteristic impedance of each trace to the even mode impedance, which is larger than the un-coupled characteristic impedance. When two signals travel in opposite directions through those lines (one signal switches from 0 to 1 and the other from 1 to 0), the coupling will modify the characteristic impedance of each trace to the odd mode impedance, which is smaller than the un-coupled characteristic impedance. As a result, the impedance of each trace will not be constant in time but will vary according to the switching of the adjacent signals. This impedance variation gets larger as the traces are more closely spaced and will cause signal reflections due to discontinuities. Figure 4.13 illustrates the impedance variation of two 60 [Ω] microstrip traces with their clearance. In order to minimize the reflection noise caused by impedance variation the bus clearance should be as large as practical.

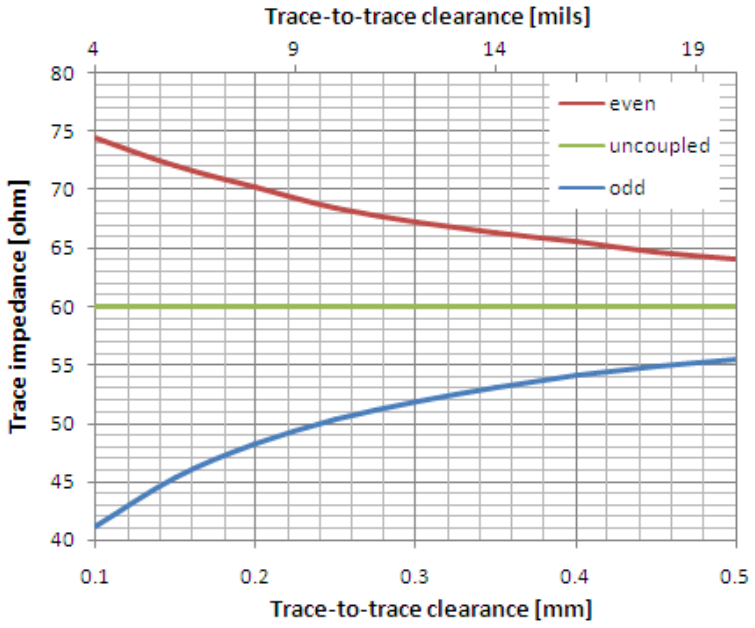

Fig. 4.13 Impedance variation caused by coupling between bus traces

- ***Skew***: if all bus lines don't have exactly the same propagation time then various signals will arrive at the receiver with various delays, an effect called "skew". Even if all the traces have exactly the same length, the coupling between microstrip traces will affect the propagation delays in the same way as the impedance, so a certain amount of skew

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should be expected. For a numerical prediction of the skew caused by coupling between bus lines, a field solver such as HyperLynx should be used. Please note that stripline traces do not exhibit skew due to coupling as the odd mode and even mode propagation speeds are identical. Figure 4.14 illustrates the propagation time variation of two 60 [Ω] microstrip traces with their clearance. In order to minimize the skew caused by propagation time variation the bus clearance should be as large as practical.

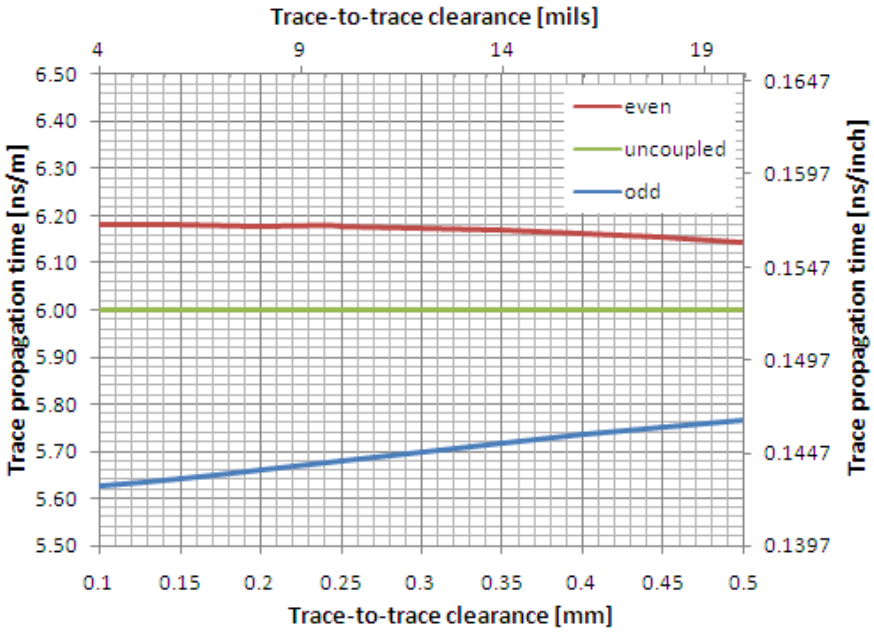

Fig. 4.14 Delay variation caused by coupling between bus traces

- ***Crosstalk***: when a signal switches it will induce a small amount of noise into nearby traces doe to capacitive and inductive coupling (for details see paragraph 4.6 on crosstalk). When several signal switch simultaneously, the crosstalk effect is multiplied and a large amount of noise can be induced into nearby traces. Buses are very “aggressive” with respect to crosstalk and should be kept as far as practical from other signals, especially sensitive ones (analog). The crosstalk effect is lower between stripline traces than microstrip, so it is highly recommended to route the buses on a stripline layer.

- ***Radiation***: when a signal switches it will radiate an electromagnetic field in the surrounding environment (for details see chapter 7 on EMC). When several signal switch simultaneously, the radiation effect is multiplied and might exceed EMC regulations. The radiation can be minimized by reducing the bus length, shielding between reference planes and reducing the signal rise time. To keep the radiation to a minimum, route the buses as short as possible on a stripline layer, terminate all lines and, if necessary and possible, reduce the signal rise time using filters.

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2.5.3 Corners

Corners routed at 90° will introduce small impedance discontinuities because at the corner location the trace width will be larger than on the straight trace. This will cause a localized increase of the characteristic capacitance of the trace, hence a decrease of the characteristic impedance. To avoid this effect, it is a good practice to avoid routing with 90° angles and to use instead 45° or rounded corners. Figure 4.15 illustrates the three possible corner geometries.

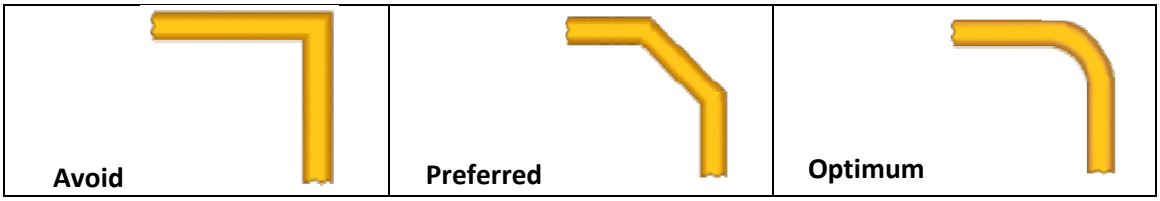

Fig. 4.15 Corner geometries

It should be noted that although the previous considerations are in theory correct, in practice the corners effect is insignificant unless the signal has very small rise time. As a rule of thumb, precautions regarding corners should be taken when operating with rise times smaller than 0.1 [ns] or with radiofrequency signals.

2.5.4 Vias

Signal vias that penetrate reference planes should be regarded as impedance discontinuities because of the capacitance created between the copped barrel and the planes. Via capacitance increases with the height of the board, the hole size and the number of reference planes penetrated, so largest capacitances should be expected for large PTH vias. Typical via capacitances are below the [pF] range, so their effect is usually small. However, since the reflection noise accumulates, traces with large number of vias carrying high speed signals may pose signal integrity problems. To avoid them, use the least possible vias, make them small and allow a large clearance to reference planes. For a numeric prediction on the vias effect on a particular signal, use a field solver combined with a transmission line simulator.

2.5.5 Differential Routing

Differential signals require some routing precautions in order to benefit of the advantage of common mode noise suppression. Those requirements can be ordered as follows:

(i) Equalized propagation time

A difference in the propagation time of the differential signals (skew) will put the receiver in an undetermined state for the time interval between the arrival of the fastest and slowest signals. Figure 4.16 illustrates this effect for a differential pair with a common mode voltage of 1 [V] and a differential voltage of ±2 [V]. When the receiver has a 0 [V] differential voltage at its inputs it will be in an undetermined state. This situation should be avoided and if necessary the length of the fastest trace should be increased using serpentine routing, as illustrated by figure 4.16, in order to equalize the propagation times of the two traces. Please note that as the characteristic propagation time may vary from one layer to another, it might not be enough to

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equalize the lengths in order to equalize the propagation times. It is recommended that the traces of a differential pair will have the same length on each layer used for their routing.

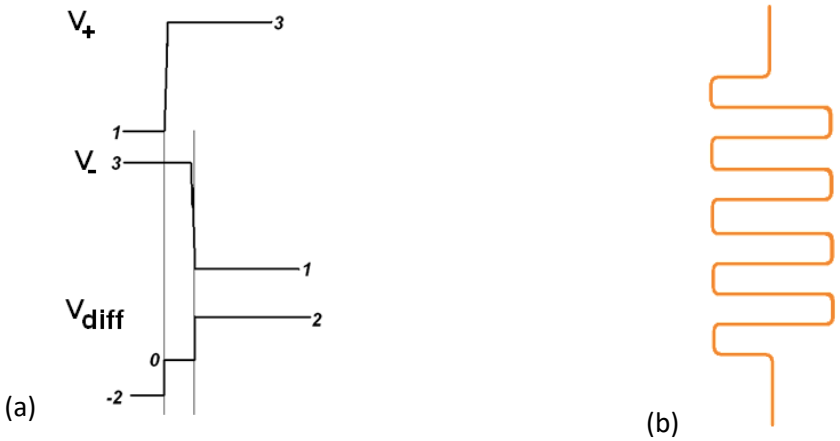

Fig. 4.16 (a) Undetermined state at the receiver caused by skew (b) Serpentine routing

(ii) Symmetry

To suppress the noise, both traces of a differential pair should be equally affected by any possible noise source, such that any noise would manifest as differential. To prevent crosstalk noise to act as common mode noise, the differential pair should be routed symmetrically with respect to any possible "aggressor" signal. When an obstacle such as a via or IC pin must be detoured, the two traces should detour on both sides in order to avoid any potential crosstalk from the obstacle to affect one trace more than another. Figure 4.17 illustrates the recommended detouring of obstacles for differential pairs.

Fig. 4.17 Differential pair detouring of obstacles

(iii) Tight coupling

The characteristic impedance of each trace is influenced by the coupling with adjacent traces. Since the coupling of a differential trace with its pair is always odd mode coupling, this allows a precise control of the differential impedance. However, coupling with adjacent traces may also affect the characteristic impedance of each differential trace, hence the differential impedance. Since coupling with adjacent traces may either odd or even depending on the operating conditions, this will cause variations in time of the differential impedance. To minimize this effect, differential traces should by tightly coupled (have a small clearance) between them and loosely coupled (have a large clearance) with other traces.

Furthermore, tight coupling means that any noise that affects a single trace of the pair will be also coupled to the other trace, transforming differential noise into common mode noise, which is suppressed. Tight coupling aids symmetry.

(iv) Homogeneity

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To avoid noise caused by reflections, the characteristic impedances of each trace of a differential pair should be kept constant across its entire length, by keeping the width and clearance constant on each routing layer. However, this is the least stringent requirement as reflection noise caused by trace heterogeneity has less detrimental effects on signal integrity than the noise caused by skew, asymmetry or loose coupling. The recommended routing geometries illustrated by fig. 4.16 and 4.17 are both heterogeneous.

2.5.6 Proximity to Board Edge

Near the board edge the electric fields will close partly through the dielectric and partly to the air surrounding the board. There are two concerns regarding proximity to board edge:

(i) High speed signals

PCB traces signals routed close to the board edge will have a different characteristic impedance and propagation time than traces routed inside the PCB. It is recommended to avoid routing high speed signals closer to 10·H to the edge of the board, H being the distance between the signal layer and the farthermost reference plane.

(ii) Power planes

At the edge of the board the VCC-GND pair of planes will radiate electromagnetic fields higher than if the fields were completely contained by the PCB dielectric. A rule of thumb, called "The 20-H rule", recommend that the VCC plane should be smaller than the GND plane with 20·H on each side of the board, in order to reduce electromagnetic radiation. This rule is illustrated by fig. 4.18

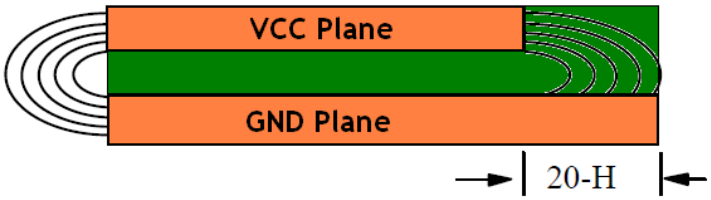

Fig. 4.18 The 20H rule

Experimental measurements suggest that the effects of the 20-H rule on the far field radiated by the PCB are practically null (see for instance http://www.sigrity.com/papers/epep2000/epep_20h.pdf). The 20-H rule only seems effective to reduce the electromagnetic coupling between the PCB and cables routed close to the board edge, so it is recommended to be applied only in this situation.

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2.6 Signal Timing

Rule of thumb for time-critical signals

- ***High speed signals with propagation time greater than 1/10 of the clock period should be regarded as time-critical signals.***

Hint on timing

- ***Always perform an eye diagram analysis of time-critical signals***

2.6.1 Identifying time-critical signals

High speed signals are affected by reflection and crosstalk noise on each rising and falling edge, which will cause the signal to "fly" a certain time interval before stabilizing at the DC value. Figure 4.19 illustrates these phenomena for a rising edge.

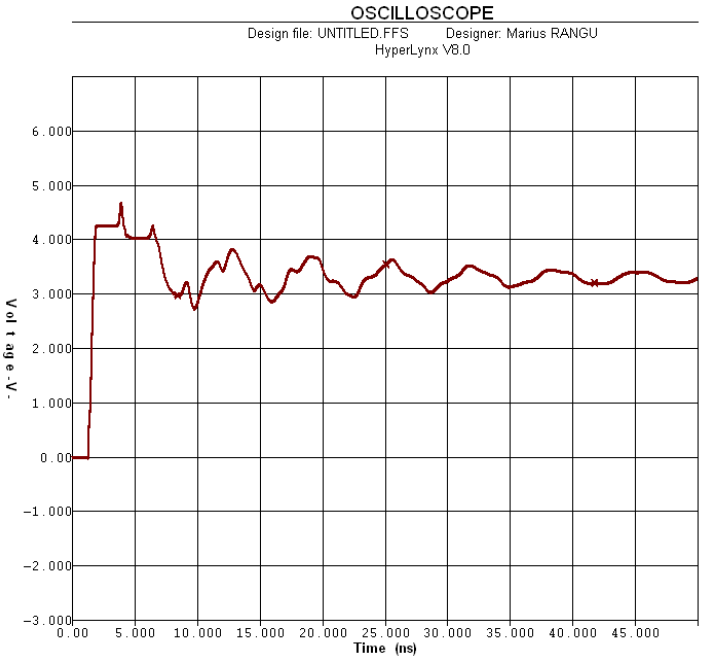

Fig. 4.19 Distortion of a rising edge due to reflections and crosstalk

The flight time is determined by the following parameters:

- Rise time of the signal
- Output impedance of the driver
- Capacitive loading of the line due to the PCB trace capacitance
- Capacitive loading of the line due to receiver ICs package and input capacitance
- Propagation time of the PCB trace

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If the time available for the signal to reach its DC value is much larger than the flight time, then this might not be an issue. If, on the other hand, those are comparable, then the signal should be regarded as a time-critical signal.

It is not easy to accurately predict the flight time of a signal, as it depends on many particular parameters of the PCB and ICs. This can only be accomplished using an electromagnetic field solver and a transmission line simulator able to operate with IBIS models.

A rule of thumb commonly found in literature states that if a signal has a propagation time more than half the clock period associated with that signal, then it should be regarded as a time-critical signal. If one tries to apply this rule in practice, one might find that it is far too permissive: signals may become time-critical at much shorter propagation times. It is so recommended that signals with propagation times greater than 1/10 of the clock period should be regarded as time-critical signals.

2.6.2 Propagation time

One of the main components of timing analysis of high speed signals is the propagation time. This is determined by the PCB trace length and the layer stackup.

The propagation speed of a signal is determined by the properties of the dielectric surrounding the conductor. For stripline routing layers the electric and magnetic fields are completely confined inside the dielectric, which makes the propagation speed constant:

$$v_{stripline} = \frac{11.8}{\sqrt{\varepsilon_r}} \left[\frac{inch}{ns}\right] \tag{4.8}$$

For stripline layers in FR-4, the propagation time is determined only by the trace length:

$$tp_{stripline\_FR4} \approx 0.18\left[\frac{ns}{inch}\right] \approx 7\left[\frac{ps}{mm}\right] \tag{4.9}$$

For microstrip routing layers the electric and magnetic fields are not completely confined inside the dielectric, which make the propagation speed to vary with the distance to the reference plane and trace width. Those variations are however small, so an estimation of the propagation speed in microstrip layers is possible using the equation:

$$v_{microstrip} = \frac{11.8}{\sqrt{0.475 \cdot \varepsilon_r + 0.67}} \left[\frac{inch}{ns}\right] \tag{4.10}$$

For microstrip layers in FR-4, the propagation time is almost constant:

$$tp_{microstrip\_FR4} \approx 0.142\left[\frac{ns}{inch}\right] \approx 5.6\left[\frac{ps}{mm}\right] \tag{4.11}$$

2.6.3 Eye diagram analysis

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Time-critical signals require a thorough analysis of the relation between the flight time and clock period. While the clock period is (almost) constant, the flight time varies with the operating conditions such as the switching pattern and previous signal states. The flight time cannot be accurately predicted using closed-form equations, so a more complex investigation tool must be employed. This is the eye diagram analysis, which can be done prior to layout design, using a transmission line simulator, or after the layout design, using a transmission line simulator integrated with a field solver or through experimental measurements.

The eye diagram presents the waveforms of a time-critical signal measured at the receiver against a mask that defines the forbidden zones, which the signal should never trespass. Multiple signal periods are superimposed on the same mask in order to take into account various operating conditions. Figure 4.20 illustrates the eye diagram.

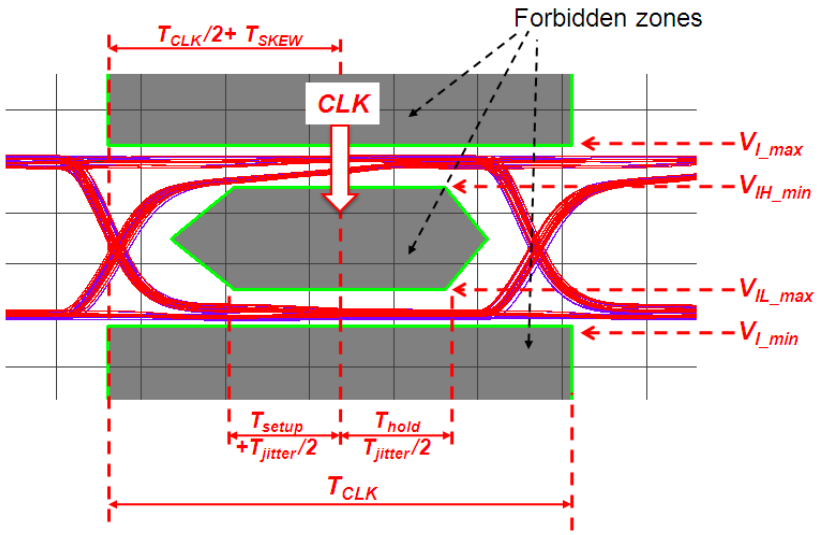

Fig. 4.20 Eye diagram

The eye diagram mask parameters are:

- T_{CLK} = clock period
- T_{SKEW} = the difference between the clock and data propagation time
- T_{JITTER} = clock + data jitter (peak-to-peak)
- T_{SETUP}, T_{HOLD} = setup and hold times of the receiver IC
- V_{I_min}, V_{I_max} = minimum and maximum voltage levels allowed at the receiver input
- V_{IL_max} = maximum voltage level at the receiver input in the LOW state
- V_{IH_min} = minimum voltage level at the receiver input in the HIGH state

An eye diagram analysis should always be performed for critical signals in order to avoid spurious faults during operation.

2.7 Oscillators / Crystals

Cristal oscillators are low-power circuits that are especially sensitive to perturbations. Most such oscillators use an external crystal and an internal amplifier, which requires the crystal-amplifier connections to be routed with special precaution. Those are low amplitude

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analog signals generated by a high impedance source, so they fit perfectly into the definition of a potential victim to crosstalk.

The following recommendations should be followed when placing / routing crystal oscillators:

(i) Place the crystal and the load capacitors as close as possible to the IC oscillator pins of the IC

(ii) Route the crystal – capacitors – IC connections as short as possible

(iii) Route the crystal – capacitors – IC connections as far apart as practical from each other and the ground traces

(iv) Route the ground directly to the GND pin of the IC and only there to the ground of the rest of the circuit (oscillator signals should not share the return path with other signals)

(v) Ground the crystal housing and route a ground loop around the oscillator circuit

(vi) If possible provide a reference plane beneath the oscillator

(vii) Don't route any aggressor signals in the oscillator zone

Figure 4.21 presents an example of placement / routing of a crystal oscillator.

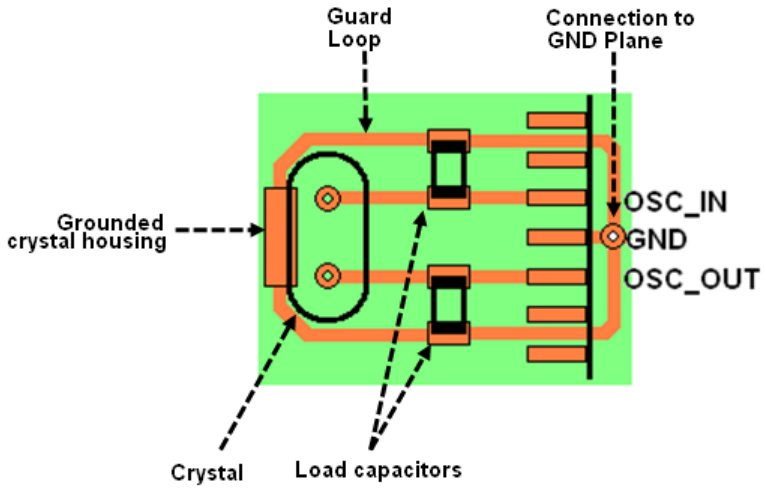

Fig. 4.21 Example of placement / routing of a crystal oscillator

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3. Crosstalk

3.1 Identifying Victims and Aggressors

Rule of Classification for Crosstalk

- ***High amplitude + high frequency + small rise time = Aggressor***
- ***Low amplitude + high impedance = Victim***

The basic rule of minimizing crosstalk

- ***Keep aggressors and victims as far apart as possible and close to the ground.***

Crosstalk is the noise coupled between adjacent conductors through near electric field (capacitive coupling) and magnetic field (inductive coupling). While any adjacent conductors exhibit crosstalk, it is especially detrimental to signal integrity when it appears between aggressive and sensitive signals.

Some signals are particularly sensitive to crosstalk, either because of their nature or their functional role in the circuit. Those signals are potential ***victims*** to crosstalk. Those signals are:

- Analog signals: they are inherently more sensitive to noise than digital signals, so they should always be regarded as potential victims, especially if they have low amplitudes.
- High impedance control signals: Enable, reset, oscillator and feedback signals are the type of control signals that should not be disturbed because of their effect on the functionality of the circuit. If such signals are generated by a low impedance source, such as a high-value pullup / pulldown resistor or a crystal oscillator, they will be easily disturbed by capacitive crosstalk. Such signals should be also regarded as potential victims, especially if they have low amplitudes.

On the other hand, some signals can easily induce noise on potential victims and are considered potential ***aggressors*** with respect to crosstalk. To easily identify potential aggressors, remember that crosstalk is caused by coupling capacitances and inductances between PCB traces. The current injected by a coupling capacitance into a victim trace is:

$$I_C = C_{between\_traces} \cdot \frac{d}{dt}\left(Potential\_difference\_between\_traces\right) \quad (5.1)$$

The voltage induced by a coupling inductance on a victim trace is:

$$V_L = L_{mutual} \cdot \frac{d}{dt}\left(Current\_through\_aggressor\right) \quad (5.2)$$

Based on those considerations, the potential aggressors in a circuit are:

- Signals with high amplitude (either voltage or current)
- Fast signals (either in terms of small rise time or high frequency)

While crosstalk can never be completely avoided, the main task in crosstalk control is to avoid it to occur between potential victims and potential aggressors.

3.2 Layer Assignment

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Hint on layer assignment

- ***Stripline layers are quieter than microstrip layers***

The obvious countermeasure to crosstalk is to keep aggressors and victims as far apart as possible, to avoid coupling capacitances and inductances. The first step in doing so is to avoid routing aggressors and victims on the same layer. If enough routing layers are available, a design rule should be imposed to prevent aggressors and victims to share the same inner layer. Proper system partitioning and zoning should make this precaution unnecessary as aggressors and signals should not be routed in proximity anyway, so layer assignment should be taken into consideration whenever zoning cannot provide complete separation or the application requires very aggressive signals.

A reference plane between routing layers will greatly reduce the crosstalk between signals on those layers, so if possible assign aggressors and victims to different layers separated by at least a ground or supply plane.

Note that crosstalk on stripline layers is smaller than on microstrip layers, so if aggressors and victims must share the same zone and same layer, it should be a stripline layer. Also note that layers closer to a reference plane will exhibit less crosstalk than layers located farther to reference planes, so if crosstalk on the same layer must occur, it is better to allow it on layers closer to planes.

3.3 Orthogonality

Routing on each layer naturally tends to follow a single preferential direction, either horizontal or vertical, because otherwise intersections between traces will occur. This is a practice that should be promoted as it may have beneficial effects on crosstalk. By assigning to each routing layer a single direction and alternate the directions of adjacent layers, both capacitive and inductive coupling can be greatly reduced. This technique is called “orthogonal routing” and is illustrated by fig. 5.1.

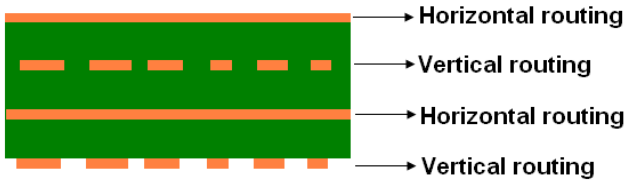

Fig. 5.1 Orthogonal routing

When orthogonality cannot be applied or for the layers with the same routing direction that are not separated by a reference plane, crosstalk can also be reduced by staggering long signal traces, as illustrated by fig. 5.2.

Fig. 5.2 Staggered traces

3.4 Parallelism

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If routing aggressors and victims on different layers is not possible, parallelism restrictions should be enforced. The amount of crosstalk noise between traces routed in parallel depends (among many other things) on the length of the parallel traces and clearance between them. The smaller the clearance, the larger the length that traces are allowed to be routed in parallel for the same amount of crosstalk.

Parallelism between aggressors and victims should be avoided from the first place, but if this is not possible then coupling should be carefully analyzed before enforcing a parallelism rule. As crosstalk depends not just on the parallelism but also on signal, ICs and PCB characteristics, a field solver and a transmission lines simulator should be used to predict the amount of crosstalk noise to be expected for each particular case and to decide on appropriate parallelism restrictions.

A rule of thumb regarding parallelism is called "***The 3W Rule***" and it states that in order to avoid crosstalk between parallel traces routed on the same layer, a minimum spacing between traces centers of 3·W should be kept. Figure 5.3 illustrates the 3W rule.

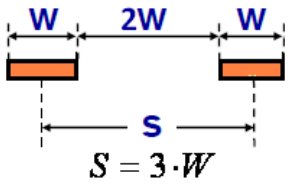

Fig. 5.3 the 3W rule

While crosstalk will be indeed reduced by applying the 3W rule, the actual value is of 3W might be expensive in terms of board space and might not be enough for very aggressive couplings. The 3W rule should be used only if detailed electromagnetic investigations are not available.

3.5 Guarding

An additional measure to reduce crosstalk between parallel traces routed on the same layer is to separate them using a trace connected at both ends to ground, called ***guard trace***, as illustrated by fig. 5.4. It is essential that the guard trace is connected at all ends to ground, otherwise it will behave like an antenna.

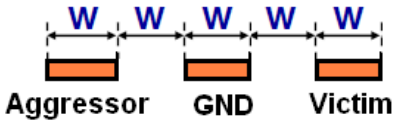

Fig. 5.4 Guarding

Experimental investigations of the guarding techniques suggest that by simply separating the victim to the aggressor in order to make room for the guard trace, the same crosstalk reduction can be achieved even if the guard trace is not present (this is equivalent to a 4W parallelism
rule !). However, a guard traces will also have beneficial effects on the electromagnetic interference of the trace with the surrounding environment, so guarding very aggressive and very sensitive signals is still recommended.

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Notice that guard traces will affect the characteristic impedance and propagation time of signal traces! If applied to controlled impedance traces those effects should be investigated using a field solver and taken into consideration!

3.6 Return paths

Hint on return paths

- ***Currents always return on the path of least impedance. Keep the return path close to the signal path and avoid aggressors and victims sharing the same return path.***

All currents return to the source that generated them through the ground connection (DC) and also through the voltage supply connection (AC). The return path is always the path of least impedance, which in DC means „least resistance" and in AC means „least inductance". The resistance is determined mainly by the width of the return trace and the inductance mainly by the signal-reference loop area. Figure 5.5 illustrates the return paths in AC and DC.

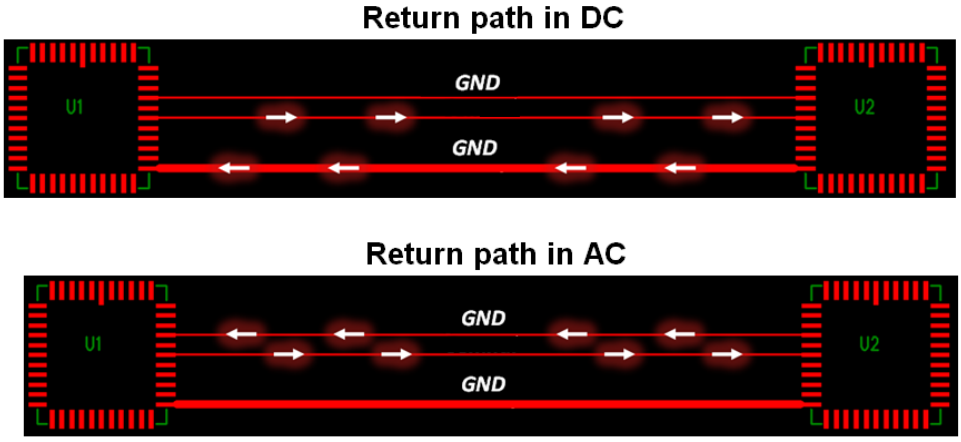

Fig. 5.5 Currents return on the path of least impedance

The signal-return loop should be kept as small as possible in order to avoid large self and mutual inductances, which increase crosstalk. Special attention to return paths should be paid for:

- High speed signals: the return path should be kept constant along high speed traces in order to maintain their impedance constant
- Potential aggressors and victims: they should be routed close to the return path, otherwise the signal-return loop will behave like an antenna, receiving and radiating electromagnetic waves. Also aggressors and victims should not share the same return path !

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3.7 Receiver Placement

Hint on receivers placement

- ***Receiver ICs location with respect to the aggressor drivers greatly influences how they are affected by crosstalk noise. A thorough investigation is required in order to identify the optimum placement.***

Crosstalk between high speed signals has different effects at the ends of the victim trace, because it will not behave as an equipotential connection but as a transmission line. The end of the victim line that is closer to the aggressor driver is called the "near end" and noise measured here is called ***NEXT*** ("Near End Crosstalk"), while the end of the victim line that is farther to the aggressor driver is called the "far end" and noise measured here is called ***FEXT*** ("Far End Crosstalk"). This naming convention is illustrated by fig. 5.6.

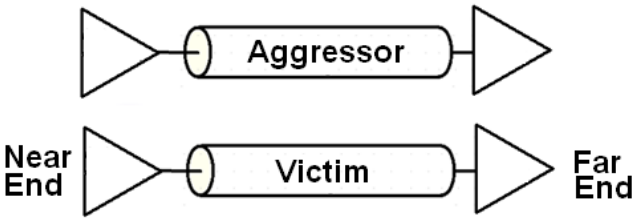
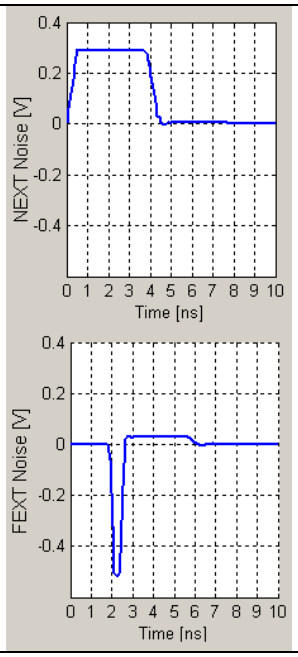


Fig. 5.6 Near and far ends of the victim line

The NEXT noise is caused by capacitive and inductive coupling currents traveling in the same direction, while the FEXT noise is caused by capacitive and inductive coupling currents travelling in opposite directions. The NEXT noise will begin as soon as the aggressor signal switches, while the FEXT noise will begin only after the propagation time of the victim line. Terminations at the ends of the victim and aggressor line also influences how the crosstalk will manifest at each end. Figure 5.7 summarizes the typical waveforms that should be expected for two microstrip coupled lines when the aggressor driver launches a rising edge.

Victim line terminated at both ends		• NEXT duration = twice the propagation time • NEXT amplitude doesn't depend on coupling length • FEXT amplitude proportional to coupling length

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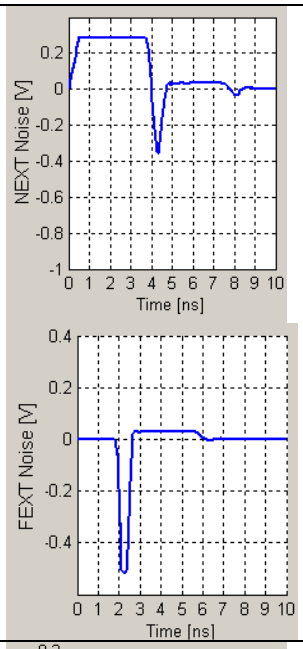
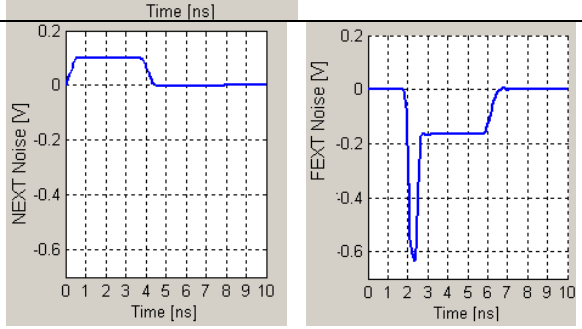
Victim line terminated at near end only		• NEXT pulse is followed by a pulse identical to the FEXT of a line terminated at both ends • FEXT amplitude doubles as compared to a line terminated at both ends
Victim line terminated at far end only		• NEXT pulse has half the value it would have if the line was terminated at both ends • FEXT amplitude doubles as compared to a line terminated at both ends • FEXT pulse is followed by a pulse identical to the NEXT of a line terminated at both ends, but with opposite polarity

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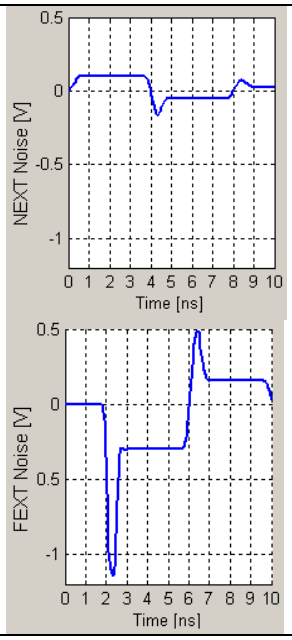
Victim line un-terminated at both ends		• NEXT pulse has half the value it would have if the line was terminated at both ends • Pandemonium at the far end due to multiple reflections

Fig. 5.7 Typical crosstalk noise for microstrip coupled lines

Figure 5.8 illustrates the dependency of the NEXT and FEXT noise to the coupling length, for both microstrip and stripline configurations when both the aggressor and victim lines are terminated at both ends.

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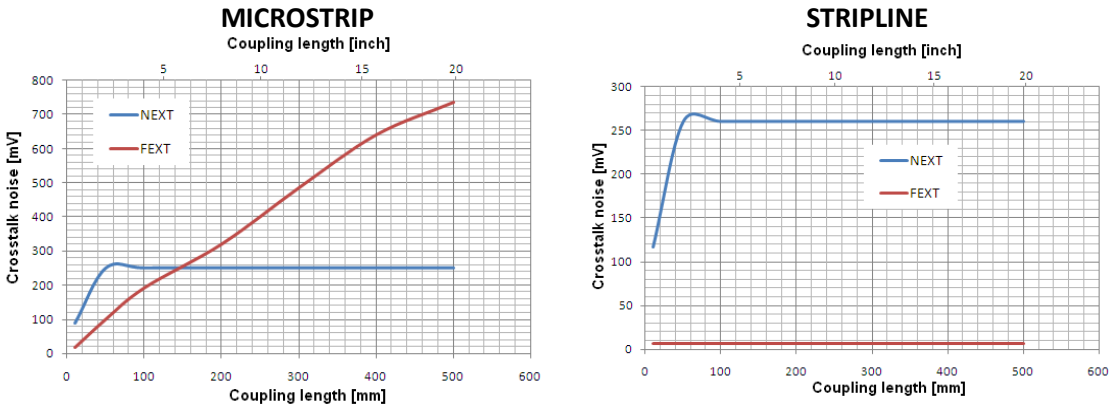

Fig. 5.8 Crosstalk noise for tightly coupled parallel traces

Since the capacitive and inductive coupling currents travelling towards the far end of the victim line have opposite polarities, FEXT noise might cancel if they are equal. This is the case for stripline traces, which do no exhibit FEXT noise. Note though that if the victim line is un-terminated at the near end, the far end will exhibit noise even in stripline configuration due to reflections.

Crosstalk should not be allowed to generate noise at the input of signal receivers, at least not beyond their noise margin. Signal drivers on the other hand are not sensitive to crosstalk noise, which in general does not reach amplitudes high enough to damage the IC. From the previous considerations it can be seen that the location of the receiver circuit with respect to the aggressor driver, the layer configuration and the termination type greatly influences the way crosstalk will affect the receiver. For point-to-point interconnects the optimum placement of the receiver can be deduced from a simple analysis based on the data presented in fig. 5.7 and 5.8. For multi-point interconnect topologies the optimum placement of the receivers with respect to aggressor drivers can be deduced using a transmission line simulator.

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4. EMC Considerations

4.1 General Considerations

The electromagnetic compatibility (EMC) represents the ability of equipment to operate in an electromagnetic environment without interfering with other equipment above certain regulated limits. EMC has two components:

- Emission – the generation of electromagnetic energy by the equipment
- Immunity – the ability to operate correctly in the presence of electromagnetic energy emitted by other sources

To receive an EMC compliance certification, the equipment must provide low emission and high immunity according to current regulations.

There is no strict distinction between signal & power integrity and electromagnetic compatibility issues, as both deal with electromagnetic interference (EMI); if signal & power integrity is concerned with interference within the different parts of a product, EMC deals with interference between the product and the external electromagnetic environment. Good signal & power integrity practices, as those presented in the previous chapters, also have a beneficial effect on the electromagnetic compatibility. This chapter explains some guidelines that are more specific to emission and immunity, with the provision that for good EMC it is also necessary to fulfill the requirements specific to power supplies, grounding, high speed and crosstalk.

4.2 Components

Hint on component selection

- ***Always choose the slowest components that satisfy the application requirements. Favor SMD over THD.***

Hint on analog bandwidth

- ***If application allows, reduce the analog bandwidth of high speed signals using low pass filters placed near the signal generator***

Hint on unused pins

- ***Connect unused input pins to a DC potential (VCC or GND)***

Hint on heatsinks

- ***Ground the heatsinks using multiple connection points distributed on the perimeter***

The analog bandwidth of the signal is determined by its frequency content for analog signals and rise time for digital signals (see effective frequency in paragraph 6.2). The higher the bandwidth of the signal, the higher the electromagnetic emission and lower the immunity will be. Depending on the application specifics, the entire analog bandwidth might not be required and EMI problems will be generated without any functional benefit. As a consequence, the analog bandwidth should be limited to the minimum required by the application, or conversely the rise time should be increased to the maximum allowed by the application. This can be accomplished by an appropriate choice of ICs and by filtering.

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4.2.1 Component selection

Depending on their function, analog and mixed signal ICs may have a "speed" specification expressed as maximum operating frequency, sampling rate, bandwidth or slew rate. Digital ICs may have a "speed" specification expressed as maximum operating frequency or typical rise time. The speed at which an IC can operate should be slightly higher than the application requires it.

The package of the component also has influence of its behavior at high frequencies, because of the parasitic capacitance between pins and their self and mutual inductances. It is recommended to use exclusively surface mount packages for all the high speed components.

4.2.2 High speed filters

Another way to restrict the analog bandwidth of high speed signals is by using low-pass filters to remove the high frequency content. This can be accomplished using R-C filters connected in close proximity to the signal source, as illustrated by figure 6.1

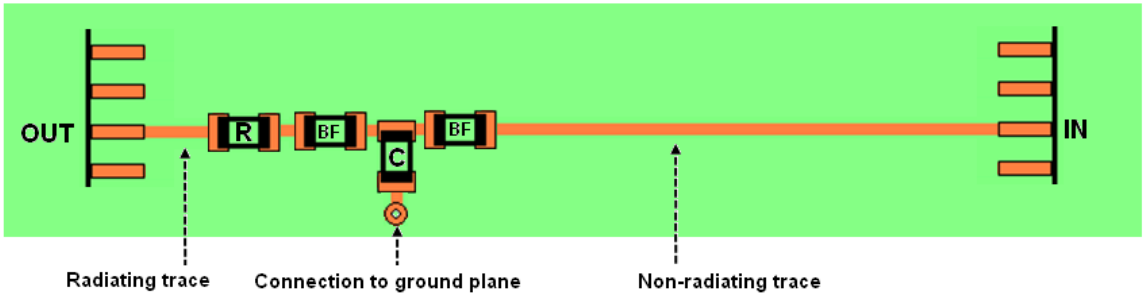

Fig. 6.1 Optimum filtering of high-speed signals

This configuration can be used in conjunction with a termination, by using the series termination resistor as the resistive component of the low-pass filter. SMD ceramic capacitors on small packages are the most suitable for high-frequency filtering because of their low impedance at high frequency. Three-terminal capacitors should be used for low-impedance drivers, as they have two series inductances that form with the capacitor a "T" filter. To further improve EMC performance, bead ferrites can be connected near the filtering capacitor.

The common mode radiation of differential signals can also be attenuated using common mode chokes.

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4.2.3 Unused pins

Unused input pins should not be left floating, as they might oscillate due to electromagnetic interference and increase the dynamic supply current. Unused input pins should be connected to a DC potential, either VCC or GND.

Unused output pins should be left unconnected

Unused bidirectional pins should be configured as inputs and connected to VCC or GND. If they cannot be permanently configured as inputs they should be connected to VCC or GND using a high value resistor. Note that this resistor will act as a pullup or pulldown when the bidirectional pin is configured as input and as a load when the pin is configured as output, so it will determine the current sourced / sunk by the IC.

4.2.4 Heatsinks

Heatsinks are large metallic objects that may be energized to a high frequency potential caused by:

- Galvanic connection to a switching potential, such as the drain or source of a power MOSFET
- Parasitic capacitance to a noise source such as a high-frequency IC

While galvanic connection to a high-frequency switching potential can be avoided by electrically insulating the heatsink to the component, the insulation foil must be thin for good thermal transfer so a high capacitive coupling will still occur. If the heatsink is allowed to become energized at a high frequency potential it will generate electromagnetic radiation. Furthermore, if the heatsink is close to the walls of a metallic enclosure, it will energize it through the parasitic heatsink-enclosure capacitance, increasing the radiation level. To avoid this, a few countermeasures should be considered:

(i) Isolate heatsinks from switching potentials

(ii) Keep heatsinks away from high-frequency signals

(iii) If *(ii)* is not possible, ground the heatsink using multiple connections point distributed on the perimeter or a continuous conductive gasket.

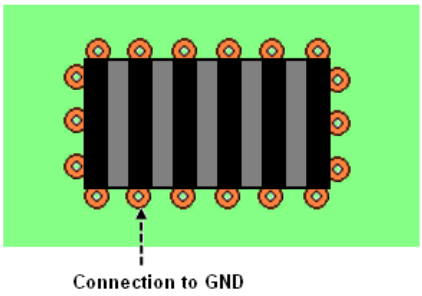

Fig. 6.2 Multi-point grounding of a heatsink

4.2.5 Shielded components

Some components such as RF communication modules or LCDs are manufactured with a shield, either to protect sensitive internal signals against external perturbations or to prevent excessive radiation from the module. In such cases, the shield should be grounded in multiple points distributed on the perimeter, in a way similar to heatsink grounding.

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4.3 Power Supply

Hint about mains voltage

- ***Keep the mains voltage hidden from the rest of the circuit i.e. electrically and proximity***

Hint on routing SMPSs

- ***Minimize the high switching current loop lengths***
- ***Use multiple vias to power plane to reduce series inductance***

4.3.1 Mains

The mains supply is the primary way of conducting perturbations in and out electronic equipments and should be considered a potential aggressor. Although the mains should in principle have a predictable waveform and frequency spectrum, and thus be easy to take countermeasures, in practice the mains may have a much wider bandwidth caused by:

- Voltage distortion
- Transients caused by various loads switching
- Power line communication (PLC) that my share the same network

The primary protection against such conducted perturbations is the mains filter, illustrated by fig. 6.3. It should be connected as close as possible to the mains connector and prior to the mains switch.

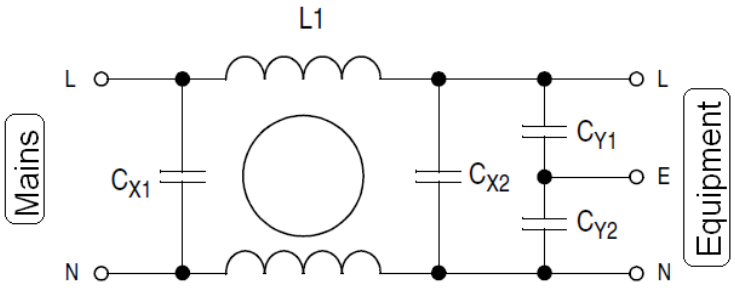

Fig. 6.3 Mains filter

Besides conducted radiation, the relatively high voltage of the mains generates low frequency electric fields that can couple to the rest of the circuit. To avoid this, parasitic capacitances between any conductor at the mains potential and the low-voltage circuit (including ground and chassis) should be avoided. If close proximity between the mains circuit and potential victims cannot be avoided, an electromagnetic shield should be considered.

4.3.2 Voltage regulators

Voltage regulators must not just provide a specific voltage level but also to eliminate any spectral component other than DC. To accomplish this it is mandatory to use filtering capacitors both at the input and output and to follow some specific design recommendations:

- Use two filtering capacitors, a large one for low frequencies and a small one for high frequencies

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- Place the small input filtering capacitor next to the low voltage entry point (transformer or connector)
- Use a short ground connection between the small input filtering capacitor and low voltage entry point ground. This is necessary to reduce at minimum the high frequency input current loop
- Place and route the components such that the input current follows this current path: entry point → small capacitor → large capacitor → voltage regulator → small capacitor → large capacitor → supply distribution. If a VCC plane is used, the regulated voltage should be connected to the plane only after the final capacitor. Figure 6.4 presents an example of placement and routing for such a current path.

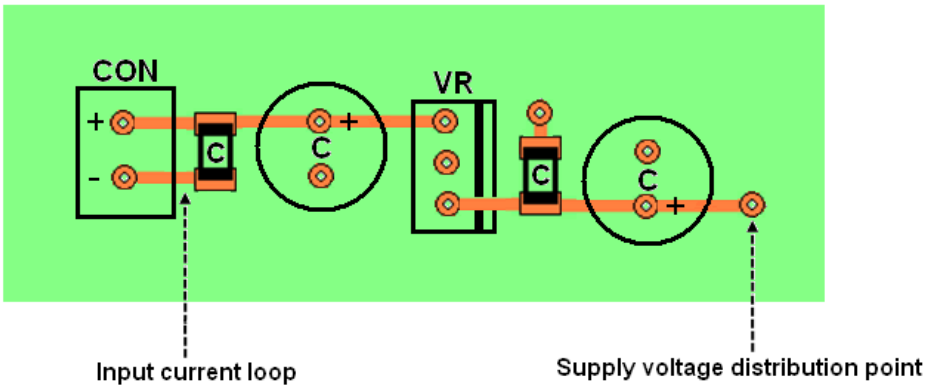

Fig. 6.4 Example of voltage regulator placement / routing

- Use a low-impedance ground connection (GND plane or wide traces)

If no voltage regulator is present on the PCB, the input filtering capacitors should still be present and placed and routed as presented above.

4.3.3 Switching mode power supplies

Switching mode power supplies requires special precautions because of the high di/dt ratio that generates radiated perturbations. As the switching frequency and load current increases, more radiation should be expected. While each SMPS topology requires a specific analysis, some considerations are general:

- Group all the SMPS components as tight as possible
- Minimize the loop of high di/dt currents
- Use a small ground recovery loop
- Use a local star ground separated from the ground of the rest of the circuit
- Consider connecting the ground point of the SMPS to the ground of the rest of the circuit through a ferrite bead.
  Figure 6.5 illustrates the current loops for a buck converter.

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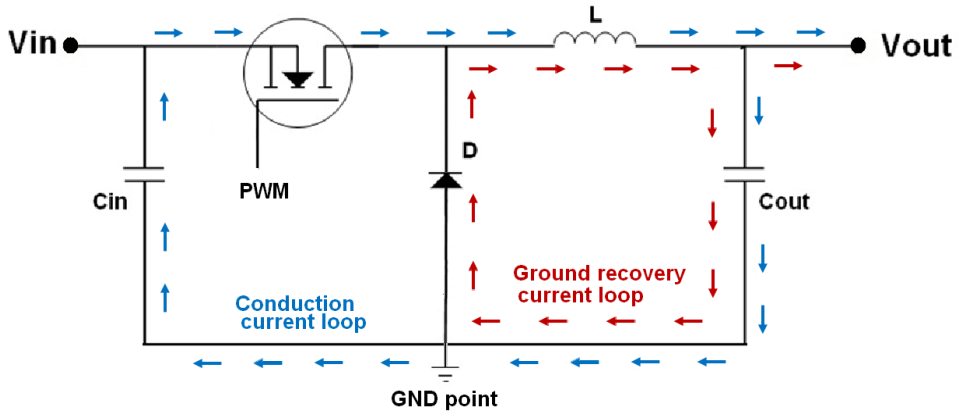

Fig. 6.5 Current loops for a buck converter

4.4 Routing

Hint about clock distribution

- ***Clock traces should always be located close to ground***

Guarding mythology

- ***Guarding is no silver bullet – don't expect it to perform miracles!***

Hint on stubs

- ***Stubs = antennas, avoid them at all times!***

4.4.1 Clock distribution

The clock signal is usually one of the main causes of emitted radiation, for several reasons:

- It probably has the highest frequency in the circuit
- It has a rectangular waveform, meaning a high bandwidth
- It usually reaches a large number of ICs, so the clock traces are long

For those reasons, the clock should be distributed carefully in order to avoid creating radiating loops. Some basic recommendations should be followed:

- Reduce the fanout of the clock generator using buffers, in order to reduce the current travelling on the clock traces
- Use series termination at the clock generator, in order to further reduce the current travelling on the traces
- Route the clock traces in close proximity to the ground on their entire length (over a ground plane or using guard traces), in order to reduce the area of the radiating loop
- If possible route the clock traces on stripline layers, which can provide shielding and reduce radiation
- Avoid routing the clock traces near the edges of the board

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4.4.2 Guarding

Guarding high-bandwidth signals is considered to be a major contributor to the reduction of electromagnetic interference. However, experimental measurements proved that it can only provide moderate attenuation of emissions, which usually don't justify the board space required.

Guarding can be implemented in several ways, illustrated by fig. 6.6

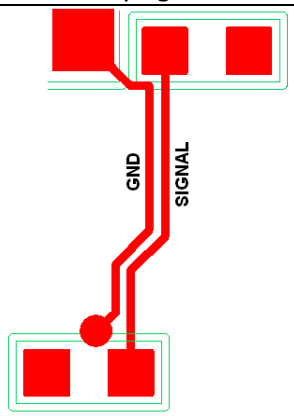
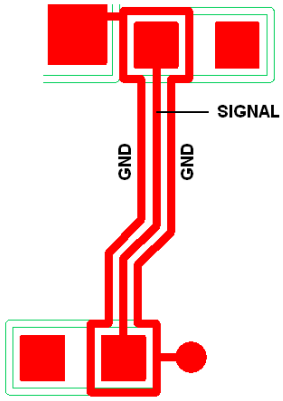
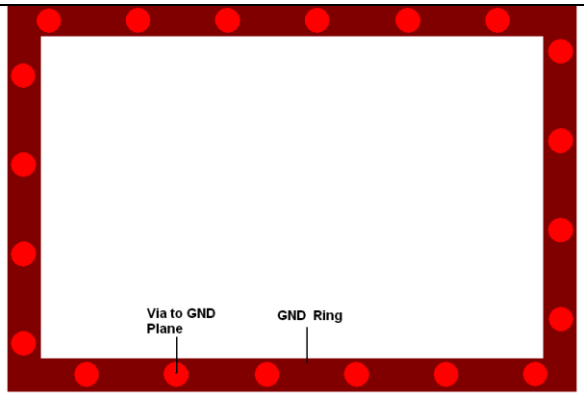
Guard trace • The GND trace should run in parallel to the signal trace • The GND trace should be connected to ground at both ends	
Guard loop • A GND trace should create a loop around the signal trace • The GND trace should be connected to ground at both ends	
Picket fence (Faraday Cage) • A guard ring should be routed on the perimeter of the board or a zone • The ring should be connected to a ground plane (or a ground ring on another layer) using multiple vias • The maximum distance between vias should be 1/10 of the wavelength of the maximum frequency content of the guarded signals	

Fig. 6.6 Guarding techniques

While proper guarding cannot hurt in terms of electromagnetic interference, it should be only used as a last resort. Not generating electromagnetic radiation in the first place is better than trying to contain it.

4.4.3 Stubs

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Stubs are segment of a trace or via that are not on any current path. Figure 6.7 illustrates the types of stubs that can be accidentally created on a PCB.

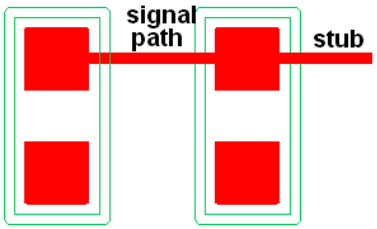
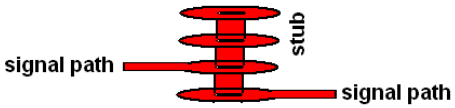
Trace stub = a segment of trace unconnected at one end	
Via stub = a via that is not on the signal path on its entire height	
Test point stub = a test point that is routed apart from the signal trace (not on the signal path during normal operation)	

Fig. 6.7 PCB Stubs

Stubs are antennas. Depending on the frequency content of the signal, the stub length and dielectric properties, it might be a very good or a poor antenna. It is not easy to decide whether a stub will cause EMI problems without an electromagnetic field simulator, so stubs should be avoided at all times. If via stubs cannot be avoided for reasons dealing with the PCB manufacturing technology, their number on high speed signals should be kept to minimum.

4.5 System design

Hint on chassis grounding

- ***Chassis ground should be connected to signal ground at a single point***

Hint on cables and connectors

- ***Cables and connectors should be segregated according to the signal***

4.5.1 Chassis grounding

If the equipment will be installed in a conductive housing (chassis), this should be connected to the ground potential to provide shielding against electromagnetic interference. The chassis ground should not be connected directly to the signal ground, as it might induce high frequency noise. The best practice is to use a discontinuous chassis ground around the edges of the board, connected to the chassis through the mounting holes, as illustrated by fig. 6.8. The PCB chassis ground should be discontinuous in order to avoid creating a loop antenna.

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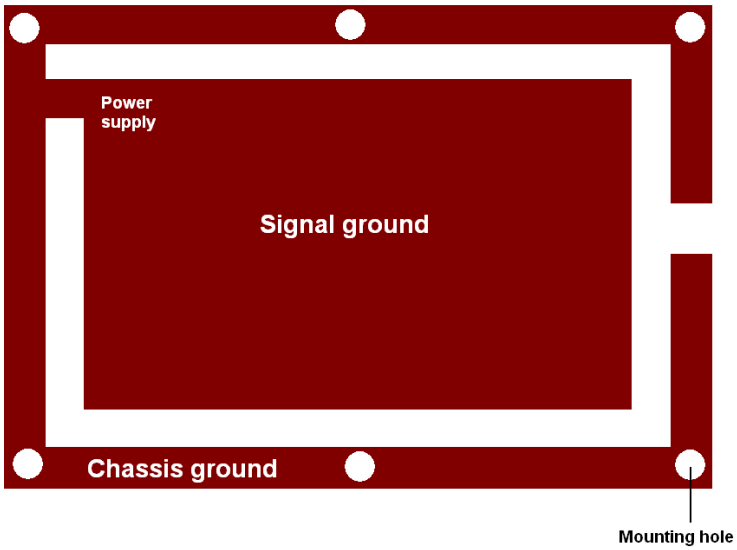

Fig. 6.8 Multi-point chassis grounding

If protection of the electronics against potential high-current discharges through the chassis ground is a concern, perhaps because the chassis ground is earthed to protect the human operator, than the connection signal-chassis ground should be made through a capacitor instead of a conductor. Typical values for this capacitor range between 10 [nF] and 100 [nF]. This will allow high-frequency currents to pass between the grounds, so that the chassis will still provide shielding, but will prevent high current discharges through the signal ground.

If such grounding is not possible then a star point grounding should be used, with a single connection between the signal and chassis ground, near the power supply of the circuit. If this is the case then mounting holes should be left unconnected. Capacitive coupling should again be considered if the chassis ground is earthed.

4.5.2 Cables

Cables should be classified according to the characteristics of the signals they carry, in order to decide on the proper cable layout and connector placement. Cables of any class are recommended to be provided with a ferrite on each end. Shielded cables should have the shield grounded at both ends.

Type	Typical Usage	Recommendation
Class 1: Sensitive	Low level analog signals generated by high impedance sources	Use shielded cables Use twisted pairs for differential signals Use a single cable for each signal Use ferrite
Class 2: Slightly sensitive	Medium level analog signals, low speed digital signals	Use shielded or twisted pair cables
Class 3: Slightly noisy	DC Power, high level filtered analog signals,	
Class 4: Noisy	Mains, high speed digital signals, high level unfiltered analog signals, switched loads	

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Cables should be as short as possible and their layout should be designed such that they are in close proximity to a parallel earth conductor (PEC), which should have a low resistance and be connected to earth at all ends. The main purpose of the PEC is to divert any discharging currents away from the cable shielding.

The cables should not be bundled and should provide and a large clearances between dissimilar class cables should be provided. Figure 6.9 presents some recommendations regarding the minimum clearance between cables, according to their class.

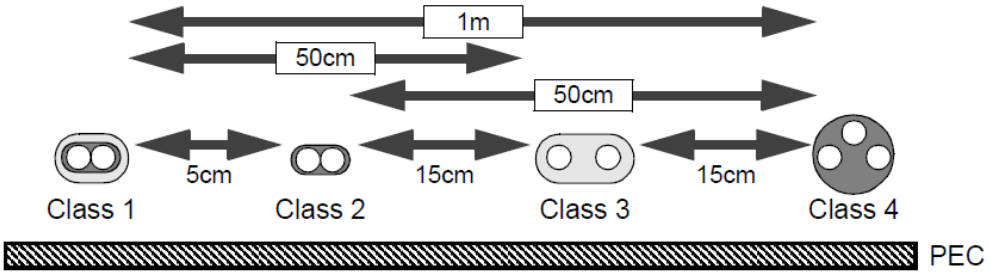

Fig. 6.9 Minimum clearance between cables

4.5.3 Connectors

Connector placement enables or disables the appropriate cable clearance, so it should also take into account the signal classes presented in the previous paragraph. Furthermore, connectors should be considered as part of the functional block containing the signals carried by the cable and placed on the PCB accordingly (see paragraph 6.5 on placement). Connector placement might be also restricted by mechanical consideration, so an appropriate planning should be done during system design.

As noise might be coupled on the cable, it is important to place signal filters in the close proximity of the connector (see paragraph 6.3.2 on filters). A large low-impedance ground should be provided at least in the connector – filter area, using a ground plane (or at least a local ground island if not possible) and grounding as many pins as possible.

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4.6 ESD & Safety

4.6.1 Connectors

Hint on ESD protection

- ***Where possible, provide a transient suppressor for each signal destined for the outside world via a connector***

Static electricity can accumulate on human operators and equipment and discharge through the ICs with destructive effects. The most dangerous discharge path is through direct contact and the parts of a circuit most likely to suffer from electrostatic discharges (ESD) are the ones available outside the enclosure, through connectors. The discharge pulse may have an energy of tens or hundreds of mJ, while most ICs can only withstand several mJ, so additional protection is required. Figure 6.10 illustrates a typical discharge pulse according to the human body model (HBM).

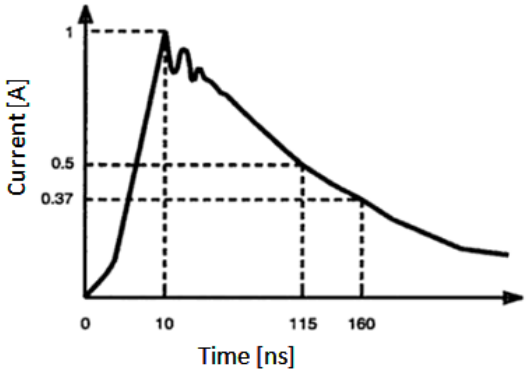
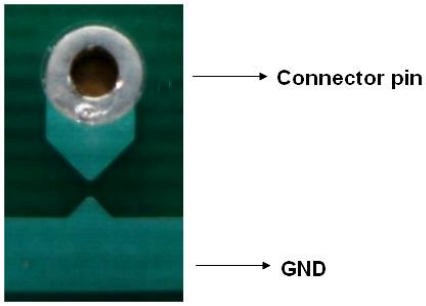


Fig. 6.10 Typical HBM discharge pulse

The transient suppressors are components added to the circuit specifically to divert the ESD pulse away from the sensitive ICs. The following suppressors can be used:

Suppression Type	Typical Implementation	Pros and Cons
Spark gaps		• The gap between the sharp tips should be 0.1 … 0.6 [mm] • Low cost • Long response time • Discharge threshold depends on pressure and temperature and can change in time

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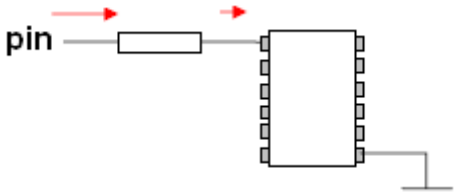
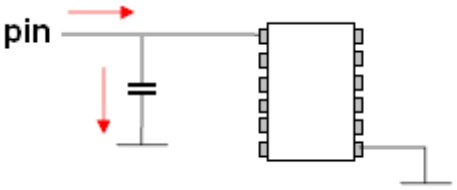
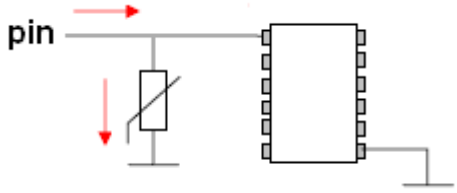
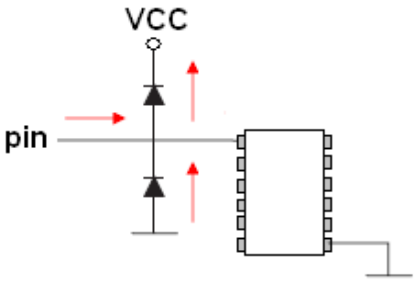
Resistor		• The resistor reduces the amplitude of the ESD pulse • Can't divert ESD pulse to ground
Capacitor		• The capacitor diverts the ESD pulse to ground and away from the IC • The capacitor value should be 1…100 [nF] • Response time: tens of [ps]
Varistor		• Can discharge high currents • Response time: hundreds of [ps] • Higher cost
TVS Diode		• Keeps a low voltage at IC pin • Fast response time • Higher cost • Most digital ICs already have integrated TVS diodes, but the ESD pulse must be diverted at the entry point to prevent discharge to adjacent traces

Regardless of the suppressor type used, it should be located near the connector pin. Furthermore, the signal should not be routed directly from the connector pin but from the transient suppressor. Figure 6.11 illustrates poor and good routing of a signal from the connector.

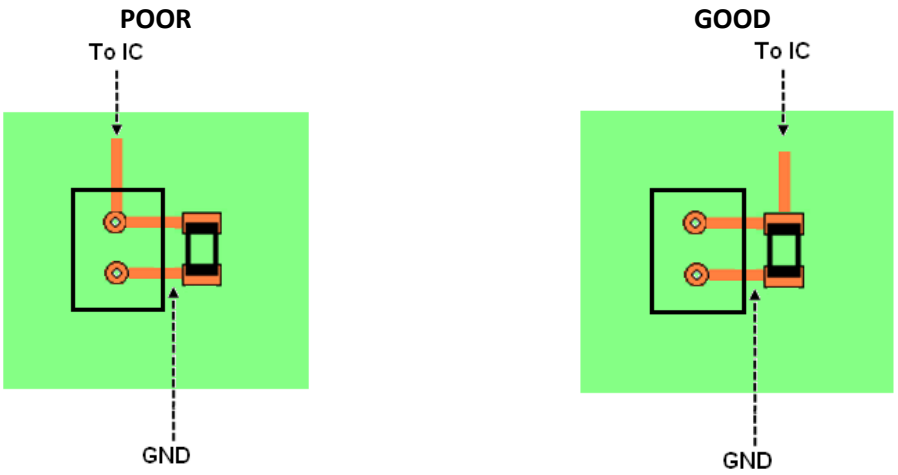


Fig. 6.11 Poor and good routing of the transient suppressor

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4.6.2 Sensitive pins

Many programmable devices such as microcontrollers and FPGAs use the reset pin to supply the voltage required for in-circuit programming, a voltage that is usually higher than the supply voltage. Some output pins might not be driven by a push-pull driver but using an open drain configuration. Some input pins of low-voltage devices are tolerant to higher voltage (for instance ICs powered by 3.3 [V] might be 5V-tolerant).

This prevents the integration of a clamping diode to VCC, making such pins more sensitive to ESD discharges. Figure 6.12 presents an example of the ESD protection for the Reset pin, integrated into the IC.

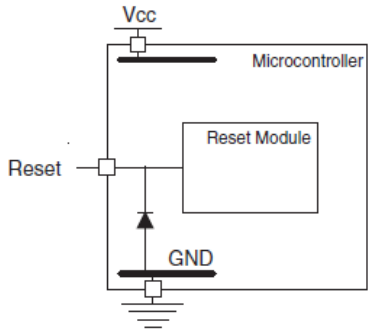

Fig. 6.12 Typical Reset pin ESD protection

Also pins that don't have integrated ESD protection and are pulled up or down by high value resistors are sensitive to discharges.

Such pins require special precaution regarding placement and routing:

- Should not be located or routed near the board edge
- Should not be located or routed near the chassis ground
- Should not be located or routed near conductive mounting holes
- Should be provided with some external transient suppressor.

If in-circuit programming (ICP) is not used in the application, an external diode should be provided external to the IC, between the Reset pin and VCC pin. If the in-circuit programming is used then such a diode cannot be added and the only protection available is the transient suppressor connected near the ICP connector. Even if ICP is not used, a capacitor is recommended to be placed on the Reset line near the IC pin, to provide filtering and avoid spurious system reset.

4.6.3 High Voltage

If the circuit operates with high voltages, those can present a danger to the human operator. It is considered that voltages higher than 40 [V] can represent a danger for the human body, so voltages higher than 40 [V] should be regarded as "high voltage". In such cases it is mandatory to connect any metallic part that can be touched by the personnel to earth. Applicable safety regulations should be followed.

Circuits operating with high voltage require additional precautions regarding the clearance between conductive parts that can have different potentials, in order to prevent discharges in air or dielectric. This is applicable to PCB copper clearances and also to clearance between PCB copper and other metallic parts (components, chassis, etc). The minimum clearances depends on layer (internal / external), coating and elevation, and are detailed in the IPC-2221 standard, pp. 39-40. For voltages lower than 15 [V] (DC or AC peak) the minimum

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clearance is below the minimum clearance restricted by common PCB manufacturing processes, so no special precautions are required.

5. Design for Test

5.1 Test Points

In order to allow the electrical testing of the finished PCB assembly, some or all the signals should be provided with test points. The following features may be used as test points:

(i) ***Vias:*** not recommended for several reasons. First, this will prohibit changing the via locations during an eventual design review, because changing via locations will require rebuilding the test fixture, with additional costs. Second, test probes can be trapped and break in the via holes, so vias must be filled with solder. Third, vias used as test points cannot be located under components, which is an additional design restriction.

(ii) ***Dedicated test pads:*** this is the recommended choice. Test pads should be round SMT pads, either with a minimum diameter of 35 [mils] located on a 100 [mils] or 75 [mils] grid, or with a minimum diameter of 40 [mils] located on a 50 [mils] grid.

IPC recommend the following clearances for test points:

- 20 [mils] to any other conductor
- 40 [mils] to small components
- 200 [mils] to tall components that require milling in the test fixture

The exact clearance requirement might be different from a manufacturer to another. If test pad size and clearance recommendations are not available from the PCBA manufacturer, the IPC values should be used.

Test points should be distributed evenly on the PCB, to prevent flexing caused by the mechanical action of the test probes. The test point density should not exceed 100 / inch^2 for mechanical fixtures or 25 / inch^2 for vacuum fixtures, unless specified otherwise by the PCBA manufacturer.

It is highly recommended to place test points on a single side of the PCB, as double side test fixtures will increase cost. If this is possible then all the test points should be located on the side unpopulated with tall components.

5.2 Tooling Pins

For a precise registration of the PCB with the test fixture, two or three tooling pins are used, placed assymmetrical on the corners of the board, as illustrated by figure 7.1.

Fig. 7.1 Location of tooling pins

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Two or three unplated holes should be provided for the tooling pins. The diameter of the holes depends on the diameter of the tooling pins used by the manufacturer of the test fixture, and is usually 3 [mm] or 125 [mils]. A minimum clearance of 100 [mils] to the edge of the board should be used. If no specific requirements are available from the PCBA manufacturer, the above recommendations should be used in the checklist. The holes for the tooling pins should be marked explicitly on the mechanical drawings.

5.3 Push fingers

If a mechanical test fixture will be used, push fingers required to press the PCB against the probes. Component-free areas should be distributed evenly across the board, on a 1.5 … 2 [inch] grid, to allow push finger to make contact with the board. The component-free areas should have 150…200 [mils] in diameter, unless specified otherwise by the PCBA manufacturer. The push finger locations should be explicitly marked on the mechanical drawings.

5.4 Sealing

Vacuum test fixture to not use push fingers but require some precautions regarding sealing to prevent loss of air pressure:

- Components should have a minimum clearance of 150 [mils] to board edges to prevent damage to the sealing gasket.
- All holes should be covered with solder or by the solder mask
- It is recommended that the board has a rectangular shape to reduce test fixture cost.

5.5 AOI

To allow an automated optical inspection (AOI) of the solder joints at the end of the assembly process, tall components should not be placed close to soldering pads in order to prevent the obstruction of the viewing line of the camera. The minimum clearance around tall components (X) depends on the height of the component (Y) and the viewing angle of the camera (α) and can be calculated as:

$$X \geq Y \cdot \cot \alpha \qquad (7.1)$$

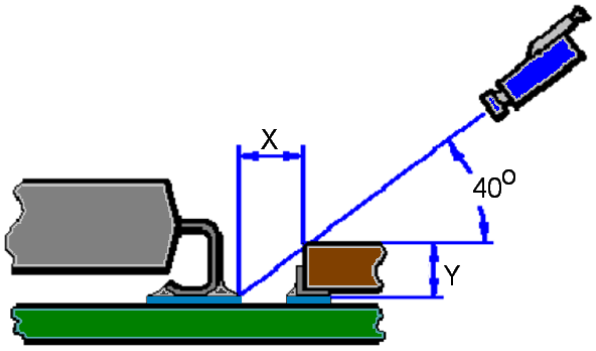

Fig. 7.2 Viewing angle of AOI camera

Additionally, the solder mask should be mat to prevent excessive light reflection. With white solder mask AOI capabilities are limited.

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6. Design for Manufacture

6.1 Stackup

6.1.1 Symmetry

Typical PCBs are manufactured by laminating pairs of copper foils on both sides of a core, through intermediate prepreg dielectrics. This process is illustrated by figure 8.1.

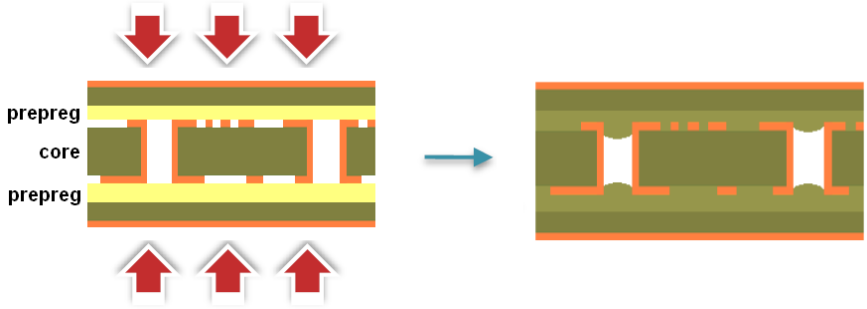

Fig. 8.1 PCB Lamination process

To allow such a manufacturing process, the designed stackup should be symmetrical to the core. However, PCBs may be manufactured using multiple cores or build-up technology, which does not necessary require stackup symmetry. Check the manufacturing specifications upon deciding if an asymmetrical stackup is allowed.

6.1.2 Drill pairs

Depending on the PCB manufacturing process one or more drill configurations might be available. The restriction comes from the order of PCB manufacturing operations, which determines drilling pairs. Only vias between the layer pairs that can be physically drilled are allowed. In the figure below a 6-layer PCB is manufactured using two cores, which leads two the following drill pairs:

- Layer 2 – Layer 3 (from manufacturing of the upper core)
- Layer 4 – Layer 5 (from manufacturing of the lower core)
- Layer 1 to Layer 6 (final drilling after stack lamination)

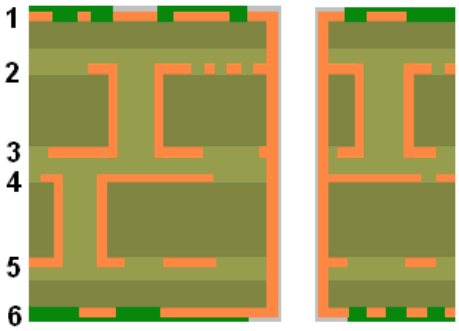

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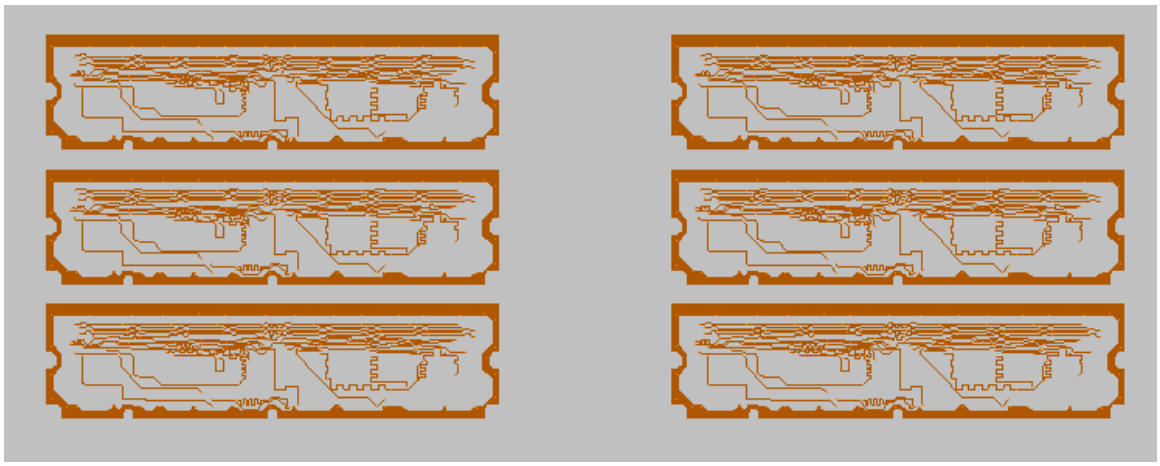
Fig. 8.2 Example of a PCB with two cores and three drill pairs

The aspect ratio of each pair (height / diameter) determines the minimum hole size that can be plated. This information should be provided by the PCB manufacturer.

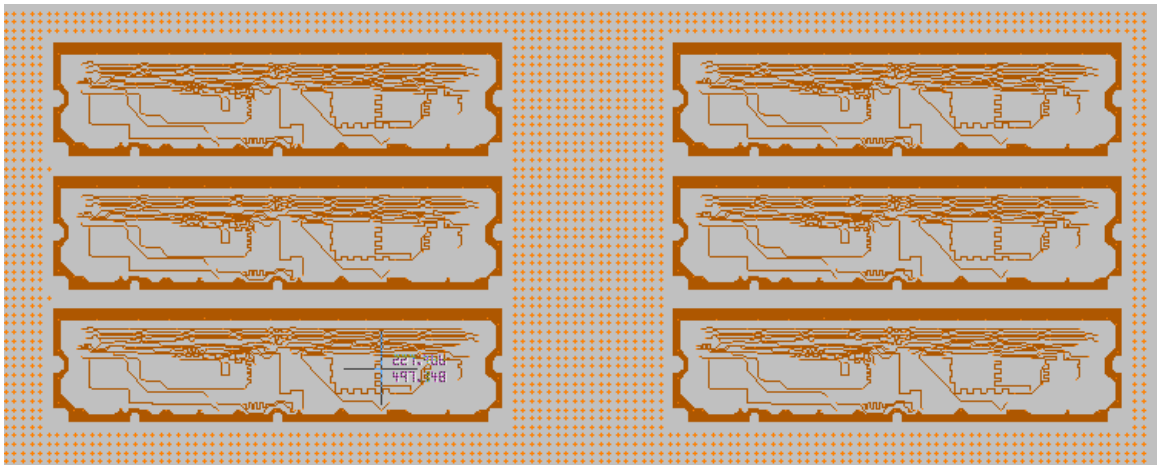
6.1.3 Copper balance

During the lamination process, the board can warp and the layers may lose alignment if the local copper density is not uniform on the entire surface of the board. To prevent this, on each inner layer the areas free of traces / pads should be covered with copper on a dot or hatched pattern (other options are available). It is not recommended to design copper balancing using continuous copper as this will prevent the flow of resin during high temperature lamination and may cause warp. Figure 8.3 presents a few examples of copped balancing.

UNBALANCED



DOT BALANCED



HATCH BALANCED

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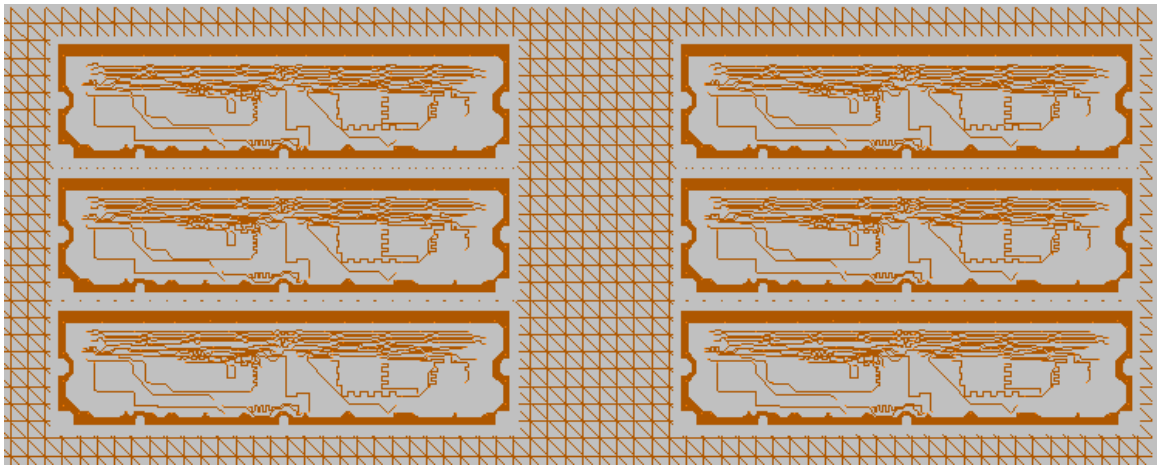

Fig. 8.3 Examples of copper balancing

6.2 Design Rules Check

6.2.1 Clearance

Minimum clearance between copper features on a PCB layer is restricted by the PCB manufacturing process. The clearance is measured between the outer edges of traces, pads and graphics, as illustrated by fig. 8.4

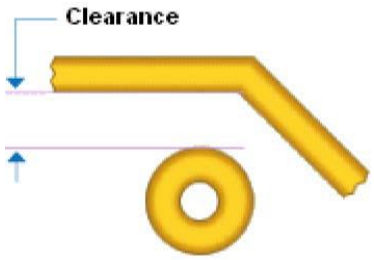

Fig. 8.4 Minimum copper clearance

Clearance requirements might be different for pairs of different copper features. Check with your manufacturer for minimum clearances and make sure that your DRC checks for any violations of those values.

Note that minimum clearances might differ from one layer to another, especially if layer thicknesses are different. Check PCB manufacturer capabilities!

6.2.2 Width

The minimum width is restricted by the PCB manufacturing process. Just like the minimum clearance, it might be different for layers with different thicknesses. Check PCB manufacturer capabilities!

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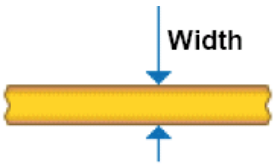

Fig. 8.5 Minimum width of traces and graphics

The minimum width should be checked for:

- Traces
- SMT Pads
- Graphics

6.2.3 Annular Ring

The minimum hole size is determined by the drilling equipment capabilities, the board thickness and the required plating thickness. The minimum annular ring is determined by the etching process and the drilling tolerances. Together, those two parameters determine the minimum pad size for THT components and the minimum via size.

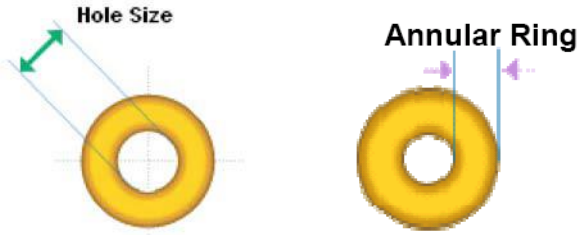

Fig. 8.6 Hole size and annular ring

6.2.4 Slivers

Slivers are design features that are so small that they surface area might be too small to adhere to the board. Slivers are a reliability risk, especially if they have an electrical function, and should be avoided. The minimum allowed sliver should be defined by the manufacturer in conjunction with registration tolerances. Figure 8.7 exemplifies the solder mask sliver.

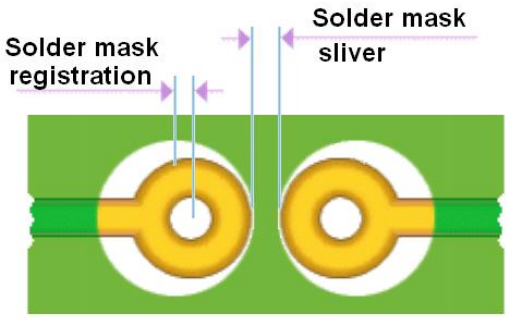

Fig. 8.7 Solder mask sliver

Slivers should be checked for:

- Soldering pads

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- Copper graphics
- Solder mask
- Silkscreen graphics

6.2.5 Acid Traps

Acid traps are areas that do not allow the flow of the etching acid and slows down the etching process. The most common cause of acid traps are the traces routed with acute angles. Figure 8.8 illustrates the relationship between the routing geometries and acid traps.

Fig. 8.8 Routing geometries and acid traps

PCBs with acid traps can still be manufactured, but with a lower yield. Acid traps should be checked for:

- Traces
- Copper graphics
- Trace-to-pad contacts

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6.2.6 Silkscreen Over Pads

Silkscreen graphics such as components outline or reference designators should not be overlapped with the soldering pads, as soldering cannot be done on paint. A minimum clearance between silkscreen and pads is required to allow for registration tolerances.

Fig. 8.9 Silkscreen over pads

6.3 Mechanical

6.3.1 Mechanical Drawings

Mechanical drawings should be included in the PCB manufacturing documentation to allow the PCB manufacturer to understand how he finished product should look and avoid later misunderstandings. Mechanical drawings should include at least:

- Board (panel) size
- Mounting holes
- Fiducial marks
- Slots
- Mechanical tolerances

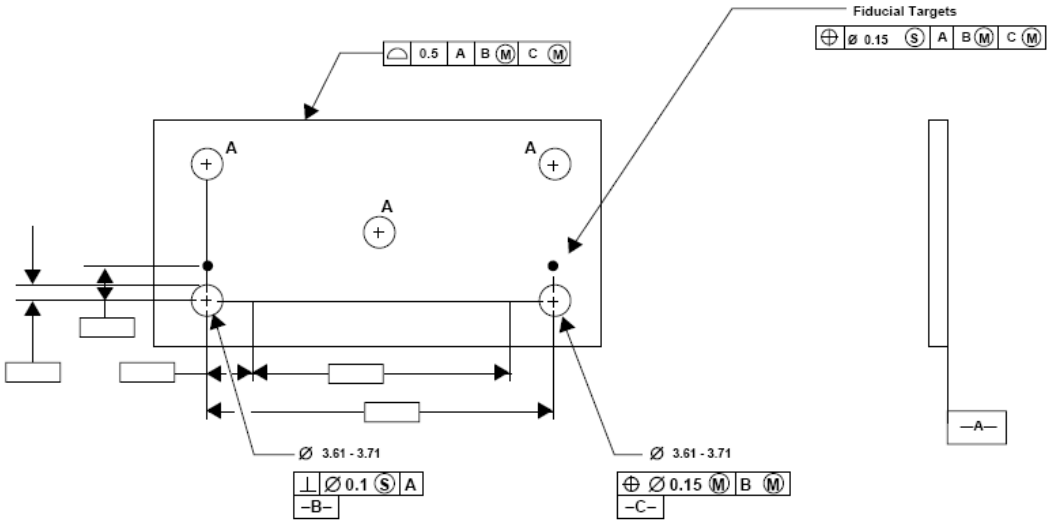

Fig. 8.10 Elements of the mechanical drawings

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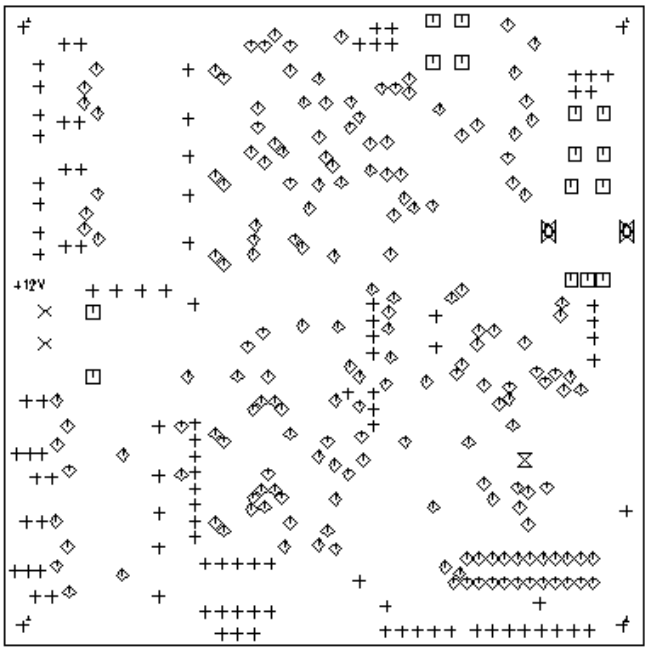
6.3.2 Drill Drawings

Drill drawings are used as a check aid for the drill operations during PCB manufacturing process. The drill drawings must contain:

- Drill location using a distinct graphical symbol for each drill size
- Legend of drill symbols

A drill drawing should be generated for each drill pair. If a drill pair includes both plated and unplated holes, it is recommended that two distinct drill drawings are provided. Plated and unplated holes are not drilled in the same manufacturing step.



SIZE	QTY	SYM	PLATED	TOL
0.8	107	+	YES	+/-0.0
1.3	2	X	YES	+/-0.0
1	15	□	YES	+/-0.0
0.6	185	◇	YES	+/-0.0
3	1	⧖	YES	+/-0.0
1 x 2.6	2	⋈	YES	+/-0.0
3	4	⊹	NO	+/-0.0

Fig. 8.11 Drill drawings

6.3.3 Slots

Slots are elongated holes created by drilling repeatedly closely spaced holes. They are made using a drilling tool, not a milling tool. Slots can also be created by milling, but if they must be plated than this will increase the manufacturing cost, as milling is normally done only at the end of the manufacturing flow, after plating. Milled slots should only be used if they are unplated. Caution should be taken, as drilled slots must be specified in a drill file and milled slots in the border outline file. Slots location and type should be specified explicitly on the mechanical drawings.

Fig. 8.12 Drilled slot

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6.3.4 Mounting holes

Mounting holes position and size is determined by the mechanical restrictions related to PCB assembly inside an enclosure or rack. Mounted holes should be unplated unless electrical contact is required for high speed or EMC considerations. The diameter of unplated mounting holes may be equal to the screw size, but plating will reduce the finished diameter of the holes. For this reason, plated mounting holes should have a diameter larger than the screw size with at least twice the plating thickness.

Large mounting holes should be milled instead of drilled because of drilling equipment capabilities. The exact diameter limit that determines if a hole should be drilled or milled is determined by the maximum hole size specification of the PCB manufacturer capabilities. If such holes must be used, a specific request including plating type should be added to the PCB manufacturing specifications.

Mounting holes should be specified explicitly on the mechanical drawings.

6.3.5 Panelization

If the PCB manufacturing panel is defined by the designer, it should be optimized for an efficient usage of panel space. A typical panel size is 460 x 610 [mm], but the exact size comes from the PCB manufacturer capabilities.

The panel should define:

- A keepout area on each side to allow for manipulation
- Tooling holes for equipment registration. Those should be placed asymmetrical to prevent wrong registration
- Scoring lines if scoring can be used for depanelization
- Depanelization routing if scoring cannot be used

Figure 8.13 illustrates the IPC recommendations regarding PCB manufacturing panels. The exact requirements for panel definitions should be extracted from the PCB manufacturer capabilities.

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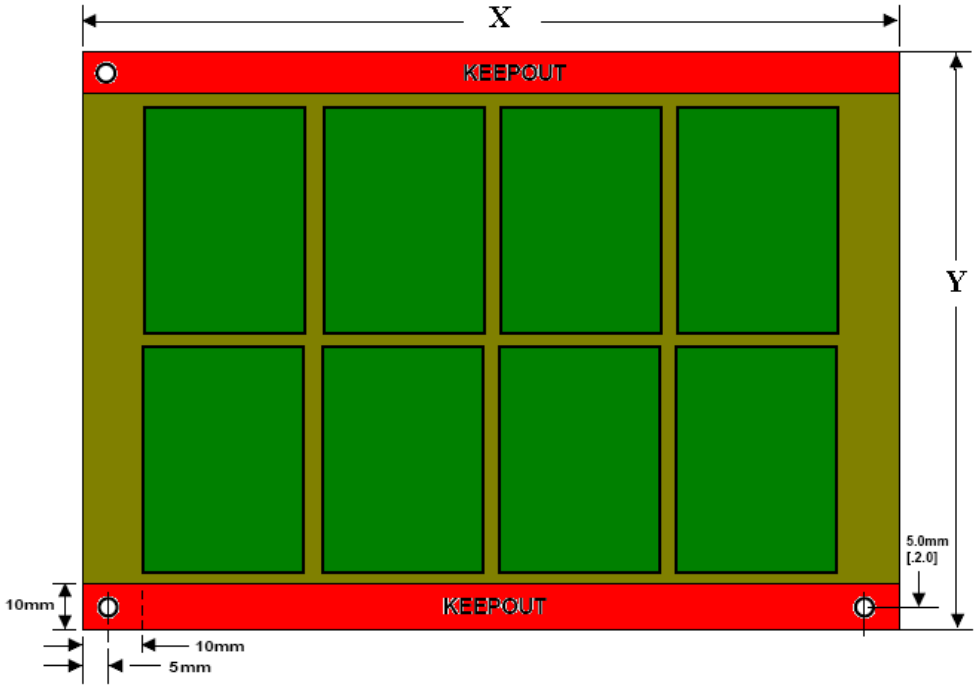

Fig. 8.13 IPC recommendations regarding panelization

If a manufacturing panel is defined by the designer in the CAM files, it should have an associated mechanical drawing. If the manufacturing panel is not defined in the CAM files but there are specific requirements regarding board-to-board positioning, a mechanical drawing should be provided and an explicit request included in the manufacturing specifications. Be aware that panelized assembly requires the panel definition to be exactly matched with the stencil definition.

6.3.6 PCB manufacturing specifications

The PCB designer should remember that, while he or she has been working on a project for a certain period of time, the PCB manufacturer has only a short period of time available between receiving the project documentation and sending it to manufacturing. Some details are likely to be omitted by the manufacturer, however obvious might seem for the designer, if not specified explicitly. The PCB manufacturing documentation should include a specification sheet with all the requirements detailed, including at least:

- Dielectric properties
- Solder mask color
- Silkscreen color and thickness
- Soldering pads finish
- Electrical / optical testing specification
- Special requirements

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6.4 Assembly Considerations

The assembly and soldering of the PCB is usually done by another party than the PCB manufacturing, which will be further identified as the PCBA manufacturer.

6.4.1 Assembly Flow

The assembly flow should be agreed with the PCBA manufacturer prior to PCB design, as each step has specific requirements. An assembly requirements report should be written, including at least:

- Assembly flow
- Components placement side
- Components grid and orientation
- Components clearance
- Special requirements (panel size, conformal coating, fillers, etc)

Such an assembly requirements report is required for the appropriate review of the assembly considerations. The PCB design should be checked against this report prior to CAM release.

6.4.2 Stencils

If reflow soldering technology is part of the assembly flow, the stencils for solder paste deposition should be designed. The stencil apertures should be slightly larger than the PCB soldering pads. The recommended oversize of the aperture depends on the type of soldering paste used and the stencil thickness and should be agreed with the PCBA manufacturer prior to releasing the manufacturing files.

Figure 8.14 illustrates the geometrical parameters of a stencil aperture.

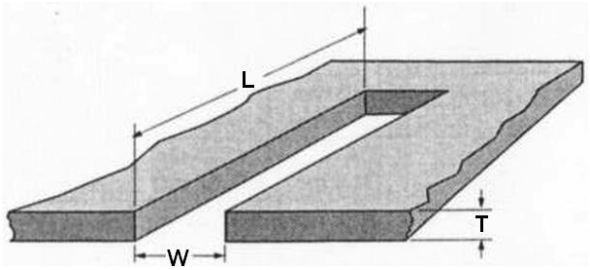

Fig. 8.14 Stencil aperture

IPC recommends that the stencil apertures meet two requirements:

(i) ***Aspect ratio*** (width / thickness):

$$\frac{W}{T} > 1.5 \tag{8.1}$$

(ii) ***Area ratio*** (pad area / aperture walls area):

$$\frac{L \cdot W}{2 \cdot (L + W) \cdot T} > 0.66 \tag{8.2}$$

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6.4.3 Panelized Assembly

If several PCBs shall be assembled as a single unit then an assembly panel should be defined. In this case is essential that both the PCB manufacturing panel and assembly panel are defined by the designer prior to PCB release, to allow him to control the exact positioning of each board on the panel. As PCB manufacturing panels are usually larger than soldering equipments can accommodate, the manufacturing panel must include several assembly panels. Several cautions should be considered:

- The assembly panel size and shape should be previously agreed with the PCBA manufacturer
- Each assembly panel should include an assembly keepout zone, determined by the board carriers used on the assembly line
- The board-to-board clearance should be restricted such that the minimum component-to-component clearance will be kept between components placed near opposite edges of the board.

6.4.4 Decals

The PCB footprints (decals) are essential for a successful assembly, as poorly designed footprints are one of the main causes of soldering defects that require manual rework. It is recommended to reuse footprints verified in previous successful projects and to mark them as verified in the CAD footprints library.

If previously verified footprints are not available then footprints compliant with the IPC-7351 standard should be used. The *IPC LP Viewer* software (see utility 11.1) presents an extensive library of standard footprints compliant with IPC-7351. Figure 8.15 presents a screenshot of this application, showing the footprint data for the Aluminum Electrolytic Capacitor with land pattern name CAPAE1030X1750N.

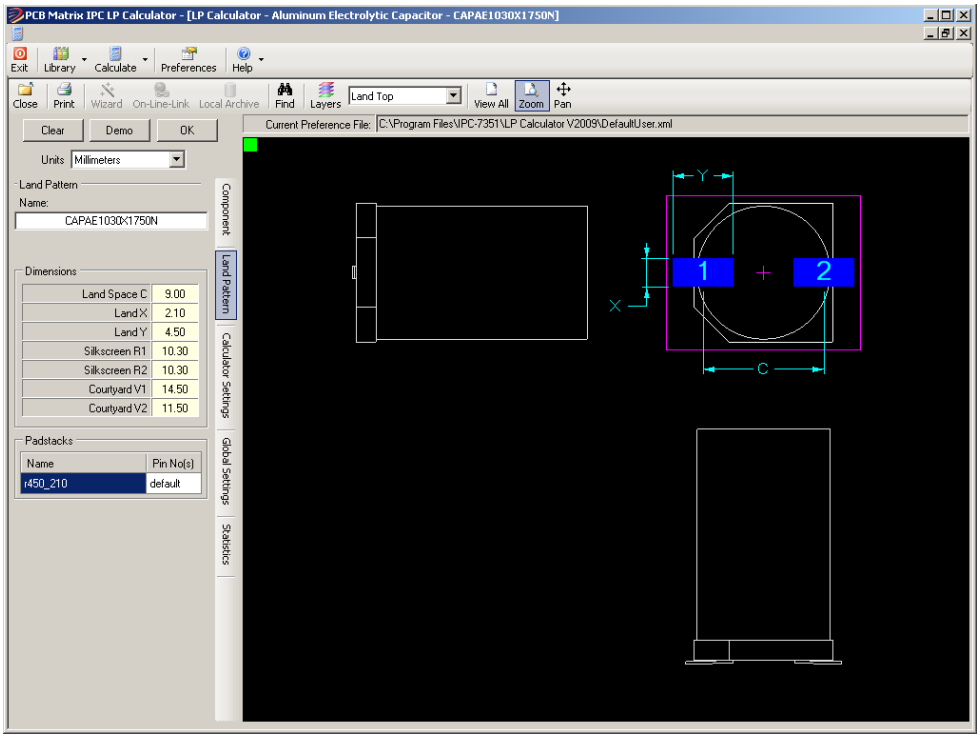

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Fig. 8.15 IPC LP Viewer / Calculator

For non-standard packages, the *IPC LP Calculator* software should be used to generate land patterns compliant with the IPC-7351 standard. If this is not available then the component manufacturer datasheet should be consulted for footprint recommendations. If such data is not available then the footprint should be checked against component size, to make sure all terminals fit on their pads and a sufficient courtyard is defined.

6.4.5 Fiducials

Fiducial marks are used by the automated manufacturing equipments for precise registration of the PCB. Three types of fiducial marks are required, as illustrated by fig. 8.16.

- Panel fiducials: three marks placed asymmetrical on the corners of the panel
- PCB fiducials: three marks placed asymmetrical on the corners of the PCB
- Local fiducials: two marks placed on opposite corners of fine pitch components

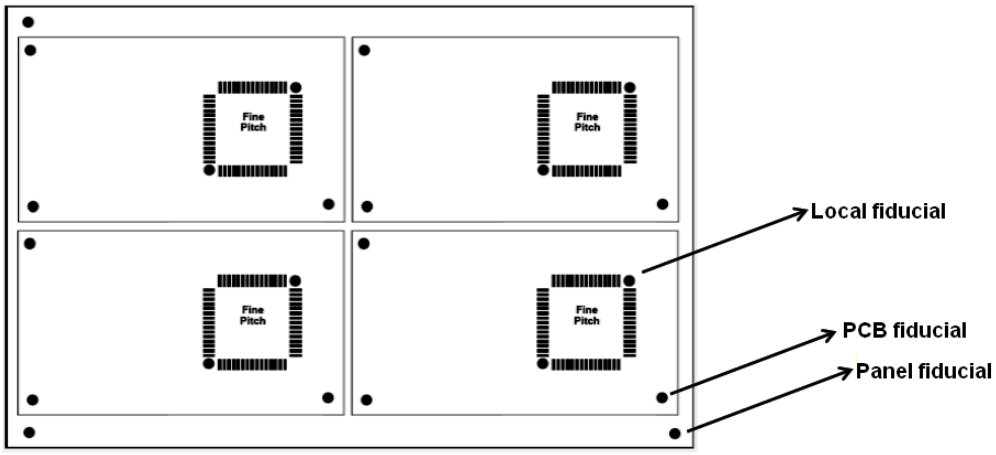

Fig. 8.16 Fiducial marks

Fiducial marks are copper features placed on top layer, with a clearance zone clear of solder mask and copper. IPC recommend using the size and clearance for fiducial mark illustrated by fig. 8.17

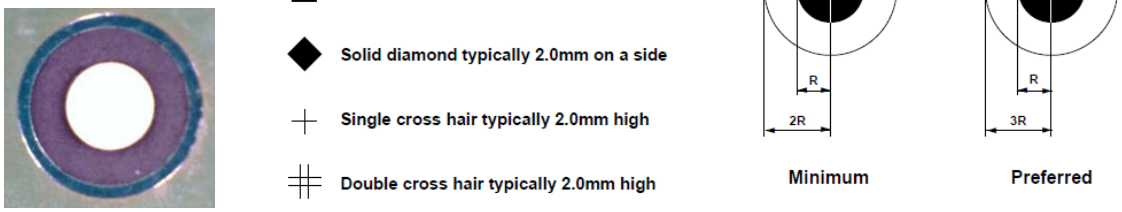

Fig. 8.17 Fiducial marks shape, size and clearance

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6.4.6 Thermal Relief

The electrical contact between soldering pads and large copper areas such as cooling zones or planes should not be made using continuous copper, but through two, three or four traces. This is required in order to avoid heat dissipation into the large copper area during soldering, which may prevent the solder to fully melt. Such a pad-plane contact, as illustrated by fig. 8.18, is called a “thermal relief pad”.

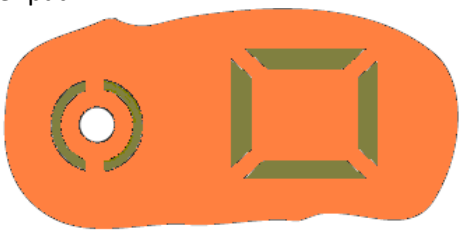

Fig. 8.18 Thermal relief pad

IPC recommends calculating the spoke width according to the equation:

$$W = 0.6 \cdot \frac{Pad\_size}{Nr\_of\_spokes} \tag{8.3}$$

This calculation should only be used as a guideline, as the tolerances regarding spoke width, geometry and pad-to-plane clearances are much larger than IPC specifications. However, a minimum number of two spokes should be mandatory for each thermal relief pad.

The thermal relief may have detrimental effects on the thermal management as it will increase the thermal resistance between the component terminal and the PCB. If this is a concern then manufacturing without thermal reliefs should be considered. This requires larger soldering temperatures and should be discussed with the PCBA manufacturer prior to PCB design, as it has to be accounted for when deciding the soldering technology used, the solder alloy and thermal profile.

6.4.7 Assembly drawings and BOM

Although all the information regarding the assembly process can be transferred to the PCBA manufacturer through CAM files, assembly drawings are still required to allow the manufacturing engineer to check the placement and detect potential design flaws. Assembly drawings should be specified distinctly for each component placement step in the assembly flow and should include at least:

- Components outline
- Reference designators
- Part numbers
- Soldering pads

Figure 8.19 illustrates an example of an assembly drawing. Remember that such documents are addressed to an engineer not a machine, so they should be easy to read and understand. Choose the amount on information included and the color contrast to a level that makes the document friendly to the user.

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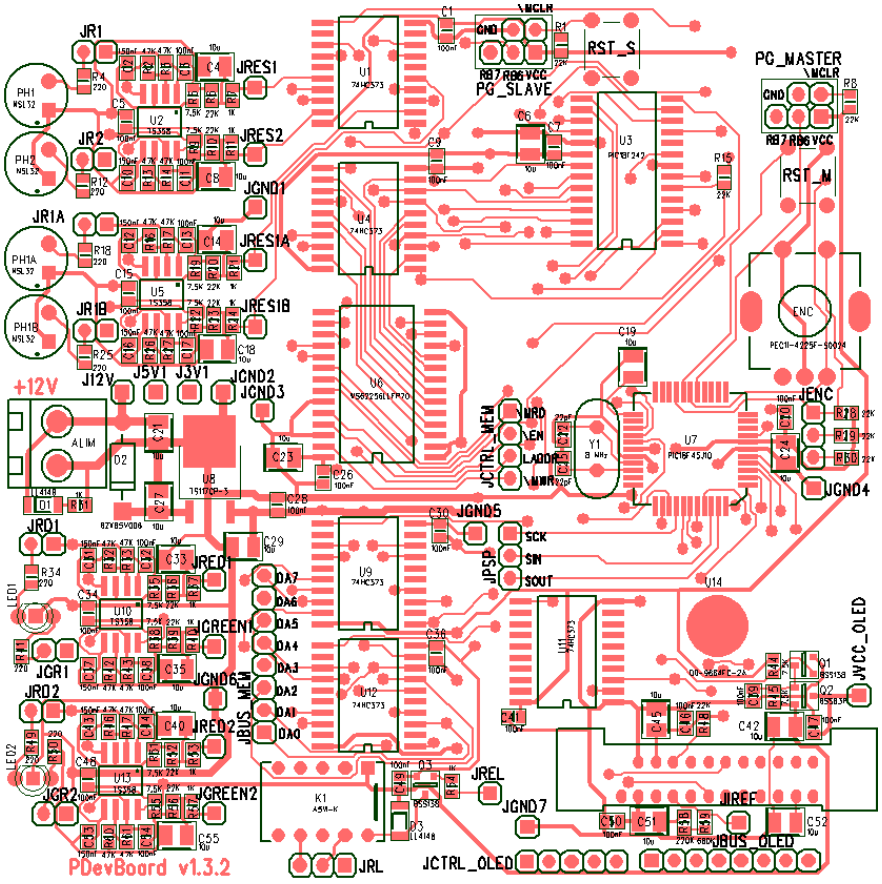

Fig. 8.19 Assembly drawing

The assembly drawings should be accompanied by a bill of materials (BOM) which can include additional data relevant to the PCBA manufacturer (package name, ordering codes, potential replacements, ROHS compliant, maximum soldering temperature, etc.).

6.4.8 PCB Assembly Specifications

For the same reasons as the PCB manufacturing specifications, the assembly documentation should include an assembly specifications document. This should include any requirement that is not apparent from the rest of the assembly documentation, such as:

- Soldering alloy of choice
- ROHS specifications
- Warnings about temperature sensitive components
- Details about components requiring special treatment (manual soldering, selective wave soldering, stiffening filler)
- Optical inspection requirements
- Traceability requirements
- Any other data relevant to the assembly engineer

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6.5 Manufacturing files

The computer aided manufacturing files (CAM) should be accompanied by a CAM list, specifying:

- File name
- Data description (top layer, solder mask top, etc)
- File format (RS274D, RS274X, etc)
- File format specification (units, M.N, coordinate mode, zero suppression, etc)

It is recommended to generate and include in the manufacturing documentation a PDF printout for each CAM file, to allow a visual check of the import.

Remember than manufacturing files must reach two manufacturers: PCB manufacturer and PCBA manufacturer, so two distinct packs should be prepared.

6.5.1 Gerber

The CAM pack for PCB manufacturing should include the following Gerber files:

- Each copper layer
- Solder mask top and solder mask bottom
- Silkscreen top and silkscreen bottom (if used)
- Paste mask for each reflow process in the manufacturing flow. Caution: if the stencil may be manufactured by the PCB manufacturer, ordered by the PCBA manufacturer or ordered by the designer to a third party. The receiver of the paste mask Gerber files should be selected accordingly.
- Board outline
- Drill drawing for plated and unplated holes

The CAM pack for PCB assembly should include the following Gerber files:

- Top layer (including fiducial marks)
- Paste mask, if necessary
- Silkscreen for each populated side (for optical inspection)

6.5.2 NC Drill

The NC drill files are only required by the PCB manufacturer. A distinct drill file should be included for plated and unplated holes.

6.5.3 Pick & Place

The pick and place files are only required by the PCBA manufacturer. Each component placement in the assembly flow requires a distinct pick & place file. Care must be taken to ensure that each component position reported in the pick & place file is located in the center of the component, not on pin1 as the component origin defined by some CAD libraries.

6.5.4 Test Point Report

The test point report is required by the manufacturer of the test fixture for in-circuit and/or functional test. This is usually managed by the PCBA manufacturer, as test fixtures must

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match test equipments, to the assembly pack should also include a test point report for each side of the board where test points are used.

7. Thermal considerations

7.1 Power Dissipation

The power is dissipated on electronic components as heat, which will increase the temperature of the components and can cause low reliability or even catastrophic failure of the system. To avoid this, the heat produced by the application should be evacuated into the surrounding environment with a rate that will keep the equilibrium temperatures below dangerous thresholds.

To account for thermal effects, the average power dissipated on electronic components should be first calculated. Not all components in a circuit should be considered for power dissipation calculation, but those operating with high currents and / or high voltage. Such calculations should be provided by the hardware designer based on the specifics of each component and simulated operating conditions.

7.2 Heatsinks

Components with high power dissipation require a heatsink and/or air flow to increase the cooling rate and avoid thermal damage. To decide if an individual component needs a heatsink, the junction-to-ambient thermal resistance and the maximum junction temperature should be considered.

The junction-to-ambient (or "junction-to-air") thermal resistance is defined as:

$$\theta_{J-A} = \frac{T_{junction} - T_{ambient}}{Dissipated\_Power}\left[\frac{K}{W}\right] \quad (9.1)$$

Based on eq. (9.1) the junction temperature can be estimated. If this is higher than the maximum junction temperature specified in the component datasheet then a heatsink is required. An error margin of at least 15% is necessary, caused mainly by the unrealistic way that JEDEC standards require for the setup of thermal resistance measurements.

The ambient temperature should be considered on worst case and should account for maximum air temperature, enclosure size and type, PCB position in the enclosure and many other factors. Such estimations cannot be done precisely by hand calculations and require the use of a computational fluid dynamics (CFD) simulator such as *Flotherm*. If such thermal simulations are not available, it is recommended to use a reference ambient temperature based on previous measurements with similar enclosures and similar dissipated power.

The choice of the appropriate heatsink should consider its thermal resistance and the junction-to-case thermal resistance of the component. For an accurate prediction of the heatsink efficiency a CFD simulator should be employed.

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7.3 Cooling Areas

Cooling areas are large copper areas that can transfer heat from the terminals and thermal pads of the components to the PCB and surrounding environment. The efficiency of the cooling areas should be previously analyzed using CFD simulations to make sure that it can provide a thermal resistance low enough for the efficient cooling of the component.

Some general guidelines related to cooling areas should be considered:

- They should have a surface area as large as possible and should be located on multiple layers
- Internal cooling areas should be thermally connected to at least an external cooling area
- If the cooling area is located on multiple layers, a large number of vias should be placed between them, to allow an efficient heat transfer
- Cooling areas should not be located underneath components
- Thermal relief should not be used for soldering pads that are used as cooling areas
- Cooling areas on external layers should not be covered by solder mask.

7.4 Current Carrying Capacity

The maximum current a PCB trace can carry (or the “current carrying capacity” or “ampacity”) is determined by:

- Copper thickness
- Trace width
- Layer location (internal / external)
- Maximum temperature difference allowed between the trace and ambient
- Routing density

The current carrying capacity is covered by the IPC-2152 standard, which gives recommendations regarding the relationship between some of those parameters. As a rule of thumb, the chart presented in fig. 9.1 can be used to estimate the current carrying capacity of 1 oz/sqf (35µm) copper traces allowing a 10 [K] overheat on the external layers and 20 [K] overheat on the internal layers.

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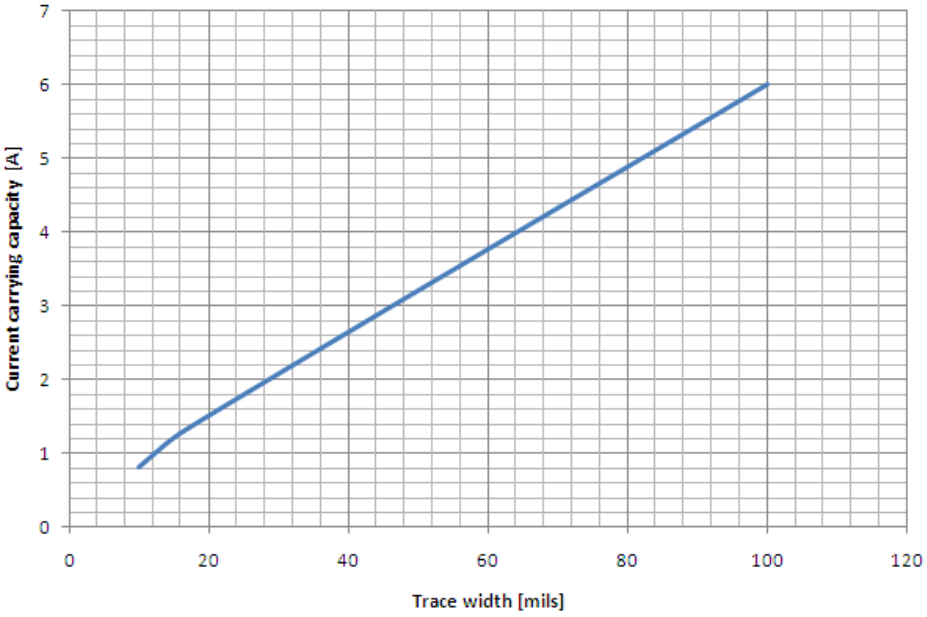

Fig. 9.1 Current carrying capacity

The above chart assumes a dense routed PCB without any other heat source in the proximity. Please note however that IPC specifications, rules of thumb and analytical formulas for current carrying capacity are contradicted by almost any experimental measurement. Like any thermal aspect it is highly dependent on many factors (just rotating the PCB will change the temperature significantly) and can only be predicted by CFD simulations.

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8. Helpful Utilities

8.1 IPC7351 Land Pattern Calculator

One of the most useful applications around for PCB layout engineers. This has been bought-out by Mentor who now charge for the product.

No.	Company	Tool	Features	Cost	Link
1	PCB Matrix Corp.	Land Pattern Calculator	Library of standard component geometries Auto-generate new components	$$	Link

8.2 PCB Fabrication Wall Chart

No.	Company	Tool	Features	Cost	Link
1	Morris Productions	Wall Chart	Shows PCB manufacturing process Indicates standard minimum geometries	Free	Link

8.3 PCB Calculators

Trace Impedance Calculators

No.	Company	Tool	Features	Cost	Link
1	Ultracad Design Inc.	PCB Trace Calculator	Full featured trace impedance calculator tool	$200	Link
2	Polar Instruments	Si8000m	High end field solver. Goal seek.	$$$	Link
3	Saturn PCB	PCB Toolkit	Fantastic utility for many PCB related calculations	Free	Link

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Power Distribution Network Analysis (PDN) software

No.	Company	Tool	Features	Cost	Link
1	Ultracad Design Inc.	PDSI	Slick user interface. User friendly, good comparison feature.	$75	Link
2	Altera	PDN Tool	Excellent full featured free utility. Spreadsheet interface.	Free	Link

Signal integrity simulator:

No.	Company	Tool	Features	Cost	Link
1	Mentor Graphics	Hyperlynx	High end signal integrity and power analysis software	$$$	Link

8.4 Filter Selection Simulator

No.	Company	Tool	Features	Cost	Link
1	Murata	MEFSS	Simulates the effects of chokes and capacitors	Free	Link

8.5 Circuit Simulation Tools

No.	Company	Tool	Features	Cost	Link
1	Linear Technologies	LT Spice	Good circuit simulation tool with simple schematic editor	Free	Link
2	National Semiconductor	WebBench	Auto-generate power supply designs, amplifier circuits, filters etc.	Free	Link

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