Chapter 11

Layout and grounding

Designing for good EMC starts from the principle of controlling the flow of interference into and out of the equipment. You must assume that interference will occur to and will be generated by any product which includes active electronic devices. To improve the electromagnetic compatibility of the product you place barriers and route currents such that incoming interference is diverted or absorbed before it enters the circuit, and outgoing interference is diverted or absorbed before it leaves the circuit. A good analogy is to think of the circuit as a town, and the EMC control measures as bypasses or ring roads. The interference (traffic) is routed around the town rather than being forced to flow through it; the disruption to the town's operation is that much less.

In either case, you can conceive the control measures as applying at three levels, primary, secondary and tertiary, as shown in Figure 11.1.

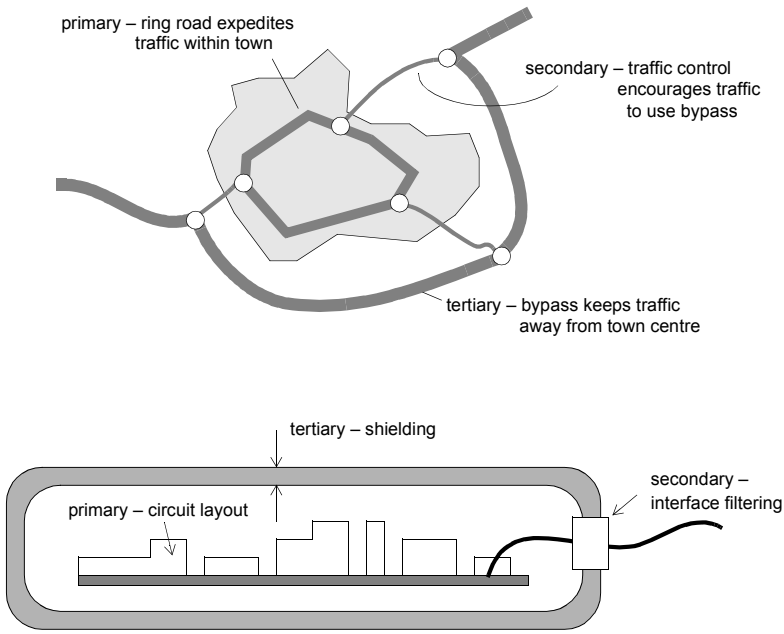


Figure 11.1 EMC control measures

Control at the primary level involves circuit design measures such as decoupling, balanced configurations, bandwidth and speed limitation, and especially board layout and grounding. For some low-performance circuits, and especially those which have no connecting cables, such measures may be sufficient in themselves. At the secondary level you must always consider the interface between the internal circuitry and external cables. This is invariably a major route for interference in both directions, and for some products (particularly where the circuit design has been frozen) all the control may have to be applied by filtering at these interfaces. Choice and mounting of connectors forms an important part of this exercise.

Full shielding (the tertiary level) is an expensive choice to make and you should only choose this option when all other measures have been applied. But since it is difficult or impossible to predict the effectiveness of primary measures in advance, it is wise to allow for the possibility of being forced to shield the enclosure. This means adapting the mechanical design so that a metal case could be used, or if a moulded enclosure is essential, you should ensure that apertures and joints in the mouldings can be adequately bonded at RF, that ground connections can be made at the appropriate places and that the moulding design allows for easy application of a conductive coating.

Chapter 12 looks at circuit design, and Chapters 13 and 14 consider the "classical" aspects of interfaces, filters and shielding. This chapter covers layout and grounding.

11.1 Equipment layout and grounding

The most cost-effective approach is to consider the equipment's layout and ground regime at the beginning. No unit cost is added by a designed-in ground system. Ninety per cent of post-design EMC problems are due to inadequate layout or grounding: a well-designed layout and ground system can offer both improved immunity and protection against emissions, while a poorly designed one may well be a conduit for emissions and incoming interference. The most important principles are:

- partition the system to allow control of interference currents;
- consider ground as a path for current flow, both of interference into the equipment and conducted out from it;
- consider it also as a means of preventing interference currents from affecting signal circuits; this means careful placement of grounding points, and minimizing both the ground impedance itself and its transfer impedance to the circuit;
- design the conducting parts of the mechanical structure in the knowledge that they are unavoidably carrying interference currents, which you want to keep separate from your circuit.

11.1.1 System partitioning

The first design step is to partition the system. A poorly partitioned, or non-partitioned system (Figure 11.2) may have its component sub-systems separated into different areas of the board or enclosure, but the interfaces between them will be ill-defined and the external ports will be dispersed around the periphery. This makes it difficult to control the common mode currents that will exist at the various interfaces. Dispersal of the ports means that the distance between ports on opposite sides of the system is large, leading to high induced ground voltages as a result of incoming interference, and efficient coupling to the cables of internally generated emissions.

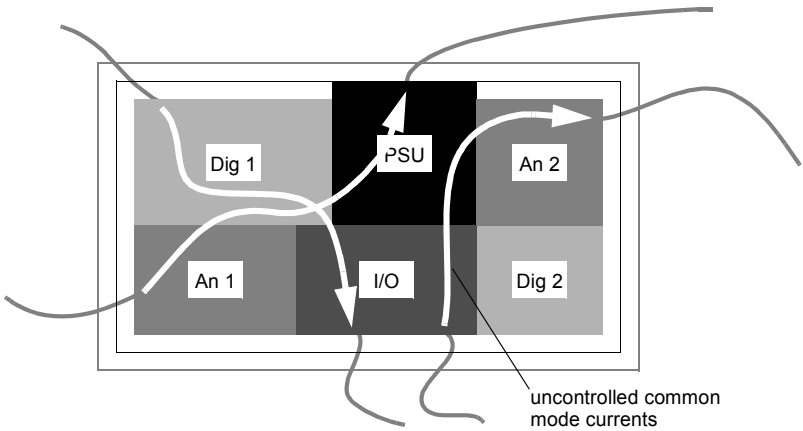


Figure 11.2 The haphazard system

Usually the only way to control emissions and immunity of such a system is by placing an overall shield around it and filtering each interface. In many cases it will be difficult or impossible to maintain integrity of the shield and still permit proper operation – the necessary apertures and access points will preclude effective attenuation through the shield.

11.1.1.1 The partitioned system

Partitioning separates the system into critical and non-critical sections from the point of view of EMC. Critical sections are those which contain radiating sources such as microprocessor logic or video circuitry, or which are particularly susceptible to imported interference: microprocessor circuitry and low-level analogue circuits. Non-critical sections are those whose signal levels, bandwidths and circuit functions are such that they are not susceptible to interference nor capable of causing it: non-clocked logic, linear power supplies and power amplifier stages are typical examples. Figure 11.3 shows this method of separation.

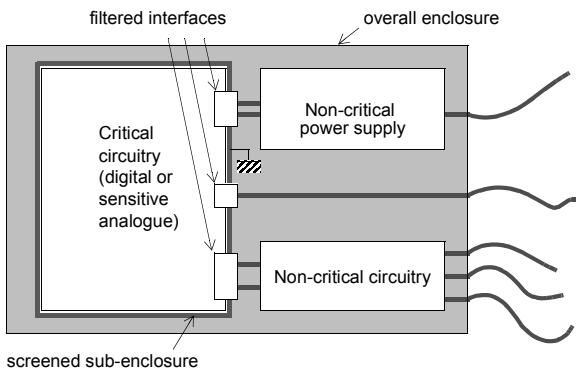


Figure 11.3 System partitioning

Control of critical sections

Critical sections can then be enclosed in a shielded enclosure into and out of which all external connections are carefully controlled. This enclosure may encase the whole product or only a portion of it, depending on the nature of the circuits: your major design goal should be to minimize the number of controlled interfaces, and to concentrate them physically close together. Each interface that needs to be filtered or requires screened cabling adds unit cost to the product. A product with no electrical interface ports – such as a pocket calculator or infra-red remote controller – represents an ideal case from the EMC point of view.

Note that the shield acts both as a barrier to radiated interference and as a reference point for ground return currents. In many cases, particularly where a full ground plane PCB construction is used, the latter is the more important function and it may be possible to do without an enclosing shield.

11.1.2 Grounding

Once the system has been properly partitioned, you can then ensure that it is properly grounded. Before continuing, it is as well to note that there is some confusion in terminology. In conventional electrical usage, "grounding" is American for the same function as is "earthing" in English; that is, a safety protective function. Since this is an English book and the EMC function is different, the words "ground" and "grounding" will be used here to distinguish the EMC function while "earth" and "earthing" will be used for the safety function.

The accepted purpose for grounding is to give a reference for external connections to the system. The classical definition of a ground is "an equipotential point or plane which serves as a reference for a circuit or system". Unfortunately this definition is meaningless in the presence of ground current flow. Even where signal currents are negligible, induced ground currents due to environmental magnetic or electric fields will cause shifts in ground potential. A good grounding system will minimize these potential differences by comparison with the circuit operating levels, but it cannot eliminate them. It has been suggested [5] that the term "ground" as conventionally used should be dropped in favour of "reference point" to make the purpose of the node clear.

An alternative definition for a ground is "a low impedance path by which current can return to its source" [105]. This emphasizes current flow and the consequent need for low impedance, and is more appropriate when high frequencies are involved. Ground currents always circulate as part of a loop. The task is to design the loop in such a way that induced voltages remain low enough at critical places. You can only do this by designing the ground circuit to be as compact and as local as possible.

The most important EMC function of a ground system is to *minimize interference voltages at critical points compared to the desired signal*. To do this, it must present a low *transfer* impedance path at these critical locations. The concept of transfer impedance is introduced in section 11.1.2.2.

11.1.2.1 Current through the ground impedance

When designing a ground layout you must know the actual path of the ground return current. The amplifier example in Figure 11.4 illustrates this. The high-current output ΔI returns to the power supply from the load; if it is returned through the path Z1–Z2–Z3 (Figure 11.4(a)) then an unwanted voltage component is developed across Z2 which is in series with the input V_S, and depending on its magnitude and phase the circuit will oscillate. This is an instance of common impedance coupling, as per section 10.1.1.

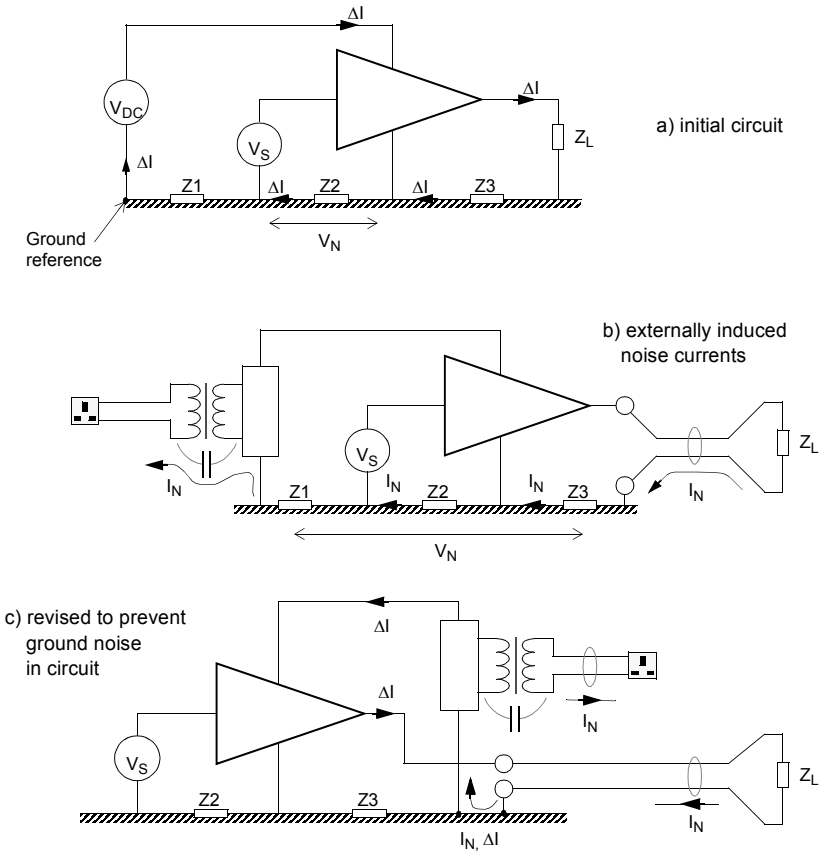


Figure 11.4 Ground current paths in an example circuit

For EMC purposes, instability is not usually the problem; rather it is the interference voltages V_N which are developed across the impedances that create emission or susceptibility problems. At high frequencies (above a few kHz) or high rates of change of current the impedance of any linear connection is primarily inductive and increases with frequency ($V = -L \cdot di/dt$), hence ground noise increases in seriousness as the frequency rises. The effect of adding external connections is illustrated in Figure 11.4(b). Interference current I_N induced in, say, the output lead, flows through the ground system, passing through Z2 again and therefore inducing a voltage in series with the input, before exiting via stray capacitance to the mains supply connection. The same route could be taken in reverse by incoming mains-borne noise.

To deal with the problem, it is simply necessary to ensure that the interfering currents are not allowed to flow through the sensitive part of the ground network, as is shown by the rearrangement of Figure 11.4(c). On a circuit diagram these circuits would appear identical; in practical realization, when laid out on a PCB, they are different.

11.1.2.2 Transfer impedance

For EMC purposes, grounding provides a set of interconnected current paths, designed to have a low transfer impedance Z_T, in order to minimize interfering voltages at sensitive interfaces which may or may not be ground-referred. Z_T determines the strength of the unwanted source in the signal circuit due to interference current flowing in the common mode circuit. Depending on the interface under consideration, we tackle the transfer impedance of an appropriate part of the interconnected grounding paths. The result is a grounding structure, whose three-dimensional shape is designed for low Z_T. The structure can be realized as a "shielding" enclosure, a chassis plate, a plane layer on a PCB, or a cable conduit, whatever is required by the application.

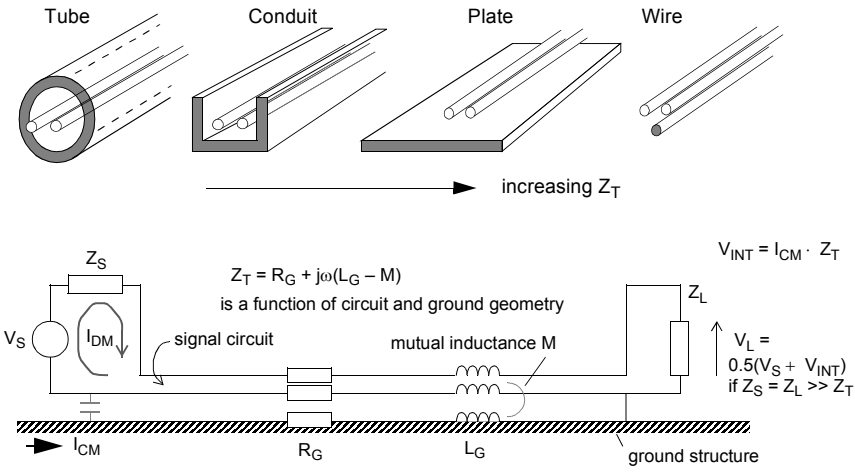


Figure 11.5 Transfer impedance of the ground structure

The important quality of such a structure (Figure 11.5) is that when a disturbance current flows in it, only a small interference voltage V_{INT} is generated differentially in the signal circuit. The dominant contribution to Z_T for external interference currents flowing in the ground is mutual inductance between common and differential mode circuits. Z_T is reduced in proportion to the mutual inductance linking the structure and the circuit. The grounding structure should have minimum resistance R_G and self-inductance L_G. Z_T is minimized by a solid enclosing tube – you may recognize this as a coaxial shielded cable – and is worst if the structure is non-existent, since all interference current then flows in the circuit. A haphazard ground structure with appreciable series impedance – caused by apertures and discontinuities, see section 14.1.3 – is little better, and the first level of usefulness is offered by a parallel wire conductor. Practical compromise structures are the conduit or the flat plate. The closer the differential mode circuit is physically to such a grounding structure, the less the Z_T, provided that the structure is unbroken in the direction of current flow.

This discussion has concentrated on ground currents, since in general the low inherent impedance of ground structures allows relatively high interference currents to flow; EMC consists in recognizing this and taking the appropriate precautions. It is important, though, that noise voltages are not allowed to build up on the grounding

structure relative to the circuit, since the close coupling recommended above for low Z_T purposes also implies a high capacitance, which in turn would allow such voltages to couple more readily into the circuit. This suggests that the circuit 0V reference should itself be connected to the ground structure at least at one point, normally close to the most sensitive part of the circuit; but this will *encourage* the distribution of current between the ground structure and the circuit! This paradox can only be resolved by physically designing the ground structure for the least possible Z_T.

11.1.3 Ground systems

Ignoring for now the need for a safety earth, a grounding system as intended for a circuit reference can be configured as single point, multi-point or as a hybrid of these two.

11.1.3.1 Single point

The single point grounding system (Figure 11.6(a)) is conceptually the simplest, and it eliminates common impedance ground coupling and low frequency ground loops. Each circuit module has its own connection to a single ground, and each rack or sub-unit has one bond to the chassis. Any currents flowing in the rest of the ground network do not couple into the circuit. This system works well up to frequencies in the MHz region, but the distances involved in each ground connection mean that common mode potentials between circuits begin to develop as the frequency is increased. At distances of odd multiples of a quarter wavelength, the circuits are effectively isolated from each other. At the same time, stray capacitance starts to contribute to "sneak" current paths that bypass the single point wiring.

A modification of the single point system (Figure 11.6(b)) ties together those circuit modules with similar characteristics and takes each common point to the single ground. This allows a degree of common impedance coupling between those circuits where it won't be a problem, and at the same time allows grounding of high frequency circuits to remain local. The noisiest circuits are closest to the common point in order to minimize the effect of the common impedance. When a single module has more than one ground, these can be tied together with back-to-back diodes to prevent damage when the circuit is disconnected.

11.1.3.2 Multi-point

Hybrid and multi-point grounding (Figure 11.6(c)) can overcome the RF problems associated with pure single point systems. Multi-point grounding is necessary for digital and large signal high frequency systems. Modules and circuits are bonded together with many short ($< 0.1\lambda$) links to minimize ground-impedance-induced common mode voltages. Alternatively, many short links to a chassis, ground plane or other low impedance conductive body are made. This may not be suitable for sensitive audio circuits, if the loops that are introduced then create magnetic field pick-up. It is difficult to keep 50/60Hz interference out of such circuits, but this is only a problem if the circuits themselves can be affected by it, and if its amplitude is large because the loop areas are large. Circuits which operate at higher frequencies or levels are generally not susceptible to this interference. The multi-point sub-system can be brought down to a single point ground in the overall system.

11.1.3.3 Hybrid

Hybrid grounding uses reactive components (capacitors or inductors) to make the grounding system act differently at low frequencies and at RF. This may be necessary

in sensitive wideband circuits. In the example of Figure 11.6(c), the sheath of a relatively long cable is grounded directly to chassis via capacitors to prevent RF standing waves from forming. The capacitors block DC and low frequencies and therefore prevent the formation of an undesired extra ground loop between the two modules.

When using such reactive components as part of the ground system, you need to take care that spurious resonances (which could enhance interference currents) are not introduced into it. For example if 0.1μF capacitors are used to decouple a cable whose self-inductance is 0.1μH, the resonant frequency of the combination is 1.6MHz. Around this frequency the cable screen will appear to be anything but grounded!

When you are using separate DC grounds and an RF ground plane (such as is offered by the chassis or frame structure), reference each sub-system's DC ground to the frame by a 10–100nF capacitor. The two should be tied together by a low impedance link at a single point where the highest di/dt signals occur, such as the processor motherboard or the card cage backplane.

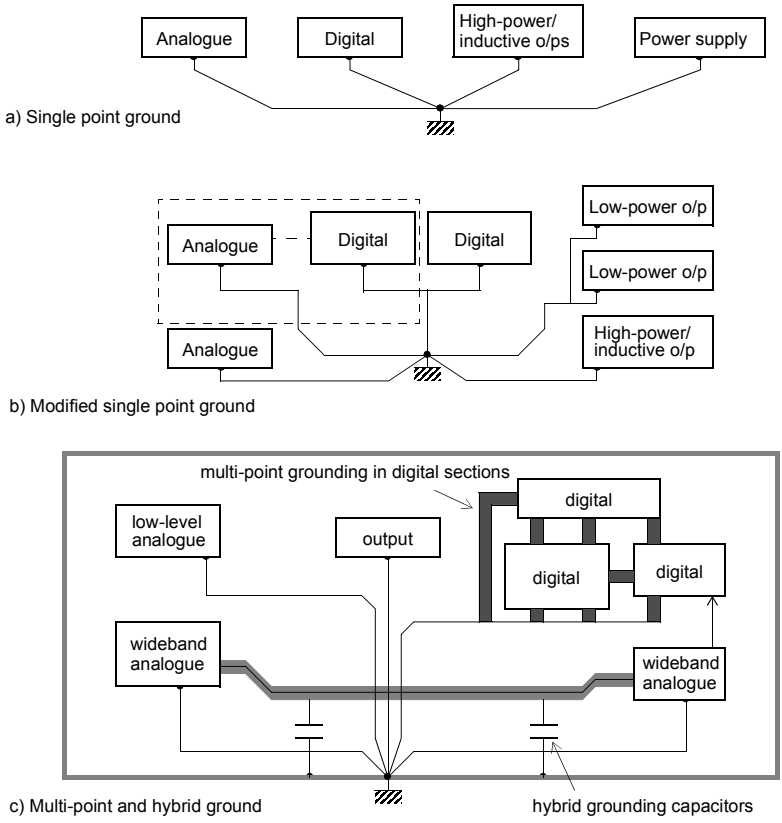


Figure 11.6 Grounding systems

11.1.3.4 The impedance of ground wires

When a grounding wire runs for some distance alongside a ground plane or chassis before being connected to it, it appears as a transmission line. This can be modelled as an LCR network with the L and C components determining the characteristic impedance Z_0 of the line (Figure 11.7).

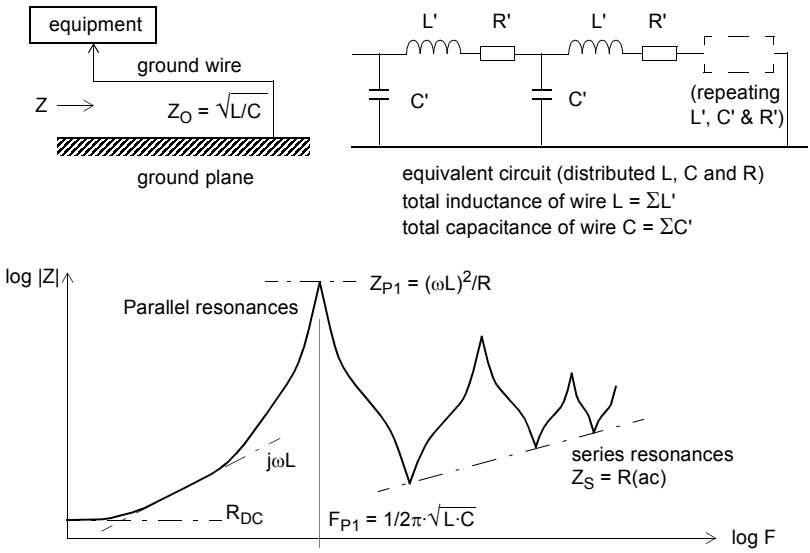


Figure 11.7 The impedance of long ground wires

As the operating frequency rises, the inductive reactance exceeds the resistance of the wire and the impedance increases up to the first parallel resonant point. At this point the impedance seen at the end of the wire is high, typically hundreds of ohms (determined by the resistive loss in the circuit). After first resonance, the impedance for a lossless circuit follows the law:

$$Z = Z_O \,.\, \tan [\omega \,.\, x \,.\, \sqrt{(L/C)}] \qquad (11.1)$$

where x is the distance along the wire to the short

and successive series (low impedance) and parallel (high impedance) resonant frequencies are found. As the losses rise due to skin effect, so the resonant peaks and nulls become less pronounced. To stay well below the first resonance and hence remain an effective conductor, the ground wire should be less than 1/20th of the shortest operating wavelength.

11.1.3.5 The safety earth

From the foregoing discussion, you can see that the safety earth (the green and yellow wire) is not an RF ground at all. Many designers may argue that everything is connected to earth via the green and yellow wire, without appreciating that this wire has a high and variable impedance at RF. In general the safety earth connection is not necessary for EMC purposes: after all, battery powered apparatus can function quite successfully

without it. A good low impedance connection to an RF reference provided locally by a chassis, frame or plate *is* necessary and in many cases must be provided *in parallel with* the safety earth. On the other hand, if we are considering mains emissions or incoming mains-borne disturbances, which are propagating in common mode with respect to the safety earth, then a safety earth connection is required for EMC purposes, so that filter capacitors can be tied to it. This is not because it is an earth, but because it is the return path for the disturbance currents.

It may even be necessary for you to take the safety earth *out* of the RF circuit deliberately, by inserting a choke of the appropriate current rating in series with it (see section 13.2.3.6). This is because it can offer an alternative path for interference currents to invade or circulate within the system, and interrupting this path is a simple way of improving EMC.

11.1.3.6 Ground map

A fundamental tool for use throughout the equipment design is a ground map. This is a diagram which shows all the ground reference points and grounding paths (via structures, cable screens, etc. as well as tracks and wiring) for the whole equipment. It concentrates on grounding only; all other circuit functions are omitted or shown in block form. Its creation, maintenance and enforcement throughout the project design should be the responsibility of the EMC design authority.

11.1.3.7 Summary

In the context of product-level grounding, and so for dimensions up to say 1m, at frequencies below 1MHz single point grounding is possible and in some circumstances preferable. Above 10MHz a single point ground system is not feasible because wire and track inductance raises the ground impedance unacceptably, and stray capacitance allows unintended ground return paths to exist. For high frequencies multi-point grounding to a low inductance ground plane or shield is essential. This creates ground loops which may be susceptible to magnetic field induction, so should be avoided or specially treated in a hybrid manner when used with very sensitive circuits.

For EMC purposes, *even a circuit which is only intended to operate at low frequencies must exhibit good immunity from RF interference*. This means that those aspects of its ground layout which are exposed to the interference – essentially all external interfaces – must be designed for multi-point grounding. At the bare minimum, some low inductance ground plate or plane must be provided at the interfaces.

Grounding principles

- All conductors have a finite impedance which increases with frequency
- Two physically separate ground points are not at the same potential unless no current flows between them
- At high frequencies there is no such thing as a single point ground

11.2 PCB layout

The way in which you design a printed circuit board makes a big difference to the overall EMC performance of the product which incorporates it. The principles outlined above must be carried through onto the PCB, particularly with regard to partitioning, interface layout and ground layout. This means that the circuit designer must exert tight control over the layout draughtsman, especially when CAD artwork is being produced. Conventional CAD layout software works on a node-by-node basis, which if allowed to will treat the entire ground system as one node. This is fine if you are designing with a single ground plane for the whole product, but will cause problems with multiple ground planes if left uncorrected.

Design of a PCB with multilayer technology is discussed shortly. But if you are using older technology, i.e. double- or single-sided, the safest way to lay out a PCB is to start with the ground traces, manually if necessary, then to incorporate critical signals such as HF clocks or sensitive nodes which must be routed near to their ground returns, and then to track the rest of the circuitry at will. As much information should be provided with the circuit diagram as possible, to give the layout draughtsman the necessary guidance at the beginning. These notes should include:

- physical partitioning of the functional sub-modules on the board;
- positioning requirements of sensitive components and I/O ports;
- marked up on the circuit diagram, the various ground nodes that are being used, together with which connections to them must be regarded as critical;
- where the various ground nodes may be commoned together, and where they must *not* be;
- which signal tracks must be routed close to the ground tracks, plus any other constraints on the signal track routing.

One consequence of the universal single ground plane approach, evaluated in section 11.2.3.3, is that it eases the dilemmas that flow from the third and fourth points above.

11.2.1 Ground layout without a ground plane

11.2.1.1 Track impedance

Careful placement of ground connections goes a long way towards reducing the noise voltages that are developed across ground impedances. But on any non-trivial printed circuit board it is impractical to eliminate circulating ground currents entirely. The other aspect of ground design is to minimize the value of the ground impedance itself.

Track impedance is dominated by inductance at frequencies higher than a few kHz (Figure 11.8). You can reduce the inductance of a connection in two ways:

- minimizing the length of the conductor, and if possible increasing its width;
- running its return path parallel and close to it.

The inductance of a PCB track is primarily a function of its length, and only secondarily a function of its width. For a single conductor of diameter d and length l inches, equation (11.2) gives the self-inductance (further equations are given in Appendix D):

$$L = 0.0051 \cdot l \cdot (\ln(4l/d) - 0.75) \text{ microhenries} \quad (11.2)$$

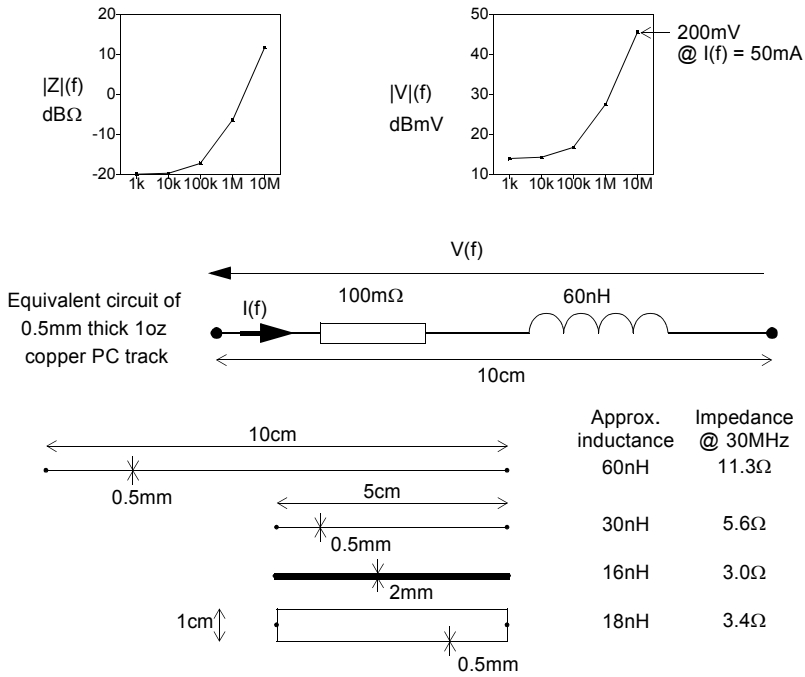


Figure 11.8 Impedance of printed circuit tracks

Because of the logarithmic relationship of inductance and diameter, doubling this dimension does not produce a 50% decrease in inductance. Paralleling tracks will reduce the inductance *pro rata* provided that they are separated by enough distance to neutralize the effect of mutual inductance (see Figure 10.4 on page 226). For narrow conductors spaced more than 1cm apart, mutual inductance effects are negligible.

11.2.1.2 Gridded ground

The logical extension to paralleling ground tracks is to form the ground layout in a grid structure (Figure 11.9). This maximizes the number of different paths that ground return current can take, and therefore minimizes the ground inductance for any given signal route. Such a structure is well suited to low cost digital double-sided PCB layout with multiple packages, when individual signal/return paths are too complex to define easily [71]. The grid structure doesn't have to be regular, and indeed in most such layouts the sizes of the apertures in the grid are anything but uniform.

A wide ground track is preferred to narrow for minimum inductance, but even a narrow track linking two otherwise widely-separated points is better than none. The grid layout is best achieved by putting the grid structure down first, before the signal or power tracks are laid out. You can follow the X-Y routing system for double-sided boards, where the X-direction tracks are all laid on one side and the Y-direction tracks all on the other. Offensive (high di/dt) signal tracks can then be laid close to the ground tracks to keep the overall loop area small; this may call for extra ground tracking, which should be regarded as an acceptable overhead.

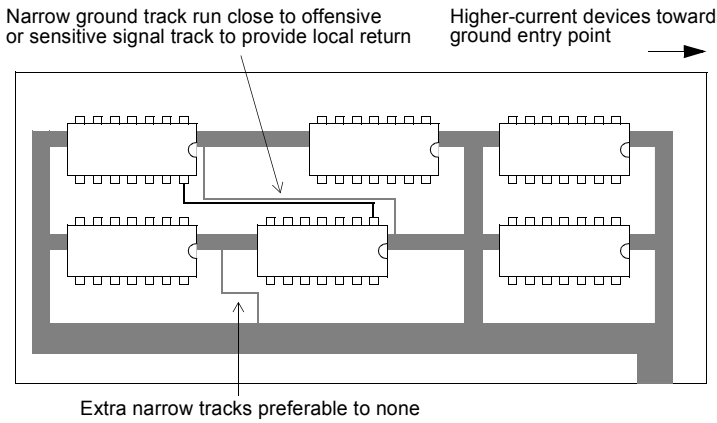


Figure 11.9 The gridded ground structure

Undesirable ground style

The one type of ground configuration that you should not use for any class of circuit is the "comb" style in which several ground spurs are run from one side of the board (Figure 11.10). Such a layout forces return currents to flow in a wide loop even if the signal track is short and direct, and contributes both to increased radiation coupling and to increased ground noise generation. The significant common ground impedance introduced between packages on the board may also cause circuit malfunction. The comb can easily be converted to a proper grid by adding bridging tracks at intervals across the spurs.

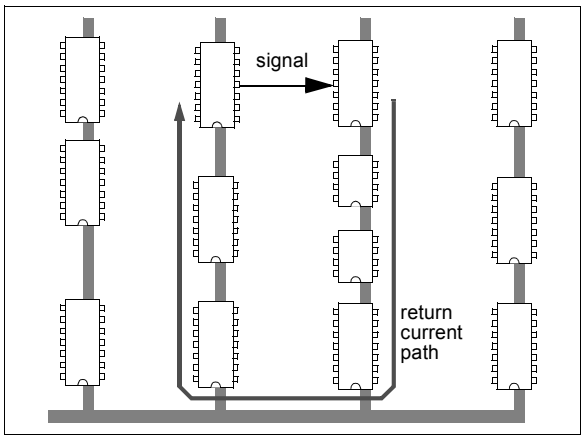


Figure 11.10 Undesirable: the comb ground structure

11.2.2 Using a ground plane

The limiting case of a gridded ground is when an infinite number of parallel paths are provided and the ground conductor is continuous, and it is then known as a ground plane. This is easy to realize with a multilayer board and offers the lowest possible ground path inductance. It is essential for RF circuits and digital circuits with high clock speeds, and offers the extra advantages of greater packing density and a defined characteristic impedance for all signal tracks [100] (see section 11.2.2.6). A common four-layer configuration includes the power supply rail as a separate plane, which gives a low power-ground impedance at high frequencies.

The main EMC purpose of a ground plane is to provide a low-impedance ground and power return path to minimize induced ground noise. Shielding effects on signal tracks are secondary and are in any case nullified by the components, which stand proud of the board. There is little to be gained in general from having power and ground planes outside the signal planes on four-layer boards, especially considering the extra aggravation involved in testing, diagnostics and rework. The exception will be where there is significant E-field (dv/dt) coupling to or from the tracks which exceeds the coupling due to the components. In this case putting the power and ground planes to the outside of the board will provide an E-field shield to these tracks, but it is rare that such coupling is the dominant factor (backplanes are the most typical exception), and EMC performance is usually best served by keeping the power and ground plane layers adjacent and very close.

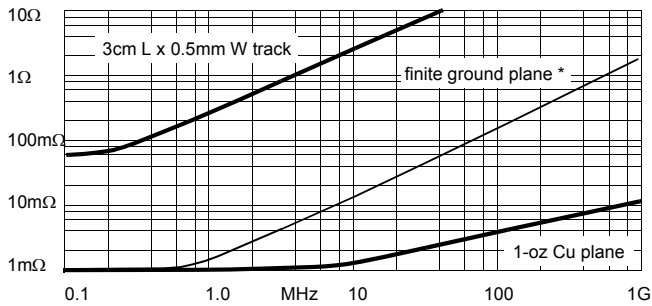


Figure 11.11 Impedance of ground plane versus track

Figure 11.11 compares the impedance between any two points (independent of spacing) on a ground plane *of infinite extent* with the equivalent impedance of a short length of track. The impedance starts to rise at higher frequencies because the skin effect increases the effective resistance of the plane, but this effect follows the square root of frequency (10dB/decade) rather than the inductive wire impedance which is directly proportional to frequency (20dB/decade). For a *finite* ground plane, the geometrical centre should see the ideal impedance while points near the outside will see much higher values as the impedance becomes markedly inductive. The corollary of this is that you should never place critical tracks or devices near the outside edge of the ground plane. An approximation for the inductance of the return path per unit length for a given signal track in the bulk of the PCB has been given by [56] as:

$$L \approx 5\,(h/w)\ \text{nH/cm} \qquad (11.3)$$

where w is the width of the plane, h is the distance between the signal track of interest and the return plane, and the length of the return path is much greater than h.

11.2.2.1 Ground plane on double-sided PCBs

A partial ground plane is also possible on double-sided PCBs. This is not achieved merely by filling all unused space with copper and connecting it to ground – since the purpose of the ground plane is to provide a low inductance ground path, it must be positioned under (or over) the tracks which need this low inductance return. At high frequencies, return current does not take the geometrically shortest return path but will flow preferentially in that part of the plane which is in the neighbourhood of its signal trace. This is because such a route encloses the least area and hence has the lowest overall inductance. Thus the use of an overall ground plane ensures that the optimum return path is always available, allowing the circuit to achieve minimum inductive loop area by its own devices [131].

A partial ground plane

Figure 11.12 illustrates the development of the ground plane concept from the limiting case of two parallel identical tracks. To appreciate the factors which control inductance, remember that the total loop inductance of two parallel tracks which are carrying current in *opposite* directions (signal and return) is given by equation (11.4):

$$L_{tot} = L_1 + L_2 - 2M \qquad (11.4)$$

where L_1, L_2 are the inductances of each track and
M is the mutual inductance between them

M is inversely proportional to the spacing of the tracks; if they were co-located it would be equal to L and the loop inductance would be zero. In contrast, the inductance of two identical tracks carrying current in the *same* direction is given by:

$$L_{tot} = (L + M)/2 \qquad (11.5)$$

so that a closer spacing of tracks *increases* the total inductance, towards that of one track on its own. Since the ground plane is carrying the return current for signal tracks above it, it should be kept as close as possible to the tracks to keep the loop inductance to a minimum. For a continuous ground plane this is set only by the thickness of the intervening board laminate.

11.2.2.2 Ground planes for low cost boards

The ground plane approach is well established for high-value, high-speed digital circuits for which multilayer PCBs are the norm. What is sometimes less appreciated is that it is directly relevant to low-cost analogue circuits as well. Adding a ground plane to a cheap single-sided analogue board is often the single most cost-effective change for improving EMC.

Despite the encroachment of digital technology, analogue circuits are still widely used for simple, cost-sensitive applications, particularly in the consumer market. Examples are security sensors, timers and residual current detectors. For these products, cost is the driving factor and both component count and assembly time must be kept to a minimum. Volumes may be high and assembly is often done in low labour cost areas, so that through hole insertion may still be economic by comparison with surface mounting. PCB technology may be single sided on PRBF, if double-sided PTH

on fibreglass represents too high a cost. These products typically are unconcerned with RF emissions, and historically EMC has never been considered in their design. Under the EMC Directive though, RF and transient immunity is important, even as it is for reliability of operation. This immunity can frequently best be achieved by implementing a ground plane on the board.

Adding a grounded copper layer

A plane can be implemented retrospectively by simply adding a top copper layer to a single-sided board design, without changing the original layout (Figure 11.13). The top copper etch pattern is limited to clearance holes around each component lead – the original pad pattern in reverse. The top layer is connected by a through wire or eyelet to the 0V track on the underside.

This construction does not make the plane behave in the optimum fashion, where current flowing within it minimizes magnetic coupling to the circuits – the plane ensuring minimum possible loop area for each circuit path. It cannot do this as long as the 0V returns for each and every circuit are not connected to it. It does, though, act as

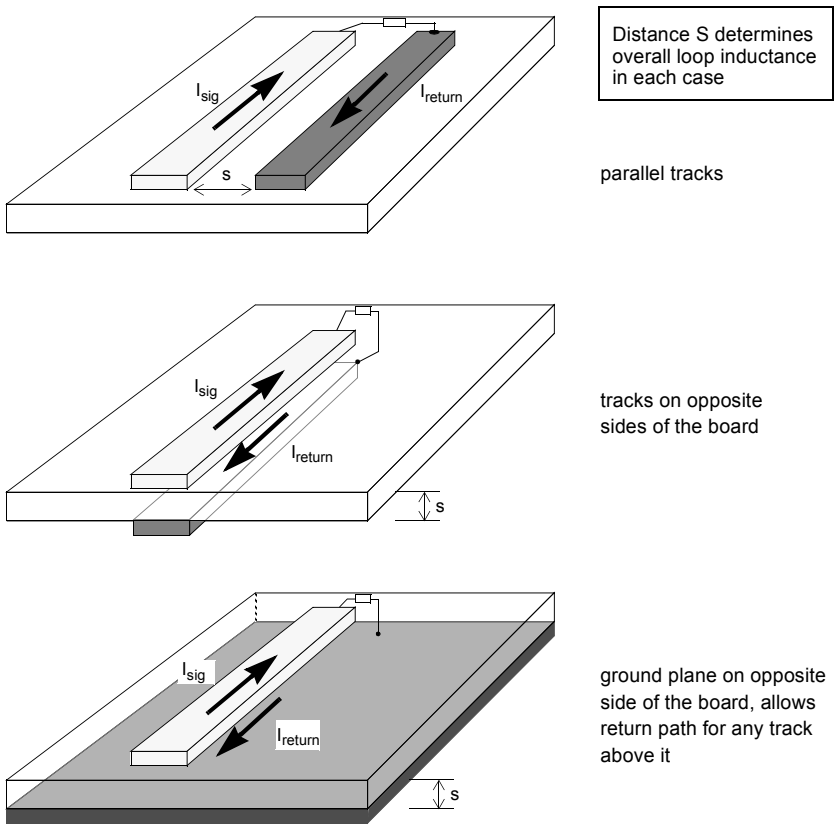


Figure 11.12 Return current paths

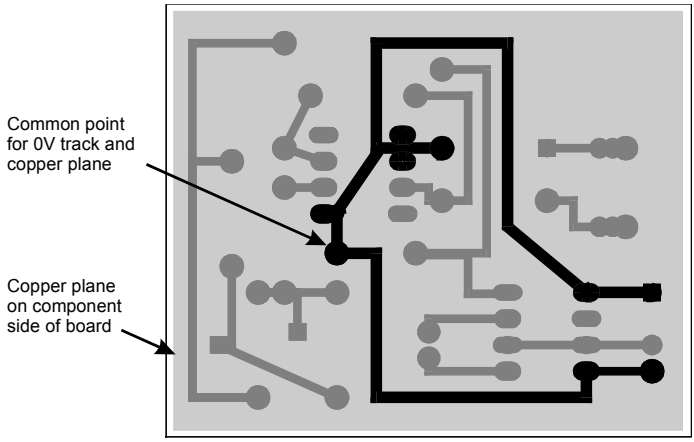


Figure 11.13 Simple copper layer added to a single-sided PCB

a partial electric field screen, reducing the effect of capacitive coupling to the tracks. This is most effective for higher impedance circuits where capacitive coupling is the prime threat. It will also reduce differential voltages across the length and width of the PCB, induced either magnetically or electrically. You can think of it as creating a "quasi-equipotential" area for RF interference over the region of the circuit. The "image plane" discussed in section 14.1.5 works in a similar fashion.

Its effect is maximized if the 0V connection is made in the vicinity of the most sensitive part of the circuit, and if this part of the circuit is located away from the edges of the plane. The purpose of this is to ensure that the remaining interference-induced voltage differences between the plane and the circuit tracks are lowest in the most critical area.

Making the copper layer into a ground plane

If some cost increase is permissible and a double-sided PTH (plated through hole) board can be used, then it is preferable to transfer all 0V current onto the plane layer, which then becomes a true ground plane. All circuit 0V connections are returned to the ground plane via PTH pads and the original 0V track is redundant. In a revised or new layout, the 0V track is omitted entirely, possibly allowing a tighter component and tracking density. Figure 11.14 shows this transition.

This will have the effect not only of reducing capacitive coupling to the circuit, as discussed above, but also magnetic coupling, since all circuit paths now inherently have the least loop area. As long as sensitive circuits are located well inboard of the edges of the plane they will enjoy the greatest protection. Fringing fields at the edge of a ground plane increase its effective inductance, and magnetic coupling to the circuit tracks worsens.

It is not essential that the ground plane area covers the whole of the board, or even all of the tracks, as long as it does cover the tracks and circuit areas which are critical for immunity.

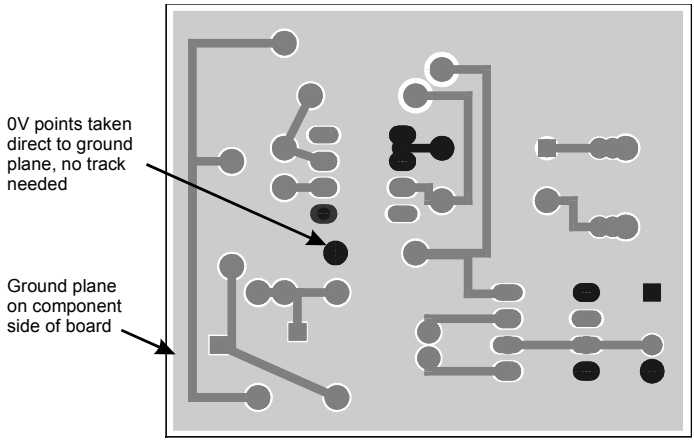


Figure 11.14 Taking all 0V connections to the ground plane

11.2.2.3 Breaks in the ground plane

What *is* essential is that the plane remains unbroken in the direction of current flow. Any deviations from an unbroken plane effectively increase the loop area and hence the inductance. If breaks are necessary it is preferable to include a small bridging track next to a critical signal track to link two adjacent areas of plane (Figure 11.15) – this then develops the layout into a ground grid. A slot in the ground plane will nullify the beneficial effect of the plane if it interrupts the current, however narrow it is. This is why a multilayer construction with an unbroken internal ground plane is the easiest to design, especially for fast logic which requires a closely controlled track characteristic impedance. If you use double-sided board with a partial ground plane, bridging tracks as shown in Figure 11.15 should accompany all critical tracks, especially those which carry sensitive signals a significant way across the board.

The most typical source of ground plane breaks is a slot due to a row of through hole connections, such as required by a SIL or DIL IC package (Figure 11.16). The effect of

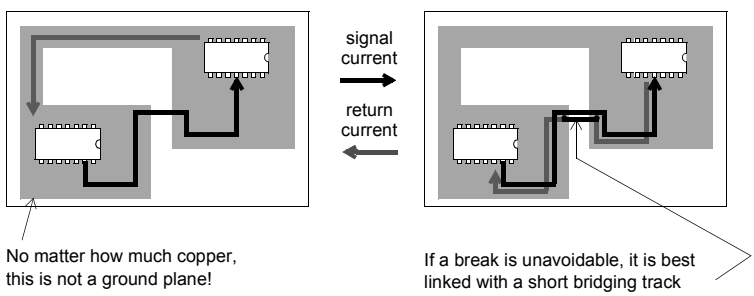


Figure 11.15 A broken ground plane

such a slot is worst for the tracks in its centre, since the return current is diverted all the way to the edge of the slot. This translates to greater ground inductance and an unnecessary increase in induced interference voltage in this area of the board's ground network. If the slot straddles a particularly sensitive circuit then worsened immunity will result, even though you have gone to the trouble of putting a ground plane onto the board. It is a simple matter to ensure that each pair of holes is bridged by a thin copper trace – most etching technology is capable of this degree of resolution – it adds nothing to the production cost and can give several dB improvement in immunity in the best case.

The inductance of a slot in the plane can be modelled as a length of short circuited transmission line. [56] gives an approximation for this inductance as shown in Figure 11.16. It is instructive to compare the order of magnitude of values this gives versus that obtained from equation (11.3): a 3cm track over an unbroken ground plane of width 5cm, 0.8mm above it, gives 0.24nH return path inductance. A 3cm long slot under this track of width 1mm, with 4cm of board either side (i.e. board is 8cm x 5cm), will increase this inductance to 2.6nH.

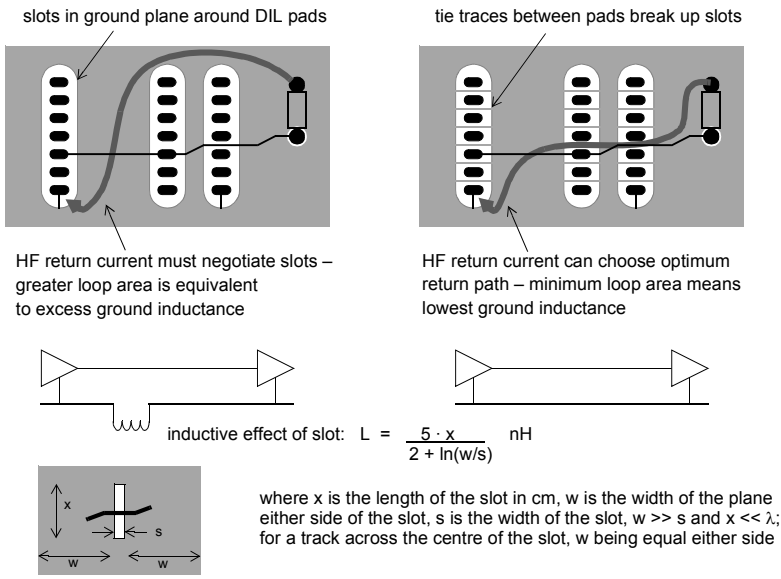


Figure 11.16 Dealing with slots at DIL pinouts

11.2.2.4 Multilayer boards

All of the foregoing, with respect to ground plane construction in the plane of the board, applies to multilayer technology. Additionally, the order of the layers becomes significant when high-speed circuits are implemented on multilayer boards.

In these configurations, the most important aspect is that every critical signal layer should be adjacent to a ground or power plane layer. Also, power and ground planes should be on adjacent layers to take advantage of the inter-layer capacitance for high frequency decoupling. Critical tracks should be routed adjacent to ground rather than power planes, for preference. Such tracks (typically carrying high di/dt signals such as

clocks) should also not jump through vias from one ground reference layer to another, unless the ground layers are tied together with vias at that point. In general, using multiple ground (0V) layers is perfectly acceptable and sometimes essential, but it should be accompanied by via stitching widely distributed around the planes (see also sections 11.2.2.6 and 11.2.2.7 shortly).

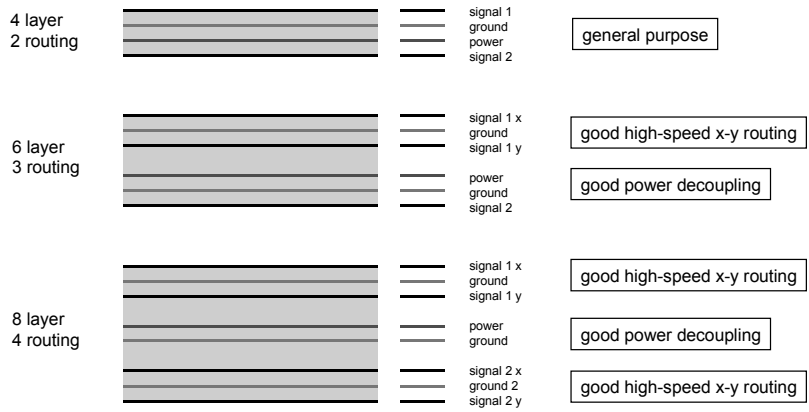


Figure 11.17 Layer stacking on a multilayer board

Figure 11.17 illustrates possible (not by any means mandatory) layer configurations for various layer multiples. If x- and y-orientation layers share a common ground plane this allows both constant impedance and minimum separation from the plane layer for high-speed routing. High-density designs can use more than one set of x-plane-y layers as shown in the 8-layer example above. If high-speed tracks can be distinguished from non-critical ones, the non-critical tracks can be run on a separate layer adjacent to a second plane (marked signal 2 in the six-layer example). In all cases, putting power and ground planes on adjacent inner layers gives maximum distributed decoupling capacitance between them.

The main EMC purpose of a ground plane is to provide a low impedance return path to minimize induced ground noise. Shielding effects on signal tracks are secondary. Putting power and ground planes outside the signal layers on multilayer boards will only be a significant advantage if E-field shielding of the tracks is necessary, and this will in any case be compromised by the unavoidable fields from the components. But an extra ground plane on the outside layer of a board can be helpful when capacitive coupling, such as from large-area components carrying HF voltages, needs to be dealt with by extra shielding measures. [114] describes a situation in which a microprocessor heatsink was electrically bonded to a ground plane on the board (see section 11.2.2.8 later), and the inductance of the bond connection was noticeably more significant when the ground plane was on an inside layer than when it was outside. This resulted in several dB increase in emissions in the frequency range around 1GHz. If your circuit has very wideband EMC aspects then such an approach is worthwhile, but for less demanding applications the physical disadvantages associated with outside plane layers tend to make them unattractive.

11.2.2.5 Crosstalk

A ground plane is a useful tool to combat crosstalk, which is strictly speaking an internal EMC phenomenon. Crosstalk coupling between two tracks is mediated via inductive, capacitive and common ground impedance routes, usually a combination of all three (Figure 11.18). The effect of the ground plane is to significantly reduce the common ground impedance Z_G, by between 40–70dB, in the case of an infinite ground plane compared to a narrow track.

The ground plane may also reduce mutual inductance coupling (M_{12}) by ensuring that the coupled current loops are not co-planar. Capacitive coupling between the tracks will not be directly affected by the ground plane, but the lowered impedance of the line (equivalent to saying that C_{1G} and C_{2G} have been increased) will reduce capacitive crosstalk amplitude.

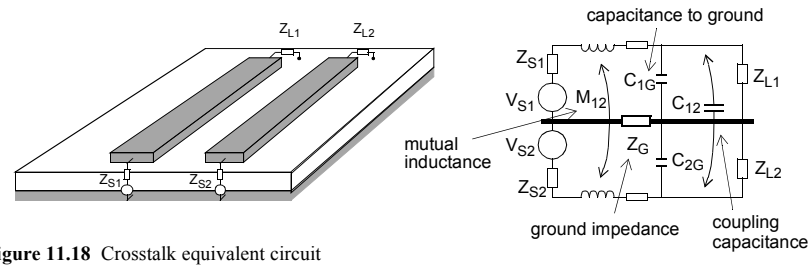


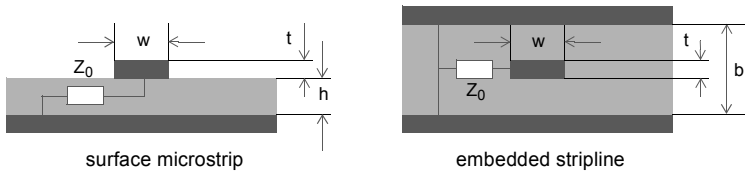
Figure 11.18 Crosstalk equivalent circuit

Crosstalk problems, or internal interference coupling, are by no means limited to digital circuits, although these tend to make the problem most visible. A common threat to the immunity of analogue circuits is crosstalk from other circuits carrying high interference currents or voltages. Mains-borne interference is the most widespread, but RF or transient interference induced onto signal cables can also be significant. You should always be on the lookout to minimize crosstalk from these sources by ensuring the maximum separation (hence minimum M_{12} and C_{12}) between the circuits; or by interposing electric field screening between them, if C_{12} is dominant; or by implementing a ground plane, to minimize Z_G and maximize C_{1G} and C_{2G}.

11.2.2.6 Constant impedance track layers

High frequency circuits need matched impedances – see section 12.1.2.4. When an HF signal has to be passed across a board without distortion due to variations in the geometry of the tracks carrying it, these have to be designed as transmission lines with a known, constant impedance. This invariably means that they should be placed on a layer next to a reference ground plane and should remain on that layer for the whole of their run: any vias which might take them to another layer represent a discontinuity in impedance, as would any jump to another reference plane. The characteristic impedance looking along the line is determined entirely by the cross-sectional geometry, and so the same geometry has to be maintained for the total length. No variations in width (w) or separation (h) from the ground plane are permissible.

Various equations have been published which offer a simple analytical way to calculate the characteristic impedance of a given geometry, but these are always approximations, valid over restricted dimensional ranges (typically worse for larger w/h), and are subject to varying degrees of error. Complicated equations are usually more accurate, and numerical modelling rather than analytical calculation gives the



Approximate widths for given impedances: t = 35µm, ε_r = 4.2

	w mm for surface microstrip		w mm for embedded stripline	
Z_0 Ω	h = 0.25 mm	h = 0.5 mm	b = 0.3 mm	b = 0.6 mm
30	0.77		0.21	0.47
50	0.43	0.9	0.09	0.21
70	0.23	0.5		0.09
90	0.12	0.28		
100		0.2		

Figure 11.19 Track geometries and impedances (see Annex D section D.5.3 for equations)

most accurate result [42]. Several proprietary software packages are available to perform this modelling, using the geometry to determine the per-unit-length inductance and capacitance L_0 and C_0 and then calculating Z_0 from $Z_0 = \sqrt{(L_0/C_0)}$. Some equations for the more common configurations are given in Appendix D (section D.5.3), and Figure 11.19 shows some figures for typical applications using these equations.

You can see from this that surface microstrip lines are more suited to higher impedances than embedded striplines; the latter are more suitable for high energy clocks simply because the use of two reference planes encloses the magnetic field radiation more effectively. Single-ended line configurations are shown above; a differential transmission line formed from two striplines or microstrips against a common ground plane is harder to model because of the coupling between the two lines. If they are widely separated such that the coupling between them is low, the differential characteristic impedance $Z_{0(diff)}$ can be approximated by twice the Z_0 of each half of the pair. For closer pairs with greater mutual coupling then $Z_{0(diff)} = 2 \cdot Z_0 \cdot (1 - k)$ where k is the coupling factor between them.

The impedances depend on practical dimensions of w and h and also on the exact relative permittivity ε_r of the board material. Each of these is subject to some error, for instance ε_r is generally given at 1MHz by default whereas a track's Z_0 is of most interest in the range above 500MHz; at these frequencies ε_r can fall by typically 5%. The value depends on the glass-to-resin content of fibreglass materials and different materials of the same generic type can vary by several percent. Also the specified width of a track is subject to deviations in the PCB manufacturing process, as is the thickness of the layers. Even with the narrowest production trace width, striplines and microstrip cannot achieve high impedances: a practical range of impedances is between 50 and 100 ohms. In all cases, high impedances require large separations and hence very thick dielectrics, making PCBs excessively thick. Lower values are easier to achieve but the track width with thin separations becomes unwieldy in practical layouts.

For all these reasons, and because PCB manufacturers are themselves normally in the best position to determine the actual Z_0 of tracks on their boards, a usual approach

is to specify on the PCB drawing the actual intended impedance of tracks of a given width on a specified common impedance layer.

11.2.2.7 Power planes

The subject of power planes raises two issues:

- should they be board-wide or segmented into islands?
- how should they be coupled to the ground plane?

The assumption is that the ground (0V) plane is the reference for the whole circuit. Then each supply (there may be more than one supply voltage) needs to be decoupled to this 0V. Such decoupling is most effective if the power plane is on the next layer to a 0V plane, and if the separation distance is minimized. This gives maximum capacitance between the two, or to put it another way, it creates a transmission line structure with the lowest possible Z_0. So given a single 0V plane on an inner layer, this allows a maximum of two power plane layers within the same area (one each side of the 0V plane, see Figure 11.20).

Doing this will of course deny the 0V plane to any signal tracks that might need it; so in practice, if you have more than one supply voltage to a VLSI IC, you will need at least two 0V plane layers, one for the power supplies and one for the signals. Yet more supply voltages will need further 0V planes, or will compromise the decoupling of some of the power planes. Multiple 0V planes need many stitching vias in order to maintain the lowest high frequency voltage differential between them. If at any point you choose to allow tracks to jump from a layer next to one plane to a layer next to another, at least one via next to the jump is mandatory to keep integrity of the return current path.

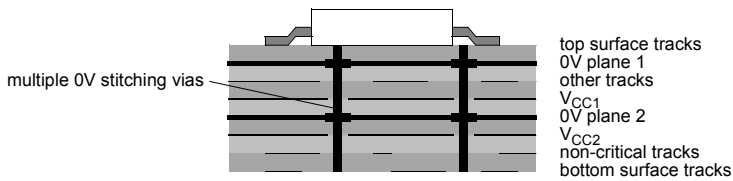


Figure 11.20 Layer stack-up for two supply planes

Segmentation

The mention of transmission lines above gives a hint of the problem that can be caused by a single large power plane – particularly one (say 3V3 or 5V) that spreads across the whole PCB and mirrors the 0V plane. This creates a transmission line "sandwich" that will have principal resonances determined by its x and y dimensions. At the resonant frequencies two undesirable things happen: the impedance between V_{CC} and 0V becomes high at certain positions around the board, and the radiating efficiency of the edges of the sandwich is maximized. The resonant frequencies are affected by the dielectric between the planes. For FR4 with $\varepsilon_r = 4.2$, the frequency is reduced by $\sqrt{4.2}$ from the free-space value, so a board with dimensions 30cm x 12cm will have a bare-board resonance in the y direction of 610MHz and in the x direction of 244MHz. Clock energy at these frequencies will radiate effectively, and RF susceptibilities can be expected to be worst at the same frequencies.

The solution to this problem is, firstly, not to allow the power plane to exactly mirror the 0V plane; if the power plane edge is inset from the ground plane edge by at least 10 · h (Figure 11.21) then the radiating efficiency of the edges of the resulting transmission line is noticeably reduced. But beyond this, consider breaking a large, homogeneous area of power plane into islands. Separating a large plane into individual smaller planes, each with its own decoupling capacitors and supplied via an isolating series choke, pushes the transmission line resonances typically into the GHz region where they are likely to be less harmful. It also reduces cross-coupling via the power plane of different circuits on the board, and reduces the spread of V_{CC} noise across the board. The series chokes – for instance, surface mount ferrites – need only have a few tens of ohms impedance in the VHF range to be effective at segregating the individual planes. The segmentation boundaries should follow natural divisions in the circuit structure, particularly with respect to clock distribution, as far as possible.

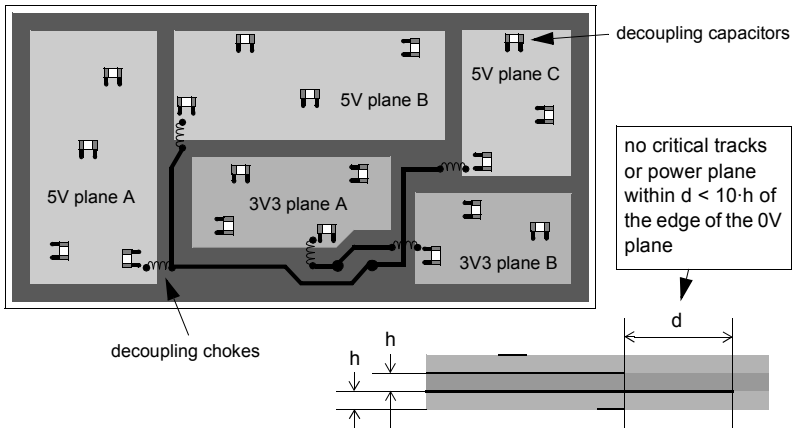


Figure 11.21 Power plane segmentation and the 10 · h rule

This segmentation approach is not appropriate for ground planes, which should always be continuous over the whole PCB.

As we have seen, several aspects of the EMC performance depend on the layer separation distance, so that the detail of the vertical sandwich construction of the PCB can be as important for its EMC as is the layout. The separation is determined by the thickness of the pre-preg and core materials used in the build of the bare board. This is often left to the PCB manufacturer and is not specified by the circuit designer, or anyone else. As a result you end up with the default thicknesses used by a particular board supplier, which might be perfectly adequate for the EMC performance of the product and so is never questioned; but if another board supplier is chosen during the product life cycle, it is entirely possible that a different set of thicknesses could be used which result in changed performance. To guard against this, make sure that you specify layer thicknesses in the PCB drawing, if necessary checking with your preferred supplier what their defaults will be.

11.2.2.8 Heatsinks on PCBs

Heatsinks can be a particular cause of EMC difficulties on PCBs. The subject is touched on again in section 12.1.5.2 on SMPS design. Here, the concern is the effect of stray

capacitance from heatsinks on digital devices carrying RF voltages, such as microprocessors and ASICs.

Consider a simplified equivalent circuit of a PCB with a 0V plane, a processor, a heatsink on the processor, and an enclosure around the whole assembly (Figure 11.22).

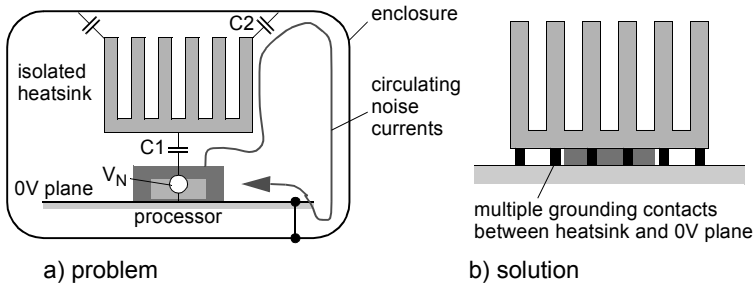


Figure 11.22 Heatsinks on processors

The processor is the source of the RF noise: voltages V_N on the silicon at clock frequencies appear with respect to the 0V plane and are capacitively coupled directly to the metal of the heatsink. The heatsink must have good thermal contact to the chip, and a by-product of this is a high coupling capacitance C1. In its turn, the heatsink is a large chunk of metal, and it has a high capacitance C2 to its surroundings, particularly the enclosure.

The effect of this is to energize the entire enclosure with circulating currents at the clock frequency and its harmonics. Any weakness in the enclosure will allow these frequencies to radiate. To control this, the most effective measure is to prevent the heatsink from carrying high levels of clock noise. This means it must be grounded to the 0V plane on the PCB, and cannot be allowed to float. Capacitance C1 and noise source V_N cannot be removed, but if the heatsink is grounded then the circulating noise currents remain in its locality and the voltage on the heatsink is minimized. The enclosure itself is not stressed, since C2 is not fed from a noise source.

The catch with this is that any grounding inductance resonates in parallel with the capacitance of the heatsink so that at the resonant frequency, even a supposedly grounded heatsink will carry high levels of noise and couple them out to the enclosure. A heatsink self-capacitance of 10pF and an inductance of 3nH (no more than a few mm of grounding contact) results in a resonant frequency of 900MHz, which could well be troublesome for many types of processor. If you take the above advice, ground the heatsink at one point and the emissions at some frequencies go up, this is most probably what is happening. The inductance of the grounding connection needs to be well below 1nH to be effective, and this means that many grounding contacts around the outside of the heatsink must be provided, not just one or two. The most effective designs use a continuous conductive gasket around the periphery of the heatsink (which must be conductively finished) to a ground plane contact strip on the surface of the PCB.

11.2.3 Configuring I/O and circuit grounds

11.2.3.1 The interface ground structure

Decoupling and shielding techniques to deal with common mode currents appearing on cables both require a “clean” ground area, not contaminated by internally generated

noise, and to which external disturbances can be filtered to prevent them passing into the circuit. This forms the low transfer impedance grounding structure, as per section 11.1.2.2, for the cable interface. *Filtering at high frequencies is next to useless without such a ground*. Unless you consider this as part of the layout specification early in the design phase, such a ground will not be available. Provide an interface ground by grouping all I/O leads in one area, and connecting their shields and decoupling capacitors to a separate ground plane in this area. This interface ground plane can be on a separate part of the main circuit PCB [106] as shown in Figure 11.23, or it can be a metal plate on which the connectors are mounted. The external ground (which may be only the mains safety earth) and the metal or metallized case, if one is used, are connected here as well, via a low inductance link. It is also possible for the interface to be an entire PCB in itself, with an integral ground plane to which the filter components and cable screens are connected and which is then connected to an external metal or metallized chassis via suitable gaskets or other forms of bonding. The filtered signals and power are then passed through to internal PCBs via a board-to-board connection. Figure 11.24 shows a typical arrangement for a product with digital, analogue and interface sections.

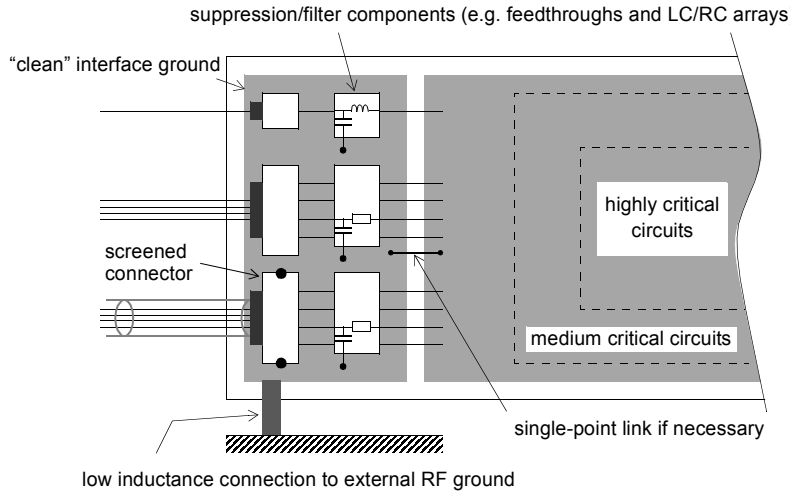


Figure 11.23 The interface ground on a PCB

This interface ground should only connect to the internal circuit ground, if at all, at one point. This prevents noise currents flowing through the interface ground plane and "contaminating" it. No other connections to the interface ground are allowed. As well as preventing common mode emissions, this layout also shunts incoming interference currents (transient or RF) to the interface ground and prevents them flowing through susceptible circuitry. If for reasons of enclosure design it is essential to have cables interfacing with the unit or PCB at different places around its periphery, you should still arrange to couple them all to a separate ground structure through which no circuit currents are flowing. In this case a chassis plate is mandatory.

These requirements can be ensured by devoting an area along one edge of the PCB to the interface ground plane, including the I/O resistive, capacitive and inductive

filtering and suppression elements on it (but no other circuits), and separating the circuit 0V from it either absolutely, or by a single connecting link. RF-critical circuitry should be widely separated from the I/O area.

For ESD protection the circuit ground *must* be referenced to the chassis ground; this prevents transient high voltages appearing between the two and creating a secondary discharge (*cf* sections 10.3.3.3 and 12.2.1.2). This can easily be done by using multiple plated-through holes to the ground plane and metallic standoff spacers. If there has to be DC isolation between the two grounds at this point, use a 10–100nF RF ceramic capacitor at each location. You can provide a clean I/O ground on plug-in rack mounting cards by using wiping finger style contacts to connect this ground track directly to the chassis.

11.2.3.2 Separate circuit grounds

There are two schools of thought as to maintaining separate 0V references for different operational parts of a circuit. The first (see Figure 11.24) says that you should never extend a digital ground plane over an analogue section of the PCB as this will couple digital noise into the analogue circuitry. A single point connection between digital and analogue grounds can be made at the system's analogue-to-digital converter. It is very important in this arrangement *not* to connect the digital circuitry separately to an external ground [46]. If you do this, extra current paths are set up which allow digital circuit noise to circulate in the clean ground.

Interfaces directly to the digital circuitry (such as a port input or output) should be buffered so that they do not need to be referenced to the digital 0V. The best interface is an opto-isolator or relay, but this is of course expensive. When you can't afford isolation, a separate buffer IC which can be referenced to the I/O ground is preferable;

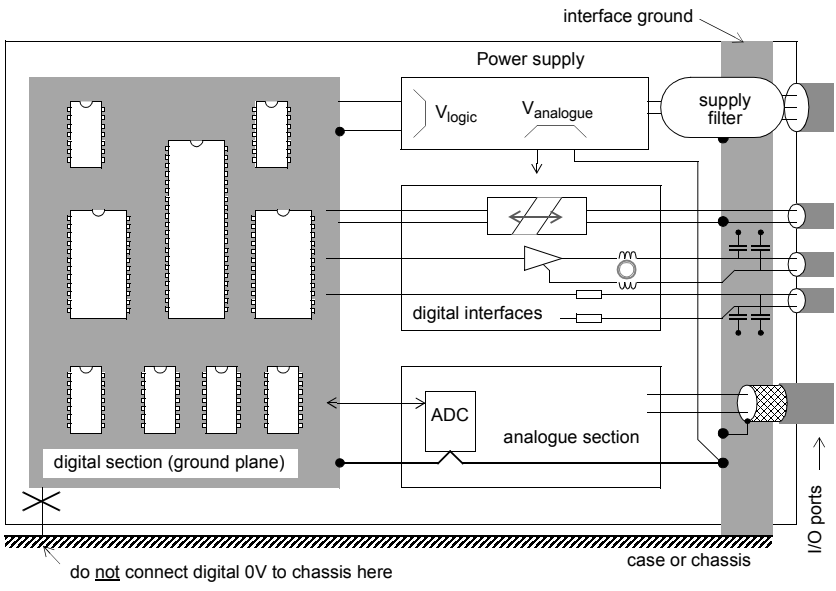


Figure 11.24 Multiple ground areas

otherwise, buffer the port with a series resistor or choke, and decouple the line *at the board interface* (not somewhere in-board) with a capacitor and/or a transient suppressor to the clean ground. More is said about I/O filtering in section 13.2.4.

Notice how the system partitioning, discussed in section 11.1.1, is essential to allow you to group the I/O leads together and away from the noisy or susceptible sections. Also the mains cable, as far as EMC is concerned, is another I/O cable. Assuming that you are using a block mains filter, fit this to the "clean" ground reference plate directly.

11.2.3.3 Solid universal circuit ground

The second school of thought, diametrically opposed to the first, says that all parts of the circuit should be referenced to a single, unbroken 0V reference plane. If this approach is chosen, it is crucial that a high quality, low impedance plane is used; any 0V tracks would be unacceptable. The effect of this construction is that all signal and power return currents flow in the plane, so that common impedance coupling between different parts of the circuit is unavoidable, and it is only careful layout and the low impedance of the plane which mitigates this coupling to an acceptable extent. Mixing sensitive analogue with high-speed digital circuits on the same board is risky, although with careful partitioning it can still be successful.

But in an unscreened product, the PCB is exposed directly to the RF environment and multiple planes will act as effective dipole antennas, concentrating induced interference at their junctions, or radiating fields due to voltage differences between them. The advantage of a single plane is that there is no opportunity for voltage differences to arise, as a result of interference or for any other reason, between different 0V nodes, since there are no different nodes. The tricky question of where exactly to place the separation boundary is avoided. So is the hazard of 0V differentials, potentially a problem with the first approach. If the board is mounted on a metal chassis, the ground plane can be tied to this chassis at multiple points, and this improves the RF "solidity" of the whole assembly, so that induced interference currents will inherently cause a lower level of internal disturbance.

In the end, you are free to use either approach, as long as the implications of the decision are appreciated. Segregation of grounds removes the threat of cross-interference between different parts of the circuit but requires you to think carefully about placing the boundaries and defining the circuit's relationship to the chassis; with complex multi-sectioned circuits it can be difficult to administer. Unifying the ground makes it easy to control the ground design but increases the risk of one part of the circuit interfering with another.

11.2.3.4 Cable screen connection

Input/output decoupling is of critical importance with either circuit grounding regime because it is vital to keep cable common mode interference currents to a minimum. As an example, consider Figure 11.25. If the cable screen or return is taken to the wrong point with respect to the output driver decoupling capacitor, the high-speed current transitions on the driver supply (which flow through the decoupling capacitor traces) generate common mode voltage noise V_N which is delivered to the cable and which appears as a radiated emission. Cable screens must always be taken to a point at which there is the minimum noise with respect to the system's ground reference. This means that the dedicated interface ground area must always be implemented and all cable connections either taken directly to it (screens) or filtered to it (signal and power lines).

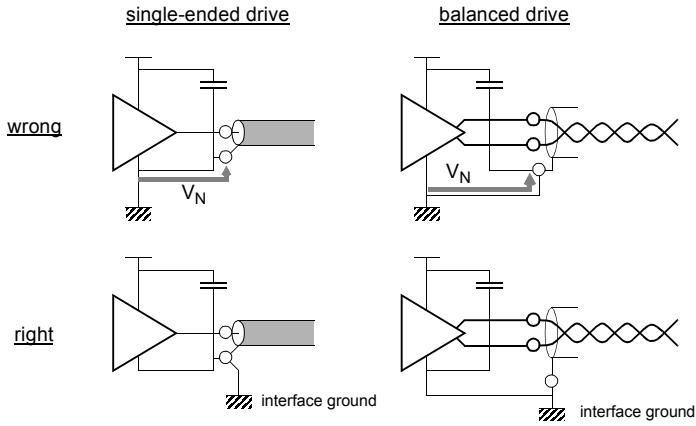


Figure 11.25 The point of connection of I/O cable screens

11.2.4 Rules for PCB layout

Because it is impractical to optimize the PCB layout for all individual signal circuits, you have to concentrate on those which are the greatest threat. These are the ones which carry the highest di/dt most frequently, especially clock lines and data bus lines, and square-wave oscillators at high powers, especially in switching power supplies. From the point of view of susceptibility, sensitive circuits – particularly edge-triggered inputs, clocked systems, and precision analogue amplifiers – must be similarly treated. Once these circuits have been identified and partitioned you can concentrate on dealing with their loop inductance and ground coupling. The aim should be to ensure that circulating ground noise currents do not get the opportunity to infect the system.

A structured approach to PCB layout for EMC

These rules can at least partly form the basis for an in-house EMC design policy and design review checklist; some can be implemented in a CAD design rule checker. They assume that you will use at least one 0V (ground) plane.

Before routing begins,

- identify and label high di/dt circuits
- identify and label sensitive circuits
- identify 0V plane(s) including separate areas
- identify power plane segments
- identify the interface ground plane
- decide on layer stack-up:
  - identify 0V plane layers
  - identify constant impedance layer(s)
  - identify power plane layer(s), next to 0V plane: some of these may also carry tracks in areas where power planes aren't needed

- check component placement to ensure:
  - no unnecessarily long track routes
  - no proximity of noisy components to sensitive ones
  - critical circuits away from ground plane edge
  - maximum partitioning of interfaces and functional sections: no unprotected interface routes to pass close to operational circuits
  - all filter components at the interface they are protecting
- board-to-board connections: ground pins should be distributed along multi-way connectors close to high-speed or sensitive signals
- identify points for bonding the ground plane(s) to chassis

During routing,

- ensure no tracks cross any breaks in a 0V plane
  - if they must, then make sure series buffer resistors are placed appropriately at the break
- flag any breaks or gaps in a 0V plane and decide whether they are necessary or can be minimized
- check that critical and constant-impedance tracks do not swap layers
  - if they must, they should be routed above or below a single 0V plane, not jump to a different 0V plane
- check adequate placement of decoupling capacitors
  - near device power pins
  - minimum inductance track/via layout
- ensure that interface filtering and transient protection is tracked with low inductance to the interface ground plane
- identify and control common impedance current paths for power switching circuits and sensitive wideband circuits
- check implementation of $10 \cdot h$ rule for power planes and critical tracks versus the ground plane edge
- for balanced differential signal track pairs, confirm that adequate balance is maintained along the entire run – separation of at least $3 \cdot h$ from other tracks is usually enough
- minimize surface areas of nodes with high dv/dt
- if empty areas of any layer are flood filled with copper, ensure that each such area is connected to 0V, not floating

If you have to design a PCB without a 0V plane,

- identify critical (high-current, high di/dt or sensitive) circuit loops, including the appropriate segment of the 0V track
- minimize enclosed loop areas in these loops
- flood-fill and mesh the 0V tracks as much as possible