Lecture Notes

Dated-08/10/13

Master-Slave Latch(Revision)

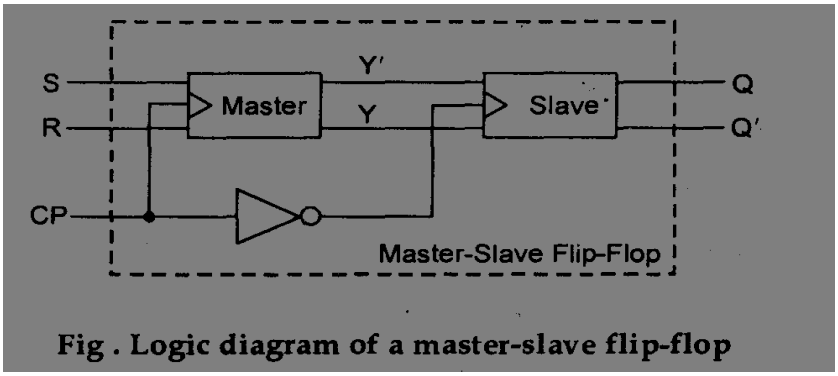


Fig . Logic diagram of a master-slave flip-flop

- When clock =1 then clock in slave =0

1.Master Latch behaves as normal RS latch.

R	S	Q_{M+1}
0	0	Q_M
0	1	1
1	0	0
1	1	illegal

2. Slave latch is in hold condition as RS=00(hold)

3. As long as clock=1,the changes in input values of R and S will affect only Q_M and Q_S remains unchanged.

- **When clock=0,**

1. **Master is on hold condition as RS=00.**
2. **Clock input =1 for slave latch.**

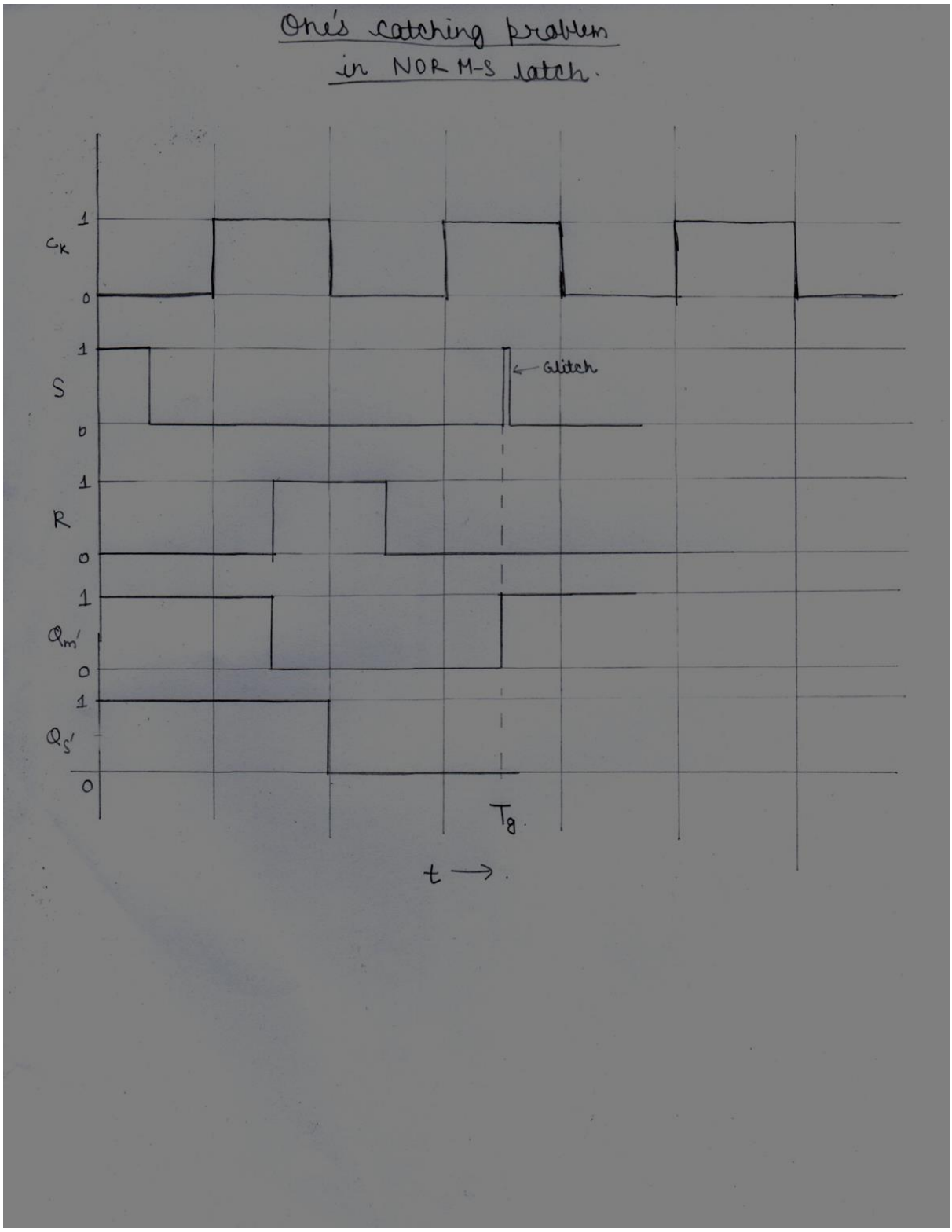
3. **In slave latch,**

$R=Q^{C}_{M}$

$S=Q_M$

4.If Q_M=0, then R_s=1 and S_s=0 => Q_s =0 (Reset Condition) and vice-versa.

- **Output of Master-Slave latch can only be changed when clock=1.**
- **Whatever was the last input before clock becomes 0 is captured by Master-Slave latch and output of Master Latch will be passed to Slave Latch.**
- **This combination is called Negative Edge Triggered Master-Slave Latch Combination.**
- **For the outside world, only the output of the Slave latch is available.**
- $Q_{S+1} = S_M + R_M{}^{C} Q_S$
- **Output of Master – Slave latch is available when clock completes its cycle.**



ONE'S CATCHING PROBLEM

- **One's catching problem arise in MASTER SLAVE LATCH made up of NOR gates, i.e NOR M-S LATCH.**

- **RS latch made up of two NOR gates holds previous state when the inputs are 0 as it has HOLD STATE at R=S=0.**
- **If now set transitions to 1 then we get the state S=1 and R=0 which is the set condition.**
- **If set subsequently transitions back to 0, then again the HOLD STATE will be reached and it will now hold the value which was set previously.**
- **Now in the above fig at time Tg the set glitches and jumps to 1 and then back to 0 quickly,**
- **Whe the set glitches to 1 the state S=1 and R=0 is reached which is the SET condition so Qm gets set to 1.**
- **Now subsequently when S gets back to 0 the state S=0 and R=0 is reached which is the HOLD CONDITION, the state with Qm=1 will be held instead of the state with Qm=0**
- **I.E The latch catches the 1 even though the transition is very quick.**
- **To avoid one's catching problem the easiest solution is to set S != R. As the condition S=R=0 will vanish, hence no hold condition occurs at the RS latch and hence there will be no catching problem.**

ZERO'S CATCHING PROBLEM

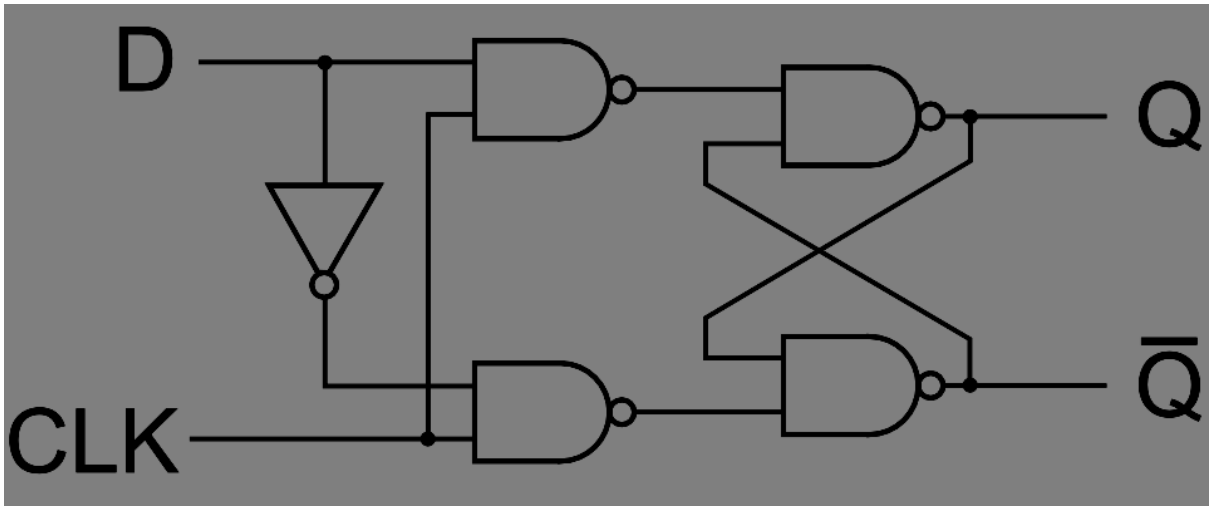
- **Zero's catching problem arise in NAND M-S-LATCH.**
- **Latch made up of NAND gets hold previous stae when the inputs are 1. As it's HOLD STATE occur at S=1, R=1**

- **Its SET CONDITION is S=0, R=1.**
- **If there's a glitch that makes the transition from S=1 to S=0, then the latch may catch the 0 and set the value of Q.**
- **To avoid zero's catching problem the easiest solution is to set S != R. As the condition S=R=1 will vanish, hence no hold condition occurs at the latch and hence there will be no catching problem.**

This can be achieved using D flip flop.

D Flip Flop

Fig:-

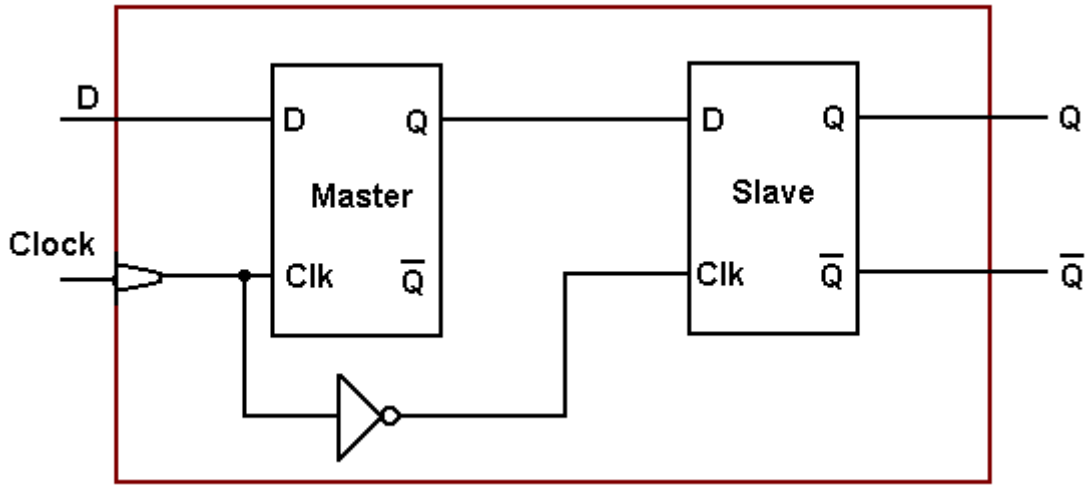


D-Flip flop using NAND gates

Characteristics:-

- **Shifts one bit of data from input to output.**
- **Only One input required**
- **$Q_{N+1} = D_N$**

Master Slave Latch using D Flip Flop



When Clock=1 ,i.e Master Active-

1. **$R_M = D^C$ and $S_M = D$**
2. **$Q_{S+1} = D$**

   Proof:

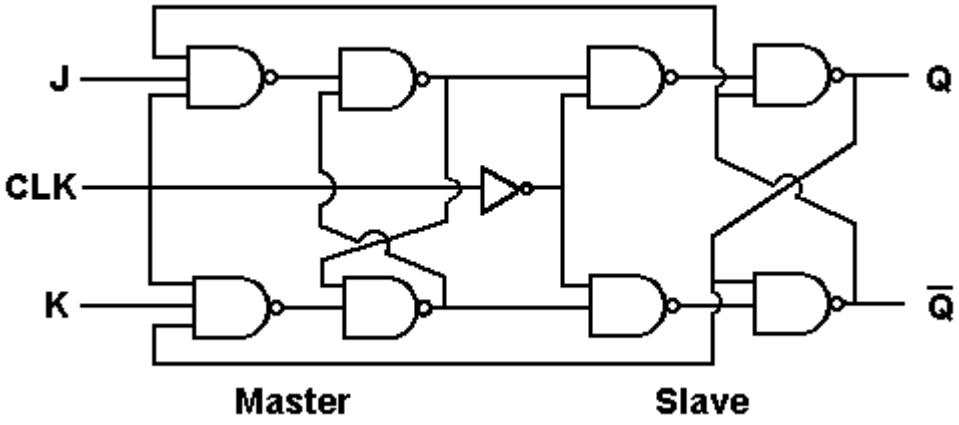
   $Q_{S+1} = S_M + R_M^C Q_S$

   $= D + D Q_S$ (Since $(D^C)^C = D$)

   $= D(1 + Q_S)$

   $= D$

Master Slave Latch using J –K Flip Flop



- **It is same as the R-S flip –Flop except we can also give J=1 and K=1 as input.**

- **When J=1 and K=1, $R_M = Q_S$**

  $S_M = Q_S^C$

  $Q_{s+1} = Q_S^C$

  Proof : $Q_{S+1} = S_M + R_M^C Q_S$

  $= Q_S^C + Q_s^C Q_S$

  $= Q_S^C (1+Q_S)$

  $= Q_S^C$

  Hence output will toggle.

- In **General, $S_M = JQ_S^C$ and $R_M = KQ_S$**
  - **$Q_{s+1} = JQ_S^C + K^C Q_S$**

    Proof: $Q_{S+1} = S_M + R_M^C Q_S$

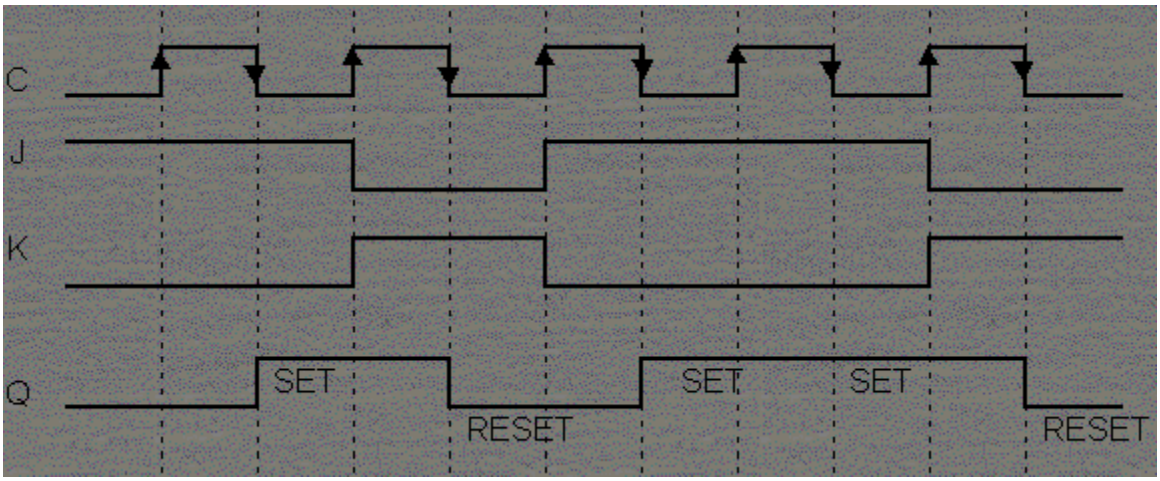
    $= JQ_S^C + (KQ_S)^C Q_S$

    $= JQ_S^C + (K^C + Q_S^C)Q_S$

    $= JQ_S^C + K^C Q_S + Q_S^C Q_S$

    $= JQ_S^C + K^C Q_S$

Timing Diagram For JK Master Slave Flip Flop



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