DIGITAL DESIGN SCRIBE

05/11/2013

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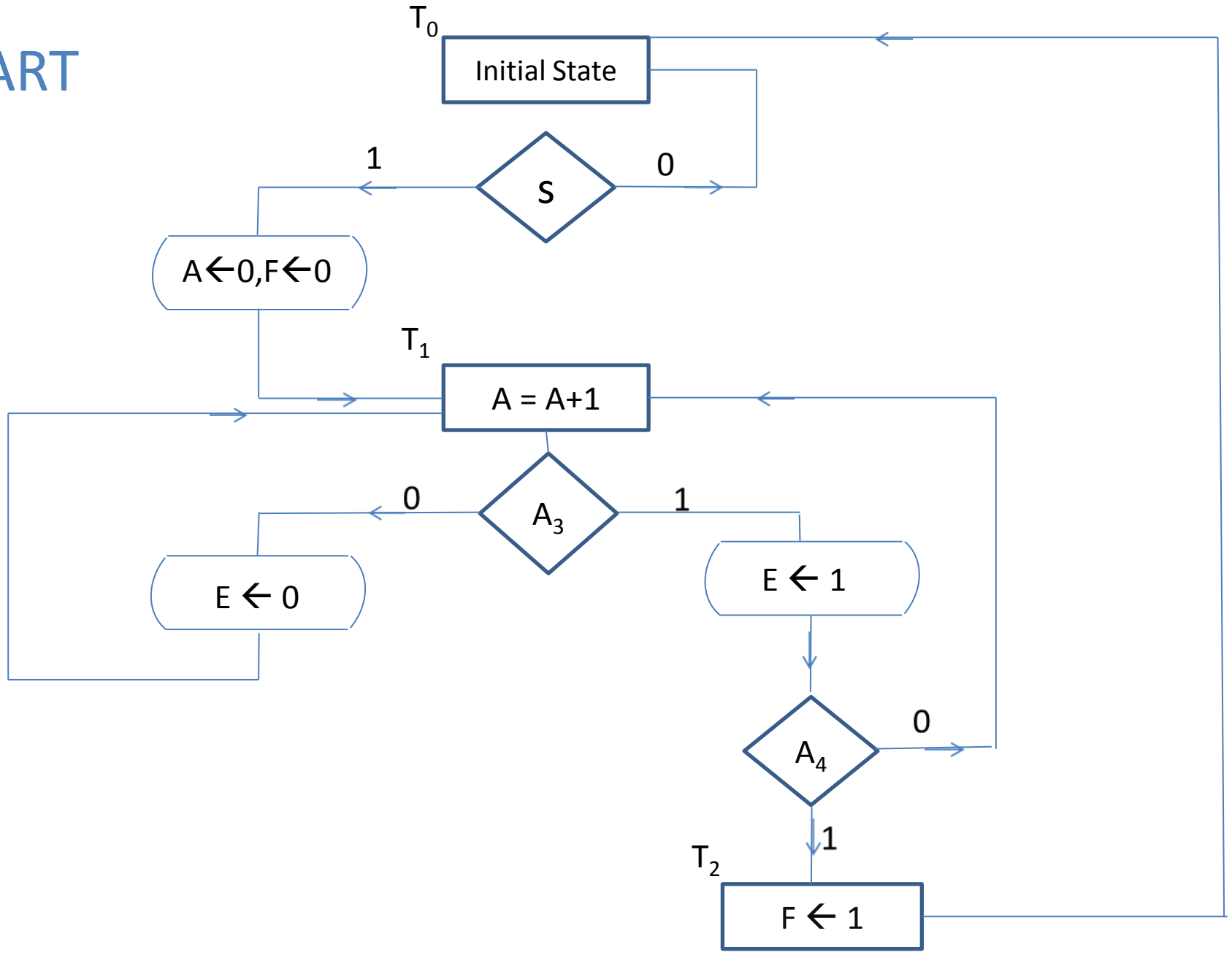
Continued from Previous Scribe

Q. Given two flip-flops E and F and a four bit binary counter (A_4 A_3 A_2 A_1), develop an ASM chart such that if A_3=0, E is cleared (E=0) and count continues if A_3=1, E is set to 1 and then if A_4=0, count continues but if A_4=1, F set to 1 on next clock so stop counting. Then, if S=0, stay in initial state but if S=1, repeat operation cycle where S is another start signal i.e. if S=1 reset to: A=0, F=0 .

To Design the ASM for the given question :-

1. Draw the ASM Chart.
2. Make the ASM transition table.
3. Design the F.S.M for the Control Logic Box.
4. List the register transfer operations.
5. Put together the above components to design the ASM.

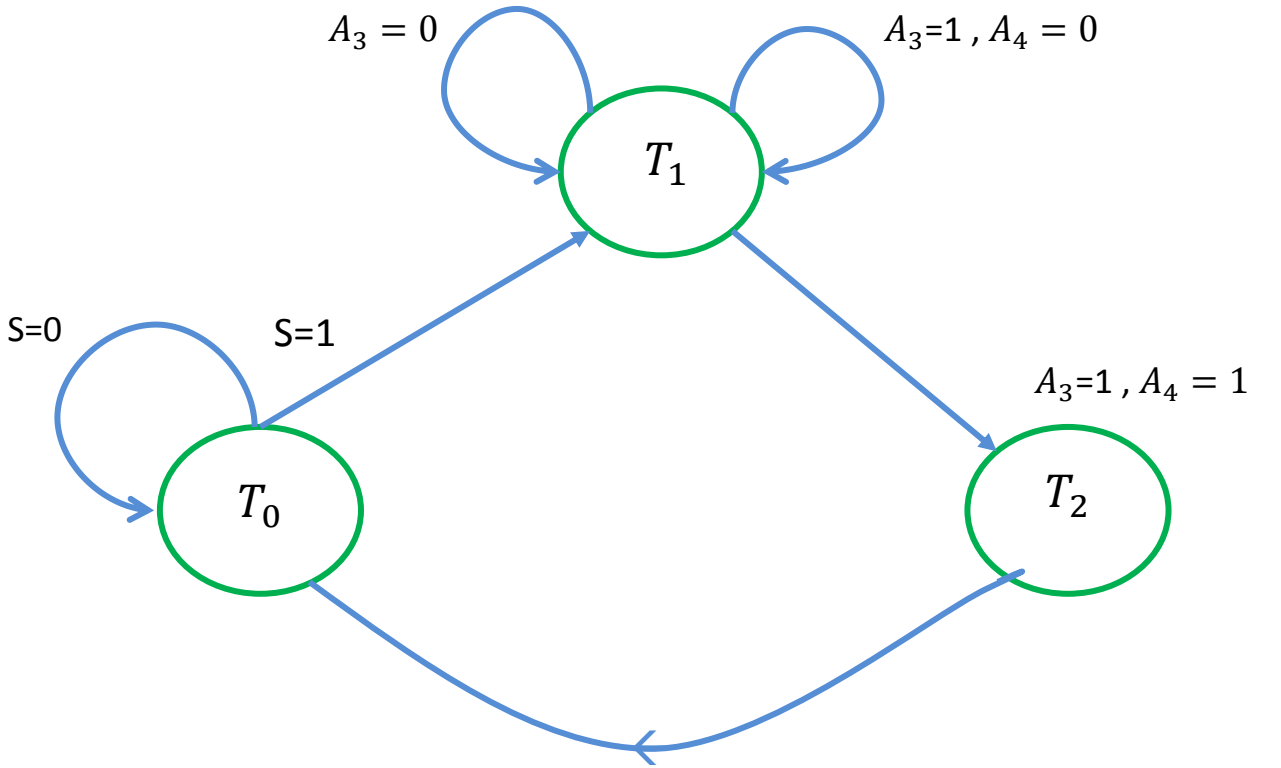
ASM CHART



ASM Transition Table

Counter				Flip-Flops		Conditions		State
A4	A3	A2	A1	E	F			T1
0	0	0	0	1	0	A3=0	A4=0	T1
0	0	0	1	0	0	A3=0	A4=0	T1
0	0	1	0	0	0	A3=0	A4=0	T1
0	0	1	1	0	0	A3=0	A4=0	T1
0	1	0	0	0	0	A3=0	A4=0	T1
0	1	0	1	1	0	A3=1	A4=0	T1
0	1	1	0	1	0	A3=1	A4=0	T1
0	1	1	1	1	0	A3=1	A4=0	T1
1	0	0	0	1	0	A3=1	A4=0	T1
1	0	0	1	0	0	A3=0	A4=1	T1
1	0	1	0	0	0	A3=0	A4=1	T1
1	0	1	1	0	0	A3=0	A4=1	T1
1	1	0	0	0	0	A3=0	A4=1	T1
1	1	0	1	1	0	A3=1	A4=1	T1
1	1	0	1	1	1	N/A		T2

State Diagram for Control Logic



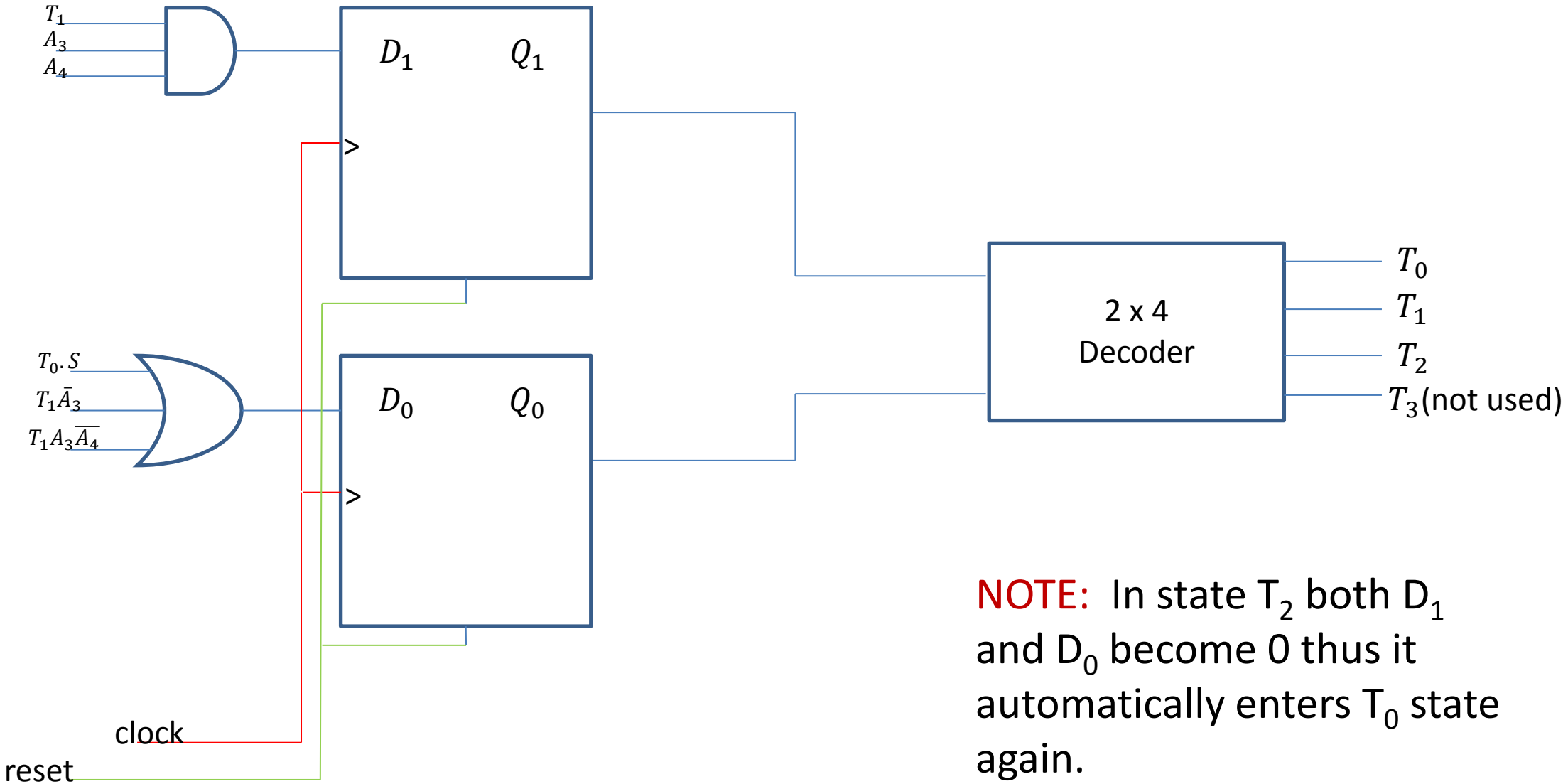
State Table for Control Logic Box

PS	S	A_3A_4	NS	T_0	T_1	T_2
0 0	0	x x	0 0	1	0	0
0 1	x	1 0	0 1	0	1	0
1 0	x	x x	0 0	1	0	0
0 0	1	x x	0 1	0	1	0
0 1	x	0 x	0 1	0	1	0
0 1	x	1 1	1 0	0	0	1

T_0=00
T_1=01
T_2=10

- $D_1 = T_1.A_3.A_4$, $D_0 = T_0 + T_1.\bar{A}_3 + T1.\bar{A}_4$
- The flip flop inputs depend on A_3, A_4 and the present state (PS).
- Note that we have used T_0, T_1, T_2 to represent the states.
- So we need a decoder to get the outputs.
- Thus we use **sequence register and decoder** logic to design the Control Logic Box.

CONTROL LOGIC BOX



NOTE: In state T_2 both D_1 and D_0 become 0 thus it automatically enters T_0 state again.

Register Transfer Representation

Mention only about the data operations occurring in a state .

- T_0 : if (S = 1)

  then A = 0 , F = 0
- T_1 : A ← A+1

  if (A_3 = 0) then E ← 0

  if (A_3 = 1) then E ← 1
- T_2 : F ← 1

Note:

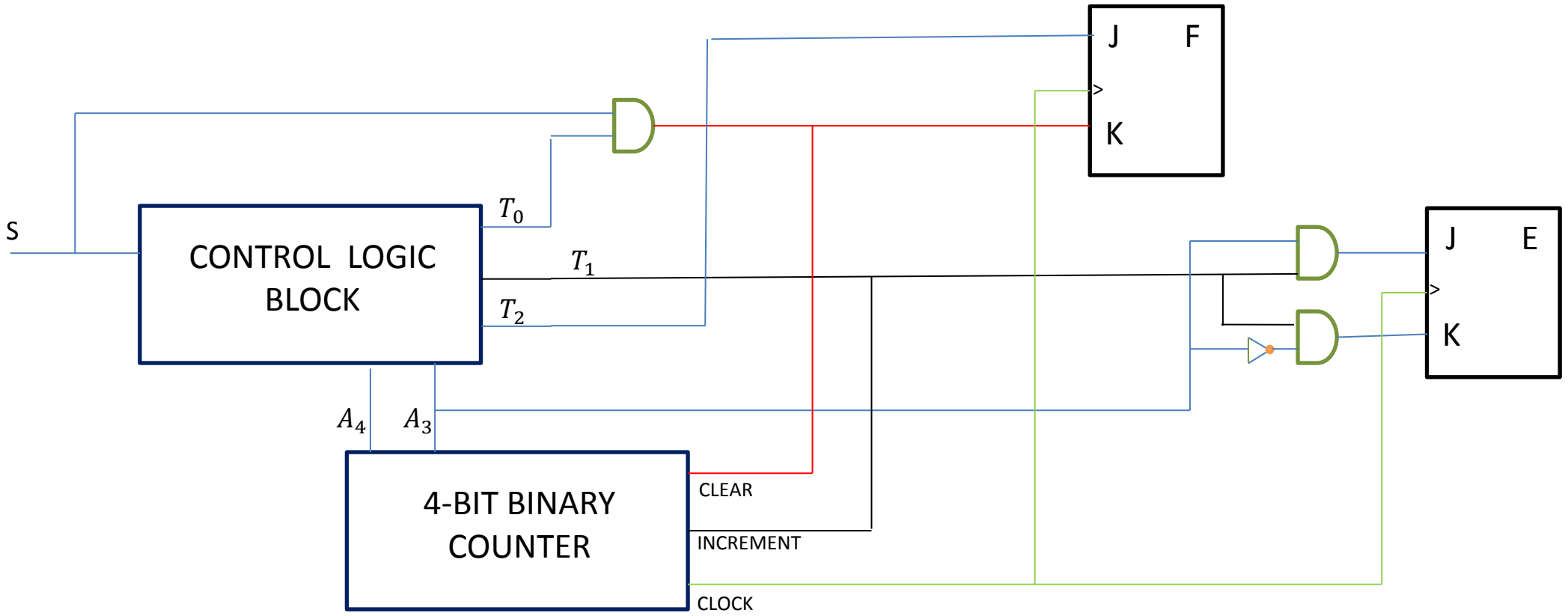
We didn't mention about A_4 , as no data operations are taking place there .

ASM Design

- The input to the control logic box comprises of A_3, A_4 from the Binary counter, and control signal (S).
- The output from the control logic box denotes the present state (either T_0 or T_1 or T_2).
- The counter increments in state T_1 thus connect T_1 to the increment input (similar to enable) in the binary counter.
- Connect T_0.S to the clear input of the binary counter since we have to clear the binary counter in state T_0 when S = 1.

- We connect T_0.S to the K input of F - flip flop so that when the control signal (S) is 1 and we are in state T_0 , F has to be reset.
- Connect T_2 to the J input of F - flip flop because we have to set F in state T_2.
- Note that T_0 and T_2 are never simultaneously 1 so F is set in state T_2 and Reset in state T_0 if control signal (S) is 1.
- In state T1 : if A_3 is 1 we have to set E, hence connect $T_1.A_3$ to the J input of the E - flip flop and if A_3 is 0 we have to reset E thus connect $T_1.\bar{A}_3$ to the K input of the E - flip flop.

ASM


S
CONTROL LOGIC BLOCK
T_0
T_1
T_2
A_4
A_3
4-BIT BINARY COUNTER
CLEAR
INCREMENT
CLOCK
J
F
>
K
J
E
>
K