Lecture Notes (09.10.2013)

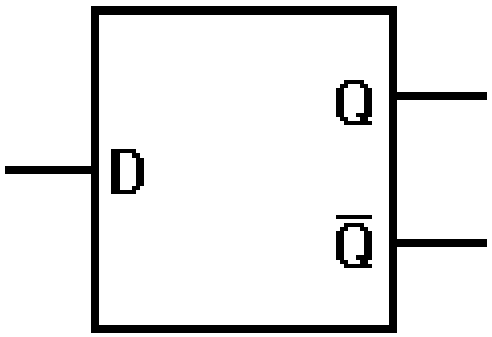
By: Shriraj Bharadwaj 120101067

Soham Kondalkar 120101070

Swapnil Agarwal 120101073

The D Flip-Flop

- The D flip-flop tracks the input, making transitions with match those of the input D. D stands for "data".
- This flip-flop stores the value that is on the data line.
- It can be thought of as a basic memory cell. A D flip-flop can be made from a set/reset flip-flop by tying the set to the reset through an inverter. The result may be clocked.

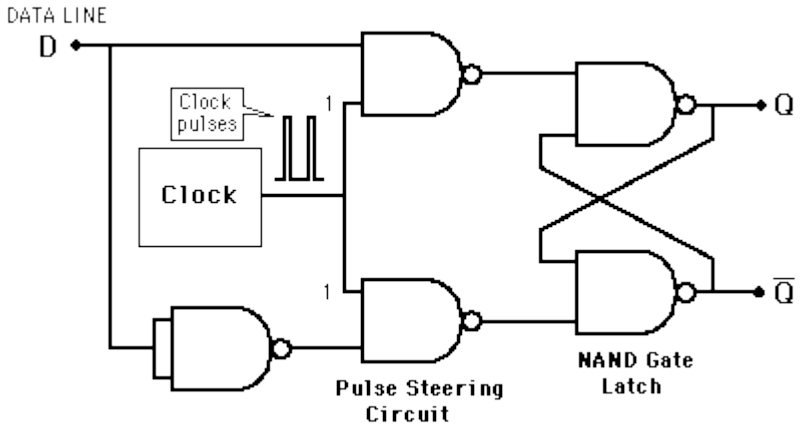


D-Type

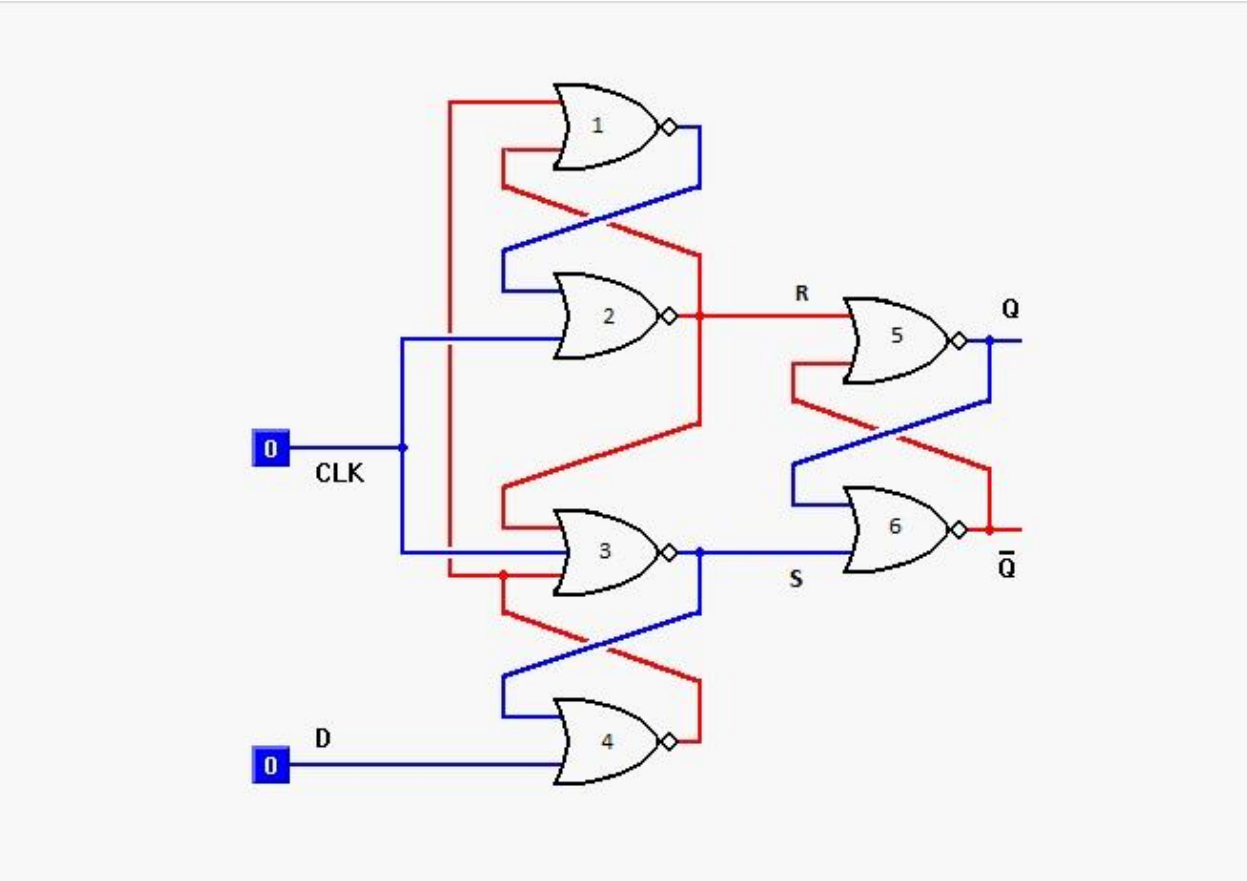
D flip-flop from NAND latch

- The output Q will track the input D so long as the flip-flop remains enabled.
- The D-type latch uses two additional gates in front of the basic NAND-type RS flip-flop, and the input usually called C (or clock) and D (or DATA). The function of the D-latch is as follows:-
    1. First, note that the clock signal is connected to both of the front NAND gates. Therefore, if the clock signal is zero, the output of the NAND gates are both 1, and implies that the RS flip-flop stores the previous value. Therefore, if the C input is 0, the flip-flop stores its value.
    2. On the other hand, if the clock signal is 1, the output of the first NAND gate is the inverse of the D input signal, and the output of the second NAND gate is not(not(D)) = D. This leads to the input

values R=0/S=1 or R=1/S=0 on the RS-flip-flop, which in turns enters the corresponding state. Therefore, if the C input is 1, the flip-flop output value follows to the value on its D input (the latch is 'transparent').



The D flip-flop using 6 nor gates

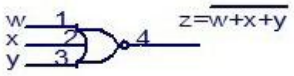


- Note that No. 4 NOR gate is 3 input NOR gate and it's truth table is as follows:-

Output for 3 input NOR gate is 1 if all the Inputs are zero otherwise 0.

3 Input NOR Gate

NOR Gate



TRUTH TABLE

INPUTS			OUTPUT
W	X	Y	Z
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

- When the clock is 1, circuit works as follows:-
    1. One of the inputs of the 2nd NOR gate is 1 (clock input), so output is 0.
    2. One of the inputs of the 3rd NOR gate is 1 (clock input), so output is 0.
    3. The inputs of the 4th NOR gate are 0 (output of the 3rd NOR gate) and D, so output of the 4th NOR gate is D^c.
    4. The inputs of the 1st NOR gate are D^c (output of the 4th NOR gate) and 0 (output of the 2nd NOR gate), so output of the 1st NOR gate is D.

5. So, the R and S for the corresponding 5^{th} and 6^{th} NOR gates will be 0 and 0 (output of the 2^{nd} and 3^{rd} NOR gates respectively), so it will be the "hold" condition.

- When the clock is 0, circuit works as follows:-
    1. The inputs of the 4^{th} NOR gate are 0 ($S_{previous}$) and D, so output of the 4^{th} NOR gate is D^c.
    2. The inputs of the 1^{st} NOR gate are D^c (output of the 4^{th} NOR gate) and 0 ($R_{previous}$), so output of the 1^{st} NOR gate is D.
    3. The inputs of the 2^{nd} NOR gate are D (output of the 1^{st} NOR gate) and 0 (clock input), so output of the 2^{nd} NOR gate is D^c.
    4. The inputs of the 3^{rd} NOR gate are D^c (output of the 2^{nd} NOR gate), 0 (clock input) and D^c (output of the 4^{th} NOR gate), so output of the 3^{rd} NOR gate is D.

5. So, the R and S for the corresponding 5th and 6th NOR gates will be D^c and D (output of the 2nd and 3rd NOR gates respectively), so it will either be the "set" or "reset" condition, depending on the value of D.

- **Analyzing the circuit when clock = 0**
    1. If D = 0, then S = D = 0 and R = D^c = 1, so Q will be updated to 0 and Q^c to 1.
    2. If D = 1, then S = D = 1 and R = D^c = 0, so Q will be updated to 1 and Q^c to 0.
    3. If another input D_{new} (≠ D) is given:
        i. The inputs of the 4th NOR gate are D ($S_{previous}$) and D^c (D_{new}), so output of the 4th NOR gate is 0.
        ii. The inputs of the 1st NOR gate are 0 (output of the 4th NOR gate) and D^c ($R_{previous}$), so output of the 1st NOR gate is D.
        iii. The inputs of the 2nd NOR gate are D (output of the 1st NOR

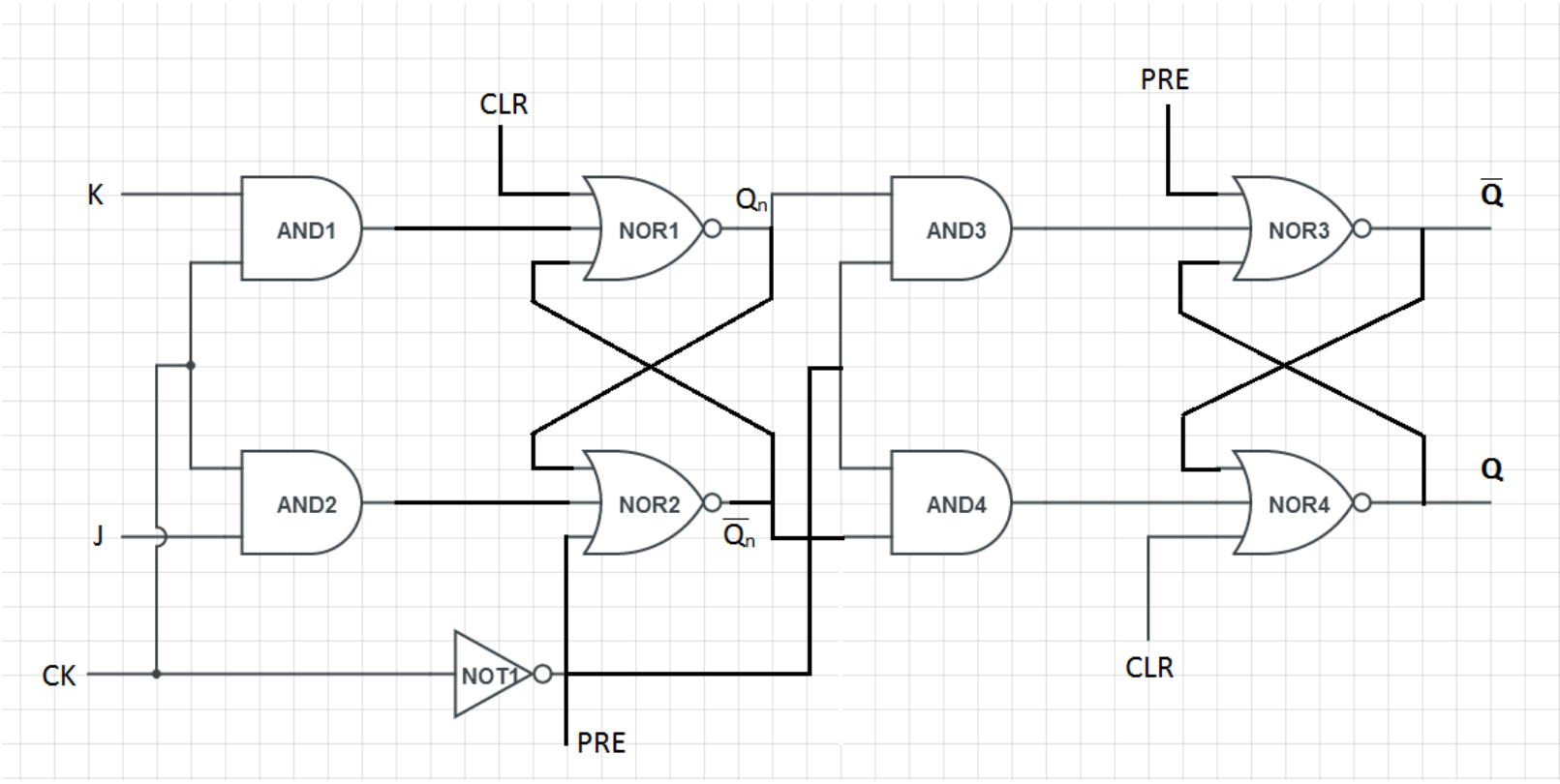
gate) and 0 (clock input), so output of the 2nd NOR gate is D^c.

iv. The inputs of the 3rd NOR gate are D^c (output of the 2nd NOR gate), 0 (clock input) and 0 (output of the 4th NOR gate), so output of the 3rd NOR gate is D.

v. So, $S = D = S_{previous}$
and $R = D^c = R_{previous}$.

vi. Therefore, the data coming as D_{new} is lost.

- **J K Flip Flop using R S flip flop**



1. PRE=0 and CLR=0
    a. When clock input is 0, the value of Q_n and Q_n^c does not change and hence Q and Q^c does not change.
    b. When clock input is 1 (Master latch is working)
        i. J=1 and K=1: $AND1_{output}$=1 and $AND2_{output}$=1. So Q_n and Q_n^c values will interchange.

ii. J=1 and K=0: $AND1_{output}$=0 and $AND2_{output}$=1. So Q_n and Q_n^c values will be respectively 1 and 0.

iii. J=0 and K=1: $AND1_{output}$=1 and $AND2_{output}$=0. So Q_n and Q_n^c values will be respectively 0 and 1.

iv. J=0 and K=0: $AND1_{output}$=0 and $AND2_{output}$=0. So Q_n and Q_n^c values will not change.

c. When clock input is 0 (Slave latch is working)

i. Q_n =1 and Q_n^c =1: $AND3_{output}$=1 and $AND4_{output}$=1. So Q and Q^c values will interchange.

ii. Q_n =1 and Q_n^c =0: $AND3_{output}$=1 and $AND4_{output}$=0. So the values of Q and Q^c will be respectively 1 and 0.

iii. Q_n =0 and Q_n^c =1: $AND3_{output}$=0 and $AND4_{output}$=1. So the values of Q and Q^c will be respectively 0 and 1.

iv. Q_n =0 and Q_n^c =0: $AND3_{output}$=0 and $AND4_{output}$=0. So the values of Q and Q^c will not change.

2. PRE=1 and CLR=0

i. Q_n^c will be 0 (Since PRE is 0) and hence Q_n will be 1. $AND4_{output}$ will be 0. Q^c will be 0(Since PRE is 1) and Q will be 1.

3. PRE=0 and CLR=1

i. Q_n will be 0 (Since CLR is 0) and hence Q_n^c will be 1. $AND3_{output}$ will be 0. Q will be 0(Since CLR is 1) and Q^c will be 1.

4. PRE and CLR can't be 1 simultaneously.