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Bcd synchronous counters

The BCD counter is just a special case of the MOD-N counter (N = 10). BCD counters are very commonly used because most human beings count in decimal. It is by default an up counter.

We prefer synchronous counter because there is not a regular pattern in the state table as it is in straight binary counter. So,we use a universal clock pulse which triggers all the flip flops simultaneously.

- BCD SYNCHRONOUS COUNTER USING T FLIP-FLOPS

State table for BCD counters

State Table for BCD Counter

Present State				Next State				Output	Flip-Flop Inputs			
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1	y	TQ_8	TQ_4	TQ_2	TQ_1
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	1

Using k-map we can find the input functions to T flip-flops as

Tq1=1, Tq2=Q8'Q1,Tq4=Q2Q1,Tq8=Q1Q8+Q4Q2Q1

k-map illustration is mentioned under:-

Q2Q1 / Q8Q4	00	01	11	10
00		1	1	
01		1	1	
11	X	X	X	X
10			X	X

k-map for Tq2 =Q1Q8'

Q2Q1 / Q8Q4	00	01	11	10
00			*1*	
01			*1*	
11	*X*	*X*	*X*	*X*
10			*X*	*X*

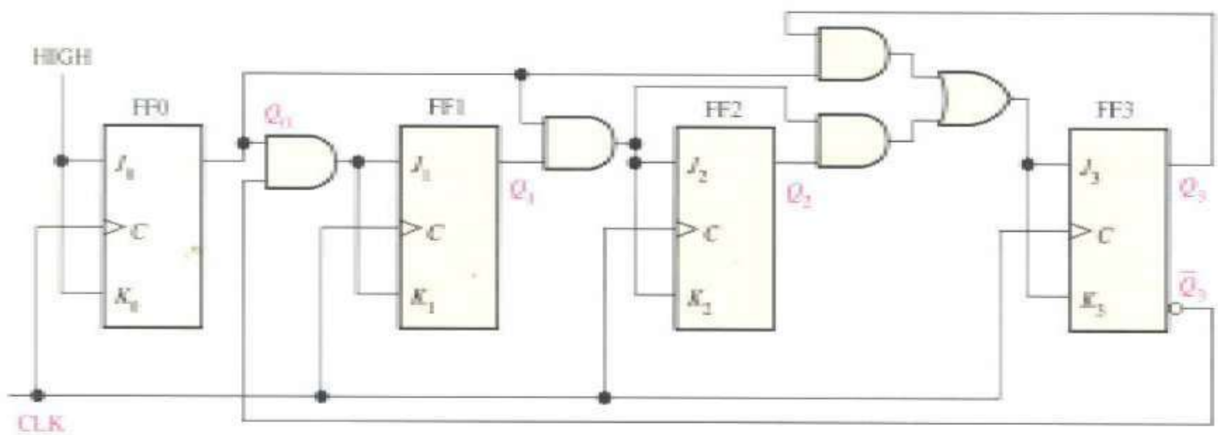
K-map for Tq4 = Q2Q1

Q2Q1	00	01	11	10

Q8Q4				
00				
01			*1*	
11	*X*	*X*	*X*	*X*
10		*1*	*X*	*X*

k-map for Tq8 is mentioned under : Q1Q8+Q1Q2Q4

Circuit diagram for synchronous BCD counters using jk flip flops:



Advantages of synchronous bcd counters:

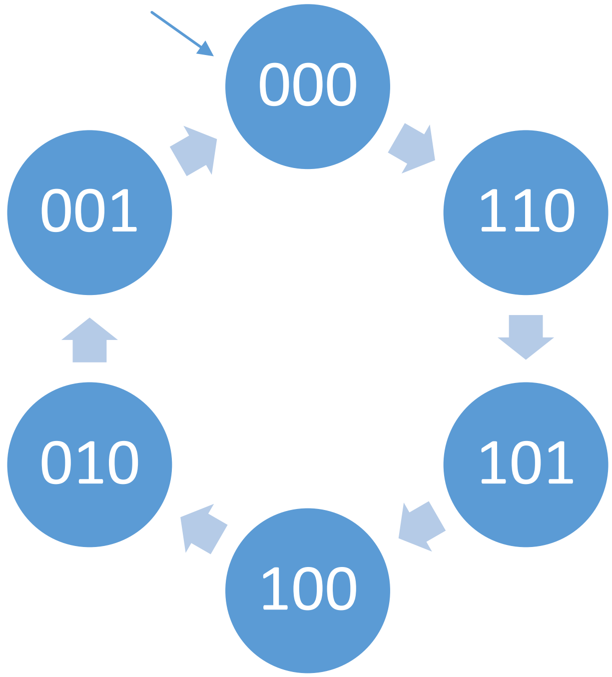
- Synchronous counters are easy to design.
- With all inputs wired together there is no inherent propagation delay.
- Overall faster operation may be achieved as compared to asynchronous counters

COUNTERS WITH UNUSED STATES

Counters with *n* flip-flops have 2^n states. For all the examples we have shown so far, we had 2^n states and used *n* flip-flops. But sometimes we may have unused, leftover states. This happens because in certain occasions, the sequential circuit uses fewer than its maximum number of states. The unused states do not play any role in specifying the sequential circuit and hence, are not listed in the stable table.

For example:

Here is a stable table that repeatedly counts 000, 001, 011, 100, 101, 110 .



PRESENT STATE			NEXT STATE		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	1	0	0
1	0	0	1	0	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	0	X	X	X
0	1	1	X	X	X

The unused states can be treated as DON'T CARE.

Using a J/K flip-flop:

PS $Q_2\ Q_1\ Q_0$	NS $Q_2\ Q_1\ Q_0$	$J_C\ K_C$	$J_B\ K_B$	$J_A\ K_A$
000	001	0X	0X	1X
001	010	0X	1X	X1
010	100	1X	X1	0X
100	101	X0	0X	1X
101	110	X0	1X	X1
110	000	X1	X1	0X

Now by K-map method:

$J_C = Q_B$

$K_C = Q_B$

$J_B = Q_A$

$K_B = 1$

J_B = complement of Q_B

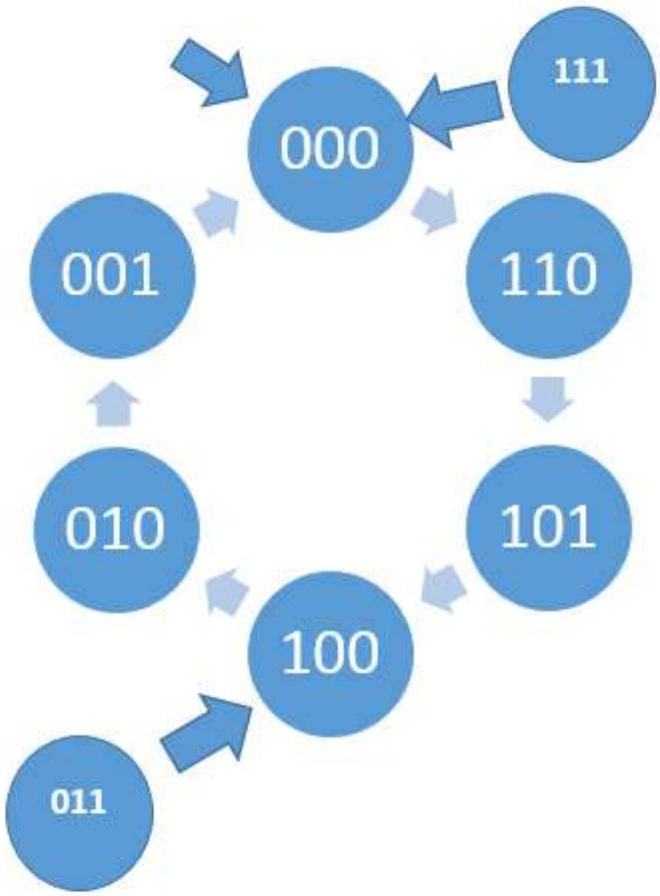
$K_B = 1$

It is possible that sometimes, outside noise can cause the counter to enter unused state. We must ensure that the counter eventually reaches valid state.

To avoid this and guarantee a safe circuit, we assign the next state to the unused states. This way, even if the circuit somehow enters an unused state, it will eventually end up in a used state.

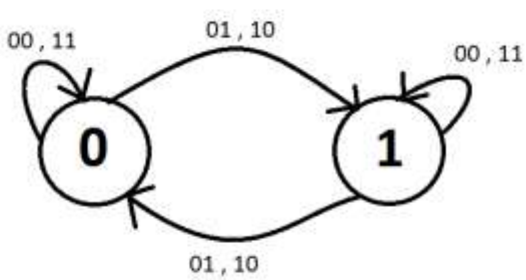
In the example given above, it is possible that the unused states 011 and 111 enter into the counter. So, we need to force one unused state to go to the used state.

PS	NS
011	100
111	000



Example 1

2 bit counter using D flip flop (2 states)



Present State	Input		Next State	D f/f
Q	x	Y	Q+	
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

D = N.S.

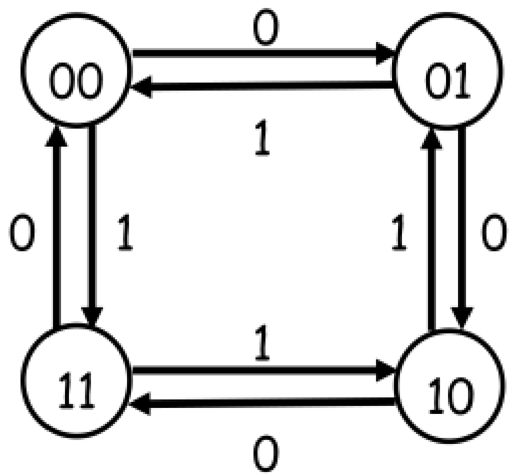
K-Map for D

Q \ xy	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$$D = Q \oplus x \oplus y$$

Example 2

1 bit counter using JK flip flop (4 states)

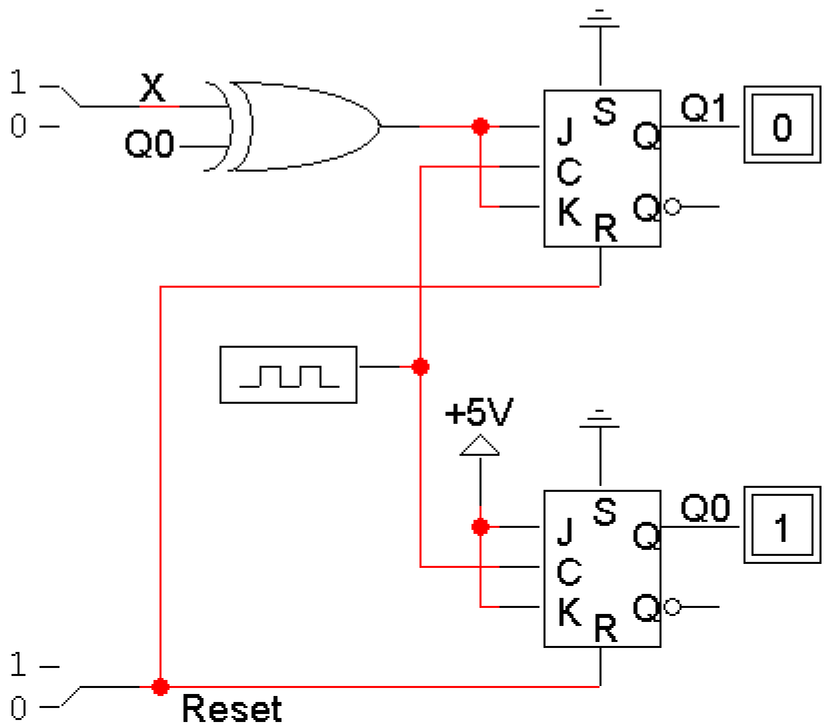


K-MAP

Present State Q_1	Present State Q_0	Inputs X	Next State Q_1	Next State Q_0	Flip flop inputs J_1	K_1	J_0	K_0
0	0	0	0	1	0	x	1	x
0	0	1	1	1	1	x	1	x
0	1	0	1	0	1	x	x	1
0	1	1	0	0	0	x	x	1
1	0	0	1	1	x	0	1	x
1	0	1	0	1	x	1	1	x
1	1	0	0	0	x	1	x	1
1	1	1	1	0	x	0	x	1

$$J_1 = K_1 = Q_0' X + Q_0 X' = Q_0 \oplus X$$

$$J_0 = K_0 = 1$$



1
0
X
Q0
S
J
Q
C
K
R
Q
Q1
0
+5V
S
J
Q
C
K
R
Q
Q0
1
1
0
Reset