DIGITAL DESIGN

Topic To Be Covered :

Optimized Master Slave D Flip Flop

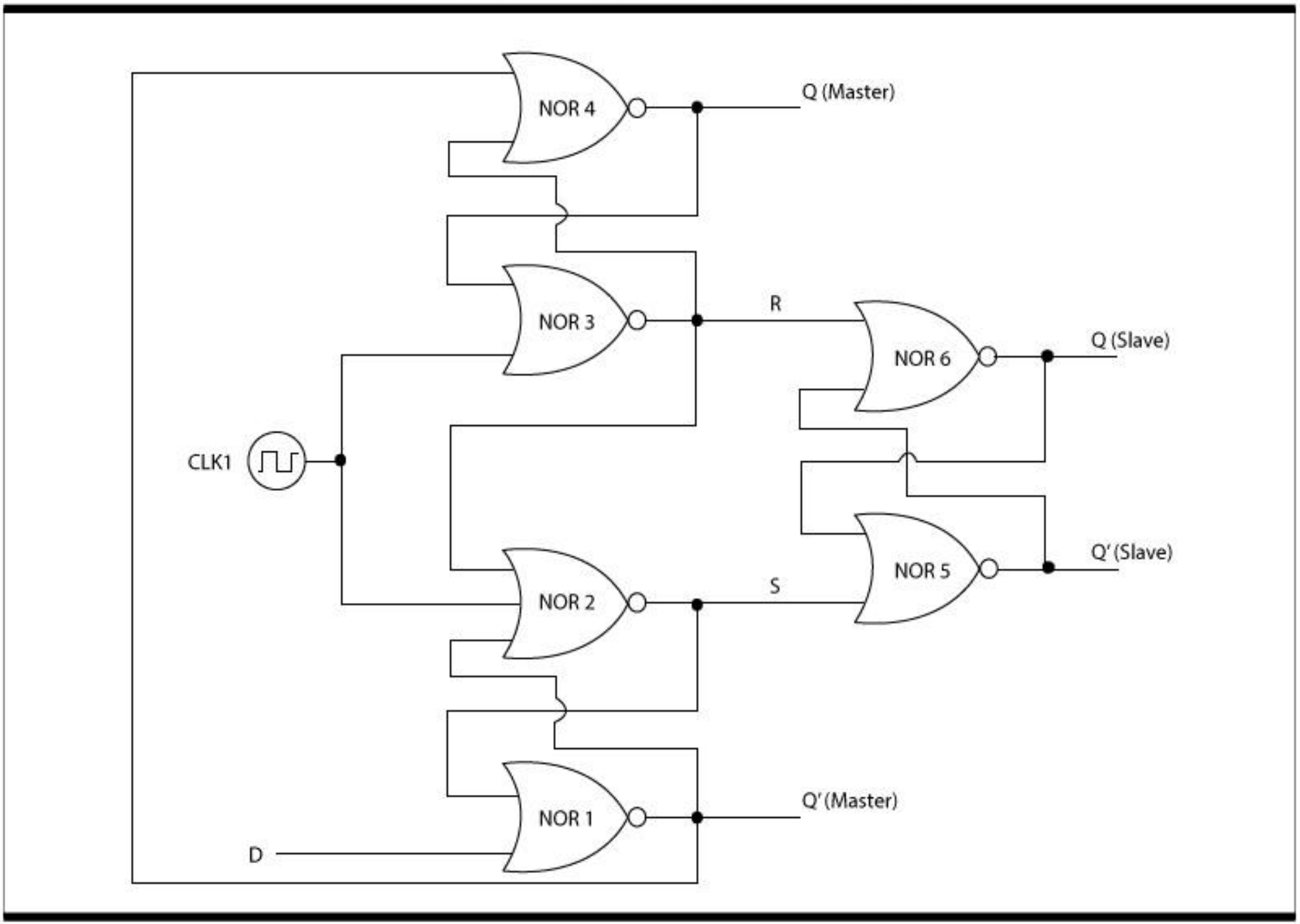
Dhruv Kohli 120123054
Aman Roonwal 120123005
Rajesh Uppala 120123045
Ajinkya Shejul 120123003

Optimized Master Slave D Flip Flop*

- Design And Facts
- Working
- Graphical Analysis
- Deriving a Boolean Function Representing the Master and Slave Outputs

* Analysis is done for negative-edge triggered Optimized Master Slave D Flip Flop

Optimized Master Slave D Flip Flop Circuit Diagram



Design And Facts

- Master Output Represented by :

  Output of NOR 1 and NOR 4
- Slave Output Represented by :

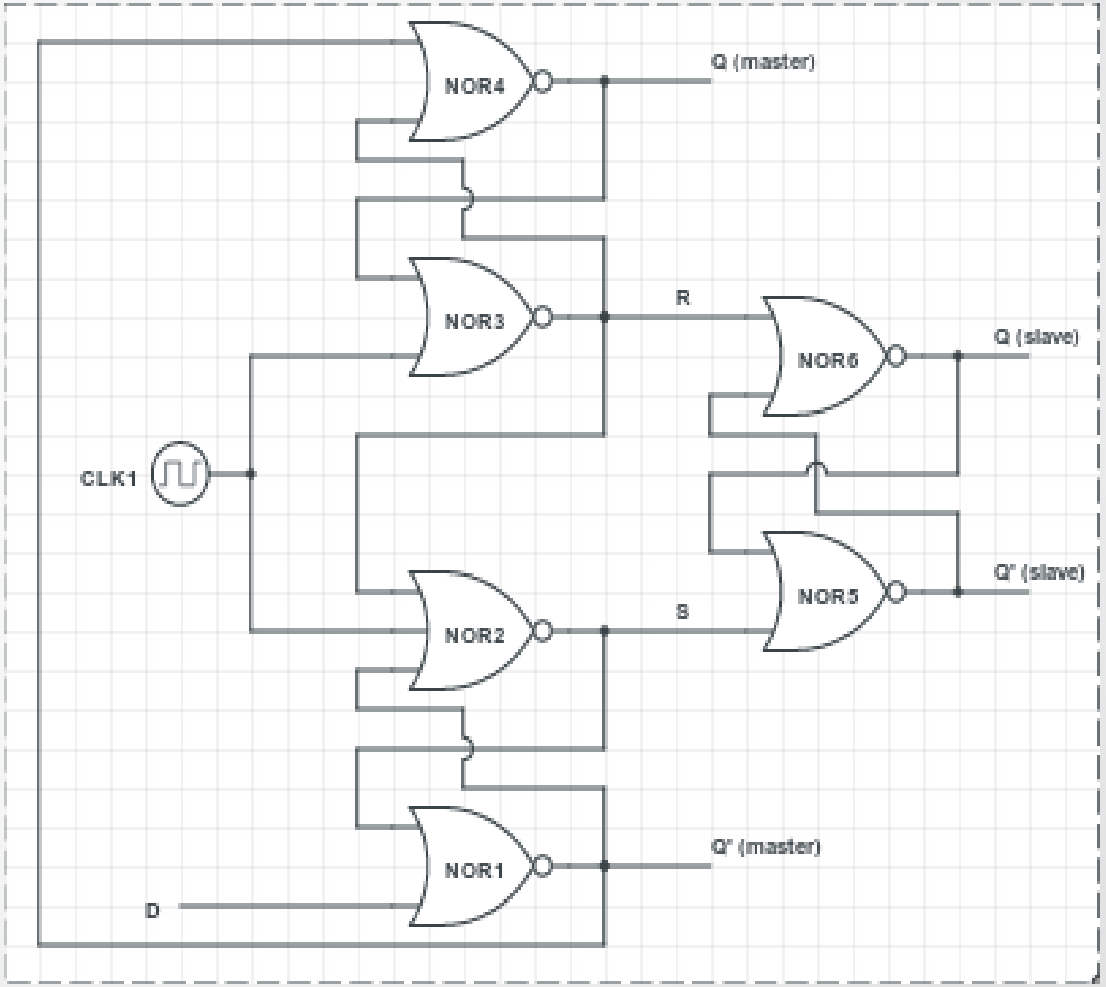
  Output of NOR 5 and NOR 6
- R and S are not directly connected to Q(master) and Q(master)'.
- Optimized due to less number of gates used in the design.

Working

+ When Clock is High i.e. CLK1 = 1
- NOR 2 and NOR 3 outputs 0.*
- NOR 1 (acts as an inverter)
  - inputs : 0 and D
  - output : D'
- NOR 4 (acts as an inverter)
  - inputs : 0 and D'
  - output : D

+ Implications :
- R = 0 and S = 0
- Q (slave) = HOLD
- Q (master) = D

+ Conclusions :
- D input is sampled by Master
- Slave is in HOLD state



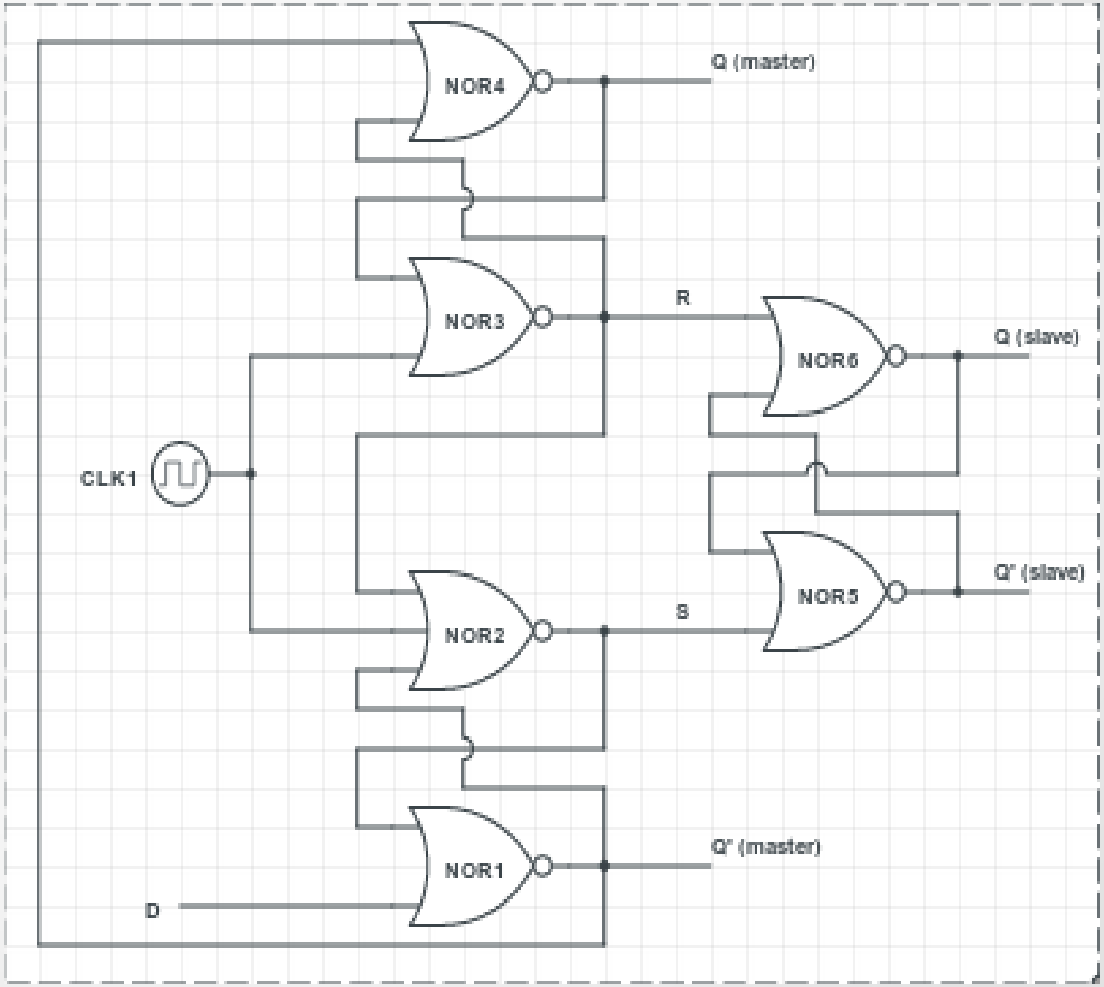
*** Fact : NOR gate with one of the inputs as 1, outputs 0.**

Working

+ **When Clock is Low i.e. CLK1 = 0**
  - NOR 2 (act as an inverter)
    - inputs : D', 0 and 0
    - output : D
  - NOR 3 (act as an inverter)
    - inputs : D and 0
    - output : D'
  - NOR 1 outputs D'*
  - NOR 4 outputs D*

+ **Implications :**
  - R = D' and S = D
  - Q (slave) = Updated accordingly
  - Q (master) = D (HOLD)

+ **Conclusions :**
  - Master is in HOLD state
  - Slave is updated



*** Fact : A+A = A => (A+A)' = A'**

Working

+ SUMMARY :

- As expected, when Clock is High, Master samples the input D and Slave remembers the previous state.
- And when Clock goes low, Master remembers the previous state and Slave is updated.

Q. What will happen when input D is changed while Clock is low i.e. CLK = 0 ?

Ans. NOR 1

- inputs : D and D(new) (As D(new)!=D implies D(new) = D')
- output : (D+D')' = 1' = 0

NOR 4 (act as an inverter)

- inputs : D' and 0
- output : D

NOR 3 (act as an inverter)

- inputs : D and 0
- output (R): D' (Same as the output given before when CLK = 0)

NOR 2

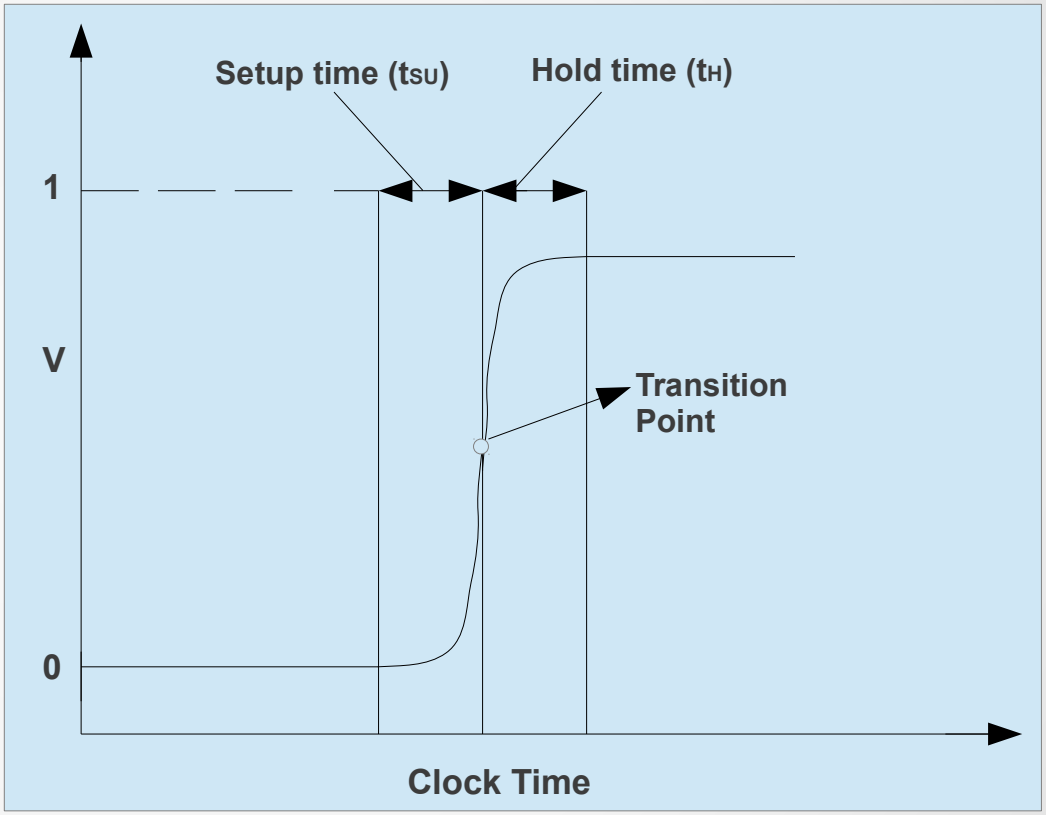
- inputs : 0, 0 and D' (bottom to top)
- output (S): D (Same as the output given before when CLK = 0)

Hence, the new input D(new) is not able to enter the Slave Latch.

Graphical Analysis

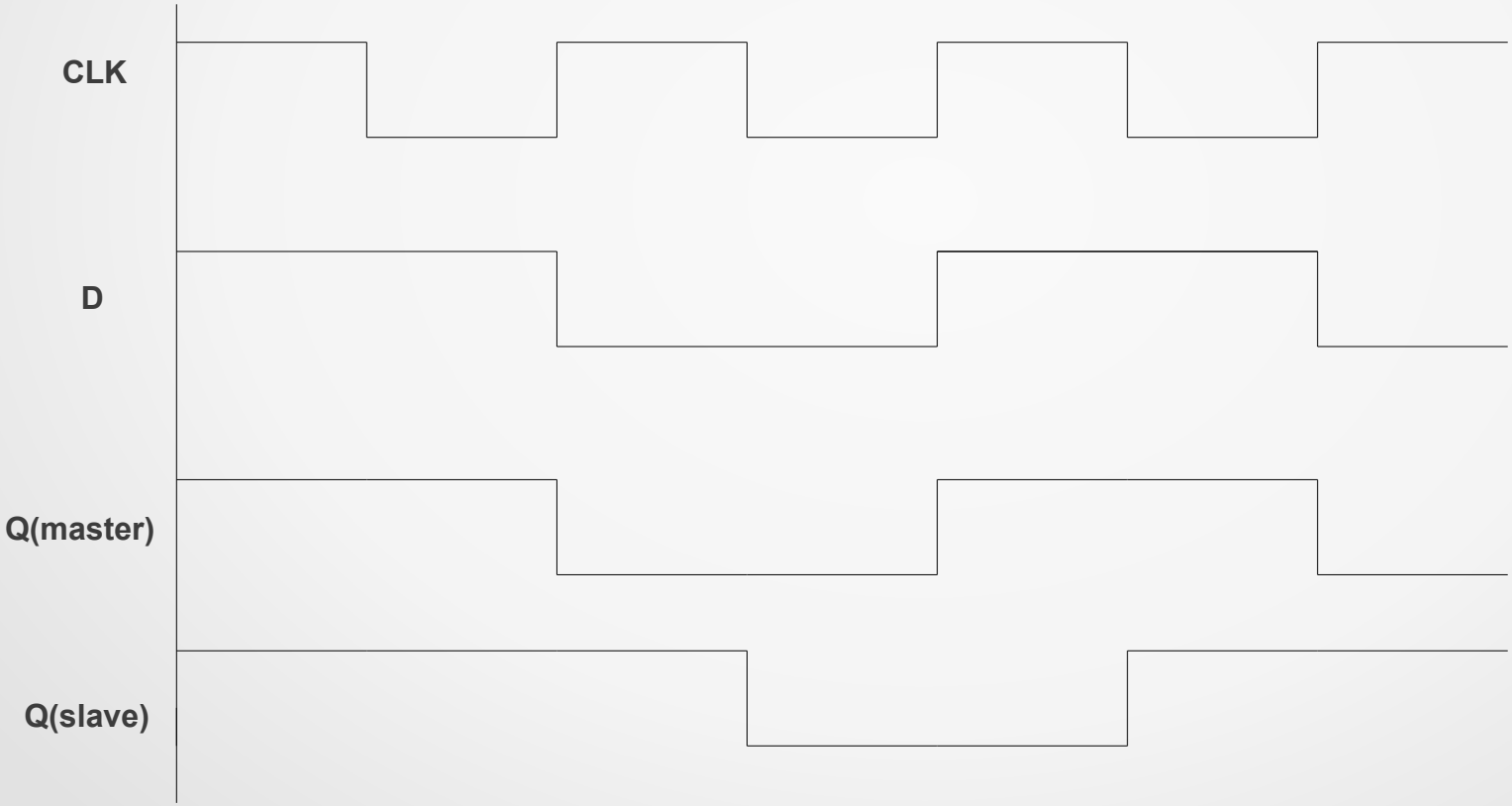
+ **Transition Point** :
  - The point below which Clock is considered to be 0 and above which the Clock is considered to Be 1.

+ **Sampling Interval** :
  - It is the sum of Setup time and Hold time.
  - R and S must be stable during sampling interval.
  - R and S are said to be Synchronous if they change with the clock else asynchronous.



Graphical Analysis

- Suppose initially both Q(master) and Q(slave) are high (i.e. = 1).



Boolean Function Derivation

- **Step 1 :**
  Draw K-Map with C(CLK), D, Q(master(old)) and Q(slave(old)) as Inputs and Q(master(new)) and Q(slave(new)) as Outputs.

Given State		Initial	Conditions	
Q_{mo} Q_{so}	CD=00	CD=01	CD=11	CD=10
0 0	0 0	0 1	1 0	0 0
0 1	0 0	0 1	1 1	0 1
1 1	1 0	1 1	1 1	0 1
1 0	1 0	1 1	1 0	0 0

Boolean Function Derivation

- **Step 2 :**
  Using the Table in Step 1 , Following are the derived Boolean Functions :

  Q(master(new)) = CQ(master(old)) + CD
  Q(slave(new)) = CQ(slave(old)) + C'D

  + SHORT NOTE

  - When CLK = 0
  Q(slave(new)) = HOLD
  Q(master(new)) = D

  - When CLK = 1
  Q(slave(new)) = S = D [As S=D and R=D']
  Q(master(new)) = HOLD