# International IslamicUniversity Islamabad Faculty of Engineering and Technology Department of Electricaland Computer Engineering

# VLSI DESIGN LAB


**EXPERIMENT Lab 9: Design and Performance Analysis of D Flip-Flop in LT-Spice**

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# Lab Performance report

- LabTask:

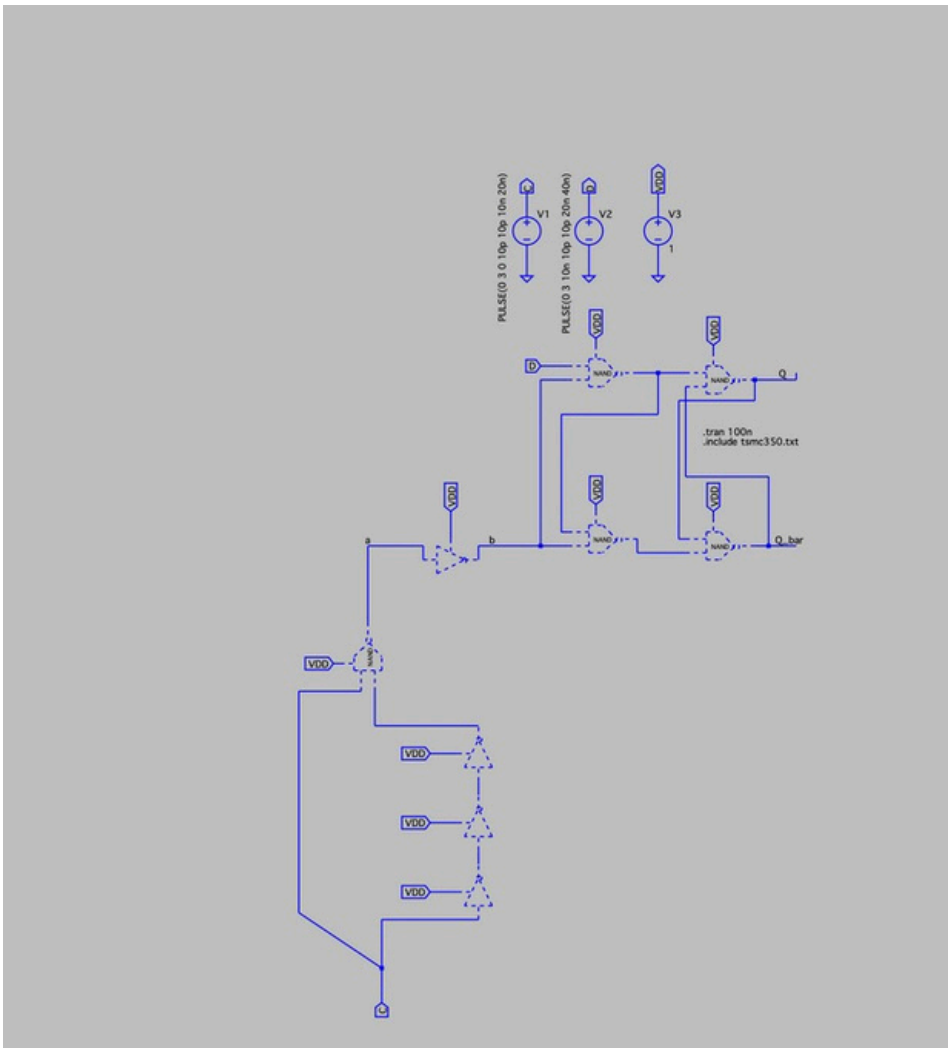
1. Verify the workingof **Edge Triggered D-latch** viatiming diagrams of your circuit. Apply inputcombinationsofyourchoice to evaluate performance completely.
2. Verify the working of **Master Slave D-Flipflop** via timing diagrams of your circuit. Apply input combinations of your choice to evaluate performance completely.

- Post Lab Task:

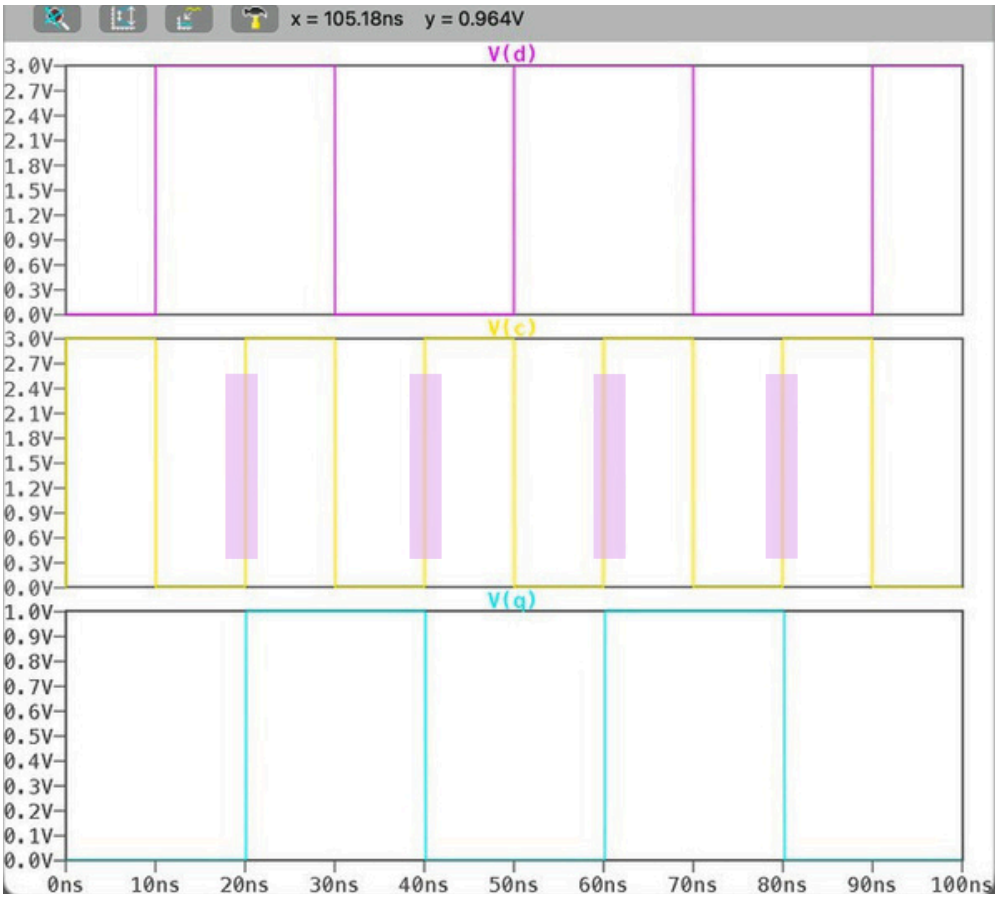
3. Make a **4-bit binary down counter** using **D-Flipflops**. Evaluate and correlate the output timing diagrams with the truth table.

## Task 1 :

**schematic**



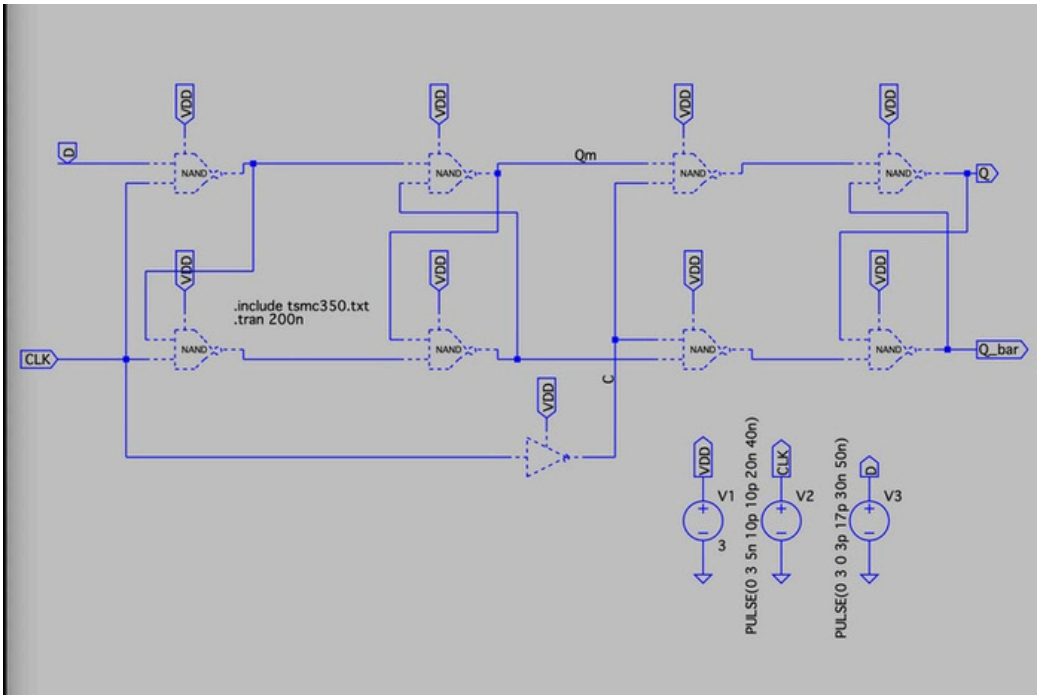

**WAVEFORM**



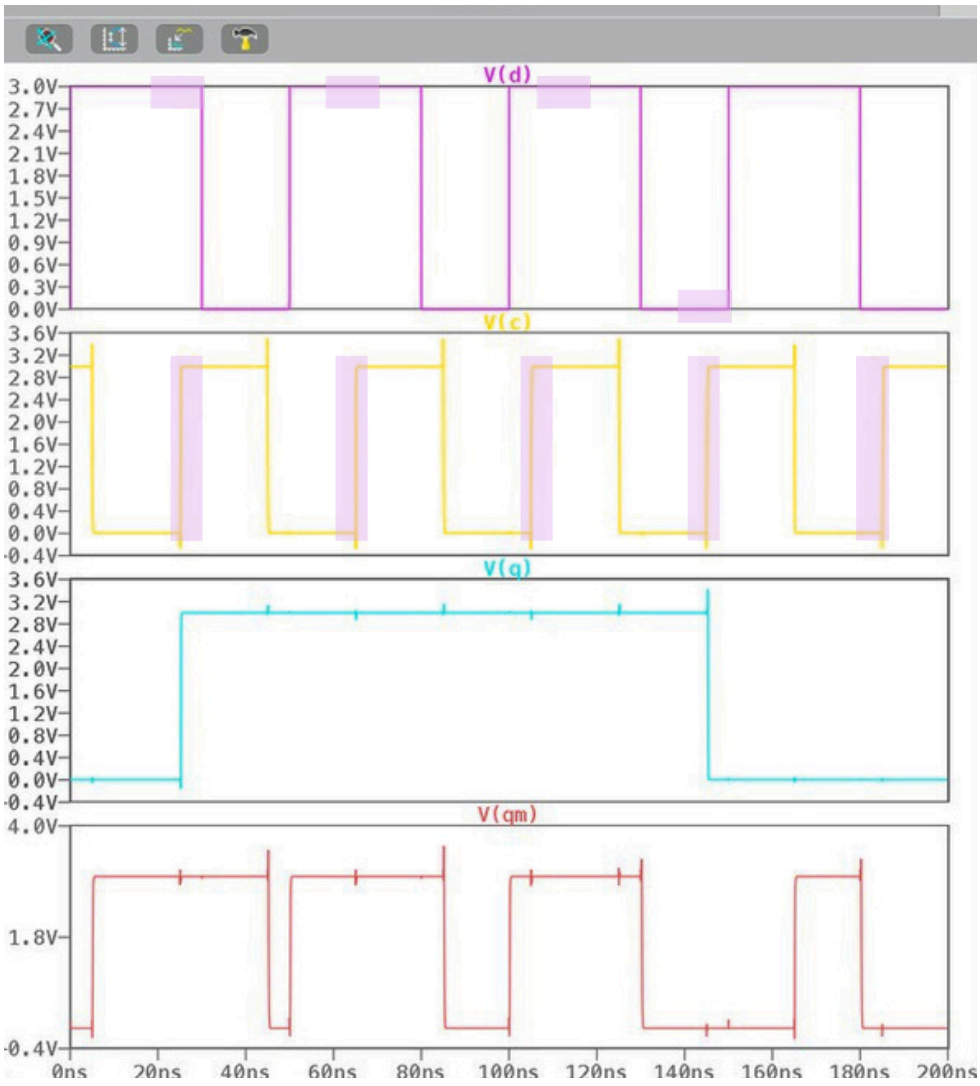

The edge-triggered D-latch operation was verified using timing diagrams. The output changes only at the clock edge.

## Task 2 :

**schematic**



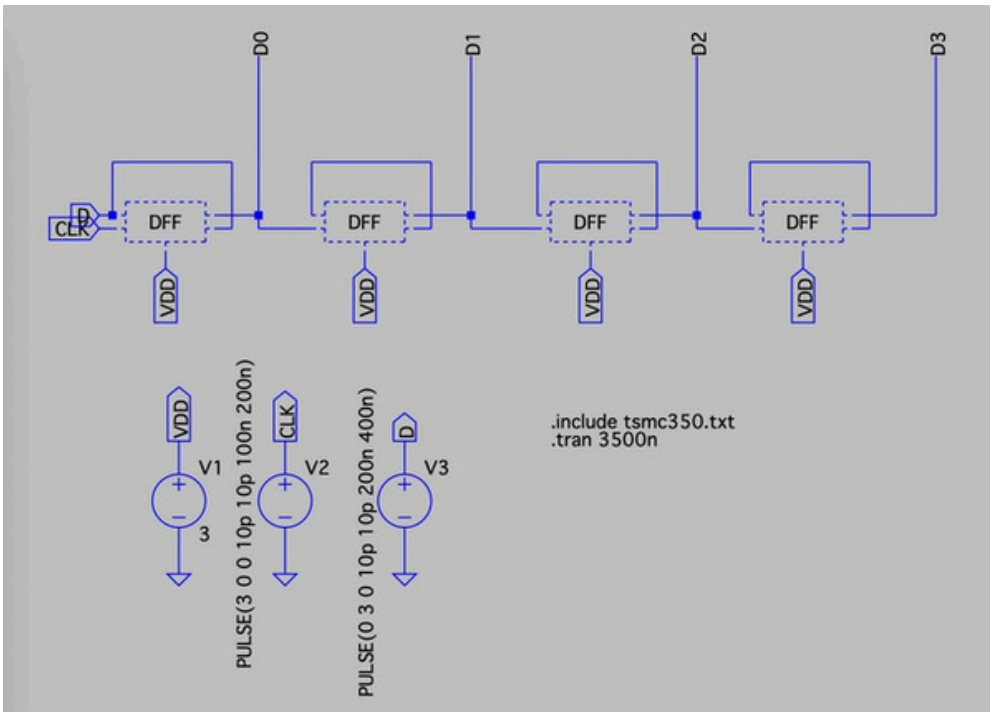

**WAVEFORM**




the working of the master-slave D flip-flop was verified through timing diagrams. The results show that the output updates only on the clock edge, eliminating race conditions and ensuring stable operation.

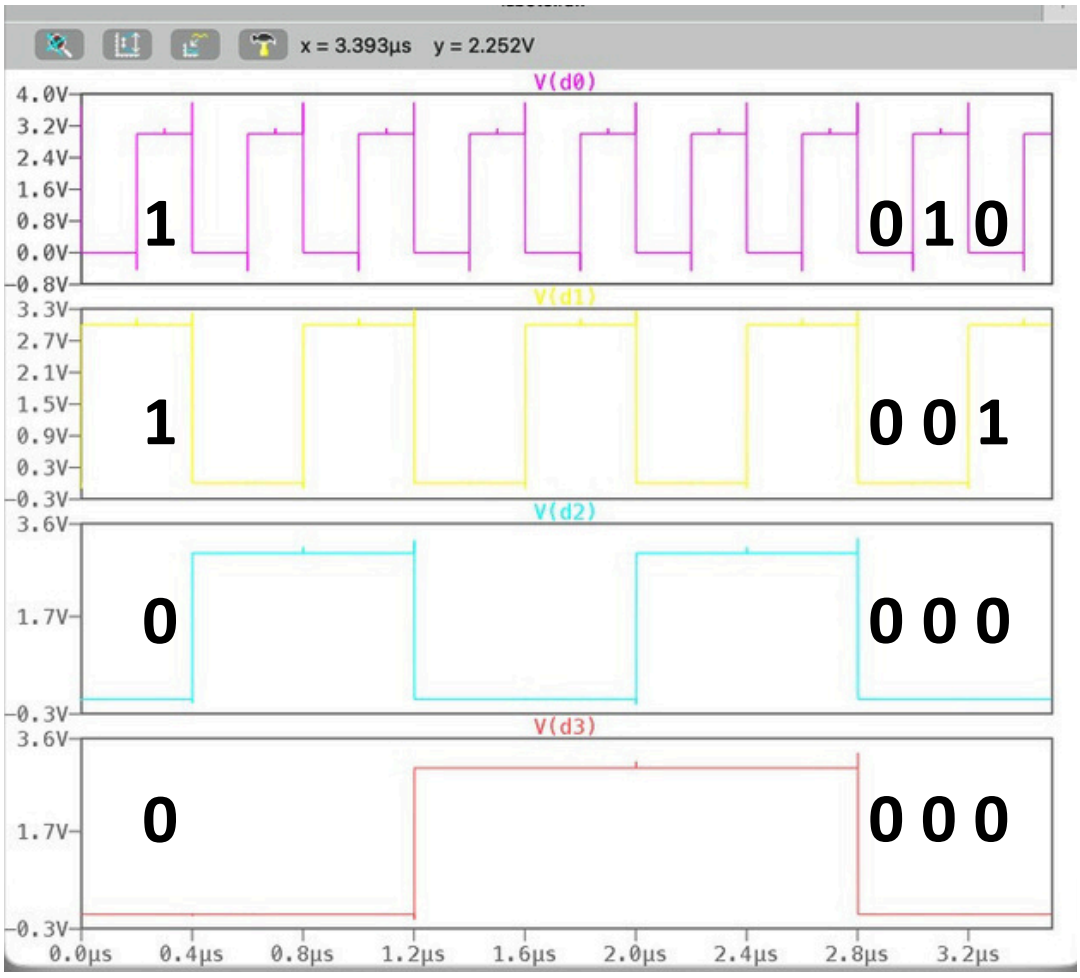
## Task 3 :

**schematic**




A 4-bit binary down counter was implemented using D flip-flops. The timing diagrams matched the truth table.

**WAVEFORM**




| Count | D | C | B | A |
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| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 |
| 11 | 1 | 0 | 1 | 1 |
| 12 | 1 | 1 | 0 | 0 |
| 13 | 1 | 1 | 0 | 1 |
| 14 | 1 | 1 | 1 | 0 |
| 15 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 |