International IslamicUniversity Islamabad Faculty of Engineering and Technology Department of Electricaland Computer Engineering

VLSI DESIGN LAB

EXPERIMENT Lab 14: Open Ended Lab

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Lab Performance Report#13

For a **2 inputXNORgate** (takeA, B,A', B' as separate inputs), presentthe Truth table and design schematics of static CMOS gates. Draw the logic graph and find common Euler Paths for pull-up and pull-down network. Sketch the corresponding stick diagram.

NOTES:

A. Draw static CMOS logic circuits that implement the given functions. For an N input gate, there should be 2N number of transistors in the circuits.

B. Draw Euler graphs for the circuits drawn in part A. Thus, derive Euler paths to determine the right input order and draw stick diagrams accordingly. **Note:** (Use multiple color markers for stick diagrams. For consistency, following color markers are recommended for all problems: **N+ active: green**, **P+ active: Brown**, **Poly: Red**, **Metal: Blue**, **VIA/ Contacts: Black**, **N-Well: Yellow**)

Task#1: **Pre-layout Simulation**:

- Design the gate schematic step by step in Electric. Perform transient analysis of
- using pulse inputs of your own choice in Electric and observe output in Ltspice

  Update the transistor widths till **tpHL = tpLH**
- Report the screenshots of schematic diagram, Spice netlist, I/O waveforms, log file
- and fill up the following table.

Sr#	Without Sizing		With Sizing	
	tpLH	**t^{pHL}**	**tpLH**	**t^{pHL}**
1.	-	-	1.6e-6 s	1.7e-6 s
2.	-	-	-	-

Task#2: **Post-layout Simulation**

- For the stick diagram drawn in, **design** the physical layout of the very gate in Electric.
- Perform the Design Rule Check (DRC) and **improve** your design till there are no errors or warnings.
- Perform the layout vs schematic analysis (NCC) in electric. Improve your design till the schematic of task#1 and the layout perfectly match.
- Perform transient analysis of the gate layout in Electric and observe output in Ltspice

- Observe and compare the results of pre-layout simulation with post layout simulation.
- Report the stick diagram, screenshots of layout diagram, Spice netlist, I/O waveforms, LTspice log file and your observations on how the post layout delays can be improved.
- Compare and improve your layout design to address any discrepancies in **tpHL, tpLH** values observed in pre-layout (with sizing) and post- layout design. Also comment on design improvement procedure implemented.

Sr#	Post-layout		Improved Design	
	tpLH	**tpHL**	**tpLH**	**t_{pHL}**
1.	—	—	1.6e-6 s	1.6e-6 s
2.	—	—	—	—

Comments:

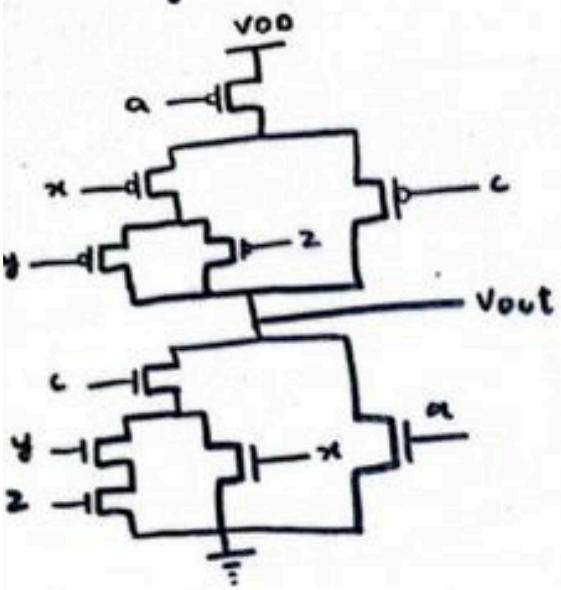
All steps of the lab were successfully completed, including schematic design, SPICE netlist extraction, transient simulation, and layout design. A clean DRC was achieved with no errors or warnings, and NCC showed a complete match between the schematic and layout.

Interestingly, the propagation delay values (tpHL and tpLH) were equal from the first attempt, so no additional transistor sizing was required. The lab objectives were fully met efficiently and accurately.

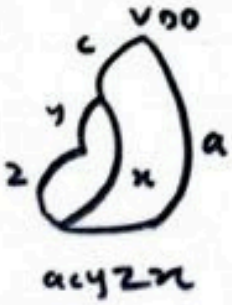
Caution: There is no unique solution to this assignment. All submissions should be different, like size of transistors, wiring of your schematic and selection of circuit parameters, inputs and outputs. **Zero marks will be awarded for exact copies, so avoid sharing your assignments with friends**.

CMOS logic circuit , Euler graph, Euler paths , stick diagrams:

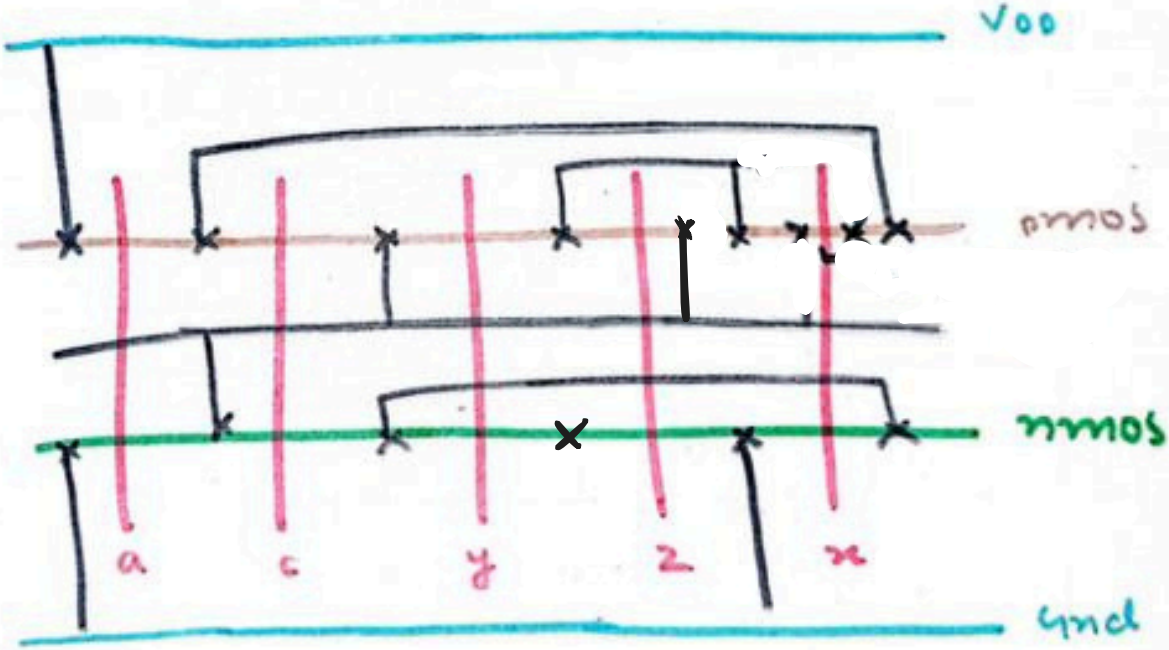
$$g = \overline{a + (c \cdot (x + (y \cdot z)))}$$



Euler path:

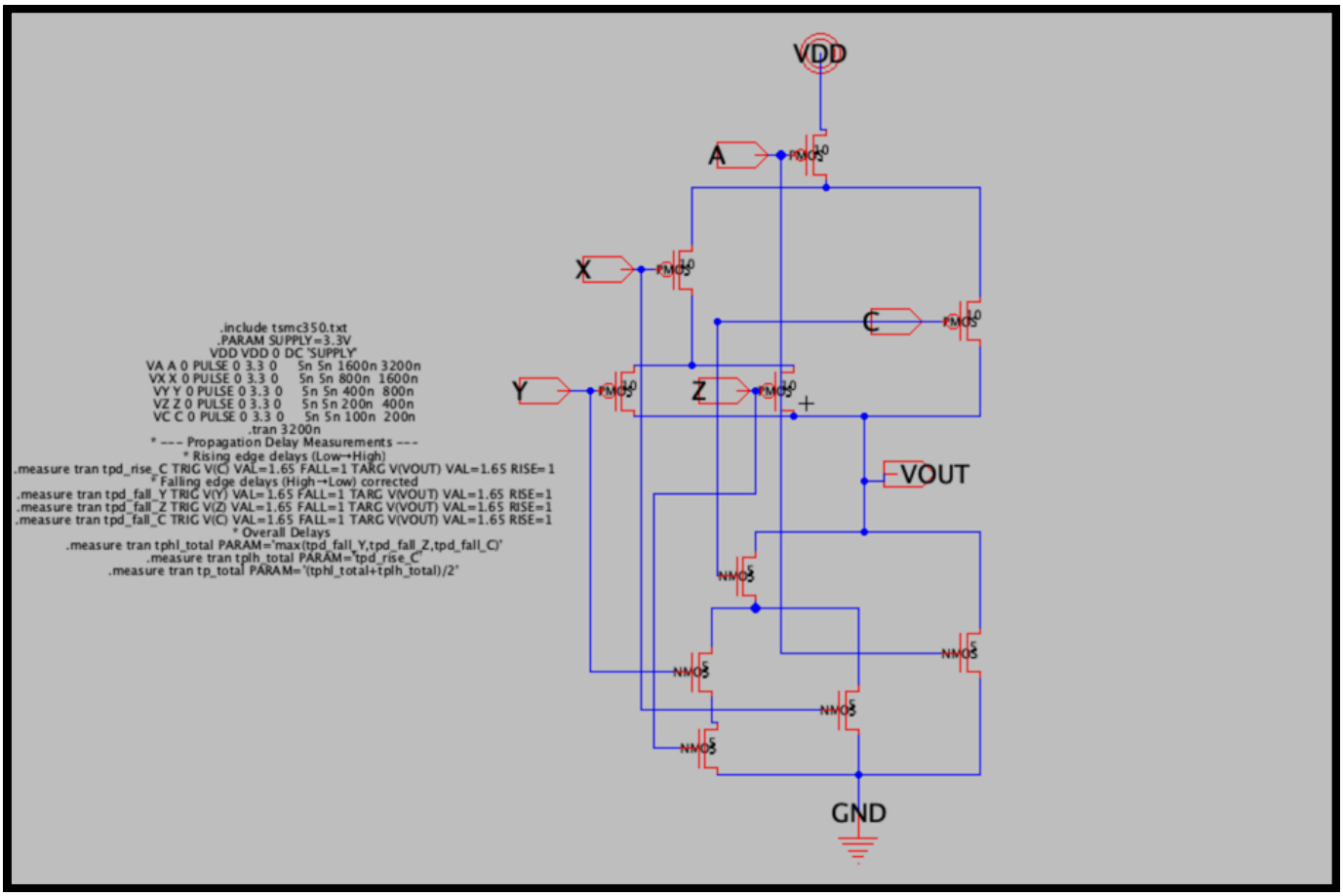


Stick diagram:



Task 1 AFTER SIZING :

schematic



SPICE Output Log

```
Direct Newton iteration for .op point succeeded.

tpd_rise_c=1.70518e-06 FROM 2.5e-09 TO 1.70768e-06
tpd_fall_y=1.30018e-06 FROM 4.075e-07 TO 1.70768e-06
tpd_fall_z=1.50018e-06 FROM 2.075e-07 TO 1.70768e-06
tpd_fall_c=1.60018e-06 FROM 1.075e-07 TO 1.70768e-06
```

tplh

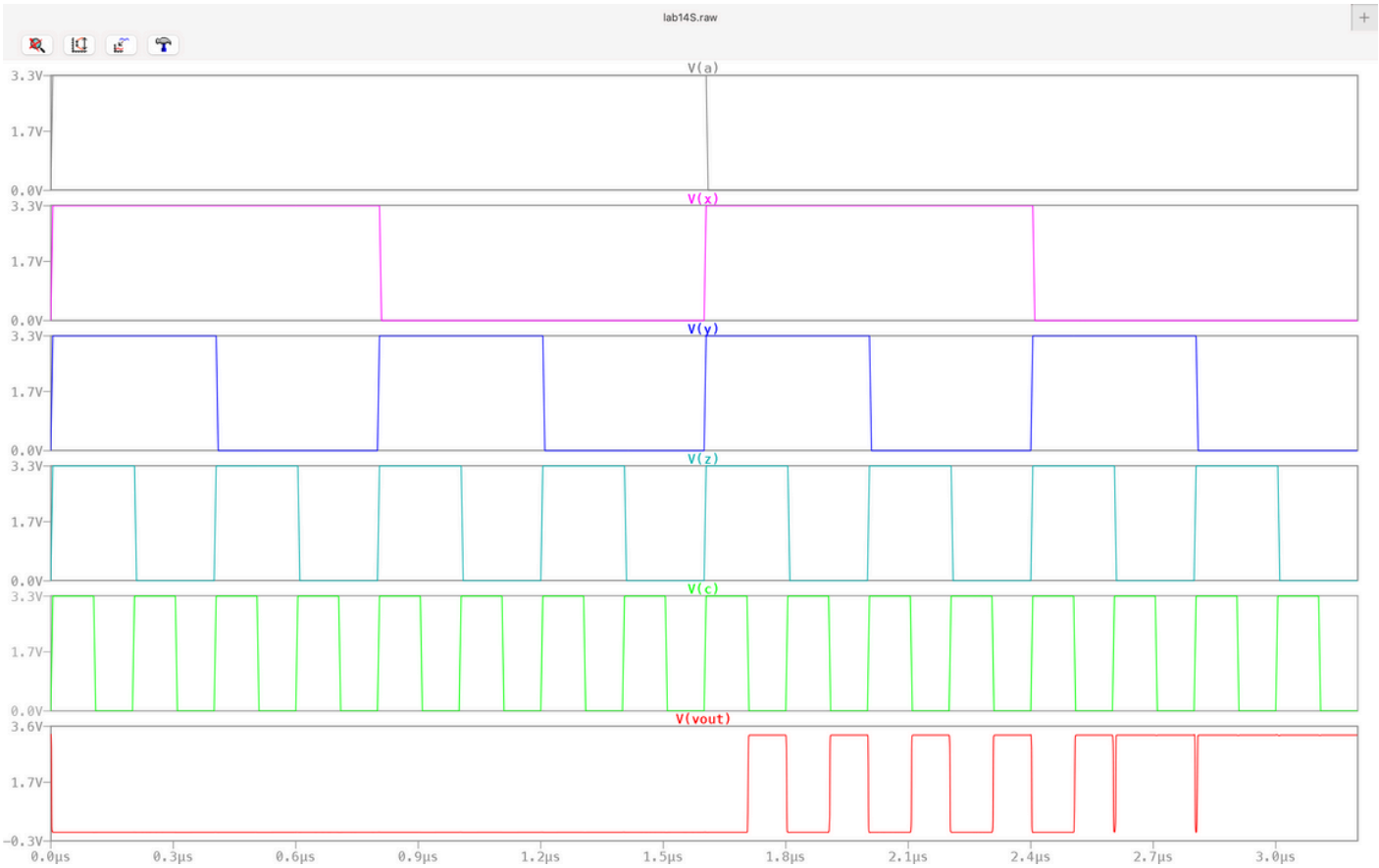
tphl

the propagation delay values (tpHL and tpLH) are equal , so no additional transistor sizing is required.

Netlist

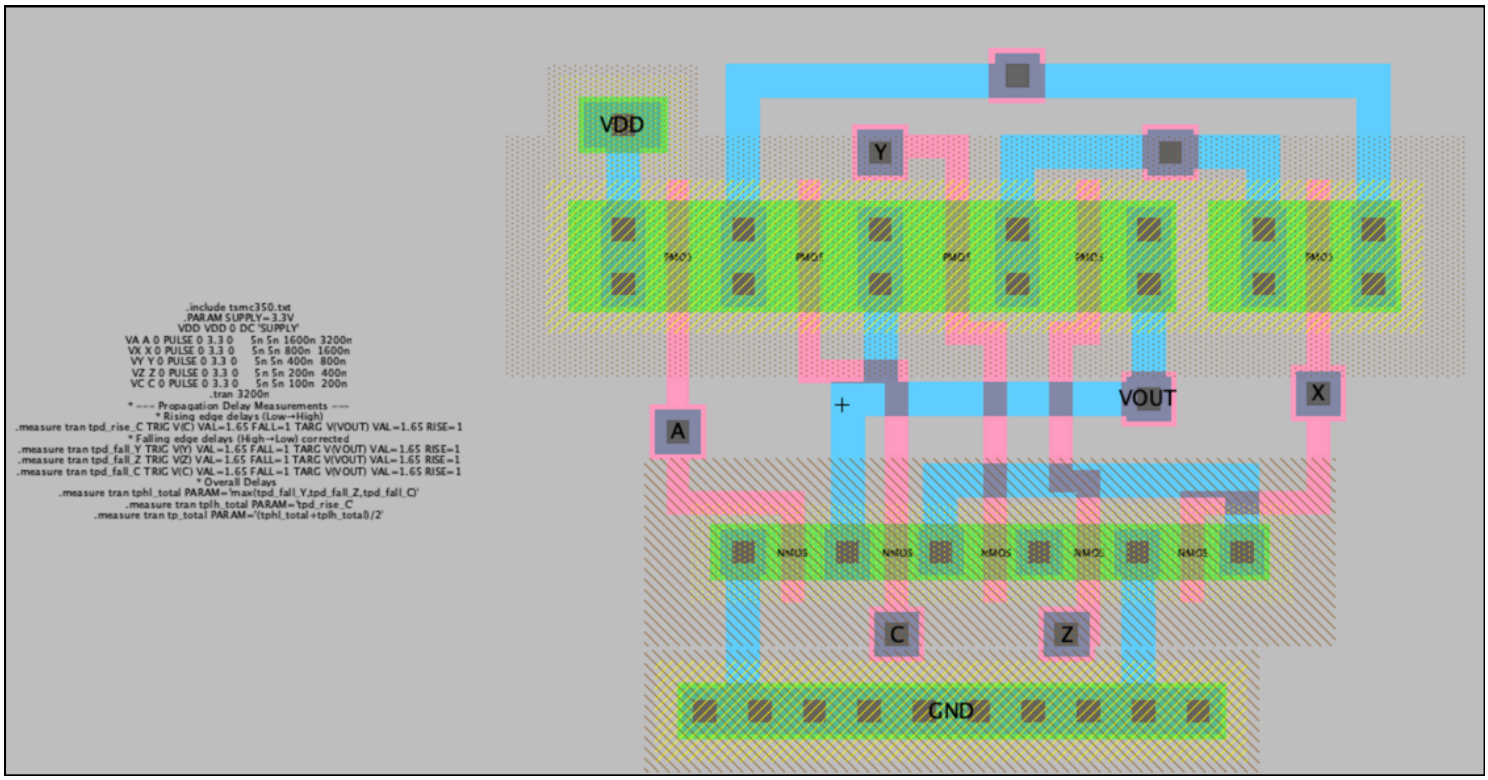
```
*** Written on 21 Dec 24, 2025 21:00:13 by Electric VLSI Design
System, version 9.07
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF
*** Lambda Conversion ***


.global gnd vdd

*** TOP LEVEL CELL: lab14:lab14{sch}
Mnmos@0 VOUT C net@21 gnd NMOS L=0.35u W=0.875u
Mnmos@1 net@21 Y net@19 gnd NMOS L=0.35u W=0.875u
Mnmos@2 net@19 Z gnd gnd NMOS L=0.35u W=0.875u
Mnmos@3 net@21 X gnd gnd NMOS L=0.35u W=0.875u
Mnmos@4 VOUT A gnd gnd NMOS L=0.35u W=0.875u
Mpmos@0 vdd A net@7 vdd PMOS L=0.35u W=1.75u
Mpmos@1 net@7 X net@4 vdd PMOS L=0.35u W=1.75u
Mpmos@2 net@4 Y VOUT vdd PMOS L=0.35u W=1.75u
Mpmos@3 net@4 Z VOUT vdd PMOS L=0.35u W=1.75u
Mpmos@4 net@7 C VOUT vdd PMOS L=0.35u W=1.75u


* Spice Code nodes in cell cell 'lab14{sch}'
.include tsmc350.txt
.PARAM SUPPLY=3.3V
VDD VDD 0 DC 'SUPPLY'
VA A 0 PULSE 0 3.3 0     5n 5n 1600n 3200n
VX X 0 PULSE 0 3.3 0     5n 5n 800n  1600n
VY Y 0 PULSE 0 3.3 0     5n 5n 400n  800n
VZ Z 0 PULSE 0 3.3 0     5n 5n 200n  400n
VC C 0 PULSE 0 3.3 0     5n 5n 100n  200n
.tran 3200n
* --- Propagation Delay Measurements ---
* Rising edge delays (Low→High)
.measure tran tpd_rise_C TRIG V(C) VAL=1.65 RISE=1 TARG V(VOUT)
VAL=1.65 RISE=1

* Falling edge delays (High→Low) corrected
.measure tran tpd_fall_Y TRIG V(Y) VAL=1.65 FALL=1 TARG V(VOUT)
VAL=1.65 RISE=1
.measure tran tpd_fall_Z TRIG V(Z) VAL=1.65 FALL=1 TARG V(VOUT)
VAL=1.65 RISE=1
.measure tran tpd_fall_C TRIG V(C) VAL=1.65 FALL=1 TARG V(VOUT)
VAL=1.65 RISE=1

* Overall Delays
.measure tran tphl_total PARAM='max(tpd_fall_Y,tpd_fall_Z,tpd_fall_C)'
.measure tran tplh_total PARAM='tpd_rise_C'
.measure tran tp_total PARAM='(tphl_total+tplh_total)/2'

.END
```

waveform

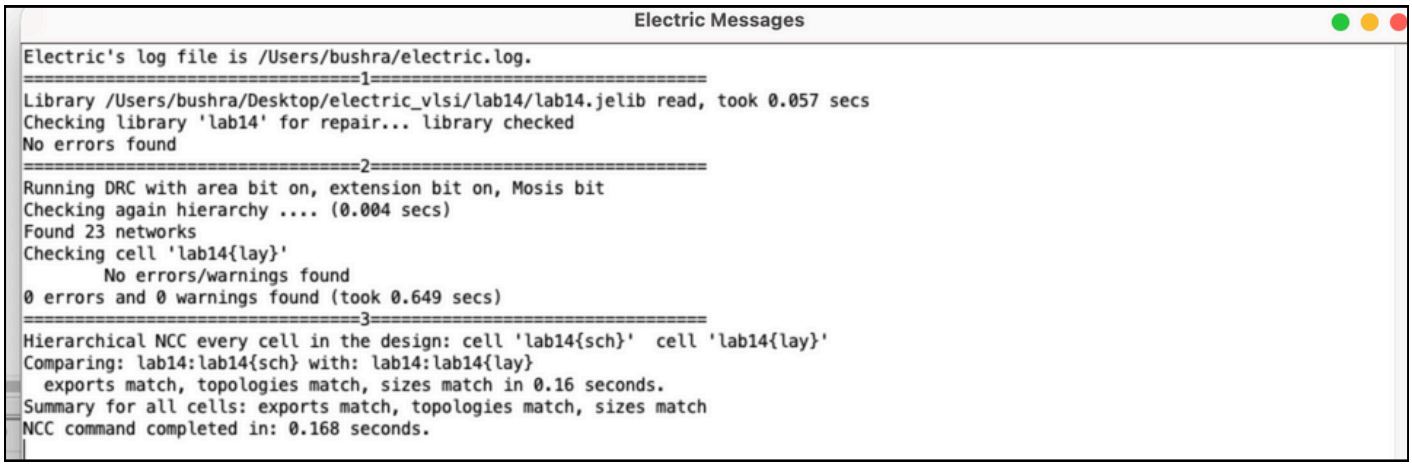


Task 2 AFTER SIZING :

LAYOUT



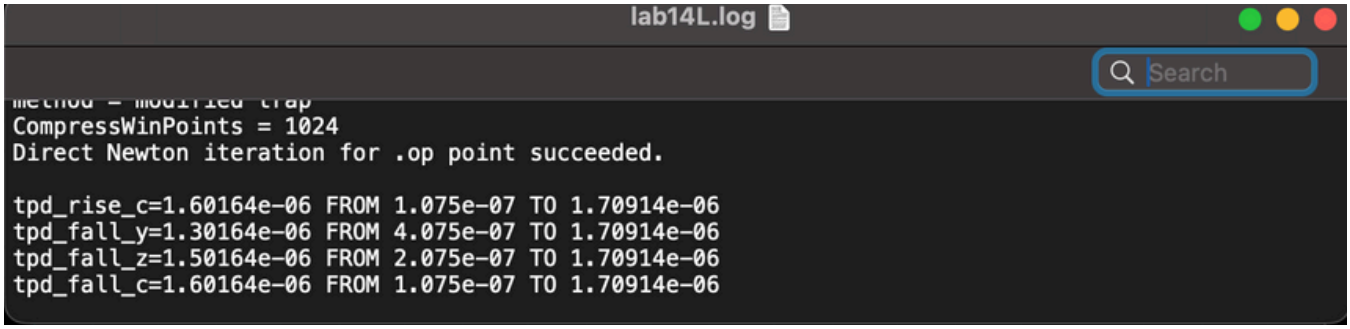
(DRC) , (NCC)



Electric Messages

```
Electric's log file is /Users/bushra/electric.log.
=================================1=================================
Library /Users/bushra/Desktop/electric_vlsi/lab14/lab14.jelib read, took 0.057 secs
Checking library 'lab14' for repair... library checked
No errors found
=================================2=================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.004 secs)
Found 23 networks
Checking cell 'lab14{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.649 secs)
=================================3=================================
Hierarchical NCC every cell in the design: cell 'lab14{sch}'  cell 'lab14{lay}'
Comparing: lab14:lab14{sch} with: lab14:lab14{lay}
  exports match, topologies match, sizes match in 0.16 seconds.
Summary for all cells: exports match, topologies match, sizes match
NCC command completed in: 0.168 seconds.
```

SPICE Output Log



lab14L.log

Search

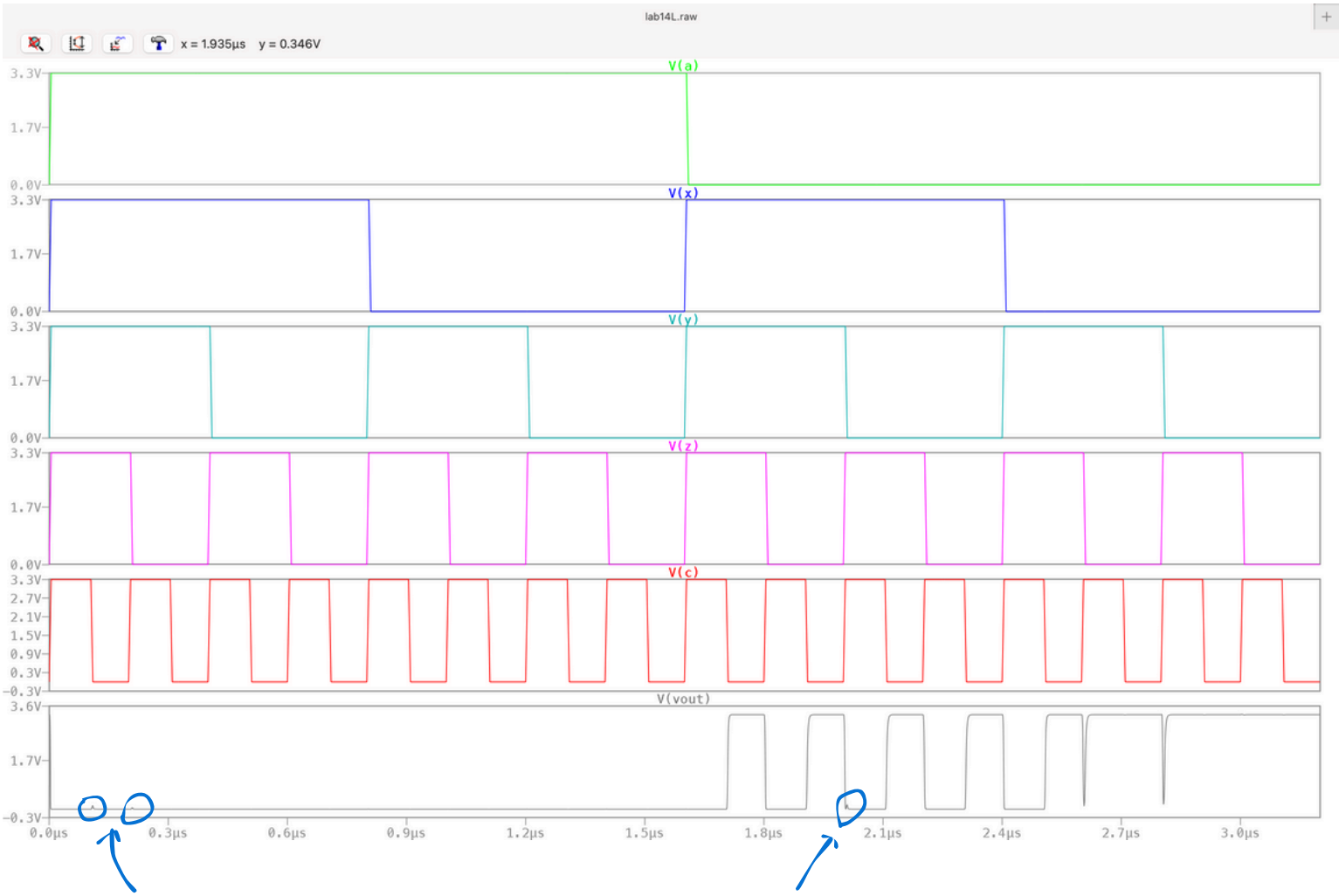
```
CompressWinPoints = 1024
Direct Newton iteration for .op point succeeded.

tpd_rise_c=1.60164e-06 FROM 1.075e-07 TO 1.70914e-06
tpd_fall_y=1.30164e-06 FROM 4.075e-07 TO 1.70914e-06
tpd_fall_z=1.50164e-06 FROM 2.075e-07 TO 1.70914e-06
tpd_fall_c=1.60164e-06 FROM 1.075e-07 TO 1.70914e-06
```

Netlist

```
Mnmos@0 VOUT C#4nmos@0_poly-left net@10 gnd NMOS L=0.35U W=0.875U AS=1.929P AD=5.553P
PS=4.725U PD=8.283U
Mnmos@1 net@10 Y#2nmos@1_poly-left net@12 gnd NMOS L= 0.35U W= 0.875U AS=1.929P AD=5.553P
PS=4.725U PD=8.283U
Mnmos@2 net@12 Z#4nmos@2_poly-left gnd gnd NMOS L= 0.35U W= 0.875U AS=1.929P AD=5.553P
PS=4.725U PD=8.283U
Mnmos@3 gnd X#0nmos@3_poly-left net@10 gnd NMOS L= 0.35U W= 0.875U AS=1.929P AD=5.553P
PS=4.725U PD=8.283U
Mnmos@4 gnd A#0nmos@4_poly-left VOUT gnd NMOS L= 0.35U W= 0.875U AS=1.929P AD=5.553P
PS=4.725U PD=8.283U

Mpmos@0 vdd A#2pmos@0_poly-right net@0 vdd PMOS L= 0.35U W=1.75U AS=32.769P AD=5.553P
PS=28.35U PD=8.283U
Mpmos@1 net@4 X#2pmos@1_poly-right net@0 vdd PMOS L= 0.35U W= 1.75U AS=32.769P AD=5.553P
PS=28.35U PD=8.283U
Mpmos@2 VOUT Y#0pmos@2_poly-right net@4 vdd PMOS L= 0.35U W= 1.75U AS=32.769P AD=5.553P
PS=28.35U PD=8.283U
Mpmos@3 net@4 Z#0pmos@3_poly-right VOUT vdd PMOS L= 0.35U W= 1.75U AS=32.769P AD=5.553P
PS=28.35U PD=8.283U
Mpmos@4 net@0 C#0pmos@4_poly-right VOUT vdd PMOS L= 0.35U W= 1.75U AS=32.769P AD=5.553P
PS=28.35U PD=8.283U

** Extracted Parasitic Capacitors ***
C0 net@0 0 4.452fF
C1 VOUT 0 3.383fF
C2 net@4 0 2.065fF
C3 net@10 0 2.015fF
C4 A 0 0.117fF
C5 X 0 0.132fF
C6 C#4nmos@0_poly-left 0 0.11fF
C7 A#1pin@0_polysilicon-1 0 0.113fF
C8 C#2pin@2_polysilicon-1 0 0.145fF
C9 Y#1pin@4_polysilicon-1 0 0.113fF
C10 X#1pin@5_polysilicon-1 0 0.141fF
C11 Z#1pin@13_polysilicon-1 0 0.106fF
C12 Z#2pin@14_polysilicon-1 0 0.106fF
** Extracted Parasitic Resistors ***
R0 A#0nmos@4_poly-left A#0nmos@4_poly-left##0 8.138
R1 A#0nmos@4_poly-left##0 A#0nmos@4_poly-left##1 8.138
R2 A#0nmos@4_poly-left##1 A#0nmos@4_poly-left##2 8.138
R3 A#0nmos@4_poly-left##2 A#1pin@0_polysilicon-1 8.138
R4 C#0pmos@4_poly-right C#0pmos@4_poly-right##0 5.425
R5 C#0pmos@4_poly-right##0 C#1pin@1_polysilicon-1 5.425
R6 C#1pin@1_polysilicon-1 C#1pin@1_polysilicon-1##0 7.75
R7 C#1pin@1_polysilicon-1##0 C#1pin@1_polysilicon-1##1 7.75
R8 C#1pin@1_polysilicon-1##1 C#2pin@2_polysilicon-1 7.75
R9 C#4nmos@0_poly-left C#4nmos@0_poly-left##0 9.3
R10 C#4nmos@0_poly-left##0 C#4nmos@0_poly-left##1 9.3
R11 C#4nmos@0_poly-left##1 C#4nmos@0_poly-left##2 9.3
R12 C#4nmos@0_poly-left##2 C#2pin@2_polysilicon-1 9.3
R13 Y#0pmos@2_poly-right Y#0pmos@2_poly-right##0 5.425
```

The layout netlist was successfully generated and includes all components, including resistors and capacitors.

waveform



The output waveform from the layout shows some small spikes compared to the schematic output. This difference occurs because the layout and schematic are simulated under different conditions, including parasitic effects in the layout. These spikes are normal and do not indicate errors; they reflect the actual behavior of the physical layout.