International IslamicUniversity Islamabad Faculty of Engineering and Technology Department of Electricaland Computer Engineering

VLSI DESIGN LAB

EXPERIMENT Lab 11: INVERTER LAYOUT

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Date of Experiment: 11-dec-2025

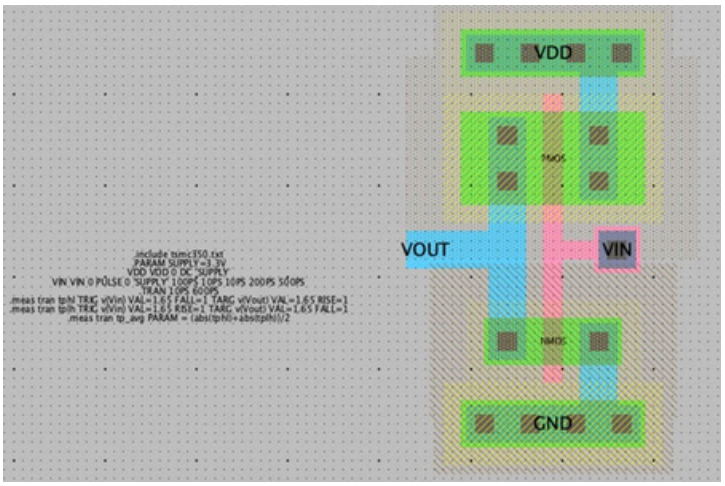
Lab Performance Report#11

- **Task#1**: **Post-layout Simulation**
  - Build up the physical layout of CMOS inverter step by step in Electric Simulation of
  - CMOS inverter layout in Electric and observing output of CMOS inverter in Ltspice
  - Perform the Design Rule Check (DRC) and improve your design till there are no errors or warnings.
  - Perform the layout vs schematic analysis (NCC) in electric. Improve your design till the schematic of task#1 and the layout perfectly match.
  - Use .meas command to evaluate propagation delay and power dissipation of the inverter layout. Observe and compare the results of pre-layout simulation with post layout simulation. Report the screenshots of layout diagram, Spice netlist, I/O waveforms, LTspice log
  - file and your observations.

- **Caution**: There is no unique solution to this assignment. All submissions should be different, like wiring of your schematic and selection of circuit parameters, inputs and outputs. **Zero marks will be awarded for exact copies, so avoid sharing your assignments with friends**.

Task 1 :

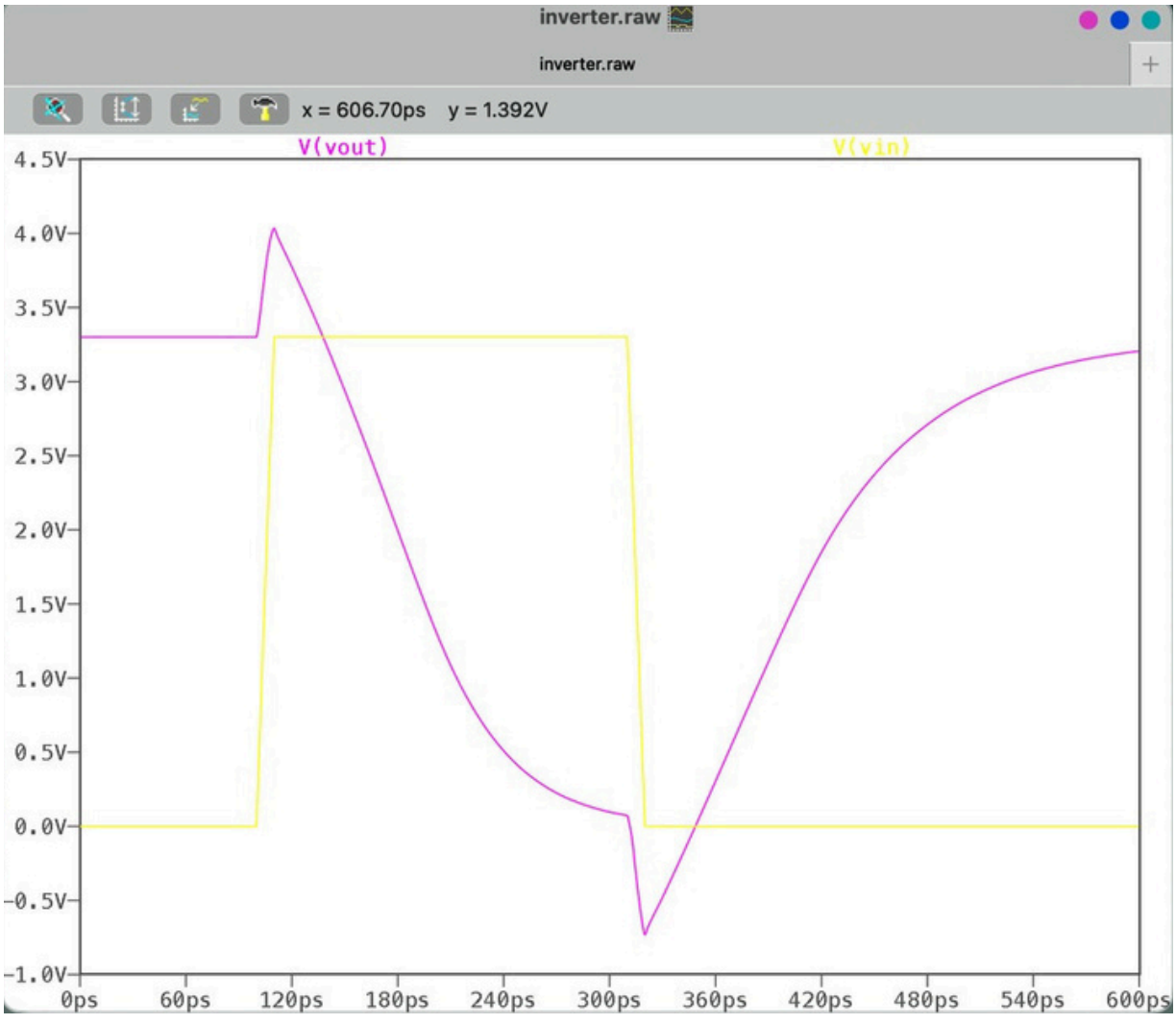
Layout



(DRC) , (NCC)

```
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.013 secs)
Found 7 networks
0 errors and 0 warnings found (took 0.021 secs)
==========================================107==========================================
Hierarchical NCC every cell in the design: cell 'inverter{sch}'  cell 'inverter{lay}'
Comparing: inverter:inverter{sch} with: inverter:inverter{lay}
  exports match, topologies match, sizes match in 0.027 seconds.
Summary for all cells: exports match, topologies match, sizes match
NCC command completed in: 0.037 seconds.
```

WAVEFORM



netlist

```
sq
***    Metal-5:areacap=0.0843FF/um^2, edgecap=0.0974FF/um,
res=0.078ohms/sq
***    Via5:   areacap=0.0FF/um^2,    edgecap=0.0FF/um,  res=0.8ohms/
sq
***    Metal-6:areacap=0.0843FF/um^2, edgecap=0.0973FF/um,
res=0.036ohms/sq
***    Hi-Res: areacap=0.0FF/um^2,    edgecap=0.0FF/um,  res=1.0ohms/
sq

*** TOP LEVEL CELL: inverter{lay}

Mnmos@0 gnd VIN#0nmos@0_poly-right VOUT gnd NMOS L=0.7U W=1.75U
AS=5.053P AD=14.394P PS=9.1U PD=23.45U
Mpmos@0 vdd VIN#2pmos@0_poly-left VOUT vdd PMOS L=0.7U W=3.5U AS=5.053P
AD=17.763P PS=9.1U PD=26.95U
** Extracted Parasitic Capacitors ***
C0 VOUT 0 3.823fF
C1 VIN 0 0.177fF
C2 VIN#0nmos@0_poly-right 0 0.118fF
C3 VIN#1pin@0_polysilicon-1 0 0.399fF
C4 VIN#2pmos@0_poly-left 0 0.105fF
** Extracted Parasitic Resistors ***
R0 VIN#0nmos@0_poly-right VIN#0nmos@0_poly-right##0 6.975
C5 VIN#0nmos@0_poly-right##0 0 0.118fF
R1 VIN#0nmos@0_poly-right##0 VIN#1pin@0_polysilicon-1 6.975
R2 VIN#1pin@0_polysilicon-1 VIN#1pin@0_polysilicon-1##0 6.2
C6 VIN#1pin@0_polysilicon-1##0 0 0.105fF
R3 VIN#1pin@0_polysilicon-1##0 VIN#2pmos@0_poly-left 6.2
R4 VIN#1pin@0_polysilicon-1 VIN#1pin@0_polysilicon-1##0 9.3
C7 VIN#1pin@0_polysilicon-1##0 0 0.177fF
R5 VIN#1pin@0_polysilicon-1##0 VIN#1pin@0_polysilicon-1##1 9.3
C8 VIN#1pin@0_polysilicon-1##1 0 0.177fF
R6 VIN#1pin@0_polysilicon-1##1 VIN 9.3

* Spice Code nodes in cell cell 'inverter{lay}'
.INCLUDE tsmc350.txt
.PARAM SUPPLY=3.3V
VDD VDD 0 DC 'SUPPLY'
VIN VIN 0 PULSE 0 'SUPPLY' 100PS 10PS 10PS 200PS 500PS
.TRAN 100PS 600PS
.meas tran tphl TRIG v(Vin) VAL=1.65 FALL=1 TARG v(Vout) VAL=1.65
RISE=1
.meas tran tplh TRIG v(Vin) VAL=1.65 RISE=1 TARG v(Vout) VAL=1.65
FALL=1
.meas tran tp_avg PARAM = (abs(tphl)+abs(tplh))/2
.END
```