International IslamicUniversity Islamabad Faculty of Engineering and Technology Department of Electricaland Computer Engineering

VLSI DESIGN LAB

EXPERIMENT Lab 12: NAND GATE

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Lab Performance Report#12

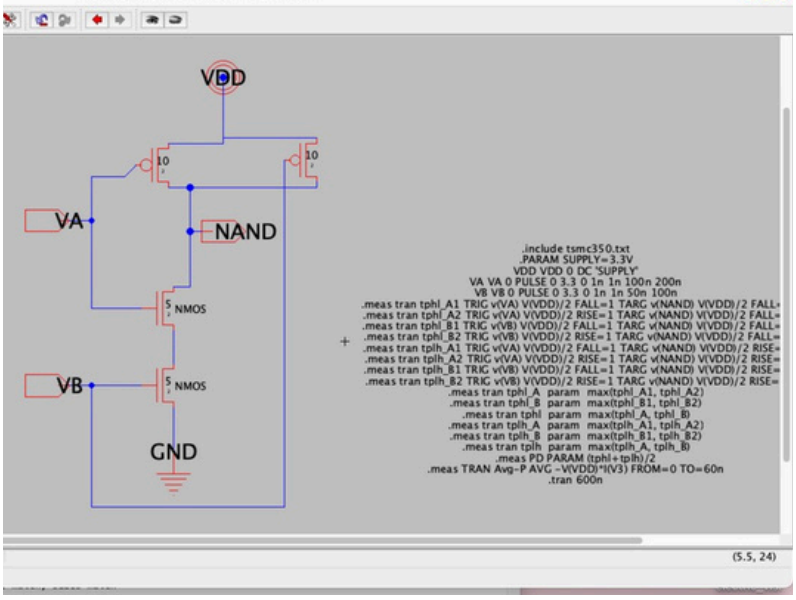
- Task#1:Pre-layout Simulation:
  - Buildup a 2 input NAND gate schematic step by step in Electric.
  - Transient analysis of NAND using pulse inputs A and B of your own choice in Electric
  - andobserve output in Ltspice
  - Use.meas command to evaluate propagation delay and power dissipation of the NAND. You may use the same commands as done in Lab#3.
  - Report the screenshots of schematic diagram, Spice netlist, I/O waveforms and log file

- Task#2:Post-layout Simulation
  - Draw stick diagram of 2 input NAND gate
  - Build up the physical layout of NAND gate step by step in Electric
  - Perform the Design Rule Check (DRC) and improve your design till there are no errors orwarnings.
  - Perform the layout vs schematic analysis (NCC) in electric. Improve your design till theschematic of task#1 and the layout perfectly match.
    Perform transient analysis of NAND gate layout in Electric and observe output in Ltspice
    Use.meas command to evaluate propagation delay and power dissipation of the NAND layout. Observe and compare the results of pre-layout simulation with post layout simulation.
  - Report the stick diagram, screenshots of layout diagram, Spice netlist, I/O waveforms, LTspice log file and your observations.

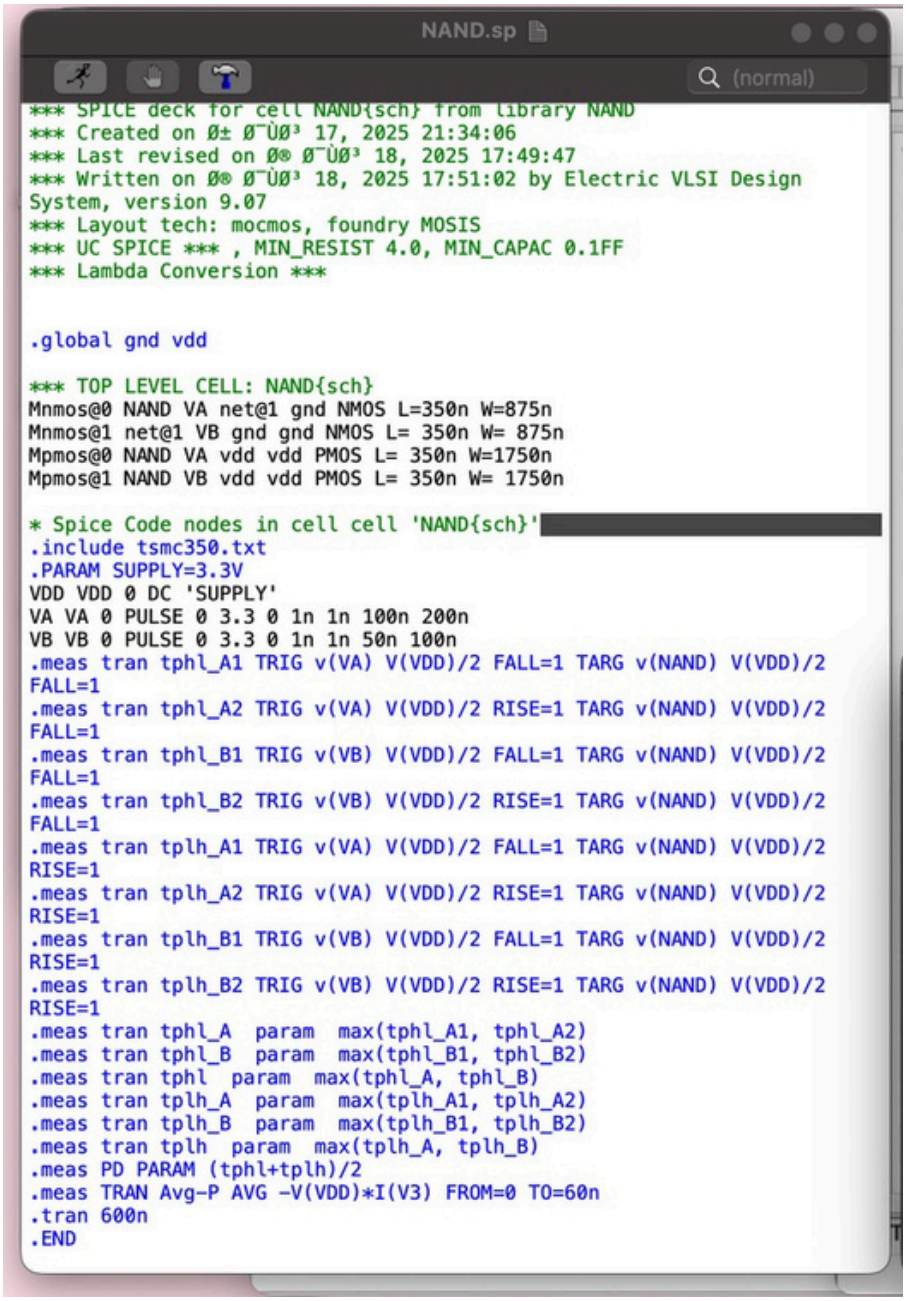
Caution: There is no unique solution to this assignment. All submissions should be different, like size of transistors, wiring of your schematic and selection of circuit parameters, inputs ando utputs. Zero marks will be awarded for exact copies, so avoid sharing your assignments with friends .

Task 1 :

schematic



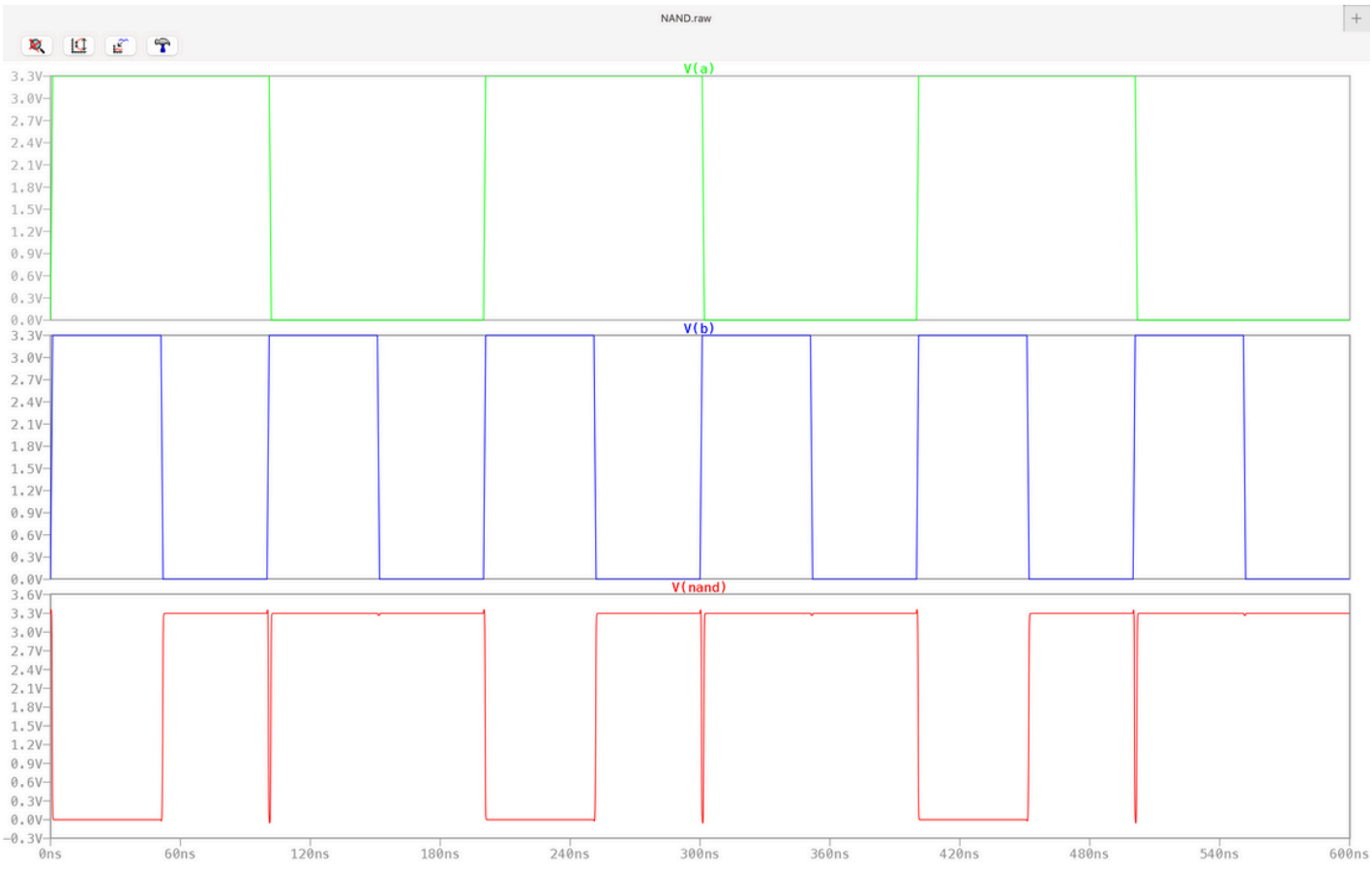
Netlist



SPICE Output Log

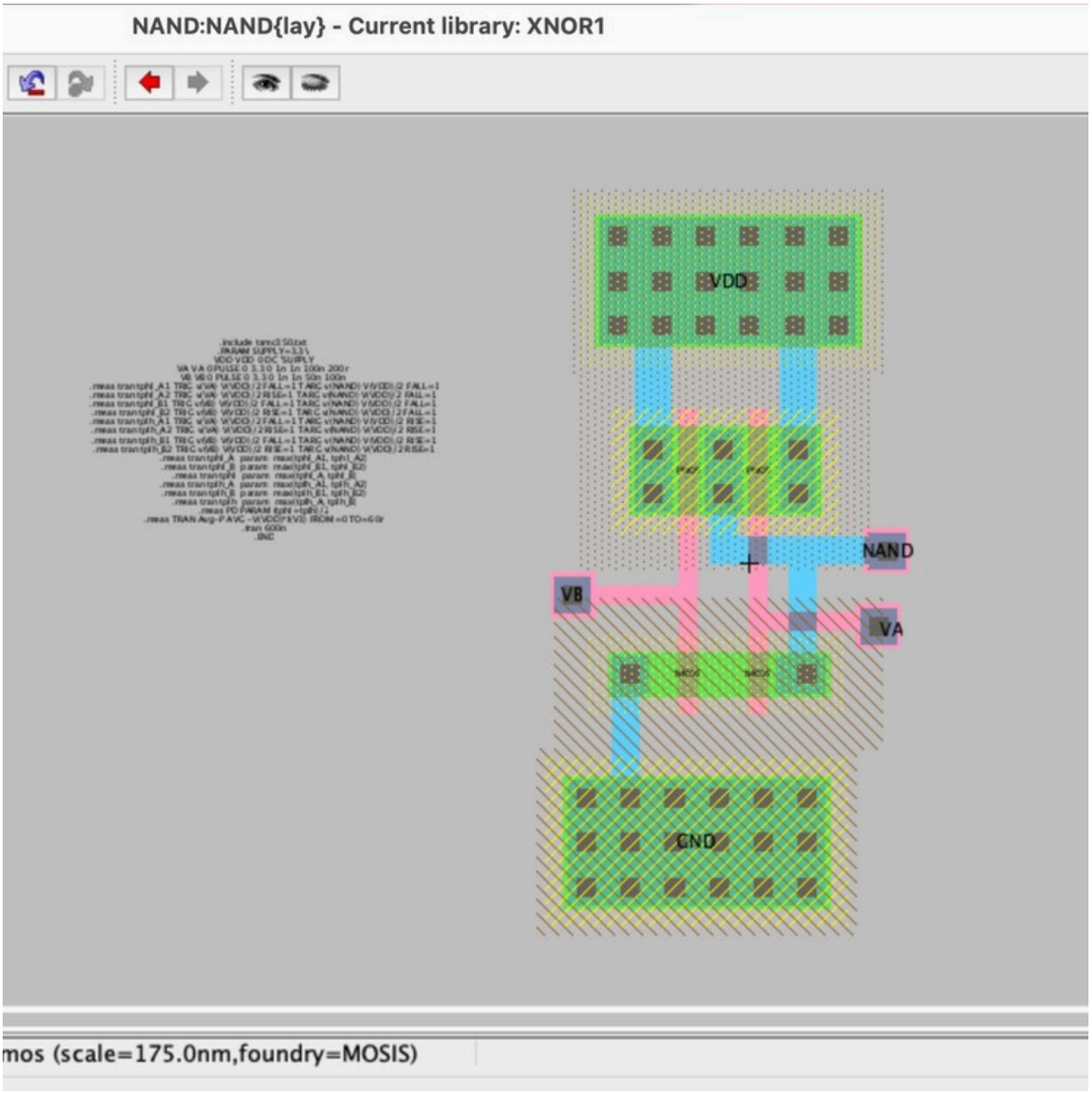
```
rect Newton iteration for .op point succeeded.

nl_a1=-1.00975e-07 FROM 1.015e-07 TO 5.24852e-10
nl_a2=2.48522e-11 FROM 5e-10 TO 5.24852e-10
nl_b1=-5.09751e-08 FROM 5.15e-08 TO 5.24852e-10
nl_b2=2.48522e-11 FROM 5e-10 TO 5.24852e-10
nh_a1=-4.98998e-08 FROM 1.015e-07 TO 5.16002e-08
nh_a2=5.11002e-08 FROM 5e-10 TO 5.16002e-08
nh_b1=1.00234e-10 FROM 5.15e-08 TO 5.16002e-08
nh_b2=5.11002e-08 FROM 5e-10 TO 5.16002e-08
nl_a: max(tphl_a1, tphl_a2)=2.48522e-11
nl_b: max(tphl_b1, tphl_b2)=2.48522e-11
nl: max(tphl_a, tphl_b)=2.48522e-11
nh_a: max(tplh_a1, tplh_a2)=5.11002e-08
nh_b: max(tplh_b1, tplh_b2)=5.11002e-08
nh: max(tplh_a, tplh_b)=5.11002e-08
  (tphl+tplh)/2=2.55625e-08

nsurement "avg-p" FAIL'ed

tal elapsed time: 0.035 seconds.
```

waveform



Task 2 :

layout



(DRC) , (NCC)

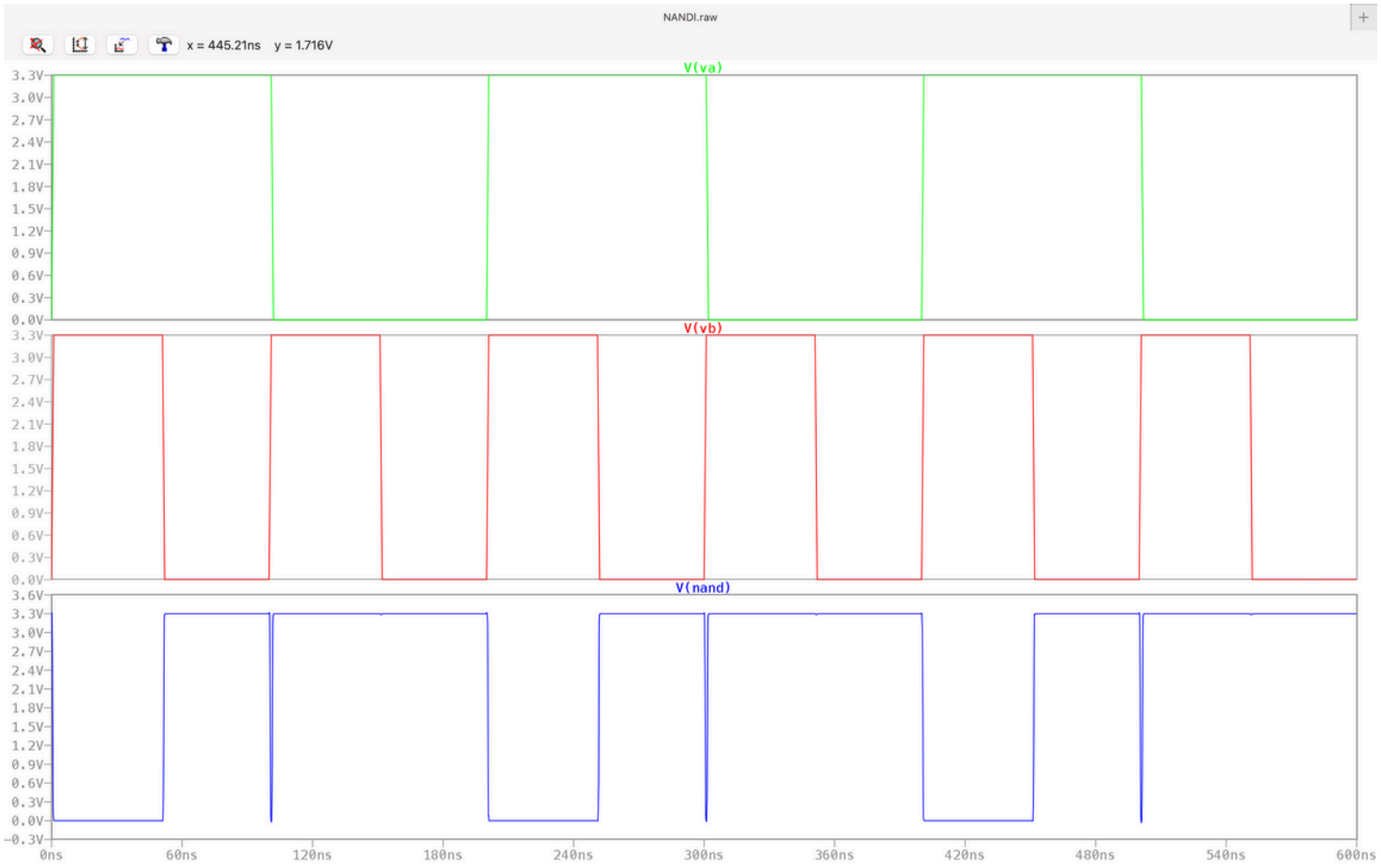
```
        No errors/warnings found
0 errors and 0 warnings found (took 0.04 secs)
================================200================================
Hierarchical NCC every cell in the design: cell 'NAND:NAND{sch}'  cell 'NAND:NAND{lay}'
Comparing: NAND:NAND{sch} with: NAND:NAND{lay}
  exports match, topologies match, sizes match in 0.017 seconds.
Summary for all cells: exports match, topologies match, sizes match
NCC command completed in: 0.02 seconds.
```

Netlist

NAND.sp

```
*** TOP LEVEL CELL: NAND{lay}
Mnmos@0 NAND A#0nmos@0_poly-left net@5 gnd NMOS L=0.7U W=2.8U AS=1.929P AD=5.553P
PS=4.725U PD=8.283U
Mnmos@1 net@5 B#0nmos@1_poly-left gnd gnd NMOS L=0.7U W=2.8U AS=26.95P AD=1.929P
PS=36.75U PD=4.725U
Mpmos@0 vdd A#2pmos@0_poly-right NAND vdd PMOS L=0.7U W=3.5U AS=5.553P AD=32.769P
PS=8.283U PD=28.35U
Mpmos@1 NAND B#2pmos@1_poly-right vdd vdd PMOS L=0.7U W=3.5U AS=32.769P AD=5.553P
PS=28.35U PD=8.283U
** Extracted Parasitic Capacitors ***
C0 AB 0 8.601fF
C1 B 0 0.137fF
C2 A 0 0.157fF
C3 A#0nmos@0_poly-left 0 0.105fF
C4 A#1pin@0_polysilicon-1 0 0.236fF
C5 B#1pin@1_polysilicon-1 0 0.236fF
C6 A#3pin@11_polysilicon-1 0 0.399fF
C7 A#4pin@12_polysilicon-1 0 0.294fF
C8 B#3pin@22_polysilicon-1 0 0.294fF
C9 B#4pin@23_polysilicon-1 0 0.294fF
C10 B#5pin@24_polysilicon-1 0 0.294fF
C11 A#2pmos@0_poly-right 0 0.131fF
C12 B#2pmos@1_poly-right 0 0.314fF
** Extracted Parasitic Resistors ***
R0 A#0nmos@0_poly-left A#0nmos@0_poly-left##0 6.2
C13 A#0nmos@0_poly-left##0 0 0.105fF
R1 A#0nmos@0_poly-left##0 A#1pin@0_polysilicon-1 6.2
R2 B#0nmos@1_poly-left B#1pin@1_polysilicon-1 6.2
R3 A#2pmos@0_poly-right A#2pmos@0_poly-right##0 7.75
C14 A#2pmos@0_poly-right##0 0 0.131fF
R4 A#2pmos@0_poly-right##0 A#3pin@11_polysilicon-1 7.75
R5 A#3pin@11_polysilicon-1 A#3pin@11_polysilicon-1##0 7.75
C15 A#3pin@11_polysilicon-1##0 0 0.131fF
R6 A#3pin@11_polysilicon-1##0 A#1pin@0_polysilicon-1 7.75
R7 A#3pin@11_polysilicon-1 A#3pin@11_polysilicon-1##0 7.233
C16 A#3pin@11_polysilicon-1##0 0 0.137fF
R8 A#3pin@11_polysilicon-1##0 A#3pin@11_polysilicon-1##1 7.233
C17 A#3pin@11_polysilicon-1##1 0 0.137fF
R9 A#3pin@11_polysilicon-1##1 A#4pin@12_polysilicon-1 7.233
R10 A#4pin@12_polysilicon-1 A#4pin@12_polysilicon-1##0 7.75
C18 A#4pin@12_polysilicon-1##0 0 0.157fF
R11 A#4pin@12_polysilicon-1##0 A#4pin@12_polysilicon-1##1 7.75
C19 A#4pin@12_polysilicon-1##1 0 0.157fF
R12 A#4pin@12_polysilicon-1##1 A#4pin@12_polysilicon-1##2 7.75
C20 A#4pin@12_polysilicon-1##2 0 0.157fF
R13 A#4pin@12_polysilicon-1##2 A 7.75
R14 B#2pmos@1_poly-right B#2pmos@1_poly-right##0 7.75
C21 B#2pmos@1_poly-right##0 0 0.157fF
R15 B#2pmos@1_poly-right##0 B#2pmos@1_poly-right##1 7.75
C22 B#2pmos@1_poly-right##1 0 0.157fF
R16 B#2pmos@1_poly-right##1 B#2pmos@1_poly-right##2 7.75
R17 B#2pmos@1_poly-right##2 B#1pin@1_polysilicon-1 7.75
R18 B#2pmos@1_poly-right B#2pmos@1_poly-right##0 9.3
C24 B#2pmos@1_poly-right##0 0 0.157fF
R19 B#2pmos@1_poly-right##0 B#3pin@22_polysilicon-1 9.3
R20 B#3pin@22_polysilicon-1 B#3pin@22_polysilicon-1##0 7.233
C25 B#3pin@22_polysilicon-1##0 0 0.137fF
R21 B#3pin@22_polysilicon-1##0 B#3pin@22_polysilicon-1##1 7.233
C26 B#3pin@22_polysilicon-1##1 0 0.137fF
R22 B#3pin@22_polysilicon-1##1 B#4pin@23_polysilicon-1 7.233
R23 B#4pin@23_polysilicon-1 B#4pin@23_polysilicon-1##0 9.3
C27 B#4pin@23_polysilicon-1##0 0 0.157fF
R24 B#4pin@23_polysilicon-1##0 B#5pin@24_polysilicon-1 9.3
R25 B#5pin@24_polysilicon-1 B#5pin@24_polysilicon-1##0 7.233
C28 B#5pin@24_polysilicon-1##0 0 0.137fF
R26 B#5pin@24_polysilicon-1##0 B#5pin@24_polysilicon-1##1 7.233
C29 B#5pin@24_polysilicon-1##1 0 0.137fF
R27 B#5pin@24_polysilicon-1##1 B 7.233

* Spice Code nodes in cell cell 'NAND{lay}'
.include tsmc350.txt
.PARAM SUPPLY=3.3V
VDD VDD 0 DC 'SUPPLY'
VA A 0 PULSE 0 3.3 0 1n 1n 100n 200n
VB B 0 PULSE 0 3.3 0 1n 1n 50n 100n
.meas tran tphl_A1 TRIG v(VA) V(VDD)/2 FALL=1 TARG v(NAND) V(VDD)/2 FALL=1
.meas tran tphl_A2 TRIG v(VA) V(VDD)/2 RISE=1 TARG v(NAND) V(VDD)/2 FALL=1
.meas tran tphl_B1 TRIG v(VB) V(VDD)/2 FALL=1 TARG v(NAND) V(VDD)/2 FALL=1
.meas tran tphl_B2 TRIG v(VB) V(VDD)/2 RISE=1 TARG v(NAND) V(VDD)/2 FALL=1
.meas tran tplh_A1 TRIG v(VA) V(VDD)/2 FALL=1 TARG v(NAND) V(VDD)/2 RISE=1
.meas tran tplh_A2 TRIG v(VA) V(VDD)/2 RISE=1 TARG v(NAND) V(VDD)/2 RISE=1
.meas tran tplh_B1 TRIG v(VB) V(VDD)/2 FALL=1 TARG v(NAND) V(VDD)/2 RISE=1
.meas tran tplh_B2 TRIG v(VB) V(VDD)/2 RISE=1 TARG v(NAND) V(VDD)/2 RISE=1
.meas tran tphl_A  param  max(tphl_A1, tphl_A2)
.meas tran tphl_B  param  max(tphl_B1, tphl_B2)
.meas tran tphl  param  max(tphl_A, tphl_B)
.meas tran tplh_A  param  max(tplh_A1, tplh_A2)
.meas tran tplh_B  param  max(tplh_B1, tplh_B2)
.meas tran tplh  param  max(tplh_A, tplh_B)
.meas PD PARAM (tphl+tplh)/2
.meas TRAN Avg-P AVG -V(VDD)*I(VDD) FROM=0 TO=60n
.tran 600n
.END
```

waveform


NANDl.raw
x = 445.21ns y = 1.716V
V(va)
V(vb)
V(nand)
0ns
60ns
120ns
180ns
240ns
300ns
360ns
420ns
480ns
540ns
600ns