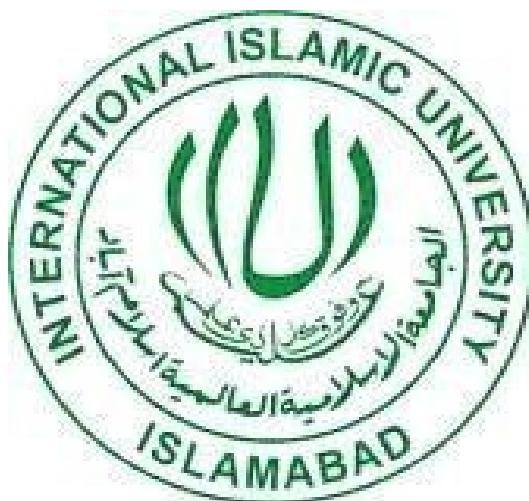


**International Islamic University Islamabad Faculty of  
Engineering and Technology Department of  
Electrical and Computer Engineering**

**VLSI DESIGN LAB**



**EXPERIMENT # 01: Operating Point and DC Analysis using Spice  
Netlist in LT-Spice**

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**Roll No.:** 1071-F22

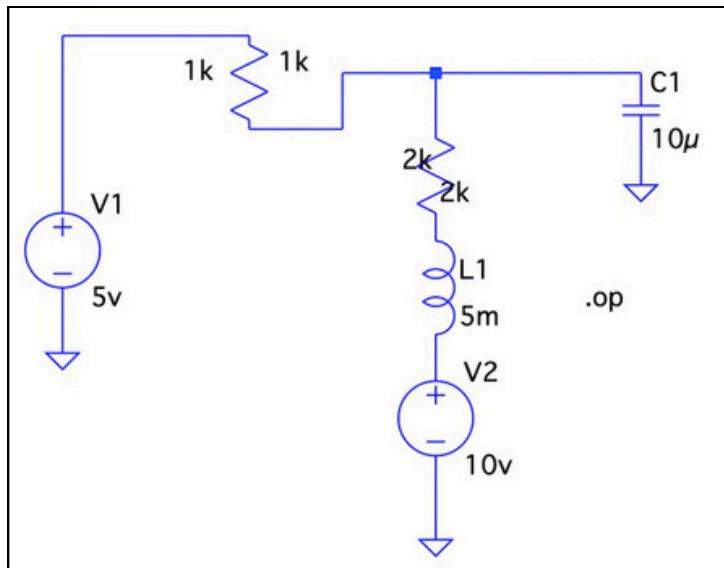
**Date of Experiment:** 18-sep-2025

# Lab Performance Report#1

- **Task1: Note:** For this task, please refer to your Circuit Analysis Text Book.
  - Choose any “5” or “more” node RLC circuit with 2 input DC voltage sources. Assign names to all the nodes (with natural numbers).
    - Create a new text document in your “Working Directory”. Write SPICE Netlist for the chosen circuit. “Save As” the text document with name: “[Name of Doc].cir”.
  - Open above-created .cir file in LTSpice and perform its operating point analysis.
  - Save screenshots of the original schematic, the netlist and the output.
- **Task2: Note:** For this task, please refer to your Electronic Circuit Design Text Book.
  - Choose any NMOS or PMOS transistor biased in Voltage Divider Bias topology. Assign names to all the circuit nodes (with natural numbers).
  - Create a new text document in your “Working Directory”. Write SPICE Netlist for the above chosen circuit. “Save As” the text document with name: “[Name of Doc].cir”.
  - Open above-created .cir file in LTSpice and perform its operating point analysis. Analyze the operating mode of the MOS transistor. Perturb the circuit element values till the MOS transistor operates in active mode.
  - Save screenshots of the original schematic, the netlist and the output.
  - Save as the netlist with a new name. Now perform **DC Sweep Analysis** of the netlist. Sweep the value of VDD from 0 to 3V in steps of 0.5V. Plot ID graph. Report your observations about the output.
  - Save screenshots of the original schematic, the netlist and the output.
- Compile and Submit a report in “**Printed Form**” within next lab whose structure should be:
  - Title Page
  - Screenshot of above tasks and analysis i.e. schematic, Spice Netlist and waveforms. Each task should be arranged on separate pages i.e. schematic on top, Netlist, waveform and observations below it.
- **Instructions:** There is no unique solution to this assignment. All submissions should be different like wiring of your schematic and selection of circuit parameters etc. Zero marks will be awarded for exact copies, so avoid sharing your assignments with friends.

**TASK 1:**

schematic



Netlist

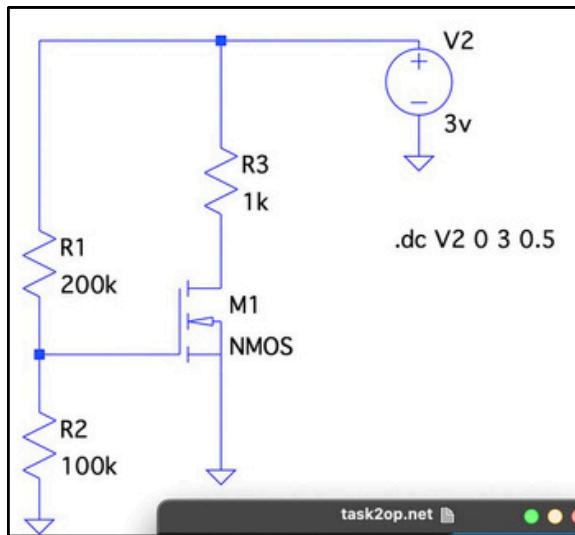
```
* /Users/bushra/Documents/LTspice/task1.asc
R$1k N001 N002 1k
R$2k N002 N003 2k
L1 N003 N004 5m
C1 N002 0 10μ
V1 N001 0 5v
V2 N004 0 10v
.op
.backanno
.end
```

**observations:**

The chosen 5-node RLC circuit with two DC sources was successfully simulated. The operating point analysis provided node voltages and branch currents as expected. The results from the netlist and schematic are consistent, confirming correct circuit implementation.

WAVEFORM



**TASK 2:****schematic****Netlist**

```
* /Users/bushra/Documents/LTspice/task2.asc
M1 N002 N003 0 0 NMOS
R1 N001 N003 200k
R2 N003 0 100k
R3 N001 N002 1k
V2 N001 0 3v
.model NMOS NMOS
.model PMOS PMOS
.lib /Users/bushra/Library/Application Support/
LTspice/lib/cmp/standard.mos
.dc V2 0 3 0.5
.backanno
.end
```

**observations:**

A DC sweep of VDD from 0 V to 3 V in 0.5 V steps was performed. The drain current (ID) increased as VDD increased, showing that the MOSFET entered the active region after a certain threshold voltage. The ID–VDD curve confirms the expected transistor behavior.

**WAVEFORM**