International IslamicUniversity Islamabad Faculty of Engineering and Technology Department of Electricaland Computer Engineering

VLSI DESIGN LAB

EXPERIMENT Lab 8: Design and Performance Analysis of SRAM Cells in LT- Spice

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Lab Performance Report#8

- Task#1: Create a schematic of 6-Transistor based SRAM cell that has logic 1 stored in the node connected with bit_line. (Note: Use initial condition .ic V(Q)=VDD and .ic V(Q_bar)=0 directives where Q and Q_bar are the internal nodes of SRAM cell that are connected to Bit line and Bit_Bar through access transistors). Simulate and record the resulting plots.

- Task#2: Using Word_Line and write driver transistors flip the data stored at node Q and Q_bar. Simulate and record the resulting plots.

- Task#3: Create a schematic of the SRAM Sense amplifier Pre_charge the Bit and Bit_Bar to VDD Now apply a voltage difference of 0.5 V between the bit and bit_bar lines and sense it using Word_Line and Sense_En inputs. The outputs Data and Data_Bar should establish a perfect logic 0 and logic 1. Simulate and record the resulting plots.

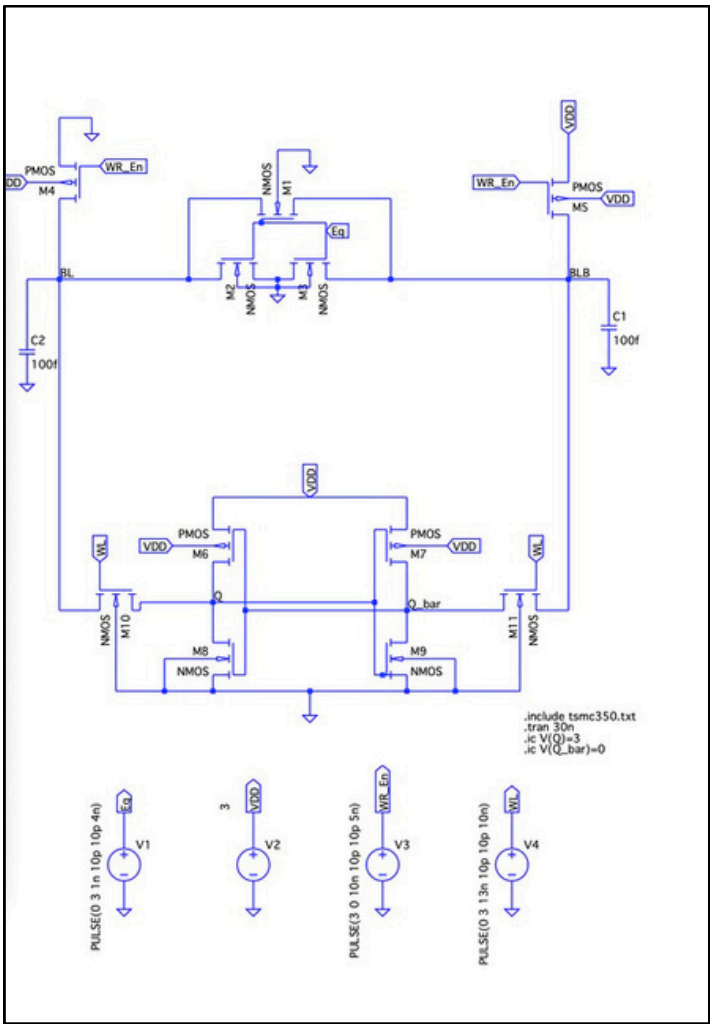
Submit a report in MS-Word format in Google Class whose structure should be:

  - Title Page
  - Screenshots of each of the above tasks. Each task should be arranged on one page i.e. schematic on top, its waveform/outputs below it and your remarks/analysis in a few lines.

Caution: There is no unique solution to this assignment. All submissions should be different, like wiring of your schematic and selection of circuit parameters, inputs and outputs. Zero marks will be awarded for exact copies, so avoid sharing your assignments with friends.

Task 1 & 2 :

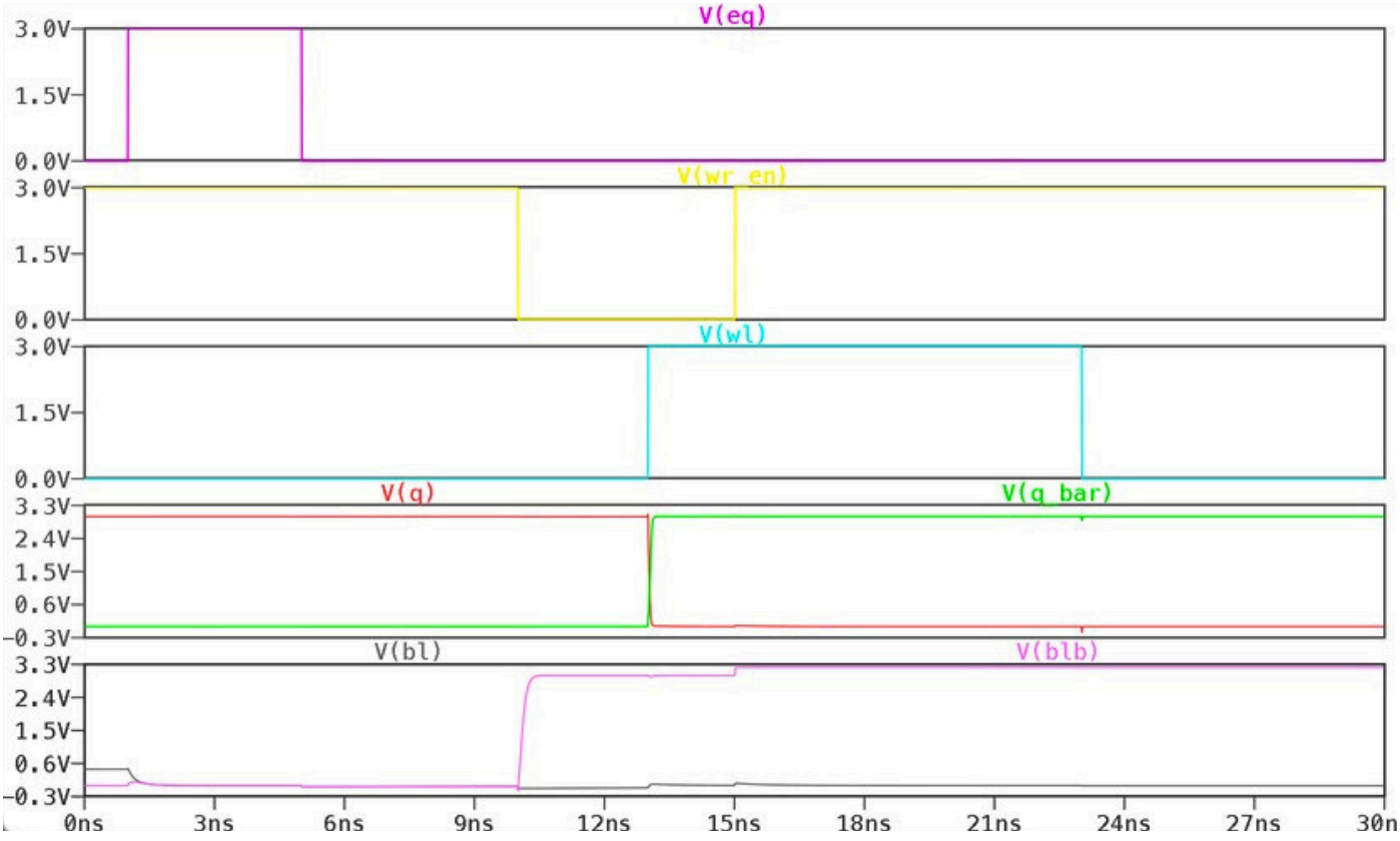
schematic



A 6T SRAM cell was designed and initialized to store logic ‘1’ at Q and logic ‘0’ at Q using initial conditions.

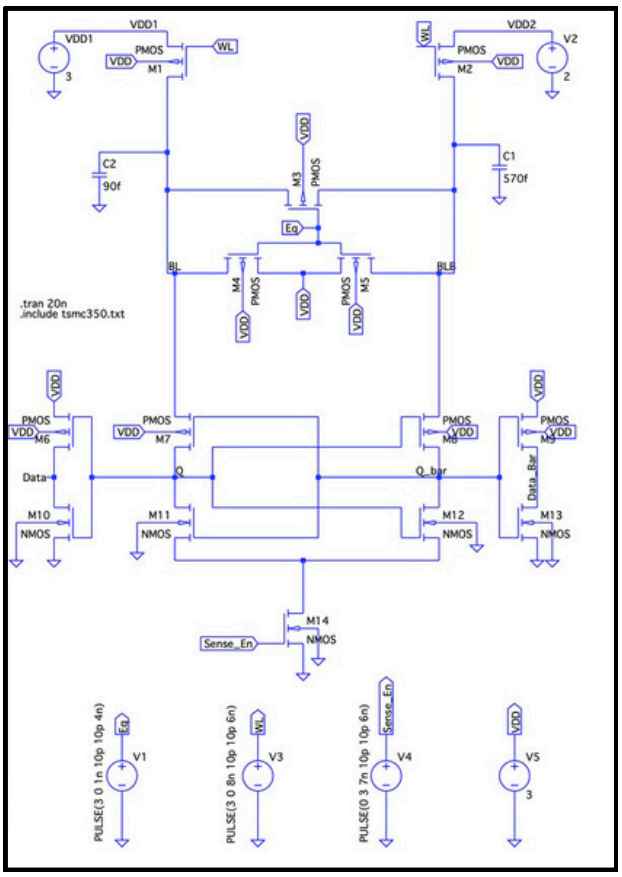
The stored data was successfully flipped using the Word_Line and write drivers, as confirmed by the simulation results.

WAVEFORM



Task 3 :

schematic



The SRAM sense amplifier was simulated by precharging Bit and Bit_Bar to VDD and applying a 0.5 V differential voltage.

When Sense_En was enabled, the amplifier correctly produced full logic levels at Data and Data_Bar.

WAVEFORM