International IslamicUniversity Islamabad Faculty of Engineering and Technology Department of Electricaland Computer Engineering

VLSI DESIGN LAB

EXPERIMENT # 05: Design and Performance Analysis of the MOSFET Amplifiers

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Lab Performance Report#5

Task#1 Creating Schematic: Create a schematic of an NMOS biased in Voltage Divider (source bypassed) configuration. Choose transistor length and resistances values of your own whereas for NMOS, W = 10xL . You may consult any text or a reference book. Try to choose a unique circuit. Task#2 Generating Symbol: Create the symbol of the amplifier that you made in Task#1. The symbol should have four I/O pins i.e. Vin , Vout, VDD, and VSS.

Task#3 DC Operating Point Analysis: Create a new schematic using the same symbol created in Task#2 and connecting it to VDD = 3.3 V and VSS = Gnd. Perform DC operating point analysis. Take a screenshot of the output popup window. Write your remarks about the output values. See if the NMOS is biased in saturation mode or not. If it is not in saturation, then change the resistance values of task#1. Re-simulate and repeat the process till NMOS comes in saturation mode. Take screenshot of your adjusted circuit of task#1 along with the results of DC operating point analysis for making the report.

Task#4 DC Sweep Analysis: Create a new schematic using the same symbol created in Task#2 and connecting it to VDD = 3.3 V and VSS = Gnd. Perform DC Sweep Analysis analysis by varying input voltage from 0 to 3.3 volt in steps of 0.1V. Plot the output vs input voltage results. Take screenshot of the schematic output. Write your remarks about the output. Why the output varies with input voltage?

Task#5 AC Transient Analysis: "Save as" the final circuit of task#3 (.asc file) and create a new schematic from it. Insert coupling capacitors at input and output pins. Choose suitable values for coupling capacitors. Insert R at output node choosing suitable value. Select any sine wave signal

L

whose amplitude is between 5mV to 50mV and frequency value between 1k to 15k Hz. Perform the transient analysis of this circuit. Report the screenshots of the schematic, output voltage, current and power waveforms and gain of the amplifier calculated via spice .meas commands.

Task#6 AC Sweep Analysis (Frequency Analysis): "Save as" the final circuit of task#5 (.asc file) and create a new schematic from it. Perform AC Sweep Analysis by varying input voltage frequency from 1Hz to 1Meg Hz keeping amplitude fixed at 70 mV. Plot the output/input ratio results. Take screenshots of the schematic and output. Observe and report the cut-off frequency and type of frequency response (i.e., Low Pass, High Pass, or Band Pass etc).

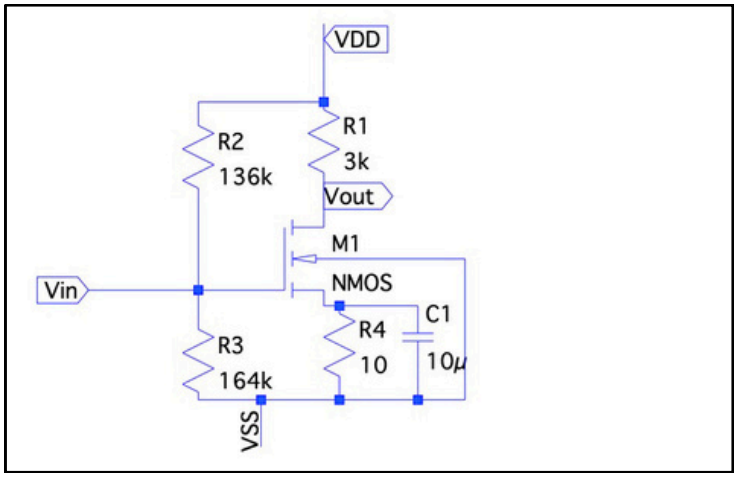
o Submit the report in printed form whose structure should be:

- Title Page
- Screenshots of each of the above tasks. Each task should be arranged on one page i.e. schematic/spice_netlist on top, its waveform/outputs below it and your remarks/analysis in a few lines.

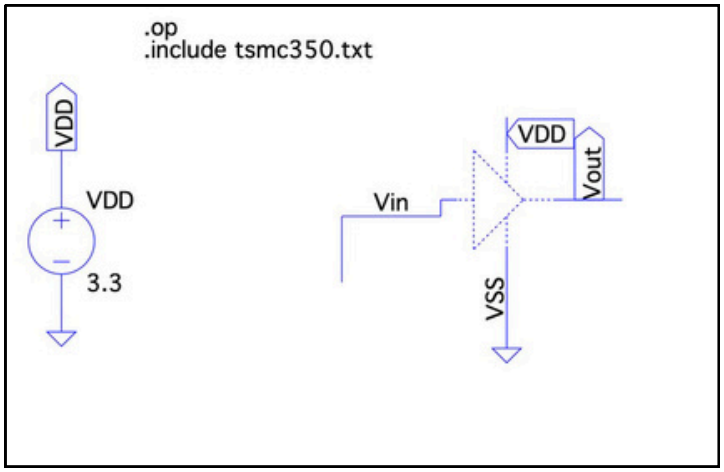
o Caution: There is no unique solution to this assignment. All submissions should be different, like wiring of your schematic and selection of circuit parameters, inputs and outputs. Zero marks will be awarded for exact copies, so avoid sharing your assignments with friends.

Task 1, 2, 3 :

schematic creation



schematic



SPICE Output Log

lab5tasks123.log

Search

```
--- BSIM3 MOSFETS ---
Name:       m:x1:1
Model:       nmos
Id:        4.82e-04
Vgs:       1.80e+00
Vds:       1.85e+00
Vbs:      -4.82e-03
Vth:       7.64e-01
Vdsat:     5.38e-01
Gm:        6.36e-04
Gds:       4.49e-05
Gmb        1.43e-04
Cbd:       0.00e+00
Cbs:       0.00e+00
Cgsov:     8.96e-16
Cgdov:     8.96e-16
Cgbov:     3.03e-17
dQgdVgb:   5.35e-15
dQgdVdb:  -7.90e-16
dQgdVsb:  -4.29e-15
dQddVgb:  -2.32e-15
dQddVdb:   8.34e-16
dQddVsb:   1.91e-15
dQbdVgb:  -7.22e-16
dQbdVdb:   1.78e-17
dQbdVsb:  -4.31e-16


Operating Bias Point Solution:
V(vdd)                        3.3   voltage
V(vout)                   1.85443   voltage
V(vin)                      1.804   voltage
I(Vdd)              -0.000492855   device_current
Ix(x1:VIN)          -3.38813e-21   subckt_current
Ix(x1:VDD)           0.000492855   subckt_current
Ix(x1:VSS)          -0.000492855   subckt_current
Ix(x1:VOUT)         -4.15298e-15   subckt_current

Total elapsed time: 0.135 seconds.
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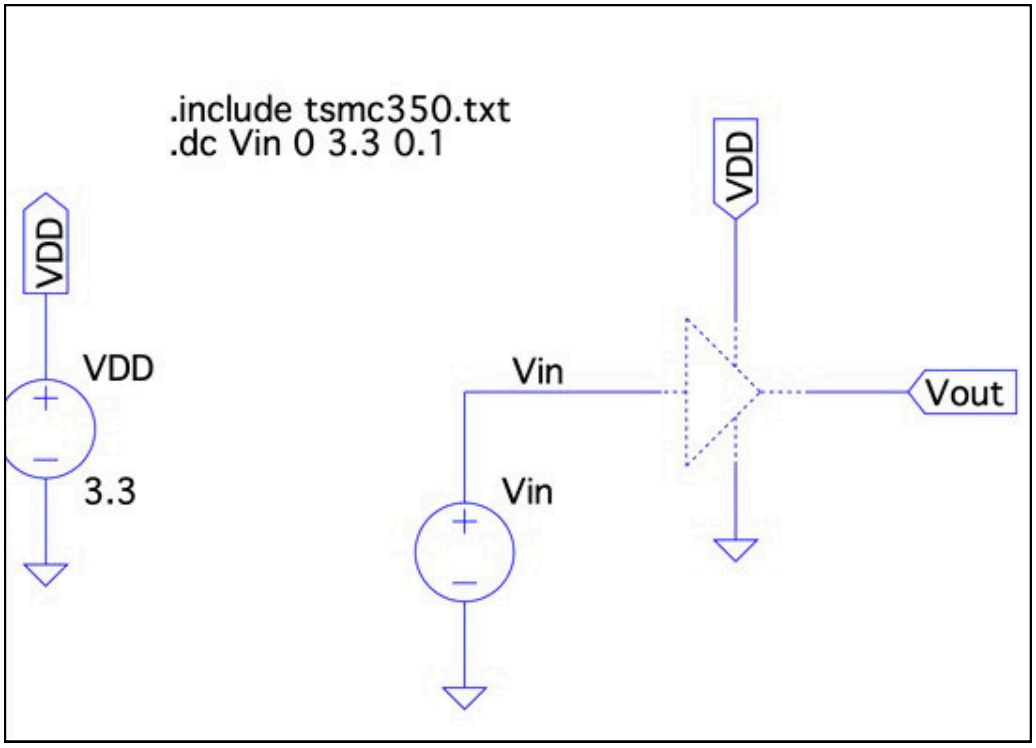
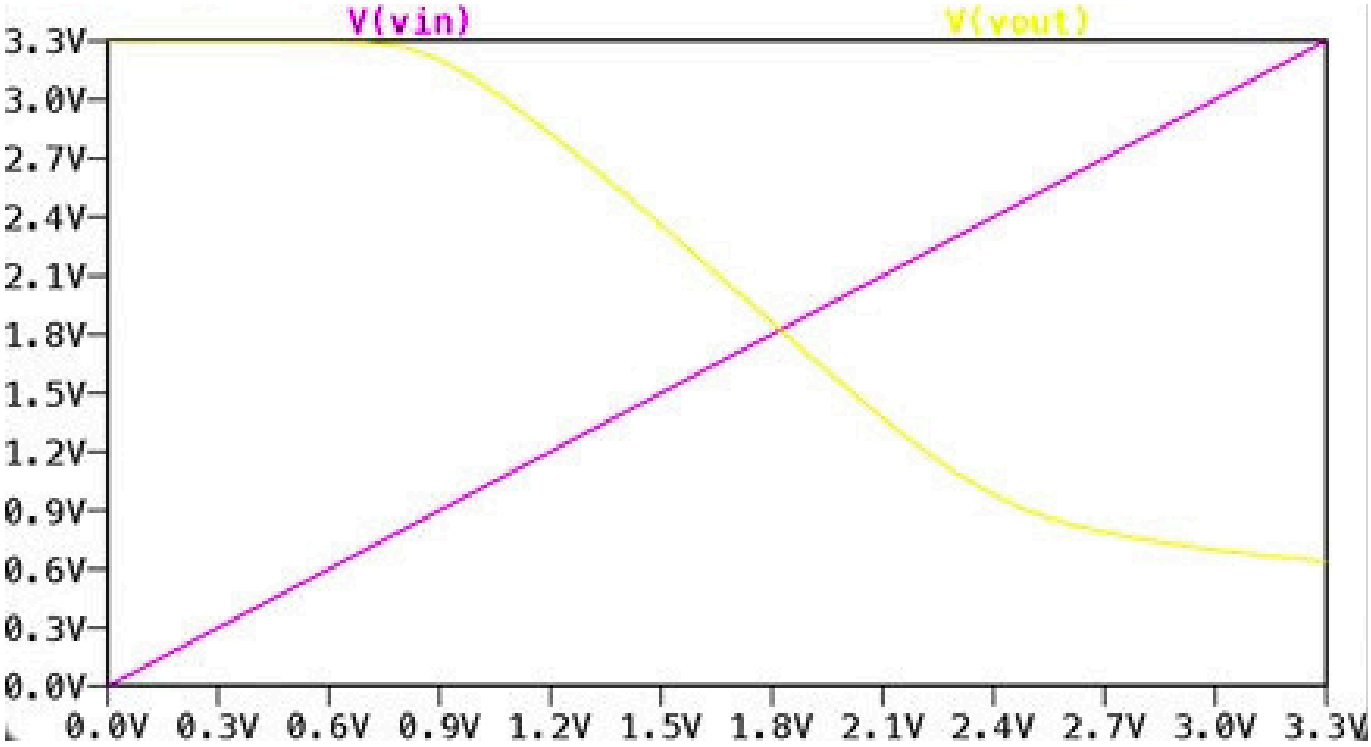
observations:

The NMOS was found to operate in saturation region after adjusting the bias resistors, confirming correct biasing conditions as VDS> VDS(SAT)

Task4 :

schematic & WAVEFORM



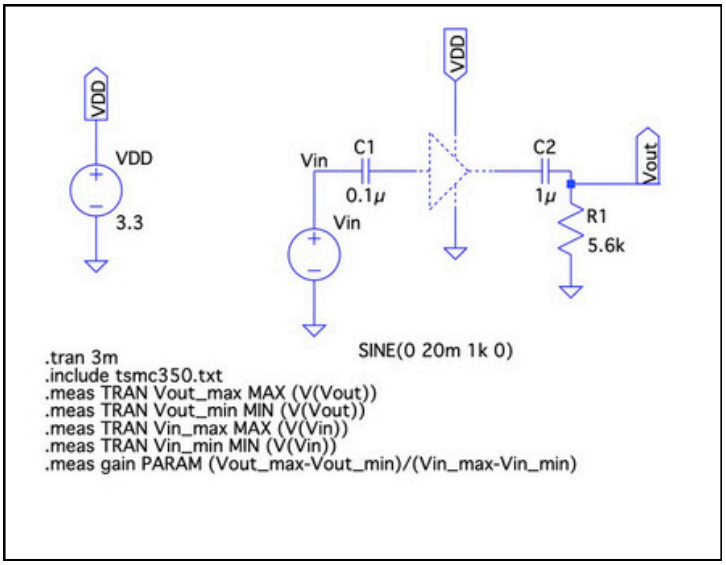


observations:

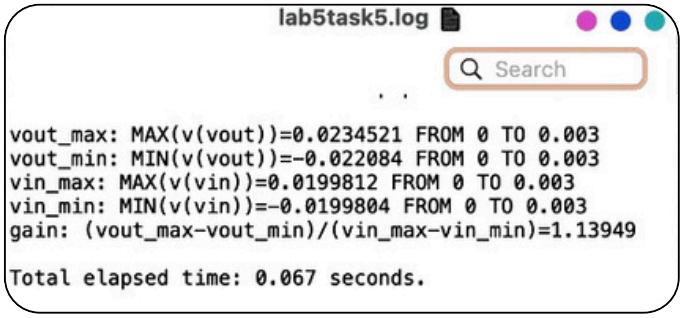
The DC sweep analysis shows that the output voltage decreases as the input voltage increases, confirming the inverting behavior of the common-source NMOS amplifier.

task 5 :

schematic



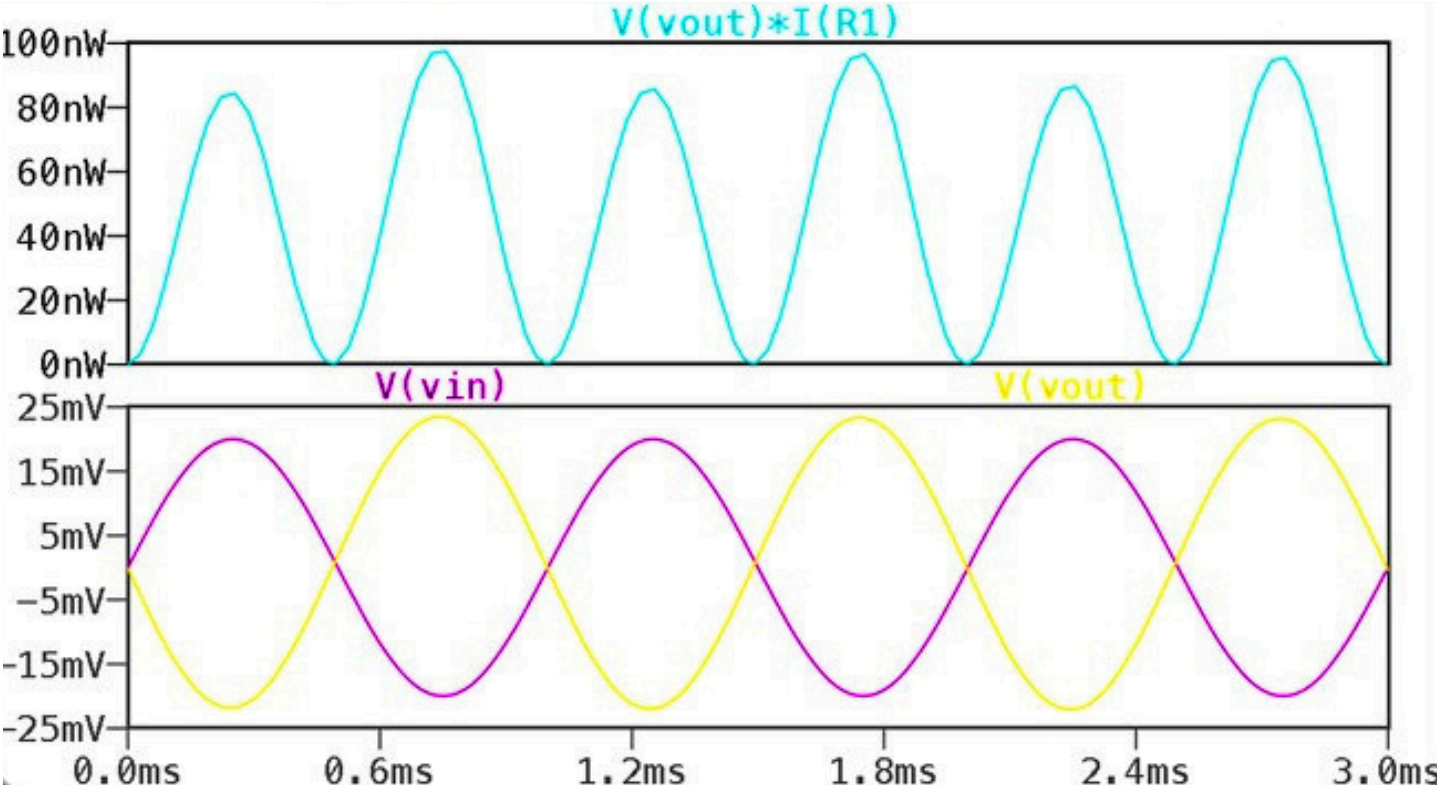
SPICE Output Log



observations:

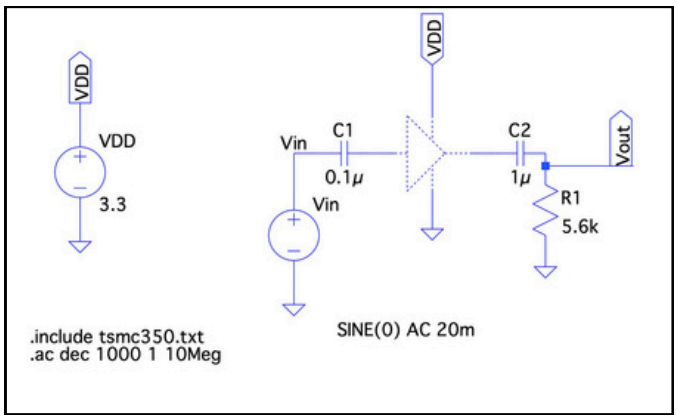
AC transient simulation was performed using a small sine input. The output waveform shows clear amplification. The gain was measured successfully using the .meas command GAIN=1.13

WAVEFORM



task 6 :

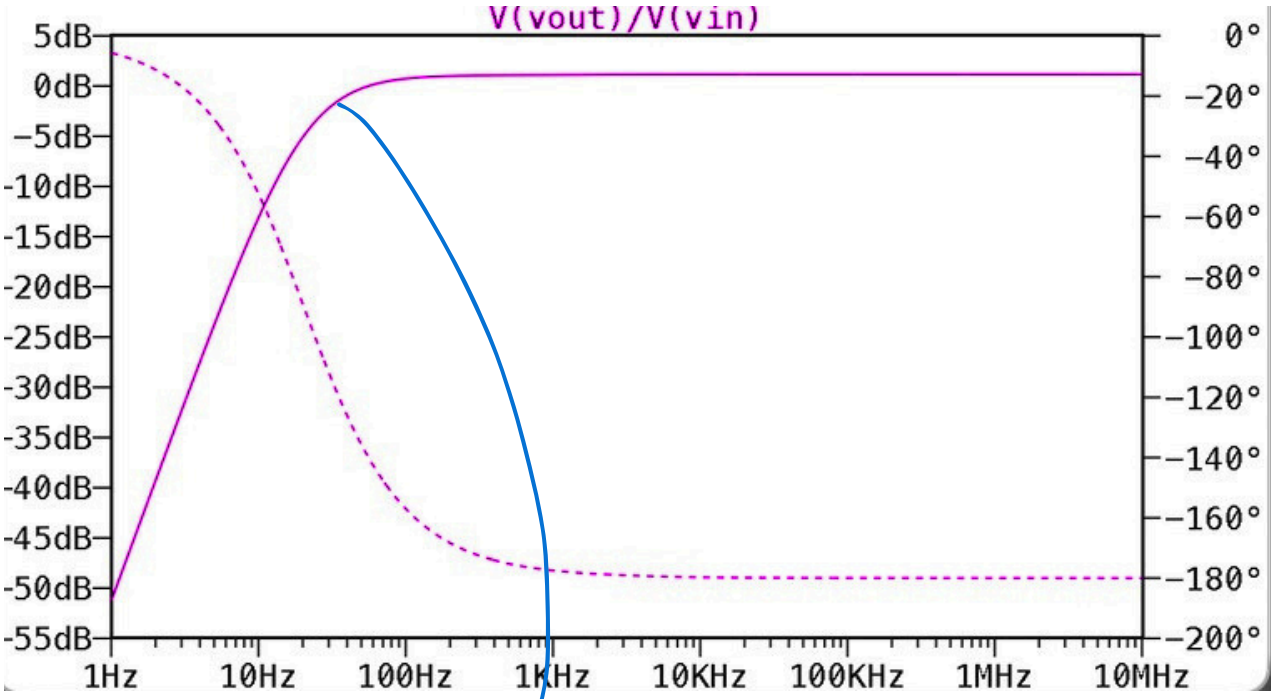
schematic



observations:

The AC sweep analysis shows a low-pass frequency response. The cutoff frequency was identified from the Bode plot Fc=30Hz

WAVEFORM



x = 29.620Hz y = -2.053dB, -23.510°