International IslamicUniversity Islamabad Faculty of Engineering and Technology Department of Electricaland Computer Engineering

VLSI DESIGN LAB

EXPERIMENT # 03: Schematic Design and Transient Analysis of NAND/NOR Gates

Name of Student: Bushra Nazir Ahmed

Roll No.: 1071-F22

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International Islamic University Islamabad

FacultyofEngineering&Technology

DepartmentofElectricalandComputerEngineering

VLSI Design Lab (EE408L)

Lab Performance Report#3

- Task#1: CreateNAND gateschematicandsymbol in LT-Spice. Callthe NAND gate symbol you created from the component library into a new schematic. Perform its transient analysis using two different pulse inputs of your own choice (make sure that each of tr and tf should be 5% of the time period.) Vary the PMOS and NMOS transistor sizes till you get a symmetric output waveform (i.e. tpHL = tpLH).
- Task#2: Create NOR gate schematic and symbol in LT-Spice. Call the NOR gate symbol you created from the component library into a new schematic. Perform its transient analysis using two different pulse inputs of your own choice (make sure that each of tr and tf should be 5% of the time period.) Vary the PMOS and NMOS transistor sizes till you get a symmetric output waveform (i.e. tpHL = tpLH).

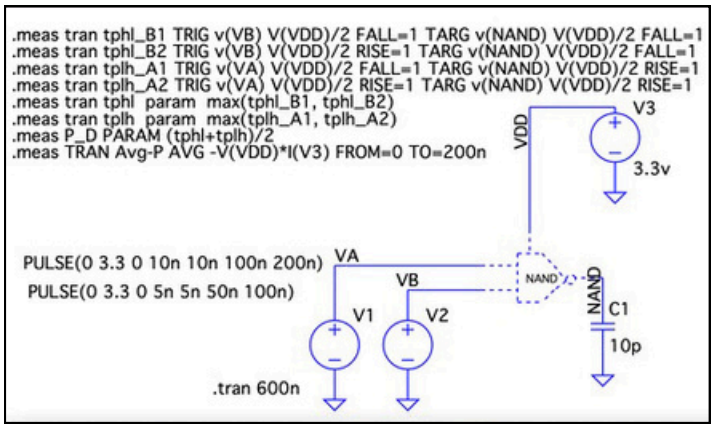
- Perform following analysis for both NAND and NOR Gates
- Analysis#1: Perform Transient analysis for 3 time periods of the input pulse (i.e., input with larger T). Show output vs input voltage waveforms. Write your observations by comparing it with truth-table.
- Analysis#2: Find the Propagation Delay using a simple waveform observation technique as discussed in the demo: tpHL , tpLH and tp1=(tpHL + tpLH). Reduce the rise and fall times of the input waveforms to 0.1% of their respective time-periods. Again, find the average propagation delay tp2. Compare tp2 with the previous tp1 to see the effect of change in tr and tf. Write down your observations in few lines.
- Analysis#3: Find the Propagation Delay this time using .meas spice directive and report the log file's screenshot. Write your observation in two lines.
- Analysis#4: Sketch instantaneous Power in new plot pane. Observe and highlight the maximum instantaneous power from the waveform.
- Analysis#5: Find Average Power consumption for one time period of the input with "longer T" using .meas SPICE directive. Report the observed results along with screenshot of the output log fille.

Task1 : NAND with tr = tf = 5% of T :

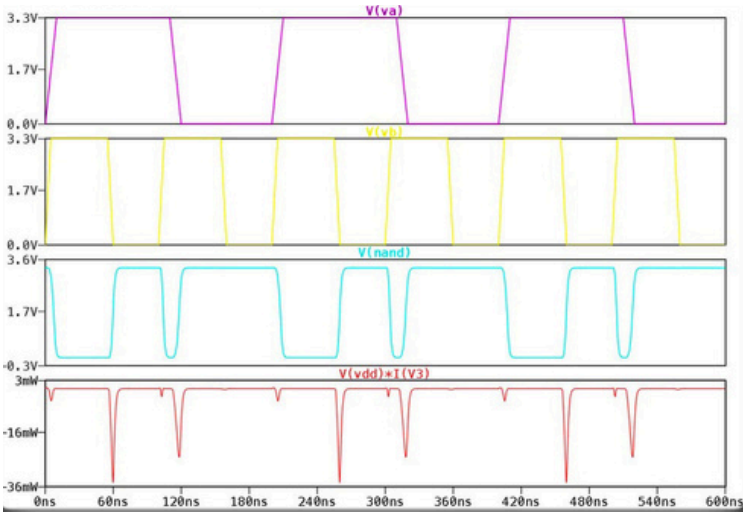
Netlist

```
* /Users/bushra/Desktop/LTspice/Lab3-task2.asc
XNAND VA VB VDD NAND nand
V1 VA 0 PULSE(0 3.3 0 10n 10n 100n 200n)
V2 VB 0 PULSE(0 3.3 0 5n 5n 50n 100n)
V3 VDD 0 3.3v
C1 NAND 0 10p

* block symbol definitions
.subckt nand VA VB VDD NAND
M1 VDD VA NAND VDD PMOS l=350n w=55u
M2 NAND VB VDD VDD PMOS l=350n w=55u
M3 NAND VA N001 N001 NMOS l=350n w=45u
M4 N001 VB 0 0 NMOS l=350n w=45u
.include tsmc350.txt
.ends nand

.model NMOS NMOS
.model PMOS PMOS
.lib /Users/bushra/Library/Application Support/LTspice/lib/cmp/
standard.mos
.tran 600n
.meas tran tphl_B1 TRIG v(VB) V(VDD)/2 FALL=1 TARG v(NAND) V(VDD)/2
FALL=1
.meas tran tphl_B2 TRIG v(VB) V(VDD)/2 RISE=1 TARG v(NAND) V(VDD)/2
FALL=1
.meas tran tplh_A1 TRIG v(VA) V(VDD)/2 FALL=1 TARG v(NAND) V(VDD)/2
RISE=1
.meas tran tplh_A2 TRIG v(VA) V(VDD)/2 RISE=1 TARG v(NAND) V(VDD)/2
RISE=1
.meas tran tphl  param  max(tphl_B1, tphl_B2)
.meas tran tplh  param  max(tplh_A1, tplh_A2)
.meas P_D PARAM (tphl+tplh)/2
.meas TRAN Avg-P AVG -V(VDD)*I(V3) FROM=0 TO=200n
.backanno
.end
```

schematic



WAVEFORM



SPICE Output Log

```
tphl_b1=-4.99989e-08 FROM 5.75e-08 TO 7.50109e-09
tphl_b2=5.00109e-09 FROM 2.5e-09 TO 7.50109e-09
tplh_a1=-5.5144e-08 FROM 1.15e-07 TO 5.9856e-08
tplh_a2=5.4856e-08 FROM 5e-09 TO 5.9856e-08
tphl: max(tphl_b1, tphl_b2)=5.00109e-09
tplh: max(tplh_a1, tplh_a2)=5.4856e-08
p_d: (tphl+tplh)/2=2.99286e-08
avg-p: AVG(-v(vdd)*i(v3))=0.00126175 FROM 0 TO 2e-07

Total elapsed time: 0.082 seconds.
```

observations:

The NAND gate schematic and symbol were successfully created. The circuit works properly with the defined connections between PMOS and NMOS transistors.

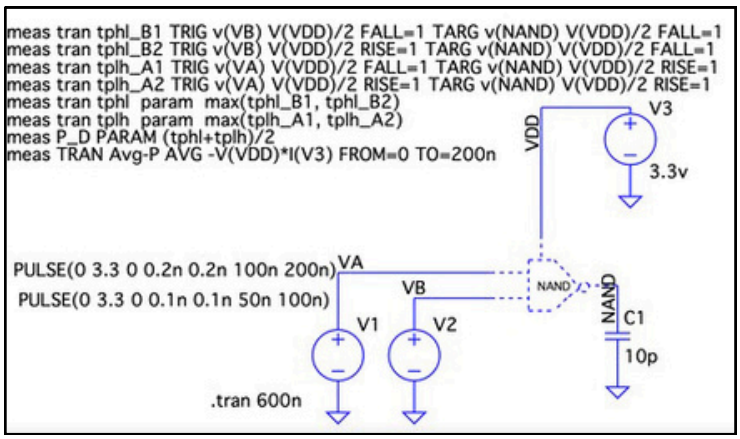
The transient analysis using two pulse inputs with tr and tf equal to 5% of the period. The output delay increased compared to faster rise/fall times (e.g., 0.1%) due to slower input transitions.

Task1 : NAND with tr = tf = 0.1% of T :

Netlist

```
* /Users/bushra/Desktop/LTspice/Lab3-task2.asc
XNAND VA VB VDD NAND nand
V1 VA 0 PULSE(0 3.3 0 0.2n 0.2n 100n 200n)
V2 VB 0 PULSE(0 3.3 0 0.1n 0.1n 50n 100n)
V3 VDD 0 3.3v
C1 NAND 0 10p

* block symbol definitions
.subckt nand VA VB VDD NAND
M1 VDD VA NAND VDD PMOS l=350n w=55u
M2 NAND VB VDD VDD PMOS l=350n w=55u
M3 NAND VA N001 N001 NMOS l=350n w=45u
M4 N001 VB 0 0 NMOS l=350n w=45u
.include tsmc350.txt
.ends nand

.model NMOS NMOS
.model PMOS PMOS
.lib /Users/bushra/Library/Application Support/LTspice/lib/cmp/
standard.mos
.tran 600n
.meas tran tphl_B1 TRIG v(VB) V(VDD)/2 FALL=1 TARG v(NAND) V(VDD)/2
FALL=1
.meas tran tphl_B2 TRIG v(VB) V(VDD)/2 RISE=1 TARG v(NAND) V(VDD)/2
FALL=1
.meas tran tplh_A1 TRIG v(VA) V(VDD)/2 FALL=1 TARG v(NAND) V(VDD)/2
RISE=1
.meas tran tplh_A2 TRIG v(VA) V(VDD)/2 RISE=1 TARG v(NAND) V(VDD)/2
RISE=1
.meas tran tphl  param  max(tphl_B1, tphl_B2)
.meas tran tplh  param  max(tplh_A1, tplh_A2)
.meas P_D PARAM (tphl+tplh)/2
.meas TRAN Avg-P AVG -V(VDD)*I(V3) FROM=0 TO=200n
.backanno
.end
```

schematic



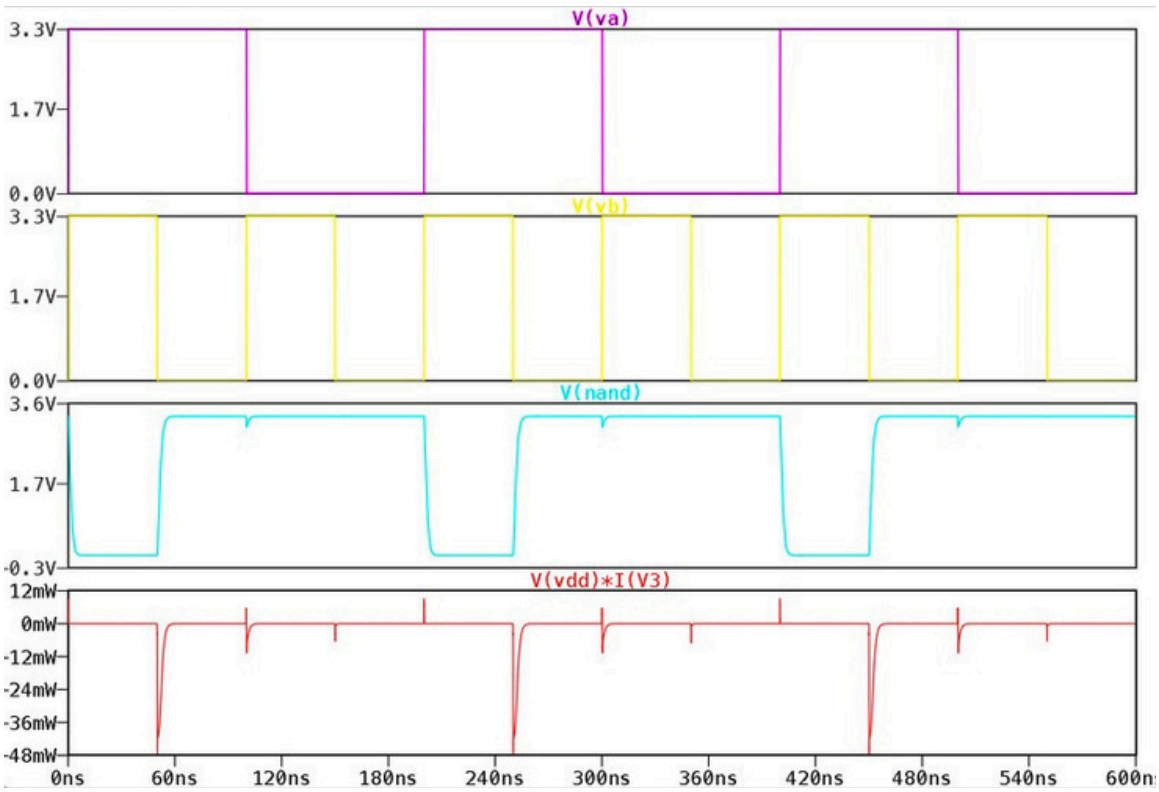
observations:

The output delay decreased

SPICE Output Log

```
tphl_b1=-4.87194e-08 FROM 5.015e-08 TO 1.43064e-09
tphl_b2=1.38064e-09 FROM 5e-11 TO 1.43064e-09
tplh_a1=-4.87099e-08 FROM 1.003e-07 TO 5.15901e-08
tplh_a2=5.14901e-08 FROM 1e-10 TO 5.15901e-08
tphl: max(tphl_b1, tphl_b2)=1.38064e-09
tplh: max(tplh_a1, tplh_a2)=5.14901e-08
p_d: (tphl+tplh)/2=2.64354e-08
avg-p: AVG(-v(vdd)*i(v3))=0.000604624 FROM 0 TO 2e-07

Total elapsed time: 0.080 seconds.
```

WAVEFORM

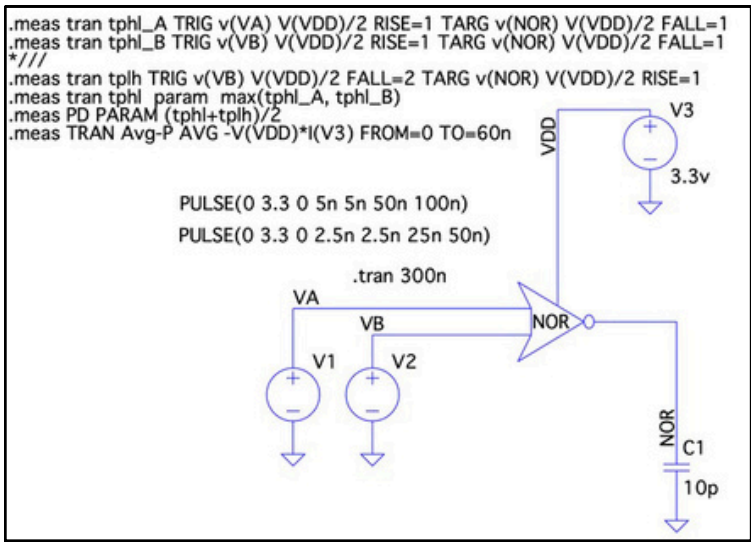


Task2 : NOR with tr = tf = 5% of T :

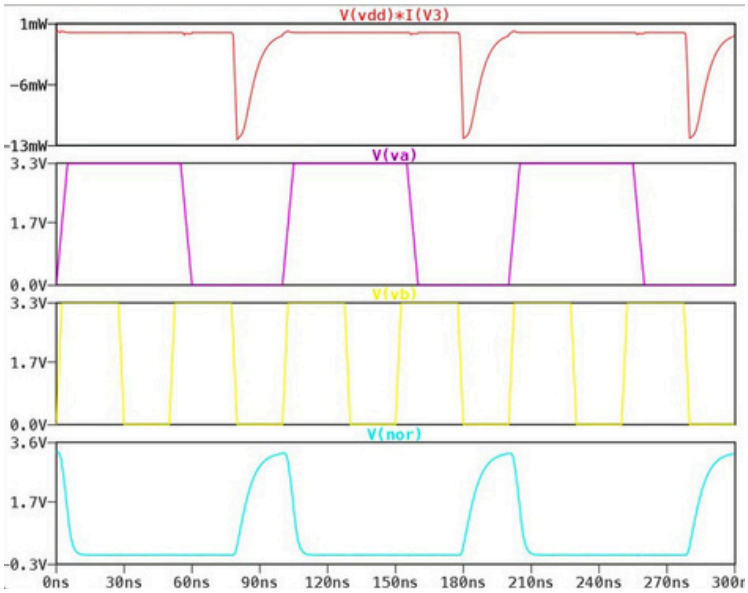
Netlist

```
* /Users/bushra/Desktop/LTspice/Lab3-NOR.asc
V1 VA 0 PULSE(0 3.3 0 5n 5n 50n 100n)
V2 VB 0 PULSE(0 3.3 0 2.5n 2.5n 25n 50n)
V3 VDD 0 3.3v
C1 NOR 0 10p
XNOR NOR VA VB VDD nor

* block symbol definitions
.subckt nor NOR VA VB VDD
M1 N002 VA VDD N001 PMOS l=350n w=30u
M2 NOR VB N002 N001 PMOS l=350n w=30u
M3 NOR VA 0 N003 NMOS l=350n w=8u
M4 NOR VB 0 N004 NMOS l=350n w=8u
.include tsmc350.txt
.ends nor

.model NMOS NMOS
.model PMOS PMOS
.lib /Users/bushra/Library/Application Support/LTspice/lib/cmp/
standard.mos
.tran 300n
.meas tran tphl_A TRIG v(VA) V(VDD)/2 RISE=1 TARG v(NOR) V(VDD)/2
FALL=1
.meas tran tphl_B TRIG v(VB) V(VDD)/2 RISE=1 TARG v(NOR) V(VDD)/2
FALL=1
*///
.meas tran tplh TRIG v(VB) V(VDD)/2 FALL=2 TARG v(NOR) V(VDD)/2 RISE=1
.meas tran tphl  param  max(tphl_A, tphl_B)
.meas PD PARAM (tphl+tplh)/2
.meas TRAN Avg-P AVG -V(VDD)*I(V3) FROM=0 TO=60n
.backanno
.end
```

schematic



WAVEFORM



SPICE Output Log

Lab3-NOR.log

Search

```
tphl_a=2.12319e-09 FROM 2.5e-09 TO 4.62319e-09
tphl_b=3.37319e-09 FROM 1.25e-09 TO 4.62319e-09
tplh=5.05075e-09 FROM 7.875e-08 TO 8.38008e-08
tphl: max(tphl_a, tphl_b)=3.37319e-09
pd: (tphl+tplh)/2=4.21197e-09
avg-p: AVG(-v(vdd)*i(v3))=1.25732e-06 FROM 0 TO 6e-08

Total elapsed time: 0.074 seconds.
```

observations:

The NOR gate schematic and symbol were successfully created. The circuit works properly with the defined connections between PMOS and NMOS transistors.

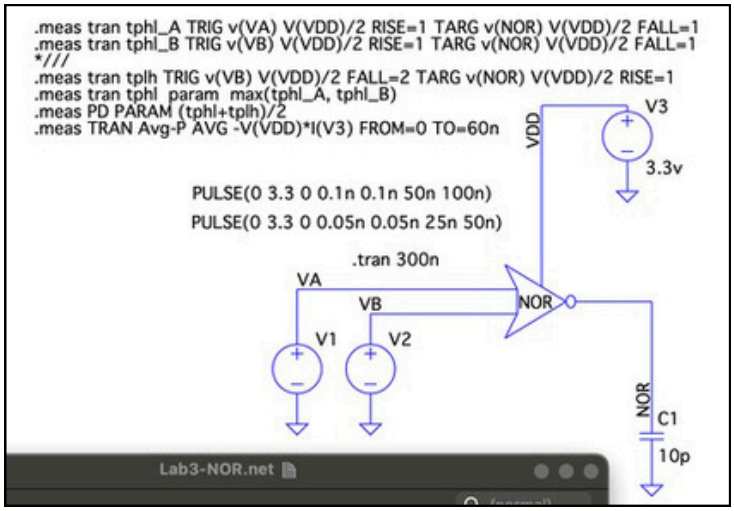
The transient analysis using two pulse inputs with tr and tf equal to 5% of the period. The output delay increased compared to faster rise/fall times (e.g., 0.1%) due to slower input transitions.

Task2 : NOR with tr = tf = 0.1% of T :

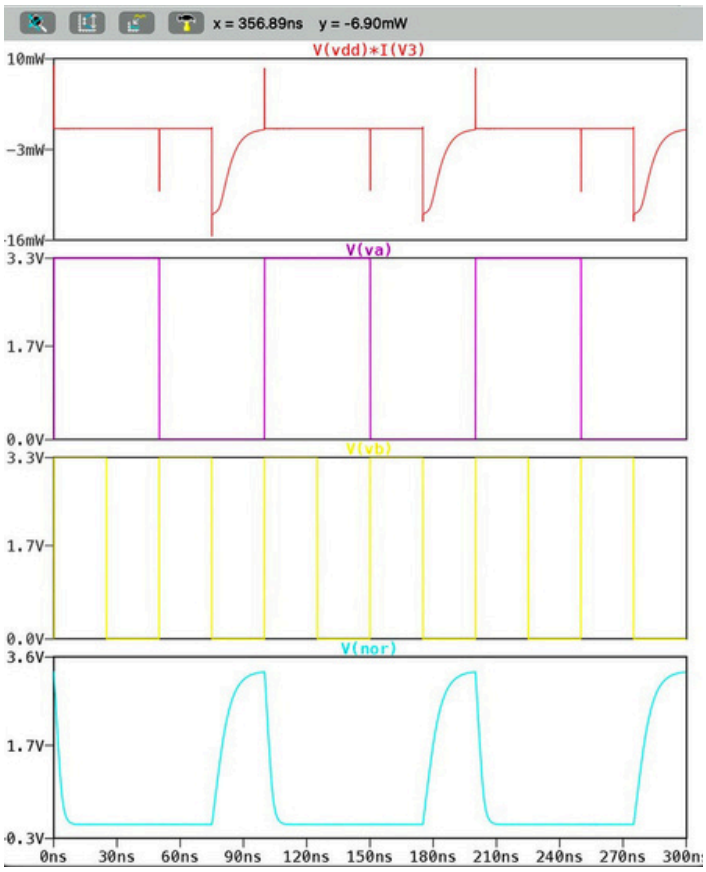
Netlist

```
* /Users/bushra/Desktop/LTspice/Lab3-NOR.asc
V1 VA 0 PULSE(0 3.3 0 0.1n 0.1n 50n 100n)
V2 VB 0 PULSE(0 3.3 0 0.05n 0.05n 25n 50n)
V3 VDD 0 3.3v
C1 NOR 0 10p
XNOR NOR VA VB VDD nor

* block symbol definitions
.subckt nor NOR VA VB VDD
M1 N002 VA VDD N001 PMOS l=350n w=30u
M2 NOR VB N002 N001 PMOS l=350n w=30u
M3 NOR VA 0 N003 NMOS l=350n w=8u
M4 NOR VB 0 N004 NMOS l=350n w=8u
.include tsmc350.txt
.ends nor

.model NMOS NMOS
.model PMOS PMOS
.lib /Users/bushra/Library/Application Support/LTspice/lib/cmp/standard.mos
.tran 300n
.meas tran tphl_A TRIG v(VA) V(VDD)/2 RISE=1 TARG v(NOR) V(VDD)/2 FALL=1
.meas tran tphl_B TRIG v(VB) V(VDD)/2 RISE=1 TARG v(NOR) V(VDD)/2 FALL=1
*///
.meas tran tplh TRIG v(VB) V(VDD)/2 FALL=2 TARG v(NOR) V(VDD)/2 RISE=1
.meas tran tphl  param  max(tphl_A, tphl_B)
.meas PD PARAM (tphl+tplh)/2
.meas TRAN Avg-P AVG -V(VDD)*I(V3) FROM=0 TO=60n
.backanno
.end
```

schematic



WAVEFORM



observations:

The output delay decreased

SPICE Output Log

```
Lab3-NOR.log
Search
tphl_a=2.19933e-09 FROM 5e-11 TO 2.24933e-09
tphl_b=2.22433e-09 FROM 2.5e-11 TO 2.24933e-09
tplh=4.71436e-09 FROM 7.5075e-08 TO 7.97894e-08
tphl: max(tphl_a, tphl_b)=2.22433e-09
pd: (tphl+tplh)/2=3.46935e-09
avg-p: AVG(-v(vdd)*i(v3))=-9.2264e-07 FROM 0 TO 6e-08

Total elapsed time: 0.086 seconds.
```