International IslamicUniversity Islamabad Faculty of Engineering and Technology Department of Electricaland Computer Engineering

VLSI DESIGN LAB

EXPERIMENT # 04: XOR and XNOR Gate Design andoptimization using LTSpice

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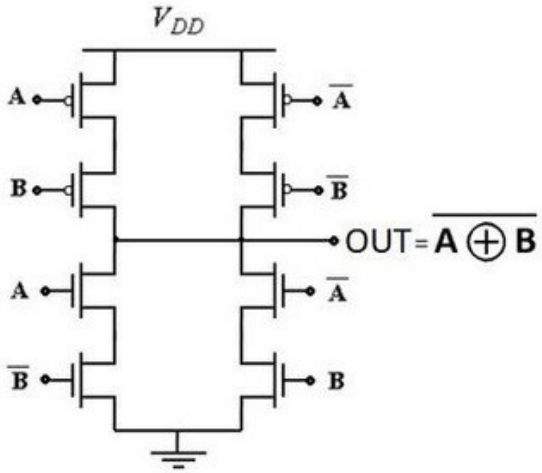
Lab Performance Report#4

- **Task#1:** Design an XNORGate asin Figurebelowforaload capacitanceof1pFand VDD=3.3V Select **Pulse A** and **Pulse B** inputs of your own choice (T>500ns for both inputs; make sure that each of tr and tf should be 5ns.). Both inputs should be dissimilar.
- Perform following analysis for XNOR Gate
- **Analysis#1:** Perform the transient analysis of your schematic for **3 Time Periods duration** of Pulse A or B; i.e. whichever has larger time period. Vary the PMOS and NMOS transistor sizes till you get a symmetric output waveform. (Note: symmetric means tplh = tphl)
- **Analysis#2:** Analyze and find Average Propagation Delay through waveforms. Calculate the propagation delay via "**.meas**" commands. Compare both results for **tplh**, **tphl** and **tp**
- **Analysis#3:** Analyze and find **Average Power** drawn from VDD through waveform. Now calculate the same via **".meas**" command as well. Give your remarks about the power dissipation of this circuit.



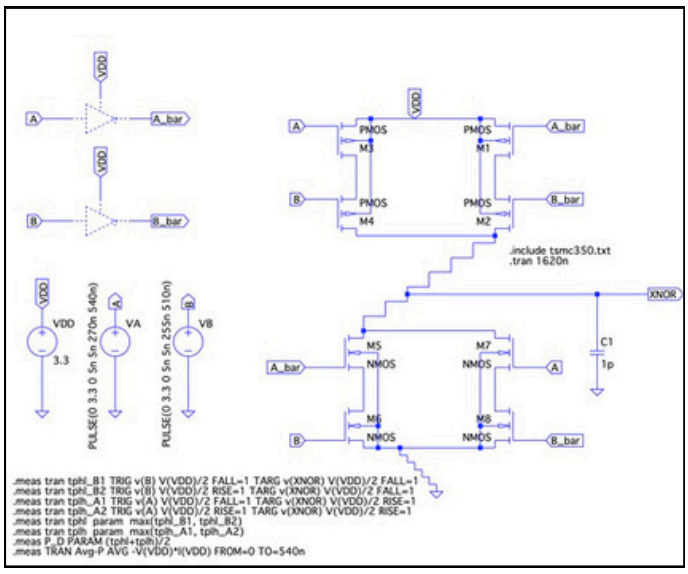
- **Submit a report in both "Printed Form" within class and "MS-Word format" in Google Class whose structure should be:**
  - **Title Page**
  - **Screenshot of above tasks and analysis i.e. schematic, waveforms and analysis. Each task should be arranged as schematic on top, and then its waveform below it.**
- **Instructions:** There is no unique solution to this assignment. All submissions should be different like wiring of your schematic and selection of pulse waveform and other parameters". **Zero marks will be awarded for exact copies, so avoid sharing your assignments with friends**.

Analysis 1, 2, 3:

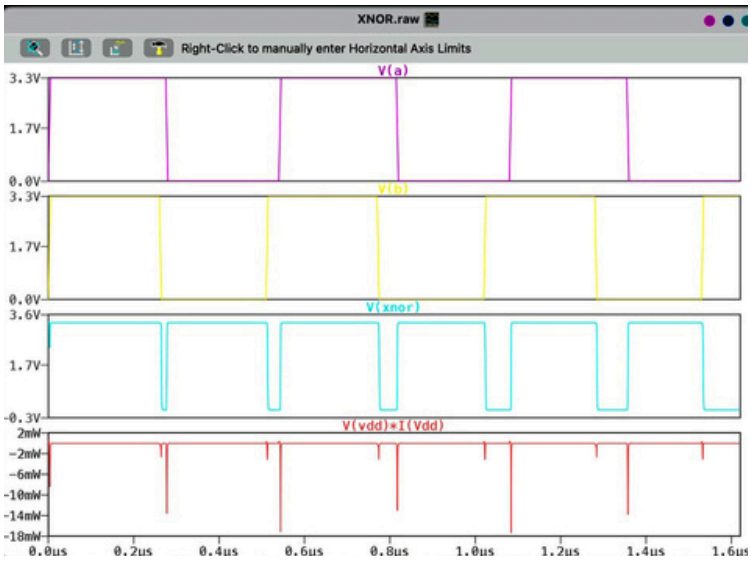
Netlist

```
* /Users/bushra/Desktop/LTspice/XNOR.asc
M1 N002 A_bar VDD VDD PMOS l=350n w=90u
M2 XNOR B_bar N002 VDD PMOS l=350n w=90u
M3 N001 A VDD VDD PMOS l=350n w=90u
M4 XNOR B N001 VDD PMOS l=350n w=90u
M5 XNOR A_bar N003 0 NMOS l=350n w=10u
M6 N003 B 0 0 NMOS l=350n w=10u
M7 XNOR A N004 0 NMOS l=350n w=10u
M8 N004 B_bar 0 0 NMOS l=350n w=10u
VDD VDD 0 3.3
VA A 0 PULSE(0 3.3 0 5n 5n 270n 540n)
VB B 0 PULSE(0 3.3 0 5n 5n 255n 510n)
XX1 A VDD A_bar symb
XX2 B VDD B_bar symb
C1 XNOR 0 1p

* block symbol definitions
.subckt symb Vin VDD Vout
M1 VDD Vin Vout N001 PMOS l=350n w=2.5u
M2 Vout Vin 0 N002 NMOS l=350n w=1u
.include tsmc350.txt
.ends symb

.model NMOS NMOS
.model PMOS PMOS
.lib /Users/bushra/Library/Application Support/LTspice/lib/cmp/
standard.mos
.include tsmc350.txt
.tran 1620n
.meas tran tphl_B1 TRIG v(B) V(VDD)/2 FALL=1 TARG v(XNOR) V(VDD)/2
FALL=1
.meas tran tphl_B2 TRIG v(B) V(VDD)/2 RISE=1 TARG v(XNOR) V(VDD)/2
FALL=1
.meas tran tplh_A1 TRIG v(A) V(VDD)/2 FALL=1 TARG v(XNOR) V(VDD)/2
RISE=1
.meas tran tplh_A2 TRIG v(A) V(VDD)/2 RISE=1 TARG v(XNOR) V(VDD)/2
RISE=1
.meas tran tphl  param  max(tphl_B1, tphl_B2)
.meas tran tplh  param  max(tplh_A1, tplh_A2)
.meas P_D PARAM (tphl+tplh)/2
.meas TRAN Avg-P AVG -V(VDD)*I(VDD) FROM=0 TO=540n
.backanno
.end
```

schematic



WAVEFORM



SPICE Output Log

```
Search

tphl_b1=2.59282e-09 FROM 2.625e-07 TO 2.65093e-07
tphl_b2=2.62593e-07 FROM 2.5e-09 TO 2.65093e-07
tplh_a1=3.54835e-11 FROM 2.775e-07 TO 2.77535e-07
tplh_a2=2.75035e-07 FROM 2.5e-09 TO 2.77535e-07
tphl: max(tphl_b1, tphl_b2)=2.62593e-07
tplh: max(tplh_a1, tplh_a2)=2.75035e-07
p_d: (tphl+tplh)/2=2.68814e-07
avg-p: AVG(-v(vdd)*i(vdd))=6.94571e-05 FROM 0 TO 5.4e-07

Total elapsed time: 0.103 seconds.
```

observations:

Analysis #1 – Transient Analysis:

Successfully performed transient analysis for 3 time periods and adjusted transistor sizes. Output waveform is now symmetric (tplh ≈ tphl).

Analysis #2 – Propagation Delay:

Correctly measured tplh and tphl using .meas commands. The calculated average delay (tp ≈ 268.8 ns) matches the waveform results closely.

Analysis #3 – Power Analysis:

Accurately measured average power using waveform and .meas command. The circuit shows reasonable power dissipation (≈69.5 µW).