International IslamicUniversity Islamabad Faculty of Engineering and Technology Department of Electricaland Computer Engineering

VLSI DESIGN LAB

EXPERIMENT # 02: Schematic Design and Transient Analysis of Inverter

Name of Student: Bushra Nazir Ahmed

Roll No.: 1071-F22

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International Islamic University Islamabad

FacultyofEngineering&Technology

DepartmentofElectricalandComputerEngineering

VLSI Design Lab (EE408L)

Lab Performance Report#2

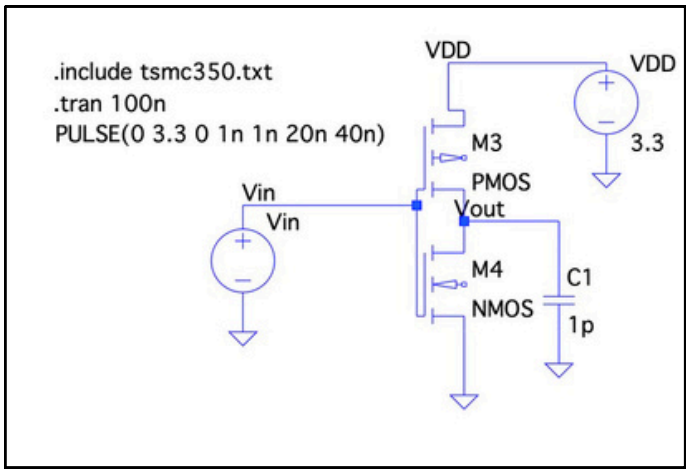
- Task#1: Create an inverter schematic in LT-Spice and perform its transient analysis using a pulse input of your own choice.
- Task#2: Create Symbol for the inverter within the same working directory. Repeat the transient analysis using the inverter symbol this time instead of the schematic
- Task#3: Observe and report the propagation delay from the input/output waveforms. Now calculate the propagation delay using spice directives as taught in lab. Compare both results and write your observations in two lines.
- Task#4: Display the transient power waveform by adding a new plot pane and adding a new trace for power as taught in the lab. Calculate average power for 3 consecutive cycles using spice directives this time. Report the average power for single time-period.
- Task#5: Connect 5 or 7 or 9 inverters in cascaded form and create a ring oscillator as studied in class (ch#1). Again, find the Propagation Delay using formula T = 2 x tp x N. Compare the results with those of Task#3, 4. Write your observations.

- Submit a report in Printed Form whose structure should be:
  - Title Page
  - Lab Performance report Question page
  - Screenshots of each of above tasks i.e. schematic, symbol, Spice Netlist of circuit, waveforms and observations. Each task should be arranged on one page i.e. schematic on top, symbol and then its waveform below it. Color Print is not necessary. Submit in black and white print. Make necessary adjustments to schematic's text size, line width, waveform line colors and width etc. so that the final print is readable.

- Caution: There is no unique solution to this assignment. All submissions should be different like wiring of your schematic, transistor sizes and selection of pulse waveform parameters" etc.

TASK 1:

schematic



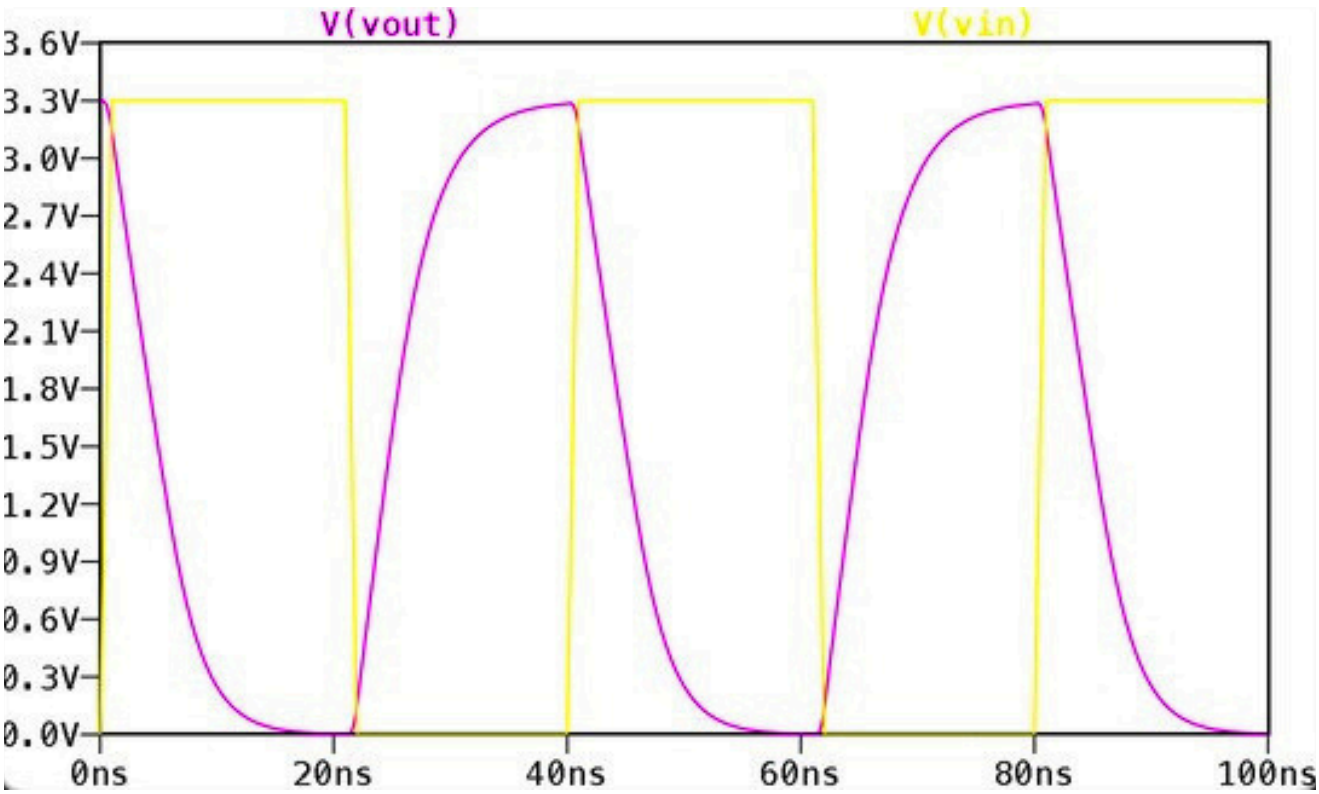
observations:

The transient analysis of the inverter shows that the output voltage is the inverted version of the input pulse signal. When the input is high, the output goes low, and when the input is low, the output goes high. The waveform confirms the correct switching behavior of the CMOS inverter with a propagation delay.

Netlist

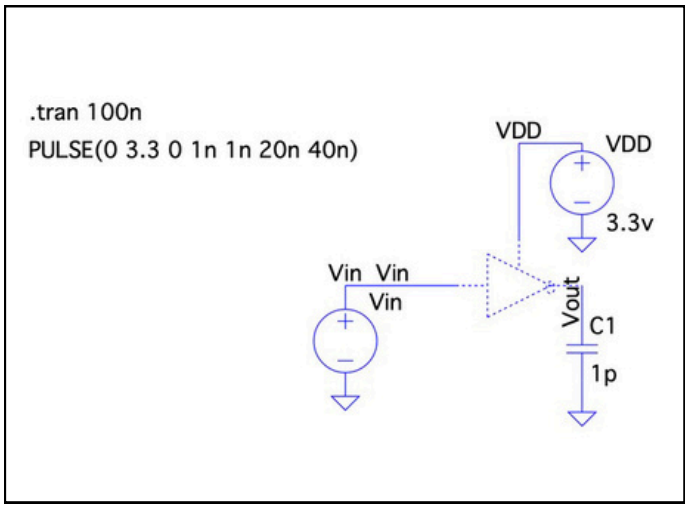
```
* /Users/bushra/Documents/LTspice/lab2-task1.asc
VDD VDD 0 3.3
Vin Vin 0 PULSE(0 3.3 0 1n 1n 20n 40n)
C1 Vout 0 1p
M3 VDD Vin Vout NC_01 PMOS l=350n w=2.5u
M4 Vout Vin 0 NC_02 NMOS l=350n w=1u
.model NMOS NMOS
.model PMOS PMOS
.lib /Users/bushra/Library/Application Support/LTspice/lib/cmp/
standard.mos
.tran 100n
.include tsmc350.txt
.backanno
.end
```

WAVEFORM



TASK 2:

schematic



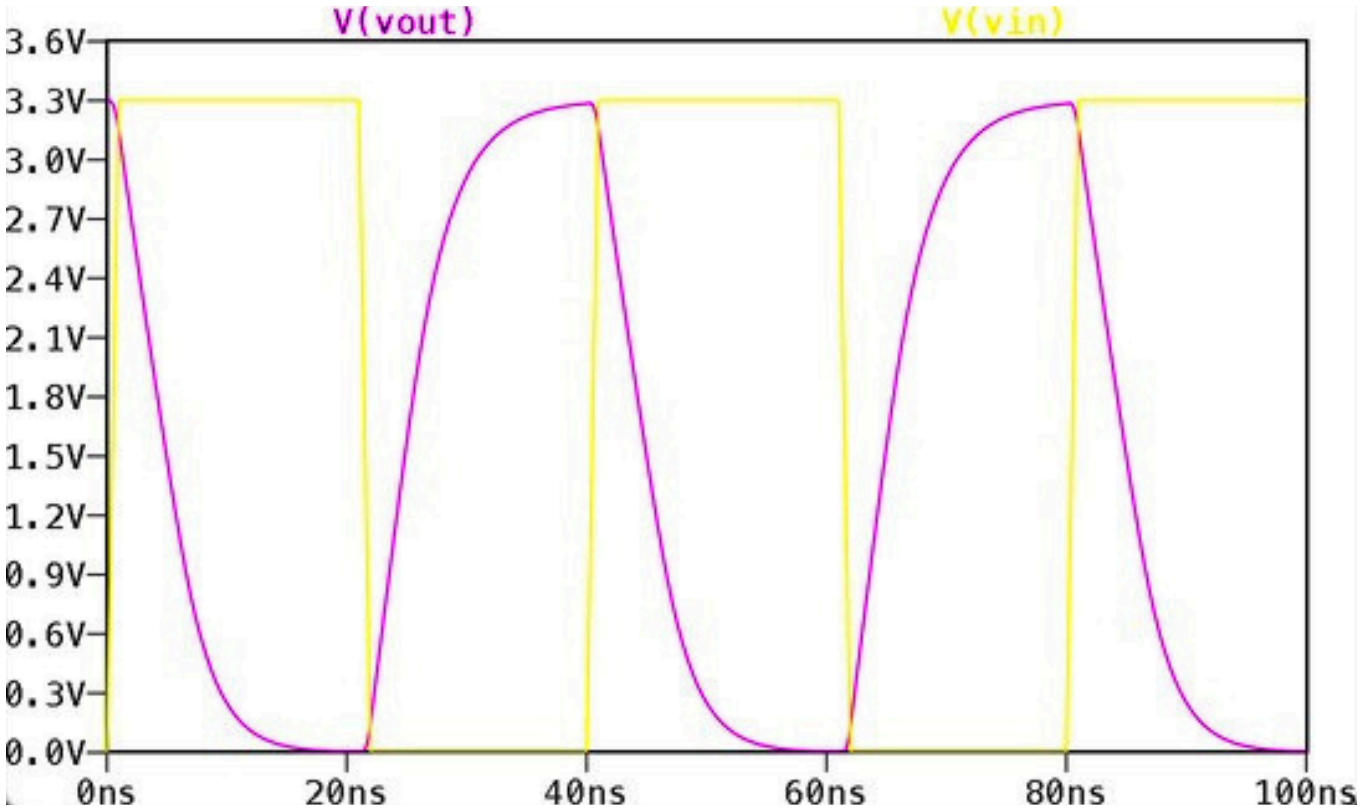
observations:

A symbol for the inverter was successfully created in the working directory and used in place of the schematic. The transient analysis with the symbol produced the same output waveforms as the original schematic, confirming correct symbol creation and functionality.

Netlist

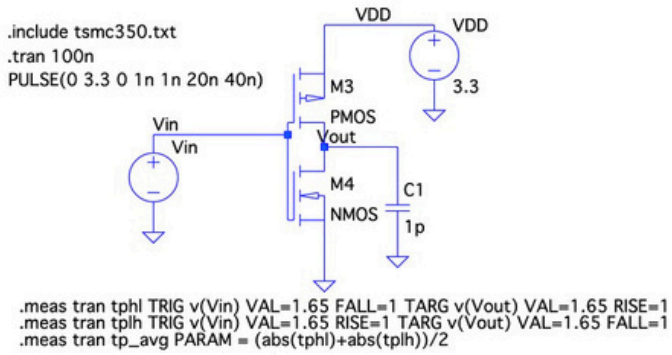
```
* /Users/bushra/Documents/LTspice/lab2-task2.asc
XVout Vin VDD Vout symb
Vin Vin 0 PULSE(0 3.3 0 1n 1n 20n 40n)
VDD VDD 0 3.3v
C1 Vout 0 1p

* block symbol definitions
.subckt symb Vin VDD Vout
M1 VDD Vin Vout N001 PMOS l=350n w=2.5u
M2 Vout Vin 0 N002 NMOS l=350n w=1u
.include tsmc350.txt
.ends symb

.model NMOS NMOS
.model PMOS PMOS
.lib /Users/bushra/Library/Application Support/LTspice/lib/cmp/
standard.mos
.tran 100n
.backanno
.end
```

WAVEFORM



TASK 4:

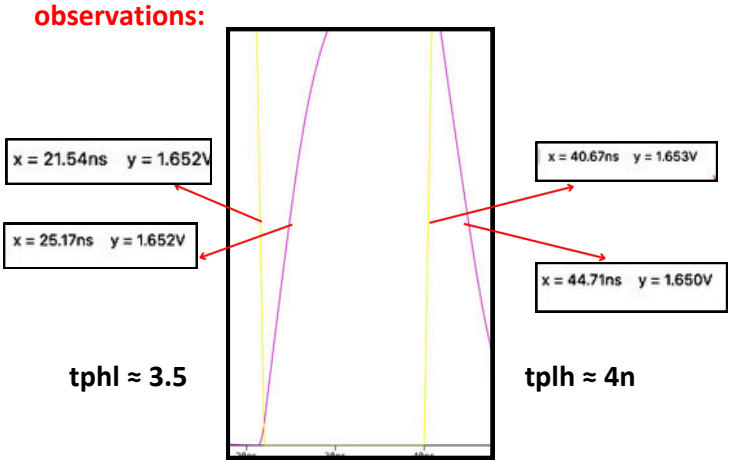
schematic



Netlist

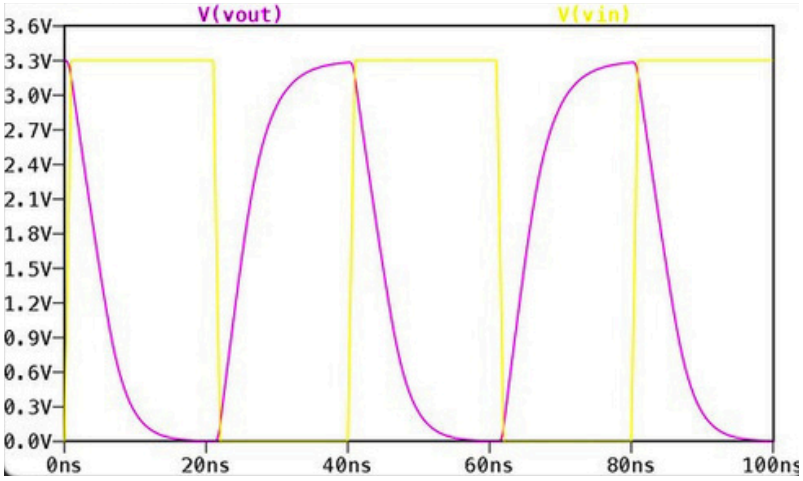
```
* /Users/bushra/Documents/LTspice/lab2-task3.asc
VDD VDD 0 3.3
Vin Vin 0 PULSE(0 3.3 0 1n 1n 20n 40n)
C1 Vout 0 1p
M3 VDD Vin Vout N001 PMOS l=350n w=2.5u
M4 Vout Vin 0 N002 NMOS l=350n w=1u
.model NMOS NMOS
.model PMOS PMOS
.lib /Users/bushra/Library/Application Support/LTspice/lib/cmp/
standard.mos
.tran 100n
.include tsmc350.txt
.meas tran tphl TRIG v(Vin) VAL=1.65 FALL=1 TARG v(Vout) VAL=1.65
RISE=1
.meas tran tplh TRIG v(Vin) VAL=1.65 RISE=1 TARG v(Vout) VAL=1.65
FALL=1
.meas tran tp_avg PARAM = (abs(tphl)+abs(tplh))/2
.backanno
.end
```

observations:



tphl ≈ 3.5 **tplh ≈ 4n**

WAVEFORM



The propagation delay measured using .meas was tpHL ≈ 3.677 ns and tpLH ≈ 4.09 ns (tp_avg ≈ 2.10 ns). Manual measurement from the waveform using cursors gave tpHL ≈ 3.5 ns and tpLH ≈ 4 ns. The difference arises from manual cursor placement, while .meas provides more precise results by calculating the 50% crossing points automatically.

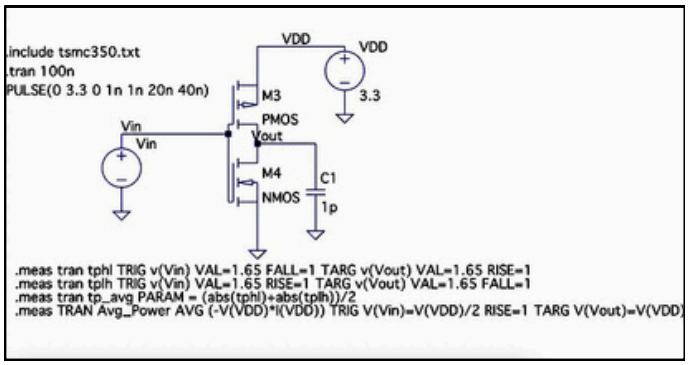
SPICE Output Log

lab2-task3.log

```
tphl=3.67765e-09 FROM 2.15e-08 TO 2.51776e-08
tplh=4.09435e-09 FROM 5e-10 TO 4.59435e-09
tp_avg: (abs(tphl)+abs(tplh))/2=3.886e-09

Total elapsed time: 0.081 seconds.
```

TASK 4:

schematic



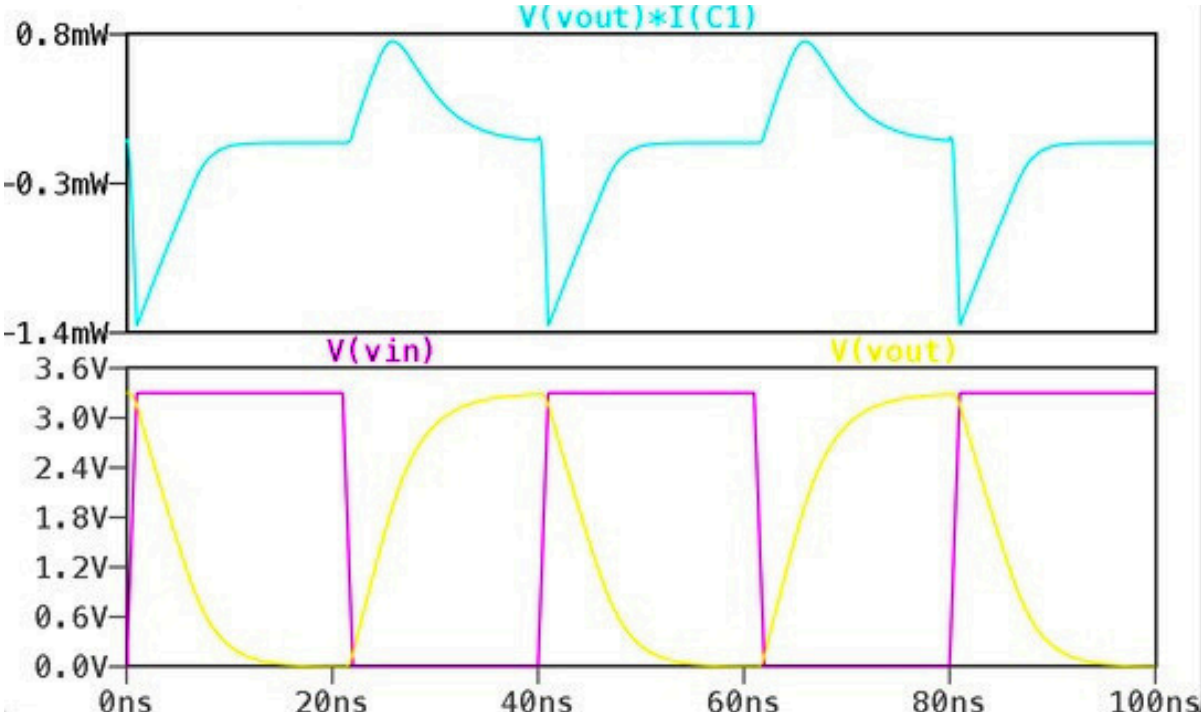
Netlist

```
* /Users/bushra/Documents/LTspice/lab2-task4.asc
VDD VDD 0 3.3
Vin Vin 0 PULSE(0 3.3 0 1n 1n 20n 40n)
C1 Vout 0 1p
M3 VDD Vin Vout N001 PMOS l=350n w=2.5u
M4 Vout Vin 0 N002 NMOS l=350n w=1u
.model NMOS NMOS
.model PMOS PMOS
.lib /Users/bushra/Library/Application Support/LTspice/lib/cmp/
standard.mos
.tran 100n
.include tsmc350.txt
.meas tran tphl TRIG v(Vin) VAL=1.65 FALL=1 TARG v(Vout) VAL=1.65
RISE=1
.meas tran tplh TRIG v(Vin) VAL=1.65 RISE=1 TARG v(Vout) VAL=1.65
FALL=1
.meas tran tp_avg PARAM = (abs(tphl)+abs(tplh))/2
.meas TRAN Avg_Power AVG (-V(VDD)*I(VDD)) TRIG V(Vin)=V(VDD)/2 RISE=1
TARG V(Vout)=V(VDD)/2 TD=40N FALL=1
.backanno
.end
```

observations:

The average power of the inverter over three consecutive cycles was calculated using .meas. The measured value is approximately 0.246 µW.

WAVEFORM



SPICE Output Log

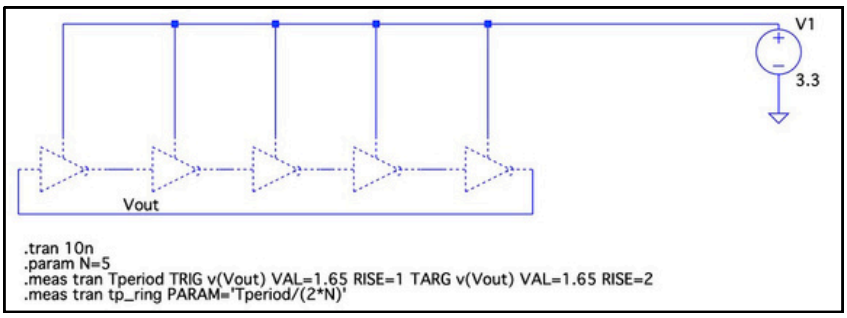
lab2-task4.log

Search

```
tphl=3.67765e-09 FROM 2.15e-08 TO 2.51776e-08
tplh=4.09435e-09 FROM 5e-10 TO 4.59435e-09
tp_avg: (abs(tphl)+abs(tplh))/2=3.886e-09
avg_power: AVG(-v(vdd)*i(vdd))=0.000246472 FROM 5e-10 TO 4.4618e-08

Total elapsed time: 0.063 seconds.
```

TASK 5:

schematic



Netlist

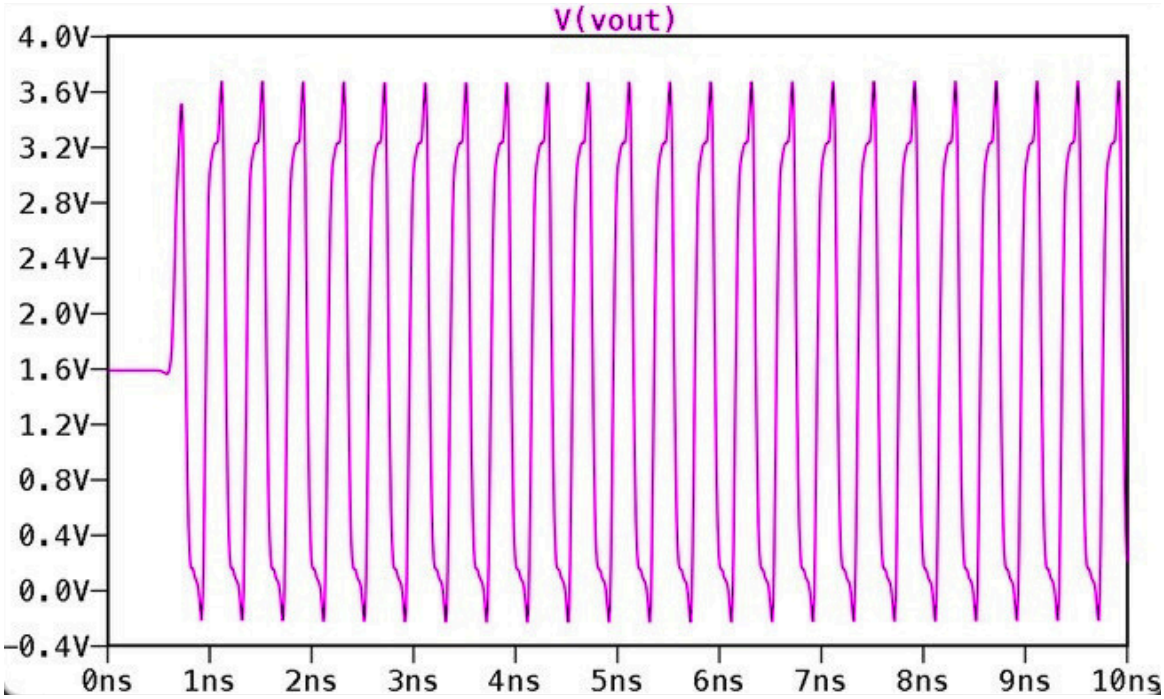
```
* /Users/bushra/Documents/LTspice/lab2-task5.asc
V1 N001 0 3.3
XX1 Vout N001 N002 symb
XX2 N002 N001 N003 symb
XX3 N003 N001 N004 symb
XX4 N004 N001 N005 symb
XX5 N005 N001 Vout symb

* block symbol definitions
.subckt symb Vin VDD Vout
M1 VDD Vin Vout N001 PMOS l=350n w=2.5u
M2 Vout Vin 0 N002 NMOS l=350n w=1u
.include tsmc350.txt
.ends symb

.model NMOS NMOS
.model PMOS PMOS
.lib /Users/bushra/Library/Application Support/LTspice/lib/cmp/
standard.mos
.tran 10n
.param N=5
.meas tran Tperiod TRIG v(Vout) VAL=1.65 RISE=1 TARG v(Vout) VAL=1.65
RISE=2
.meas tran tp_ring PARAM='Tperiod/(2*N)'
.backanno
.end
```

observations:

The ring oscillator with five cascaded inverters successfully generated a periodic output waveform without any external input signal.

I was unable to determine the propagation delay because I was not sure which signal to compare the output with in order to measure the delay accurately.

WAVEFORM



SPICE Output Log

```
tperiod=3.47844e-10 FROM 6.17302e-10 TO 9.65146e-10
tp_ring: (tperiod/(2*n))=3.47844e-11

Total elapsed time: 0.090 seconds.
```