International IslamicUniversity Islamabad Faculty of Engineering and Technology Department of Electricaland Computer Engineering

VLSI DESIGN LAB

EXPERIMENT Lab 13: XNOR GATE

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Date of Experiment: 18-dec-2025

Lab Performance Report#13

For a **2 inputXNORgate**(takeA, B,A', B' as separate inputs),presenttheTruth table and design schematics of static CMOS gates. Draw the logic graph and find common Euler Paths for pull- up and pull-down network. Sketch the corresponding stick diagram.

NOTES:

A. Draw static CMOS logic circuits that implement the given functions. For an N input gate, there should be 2N number of transistors in the circuits.

B. Draw Euler graphs for the circuits drawn in part A. Thus, derive Euler paths to determine the right input order and draw stick diagrams accordingly. **Note:** (Use multiple color markers for stick diagrams. For consistency, following color markers are recommended for all problems: **N+ active: green**, **P+ active: Brown**, **Poly: Red**, **Metal: Blue**, **VIA/ Contacts: Black**, **N-Well: Yellow**)

Task#1: **Pre-layout Simulation**:

- Design the gate schematic step by step in Electric. Perform transient analysis of
- using pulse inputs of your own choice in Electric and observe output in Ltspice

  Update the transistor widths till **tpHL = tpLH**
- Report the screenshots of schematic diagram, Spice netlist, I/O waveforms, log file
- and fill up the following table.

Sr#	Without Sizing		With Sizing	
	tpLH	**t^{pHL}**	**tpLH**	**t^{pHL}**
1.	2.6e-7	2.6e-7	2.6e-7	2.6e-7
2.	1.09e-8	7.5e-10	1.11e-8	6.1e-10

Task#2: **Post-layout Simulation**

- For the stick diagram drawn in, **design** the physical layout of the very gate in Electric.
- Perform the Design Rule Check (DRC) and **improve** your design till there are no errors or warnings.
- Perform the layout vs schematic analysis (NCC) in electric. Improve your design till the schematic of task#1 and the layout perfectly match.
- Perform transient analysis of the gate layout in Electric and observe output in Ltspice

- Observe and compare the results of pre-layout simulation with post layout simulation.
- Report the stick diagram, screenshots of layout diagram, Spice netlist, I/O waveforms, LTspice log file and your observations on how the post layout delays can be improved.
- Compare and improve your layout design to address any discrepancies in **tpHL,tpLH** values observed in pre-layout (with sizing) and post- layout design. Also comment on design improvement procedure implemented.

Sr#	Post-layout		Improved Design	
	tpLH	**tpHL**	**tpLH**	**t_{pHL}**
1.	——	——	2.7e-7	2.6e-7
2.	——	——	1.11e-8	2.7e-10

Comments:

schematic design, SPICE netlist extraction, and transient simulation, up to the physical layout design. A clean DRC was achieved with no errors or warnings, and NCC was performed successfully with a complete match between the schematic and the layout after multiple attempts and significant effort.

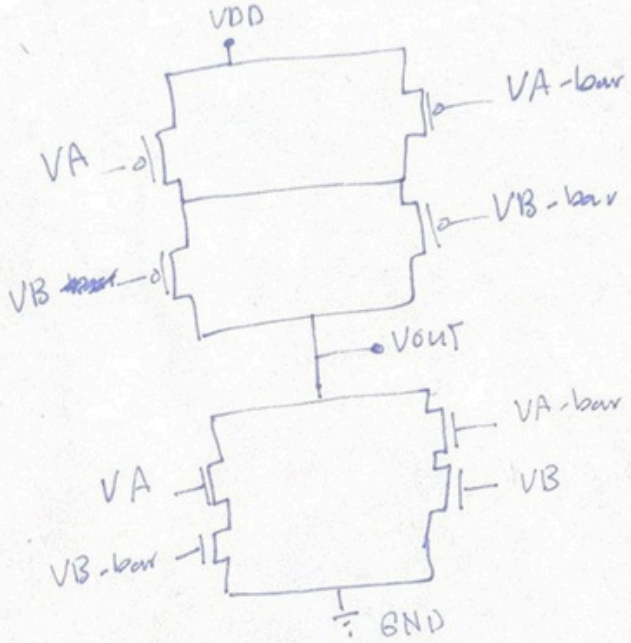
Despite repeated attempts to adjust the transistor sizing, this part of the experiment was very challenging, and an ideal equality between the propagation delay values could not be achieved. However, all other lab requirements were fully completed successfully.

Caution: There is no unique solution to this assignment. All submissions should be different, like size of transistors, wiring of your schematic and selection of circuit parameters, inputs and outputs. **Zero marks will be awarded for exact copies, so avoid sharing your assignments with friends**.

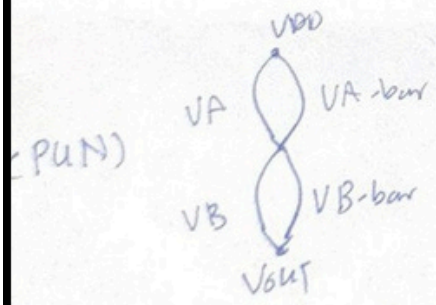
CMOS logic circuit , Euler graph, Euler paths , stick diagrams:

* 2- input XNOR :

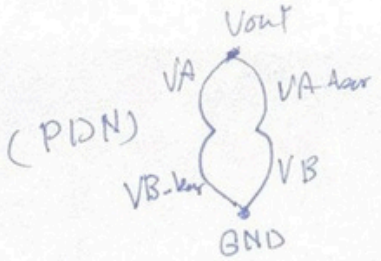
Vout = (VA . VB-bar + VA-bar . VB)



* Eular graph:

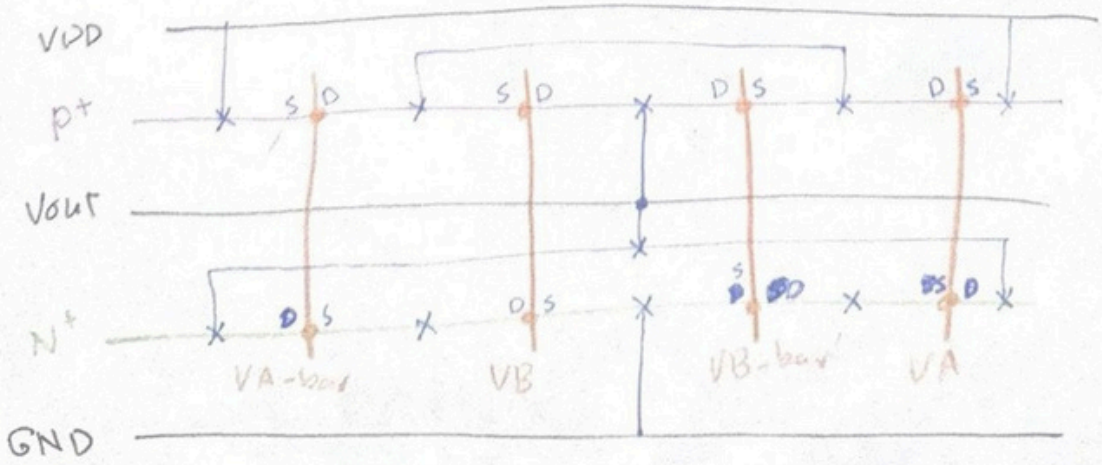


[VA-bar , VB , VB-bar , VA]



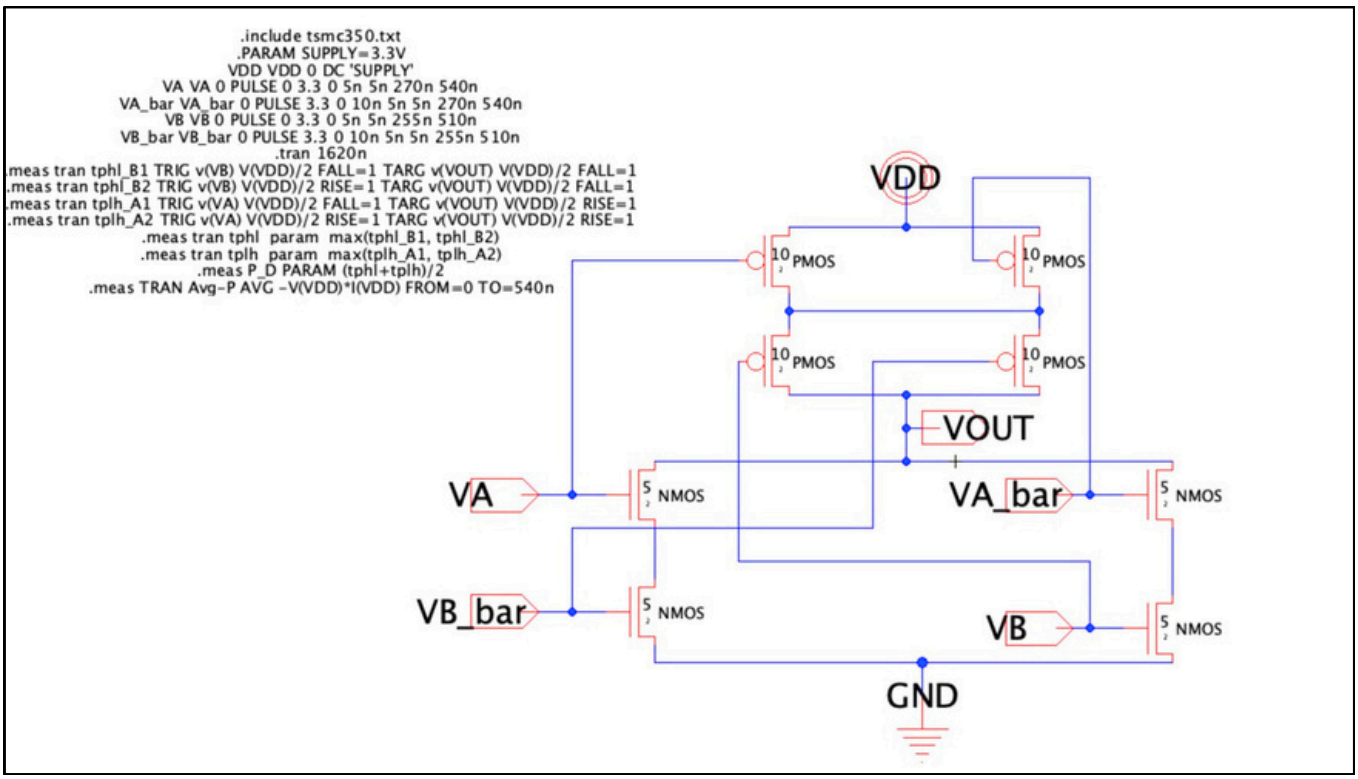
[VA-bar , VB , VB-bar , VA]

* Stick diagram:



Task 1 BEFORE SIZING :

schematic

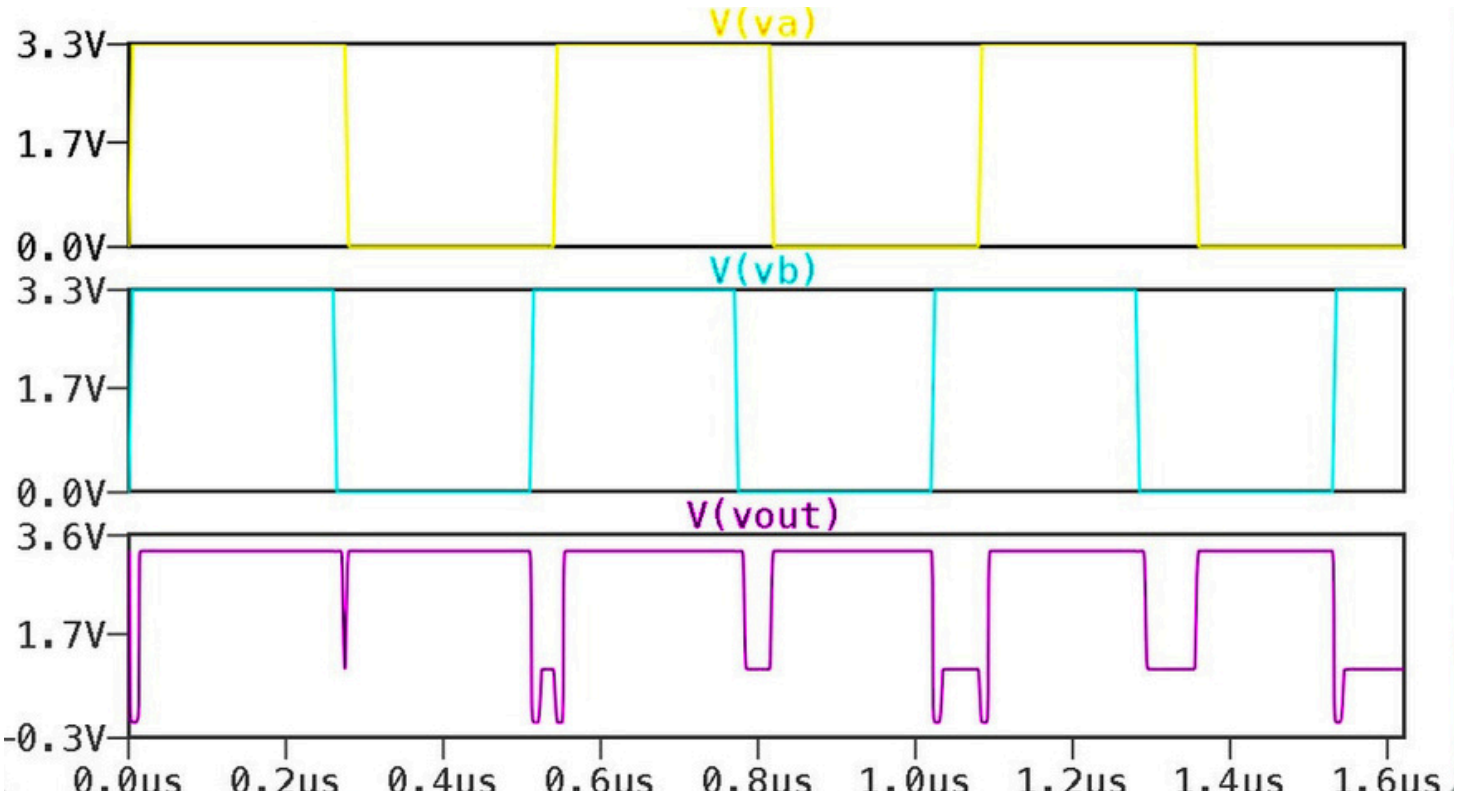


Netlist

```
*** SPICE deck for cell XNOR1{sch} from library XNOR1
*** Created on Ø³ Ø¯ÙØ³ 20, 2025 12:59:43
*** Last revised on Ø³ Ø¯ÙØ³ 20, 2025 19:14:09
*** Written on Ø³ Ø¯ÙØ³ 20, 2025 23:06:10 by Electric VLSI Design
System, version 9.07
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF
*** Lambda Conversion ***


.global gnd vdd

*** TOP LEVEL CELL: XNOR1{sch}
Mnmos@0 VOUT VA net@1 gnd NMOS L=0.35u W=875n
Mnmos@1 net@1 VB_bar gnd gnd NMOS L= 350n W= 875n
Mnmos@2 VOUT VA_bar net@4 gnd NMOS L= 350n W= 875n
Mnmos@3 net@4 VB gnd gnd NMOS L= 350n W= 875n
Mpmos@0 net@82 VB VOUT vdd PMOS L= 350n W=1750n
Mpmos@1 net@82 VB_bar VOUT vdd PMOS L= 350n W= 1750n
Mpmos@2 vdd VA net@82 vdd PMOS L= 350n W= 1750n
Mpmos@3 vdd VA_bar net@82 vdd PMOS L= 350n W= 1750n
```

```
* Spice Code nodes in cell cell 'XNOR1{sch}'
.include tsmc350.txt
.PARAM SUPPLY=3.3V
VDD VDD 0 DC 'SUPPLY'
VA VA 0 PULSE 0 3.3 0 5n 5n 270n 540n
VA_bar VA_bar 0 PULSE 3.3 0 10n 5n 5n 270n 540n
VB VB 0 PULSE 0 3.3 0 5n 5n 255n 510n
VB_bar VB_bar 0 PULSE 3.3 0 10n 5n 5n 255n 510n
.tran 1620n
.meas tran tphl_B1 TRIG v(VB) V(VDD)/2 FALL=1 TARG v(VOUT) V(VDD)/2
FALL=1
.meas tran tphl_B2 TRIG v(VB) V(VDD)/2 RISE=1 TARG v(VOUT) V(VDD)/2
FALL=1
.meas tran tplh_A1 TRIG v(VA) V(VDD)/2 FALL=1 TARG v(VOUT) V(VDD)/2
RISE=1
.meas tran tplh_A2 TRIG v(VA) V(VDD)/2 RISE=1 TARG v(VOUT) V(VDD)/2
RISE=1
.meas tran tphl  param  max(tphl_B1, tphl_B2)
.meas tran tplh  param  max(tplh_A1, tplh_A2)
.meas P_D PARAM (tphl+tplh)/2
.meas TRAN Avg-P AVG -V(VDD)*I(VDD) FROM=0 TO=540n
.END
```

WAVEFORM

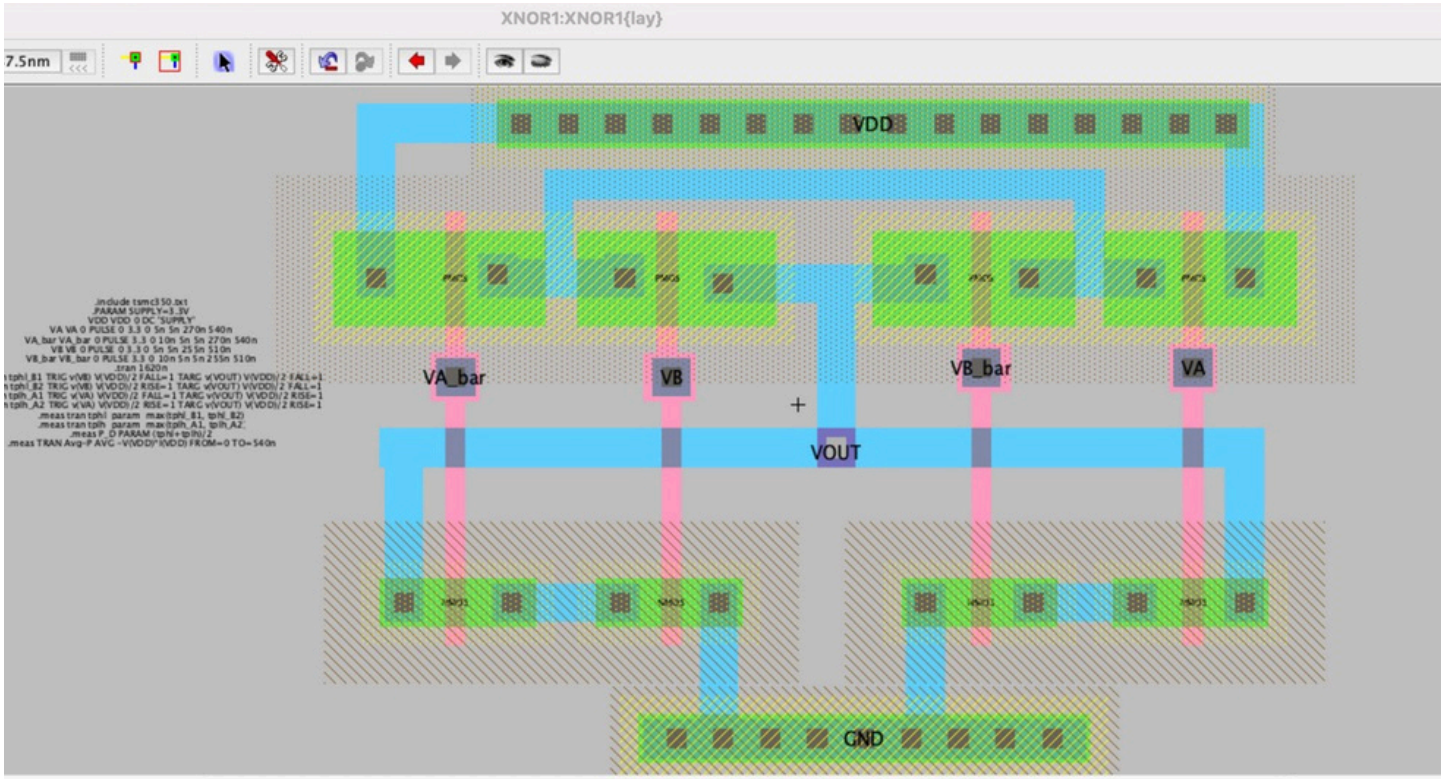


SPICE Output Log

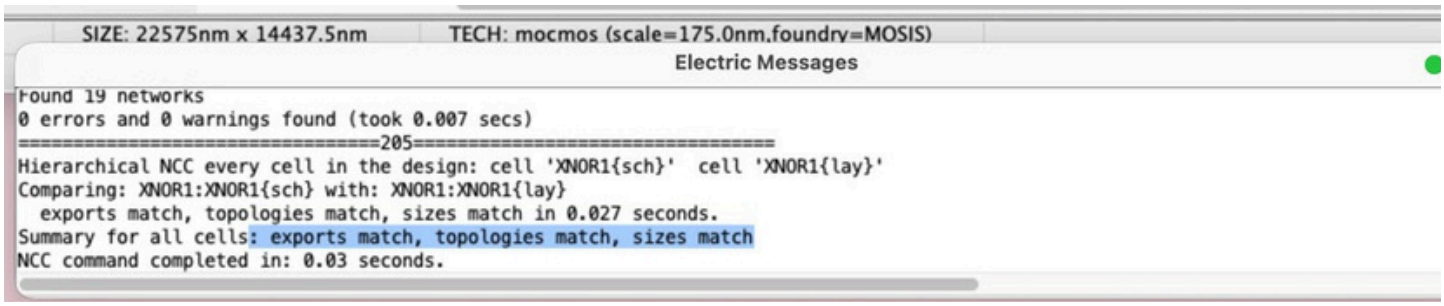
```
warning: Ps = 0 is less than W.
Direct Newton iteration for .op point succeeded.

tphl_b1=-2.60751e-07 FROM 2.625e-07 TO 1.74939e-09
tphl_b2=-7.50611e-10 FROM 2.5e-09 TO 1.74939e-09
tplh_a1=-2.64063e-07 FROM 2.775e-07 TO 1.34366e-08
tplh_a2=1.09366e-08 FROM 2.5e-09 TO 1.34366e-08
tphl: max(tphl_b1, tphl_b2)=-7.50611e-10
tplh: max(tplh_a1, tplh_a2)=1.09366e-08
p_d: (tphl+tplh)/2=5.09299e-09
avg-p: AVG(-v(vdd)*i(vdd))=2.31272e-05 FROM 0 TO 5.4e-07

Total elapsed time: 0.048 seconds.
```

Task 2 BEFORE SIZING :

LAYOUT



(DRC) , (NCC)



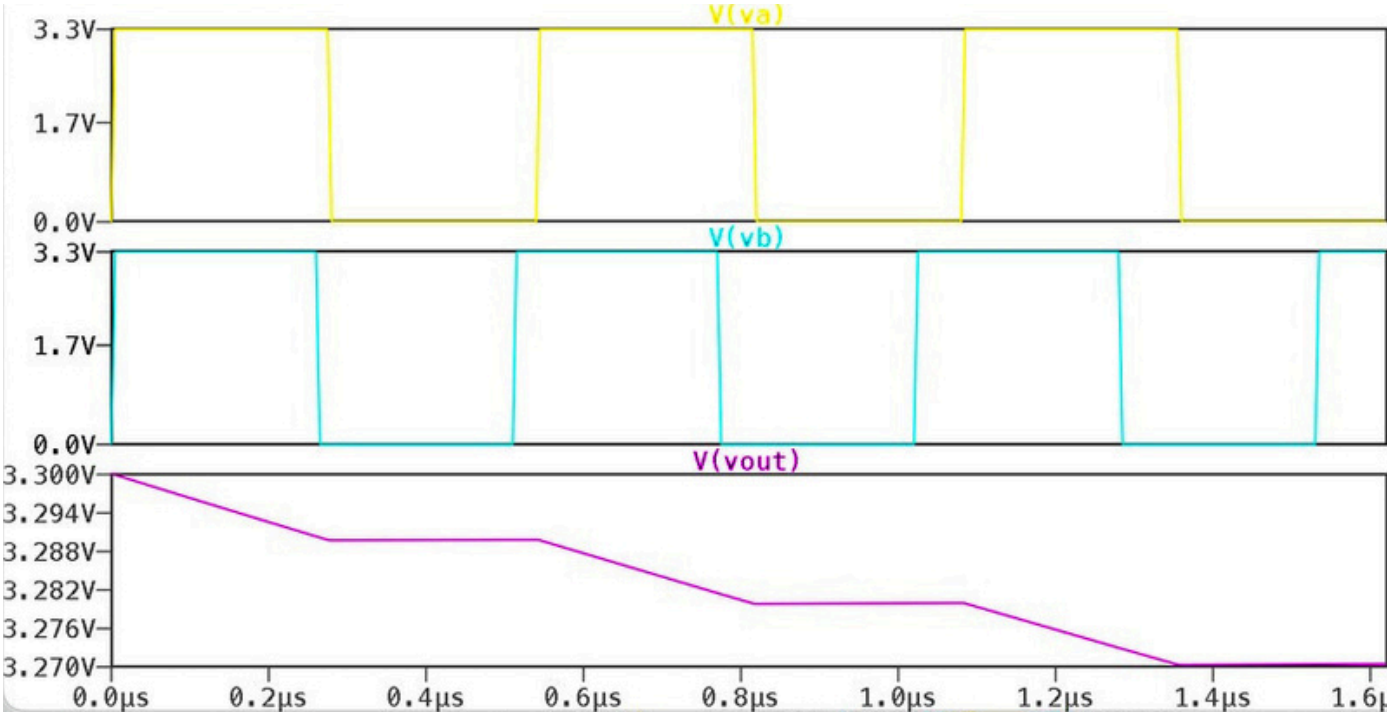
SPICE Output Log

```
Measurement "tphl_b1" FAIL'ed

Measurement "tphl_b2" FAIL'ed

Measurement "tplh_a1" FAIL'ed

Measurement "tplh_a2" FAIL'ed

Measurement "tphl" FAIL'ed

Measurement "tplh" FAIL'ed

Measurement "p_d" FAIL'ed
avg-p: AVG(-v(vdd)*i(vdd))=0.00044648 FROM 0 TO 5.4e-07

Total elapsed time: 0.071 seconds.
```

Netlist

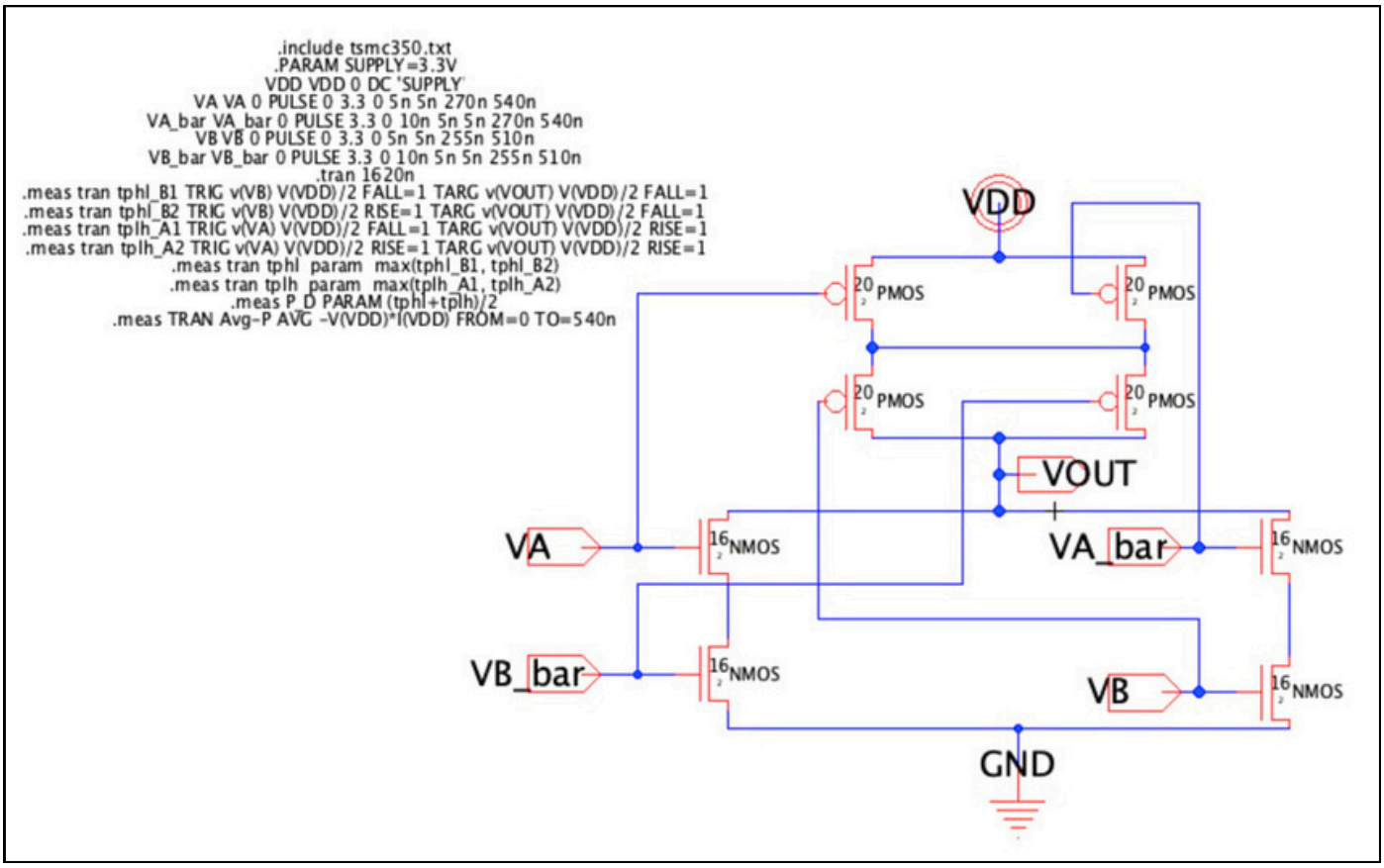
```
*** TOP LEVEL CELL: XNOR1{lay}
Mnmos@0 net@42 VA#0nmos@0_poly-left VOUT gnd NMOS L=0.35u W=0.875u
AS=2.488u AD=1.110u PS=6.081u PD=4.288u
Mnmos@1 gnd VB_bar#0nmos@1_poly-left net@42 gnd NMOS L=0.35u W=0.875u
AS=1.110u AD=4.747u PS=4.288u PD=13.475u
Mnmos@2 VOUT VA_bar#0nmos@2_poly-left net@38 gnd NMOS L=0.35u W=0.875u
AS=1.110u AD=2.488u PS=4.288u PD=6.081u
Mnmos@3 net@38 VB#0nmos@3_poly-left gnd gnd NMOS L=0.35u W=0.875u
AS=4.747u AD=1.110u PS=13.475u PD=4.288u
Mpmos@0 net@30 VB#2pmos@0_poly-right VOUT vdd PMOS L=0.35u W=1.75u
AS=2.488u AD=3.330u PS=6.081u PD=7.306u
Mpmos@1 VOUT VB_bar#2pmos@1_poly-right net@30 vdd PMOS L=0.35u W=1.75u
AS=3.330u AD=2.488u PS=7.306u PD=6.081u
Mpmos@2 net@30 VA#2pmos@2_poly-right vdd vdd PMOS L=0.35u W=1.75u
AS=10.181u AD=3.330u PS=23.012u PD=7.306u
Mpmos@3 vdd VA_bar#1pmos@3_poly-right net@30 vdd PMOS L=0.35u W=1.75u
AS=3.330u AD=10.181u PS=7.306u PD=23.012u

** Extracted Parasitic Capacitors ***
C0 VA_bar 0 0.109fF
C1 VB 0 0.131fF
C2 VB_bar 0 0.137fF
C3 VA 0 0.115fF
C4 net@30 0 5.276fF
C5 VOUT 0 8.793fF
C6 net@38 0 0.615fF
C7 net@42 0 0.588fF
** Extracted Parasitic Resistors ***
R0 VA_bar#0nmos@2_poly-left VA_bar#0nmos@2_poly-left##0 8.636
R1 VA_bar#0nmos@2_poly-left##0 VA_bar#0nmos@2_poly-left##1 8.636
R2 VA_bar#0nmos@2_poly-left##1 VA_bar#0nmos@2_poly-left##2 8.636
R3 VA_bar#0nmos@2_poly-left##2 VA_bar#0nmos@2_poly-left##3 8.636
R4 VA_bar#0nmos@2_poly-left##3 VA_bar#0nmos@2_poly-left##4 8.636
R5 VA_bar#0nmos@2_poly-left##4 VA_bar#0nmos@2_poly-left##5 8.636
R6 VA_bar#0nmos@2_poly-left##5 VA_bar 8.636
R7 VA_bar VA_bar##0 5.425
R8 VA_bar##0 VA_bar#1pmos@3_poly-right 5.425
R9 VB#0nmos@3_poly-left VB#0nmos@3_poly-left##0 8.636
R10 VB#0nmos@3_poly-left##0 VB#0nmos@3_poly-left##1 8.636
R11 VB#0nmos@3_poly-left##1 VB#0nmos@3_poly-left##2 8.636
R12 VB#0nmos@3_poly-left##2 VB#0nmos@3_poly-left##3 8.636
R13 VB#0nmos@3_poly-left##3 VB#0nmos@3_poly-left##4 8.636
R14 VB#0nmos@3_poly-left##4 VB#0nmos@3_poly-left##5 8.636
R15 VB#0nmos@3_poly-left##5 VB 8.636
R16 VB#2pmos@0_poly-right VB#2pmos@0_poly-right##0 5.425
R17 VB#2pmos@0_poly-right##0 VB 5.425
R18 VB_bar#2pmos@1_poly-right VB_bar 7.75
R19 VA#2pmos@2_poly-right VA 7.75
R20 VA#0nmos@0_poly-left VA#0nmos@0_poly-left##0 9.079
R21 VA#0nmos@0_poly-left##0 VA#0nmos@0_poly-left##1 9.079
R22 VA#0nmos@0_poly-left##1 VA#0nmos@0_poly-left##2 9.079
```

waveform



Task 1 AFTER SIZING :

schematic



SPICE Output Log

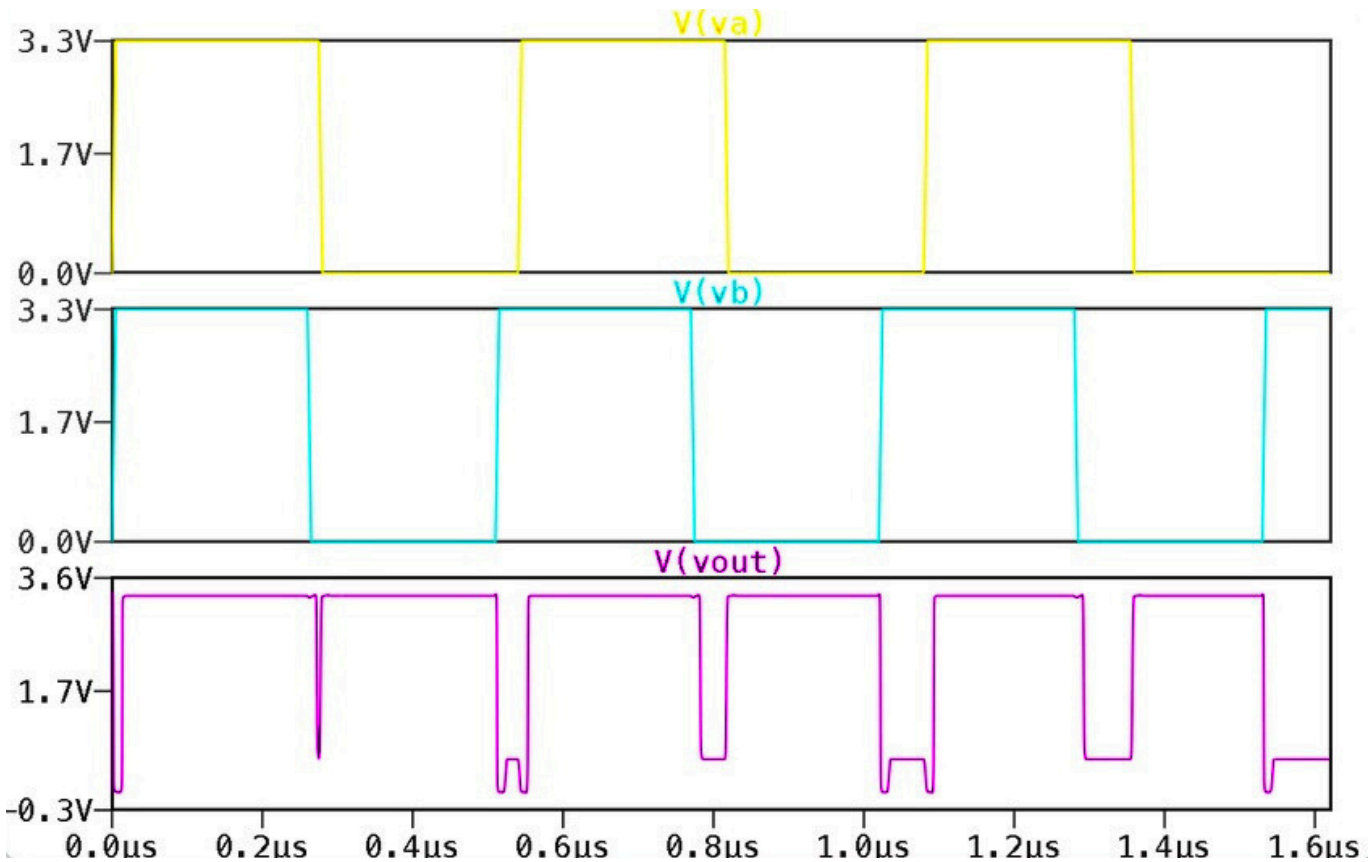
XNOR.log

```
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Direct Newton iteration for .op point succeeded.

tphl_b1=-2.60611e-07 FROM 2.625e-07 TO 1.88938e-09
tphl_b2=-6.10616e-10 FROM 2.5e-09 TO 1.88938e-09
tplh_a1=-2.63812e-07 FROM 2.775e-07 TO 1.36881e-08
tplh_a2=1.11881e-08 FROM 2.5e-09 TO 1.36881e-08
tphl: max(tphl_b1, tphl_b2)=-6.10616e-10
tplh: max(tplh_a1, tplh_a2)=1.11881e-08
p_d: (tphl+tplh)/2=5.28873e-09
avg-p: AVG(-v(vdd)*i(vdd))=3.16886e-05 FROM 0 TO 5.4e-07

Total elapsed time: 0.078 seconds.
```

Netlist

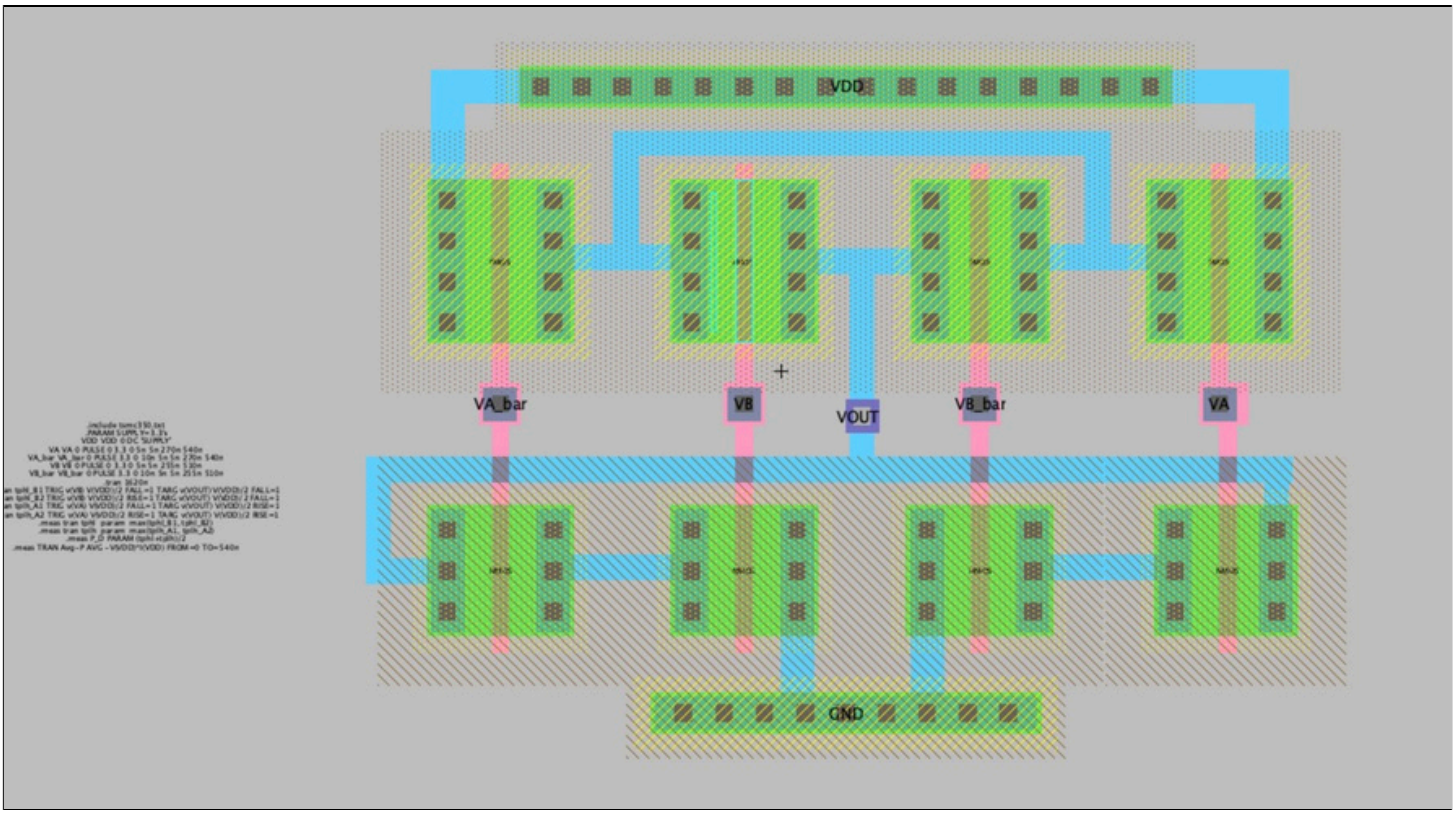
```
*** SPICE deck for cell XNOR{sch} from library XNOR
*** Created on Ø³ Ø¯ÙØ³ 20, 2025 12:59:43
*** Last revised on Ø³ Ø¯ÙØ³ 20, 2025 20:43:15
*** Written on Ø³ Ø¯ÙØ³ 20, 2025 21:39:35 by Electric VLSI Design
System, version 9.07
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF
*** Lambda Conversion ***


.global gnd vdd

*** TOP LEVEL CELL: XNOR{sch}
Mnmos@0 VOUT VA net@1 gnd NMOS L=0.7u W=2.8u
Mnmos@1 net@1 VB_bar gnd gnd NMOS L=0.7u W=2.8u
Mnmos@2 VOUT VA_bar net@4 gnd NMOS L=0.7u W=2.8u
Mnmos@3 net@4 VB gnd gnd NMOS L=0.7u W=2.8u
Mpmos@0 net@82 VB VOUT vdd PMOS L=0.7u W=3.5u
Mpmos@1 net@82 VB_bar VOUT vdd PMOS L=0.7u W=3.5u
Mpmos@2 vdd VA net@82 vdd PMOS L=0.7u W=3.5u
Mpmos@3 vdd VA_bar net@82 vdd PMOS L=0.7u W=3.5u

* Spice Code nodes in cell cell 'XNOR{sch}'
.include tsmc350.txt
.PARAM SUPPLY=3.3V
VDD VDD 0 DC 'SUPPLY'
VA VA 0 PULSE 0 3.3 0 5n 5n 270n 540n
VA_bar VA_bar 0 PULSE 3.3 0 10n 5n 5n 270n 540n
VB VB 0 PULSE 0 3.3 0 5n 5n 255n 510n
VB_bar VB_bar 0 PULSE 3.3 0 10n 5n 5n 255n 510n
.tran 1620n
.meas tran tphl_B1 TRIG v(VB) V(VDD)/2 FALL=1 TARG v(VOUT) V(VDD)/2
FALL=1
.meas tran tphl_B2 TRIG v(VB) V(VDD)/2 RISE=1 TARG v(VOUT) V(VDD)/2
FALL=1
.meas tran tplh_A1 TRIG v(VA) V(VDD)/2 FALL=1 TARG v(VOUT) V(VDD)/2
RISE=1
.meas tran tplh_A2 TRIG v(VA) V(VDD)/2 RISE=1 TARG v(VOUT) V(VDD)/2
RISE=1
.meas tran tphl  param  max(tphl_B1, tphl_B2)
.meas tran tplh  param  max(tplh_A1, tplh_A2)
.meas P_D PARAM (tphl+tplh)/2
.meas TRAN Avg-P AVG -V(VDD)*I(VDD) FROM=0 TO=540n
.END
```

waveform



Task 2 AFTER SIZING :

LAYOUT



(DRC) , (NCC)

```
SIZE: 26250nm x 16450nm        TECH: mocmos (scale=175.0nm,foundry=MOSIS)

                                                    Electric Messages
Found 19 networks
0 errors and 0 warnings found (took 0.038 secs)
==================================202==================================
Hierarchical NCC every cell in the design: cell 'XNOR:XNOR{sch}'  cell 'XNOR:XNOR{lay}'
Comparing: XNOR:XNOR{sch} with: XNOR:XNOR{lay}
  exports match, topologies match, sizes match in 0.029 seconds.
Summary for all cells: exports match, topologies match, sizes match
NCC command completed in: 0.037 seconds.
```

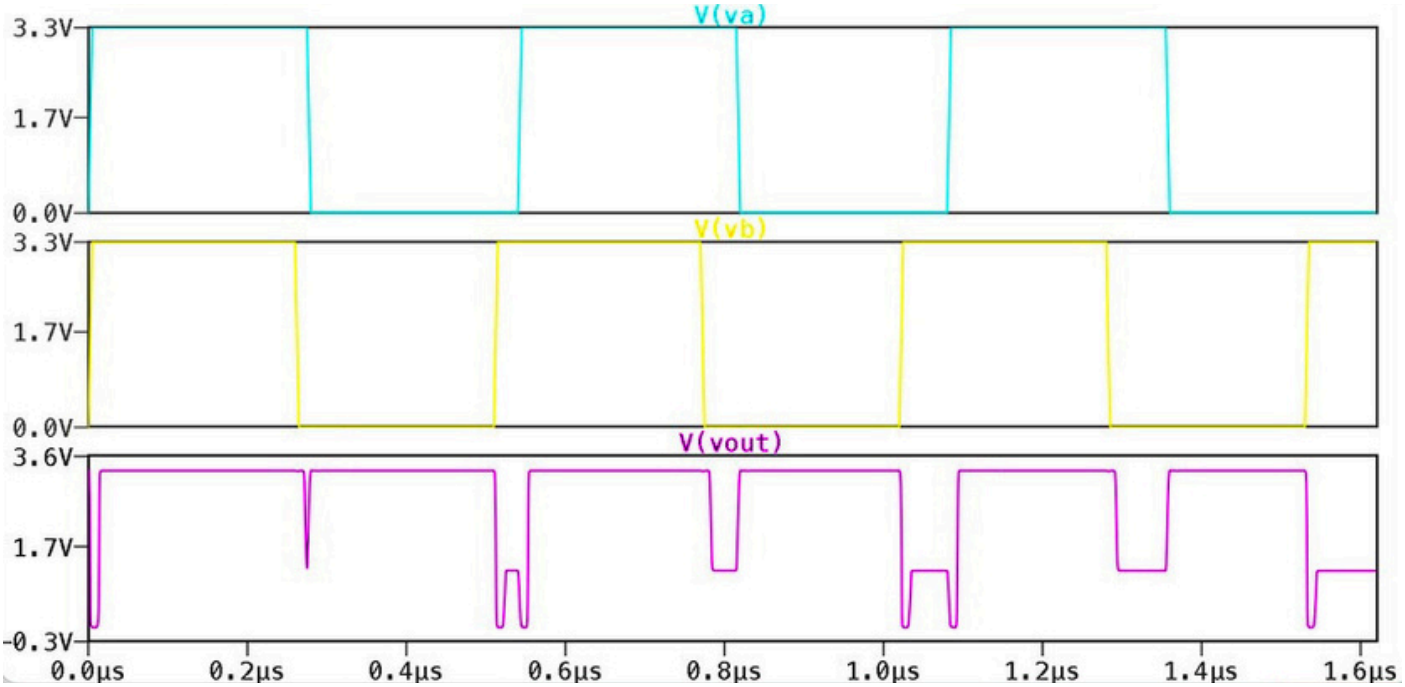
SPICE Output Log

```
WARNING: Less than two connections to node pmos@1_p-trans-well.  This node is used by mpmos@1.
WARNING: Less than two connections to node pmos@2_p-trans-well.  This node is used by mpmos@2.
WARNING: Less than two connections to node pmos@3_p-trans-well.  This node is used by mpmos@3.
Direct Newton iteration for .op point succeeded.

tphl_b1=-2.60277e-07 FROM 2.625e-07 TO 2.22254e-09
tphl_b2=-2.77457e-10 FROM 2.5e-09 TO 2.22254e-09
tplh_a1=-2.63831e-07 FROM 2.775e-07 TO 1.36687e-08
tplh_a2=1.11687e-08 FROM 2.5e-09 TO 1.36687e-08
tphl: max(tphl_b1, tphl_b2)=-2.77457e-10
tplh: max(tplh_a1, tplh_a2)=1.11687e-08
p_d: (tphl+tplh)/2=5.44564e-09
avg_p: AVG(-v(vdd)*i(vdd))=2.59356e-05 FROM 0 TO 5.4e-07

Total elapsed time: 0.073 seconds.
```

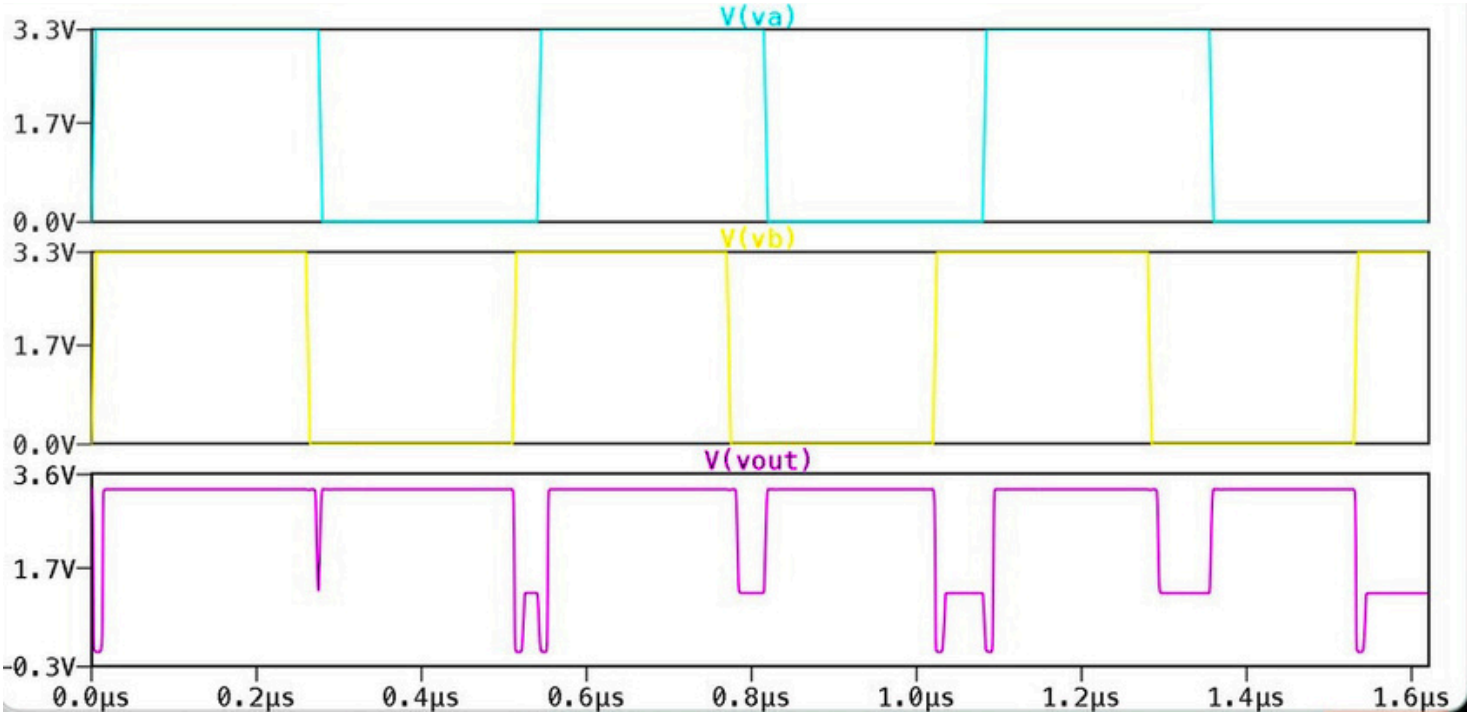
Netlist

```
R8 VA_bar##0 VA_bar#1pmos@3_poly-right 5.425
R9 VB#0nmos@3_poly-left VB#0nmos@3_poly-left##0 8.636
R10 VB#0nmos@3_poly-left##0 VB#0nmos@3_poly-left##1 8.636
R11 VB#0nmos@3_poly-left##1 VB#0nmos@3_poly-left##2 8.636
R12 VB#0nmos@3_poly-left##2 VB#0nmos@3_poly-left##3 8.636
R13 VB#0nmos@3_poly-left##3 VB#0nmos@3_poly-left##4 8.636
R14 VB#0nmos@3_poly-left##4 VB#0nmos@3_poly-left##5 8.636
R15 VB#0nmos@3_poly-left##5 VB 8.636
R16 VB#2pmos@0_poly-right VB#2pmos@0_poly-right##0 5.425
R17 VB#2pmos@0_poly-right##0 VB 5.425
R18 VB_bar#2pmos@1_poly-right VB_bar 7.75
R19 VA#2pmos@2_poly-right VA 7.75
R20 VA#0nmos@0_poly-left VA#0nmos@0_poly-left##0 9.079
R21 VA#0nmos@0_poly-left##0 VA#0nmos@0_poly-left##1 9.079
R22 VA#0nmos@0_poly-left##1 VA#0nmos@0_poly-left##2 9.079
R23 VA#0nmos@0_poly-left##2 VA#0nmos@0_poly-left##3 9.079
R24 VA#0nmos@0_poly-left##3 VA#0nmos@0_poly-left##4 9.079
R25 VA#0nmos@0_poly-left##4 VA#0nmos@0_poly-left##5 9.079
R26 VA#0nmos@0_poly-left##5 VA 9.079
R27 VB_bar#0nmos@1_poly-left VB_bar#0nmos@1_poly-left##0 9.079
R28 VB_bar#0nmos@1_poly-left##0 VB_bar#0nmos@1_poly-left##1 9.079
R29 VB_bar#0nmos@1_poly-left##1 VB_bar#0nmos@1_poly-left##2 9.079
R30 VB_bar#0nmos@1_poly-left##2 VB_bar#0nmos@1_poly-left##3 9.079
R31 VB_bar#0nmos@1_poly-left##3 VB_bar#0nmos@1_poly-left##4 9.079
R32 VB_bar#0nmos@1_poly-left##4 VB_bar#0nmos@1_poly-left##5 9.079
R33 VB_bar#0nmos@1_poly-left##5 VB_bar 9.079

* Spice Code nodes in cell cell 'XNOR{lay}'
.include tsmc350.txt
.PARAM SUPPLY=3.3V
VDD VDD 0 DC 'SUPPLY'
VA VA 0 PULSE 0 3.3 0 5n 5n 270n 540n
VA_bar VA_bar 0 PULSE 3.3 0 10n 5n 5n 270n 540n
VB VB 0 PULSE 0 3.3 0 5n 5n 255n 510n
VB_bar VB_bar 0 PULSE 3.3 0 10n 5n 5n 255n 510n
.tran 1620n
.meas tran tphl_B1 TRIG v(VB) V(VDD)/2 FALL=1 TARG v(VOUT) V(VDD)/2
FALL=1
.meas tran tphl_B2 TRIG v(VB) V(VDD)/2 RISE=1 TARG v(VOUT) V(VDD)/2
FALL=1
.meas tran tplh_A1 TRIG v(VA) V(VDD)/2 FALL=1 TARG v(VOUT) V(VDD)/2
RISE=1
.meas tran tplh_A2 TRIG v(VA) V(VDD)/2 RISE=1 TARG v(VOUT) V(VDD)/2
RISE=1
.meas tran tphl  param  max(tphl_B1, tphl_B2)
.meas tran tplh  param  max(tplh_A1, tplh_A2)
.meas P_D PARAM (tphl+tplh)/2
.meas TRAN Avg_P AVG -V(VDD)*I(VDD) FROM=0 TO=540n
.END
```

waveform



Netlist

```
R8 VA_bar##0 VA_bar#1pmos@3_poly-right 5.425
R9 VB#0nmos@3_poly-left VB#0nmos@3_poly-left##0 8.636
R10 VB#0nmos@3_poly-left##0 VB#0nmos@3_poly-left##1 8.636
R11 VB#0nmos@3_poly-left##1 VB#0nmos@3_poly-left##2 8.636
R12 VB#0nmos@3_poly-left##2 VB#0nmos@3_poly-left##3 8.636
R13 VB#0nmos@3_poly-left##3 VB#0nmos@3_poly-left##4 8.636
R14 VB#0nmos@3_poly-left##4 VB#0nmos@3_poly-left##5 8.636
R15 VB#0nmos@3_poly-left##5 VB 8.636
R16 VB#2pmos@0_poly-right VB#2pmos@0_poly-right##0 5.425
R17 VB#2pmos@0_poly-right##0 VB 5.425
R18 VB_bar#2pmos@1_poly-right VB_bar 7.75
R19 VA#2pmos@2_poly-right VA 7.75
R20 VA#0nmos@0_poly-left VA#0nmos@0_poly-left##0 9.079
R21 VA#0nmos@0_poly-left##0 VA#0nmos@0_poly-left##1 9.079
R22 VA#0nmos@0_poly-left##1 VA#0nmos@0_poly-left##2 9.079
R23 VA#0nmos@0_poly-left##2 VA#0nmos@0_poly-left##3 9.079
R24 VA#0nmos@0_poly-left##3 VA#0nmos@0_poly-left##4 9.079
R25 VA#0nmos@0_poly-left##4 VA#0nmos@0_poly-left##5 9.079
R26 VA#0nmos@0_poly-left##5 VA 9.079
R27 VB_bar#0nmos@1_poly-left VB_bar#0nmos@1_poly-left##0 9.079
R28 VB_bar#0nmos@1_poly-left##0 VB_bar#0nmos@1_poly-left##1 9.079
R29 VB_bar#0nmos@1_poly-left##1 VB_bar#0nmos@1_poly-left##2 9.079
R30 VB_bar#0nmos@1_poly-left##2 VB_bar#0nmos@1_poly-left##3 9.079
R31 VB_bar#0nmos@1_poly-left##3 VB_bar#0nmos@1_poly-left##4 9.079
R32 VB_bar#0nmos@1_poly-left##4 VB_bar#0nmos@1_poly-left##5 9.079
R33 VB_bar#0nmos@1_poly-left##5 VB_bar 9.079

* Spice Code nodes in cell cell 'XNOR{lay}'
.include tsmc350.txt
.PARAM SUPPLY=3.3V
VDD VDD 0 DC 'SUPPLY'
VA VA 0 PULSE 0 3.3 0 5n 5n 270n 540n
VA_bar VA_bar 0 PULSE 3.3 0 10n 5n 5n 270n 540n
VB VB 0 PULSE 0 3.3 0 5n 5n 255n 510n
VB_bar VB_bar 0 PULSE 3.3 0 10n 5n 5n 255n 510n
.tran 1620n
.meas tran tphl_B1 TRIG v(VB) V(VDD)/2 FALL=1 TARG v(VOUT) V(VDD)/2
FALL=1
.meas tran tphl_B2 TRIG v(VB) V(VDD)/2 RISE=1 TARG v(VOUT) V(VDD)/2
FALL=1
.meas tran tplh_A1 TRIG v(VA) V(VDD)/2 FALL=1 TARG v(VOUT) V(VDD)/2
RISE=1
.meas tran tplh_A2 TRIG v(VA) V(VDD)/2 RISE=1 TARG v(VOUT) V(VDD)/2
RISE=1
.meas tran tphl  param  max(tphl_B1, tphl_B2)
.meas tran tplh  param  max(tplh_A1, tplh_A2)
.meas P_D PARAM (tphl+tplh)/2
.meas TRAN Avg_P AVG -V(VDD)*I(VDD) FROM=0 TO=540n
.END
```

waveform