Q(5.6)

A sequential circuit with two D flip flops A and B, two inputs X and y, and one output Z is specified by the following next state and output equations:

$$A(t+1) = X'y + XB$$
$$B(t+1) = X'A + XB$$
$$Z = A$$

a) Draw the logic diagram of the circuit.
b) List the state table for the sequential circuit.
c) Draw the corresponding state diagram.

ANS

⇒ In DFF ⟹ The (Next state) equation Q^* or $Q(t+1) = D$

So:

$$D_A = X'y + XB$$
$$D_B = X'A + XB$$
$$Z = A$$

a)

* The logic Diagram of the circuit

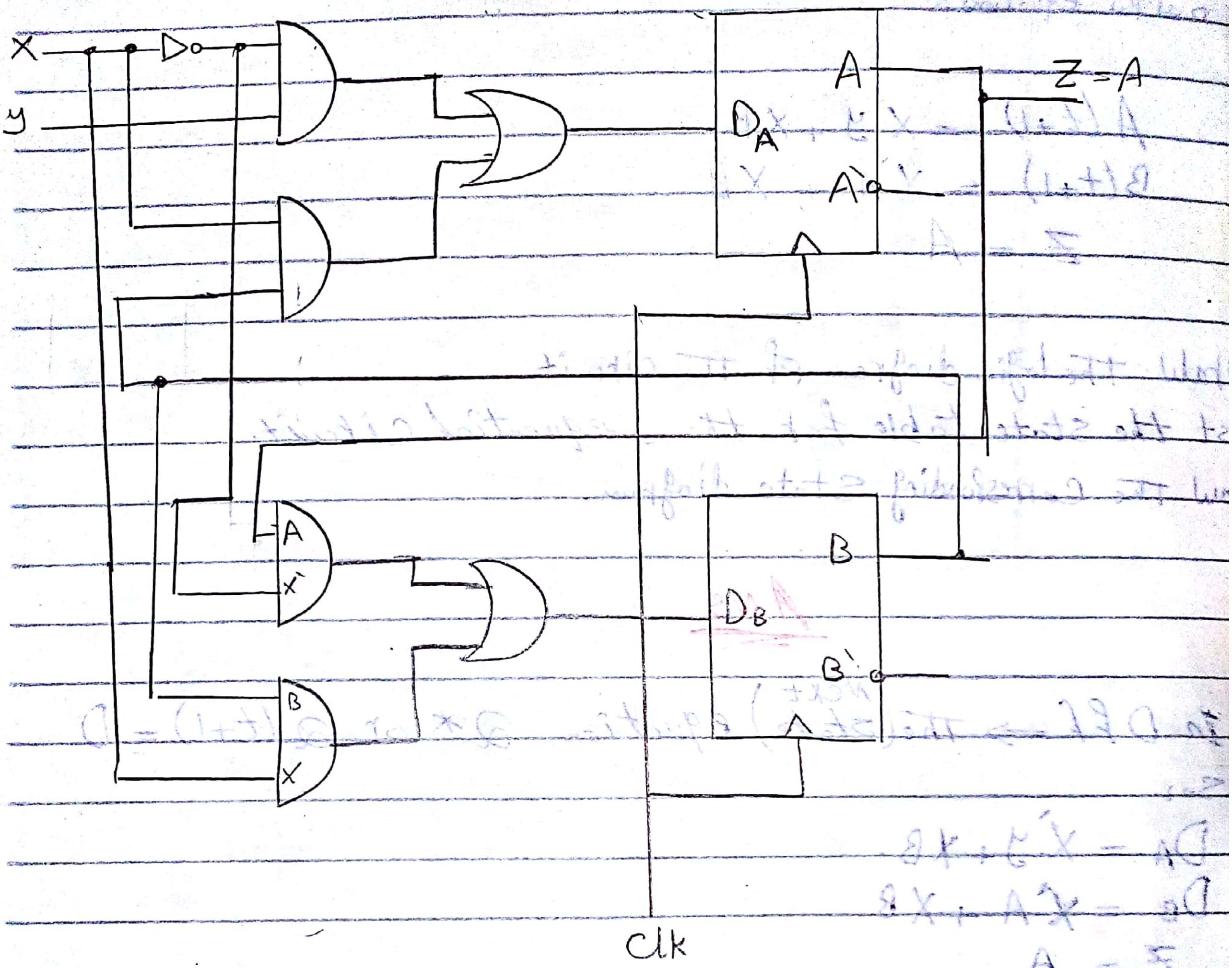
⟶

* the logic diagram of the circuit :

$D_A = X'y + XB$

$D_B = X'A + XB$

$Z = A$



For State table :

$A^* = X'y + XB$
$B^* = X'A + XB$

When $X = 0$, $y = 0$ [0 0]

$A^* = 0$
$B^* = A$

When $X = 0$, $y = 1$ [0 1]

$A^* = 1$
$B^* = A$

When $X = 1$, $y = 0$ [1 0]

$A^* = B$
$B^* = B$

When $X = 1$, $y = 1$ [1 1]

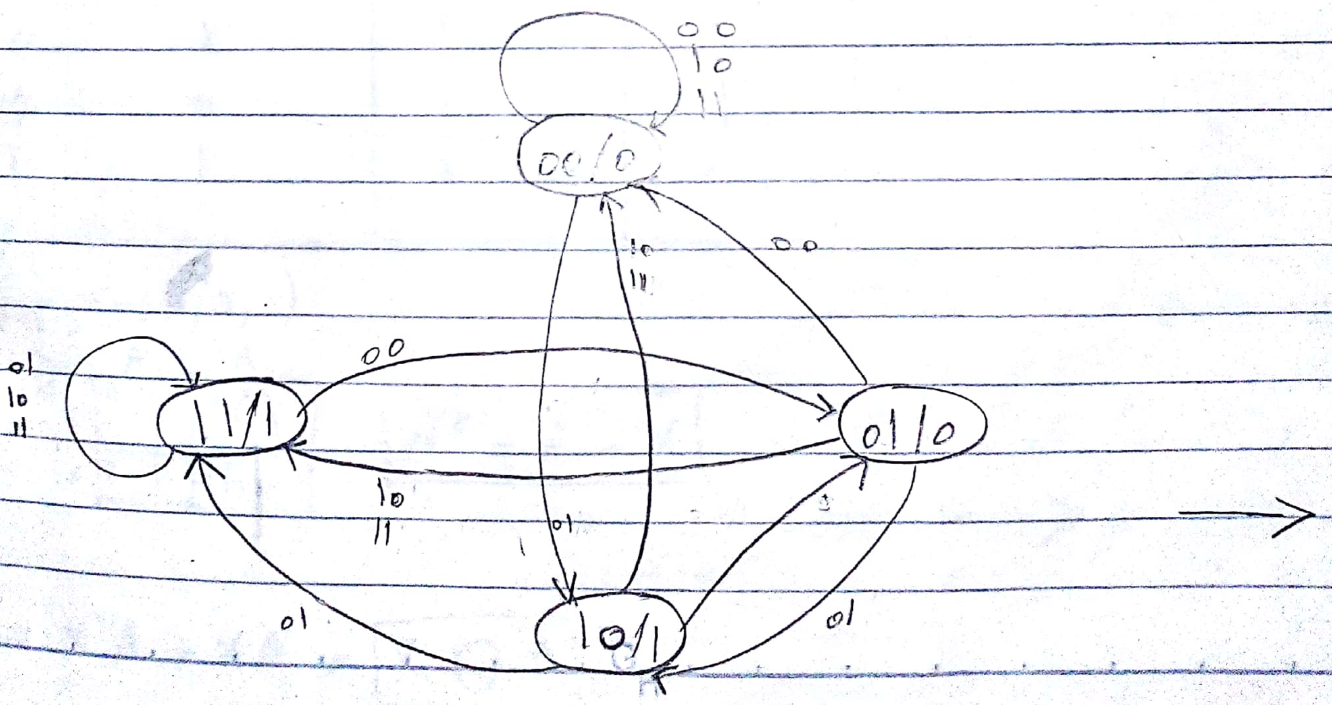
$A^* = B$
$B^* = B$

$A^* = \bar{x}y + xB$

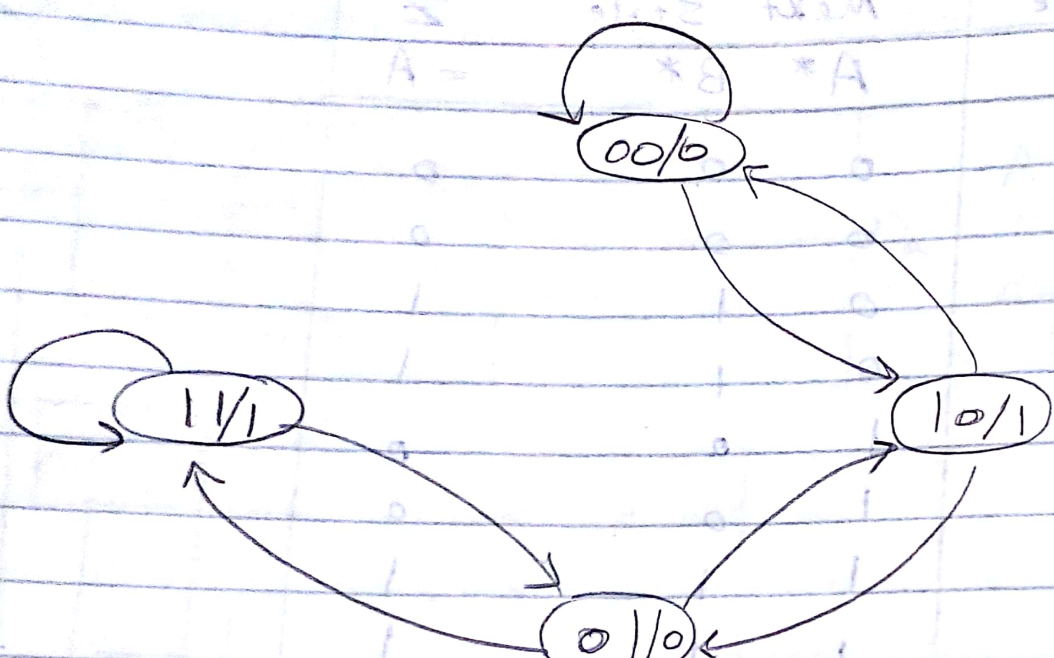
$B^* = \bar{x}A + xB$

② The state table:

Inputs		Present State		Next State		Z
x	y	A	B	A*	B*	= A
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	1	1
0	0	1	1	0	1	1
0	1	0	0	1	0	0
0	1	0	1	1	0	0
0	1	1	0	1	1	1
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	0	1	1	1	0
1	0	1	0	0	0	1
1	0	1	1	1	1	1
1	1	0	0	0	0	0
1	1	0	1	1	1	0
1	1	1	0	0	0	1
1	1	1	1	1	1	1



← ممكننا ضبط الرسمة لطريقة أفضل إذا وضعنا الـ States بهذا الترتيب.



← ممكنكم اكمال البيانات على الرسمة

(Q 5.2 in Summer-Exam) :

A synchronous sequential circuit has two T flip flops A and B, one input X and one output Y. The flip flop input equations and circuit output equations are respectively:

$$T_A = AX + BX$$

$$T_B = AX + B'X$$

$$Y = AB$$

a) Derive the state equations for $A(t+1)$ and $B(t+1)$

b) Draw the logic Diagram of the circuit.

c) Tabulate the state table.

d) Draw the State Diagram.

$\Longrightarrow$

Answer:

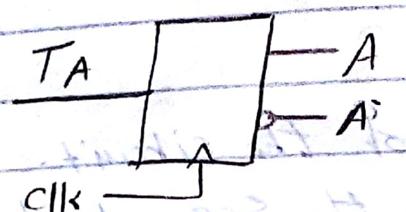
a) The state equations for $A(t+1)$ and $B(t+1)$:

In Toggle flip flop the next state equation

$$Q^* = T \oplus Q$$

$Q(t+1)$

Then for A flip flop.

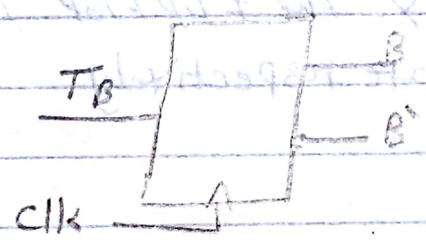


$$A^* \text{ or } A(t+1) = T_A \oplus A$$

معطى → $\boxed{T_A = AX + BX}$

$$A(t+1) = (AX + BX) \oplus A$$

& for B flip flop.



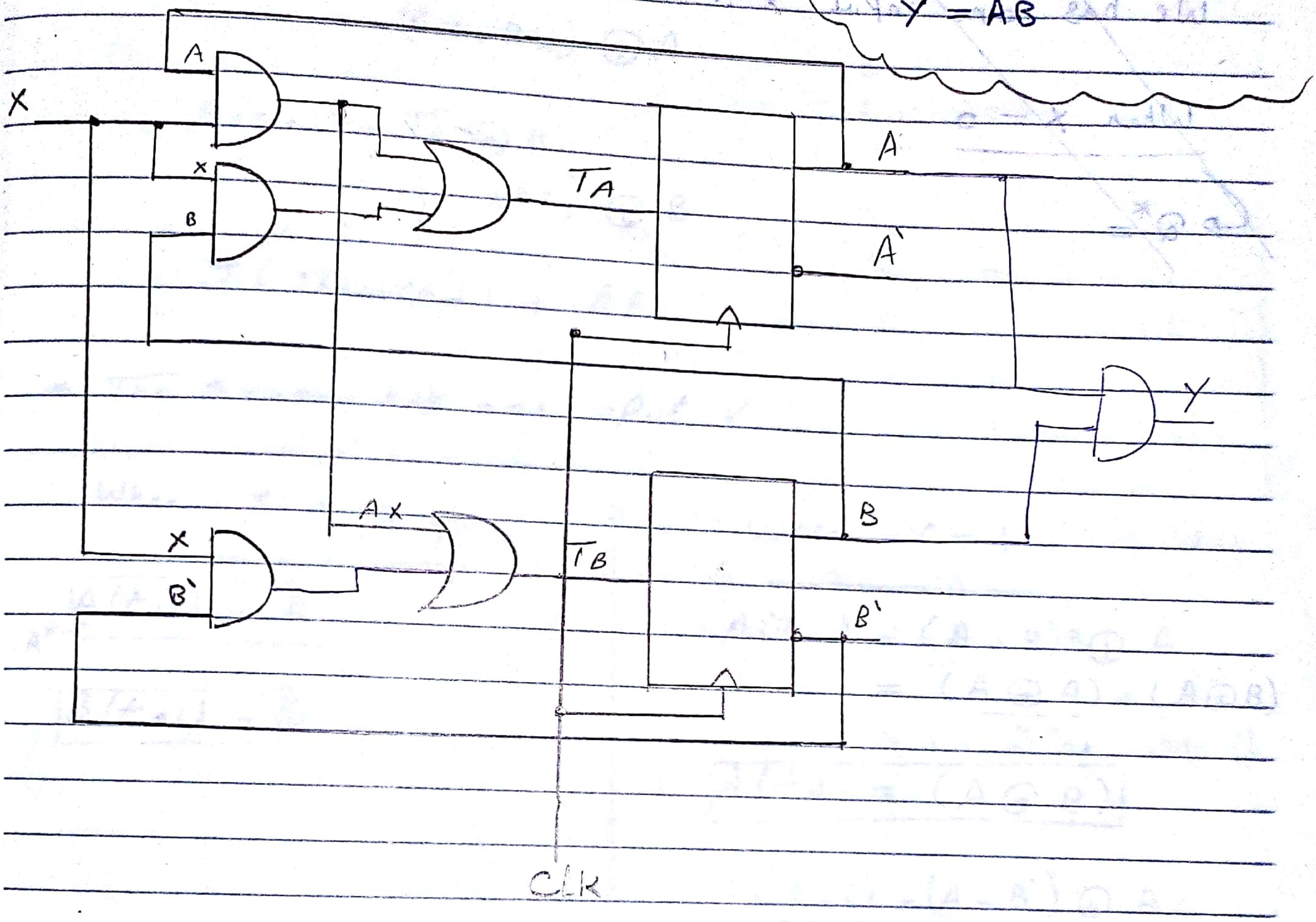
$$B(t+1) = T_B \oplus B$$

معطى → $\boxed{T_B = AX + B'X}$

$$B(t+1) = (AX + B'X) \oplus B$$

b) The logic Diagram of the circuit:

$T_A = AX + BX$
$T_B = AX + B'X$
$Y = AB$



c) The state table

⟹

c) The state table:

$$A(t+1) = (AX + BX) \oplus A$$

$$B(t+1) = (AX + B'X) \oplus B$$

$$y \text{ (The output)} = AB$$

* The system has one input X:

When $X=0$

$$A^* = 0 \oplus A$$
$$= A$$

$$B^* = 0 \oplus B$$
$$= B$$

$$y = AB$$

When $X=1$

$$A^* = (A+B) \oplus A$$

$$B^* = (A+B') \oplus B$$

$$y = AB$$

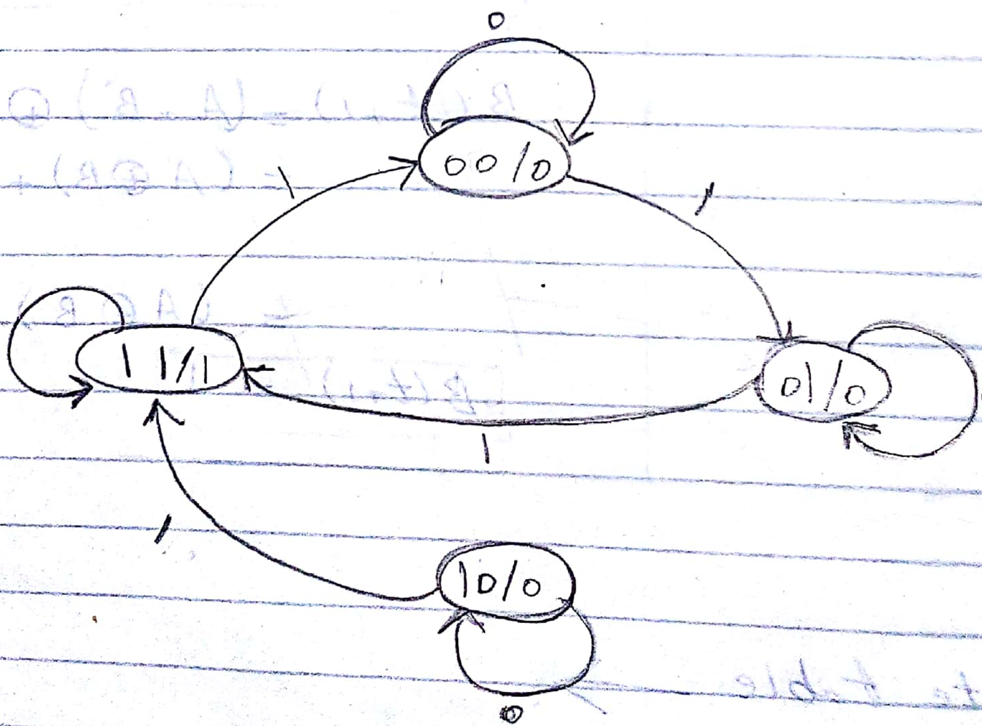
inputs	Present state		Next state		output
X	A	B	A*	B*	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	1	1
1	0	0	0	1	0
1	0	1	1	1	0
1	1	0	1	1	0
1	1	1	0	0	1

When $(X=0) \rightarrow A^* = A \,,\, B^* = B.$

" $(X=1) \rightarrow A^* = (A+B) \oplus A \,,\, B^* = (A+B') \oplus B$

The output $Y = AB.$

d) The state Diagram.



Q5.9)

A sequential circuit has two JK flip-flops A and B and one input X. The circuit is described by the following flip flop input equations:

$$J_A = X \qquad K_A = B'$$
$$J_B = X \qquad K_B = A$$

a) Derive the state equations $A(t+1)$ and $B(t+1)$ by substituting the input equations for the J and K variables.

b) Draw the state diagram of the circuit.

Answer

a) Q^* for JK flipflop is $= JQ' + K'Q$

For A flip flop:

$$A(t+1) = J_A A' + K_A' A$$
$$= XA' + (B')' A$$
$$\boxed{A(t+1) = XA' + BA}$$

For B flip flop:

$$B(t+1) = J_B B' + K_B' B$$
$$\boxed{B(t+1) = XB' + A'B}$$

b) ⇒ To draw the state diagram, ~~we~~ first, we must list the state table.

للوصول إلى (State diagram) هتكون محتاج أول الـ
→ State table

inputs	Present State		Next State	
X	A	B	A*	B*
0	0	0	0	0
0	0	1	0	1
0	1	0	0	0
0	1	1	1	0
1	0	0	1	1
1	0	1	1	1
1	1	0	0	1
1	1	1	1	0

ولتسجيل ملء الجدول ؟ نأتي بالمعادلات A(t+1), B(t+1) عندهم

$X = 0$, $X = 1$ $\quad [A(t+1) = XA' + BA$ & $B(t+1) = XB' + A'B]$

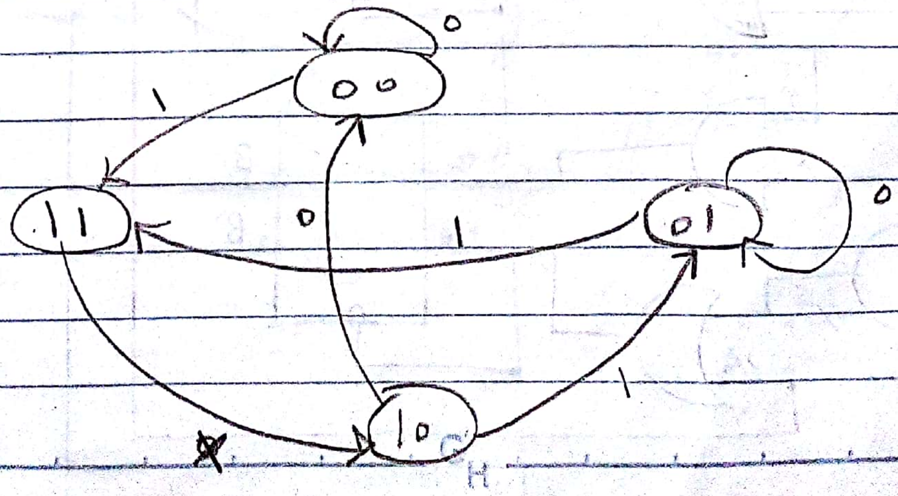
When $X = 0$

$$\boxed{A(t+1) = AB}$$
$$\boxed{B(t+1) = A'B}$$

When $X = 1$

$$A(t+1) = A' + AB$$
$$= \cancel{(A' + A)}(A' + B)$$
$$\boxed{A(t+1) = (A' + B)}$$

$$B(t+1) = B' + A'B$$
$$= (A' + B')\cancel{(B + B')}$$
$$\boxed{B(t+1) = (A' + B')}$$



Q5.10)

A sequential circuit has two JK flip flops A and B, two inputs x and y, and one output Z. The flip flop input equations and circuit output equation are:

$$J_A = Bx + B'y' \qquad K_A = B'xy'$$

$$J_B = A'x \qquad K_B = A + xy'$$

$$Z = Ax'y' + Bx'y'$$

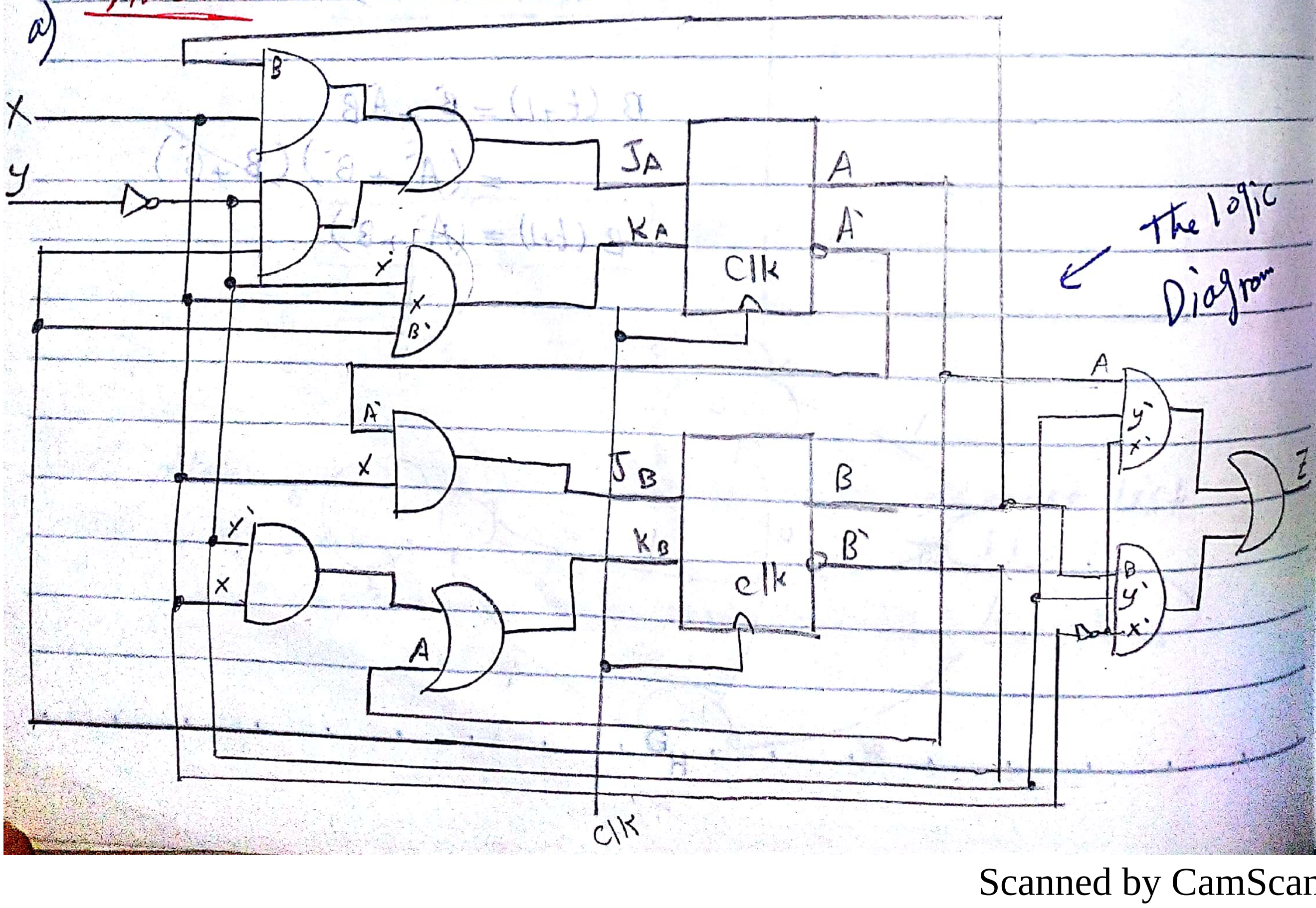
a) Draw the logic Diagram of the circuit.

b) Tabulate the state table.

c) Derive the state equations for A & B.

Answer:

a)



b) To tabulate the state table:.. $Q^*(JK) = JQ' + K'Q$

$$A(t+1) = J_A A' + K_A' A$$
$$= (Bx + B'y')A' + (B'xy')'A$$
$$\hookrightarrow (B + x' + y)$$
$$= A'Bx + A'B'y' + AB + Ax' + Ay$$

AB \ xy	x'y'	x'y	xy	xy'
A'B'	1			1
A'B			1	1
AB	1	1	1	1
AB'	1	1	1	

$$A(t+1) = Ax' + Ay + Bx + A'B'y'$$

$$B(t+1) = J_B B' + K_B' B$$
$$= A'xB' + (A + xy')'B$$
$$= A'xB' + A'(x'+y)B$$
$$= A'xB' + A'B(x'+y)$$
$$= A'xB' + A'Bx' + A'By$$

AB \ xy	x'y'	x'y	xy	xy'
A'B'			1	1
A'B	1	1	1	
AB				
AB'				

$$B(t+1) = A'Bx' + A'B'x + A'xy$$

No
Date

$A(t+1) = A x' + A y + B x + A' B' y'$ / $Z = A \bar{x} \bar{y} + B \bar{x} \bar{y}$

$B(t+1) = A' B x' + A' B' x + A' x y$

This system has Two inputs x, y

When $x=0$ & $y=0$

$A(t+1) = A + A' B'$

$\boxed{A^* = A + B'}$

$\boxed{B(t+1) = A' B}$

$Z = A + B$

When $x=0$ & $y=1$

$A^* = A + A$

$\boxed{A^* = A}$

$\boxed{B^* = A' B}$

$Z = 0$

When $x=1$ & $y=0$

$A^* = B + A' B'$

$\boxed{A^* = B + A'}$

$\boxed{B^* = A' B'}$

$Z = 0$

When $x=1$ & $y=1$

$\boxed{A^* = A + B}$

$B^* = A' B' + A'$

$\boxed{B^* = A'}$

$Z = 0$

b) The state table ⟹

inputs		Present state		Next state		output
x	y	A	B	A*	B*	Z
0	0	0	0	1	0	0
0	0	0	1	0	1	1
0	0	1	0	1	0	1
0	0	1	1	1	0	1
0	1	0	0	0	0	0
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	1	1	0
1	0	0	1	1	0	0
1	0	1	0	0	0	0
1	0	1	1	1	0	0
1	1	0	0	0	1	0
1	1	0	1	1	1	0
1	1	1	0	1	0	0
1	1	1	1	1	0	0

c) The State equations:

$$A(t+1) = Ax' + Ay + Bx + A'B'y'$$

$$B(t+1) = A'Bx' + A'B'x + A'xy$$

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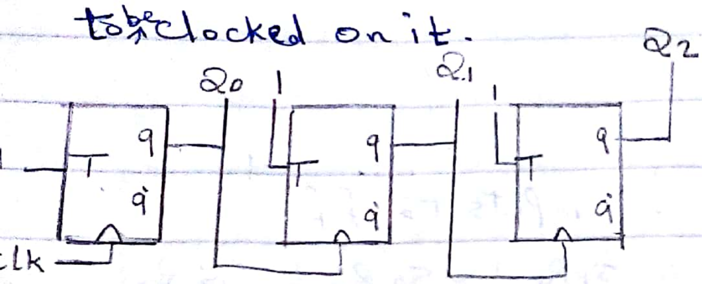
Counters :-

ASynchronous Counter

غير متزامن :-

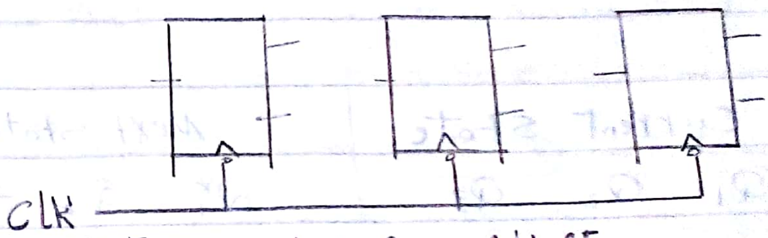
- Called Ripple Counter.
- The flipflops aren't clocked using same clock.
- each ff wait the output signal of the previous ff. to be clocked on it.



A synchronous Counter.

متزامن مع clk

- All ffs clock inputs are directly connected to the clock signal.
- And All ffs outputs change at the same time.



The Same clock for All FFs.

Examples :-

Ex1:

* Design a 3 bit up Counter by using SR ffs. That Counts.
0 1 2 3 4 5 6 7 and Repeat.

Ans:-

↳ 3 bit mean from 0 : 7 ⇒ 8 states.

↳ We will use 3 ff.

↳ each "ff" for a 1 bit.

↳ (up) mean → Counter from 0 to 7 ⇒ (0 1 2 3 4 5 6 7 0 ...)

↳ (في هذا المثال هنضيف أعمدة (Modified State Transition Table)

⇒ Modified State Transition Table:

Current State			Next State			inputs to ff.					
Q_1	Q_2	Q_3	Q_1^*	Q_2^*	Q_3^*	S_1	R_1	S_2	R_2	S_3	R_3
0	0	0	0	0	1	0	X	0	X	1	0
0	0	1	0	1	0	0	X	1	0	0	1
0	1	0	0	1	1	0	X	X	0	1	0
0	1	1	1	0	0	1	0	0	1	0	1
1	0	0	1	0	1	X	0	0	X	1	0
1	0	1	1	1	0	X	0	1	0	0	1
1	1	0	1	1	1	X	0	X	0	1	0
1	1	1	0	0	0	0	1	0	1	0	1

⇐ لملء هذا العمود نحتاج إلى ExcitationTable لـ SRff.

S R		Q	Q^*	S	R
0 0	No change	0	0	0	X
0 1	Reset				
1 0	Set	0	1	1	0
0 1	Reset	1	0	0	1
0 0	No change	1	1	X	0
1 0	Set				

لملء عمود $(S_1 R_1)$ ننظر إلى (Q_1, Q_1^*)
(Q_2, Q_2^*) " " $(S_2 R_2)$ " "
(Q_3, Q_3^*) " " $(S_3 R_3)$ " "
وذلك من Excitation Table

$S_1 = \Sigma m(3) + \Sigma d(4,5,6)$

	$Q_1'Q_2'$	$Q_1'Q_2$	Q_1Q_2	Q_1Q_2'
Q_3'			X	X
Q_3		1		X

$\boxed{S_1 = Q_1' Q_2 Q_3}$

$S_2 = \Sigma m(1,5) + \Sigma d(2,6)$

Q_3'		X	X	
Q_3	1			1

$\boxed{S_2 = Q_2' Q_3}$

$R_1 = \Sigma m(7) + \Sigma d(0,1,2)$

	$Q_1'Q_2'$	$Q_1'Q_2$	Q_1Q_2	Q_1Q_2'
Q_3'	X	X		
Q_3	X		1	

$\boxed{R_1 = Q_1 Q_2 Q_3}$

$R_2 = \Sigma m(3,7) + \Sigma d(0,4)$

Q_3'	X			X
Q_3		1	1	

$\boxed{R_2 = Q_2 Q_3}$

$S_3 = \Sigma m(0,2,4,6)$

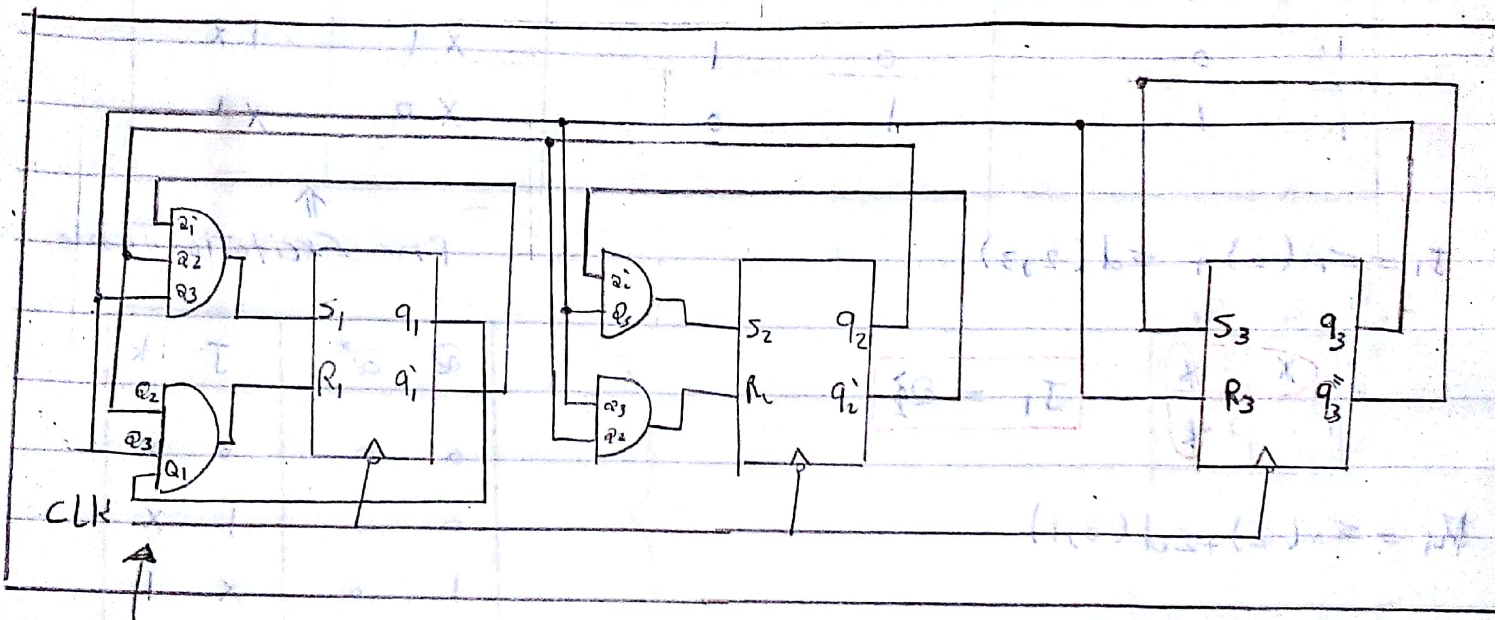
Q_3'	1	1	1	1
Q_3				

$\boxed{S_3 = Q_3'}$

$R_3 = \Sigma m(1,3,5,7)$

Q_3'				
Q_3	1	1	1	1

$\boxed{R_3 = Q_3}$



(Sequential Circuit by using SR ff.)
(Implementation)

Note :-
This System is synchronous Counter. ⇒ "The Same clock"

Ex2:

* Design: a 2 bits <u>down</u> Counter by using JK ff:

Ans:

* 2 bits from 0 : 3
* We Need to 2 ffs.

⇒ (down) means Counter from 3 to 0

3 2 1 0 3 2 1 0 ....

* Modified state Transition Table: ~~(state model)~~

Current state		Next State		inputs to ff.	
Q_1	Q_2	Q_1^*	Q_2^*	J_1 K_1	J_2 K_2
0	0	1	1	1 X	1 X
0	1	0	0	0 X	X 1
1	0	0	1	X 1	1 X
1	1	1	0	X 0	X 1

⇑ from Excitation Table

Q	Q^*	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

$J_1 = \Sigma m(0) + \Sigma d(2,3)$

	Q_1'	Q_1
Q_2'	1	X
Q_2		X

$\boxed{J_1 = Q_2'}$

$K_1 = \Sigma m(2) + \Sigma d(0,1)$

	X	1
	X	

$\boxed{K_1 = Q_2'}$

$J_2 = \Sigma m(0,2) + \Sigma d(1,3)$

	1	1
	X	X

$\boxed{J_2 = 1}$

$K_2 = \Sigma m(1,3) + \Sigma d(0,2)$

	X	X
	1	1

$\boxed{K_2 = 1}$

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* sequential Circuit by using JKff :

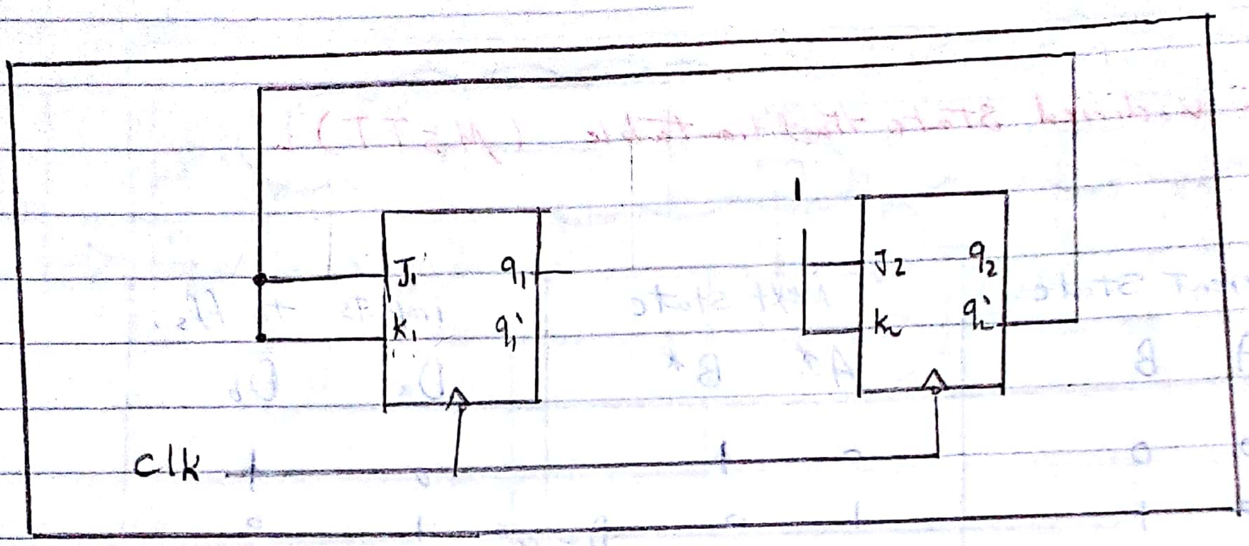
(Implementation)

$J_1 = Q_2'$

$K_1 = Q_2'$

$J_2 = 1$

$K_2 = 1$



Ex 3:

Design and implement a counter with 2 DFFs A and B, with a one bit control line X. if X = 0, it counts 0, 1, 2, 3, 3, ...
if X = 1, it counts 3, 2, 1, 0, 0, ...

ANS: ~~(Mealy model)~~

* The Modified State transition table (MSTT):

Current State			Next state		inputs to ffs.	
X	A	B	A^*	B^*	D_a	D_b
0	0	0	0	1	0	1
0	0	1	1	0	1	0
0	1	0	1	1	1	1
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	0	1	0	1
1	1	1	1	0	1	0

$D = Q^*$

$D_a = \Sigma m(1, 2, 3, 7)$

B \ XA	X\`A\`	X\`A	XA	XA\`
B\`	0	2: 1	6	4
B	1: 1	3: 1	7: 1	5

$D_a = X'A + AB + X'B$

$= X'(A + B) + AB$

$D_b = \Sigma m(0, 2, 3, 6)$

B \ XA				
	1	1	1	
		1		

$D_b = X'A + X'B' + AB'$

$= X'(A + B') + AB'$

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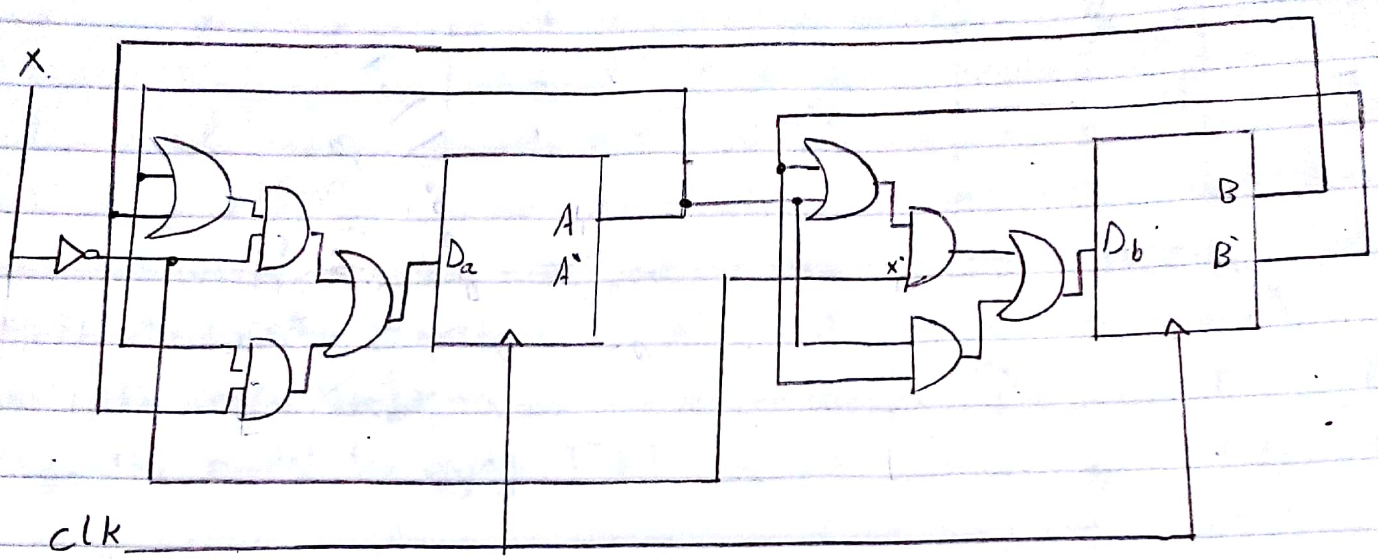
* A sequential circuit by using DFF:- (Implementation)

⇒ A solution implementation :-

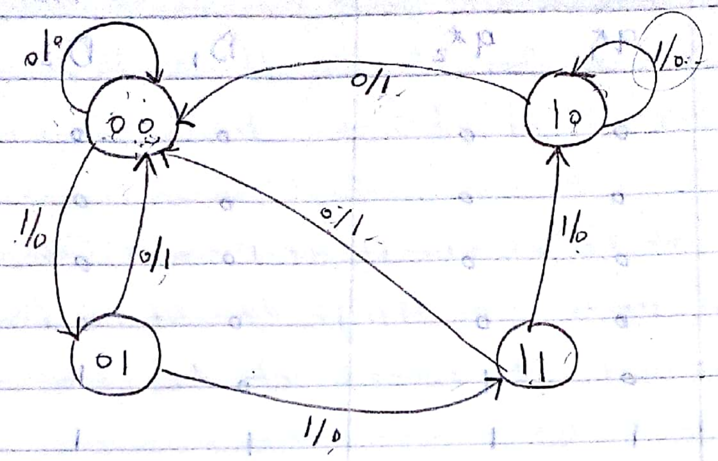
$$D_a = \bar{x}(A+B) + AB$$
$$D_b = \bar{x}(A+\bar{B}) + A\bar{B}$$



EX6:

• For the following state Diagram : "The starting from state 00"

→ Determine the state transitions. and Design this system by using DFF.



Ans:

The state table.

Present state (q)		Next state (q*)				Output (Z)	
q_1	q_2	X = 0 q_1^*	X = 0 q_2^*	X = 1 q_1^*	X = 1 q_2^*	X = 0	X = 1
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

MSTT ⟹

* Modified state transition table:

Present state			Next state		Inputs to ffs.		output
X	q_1	q_2	q^*_1	q^*_2	D_1	D_2	Z
0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	1
0	1	0	0	0	0	0	1
0	1	1	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	1	1	1	1	1	0
1	1	0	1	0	1	0	0
1	1	1	1	0	1	0	0

$\boxed{D = q^*}$

* The equations:

$D_1 = \Sigma m(5, 6, 7)$

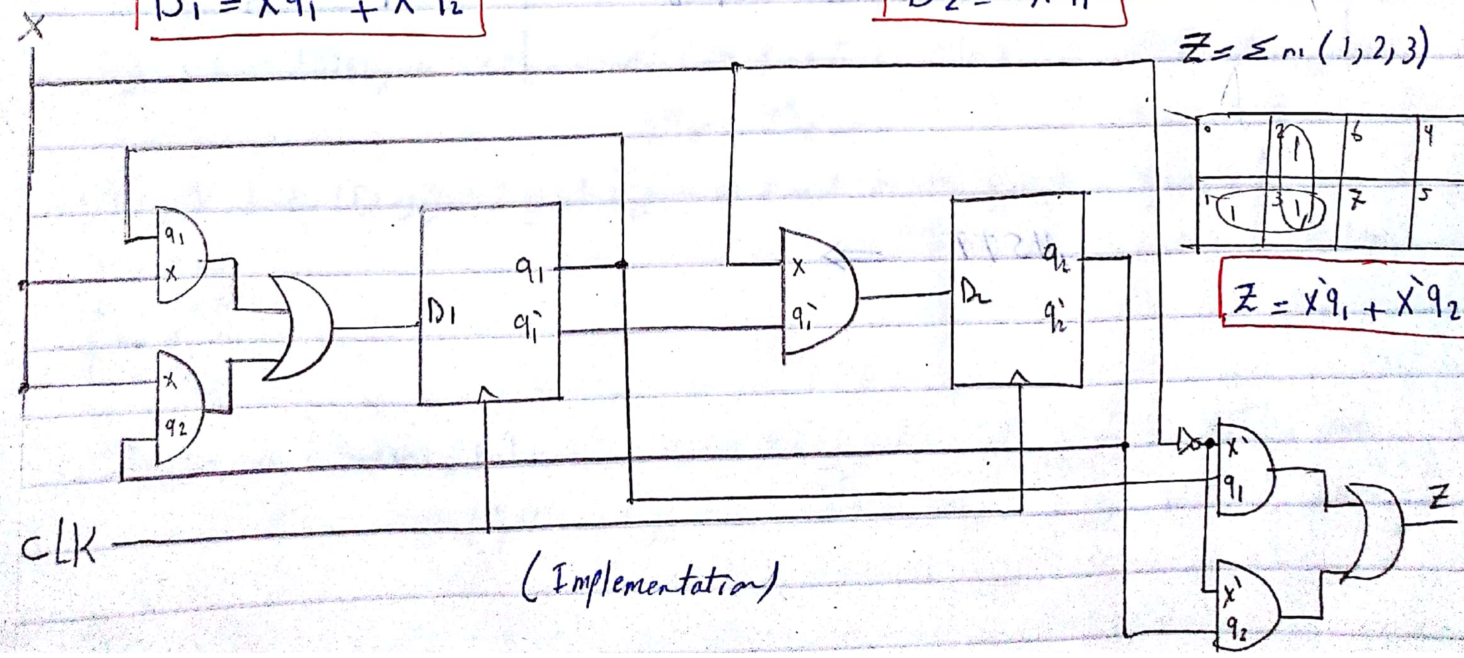
q_2 \ xq_1	$x'q_1'$	$x'q_1$	xq_1	xq_1'
q_2'	0	2	6 1	4
q_2	1	3	7 1	5 1

$\boxed{D_1 = Xq_1 + Xq_2}$

$D_2 = \Sigma m(4, 5)$

0	2	6	4 1
1	3	7	5 1

$\boxed{D_2 = Xq_1'}$



(Implementation)

$Z = \Sigma m(1, 2, 3)$

0	2 1	6	4
1 1	3 1	7	5

$\boxed{Z = x'q_1 + x'q_2}$

EX7:

* Design a sequential circuit with two DFFs A, B and one input X

a) When X = 0 ; the state of the circuit remains the same ; ~~When X = 1~~
When X = 1, the circuit goes through the state transitions from:
00, to 01, to 11, to 10, back to 00 and repeats.

b) When X = 0, the state of the circuit remains the same. ($q^* = q$)
When X = 1, the circuit goes through the state transitions from:
00 to 11, to 01, to 10 back to 00 and repeats:

ANS:

a) MSTT :

Current State			Next State		Inputs to DFF	
X	q_1 A	q_2 B	q_1^* A*	q_2^* B*	Da	Db
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	1	0	1	0
0	1	1	1	1	1	1
1	0	0	0	1	0	1
1	0	1	1	1	1	1
1	1	0	0	0	0	0
1	1	1	1	0	1	0

$D = q^*$ $\Leftrightarrow$

You Complete it ⇒ * extract the equations of D_1, D_2
* Minimize them by k.map.
* Build the Design by DFFs.

b) MSTT.

Current state			Next state		inputs to DFFs	
X	q_1 A	q_2 B	q^*_1 A*	q^*_2 B*	Da	Db
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	1	0	1	0
0	1	1	1	1	1	1
1	0	0	1	1	1	1
1	0	1	1	0	1	0
1	1	0	0	0	0	0
1	1	1	0	1	0	1

⟹ You complete it.

EX8:

* Design a sequential circuit with two JK flip flops A & B and two inputs E and F,
* If E = 0 , The circuit remains in the same state regardless of (بغض النظر عن) the value of F.
* When E=1 and F=1 , the circuit goes through the state transitions from 00 to 01 to 10 to 11 back to 00 and Repeats.
* When E=1 and F=0 , the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00 and Repeats.

Q	Q*	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Ans :

⇒ MSTT

Current state				Next state		Inputs to JK ffs			
E	F	A (q_1)	B (q_2)	A* (q_1^*)	B* (q_2^*)	J_1	K_1	J_2	K_2
0	0	0	0	0	0	0	X	0	X
0	0	0	1	0	1	0	X	X	0
0	0	1	0	1	0	X	0	0	X
0	0	1	1	1	1	X	0	X	0
0	1	0	0	0	0	0	X	0	X
0	1	0	1	0	1	0	X	X	0
0	1	1	0	1	0	X	0	0	X
0	1	1	1	1	1	X	0	X	0
1	0	0	0	1	1	1	X	1	X
1	0	0	1	0	0	0	X	X	1
1	0	1	0	0	1	X	1	1	X
1	0	1	1	1	0	X	0	X	1
1	1	0	0	0	1	0	X	1	X
1	1	0	1	1	0	1	X	X	1
1	1	1	0	1	1	X	0	1	X
1	1	1	1	0	0	X	1	X	1

E=0 ⇒ q* = q (The Same)

E=1 , F=0 (00→11→10→01)

E=1 , F=1 (00→01→10→11)

To Complete it.