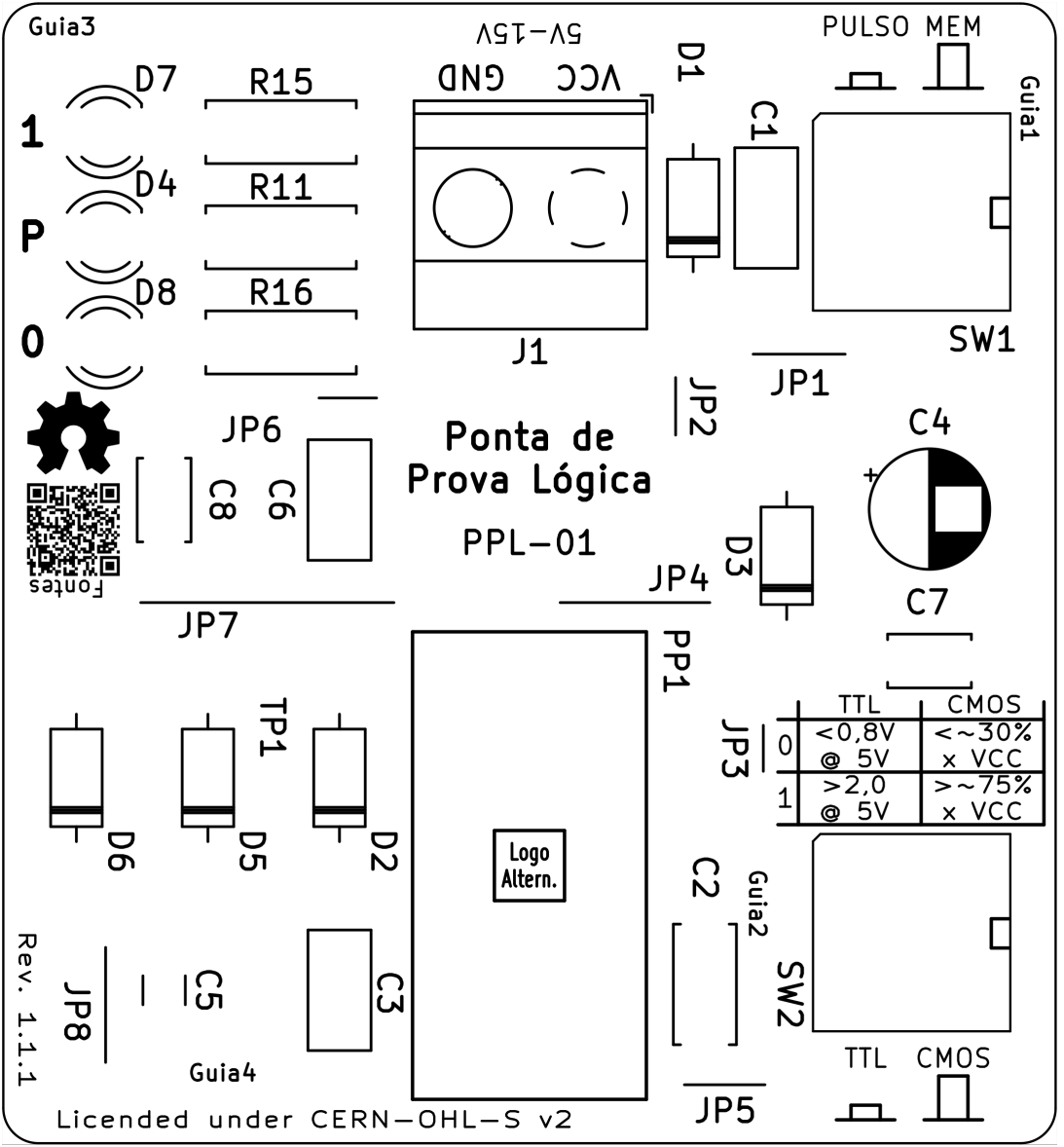
Guia3
5V–15V
VCC GND
PULSO MEM
Guia1
D7
R15
D1
C1
1
D4
R11
P
D8
R16
0
J1
SW1
JP1
JP2
JP6
C4
C8
C6
Ponta de
Prova Lógica
PPL–01
Fontes
D3
JP4
C7
JP7
PP1
TTL
CMOS
TP1
JP3
0
< 0,8V @ 5V
< ~30% x VCC
1
> 2,0 @ 5V
> ~75% x VCC
D6
D5
D2
Logo Altern.
C2
Guia2
SW2
C3
JP8
C5
Guia4
TTL
CMOS
JP5
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