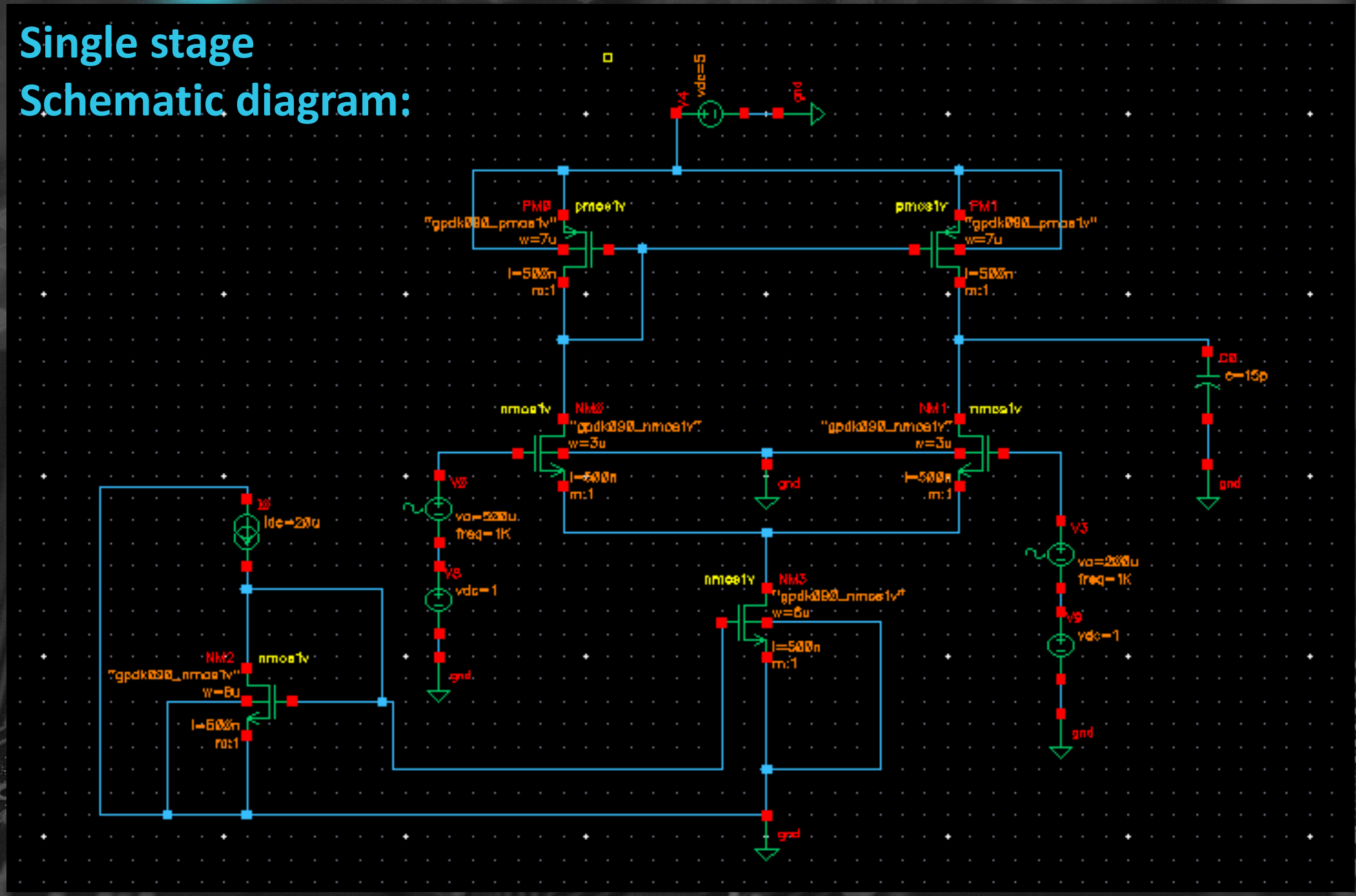
Implementation and Simulation Results

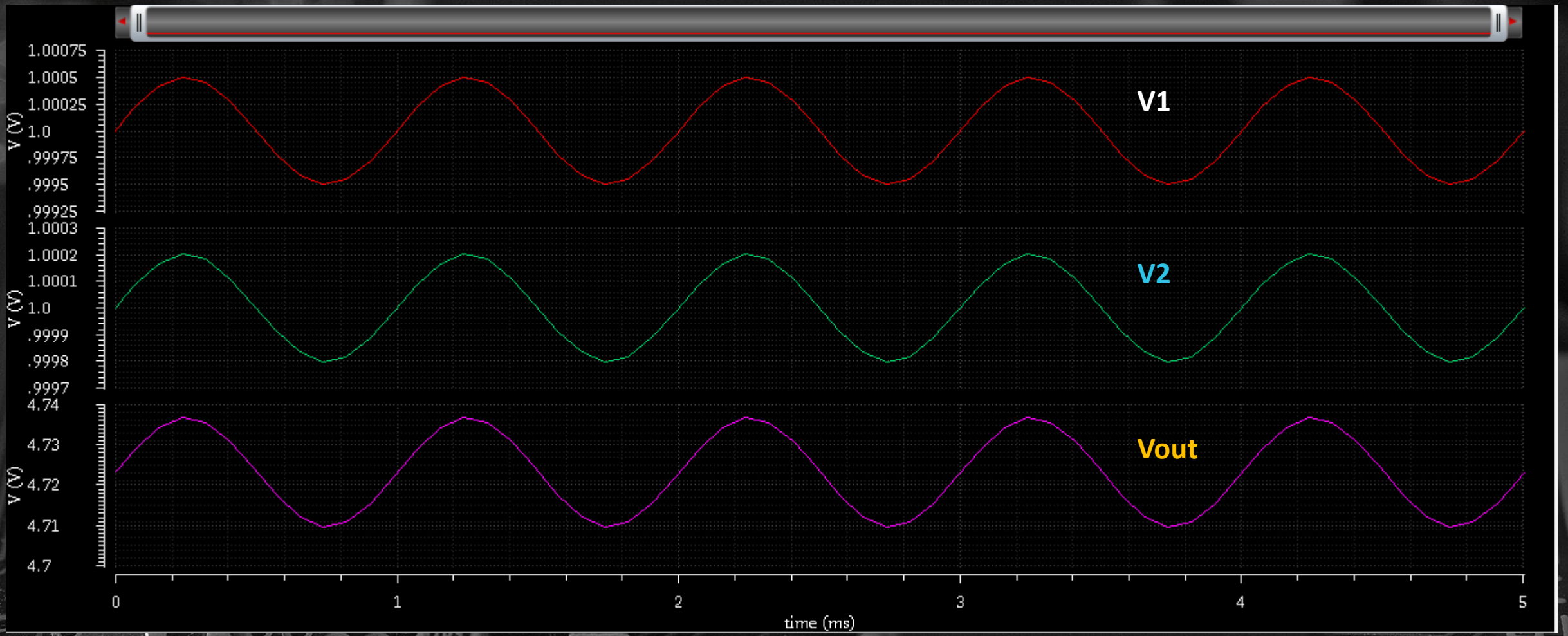
- The design is implemented using 90 nm Technology in Cadence using gpdk90 library
- The width and lengths are taken as per the specifications given in the paper
- Beside table shows the lengths and width Of the various mosfets used in the circuit

MOSFET	W/L(SIZE)
M1	3µ/500nm
M2	3µ/500nm
M3	7µ/500nm
M4	7µ/500nm
M5	6µ/500nm
M6	30µ/500nm
M7	30µ/500nm
M8	6µ/500nm
M9	6µ/500nm
C_L	3pF
C_C	680fF

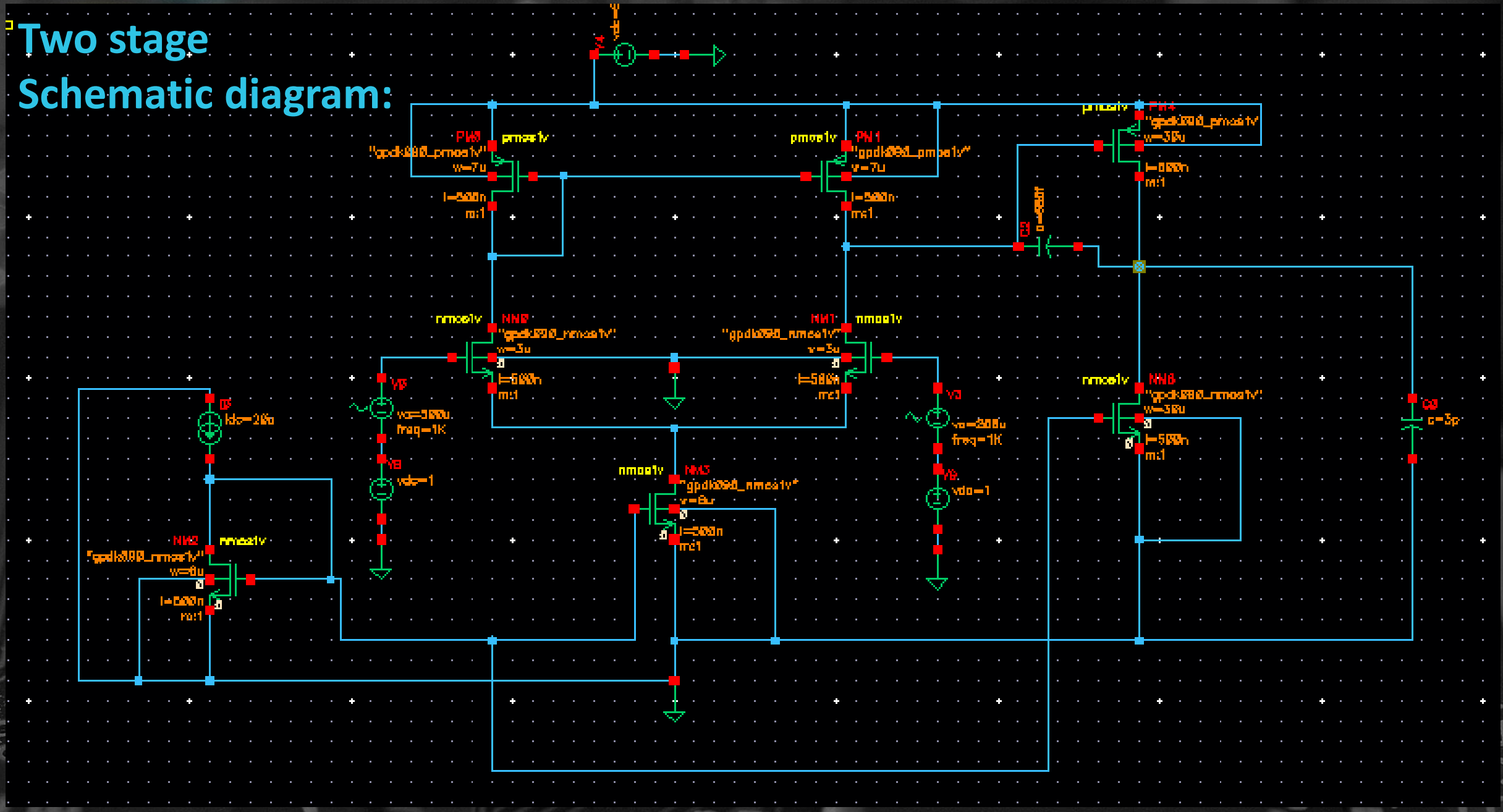
Single stage
Schematic diagram:



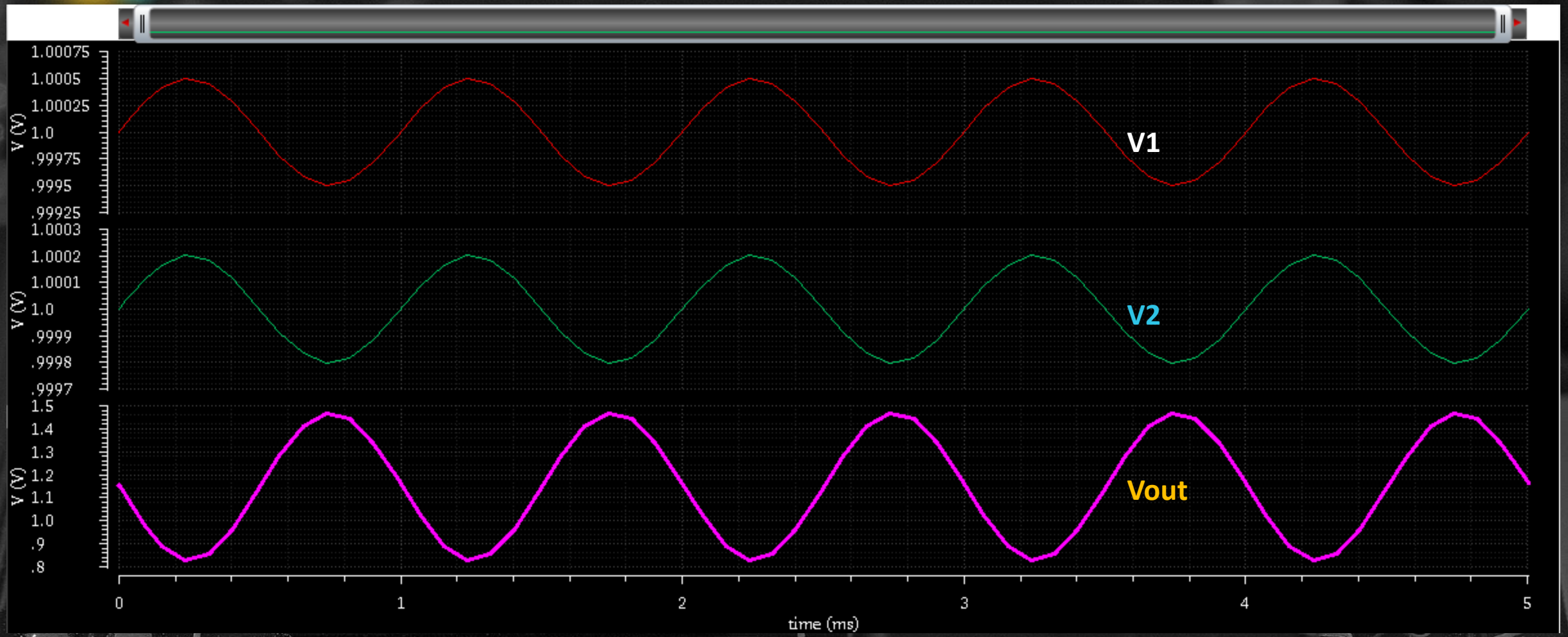
Input and Output waveforms:



Two stage Schematic diagram:



Input and Output waveforms:



Gain and CMRR Calculations

Differential mode:

V1 = 1 mV pk-pk 1kHz

V2= 0.4 mV pk-pk 1kHz

Vin = V1-V2

= 0.6 mV pk-pk

Vout = 664 mV pk-pk (from the graph)

$$Gain = \frac{Vout}{Vin} = \frac{664}{0.6} = 1106$$

$$Gain\ in\ dB = 20\log_{10} 1106 = 60.88\ dB$$

$$CMRR = \frac{A_d}{A_c} = \frac{1106}{0.2} = 5530$$

CMRR in dB = 74.8dB

common mode:

V1 = 1 mV pk-pk 1kHz

V2 = 1mV pk-pk 1kHz

$$Vin = \frac{V1+V2}{2}$$

= 1 mV pk-pk

Vout = 0.2 mV pk-pk (from the graph)

$$Gain = \frac{Vout}{Vin} = \frac{0.2}{1} = 0.2$$

$$Gain\ in\ dB = 20\log_{10} 0.2 = -14\ dB$$

Conclusion

The two stage operational amplifier was simulated in cadence with gpdk90nm technology.

After simulating the proposed circuit we have got high gain of 61dB with several other good parameters. CMRR of 75dB . the response of the circuit is very high as a result its gets an edge over other circuits and the CMRR with the proposed technique increases its value.