PROPOSED TECHNIQUE

We know that CMRR=$\frac{A_d}{A_c}$

A_d *→differential gain*

A_c *→common mode gain*

CMRR can be increased by ↑A_d *and* A_c*↓*

→A_d *is increased by using two stages*

→A_c *is decreased by increasing the* R_{DS} *of mosfet as*

$$A_c=\frac{1}{2R_{DS}}$$

→R_{DS} *is increased by using another mosfet as resistor*

→A capacitor is connected between output of stages and input of stage 2 for miller compensation to increase phase margin

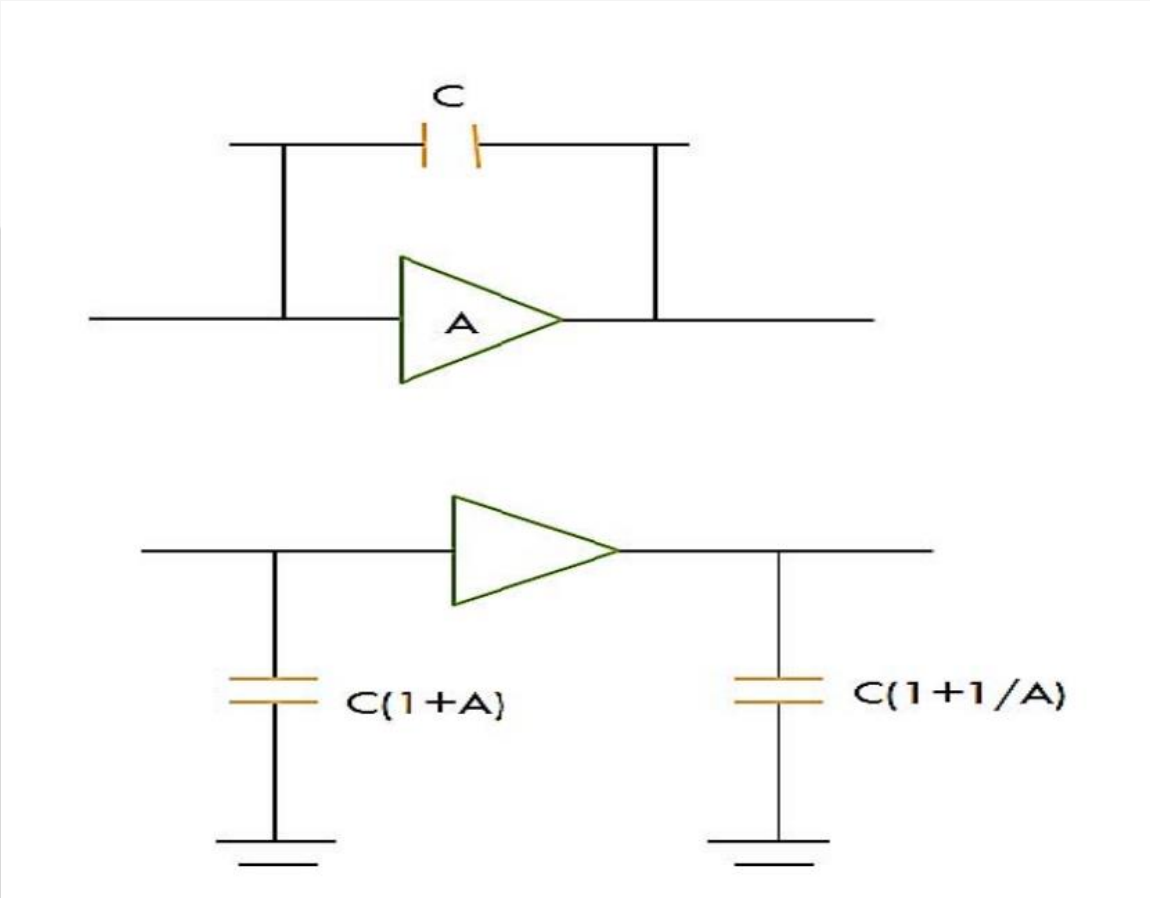
The circuit is modelled as

Cont..

MILLER EFFECT:

By using small 'C' we can get larger value of 'C' by miller effect.

- *It is used for better phase margin. If p1(pole 1) can be shifted towards left and p2(pole 2) can be shifted towards right then phase margin will be better. As we can see in the diagram above the effect of capacitance "C" in pole P1 & P2, by implementing in P1 the pole shifts greatly towards left and P2 shifts towards right. So here miller capacitor is being used to get good phase margin.*



Cont..

The proposed circuit diagram: