# 8-CHANNEL ESD ARRAY FOR PORTABLE SPACE-SAVING APPLICATIONS

**Check for Samples: TPD8E003**

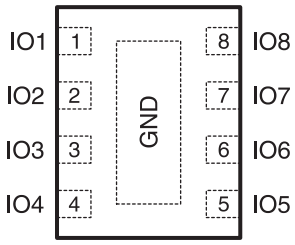
## FEATURES

- **8-Channel ESD Clamp Array to Enhance System-Level ESD Protection**
- **Exceeds IEC61000-4-2 (Level 4) ESD Protection Requirements**
  - **±12-kV IEC 61000-4-2 Contact Discharge**
  - **±15-kV IEC 61000-4-2 Air-Gap Discharge**
- **3.5-A Peak Pulse Current (8/20-µs Pulse)**
- **±15-kV Human-Body Model (HBM)**
- **Low Breakdown Voltage of 6 V**
- **Low Leakage Current**
- **Space-Saving Ultra-Thin, Small Outline No-Lead [WSON (DQD)] Package (0.4-mm Pitch)**

## APPLICATIONS

- **Keypad**
- **Touch-Screen Interface**
- **Memory Interface**
- **Docking Connector Interface**

**DQD PACKAGE**
**(TOP VIEW)**




## DESCRIPTION

The TPD8E003 is an array of 8 ESD clamps in a space saving SON (DQD) package. This integrated transient voltage suppressor device is designed for applications requiring system level ESD robustness. It is intended for use in sensitive equipment such as portable computers, cell phone, communication systems, and other applications. Its integrated design provides very effective and reliable protection for eight separate lines using only one package. The monolithic silicon technology of TPD8E003 offers superior matching between multiple lines over discrete ESD clamp solutions.

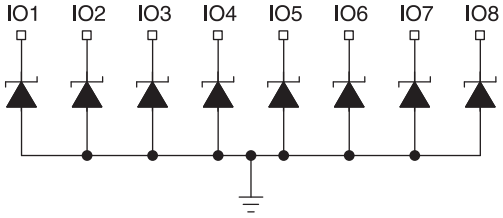
The TPD8E003 includes an ESD protection circuitry which prevents damage to the application when subjected to ESD stress exceeding IEC 61000-4-2 (Level 4). The TPD8E003 is specified for –40°C to 85°C operation.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE(1) (2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | WSON – DQD | L = 1.7 mm, W = 1.35 mm, H = 0.75 mm, pitch = 0.4 mm | TPD8E003DQDR | 65S |

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

**CIRCUIT SCHEMATIC**



## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| | IO voltage tolerance | IO pins | | 6 | V |
| $T_A$ | Operating free-air temperature range | | −40 | 85 | ºC |
| $T_{stg}$ | Storage temperature | | −55 | 155 | ºC |
| | IEC 61000-4-2 Contact Discharge | IO pins | | ±12 | kV |
| | IEC 61000-4-2 Air-Gap Discharge | IO pins | | ±15 | kV |
| | Peak pulse power (tp = 8/20 µs) | | | 55 | W |
| | Peak pulse current (tp = 8/20 µs) | | | 3.5 | Amp |
| | Human Body Model ESD | IO pins | | ±15 | kV |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{clamp}$ | Clamp voltage | $I_{IO}$ = 2 A, IO pin to ground | | | 10 | V |
| $I_I$ | Leakage current | IO pin to ground | | | 0.1 | µA |
| $C_{IO}$ | IO capacitance | $V_{IO}$ = 2.5 V, IO pins | 7 | 9 | 12 | pF |
| $\Delta C_{IO}$ | Differential line capacitance | $V_{IO}$ = 2.5 V, between IO pins | | 0.1 | | pF |
| $V_{BR}$ | Break-down voltage | $I_{IO}$ = 1 mA | 6 | | | V |
| $R_{dyn}$ | Dynamic resistance | $I_{IO}$ = 1 A, between IO pin and ground | | 1 | | Ω |

## TYPICAL CHARACTERISTICS

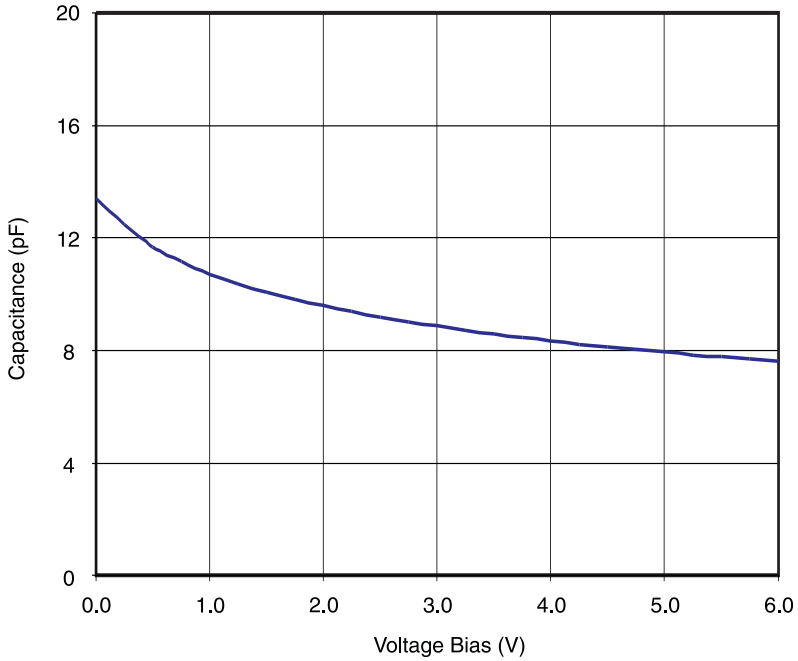



**Figure 1. IO Capacitance vs IO Voltage**

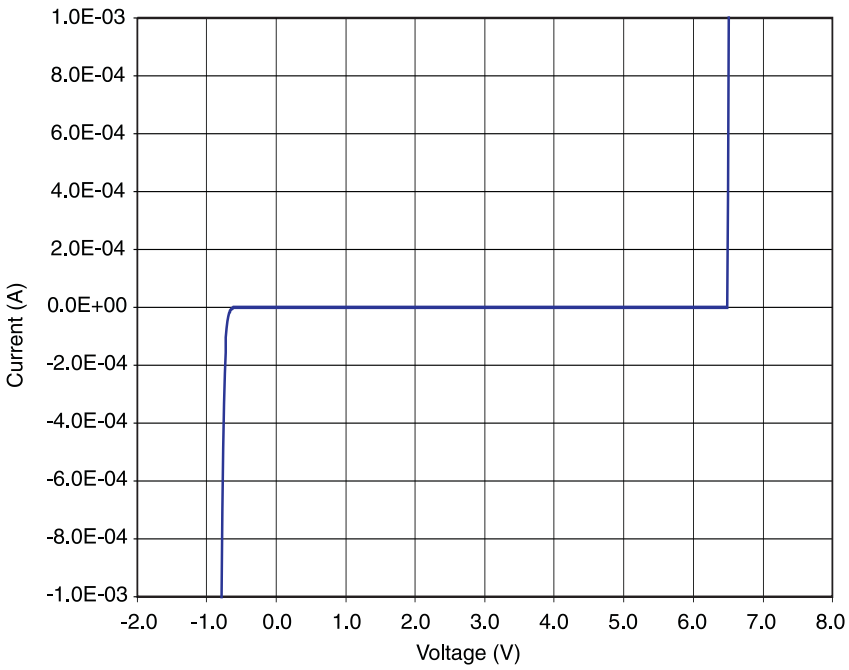



**Figure 2. DC Characteristics**

## TYPICAL CHARACTERISTICS (continued)

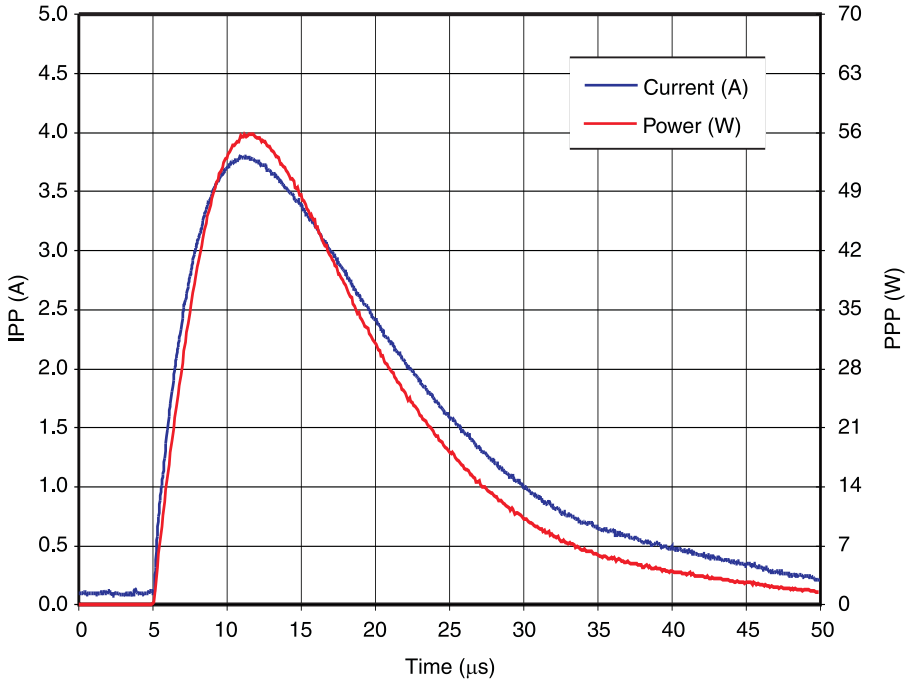



**Figure 3. Peak Pulse Waveforms**

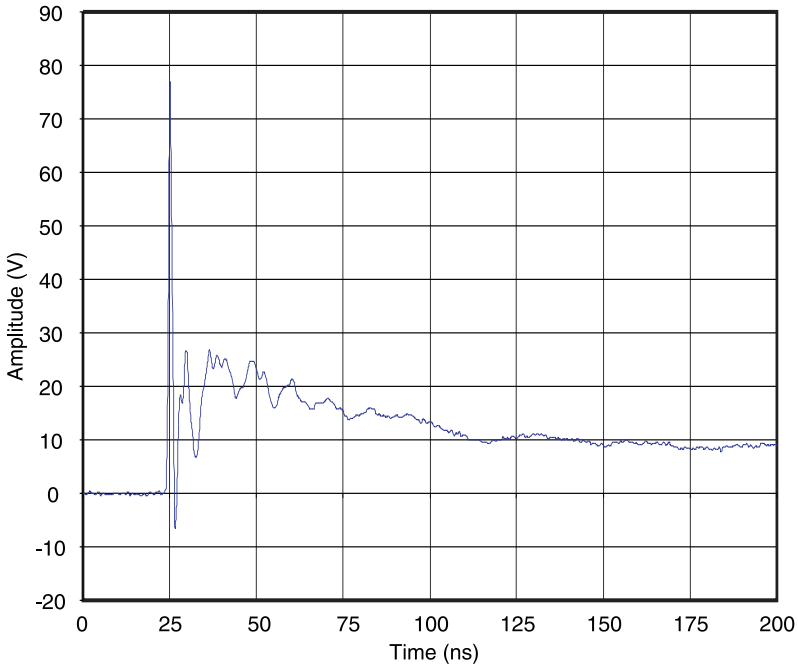



**Figure 4. IEC Clamping Waveforms 8 kV Contact**

## TYPICAL CHARACTERISTICS (continued)

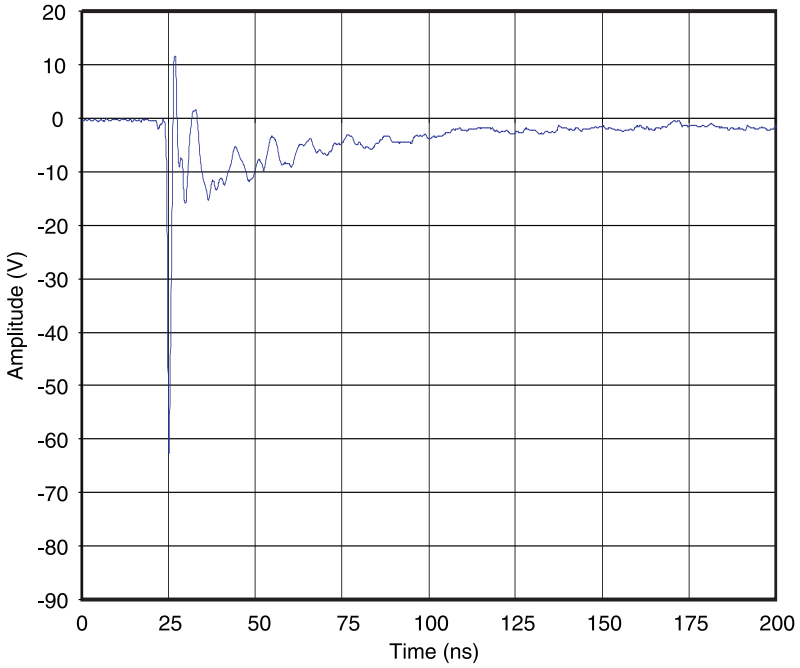



**Figure 5. IEC Clamping Waveforms -8 kV Contact**

## APPLICATION INFORMATION

The TPD8E003 offers eight ESD clamp circuits in a space-saving DQD package. When placed near the connector, the TPD8E003 ESD solution offers little or no signal distortion during normal operation due to low IO capacitance and ultra-low leakage current specifications. The TPD8E003 ensures that the core circuitry is protected and the system is functioning properly in the event of an ESD strike.

For proper operation of the ESD clamps, both during normal function and ESD events, the following layout/design guidelines should be followed:

- Place the TPD8E003 solution close to the connector. This allows the TPD8E003 to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
- It is recommended to employ two signal layers in the printed circuit board (PCB) to route through the eight ESD clamp terminals of the TPD8E003.
- Ensure that there is proper metallization for the GND vertical interconnect access (VIA). During an ESD event, the in-rush current flows to the system GND plane through the GND VIA. Having a low-impedance path allows the current to flow quickly to GND, effectively building a robust, system-level ESD immunity.
- Place the VIA under the DQD pad in locations that offer maximum flexibility in board routing.
- One common set of guidelines (not restricted to all cases)
  - Trace width: 4 mil
  - VIA diameter: 6 mil
  - DQD package pad dimensions: 8 mil × 12 mil

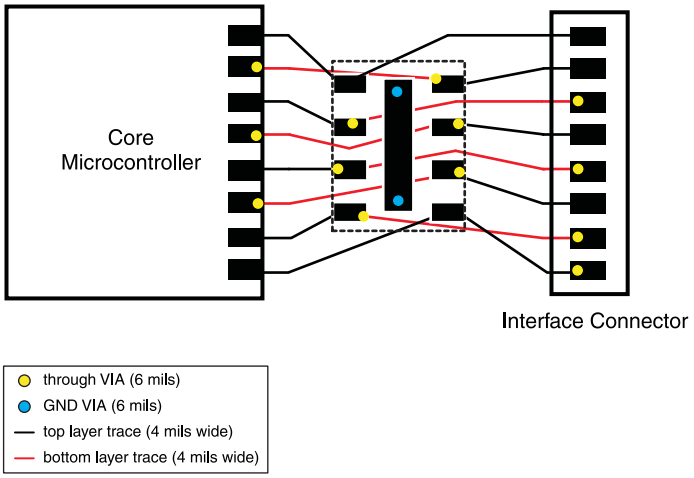
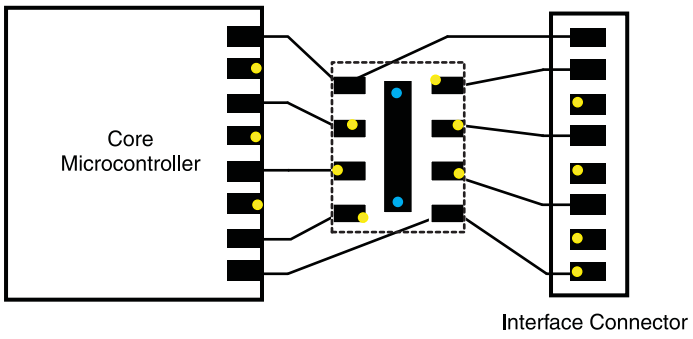
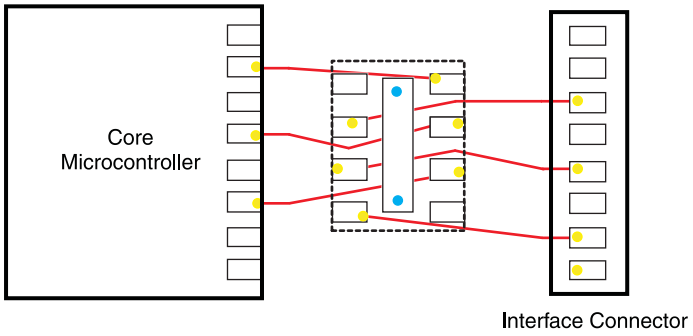



**Figure 6. Board Layout with the TPD8E003DQDR**




**TOP LAYER ROUTING**
**(INCLUDING VIAs)**




**BOTTOM LAYER ROUTING**
**(INCLUDING VIAs)**

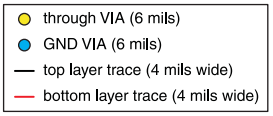



**Figure 7. Top and Bottom Layer Board Layout with the TPD8E003DQDR**

## REVISION HISTORY

**Changes from Original (June 2010) to Revision A** **Page**

- Changed pulse timing from 8/20-ms to 8/20-µs ..... 1

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPD8E003DQDR | ACTIVE | WSON | DQD | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65S | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

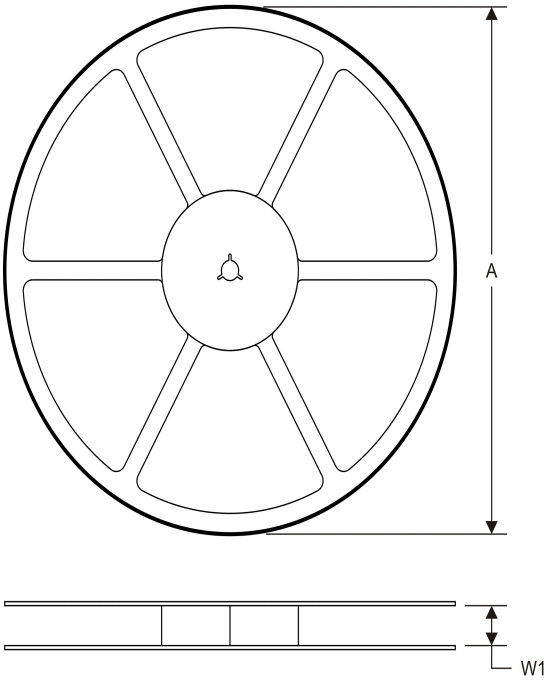
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

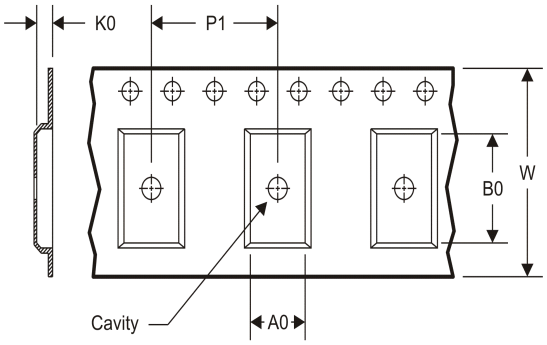
(4) Only one of markings shown within the brackets will appear on the physical device.

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS



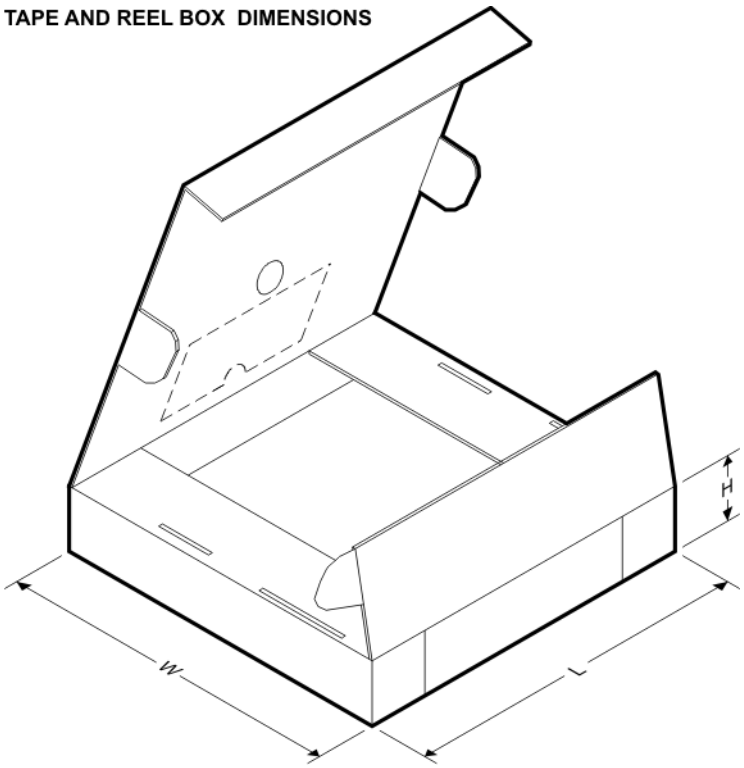

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

### TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPD8E003DQDR | WSON | DQD | 8 | 3000 | 180.0 | 8.4 | 1.65 | 2.0 | 0.95 | 4.0 | 8.0 | Q1 |

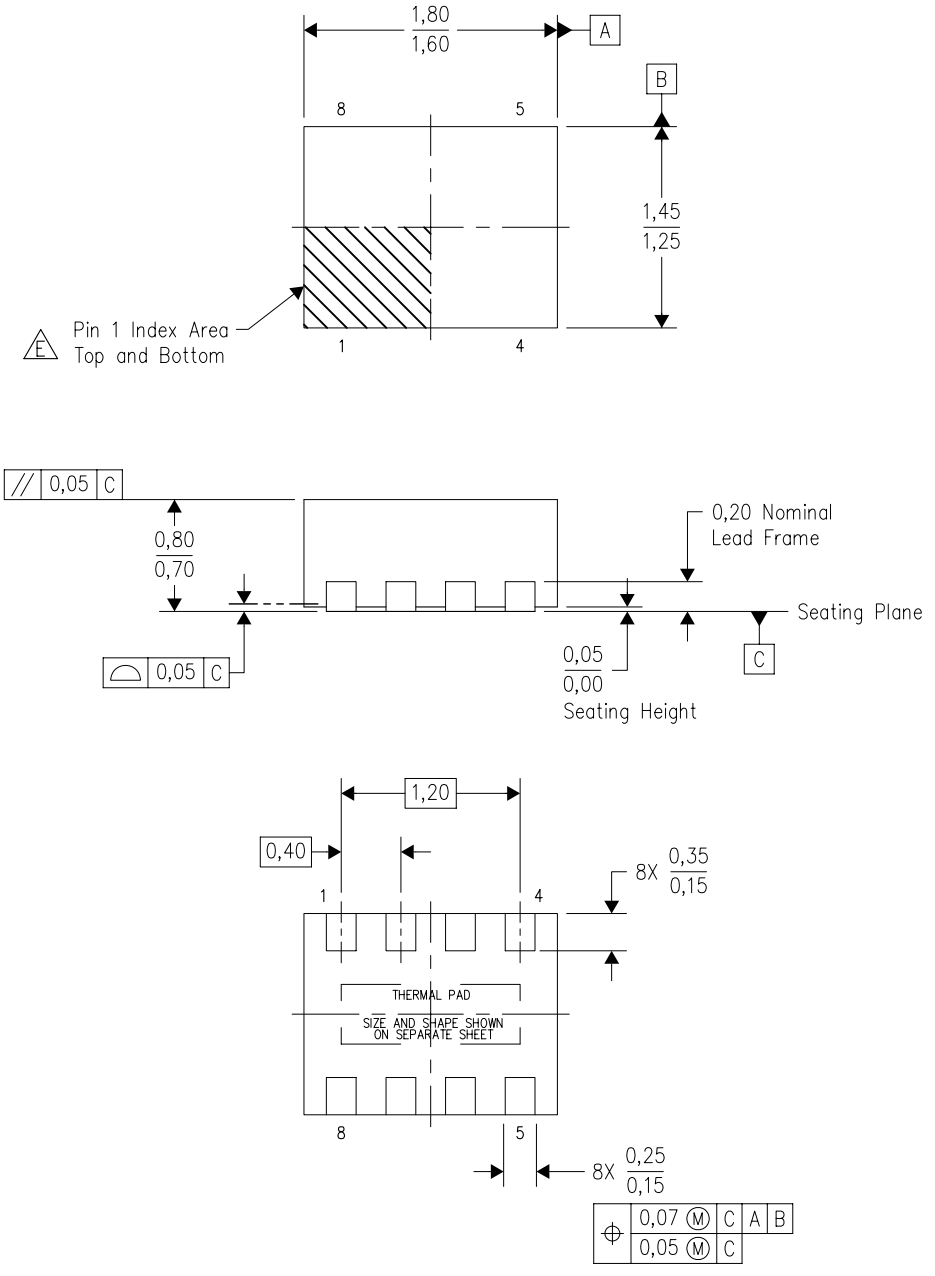
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPD8E003DQDR | WSON | DQD | 8 | 3000 | 202.0 | 201.0 | 28.0 |

DQD (R–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD




Bottom View

4209732–2/C 12/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

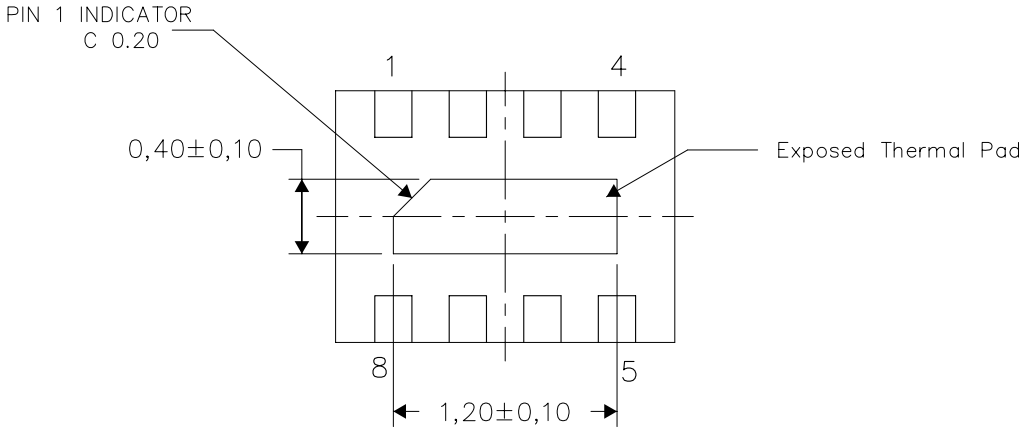
DQD (R–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Bottom View

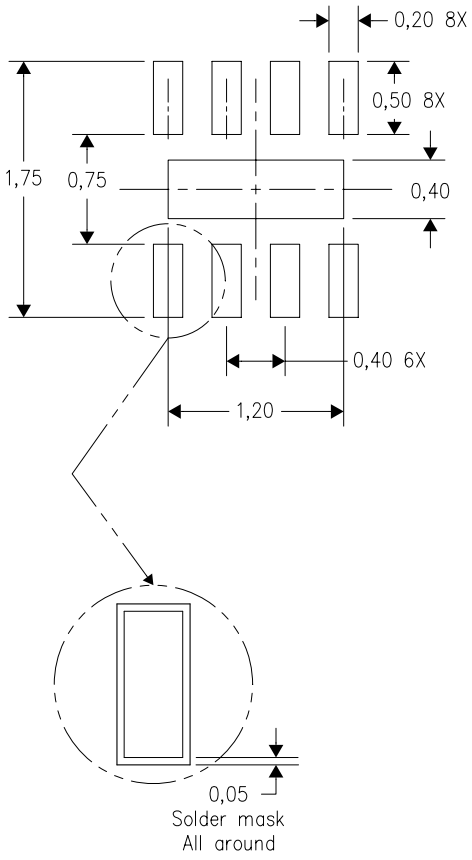
Exposed Thermal Pad Dimensions

4209733–2/C 12/11

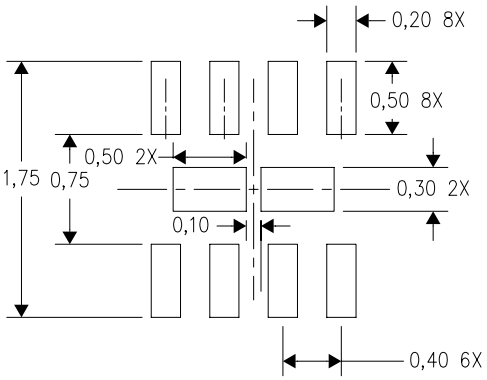
NOTE: All linear dimensions are in millimeters

DQD (R–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

Land Pattern




Stencil Pattern




Exposed Pad solder coverage 62%

4211174–2/B 01/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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