Si4063/Si4463/64/68 TX MATCHING

1. Introduction

This application note describes the matching methods for the TX Power Amplifier (PA) on the Si4063/Si4463/64/68 RFICs. This document does *not* address the matching procedure for the PA on the Si4060/Si4460/61/67 RFICs. Since the output power level on the Si4060/Si4460/61/67 RFIC is considerably lower than on the Si4063/Si4463/64/68 RFIC, the matching procedure is somewhat different. The matching procedure of the Si4060/Si4460/61/67 is described in "AN627: Si4060/Si4460/61/67 Low-Power PA Matching". The cross references in Table 1 list the application note numbers for the different IC types. Table 1 also summarizes the advantages and disadvantages of the different matching methods.

Table 1. Silicon Labs EZRadioPro Sub-GHz Wireless IC Family RF Match Cross References

Match Type	Advantages	Disadvantages	RF IC Types						
			Si4463/64/68 (TRX)	Si4461 (TRX)	Si4460/67 (TRX)	Si4438 (TRX)	Si4063 (TX)	Si4060 (TX)	Si4362 (RX)
Class E Split	High Efficiency, High Power	power varies with VDD, nonlinear power steps	**AN648**, 868/915M 20 dBm & 85 mA	**AN627**, 434/868M 13–16 dBm & 26–43 mA	**AN627**, 434/868/ 915M 10–13 dBm & 16–24 mA	**AN732**, 490 MHz, 20 dBm & 85 mA	**AN648**, 868/915M 20 dBm & 85 mA	**AN627**, 434/868/915M 10–13 dBm & 16–24 mA	—
Class E DT	High Efficiency, High power, One antenna	power varies with VDD, nonlinear power steps	**AN648**, 868/915M 20 dBm & 85 mA	**AN627**, 434/868M 13–16 dBm & 26.5–43 mA	**AN627**, 434/868/ 915M 10–13 dBm & 17–25 mA	**AN732**, 490 MHz, 20 dBm & 85 mA	—	—	—
Class E TX/RX Switch	High Efficiency, One antenna	power varies with VDD, nonlinear power steps, extra RF switch adds cost	**AN648**, 868/915M 20 dBm & 85 mA	—	—	—	—	—	—
SQW DT	High Efficiency, High power, one antenna	power varies with VDD, nonlinear power steps	**AN648**, 169M 20 dBm & 70 mA	—	**AN627**, 169M, 10 dBm & 18 mA	—	—	—	—
SWC SPLIT	Flat VDD characteristic, lower BOM (than class E), linear power steps	less efficient, medium power	—	**AN627**, 868/915M 13–14 dBm & 31–36 mA	**AN627**, 315/ 434/868/ 915M 10 dBm & 24 mA	—	—	**AN627**, 315/434/868/ 915M 10 dBm & 24 mA	—
SWC DT	Flat VDD characteristic, lower BOM (than class E), linear power steps, one antenna	less efficient, medium power	—	**AN627**, 868/915M 13–14 dBm & 31–36 mA	**AN627**, 315/434/868/ 915M 10 dBm & 24 mA	—	—	—	—
4 Element RX Match	Balun with minimum phase and magnitude error, fully matched		—	—	—	—	—	—	**AN643**, 10/13 mA

Follow these steps to achieve several, simultaneous goals with the matching network:

- Target a nominal output power level of +20 dBm (measured at connector to the antenna/load)
- Obtain nominal output power at a nominal supply voltage of V_{DD} = 3.3 V
- Minimize current consumption (i.e., maximize efficiency)
- Constrain the peak voltage at the drain of the output devices
- Comply with ETSI and FCC specifications for spurious emissions

The matching procedures outlined in this document will enable achieving these goals and are applicable for two different types of board configurations: one with separate antennas for the TX and RX paths (split TX/RX board configuration) and one with a single antenna and the TX and RX paths tied directly together without use of an RF switch (direct tie board configuration). The differences in the matching procedure required for the two board configurations are discussed in detail.

Tables 2 through 5 are provided for users who are interested in quickly obtaining matching component values rather than in the methodology used to develop the matching network. The component values shown in these tables are appropriate for a supply voltage of V_{DD} = 3.3 V.

2. Overview of Matching Procedures

The PA circuitry in the Si4063/Si4463/64/68 RFIC is not a conventional power amplifier (e.g., Class A/B/C), but is a “switching power amplifier” or “switching power converter”. Using a switching-type amplifier makes it possible to obtain levels of efficiency not achievable with conventional amplifiers. However, the matching procedure for a switching PA is quite different and may not be immediately intuitive.

The recommended matching approach depends upon the desired frequency of operation. Class-E operation is used at higher operating frequencies, while a customized class termed “Square Wave with Harmonic Termination” is used at lower operating frequencies. (The need for different matching approaches as a function of frequency is discussed in a later section.) Both matching approaches are discussed within this document. The two matching approaches are combined with the two board/antenna configurations (Split TX/RX or Direct Tie) to result in a matrix of four possible reference design topologies.

2.1. Overview of Class-E Matching Procedure

This application note discusses the Class-E matching procedure for the Si4063/Si4463/64/68 RFIC in great detail. However, some readers may be interested in quickly gaining a high-level overview of the procedure before getting into the fine details. For those readers, the main points of the Class-E matching procedure are summarized below:

- Choose L_{CHOKE} (pull-up inductor) for high impedance at Fo
- Choose C_0 (series capacitor)
- Use design equations to calculate L_0 (series inductor) and C_M (shunt capacitor)
- Design a Chebyshev LPF (for attenuation of harmonics)

2.2. Overview of Square Wave Matching Procedure

This application note also discusses the Square Wave matching procedure in considerable detail. The main points of the Square Wave matching procedure are summarized below:

- Choose L_{CHOKE} (pull-up inductor) for high impedance at Fo
- Choose C_0 (series capacitor) for low impedance at Fo
- Design a Chebyshev LPF (for attenuation of harmonics)
- Design L_H-C_H network (to provide good termination at harmonic frequencies)

2.3. Summary of Matching Network Component Values

This section summarizes the resulting component values for the PA matching network for multiple frequencies across the operating range of the Si4063/Si4463/64/68 RFIC.

The matching networks may be realized with either wire-wound SMD inductors or with multi-layer SMD inductors. The cost of a multi-layer inductor is significantly lower than that of a wire-wound inductor, and thus in cost sensitive applications, the multi-layer solution is preferred. However, the performance of a circuit realization using only wire-wound inductors is generally better due to the higher Qs and lower ohmic losses than multi-layer inductors of equivalent value. The component values shown here are for a solution using wire-wound inductors such as the 0402HP-series of wire-wound inductors from CoilCraft or the LQW15A or LQW18A series of wire-wound inductors from Murata. Due to the increased loss, a realization using multi-layer inductors typically exhibits a slight increase in current consumption for the same amount of output power.

2.3.1. Component Values for Class-E Split TX/RX Board Configuration

Table 2 provides the component values required for a Class-E match using the Split TX/RX board configuration of and a supply voltage of V_{DD} = 3.3 V.

Table 2. Class-E Match Component Values vs. Frequency (Split TX/RX Board)

Freq Band	Lchoke	L0	C0	CM	LM1	CM1	LM2	CM2	LM3
434 MHz	220 nH	33 nH	9.1 pF	15 pF	30 nH	12 pF	36 nH	10 pF	22 nH
460 MHz	220 nH	30 nH	8.2 pF	12 pF	27 nH	10 pF	36 nH	8.2 pF	22 nH
868 MHz	100 nH	15 nH	3.0 pF	5.1 pF	12 nH	3.3 pF	12 nH	N/F	0 Ω
915 MHz	100 nH	13 nH	3.3 pF	4.7 pF	11 nH	3.3 pF	10 nH	N/F	0 Ω
950 MHz	100 nH	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

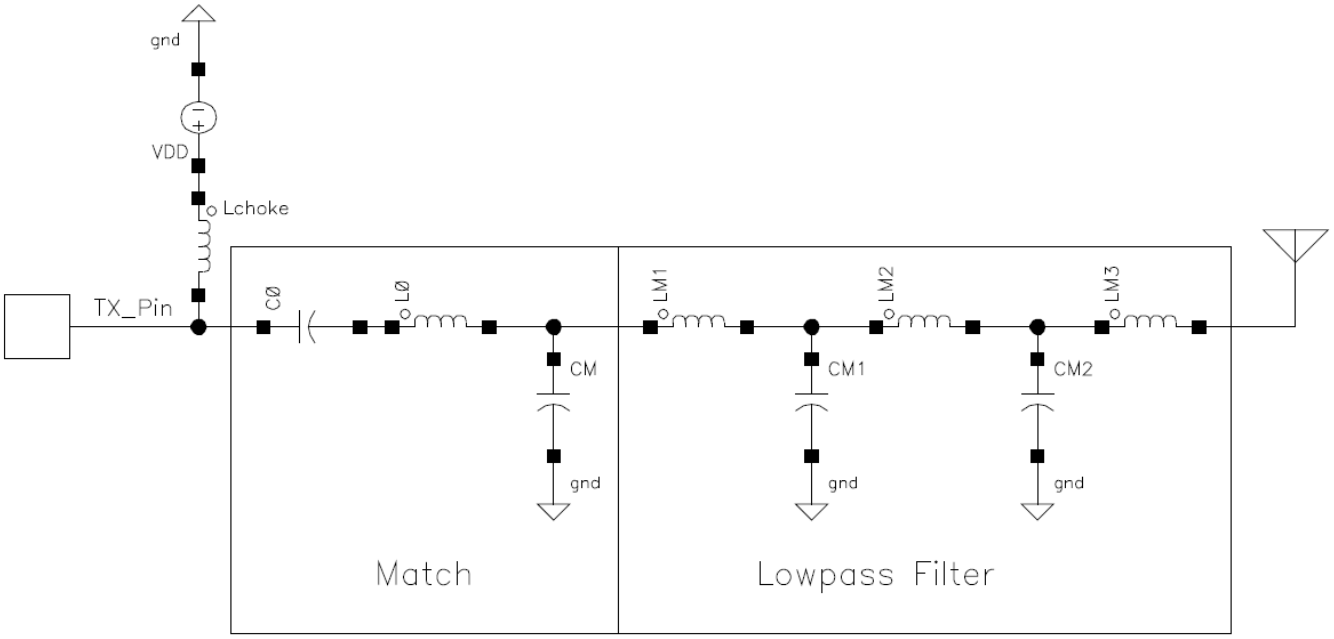

Figure 1. Class-E Matching Topology for Split TX/RX Board Configuration

2.3.2. Component Values for Direct Tie Board Configuration

Table 3 provides the component values required for a Class-E match using the Direct Tie board configuration and a supply voltage of V_{DD} = 3.3 V.

Table 3. Class-E Match Component Values vs. Frequency (Direct Tie Board)

Freq Band	RX Side				TX Side							
	LR1	LR2	CR1	CR2	Lchoke	L0	C0	LM1	CM1	LM2	CM2	LM3
434 MHz	62 nH	56 nH	4.7 pF	2.2 pF	220 nH	TBD	TBD	TBD	TBD	TBD	TBD	0 Ω
460 MHz	56 nH	51 nH	3.9 pF	2.2 pF	220 nH	TBD	TBD	TBD	TBD	TBD	TBD	0 Ω
868 MHz	20 nH	24nH	3.0 pF	1.0 pF	100 nH	TBD	TBD	TBD	TBD	TBD	TBD	0 Ω
915 MHz	18 nH	22 nH	3.0 pF	1.0 pF	100 nH	TBD	TBD	TBD	TBD	TBD	TBD	0 Ω
950 MHz	18 nH	22 nH	2.4 pF	0.9 pF	100 nH	TBD	TBD	TBD	TBD	TBD	TBD	0 Ω

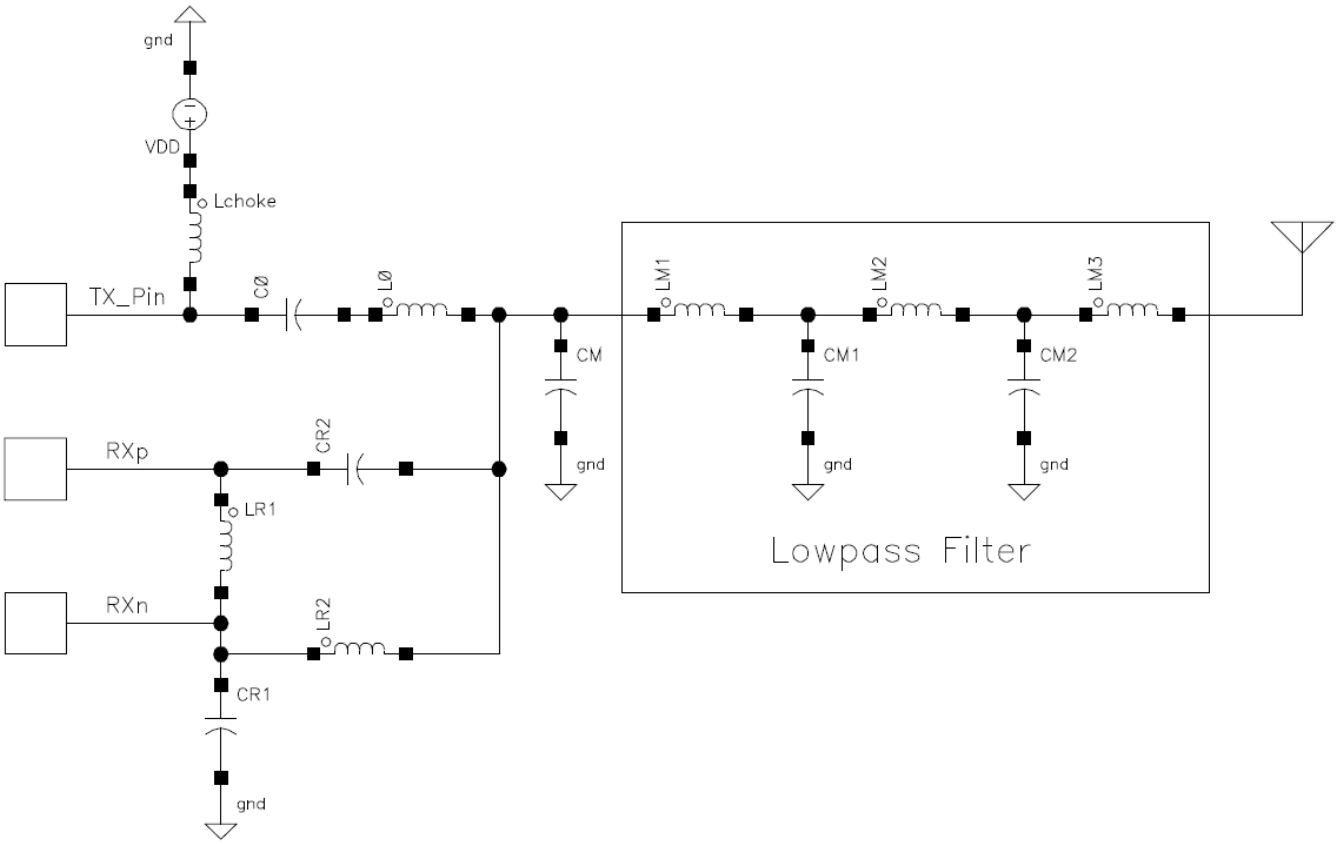

Figure 2. Class-E Matching Topology for Direct Tie Board Configuration

2.3.3. Component Values for Square Wave Split TX/RX Board Configuration

Table 4 provides the component values required for a Square Wave match using the Split TX/RX board configuration of Figure 3 and a supply voltage of V_{DD} = 3.3 V.

Table 4. Square Wave Match Component Values vs. Frequency (Split TX/RX Board)

Freq Band	Lchoke	C0	L_H	C_H	R_H	LM1	CM1	LM2/ CLM2	CM2	LM3/ CLM3	CM3	LM4
169 MHz	390 nH	470 pF	82 nH	11 pF	50	47 nH	18 pF	68 nH 3.0 pF	18 pF	47 nH 2.0 pF	11 pF	27 nH
315 MHz	330 nH	270 pF	TBD	TBD	50	TBD	TBD	TBD	TBD	TBD	TBD	TBD
390 MHz	330 nH	220 pF	TBD	TBD	50	TBD	TBD	TBD	TBD	TBD	TBD	TBD
434 MHz	270 nH	150 pF	TBD	TBD	50	TBD	TBD	TBD	TBD	TBD	TBD	TBD

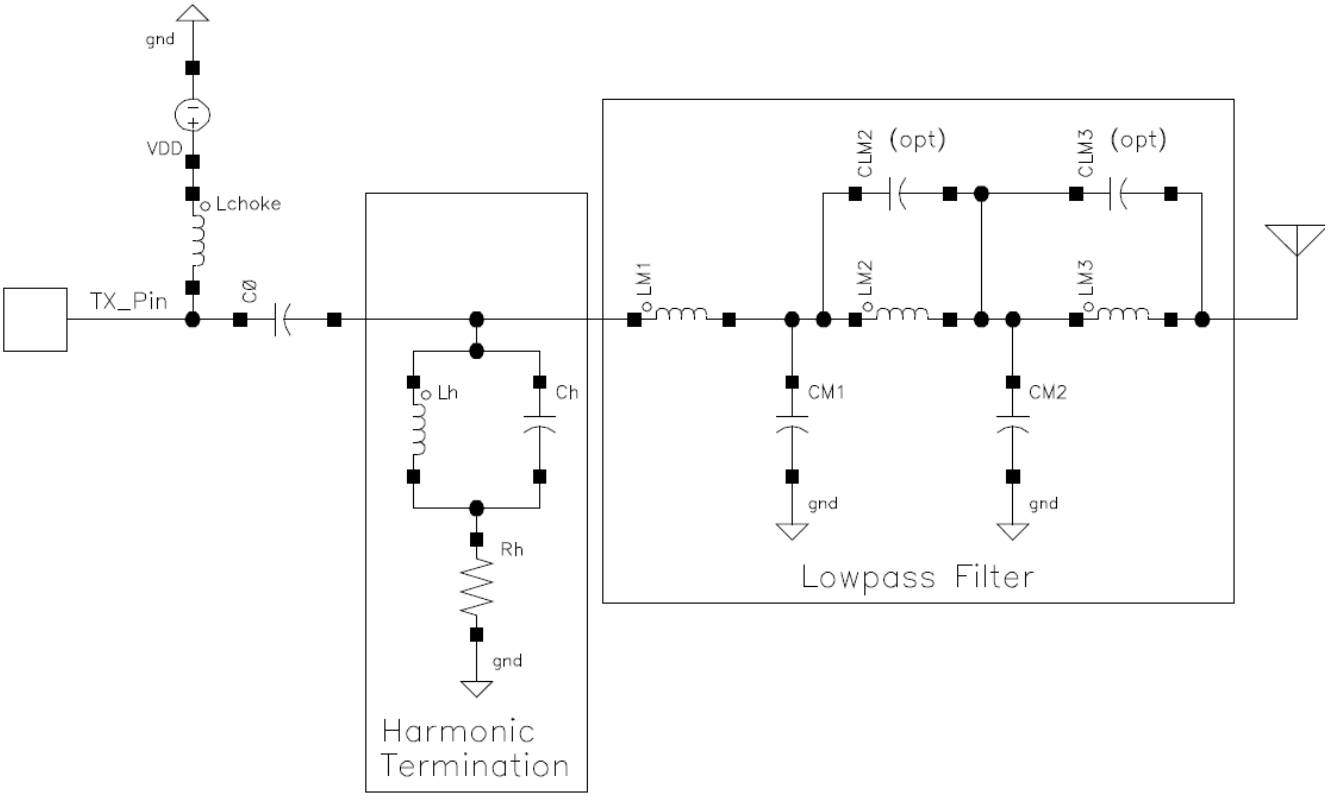

Figure 3. Square Wave Matching Topology for Split TX/RX Board Configuration

2.3.4. Component Values for Square Wave Direct Tie Board Configuration

Table 5 provides the component values required for a Square Wave match using the Direct Tie board configuration of Figure 4 and a supply voltage of V_{DD} = 3.3 V.

Table 5. Square Wave Match Component Values s. Frequency (Direct Tie Board)

Freq Band	RX Side				TX Side									
	LR1	LR2	CR1	CR2	Lchoke	C0	LH/CH	LM1	CM1	LM2/ CLM2	CM2	LM3/ CLM3	CM3	LM4
169 MHz	220 nH	150 nH	12.0 pF	6.2 pF	330 nH	470 pF	82 nH 11 pF	47 nH	18 pF	68 nH 3.0 pF	18 pF	47 nH 2.0 pF	11 pF	27 nH
315 MHz	TBD	TBD	TBD	TBD	330 nH	TBD	TBD	TBD	TBD	TBD	TBD	0 nH	TBD	TBD
390 MHz	TBD	TBD	TBD	TBD	270 nH	TBD	TBD	TBD	TBD	TBD	TBD	0 nH	TBD	TBD
434 Hz	TBD	TBD	TBD	TBD	220 nH	TBD	TBD	TBD	TBD	TBD	TBD	0 nH	TBD	TBD

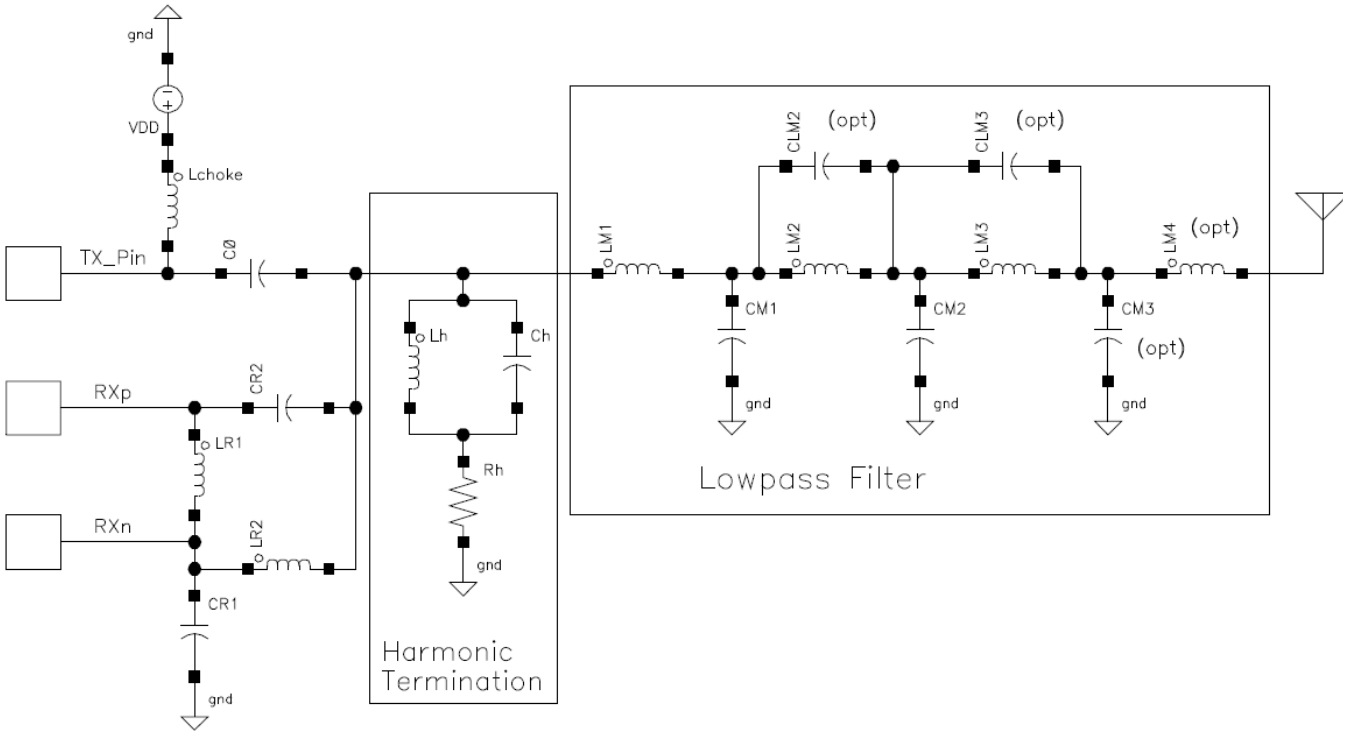

Figure 4. Square Wave Matching Topology for Direct Tie Board Configuration

Surface-mount 0603-size or 0402-size components contain parasitic elements that modify their effective values at the frequency of interest. It is convenient to use the nearest-available 5% or 10% component values rather than the exact component values predicted by Filter Design CAD software or filter prototype tables. Additionally, any printed circuit board layout has parasitics, such as trace inductance, component pad capacitance, etc., which means that it will be necessary to “tweak” the final matching values for the reader’s specific application and board layout. The above component values should be used as starting points and the values modified slightly to zero-in on the best filter response and impedance match to 50 Ω.

3. Power Amplifier Circuit Description

RF design engineers are familiar with matching conventional (Class A/B/C) power amplifiers. In such cases, the matching procedure is relatively simple: provide a load impedance that is the complex conjugate of the output impedance of the PA. The user may also employ Load Pull techniques in which a match is found that optimizes the output power but differs from the complex conjugate of the PA output impedance. In these conventional classes of power amplifiers, the output waveform ranges from a full 360 degree copy or reproduction of the driving waveform (e.g., Class A) to a partial (less than 360 degree) reproduction of the driving waveform (e.g., Class B or Class C).

As mentioned previously, the PA circuitry in the Si4063/Si4463/64/68 RFIC differs considerably from such a conventional power amplifier. The Si4063/Si4463/64/68 RFIC uses a type of PA circuit called a “switching power amplifier” or “switching power converter”. The theory of operation of such amplifiers is discussed briefly in this document; for a deeper theoretical understanding (including derivation of the design equations for Class-E amplifiers), the following papers are recommended:

- *Class E – A New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers*, N. Sokal and A. Sokal, IEEE Journal of Solid State Circuits, Vol. SC-10, No. 3, June 1975.
- *Idealized Operation of the Class-E Tuned Power Amplifier*, F. Raab, IEEE Transactions on Circuits and Systems, Vol. CAS-24, No. 12, December 1977.

3.1. Theory of Operation of an Ideal Switching PA

The switch is the core component of a switching PA. In the Si4063/Si4463/64/68, the switch is provided by an NMOS cascode transistor in an open-drain configuration, sized to handle the current required for the specified output power.

Figure 5 shows the typical matching circuitry necessary to extract RF power from a switching amplifier when matched for Class-E operation. The value of the pull-up inductor L_{CHOKE} is chosen to be a very large impedance at the frequency of operation (and its nearest harmonics), while the series-resonant output tank (L_0-C_0) is chosen to resonate at the frequency of operation. The shunt capacitance C_{SHUNT} is required to store energy during the switching cycle. This shunt capacitance also works with matching components L_X and C_X to tailor the time-domain shape of the output waveform. It is important to understand that optimization of the efficiency of a switching-type amplifier requires control of the time-domain shape of the output waveform.

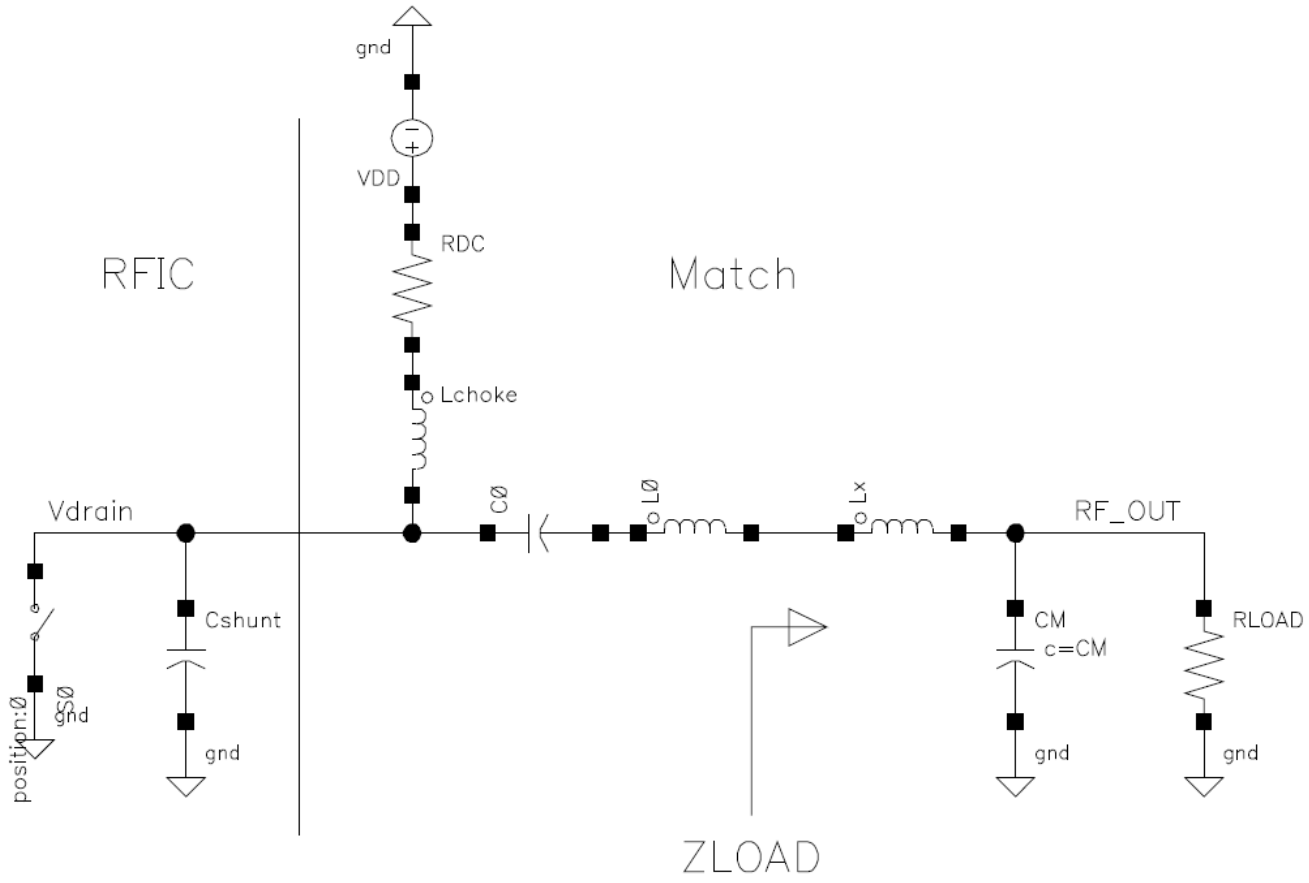

Figure 5. Basic Switching PA Circuit Topology

From purely a technical standpoint, a switch does not “amplify” an RF signal. As long as the input control signal to the switch is sufficient in amplitude to toggle the switch between its ON and OFF states, the output waveform remains the same. The amount of output power delivered to the load resistance is therefore independent of the amplitude of the input control signal (i.e., amplitude of the RF signal at the gate of the output MOS device). In such a case, defining the “gain” or amplification factor of the PA is no longer relevant. It is more accurate to refer to this circuit as a “power converter” rather than a “power amplifier.”

In an ideal switching PA matched for Class-E operation, the level of output power is dependent primarily upon three parameters: 1) the dc supply voltage, 2) the shunt output capacitance, and 3) the operating frequency. The relationship between these parameters and the output power is shown in Equation 1. (The derivation for design equations is not provided within this document; refer to the papers listed above for detailed explanation of the operational theory.)

$$P_{OUT} = \pi\omega_o C_{SHUNT} V_{DD}^{2}$$

Equation 1.

As shown in Equation 1, the output power is not a function of the load impedance. As will be shown later, it is necessary to present the correct value of load impedance to the device in order to obtain Class-E operation. However, once this load impedance is provided, the output power is adjusted either by increasing the supply voltage or by increasing the shunt capacitance C_{SHUNT} at the output of the switching device.

Furthermore, it is theoretically possible to achieve 100% efficiency in an ideal switching PA. This is a significant difference from conventional PAs. It is easily shown that the theoretical maximum efficiency of a Class-A PA is

50%, 78.5% for Class-B, and so on. However, it is possible to tailor the output waveform in a switching PA such that the voltage across the switch is always zero during any period of time that the switch is conducting current, and the current conducted by the switch is always zero during any period of time that the voltage across the switch is non-zero. Thus the power dissipated by the switching device is zero, and the efficiency approaches 100% (in the absence of any other losses in the circuit). This waveform is illustrated in Figure 6, which shows that non-zero values of the voltage and current waveforms never occur at the same time.

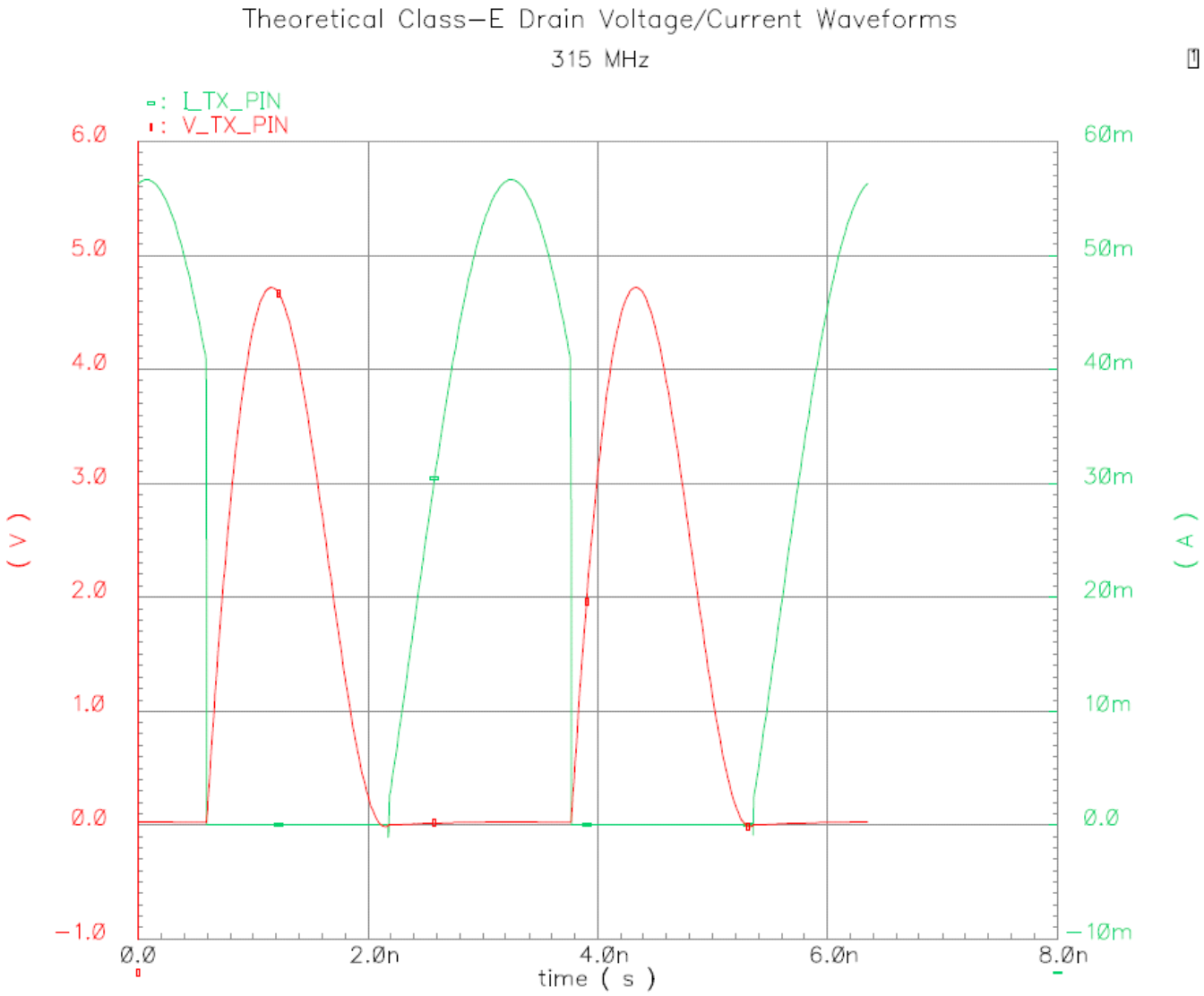

Figure 6. Theoretical Class-E Drain Voltage/Current Waveforms

3.2. Limitations of a Practical MOS Switching PA

There is no theoretical limit to the amount of power that may be extracted from an ideal switching PA. In practice, several factors prevent achieving “ideal” operation. These factors include the maximum operating voltage of the switch (i.e., MOS output device), the maximum current (limited by the size of the MOS output device), ON and OFF state resistances of the MOS output device, non-zero switching times of the MOS output device, and losses in the output matching components due to finite Qs. All of these factors combine to limit the achievable output power and efficiency.

The limitation on the maximum drain voltage of the MOS output device turns out to be a considerable constraint. RF design engineers may be quite familiar with the waveforms obtained with inductively-loaded conventional PAs, where the peak output voltage reaches a value equal to twice the dc supply voltage. However, the peak of the output voltage waveform in a switching PA may far exceed this “$2xV_{DD}$” guideline. As is shown in the papers listed above, the peak drain voltage for a Class-E switching amplifier can reach $3.56xV_{DD}$.

The operational range of supply voltage for the Si4063/Si4463/64/68 RFIC is specified as V_{DD} = 1.8 V to 3.6 V. It is apparent that if the switching PA circuit was matched for Class-E operation at V_{DD} = 3.6 V, the resulting peak drain voltage would reach 12.8 V peak. This would appear to exceed the maximum voltage at which the MOS devices can operate without damage. However, there are several mechanisms which work to allow safe operation, even at the maximum specified V_{DD} supply voltage. Internally, the PA is designed as a cascode structure, and thus the total signal swing does not appear across one device but instead is divided across several devices. Additionally, the ON-state resistance of the output devices is not zero; this resistance acts as a loss mechanism to further reduce the voltage swing across the internal device(s). As a result, Class-E matching and operation may be safely recommended for the Si4063/Si4463/64/68 RFIC.

The size of the MOS output device has the effect of limiting the amount of output power that can be extracted from a practical switching PA. In an ideal switching PA, the output power may be increased by either raising the supply voltage or by increasing the value of shunt output capacitance. As just discussed, an increase in supply voltage results in an increase in peak drain voltage swing, and thus the supply voltage may not be raised indefinitely. Increasing the shunt output capacitance is therefore the only remaining option by which the output power may be increased, which has the effect of requiring greater current handling capability in the switching device. While an ideal switch may carry an infinite amount of current, a practical MOS switch cannot. The size of the MOS output device in the Si4063/Si4463/64/68 RFIC is carefully designed to carry sufficient current to achieve its maximum specified output power; however, this level of current-handling capability is only available when the RFIC is commanded to its maximum TX output power mode (by the DDAC[6:0] field in the PA_PWR_LVL property 0x2201). The Si4063/Si4463/64/68 RFIC achieves a reduction in output power by reducing the number of active fingers (i.e., size) of the MOS output device; this effectively limits the current-handling ability of the output device to less than that desired by the combination of supply voltage and output capacitance. For example, at the maximum setting(s) of the DDAC[6:0] field, the PA output devices behave much like a switch, but at the lower settings of the DDAC[6:0] field, the output devices behave more like a switch in series with a non-negligible resistance.

4. Class-E Matching Procedure for the Si4063/Si4463/64/68

As discussed above, the cascode design of the PA output devices in the Si4063/Si4463/64/68 RFIC allows for Class-E operation without exceeding safe levels of peak drain voltage swing. Additionally, the Si4063/Si4463/64/68 RFIC contains internal diode voltage clamps on the drain node of the MOS output device. The purpose of these diode clamps is to limit brief excursions of excess peak drain voltage. Such variations in peak drain voltage may occur if the antenna load impedance varies considerably from 50 Ω (e.g., turning on the TX output without an antenna connected, etc.).

This application note is targeted at applications which require +20 dBm output power. While this level of output power is readily achievable, meeting ***all*** design constraints requires careful attention to matching component selection and good board layout techniques. It is possible to fall short of one or more design goals through poor design and board layout practices.

4.1. Overview of Class-E Matching Procedure

4.1.1. Split TX/RX Board Configuration

The following steps provide a broad overview of the matching methodology for Class-E operation on the Split TX/RX board configuration. Further details of each step will be provided later in this application note.

1. Choose L_{CHOKE} (pull-up inductor) for high impedance at Fo (and its nearest harmonics).
2. Choose/calculate values for series-resonant tank L_0-C_0 such that L_0-C_0 resonates at Fo.
3. Calculate required value of Z_{LOAD}, given the desired frequency of operation (Fo) and the shunt drain capacitance (C_{SHUNT} = ~2.5 pF on the Si4063/Si4463/64/68).
4. Calculate required value for the voltage-limiting resistor R_{DC}, given the desired output power and V_{DD} supply voltage.
5. Calculate values for matching components L_X and C_M, given the antenna load resistance (e.g., R_{ANT} = 50 Ω) and the calculated value for Z_{LOAD}.
6. Design a low-pass filter to provide sufficient attenuation of harmonic signals.

4.1.2. Direct Tie Board Configuration

The following steps provide a broad overview of the matching methodology for Class-E operation on the Split TX/RX board configuration. Further details of each step will be provided later in this application note.

1. Repeat Steps 1 through 6, as shown above.
2. Construct a 4-element balun match to the differential RXp/RXn LNA input pins, using the methodology outlined in “AN643: Si446x/Si4362 RX LNA Matching”.
3. Connect the TX and RX paths together, and deliberately mis-tune L_0 by increasing its value by approximately 20% above its calculated optimum value.

4.2. Detailed Class-E Matching Procedure for Split TX/RX Board Configuration

This section provides further detail about each step of the Class-E Split TX/RX matching procedure outlined above. A supply voltage of V_{DD} = 3.3 V is assumed.

4.2.1. Step #1: Select a Value for L_{CHOKE} Pull-Up Inductor

In Step #1, an appropriate value is selected for the pull-up inductor L_{CHOKE}.

In the theoretical derivation for Class-E switching amplifiers, the desired impedance of the pull-up inductor L_{CHOKE} is zero at dc and infinite at all other frequencies. This impedance characteristic is not achievable in practice; however, a large value of inductance provides a reasonable approximation of this performance. The value of L_{CHOKE} should be chosen such that it provides a high impedance at not only the fundamental operating frequency, but also at the first few harmonic frequencies. The inductance value should not be so large as to already be at (or past) parallel self-resonance at the desired operating frequency. The exact inductance value is not critical; however, Silicon Labs recommends the following range of inductance values (assuming 0402-size or 0603-size inductors) as a function of the desired operating frequency:

- 315 MHz: approximately 390 nH
- 470 MHz: approximately 220 nH
- 915 MHz: approximately 100 nH

4.2.2. Step #2: Choose/Calculate Values for L_0-C_0 Series-Resonant Tank

In Step #2, the L_0-C_0 tank is designed to be series-resonant at the desired operating frequency Fo.

There are infinite combinations of L_0-C_0 values that can achieve resonance at a desired frequency. However, certain broad guidelines may be used to select one particular solution of component values.

First, the inductance and capacitance values should be neither extremely large or extremely small. Discrete inductors and capacitors with extremely large values are subject to degrading effects due to self-resonance. Discrete components with extremely small values are also subject to degrading effects due to component tolerance. In either case, the actual resonant frequency of the tank may be significantly different than the frequency predicted by mathematical calculations.

Second, in the theoretical derivation for Class-E switching amplifiers, it is desired that the impedance of the L_0-C_0 series-resonant tank be zero at Fo and infinite at all other frequencies. This impedance characteristic is not achievable in practice; however, a reasonable approximation of this performance may be obtained by using values with a high L-to-C ratio.

Third, it is desirable to minimize the insertion loss of the resonant tank. As the quality factor (Q) of discrete inductors is generally much lower than that of discrete capacitors, it is important to select an L_0-C_0 ratio that maximizes the inductor Q. The Q of discrete inductors generally increases as the inductance value is also increased, until the inductance approaches the value where self-resonance becomes a concern.

Finally, it is desirable to select component values that are near standard 5% tolerance values.

These considerations lead to the following guidelines for selecting the values for L_0-C_0:

- The L_0-C_0 tank must resonate at Fo
- The value of L_0 should be chosen as large as possible, while remaining low enough that effects of self-resonance are not an issue and are close to standard 5% tolerance values

Assuming a desired operating frequency of Fo = 470 MHz as an example, these guidelines lead to selection and/or calculation of the following values for L_0-C_0:

- C_0 = 8.2 pF (chosen)
- L_0 = 13.903 nH (calculated)

4.2.3. Step #3: Calculate the Required Value for Z_{LOAD}

In Step #3, the required value of load impedance is calculated. This represents the impedance that must be presented to the output of the L_0-C_0 resonant tank, and is calculated at the fundamental operating frequency Fo.

In the theoretical derivation for Class-E switching amplifiers, the required load impedance (Z_{LOAD}) is a function of shunt drain capacitance (C_{SHUNT}) and operating frequency ($\omega_o = 2\pi Fo$) as follows:

$$Z_{LOAD(fund)} = \left(\frac{0.2815}{\omega_o C_{SHUNT}}\right) e^{j \times 49.0524°}$$

Equation 2.

This equation states that the required load impedance (Z_{LOAD}) does not vary with the desired level of output power, but depends only on the desired operating frequency and value of shunt drain capacitance. The value of internal shunt drain capacitance C_{SHUNT} is a design parameter of the Si4063/Si4463/64/68 RFIC and is not adjustable by the user. This shunt capacitance is composed primarily of the drain-source capacitance (C_{ds}) of the output MOS devices. Silicon Labs states that the value of this internal shunt drain capacitance is approximately:

C_{SHUNT} ~ 2.5 pF

Assuming a desired operating frequency of Fo = 470 MHz as an example, the following value for Z_{LOAD} may be calculated:

$$Z_{LOAD(315M)} = \left(\frac{0.2815}{2\pi \times 470M \times 2.5pF}\right) e^{j \times 49.0524°} = 24.87 + j28.66\Omega$$

Equation 3.

This value of load impedance (Z_{LOAD}) is ***not*** the same parameter as the antenna impedance (Z_{ANT}), nor do they necessarily have the same ohmic value. A matching network must be constructed that transforms the arbitrary value of antenna impedance Z_{ANT} into the required value of load impedance Z_{LOAD}, as seen at the output of the L_0-C_0 resonant circuit.

4.2.4. Step # 4: Calculate the Required Value for Voltage-Limiting Resistor R_{DC}

In Step #4, the value of the voltage-limiting resistor R_{DC} required for the desired output power is calculated, given a specified value of PA supply voltage (V_{DD_PA}).

Equation 1 shows that, for a given desired operating frequency, the only “knob” remaining to adjust the output power is the PA supply voltage V_{DD_PA}, as the value of C_{SHUNT} is an internal chip design parameter and is not adjustable by the user. This equation is solved for V_{DD_PA} and found to be:

$$V_{DD\_PA} = \sqrt{\frac{P_{OUT}}{\pi \omega_o C_{SHUNT}}}$$

Equation 4.

Continuing the design example of 470 MHz and assuming a desired output power of +20 dBm (100 mW), the required value of V_{DD_PA} may be calculated:

$$V_{DD\_PA} = \sqrt{\frac{0.1}{2\pi^2 \times 470M \times 2.5pF}} = 2.076V$$

Equation 5.

This equation states that if the voltage supplied to the top of pull-up inductor L_{CHOKE} is equal to 2.076 V and the previously-calculated value of load impedance Z_{LOAD} is presented to the chip, the resulting output power will be P_{OUT} = 100 mW = +20 dBm.

This required PA supply voltage (V_{DD_PA}) is significantly different than the general supply voltage (V_{DD}) for the rest of the RFIC. It is obviously not desirable to maintain two separate, independent sources of supply voltage for the RFIC; however, the PA output supply voltage can be easily created from the main supply voltage by means of an I-R voltage drop across a resistor. This supply voltage drop is accomplished by resistor R_{DC} as shown in Figure 3. As the *theoretical* efficiency of a Class-E switching amplifier is 100%, the average PA drain current I_{DD_PA} may be calculated as:

$$P_{OUT} = \pi\omega_o C_{SHUNT} V_{DD\_PA}^2 = I_{DD\_PA} V_{DD\_PA}$$

Equation 6.

This equation may be solved for I_{DD_PA} to obtain:

$$I_{DD\_PA} = \pi\omega_o C_{SHUNT} V_{DD\_PA}$$

Equation 7.

Given the main supply voltage for the remainder of the chip (V_{DD}), and having previously calculated the required value of PA supply voltage (V_{DD_PA}) and average PA drain current (I_{DD_PA}), the required value for R_{DC} can be calculated as follows:

$$R_{DC} = \frac{V_{DD} - V_{DD\_PA}}{I_{DD\_PA}}$$

Equation 8.

Continuing the design example of 470 MHz for +20 dBm output power, the following calculations are made:

$$I_{DD\_PA} = 2\pi^2 \times 470M \times 2.5pF \times 2.076V = 48.16mA$$

Equation 9.

Assuming a general chip supply voltage of V_{DD} = 3.3 V, the required value of R_{DC} may be calculated as:

$$R_{DC} = \frac{3.3 - 2.076}{0.04816} = 25.41\Omega$$

Equation 10.

This value of resistance must be placed in series with L_{CHOKE} in order to drop the general chip supply voltage down to the value required to obtain the desired output power.

However, these calculations for the value of R_{DC} assume theoretically-ideal Class-E operation. In practice, the circuit will not behave exactly as predicted by these equations due to non-idealities such as non-zero ON-state resistance, finite OFF-state resistance, non-zero switching times, and loss in the external matching components. As a result, the output power obtained for a given value of V_{DD} supply voltage will almost certainly be slightly less than predicted by theory. Stated another way, it will almost always be necessary to use a smaller value of R_{DC} than predicted by theory in order to obtain the desired value of output power. Some amount of post-calculation "tweaking" of the component values is considered a normal part of the PA matching process.

4.2.5. Step #5: Calculate the Values for Matching Components L_X and C_M

In Step #5, the values of the matching components (L_X and C_M) required to transform the given antenna impedance (Z_{ANT}) into the required load impedance (Z_{LOAD}) are calculated.

This matching effort may be accomplished by simple and normal design methods, such as use of a Smith Chart or impedance matching CAD software (e.g., WinSmith™). Continuing the design example for 470 MHz and assuming an antenna impedance of $Z_{ANT} = R_{ANT} = 50\ \Omega$, it is found that a shunt capacitance $C_M = 6.81$ pF and series inductance $L_X = 18.17$ nH is required to transform $R_{ANT} = 50\ \Omega$ to the required value of $Z_{LOAD} = 24.87 + j\ 28.66\ \Omega$. The resulting circuit topology is shown in Figure 5.

This is only one possible solution for the required impedance transformation; other matching topologies could have been used as well. The user should also note that the required L_X-C_M match topology depends upon the real part of the load impedance, $Re(Z_{LOAD})$. In this example, the real part of the load impedance was less than 50 Ω and thus an appropriate matching topology consisted of a shunt capacitor (C_M) and a series inductor (L_X). In the event that $Re(Z_{LOAD})$ had been greater than 50 Ω, an appropriate matching topology would have consisted of first a series inductor (L_X) followed by a shunt capacitor (C_M).

Series inductors L_0 and L_X may be combined into one equivalent inductor with a value equal to the sum of their individual inductances, in order to reduce Bill of Materials (BOM) cost. This is a normal and usual practice.

In the example shown here, the following component values were obtained through use of the above design equations:

- Fo = 470 MHz
- $P_{OUT(TARGET)} = +20$ dBm
- $V_{DD} = 3.3$ V
- $C_{SHUNT} = 2.5$ pF
- $L_{CHOKE} = 220$ nH
- $R_{DC} = 25.41\ \Omega$
- $C_0 = 6.81$ pF
- $L_0+L_X = 32.15$ nH
- $C_M = 6.81$ pF

In practice, these exact values would be rounded to the nearest available 5% tolerance parts (e.g., $L_0+L_X = 30$ nH, $C_M = 6.8$ pF, R_{DC}=24 Ω).

4.2.6. Step #6: Design a Lowpass Filter

In Step #6, a low-pass filter network is designed in order to attenuate the harmonics below the level required to meet applicable regulatory standards (e.g., FCC or ETSI).

The signal at the output of the match shown in Figure 5 will likely contain relatively high levels of harmonics. Although the bandpass response of the series-resonant L_0-C_0 tank provides some attenuation of harmonic signals, it is generally not sufficient to meet applicable regulatory standards. This is normal for a switching-amplifier and matching topology.

No single, low-pass filter design is appropriate for all customers as they may operate under widely differing regulatory standards and harmonic requirements. Also, the radiation efficiency of the antenna selected by the customer is unknown. For these reasons, Silicon Labs does not conclusively state required filter attenuation characteristics, but recommends the following design goals for the low-pass filter:

- Minimal insertion loss at the desired operating frequency
- Lowest filter order possible to achieve harmonic attenuation required to meet regulatory standard
- 1:1 impedance transformation (i.e. 50 Ω input and 50 Ω output impedance)

Note that the amplitude characteristics of the LPF in the lower portion of the passband are relatively unimportant. Because the output signal contains no frequency components below the fundamental frequency, the frequency response of the filter below the desired operating frequency is of little consequence. It is therefore acceptable to select the filter type (e.g., Butterworth, Chebyshev, Elliptic) based primarily upon the filter's attenuation characteristics rather than its passband response.

A Butterworth filter design is sub-optimal because it provides relatively poor high-frequency attenuation characteristics; there is no need to sacrifice high-frequency attenuation in order to obtain a maximally-flat, in-band frequency response.

Similarly, an Elliptic filter design (Cauer-Chebyshev) may provide insufficient attenuation at higher-order harmonic frequencies. While it may be possible (and advantageous) to tune a transmission zero in the stopband to the exact frequency of a problematic harmonic (e.g., N=2 or N=3), the consequence is a decrease in attenuation at higher harmonic frequencies. Insufficient attenuation of higher-order harmonics may result.

A Cheyshev low-pass filter design provides an acceptable type of filter response. With a Chebyshev filter, it is possible to obtain a greater rate of attenuation roll-off in the stopband by accepting a larger amount of amplitude ripple in the passband. However, this design trade-off should not be pushed too far. By designing for a limited amount of passband amplitude ripple, an upper limit is placed on the filter insertion loss due to mistuning of the component values and thus accidentally operating on a minimum of the amplitude ripple response rather than on a maximum. Silicon Labs recommends a Chebyshev passband amplitude ripple of 0.25 dB to 0.5 dB as providing a reasonable balance between high-frequency stopband attenuation and potential passband filter insertion loss due to component tolerance.

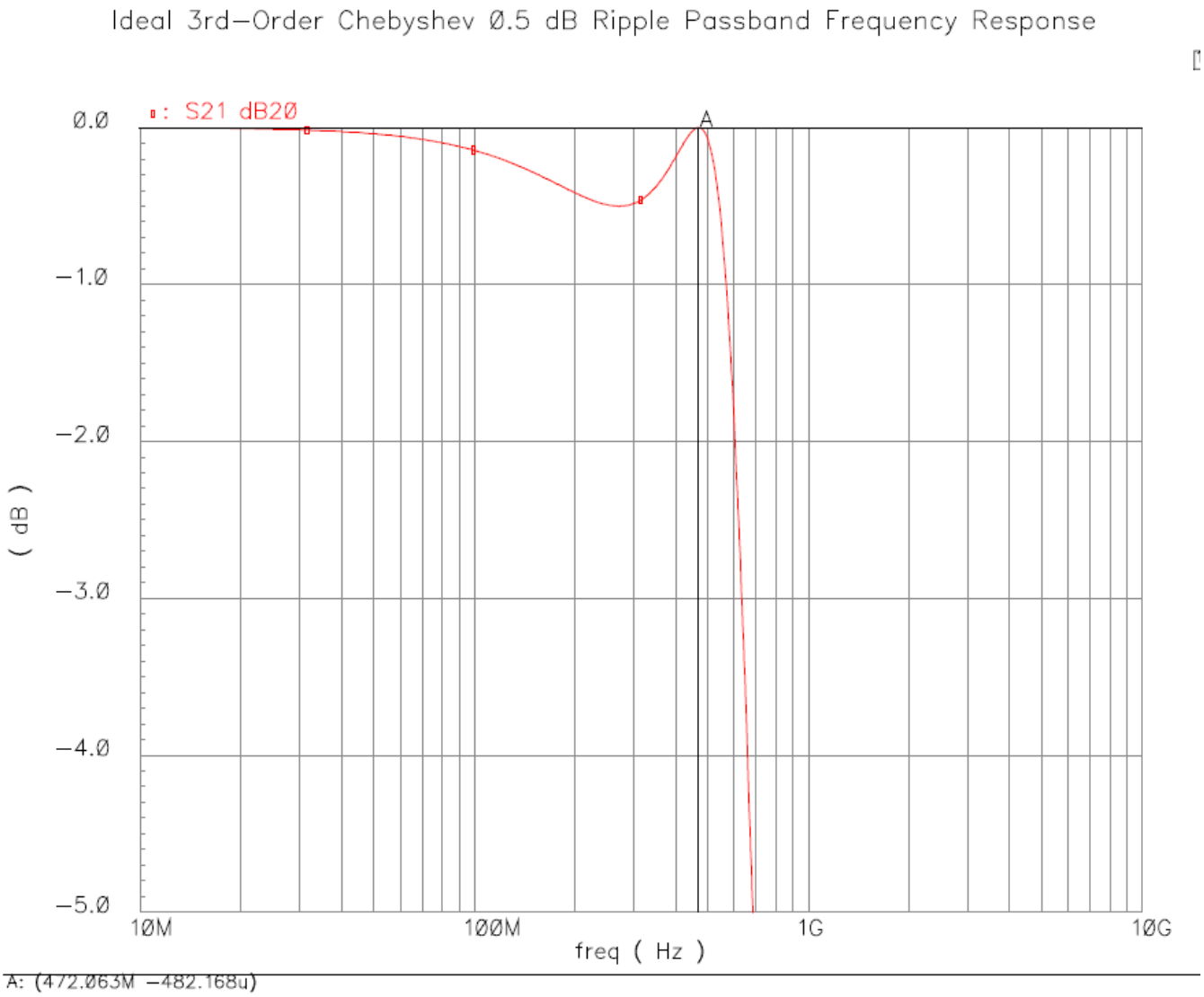

Figure 7. Ideal 3rd-Order 0.5 dB Chebyshev Filter Response at 470 MHz

Figure 7 shows the passband frequency response of an ideal (lossless) Chebyshev filter with 0.5 dB of amplitude ripple in the passband. In order to minimize the insertion loss of the filter at the desired operating frequency, it is necessary to design the cutoff frequency of the filter such that the desired operating frequency falls at one of the passband amplitude ripple peaks (Cursor "A" in the plot). If the desired operating frequency fell on a minimum of the amplitude ripple response (rather than on a maximum), the filter insertion loss would increase and the TX output power would decrease.

Filter component values may be obtained by usual design methods, such as use of Filter Design CAD software or tables of normalized filter values scaled to the desired frequency of operation. Silicon Labs recommends designing the filter such that the desired operating frequency falls at a peak of the amplitude ripple response rather than at the 3 dB cutoff frequency or at the equal amplitude ripple cutoff frequency. In this manner, the insertion loss of the filter will be minimized, and the TX output power will be maximized. For a 3rd-order 0.1 dB Chebyshev filter, the ratio of F_{3dB}:F_{PEAK} is approximately 1.60:1. That is, if the desired operating frequency is 470 MHz, the filter must be designed for a 3 dB cutoff frequency of 470 x 1.60 = 752 MHz. For a 3rd-order 0.5 dB Chebyshev filter, the ratio of F_{3dB}:F_{PEAK} is approximately 1.346:1.

SPICE model simulations of non-ideal discrete components predict an in-band filter insertion loss of approximately 1.0 dB at the desired operating frequency (470 MHz, in this example). While not desirable, this value of filter

insertion loss is fairly realistic, given the typical Qs of discrete components in 0402-size or 0603-size surface-mount packages. Discrete components of higher quality (e.g., wire-wound inductors) may be chosen in an effort to reduce insertion loss, but such parts are admittedly more expensive. The Si4063/Si4463/64/68 RFIC is capable of providing the specified output power (+20 dBm) at the antenna output connector (i.e., after the insertion loss of the match and lowpass filter).

4.3. Modification of Class-E Match for Direct Tie Board Configuration

In this section, further detail is provided about modifying the Class-E match for a Direct Tie board configuration. A supply voltage of V_{DD} = 3.3 V is assumed.

4.3.1. Concept of Direct Tie Matching

In the Direct Tie board configuration, the TX and RX paths are tied directly together at a common point without the use of an RF switch. Careful design procedure must be followed to ensure that the RX input circuitry does not load down the TX output path while in TX mode, and that the TX output circuitry does not degrade receive performance while in RX mode.

The RX input circuitry of the Si4063/Si4463/64/68 chip contains a set of switches that aids in isolation of the TX and RX functions. This set of switches is implemented internally as shown in Figure 8.

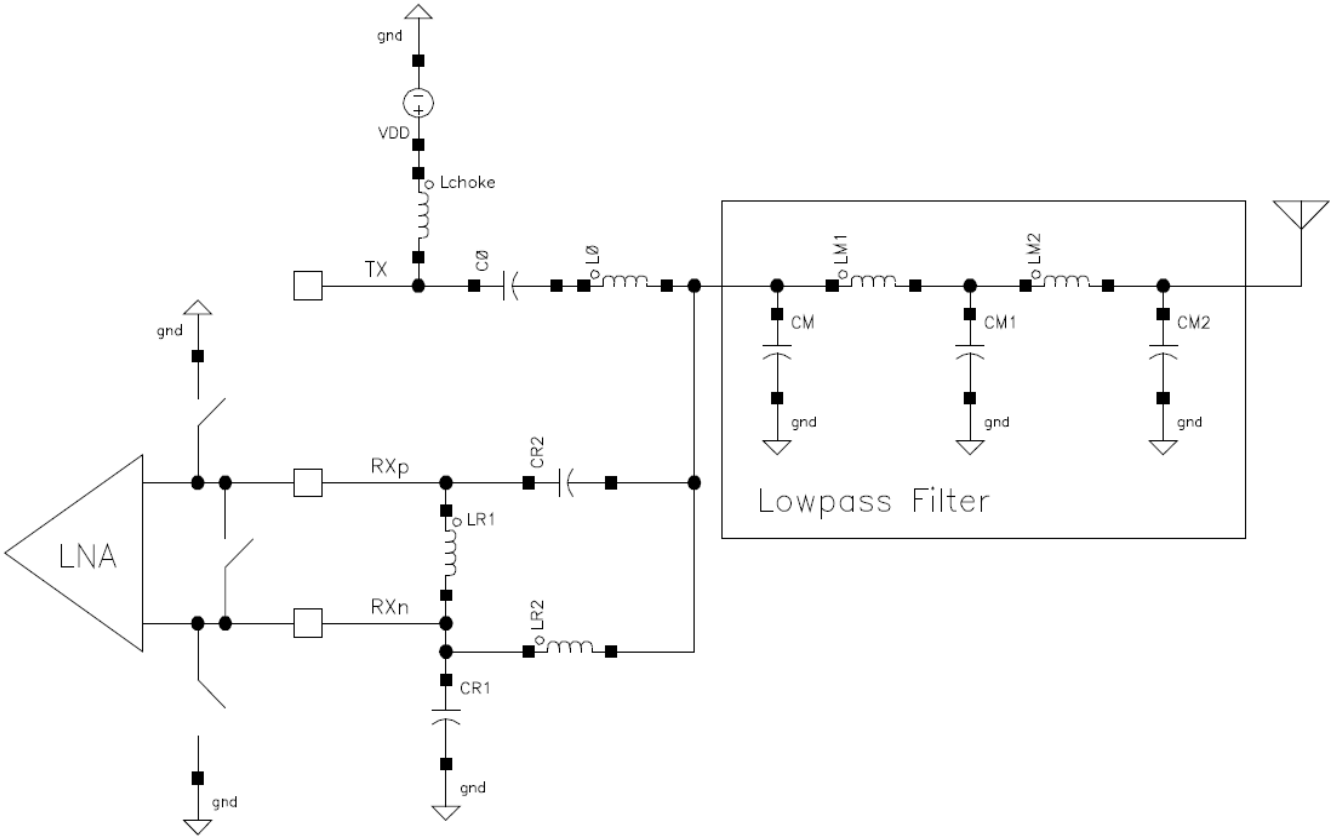

Figure 8. RX Input Switches for Direct Tie Operation

These three switches are activated and closed simultaneously upon entering TX mode; the switches remain open in all other modes, including RX mode. Closing these switches during TX mode effectively shorts the RXp and RXn input pins together and also shorts them to GND. The effective circuit may be re-drawn as shown in Figure 9. Inductor L_{R2} and capacitor C_{R2} have effectively been placed in parallel by the closure of the switches, and are connected to GND. If the values of these components are chosen for resonance at the desired operating frequency, a very high impedance is presented to the TX path resulting in very little degradation in TX output

power. Also, by shorting the input pins of the LNA together and simultaneously to GND, the LNA is protected from the large signal swing of the TX signal. This feature allows connection of the TX path to the RX path without damage to the LNA.

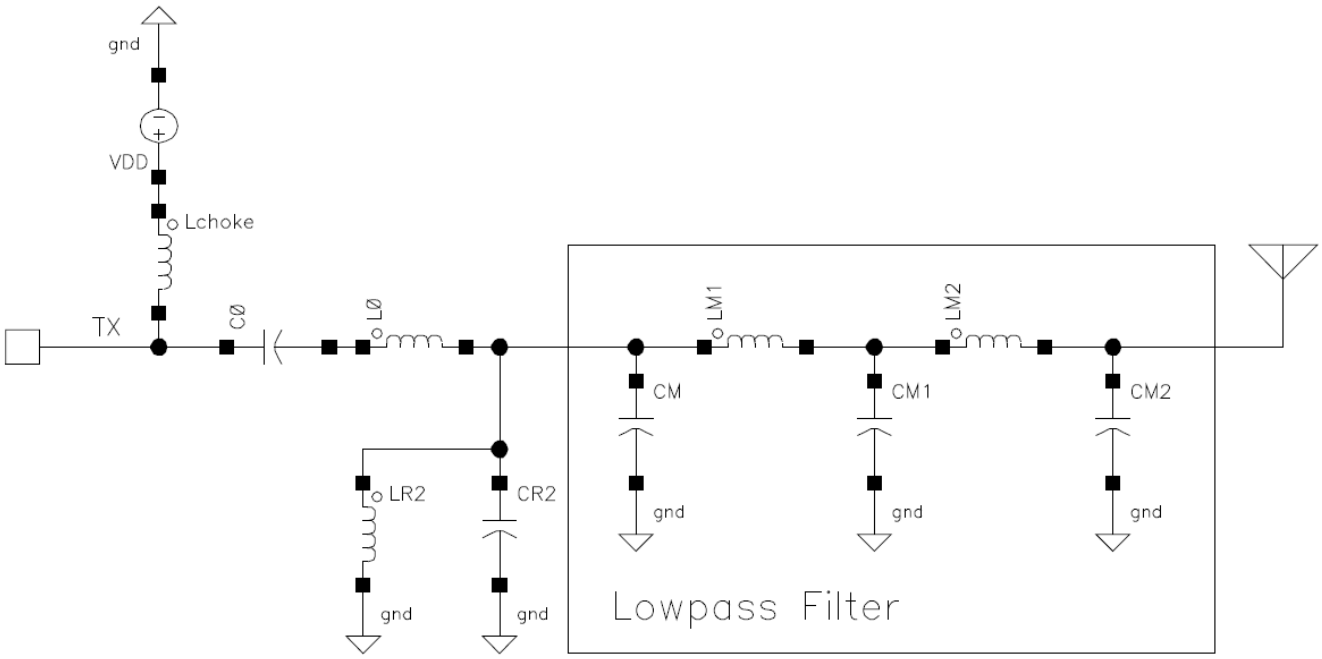

Figure 9. Effective Class-E Direct Tie Circuit in TX Mode

In RX mode, the output transistors of the PA are in the OFF state and the impedance that looks back into the TX pin is comprised mostly of the output capacitance of the transistors. (The impedance of the pull-up inductor L_{CHOKE} is quite high and may be ignored for this discussion.) This output capacitance is effectively in series with matching capacitor C_0 and will result in series-resonance with inductor L_0 at some frequency, as shown in Figure 10. At this series-resonant frequency, the input to the LNA matching network is effectively shorted to GND and thus significantly degrades receive performance. As the PA output capacitance C_{PAOFF} is fixed, it is necessary to choose L_0 and C_0 to ensure that this series-resonance does not excessively degrade RX performance at the desired operating frequency. It may be necessary to alter the values of L_0 and/or C_0 slightly away from their calculated optimum values in order to accomplish this goal, thus slightly degrading TX performance in an effort to minimize the impact to RX performance.

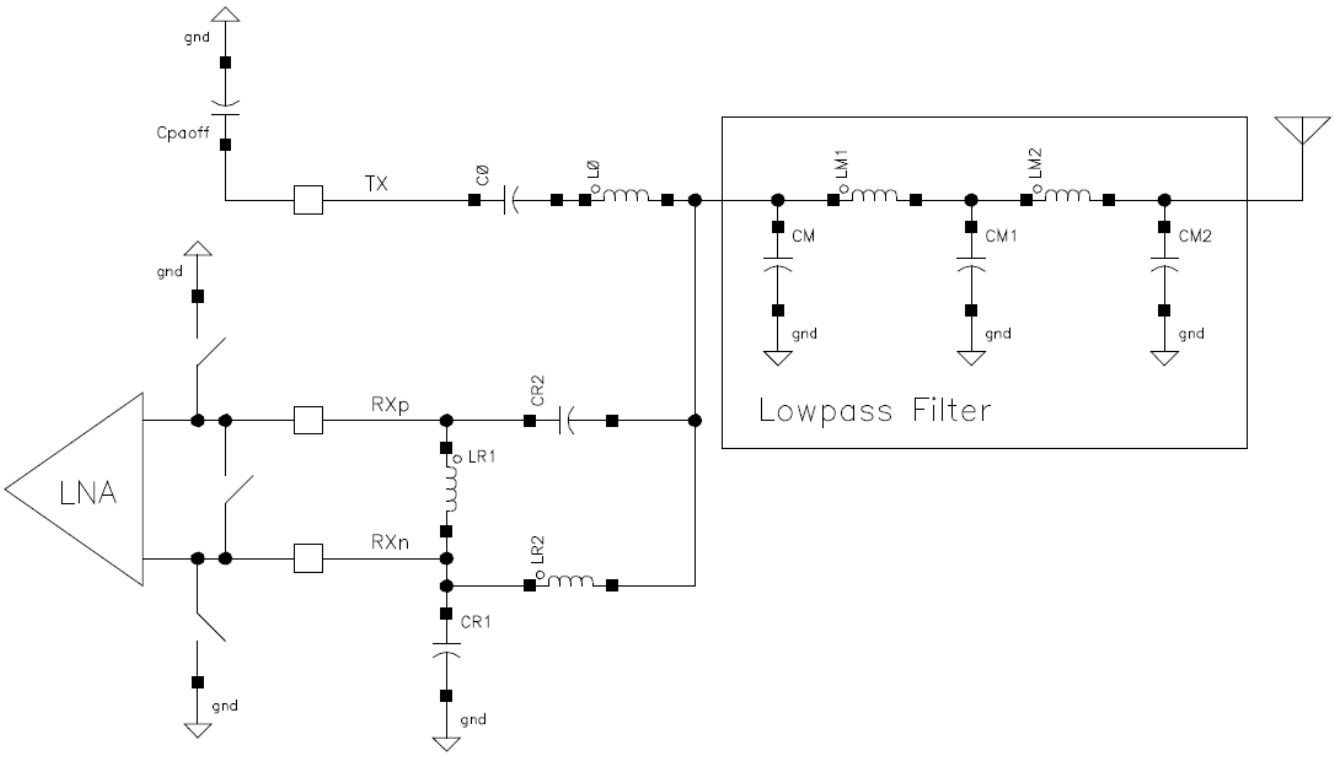

Figure 10. Effective Class-E Direct Tie Circuit in RX Mode

4.3.2. Step #7: Design RX Input Match

The next step is to construct a 4-element RX matching network to simultaneously provide an impedance match as well as to provide a single-ended to differential conversion function (i.e., balun). The mathematical derivation for the required component values has been thoroughly described in “AN643: Si446x/Si4362 RX LNA Matching”; the relevant equations from that document are shown here.

$$L_{LNA} = \frac{1}{\omega_{RF}^2 C_{LNA}}$$

Equation 11.

$$L_{R2} = \frac{\sqrt{Re(Z_{ANT})R_{LNA}}}{\omega_{RF}}$$

Equation 12.

$$L_M = \frac{2L_{R2}}{\left(\frac{2 \times Im(Z_{ANT})}{\omega_{RF} L_{R2}}\right) + 1}$$

Equation 13.

$$L_{R1} = \frac{L_{LNA} L_M}{L_{LNA} + L_M}$$

Equation 14.

$$C_{R2} = \frac{1}{\omega_{RF}^2 L_{R2}}$$

Equation 15.

$$C_{R1} = 2C_{R2}$$

Equation 16.

To make use of the above equations, it is first necessary to know the LNA differential input impedance at the desired frequency of interest. This impedance has been measured by Silicon Labs, and is summarized in “AN643: Si446x/Si4362 RX LNA Matching”. At the example design frequency of 470 MHz, the differential RX input impedance of a typical Si4063/Si4463/64/68 chip is Z_{RX_LNA} = 162.88 – j224.96 Ω; the equivalent parallel input resistance and capacitance may be calculated to be R_{LNA} = 474 Ω and C_{LNA} = 0.99 pF.

The source impedance to which the RX input is to be matched is assumed to be Z_{ANT} = 50 Ω. Plugging these values of Z_{ANT}, R_{LNA}, C_{LNA} into the above equations, the following calculated RX match component values are obtained:

- L_{R1} = 54.87 nH
- L_{R2} = 52.13 nH
- C_{R1} = 4.40 pF
- C_{R2} = 2.20 pF

These exact values may be rounded to the nearest-available 5% component tolerance values, to arrive at L_{R1} = 56 nH, L_{R2} = 51 nH, C_{R1} = 4.3 pF, and C_{R2} = 2.2 pF. If desired as an additional step of confirmation, this match may be constructed in a “stand-alone” configuration (i.e., not connected to the TX path), and its impedance measured. In this example, the input impedance and resonance were slightly off-target, likely due to parasitic trace and pad effects. The component values were adjusted slightly to optimize the impedance at the desired frequency.

- L_{R1} = 56 nH
- L_{R2} = 51 nH
- C_{R1} = 3.9 pF
- C_{R2} = 2.2 pF

4.3.3. Step #8: Connect TX and RX Paths Together, Adjust Value of L_0

In Step #8, the value of matching inductor L_0 is deliberately mis-tuned slightly away from its optimum value (as determined in Steps #1-6). As shown in Figure 10, the series-resonance of L_0-C_0-C_{PAOFF} has the potential for significantly degrading the RX performance by placing a (near) short to GND at the input of the RX matching network. It is important that this series-resonant frequency be adjusted to fall sufficiently far away from the desired operating frequency in order to minimize its effect upon RX sensitivity. This adjustment is accomplished by deliberately increasing the value of L_0 by approximately 20% above its optimum calculated value, which will push the unwanted resonance lower in frequency and minimize its effect upon RX performance. Some post-tuning of capacitor CM may also be required to improve Class-E operation after the change in value of L_0.

It is also possible to lower the resonant frequency of the L_0-C_0-C_{PAOFF} circuit by increasing the value of C_0 instead of L_0. However, as C_0 is in series with C_{PAOFF}, a larger change in value must occur to provide the same amount of mistuning. This stronger mistuning will result in even greater reduction in performance in TX mode. Therefore, tuning of L_0 is preferred and generally results in a better compromise between TX and RX performance.

Some small degradation in both TX and RX performance is expected for a Direct Tie configuration. It is not possible to directly connect the TX and RX paths together and achieve perfect isolation between the two circuit functions; each path will result in some amount of unwanted loading to the other path, and thus some small degradation in performance (relative to a Split TX/RX board configuration in which the TX and RX paths remain entirely separate). The choice of matching inductor L_0 heavily impacts the trade-off between optimizing for TX output power at the expense of degraded RX sensitivity, or vice versa. A value may generally be found which achieves a good compromise between the two, typically resulting in less than 1 dB reduction in TX output power and no more than 2-3 dB reduction in RX sensitivity. Some amount of “tweaking” of the final values of L_0 and CM may be necessary to achieve this best compromise.

5. Square Wave Matching Procedure for the Si4063/Si4463/64/68

As shown in Equation 1, the output power in Class-E operation is proportional to the operating frequency (in the absence of any frequency-dependent circuit losses due to non-ideal operation). Thus as the frequency of operation is lowered, the output power also decreases. The same equation also indicates that the output power may be increased by raising the value of shunt capacitor C_{SHUNT}; however, this capacitance is a fixed design parameter in the Si4063/Si4463/64/68 RFIC and may not be adjusted by the user. As a result, Class-E operation becomes inadvisable when operating in the lower frequency range of the chip, and it becomes necessary to match the PA using a different methodology. Silicon Labs advises use of Class-E matching when operating at frequencies above approximately 420 MHz; at frequencies below this, use of Square Wave with Harmonic Termination matching is recommended.

In the Square Wave matching methodology, a broadband pull-up inductor and series capacitor are connected between the TX output pin and a broadband resistive load. Operation of the switching-type amplifier into such a circuit results in an approximately square voltage waveform at the output pin, with a peak-to-peak voltage swing of about $2xV_{DD}$. This waveform is effective in delivering power to the resistive load with a reasonable voltage swing; however, the square waveform inherently contains odd-order harmonics and thus additional stages of lowpass filtering are required to reduce the harmonic signals.

5.1. Overview of Square Wave Matching Procedure

5.1.1. Split TX/RX Board Configuration

The following steps provide a broad overview of the matching methodology for Square Wave with Harmonic Termination operation on the Split TX/RX board configuration. Further details of each step will be provided later.

1. Choose L_{CHOKE} (pull-up inductor) for high impedance at Fo (and its nearest harmonics).
2. Choose C_0 (series capacitor) for low impedance at Fo.
3. Design a low-pass filter to provide sufficient attenuation of harmonic signals.
4. Design L_H-C_H network (to provide good termination at harmonic frequencies)

5.1.2. Direct Tie Board Configuration

The following steps provide a broad overview of the matching methodology for Square Wave with Harmonic Termination operation on the Direct Tie board configuration. Further details of each step will be provided later.

1. Repeat Steps 1 through 4, as shown immediately above.
2. Construct a 4-element balun match to the differential RXp/RXn LNA input pins, using the methodology outlined in “AN643: Si446x/Si4362 RX LNA Matching”.
3. Connect the TX and RX paths together.

5.2. Detailed Square Wave Matching Procedure

In this section, further detail is provided about each step of the matching procedures outlined above. A supply voltage of V_{DD} = 3.3V is assumed.

5.2.1. Step #1: Select a Value for L_{CHOKE} Pull-Up Inductor

In Step #1, an appropriate value is selected for the pull-up inductor L_{CHOKE}. The design constraints that influence the selection of L_{CHOKE} for Square Wave operation are the same as for Class-E operation; please refer to “4.2.1. Step #1: Select a Value for L_{CHOKE} Pull-Up Inductor” for a detailed discussion of these factors.

5.2.2. Step #2: Select a Value for C_0 Series Capacitor

In Step #2, an appropriate value is selected for the series capacitor C_0.

This capacitor is chosen to provide a low impedance at not only the fundamental operating frequency but also at the first few harmonic frequencies. Selection of a capacitor value that results in self-resonance at just above the desired operating frequency is recommended. The exact capacitance value is not critical; however, Silicon Labs recommends the following range of capacitance values (assuming 0402-size or 0603-size capacitors) as a function of the desired operating frequency

- 169 MHz: approximately 470 pF
- 315 MHz: approximately 270 pF
- 470 MHz: approximately 150 pF
- 915 MHz: approximately 39 pF

Connecting a broadband load resistance to the output of series capacitor C_0 results in the circuit configuration shown in Figure 11.

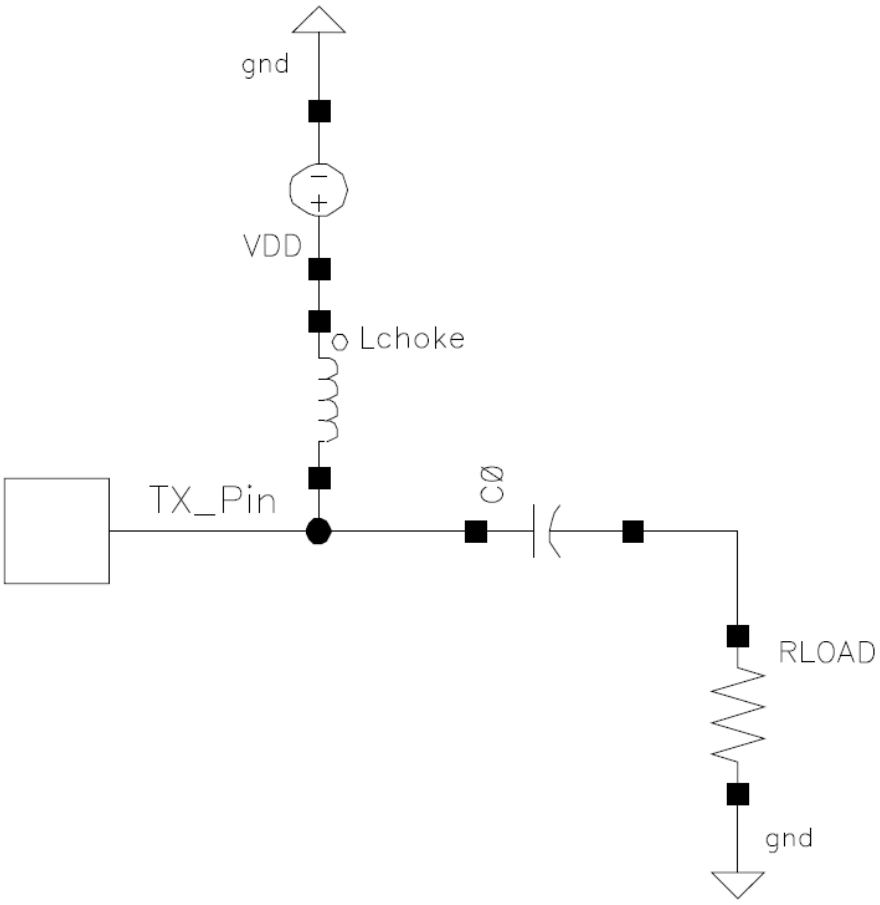

Figure 11. Simplified L-C Match into Broadband Load

The voltage waveform present at the TX output pin may be measured by using a high-impedance low-capacitance compensated probe or equivalent “resistor sniffing” network. The drain voltage waveform of Figure 12 was observed for an operating frequency of 470 MHz. In the example shown here, a reasonably square waveform was obtained by using component values of L_{CHOKE} = 220 nH, C_0 = 150 pF, and R_{LOAD} = 50 Ω.

Note that, as the operating frequency increases, it becomes more difficult not only to maintain a square waveform at the TX output but also to observe the square waveform. The input bandwidth of the oscilloscope used to display the waveform must increase in accordance with the operating frequency. Additionally, parasitic capacitances in the PCB layout, as well as in the output device(s) of the RFIC, tend to limit the high-frequency response of the amplifier.

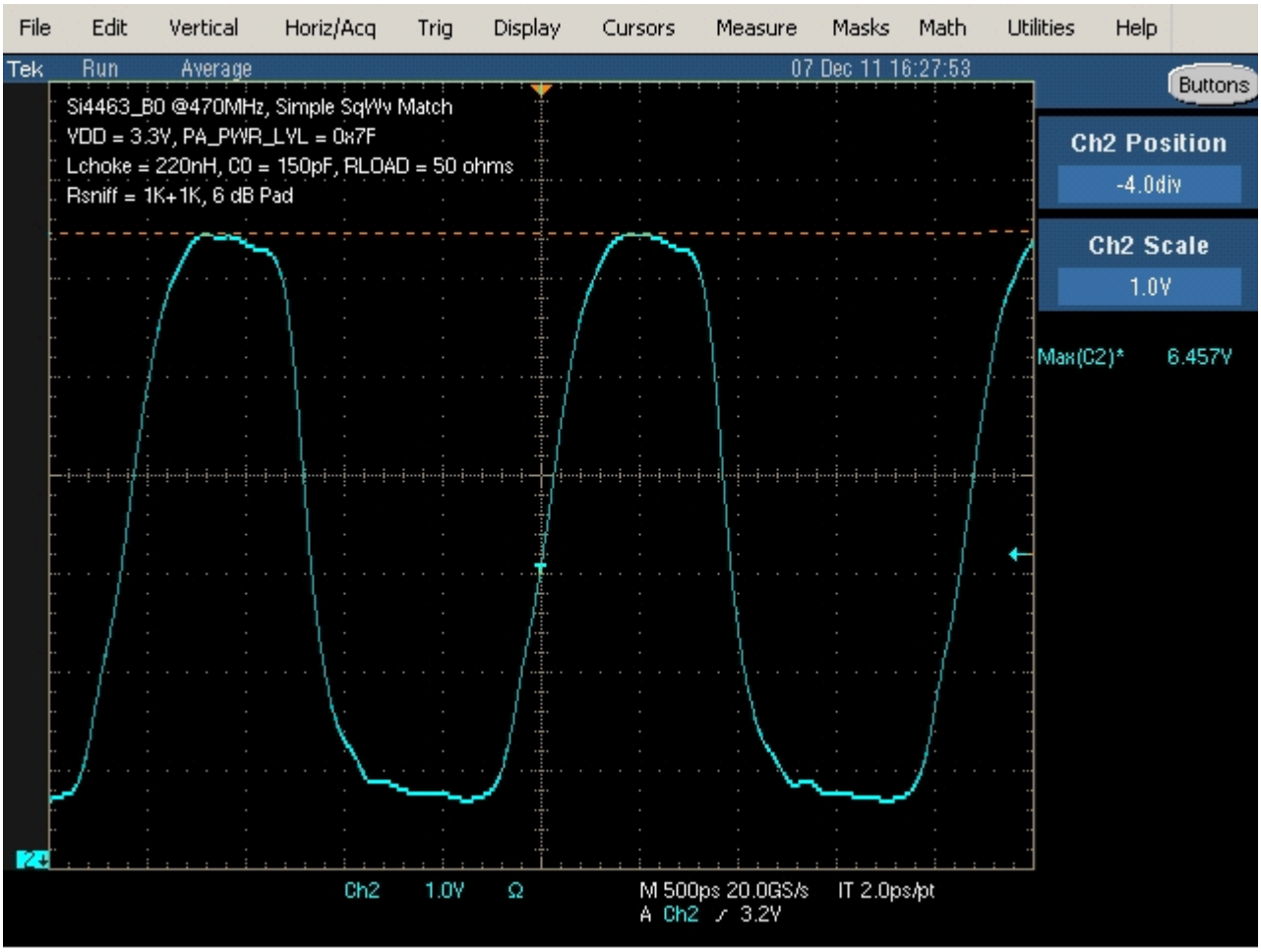

Figure 12. Drain Voltage Waveform at Fo = 470 MHz

The amount of power extracted from the Si4063/Si4463/64/68 RFIC may be increased by reducing the load resistance R_{LOAD}. However, a reduction in the value of R_{LOAD} is accompanied by an increase in the current handling required internally by the PA output devices. The size of the MOS output device in the Si4063/Si4463/64/68 RFIC is designed to carry sufficient current to readily achieve its maximum specified output power when operated into R_{LOAD} = 50 Ω; Silicon Labs does not recommend reducing the value of R_{LOAD} significantly below this value.

This optimal value of load resistance (R_{LOAD}) is not the same parameter as the antenna impedance (R_{ANT}), nor do they necessarily have the same ohmic value. Given the arbitrary impedance of the antenna, it will later be necessary to construct a matching network that transforms R_{ANT} into R_{LOAD}, as seen at the TX output pin of the RFIC. The task of constructing this lowpass filter and matching network is simplified if both impedances are the same value (e.g., 50 Ω), but it is possible to work with other values of R_{ANT} or R_{LOAD}.

5.2.3. Step #3: Design a Lowpass Filter

In Step #3, a low-pass filter network is designed in order to attenuate the harmonics below the level required to meet applicable regulatory standards (e.g., FCC or ETSI).

The design constraints that influence the construction of a lowpass filter for Square Wave operation are the same as for Class-E operation (see “4.2.6. Step #6: Design a Lowpass Filter”), but with the addition of one further constraint: a TEE-architecture is selected, to present a high input impedance at harmonic frequencies.

As mentioned previously, the square waveform at the TX output pin will inherently contain rather high levels of harmonics. This is normal for such a switching-amplifier and matching topology. The harmonic spectrum for the circuit of Figure 11 for the design example at 470 MHz (L_{CHOKE} = 220 nH, C_0 = 150 pF, R_{LOAD} = 50 Ω) is shown in Figure 13.

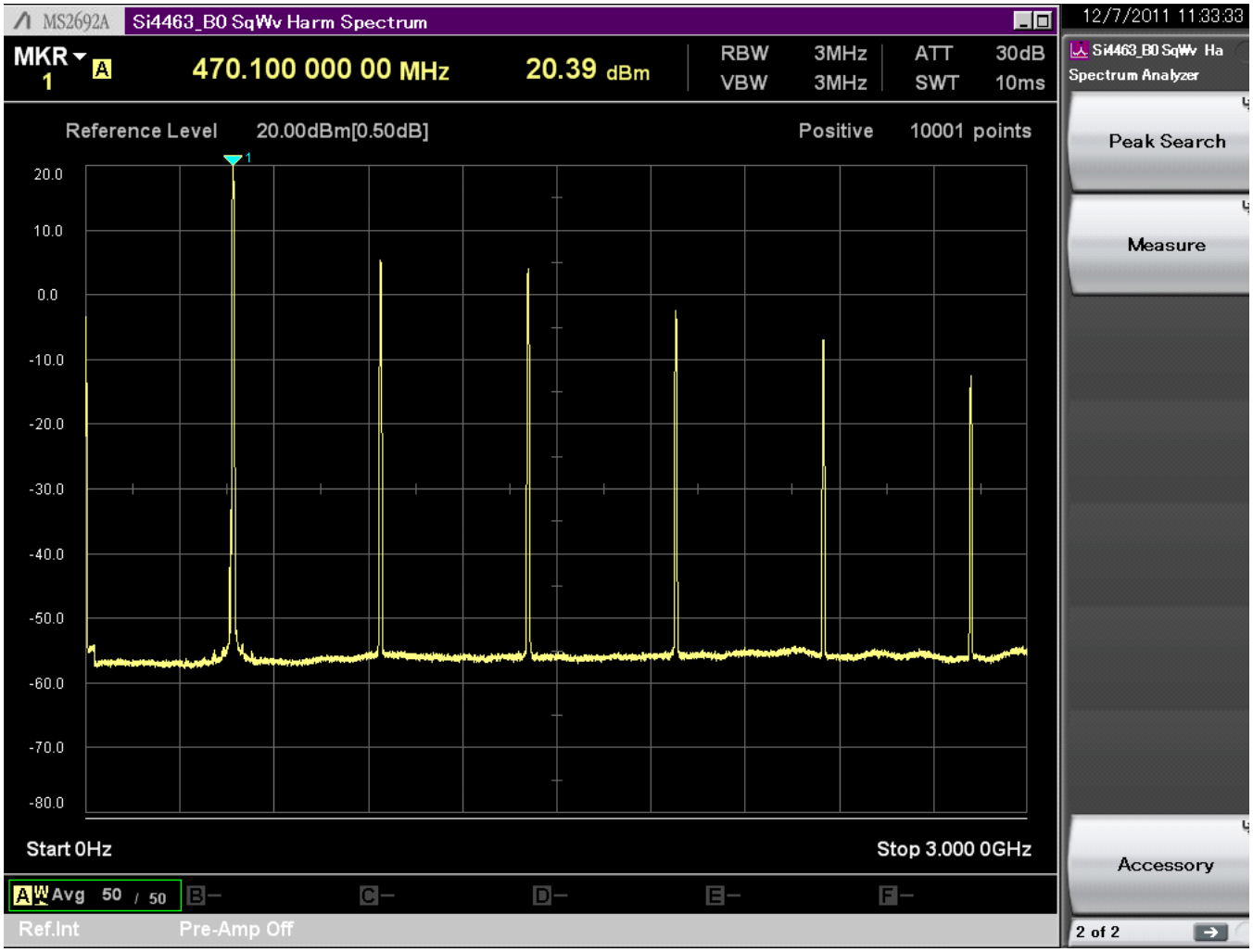

Figure 13. Unfiltered Harmonic Spectrum at TX Pin (at 470 MHz)

Adding a lowpass filter network to attenuate these harmonic signals is required. However, the desired square waveform shown in Figure 12 was obtained when operating into a **broadband** load resistance. While it is easy to design a lowpass filter that presents an input impedance equal to the desired value of R_{LOAD} at one single frequency (i.e., the desired operating frequency), it is more difficult to design the filter such that it presents this impedance at ***all*** frequencies. Simple replacement of the broadband load resistance R_{LOAD} with a conventional lowpass filter structure (e.g., PI-architecture or TEE-architecture) will significantly alter the load impedance seen by the chip at harmonic frequencies. The effect will be significant reflection of energy at certain harmonic frequencies, resulting in significant distortion of the desired square voltage waveform and possible excessive voltage peaks of the output signal.

It is thus desirable to construct a network that provides a good impedance termination at ***all*** frequencies. This may be accomplished through use of a type of diplexer network. In this approach, the fundamental signal component passes through (and is properly terminated by) a low-pass filter network while all other signal components are terminated in a separate network. The resulting voltage waveform at the TX output pin should therefore be (nearly) indistinguishable from the waveform observed when operating into a broadband resistive load.

The diplexer network consists of two “arms” connected together: a lowpass filter section in the series path, and a parallel-resonant L-C tank in the shunt path. The interaction between the two arms is minimized by ensuring that each path presents a high impedance in the frequency band in which the other path is functional. For this reason, the lowpass filter section in the series “through” path is designed using a TEE-architecture (as shown in the example of Figure 14); an architecture in which the first series component is an inductor inherently presents a higher impedance as the frequency increases.

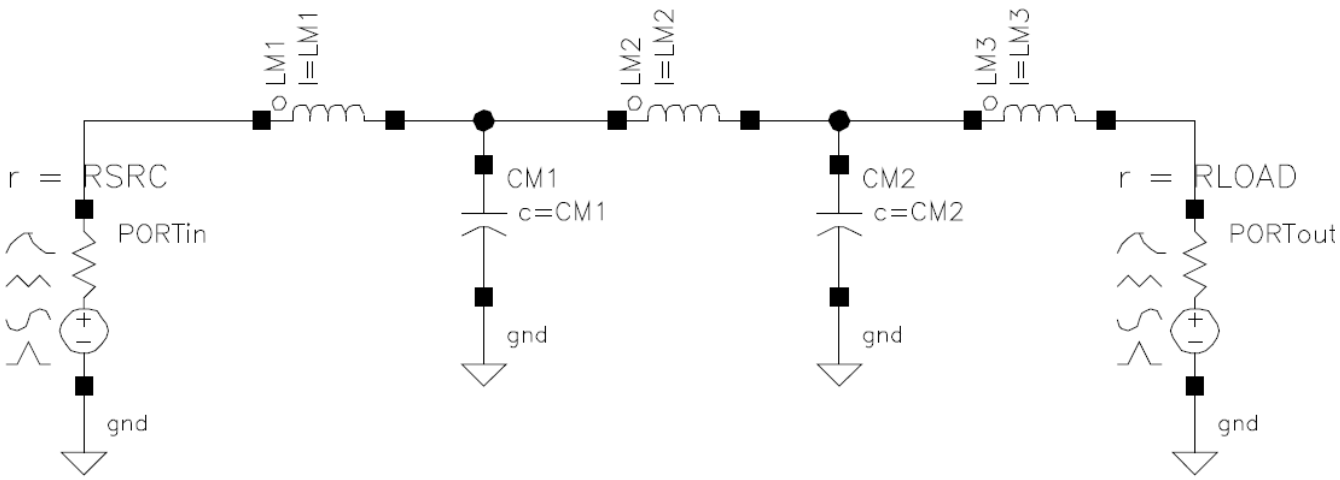

Figure 14. TEE-Architecture Low-Pass Filter

As discussed previously, filter component values may be obtained by usual design methods such as use of Filter Design CAD software or tables of normalized filter values scaled to the desired frequency of operation. Silicon Labs again recommends designing the filter such that the desired operating frequency falls at a peak of the amplitude ripple response rather than at the 3 dB cutoff frequency or at the equal amplitude ripple cutoff frequency. In this manner, the insertion loss of the filter will be minimized, and the TX output power will be maximized.

5.2.4. Step #4: Design in a Harmonic Termination Network

In Step #4, a shunt network is designed to provide good impedance termination at all frequencies other than the fundamental operating frequency.

Due to selection of the TEE-architecture for the lowpass filter path, its input impedance becomes very high at frequencies above the passband. If a separate network is designed that provides a good termination (i.e., R_{LOAD}) at harmonic frequencies but presents a high impedance at the desired frequency of operation, it may be connected in parallel to the input of the lowpass filter network with minimal interaction. This harmonic termination network may be accomplished with a parallel-resonant L-C tank and 50 Ω termination resistor, connected in shunt at the input of the lowpass filter as shown in Figure 3.

The idea is to select the values of L_H-C_H such that the tank achieves parallel resonance at the desired fundamental operating frequency. At the fundamental frequency, this resonant tank exhibits (nearly) infinite impedance and essentially disconnects the 50 Ω harmonic termination resistor (R_H) from the input of the low-pass filter. However, at all other frequencies, the L_H-C_H tank is far from parallel resonance and exhibits a low impedance, essentially connecting the 50 Ω termination resistor R_H in parallel with the input of the low-pass filter. At these high harmonic frequencies, the input impedance seen looking into only the lowpass filter is very high, and thus the PA output is essentially terminated by only the R_H resistor.

At all frequencies below the fundamental operating frequency, the PA output is terminated simultaneously by both paths and is essentially mismatched by seeing an effective 50 Ω // 50 Ω = 25 Ω load. However, this is of no consequence; there are no output signal components at any frequency below the fundamental that can be affected by such mis-termination.

The primary design requirement for selection of L_H-C_H is that they achieve parallel resonance at the desired operating frequency. There are obviously infinite combinations of L_H-C_H values that satisfy this goal; however there is an optimum L_H/C_H ratio. The simple explanation is that the L-C ratio determines how rapidly the tank impedance reduces from its maximum value of (near) infinity at its parallel resonant frequency to much lower values at frequencies far from resonance. This effectively determines how much the low-pass filter and the harmonic termination network "interact" with each other. It is preferable that these two networks not interact at all; however, in practice the two networks are not entirely independent from each other. The impedance of the harmonic termination tank does not fall off so rapidly with increasing frequency that its effect upon the low-pass filter network can be ignored. In a similar fashion, the input impedance of the low-pass filter does not increase so rapidly with frequency that its effect upon the L_H-C_H network can be ignored.

A sub-optimal L_H-C_H ratio can manifest itself in the time domain as a voltage waveform at the TX pin that is not as flat as it could be (i.e., higher peak voltage than necessary). The optimum L_H-C_H ratio has been determined by simulation, and has been found to be approximately equal to:

- L_H (in nH) / C_H (in pF) = 0.9

In practice, an L_H-C_H ratio anywhere between 0.8 and 1.0 will work reasonably well. It is suggested that the L_H-C_H component values are chosen as the nearest 5% standard values that simultaneously:

- Provide parallel resonance at the desired operating frequency
- Provide an L_H-C_H ratio between 0.8 and 1.0

5.3. Modification of Square Wave Match for Direct Tie Board Configuration

In this section, further detail is provided about modifying the Square Wave match for a Direct Tie board configuration. The concept of Direct Tie matching was discussed in detail in “4.3.1. Concept of Direct Tie Matching” and is generally applicable to a Square Wave Direct Tie match as well. The most significant difference is in the selection of the common-tie point. In the Class-E Direct Tie match configuration, the RX matching network was connected after the L_0-C_0 series resonant circuit (refer to Figure 2). In the Square Wave Direct Tie match configuration, the RX matching network is connected directly after the C_0 series capacitor (refer to Figure 4).

The effective Square Wave Direct Tie circuit in TX mode is shown in Figure 15. Inductor L_{R2} and capacitor C_{R2} have again effectively been placed in parallel by the closure of the switches, and are connected to GND. As the design equations result in L_{R2}-C_{R2} component values that achieve parallel resonance at the desired operating frequency, a very high impedance is presented to the TX path and there is very little degradation in TX output power.

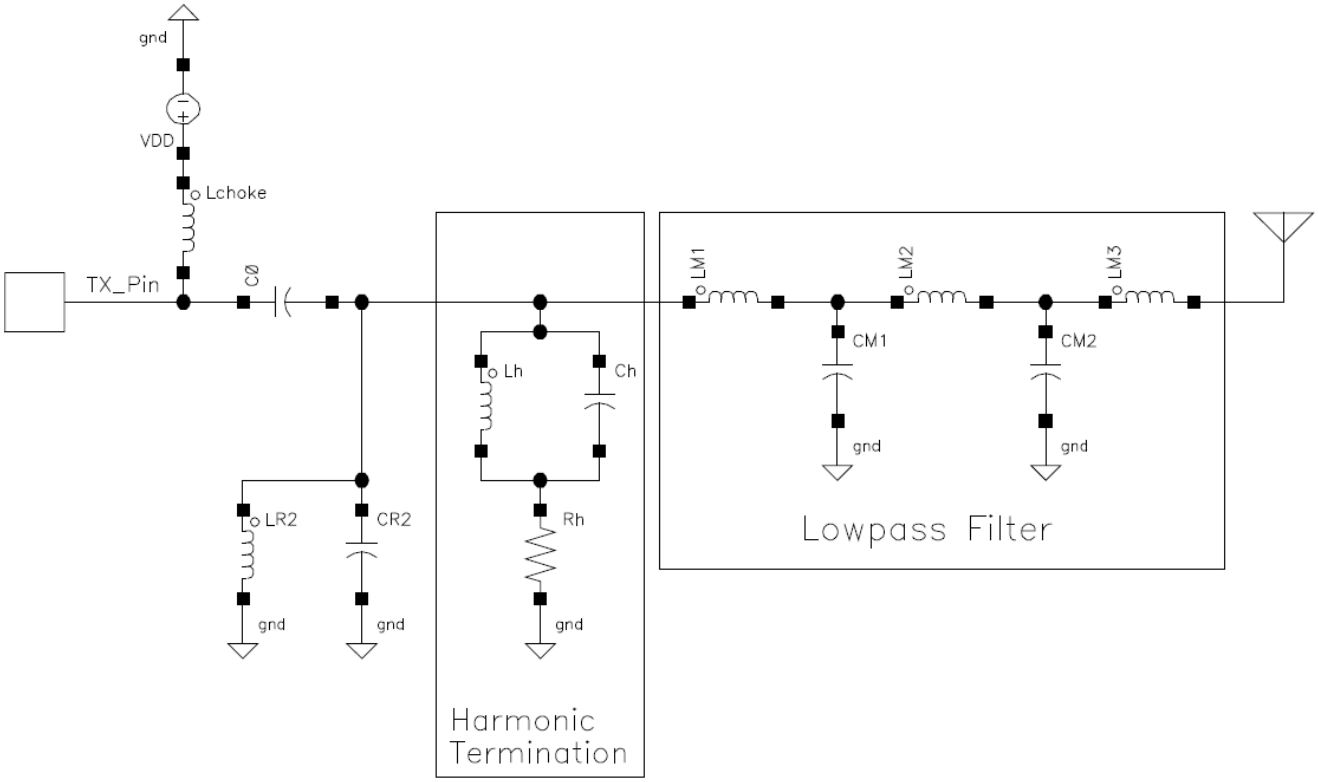

Figure 15. Effective Square Wave Direct Tie Circuit in TX Mode

The effective Square Wave Direct Tie circuit in RX mode is shown in Figure 16. The shunt harmonic termination network L_H-C_H is parallel-resonant at the desired frequency of operation and presents a very high impedance to the RX path and thus may safely be ignored. Pull-up inductor L_{CHOKE} presents a very high impedance, while series capacitor C_0 presents a very low impedance, and both may also safely be ignored. This leaves the OFF-state capacitance of the PA devices (C_{PAOFF}) as the primary degrading effect upon RX performance. This value of capacitance is C_{PAOFF} ~ 2.5 pF, and provides minimal de-tuning and degradation of the performance of the RX path.

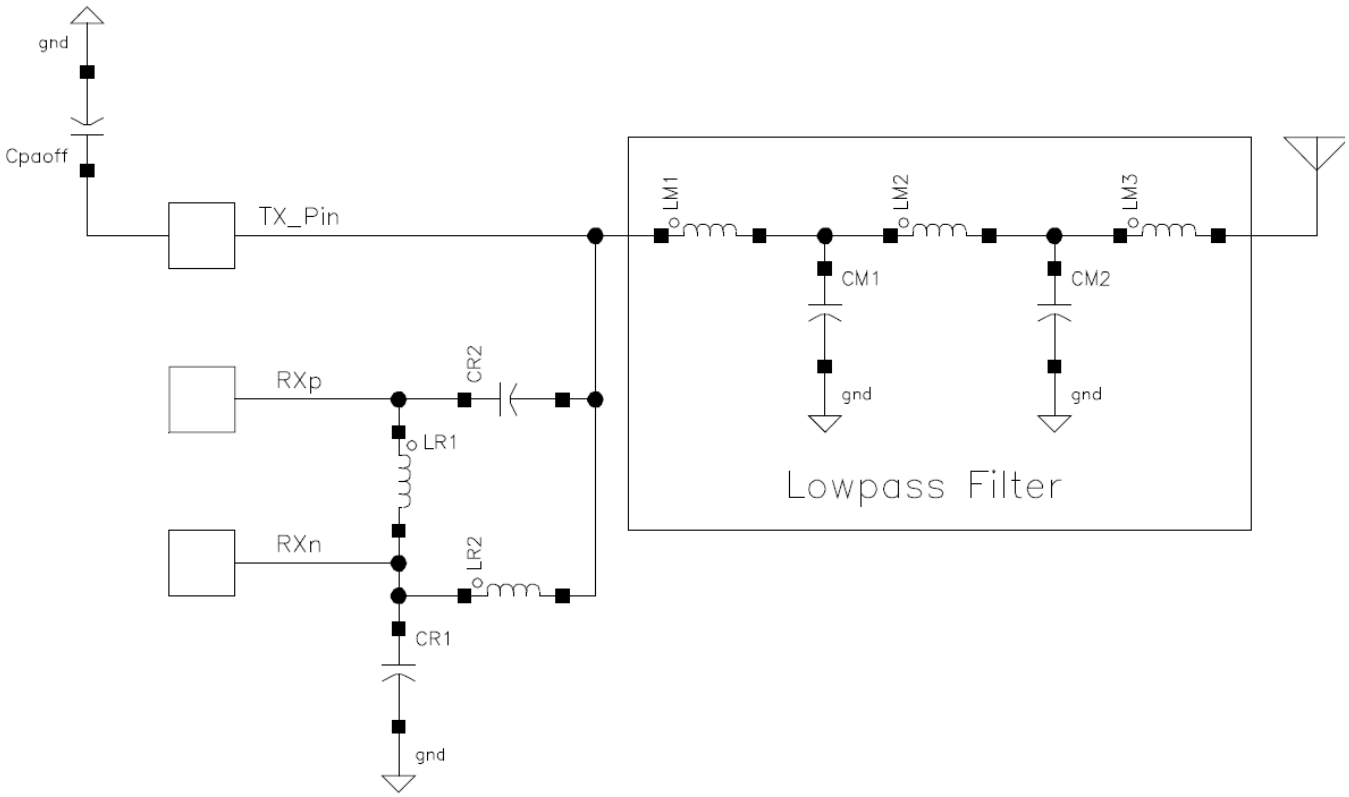

Figure 16. Effective Square Wave Direct Tie Circuit in RX Mode

5.3.1. Step #5: Design RX Input Match

It is again necessary to construct a 4-element RX match network to simultaneously provide an impedance match as well as to provide a single-ended to differential conversion function (i.e., balun). The required design equations are the same as those shown in “4.3.2. Step #7: Design RX Input Match” , and thus the resulting RX match component values are also the same as those obtained in that section.

5.3.2. Step #6: Connect TX and RX Paths Together

In Step #6, the TX and RX paths are connected together. As discussed above, the common-tie point is immediately after series capacitor C_0. No further tuning or “post-connection tweaking” of the circuit should be necessary.

6. Lowpass Filter Design Methodology for RF Switch Board Configuration

A Direct Tie match configuration is effective in reducing BOM cost by allowing use of one common antenna for both TX and RX functions. However, there is inherently some slight degradation in performance when using a Direct Tie match, as it is not possible to tie the TX and RX paths together without some amount of undesirable interaction. For users that require operation with one common antenna but also desire minimal degradation in performance, a match topology with an RF Switch may be appropriate.

In this match configuration, a SPDT switch is used to connect the TX and RX paths together. Silicon Labs recommends embedding the RFSW in the middle of the lowpass filter, as shown in Figure 17. The initial inclination may be to place the switch with the common port connected directly to the antenna and the switched ports connected to the outputs of the TX and RX matching networks. However, the RF switch itself is not a perfectly ideal component; it will re-generate some amount of harmonic energy, regardless of the cleanliness of the input signal from the TX lowpass filter. It is necessary to place some amount of lowpass filtering after the RF switch and prior to the antenna. It is not required to increase the ***total*** order of lowpass filtering (i.e., number of filter poles); instead, it is generally sufficient to split the normal amount of filtering into two half-filter sections of approximately equal cutoff frequency. The RF switch is placed between these two half-filter sections. In this fashion, the final half-filter section cleans up any harmonic energy re-generated by the RF switch.

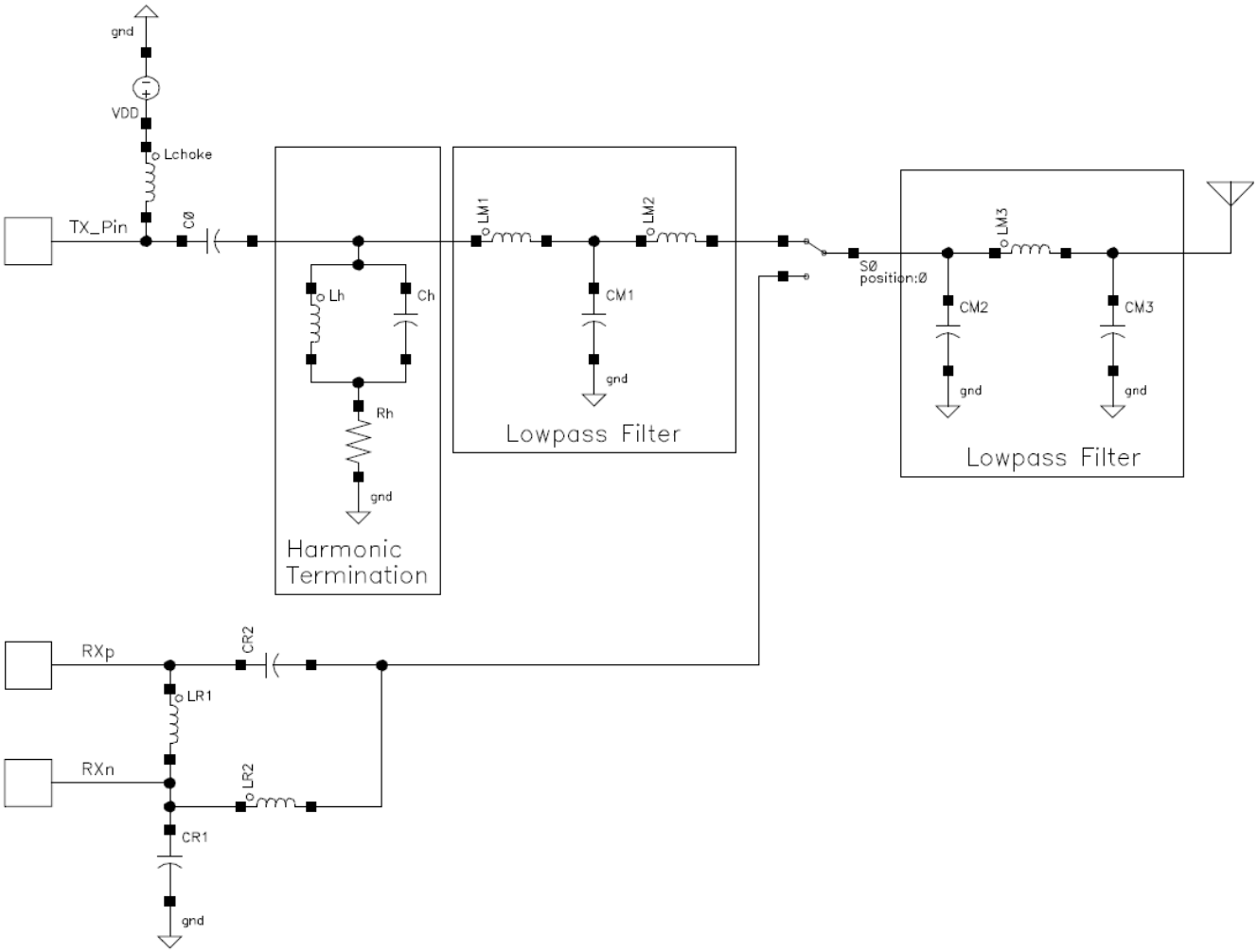

Figure 17. Matching Topology for Single Antenna with RF Switch Board Configuration

The design methodology for the two filter sections is quite simple: design one 3rd-order low-pass filter using a TEE-architecture, and another 3rd-order low-pass filter using a PI-architecture. (The use of the PI-architecture for one filter section is desirable as its shunt capacitive elements help to absorb any stray parasitic capacitance associated with the RF switch or the PCB traces.) The user should also take care to include any dc blocking capacitors that may be required by the switch selected for use, as many switches contain dc bias voltage on their input and output pins.

Document Change List

Revision 0.2 to Revision 0.3

- Added Si4467 to Si4060/Si4460/61
- Added Si4468 to Si4063/Si4463/64
- Changed AN643:Si446x to AN643:Si446x/Si4362
- Corrected equations on page 22.

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