RISC-V Single Cycle Architecture II

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Lecture 8

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2. B-type Datapath
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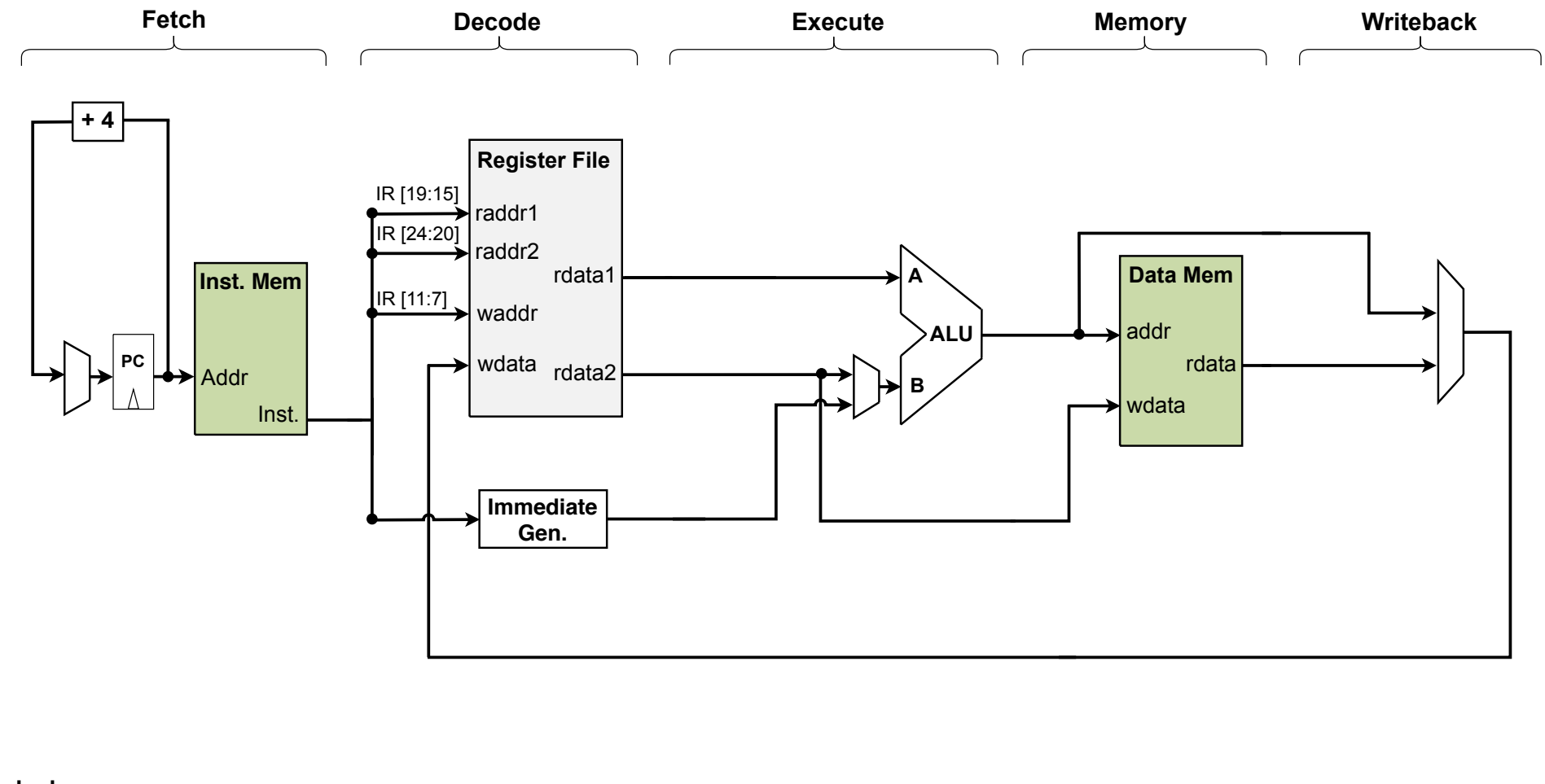
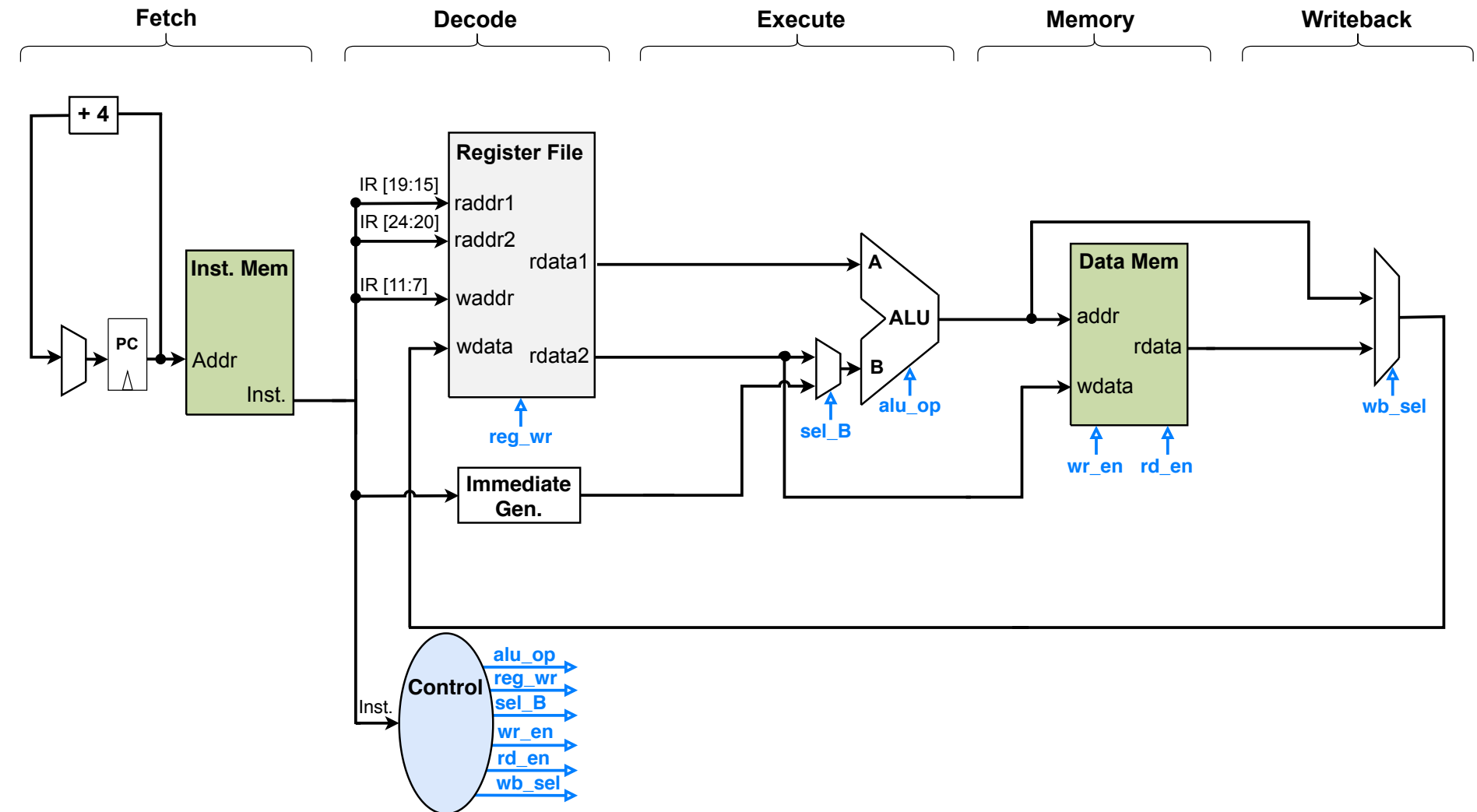
Review: ISA Supported So Far

- R, I and S type datapath

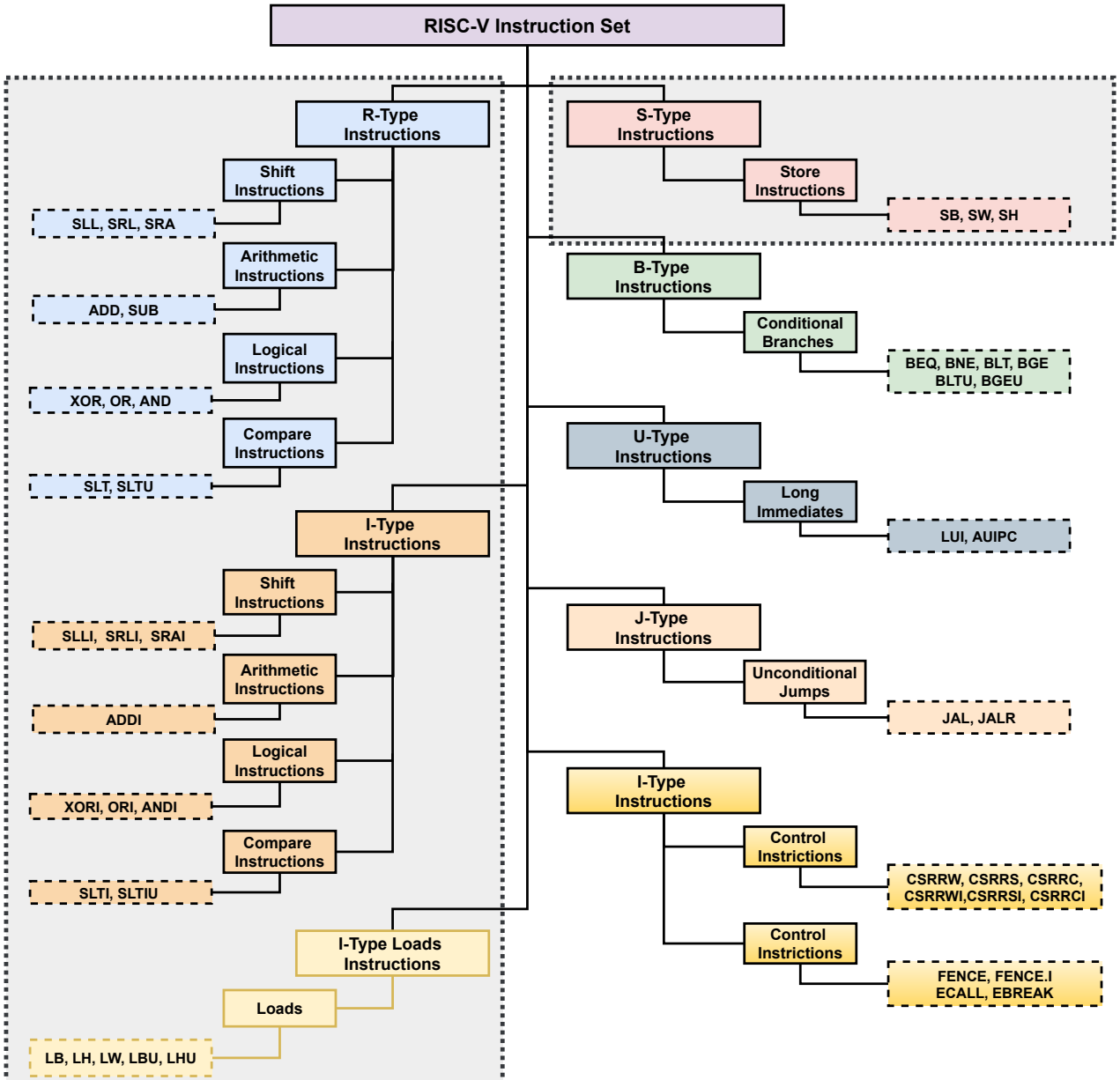


Review: ISA Supported So Far Cont'd

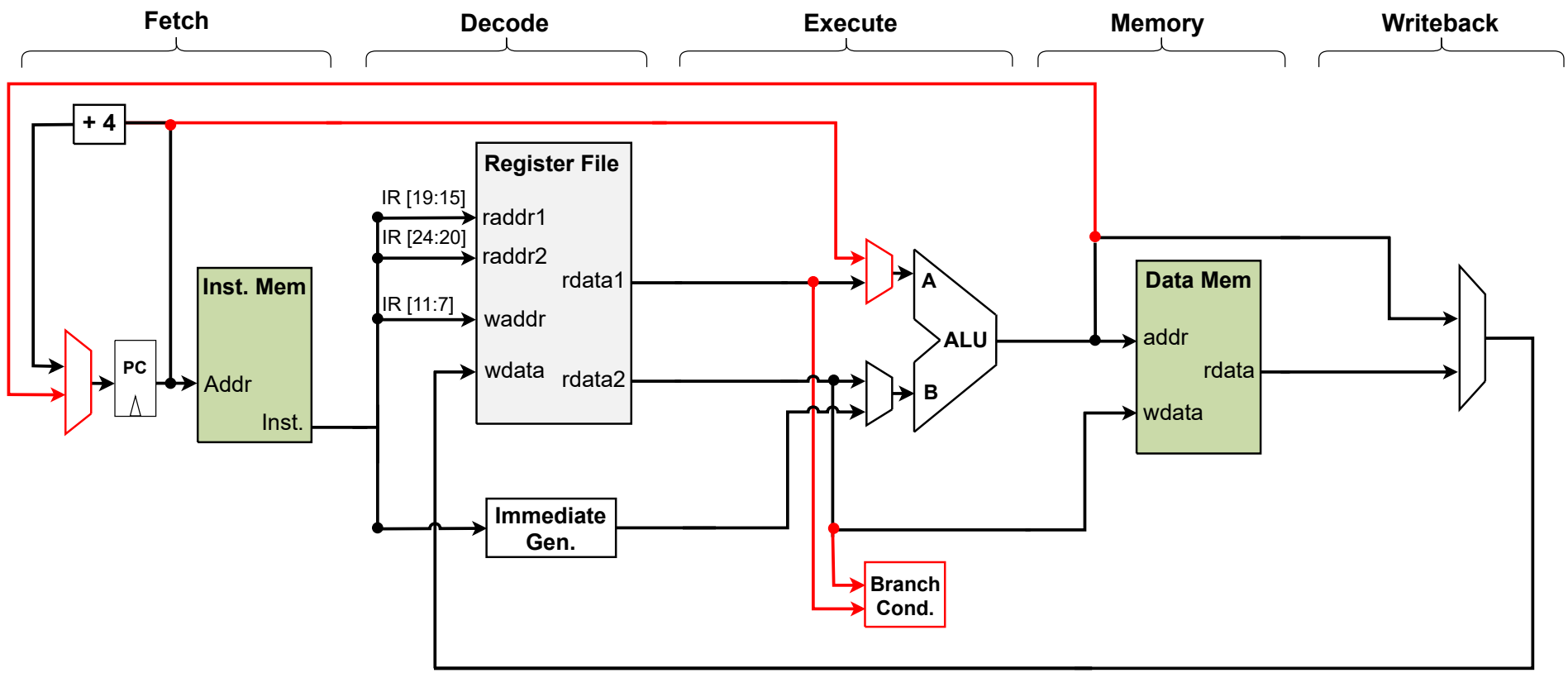
- R, I and S type datapath and control



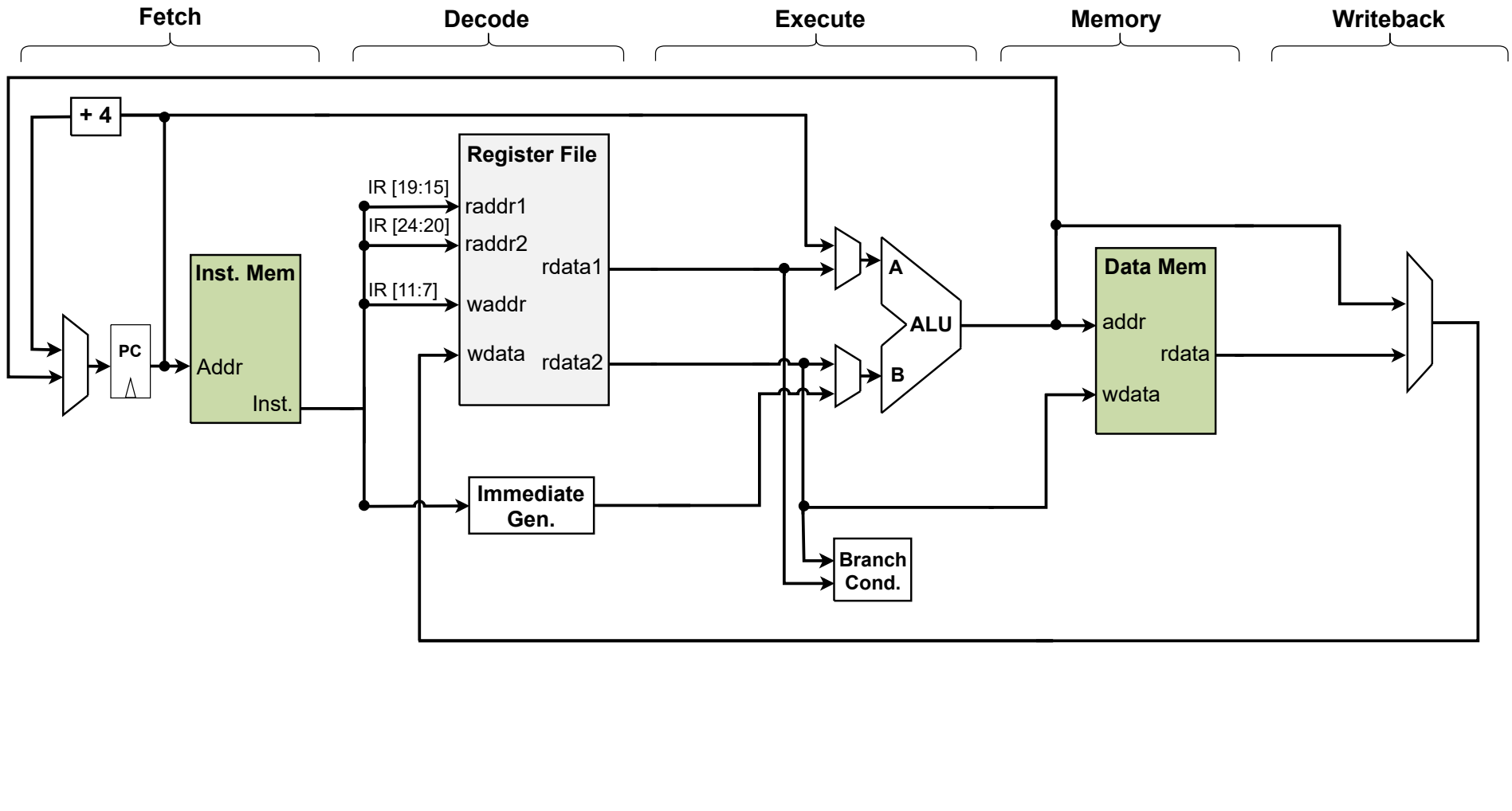
Review: ISA Supported So Far Cont'd



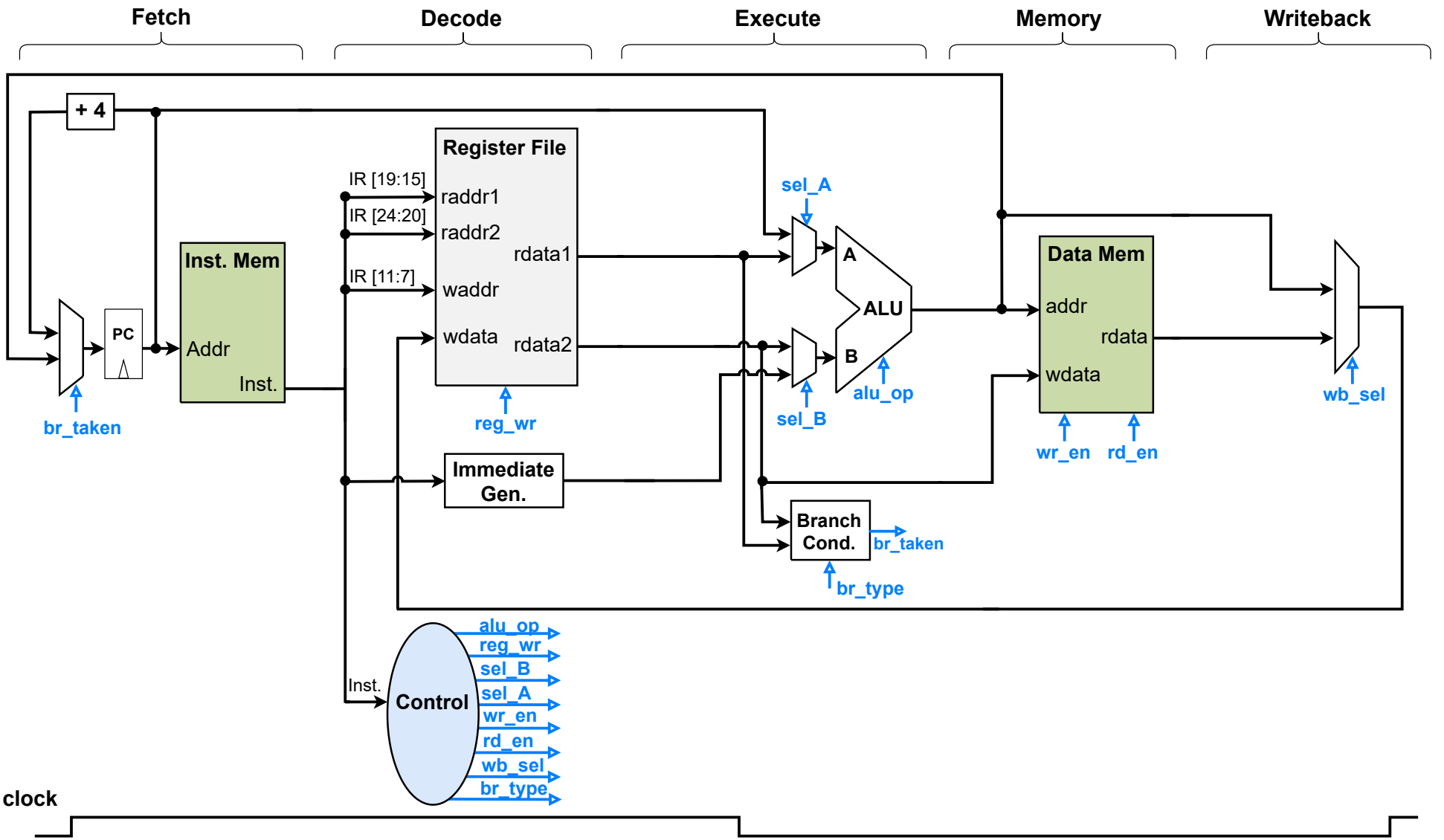
B-type: Conditional Branches



B-type: Conditional Branches Cont'd

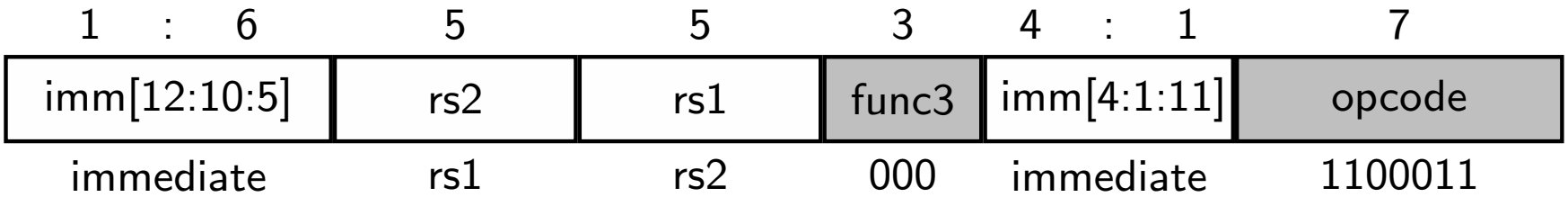


B-type: Datapath and Control



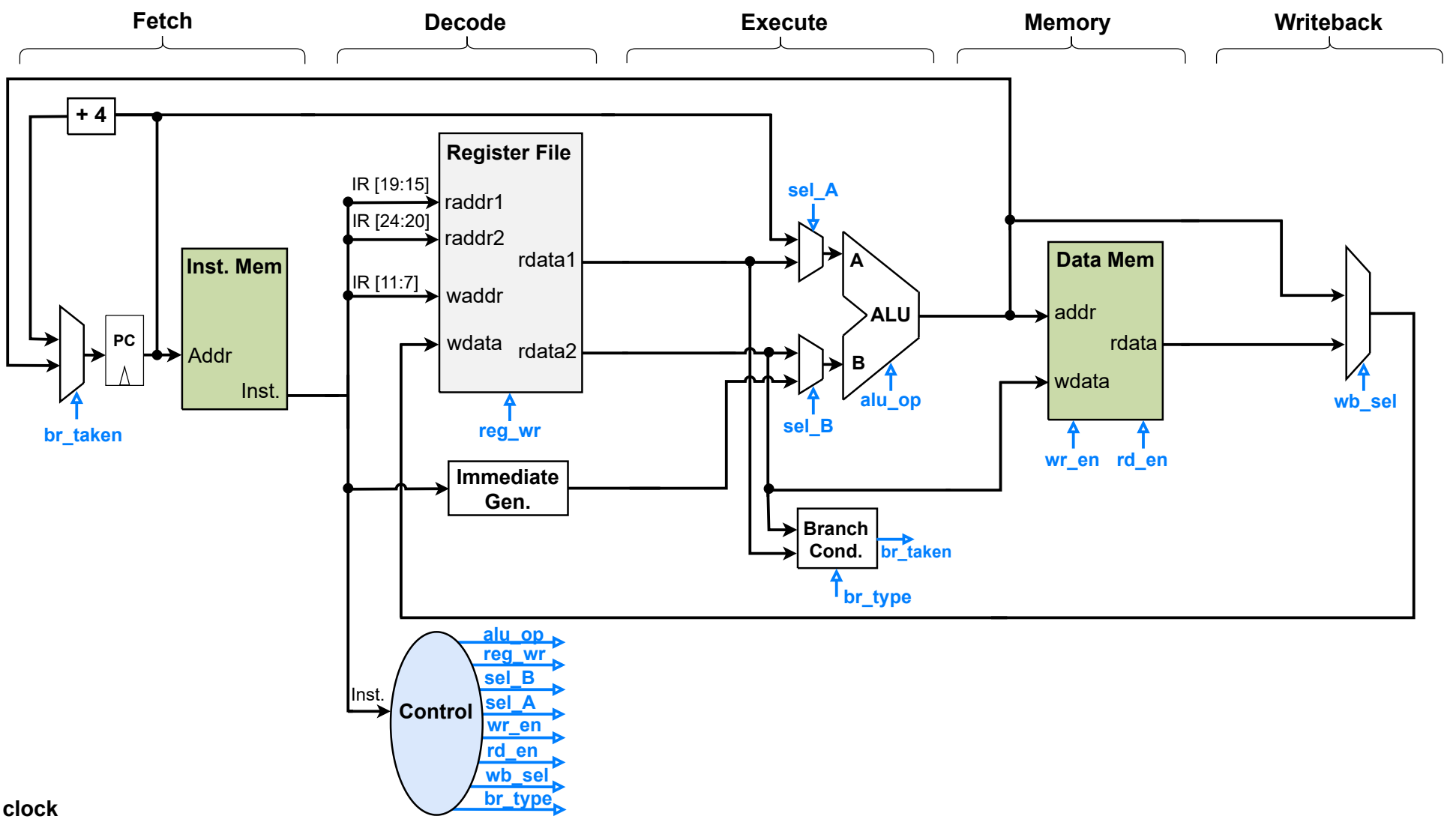
B-type: Branch Instruction Example

- B-type: Branch equal (BEQ) instruction

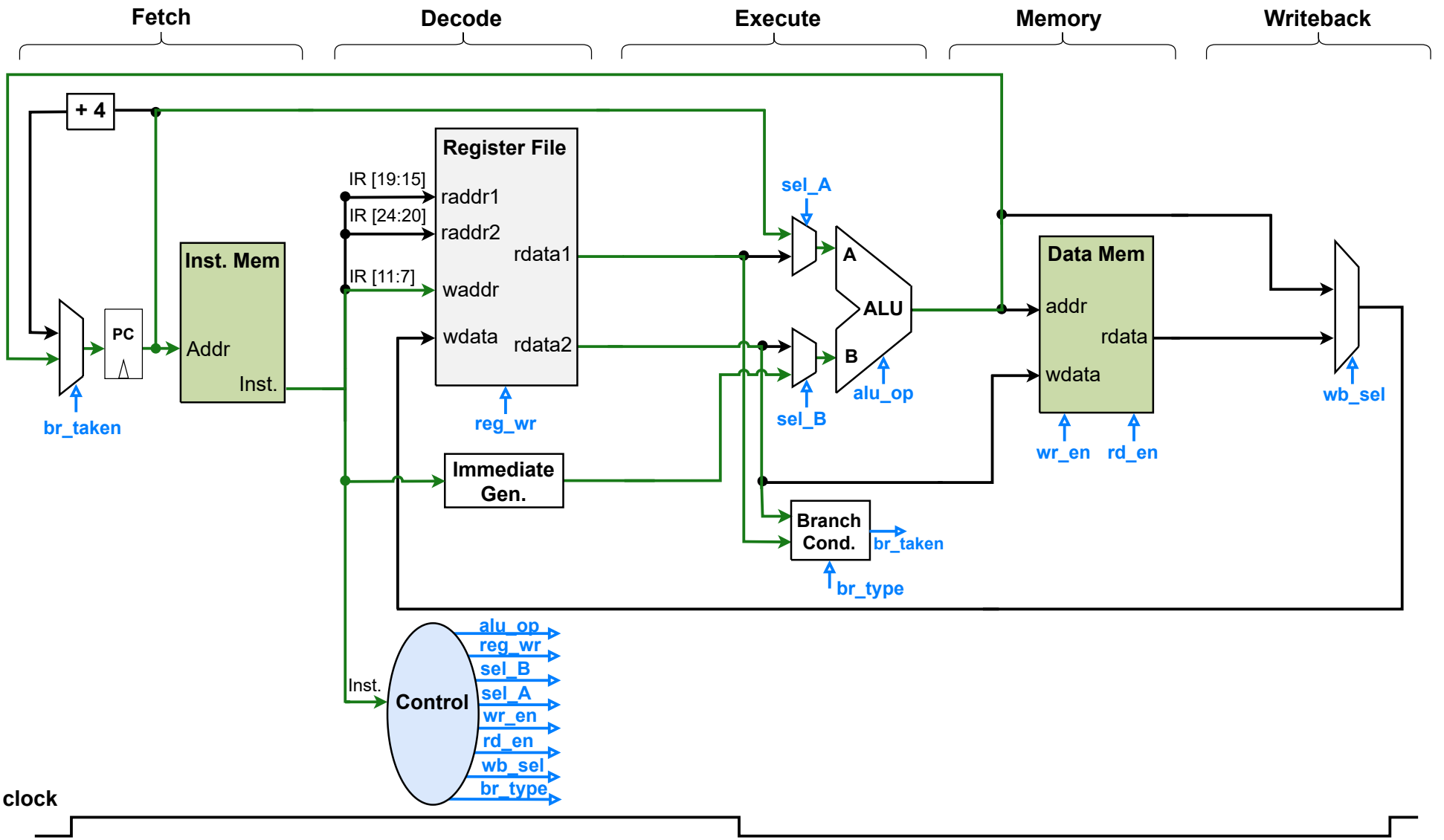


- `B-imm` = signExtend(inst[31], inst[7], inst[30:25], inst[11:8], 1'b0)
- `opcode` = BRANCH:
  pc $\leftarrow$ compare(funct3, rs1, rs2) ? pc + B-imm : pc + 4
- `funct3` = BEQ/BNE/BLT/BLTU/BGE/BGEU

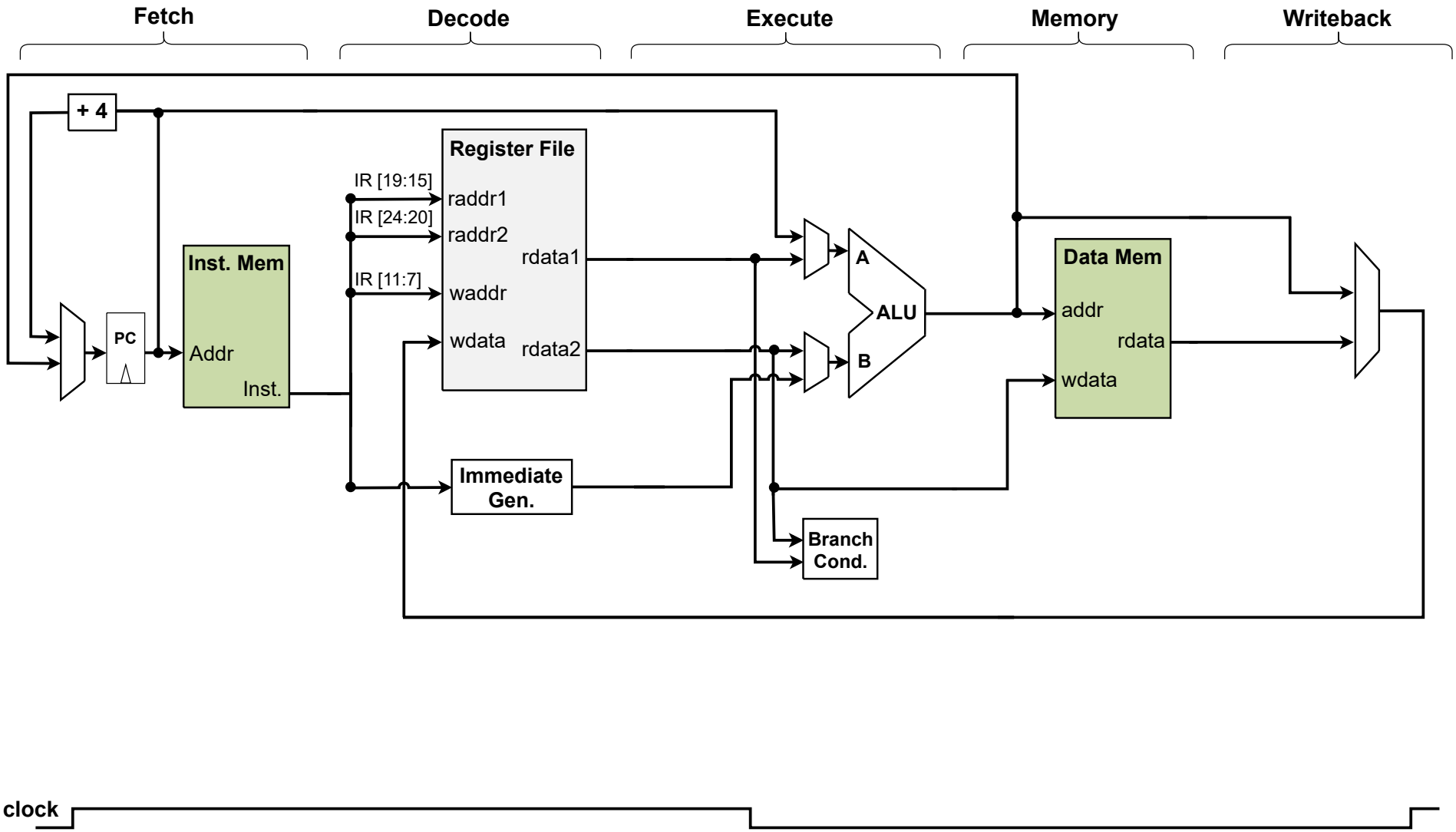
B-type: How Branch Equal Instruction Execute



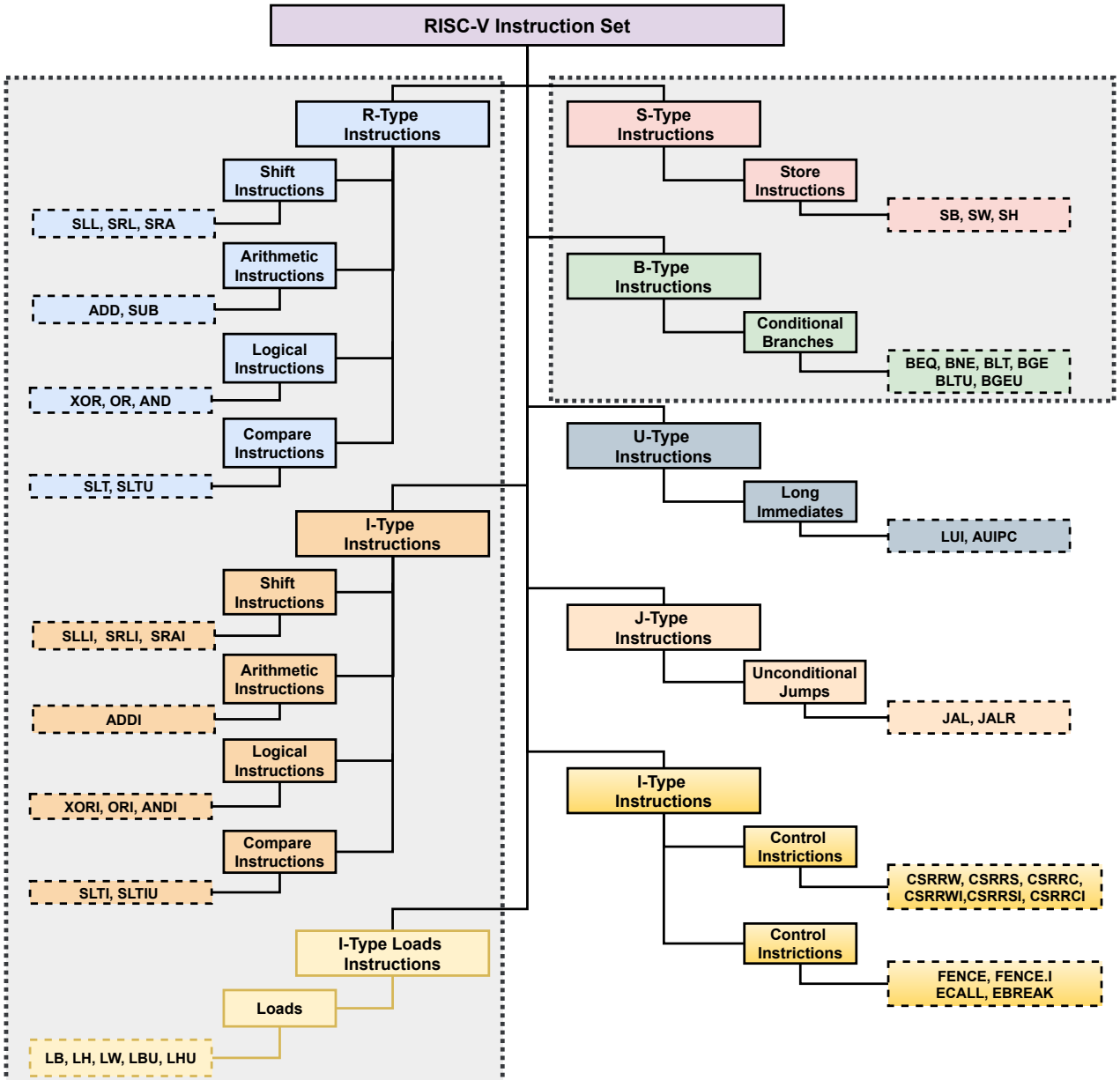
B-type: Branch Equal Instruction Execution



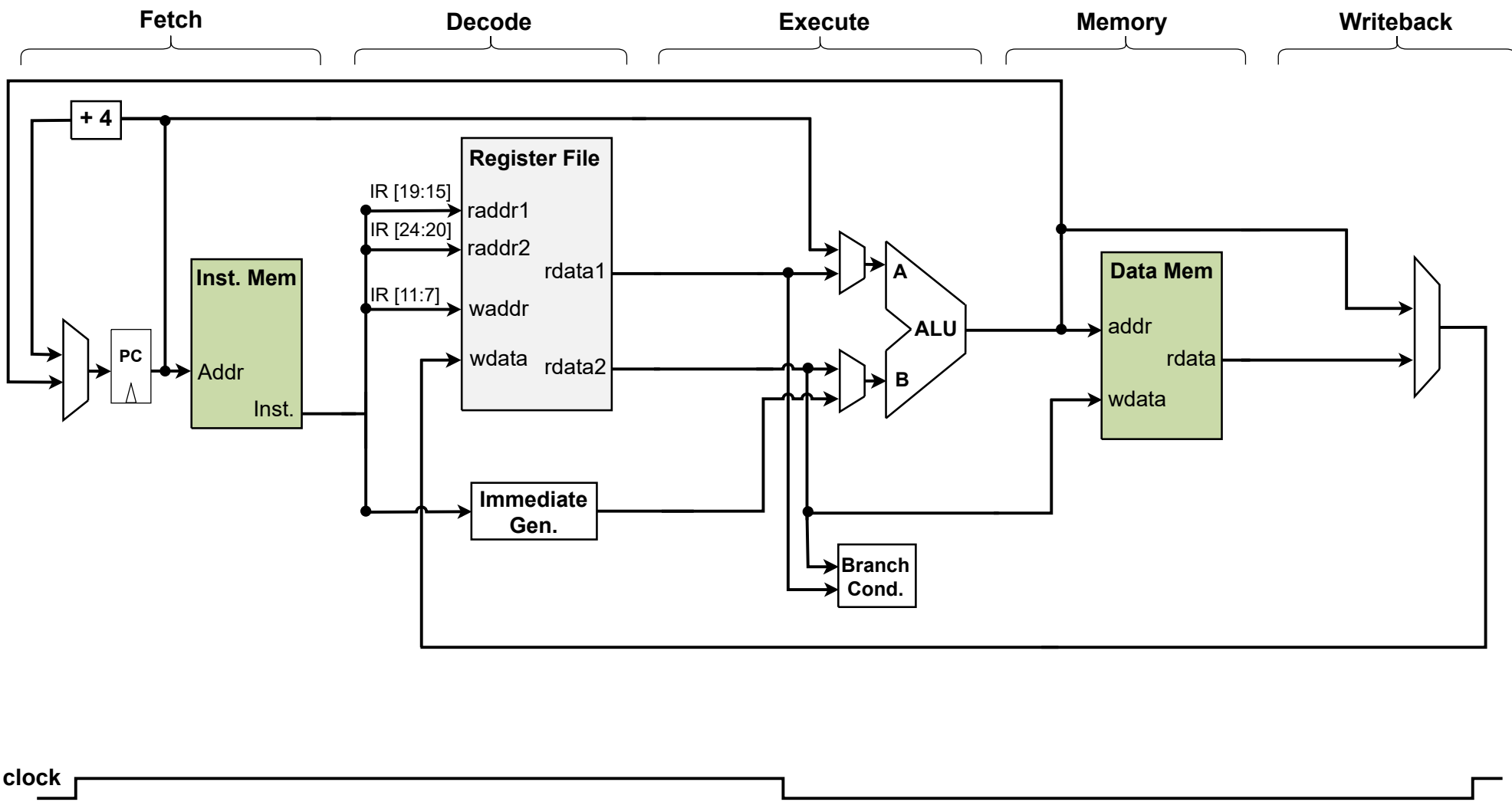
Datapath for R-, I-, S- and B-type



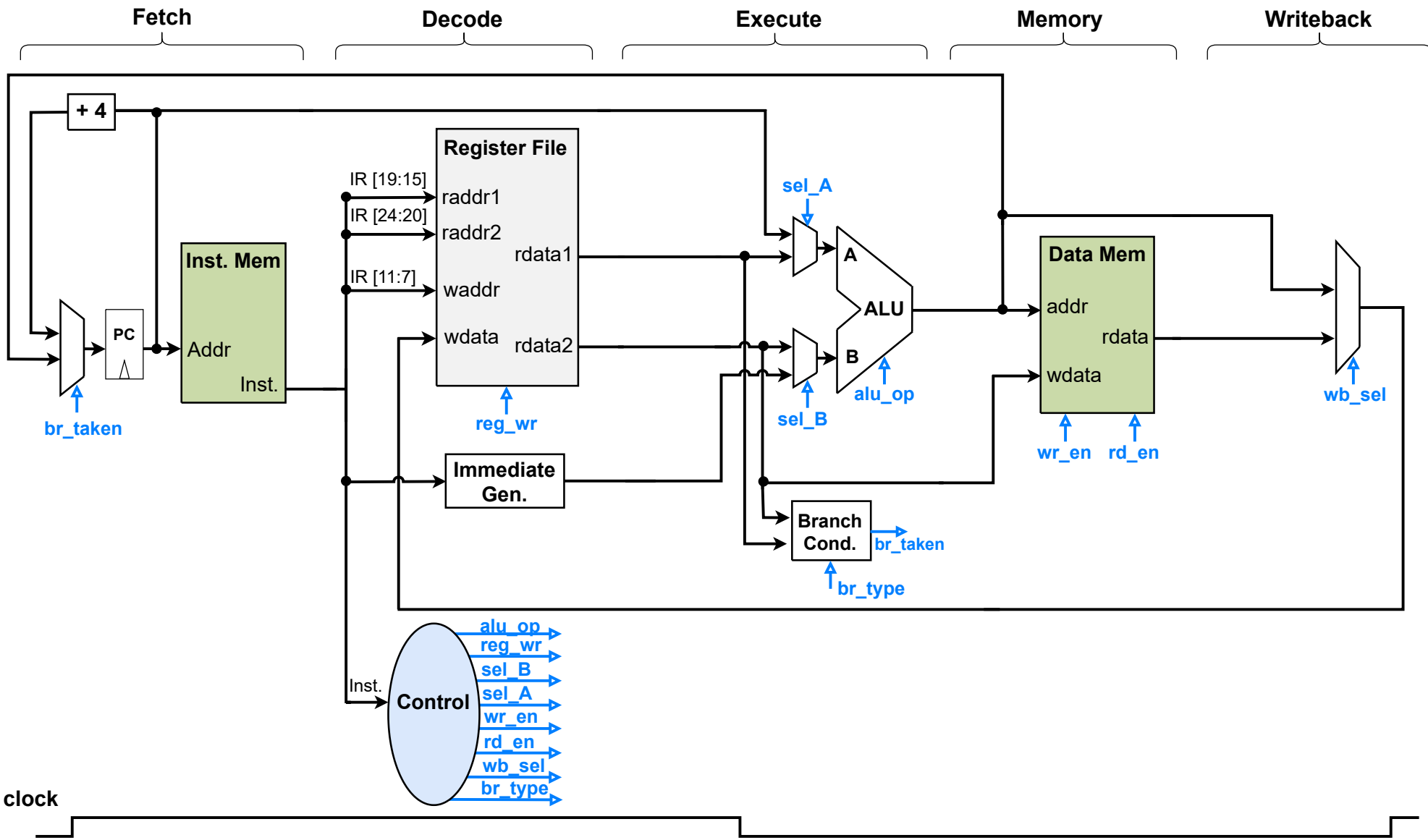
RISC-V ISA Supported by R-, I-, S- and B-type



U-type: Immediate Generation

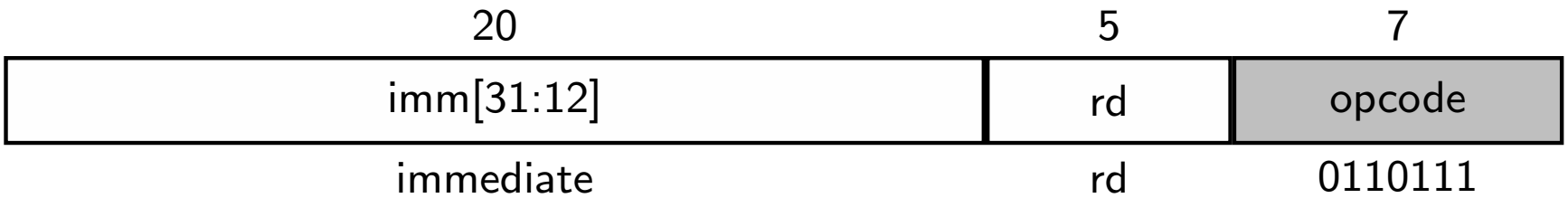


U-type: Datapath and Control



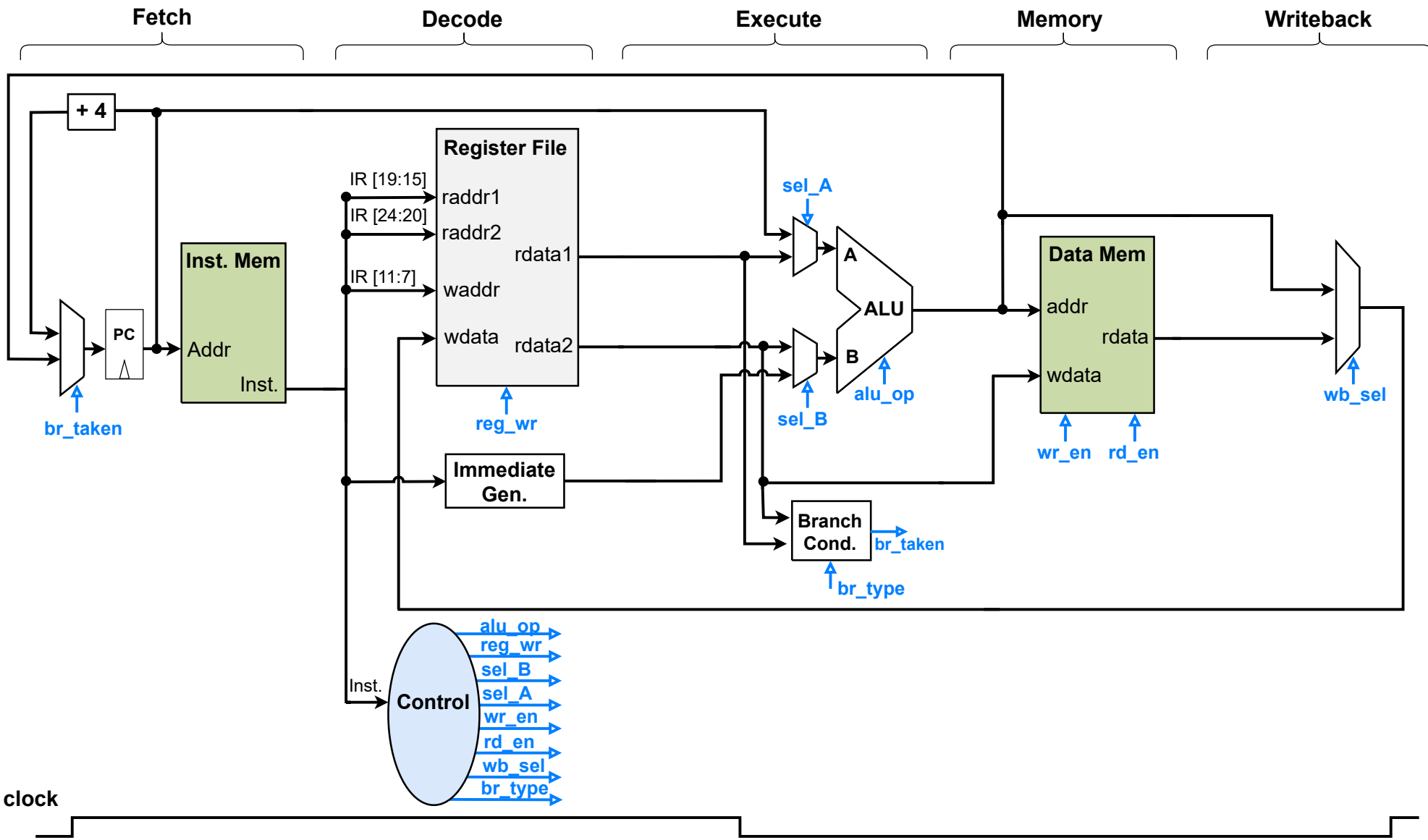
U-type: Load Upper Immediate Example

- U-type: LUI example

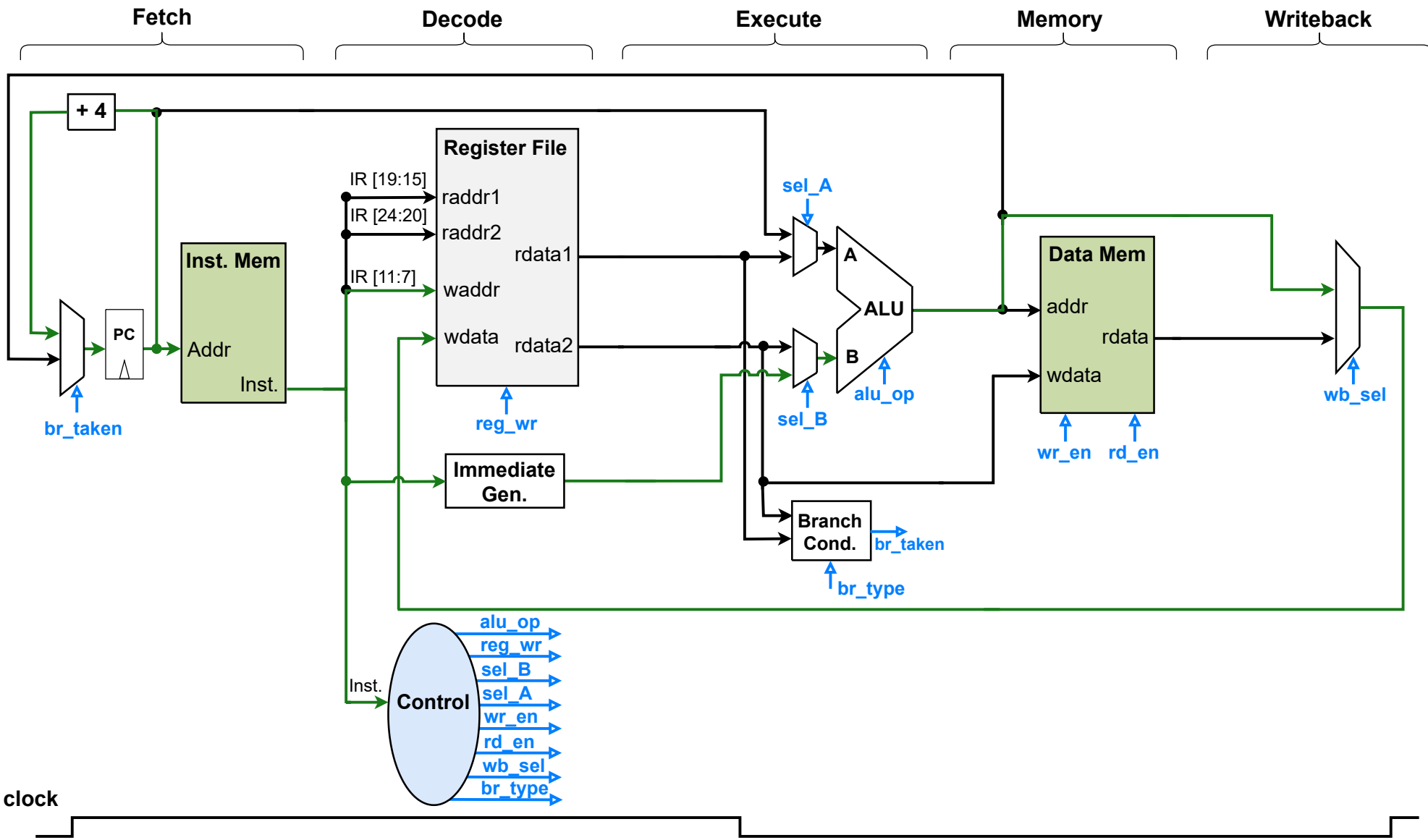


- `U-imm` = inst[31:12], 12'b0
- `opcode` = LUI : rd $\leftarrow$ U-imm
- `opcode` = AUIPC : rd $\leftarrow$ pc + U-imm

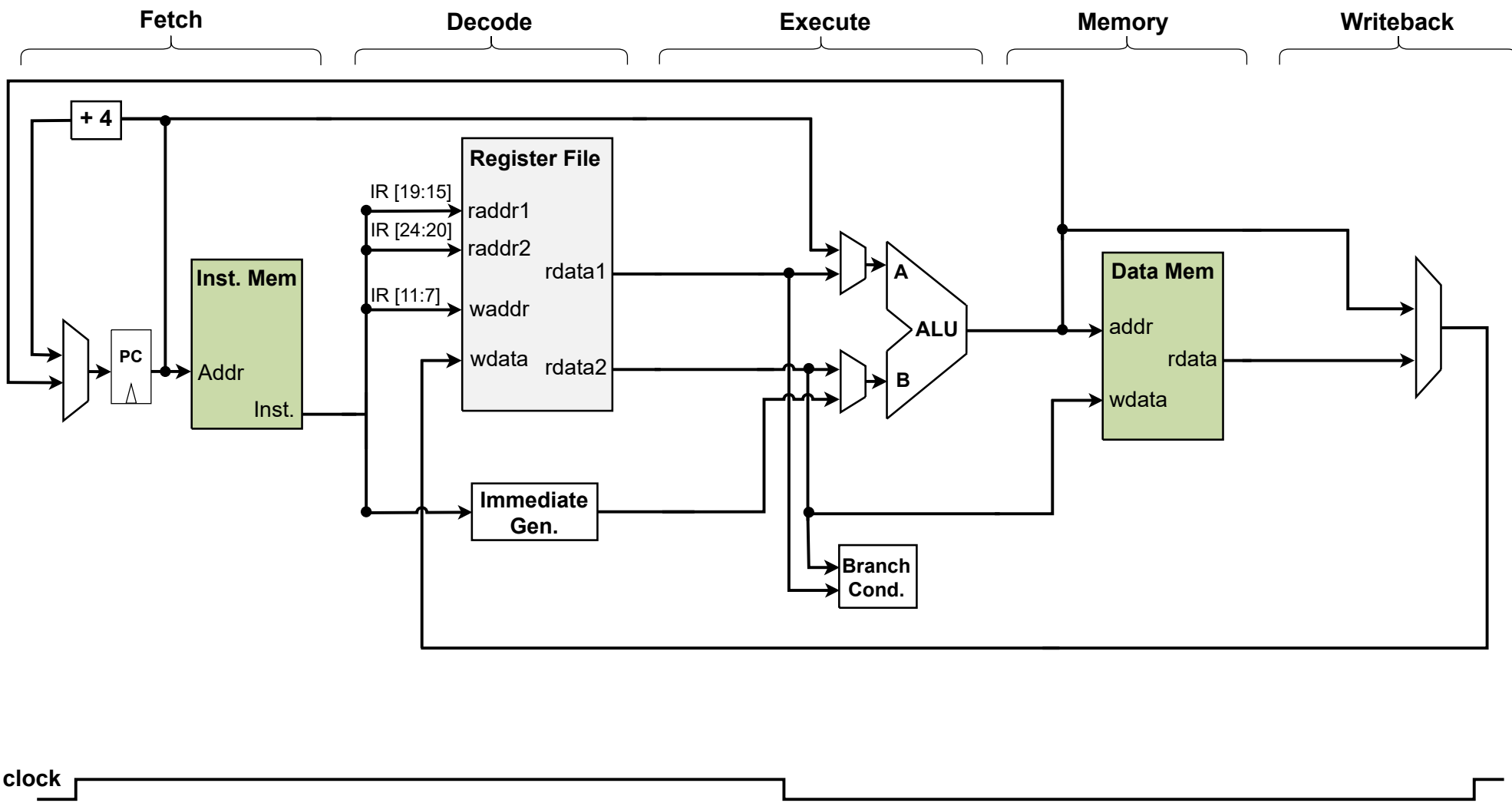
U-type: How LUI Instruction Execute



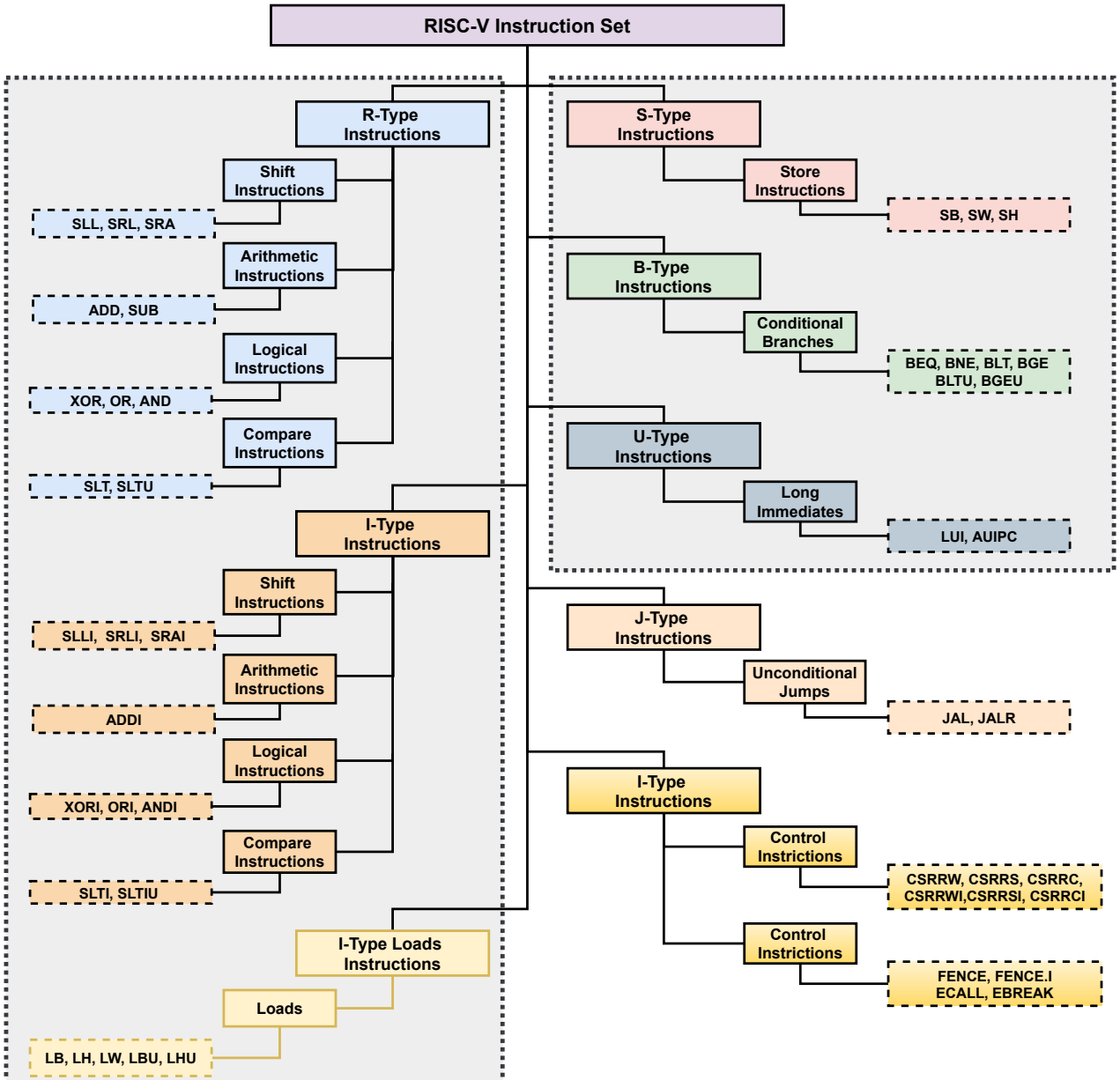
U-type: LUI Instruction Execution



Datapath for R-, I-, S-, B- and U-type

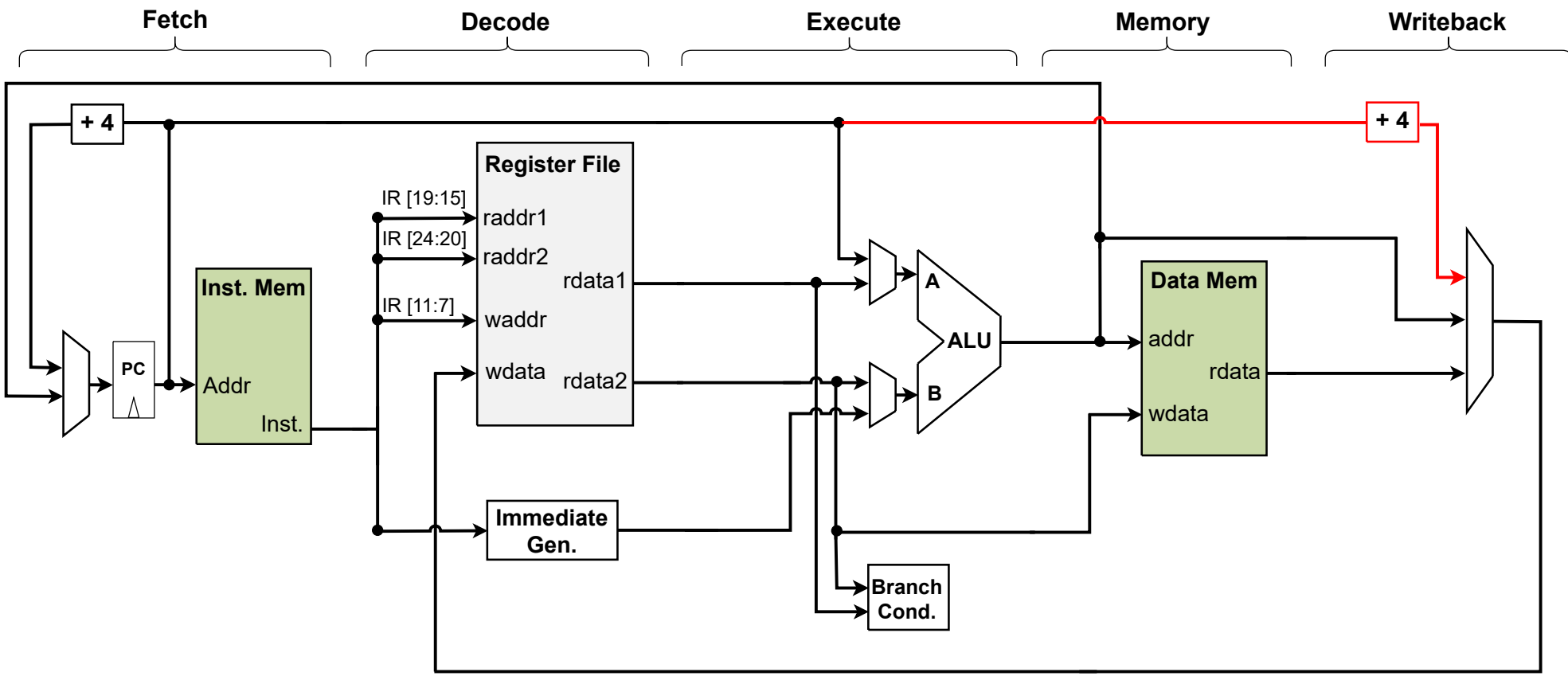


RISC-V ISA Supported by R-, I-, S-, B- and U-type

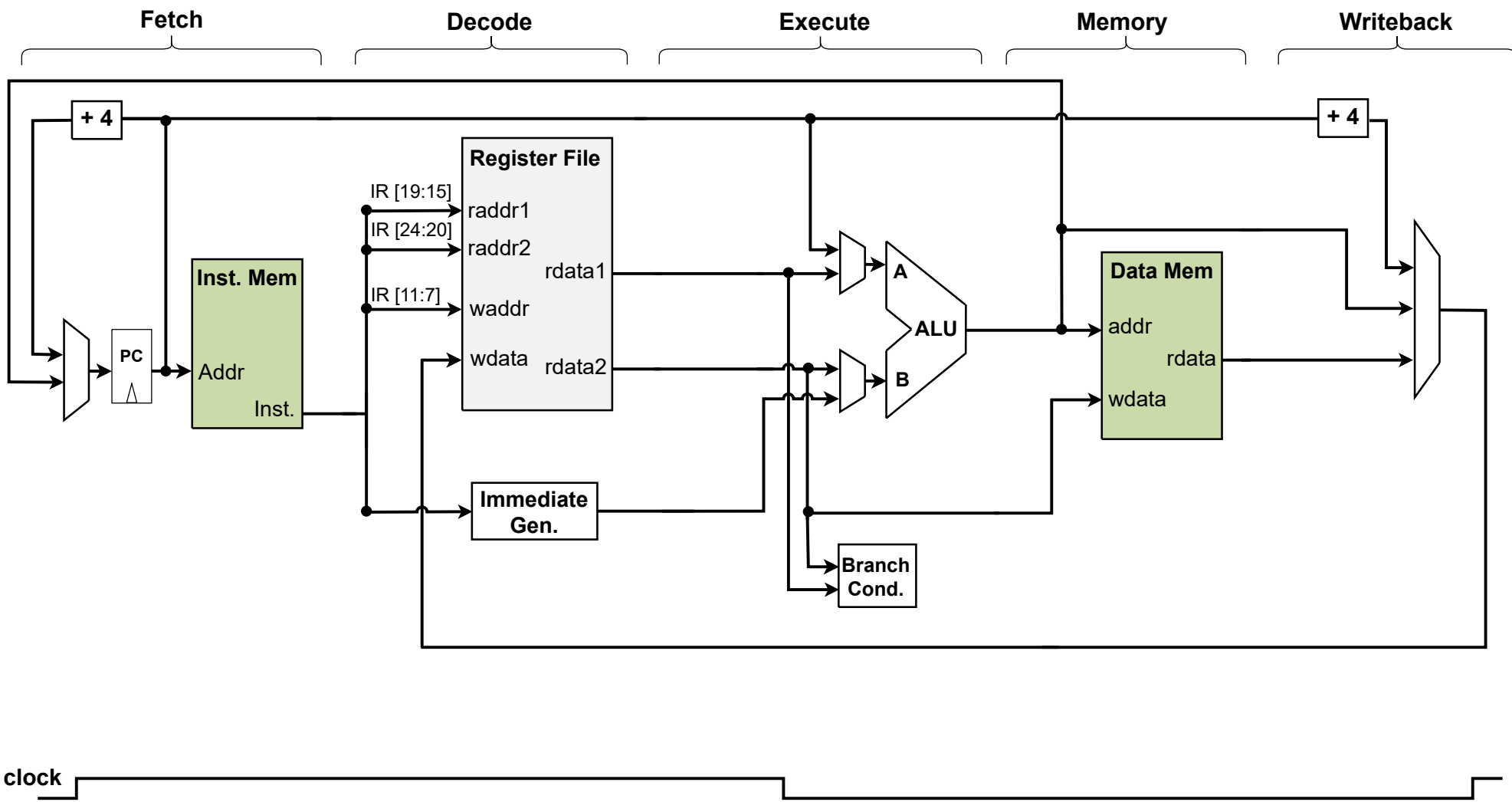


J-type: Jump Instructions

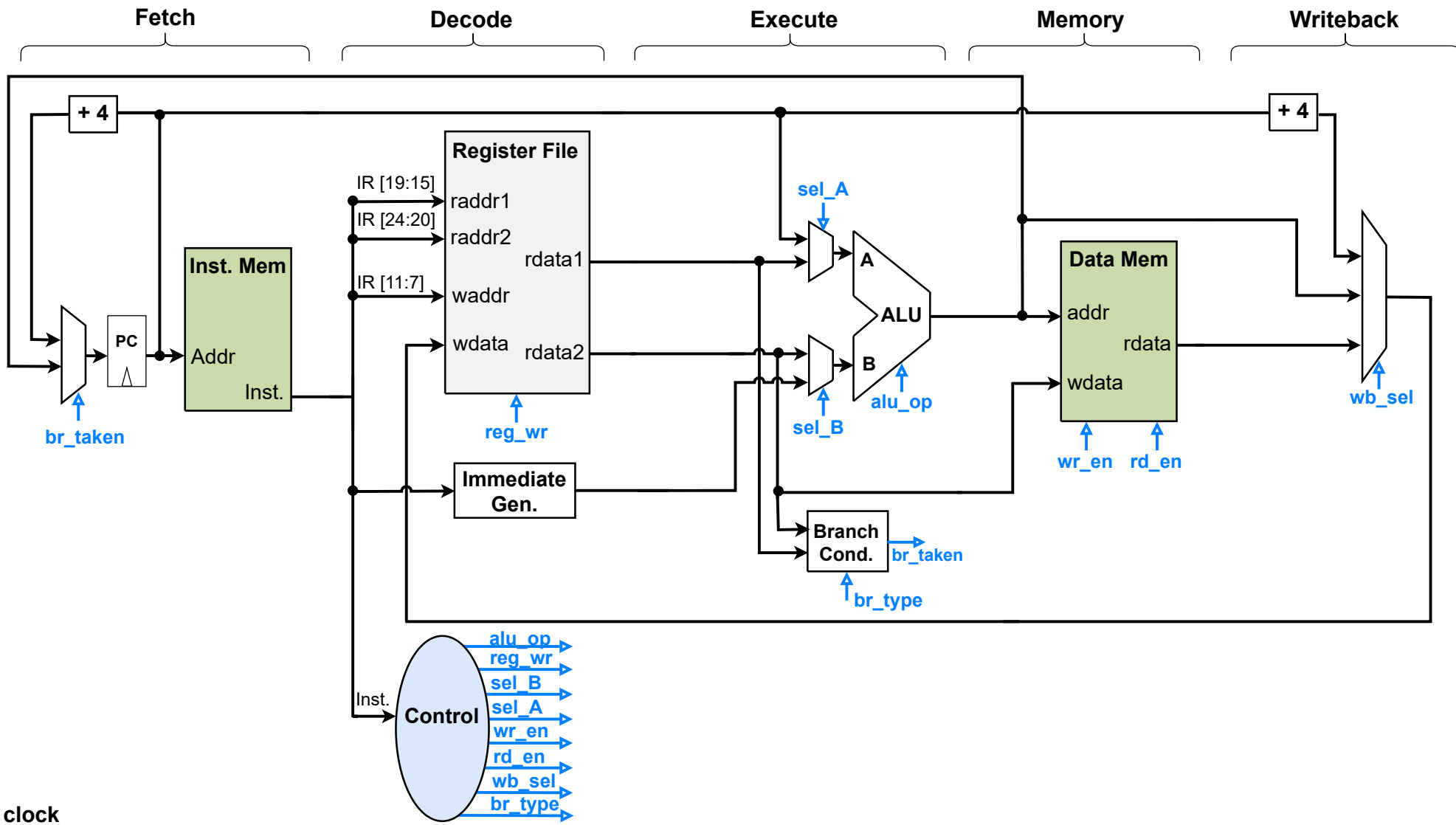
- Unconditional Jumps



J-type: Jump Instructions

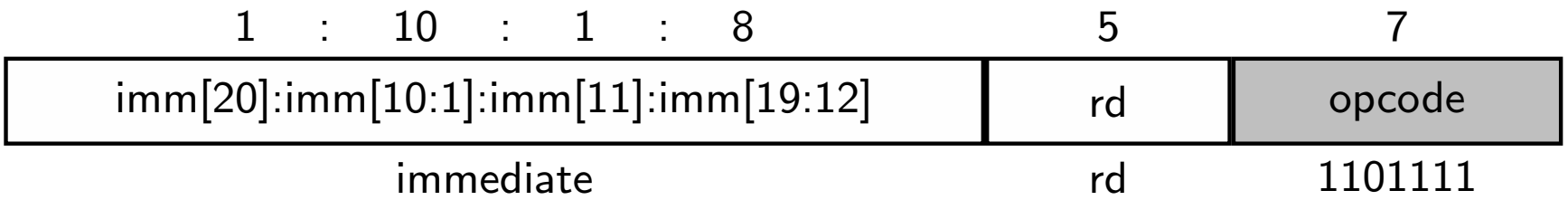


J-type: Datapath and Control



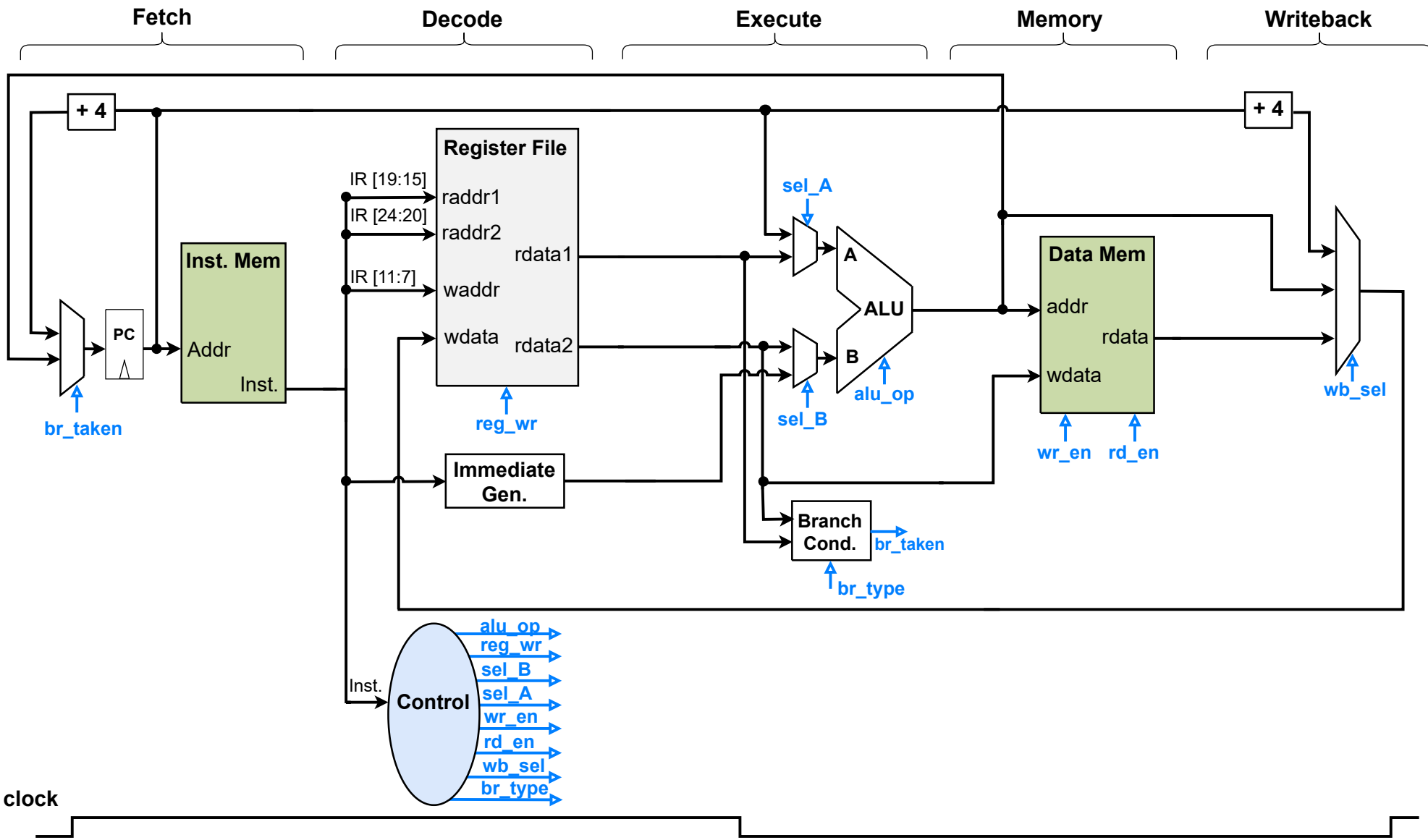
J-type: Jump and Link (JAL) Instruction

- Format: J-type

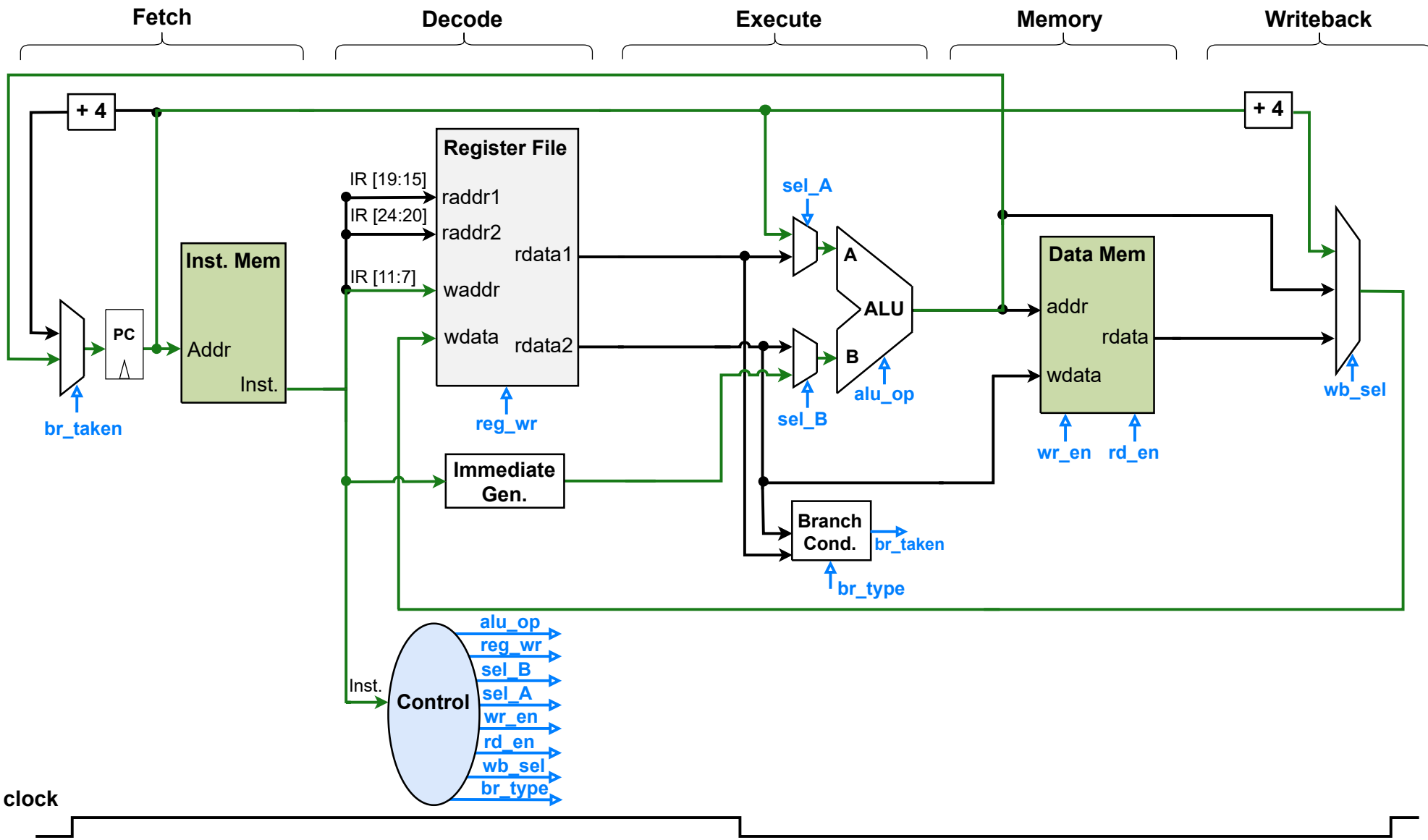


- `J-imm` = signExtend(inst[31], inst[19:12], inst[20], inst[30:21], 1'b0)
- `opcode` = JAL: rd $\leftarrow$ pc + 4;
  pc $\leftarrow$ pc + J-imm
- `Jump` = $\pm$1MB range

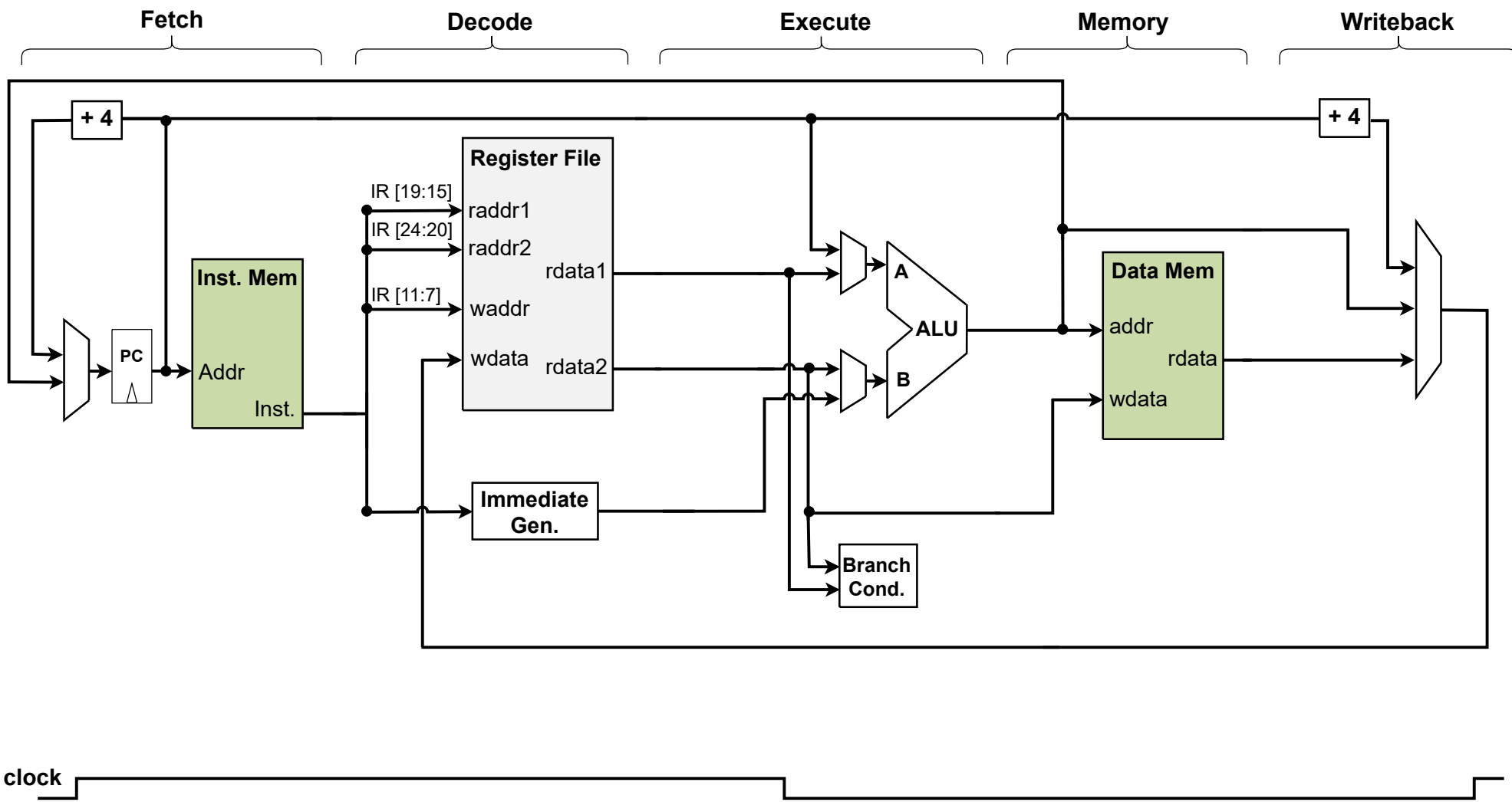
J-type: How JAL Instruction Executes



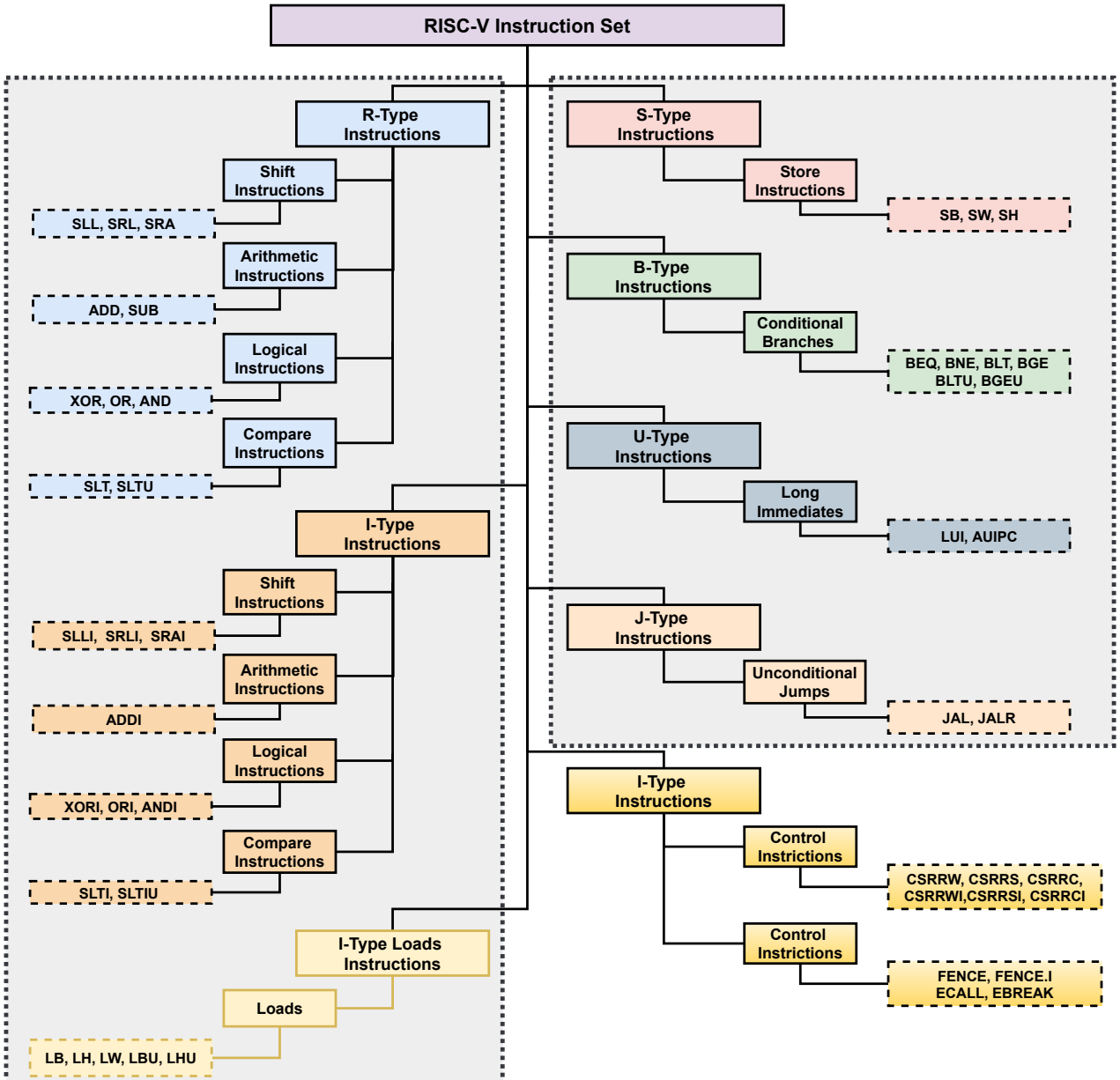
J-type: JAL Instruction Execution



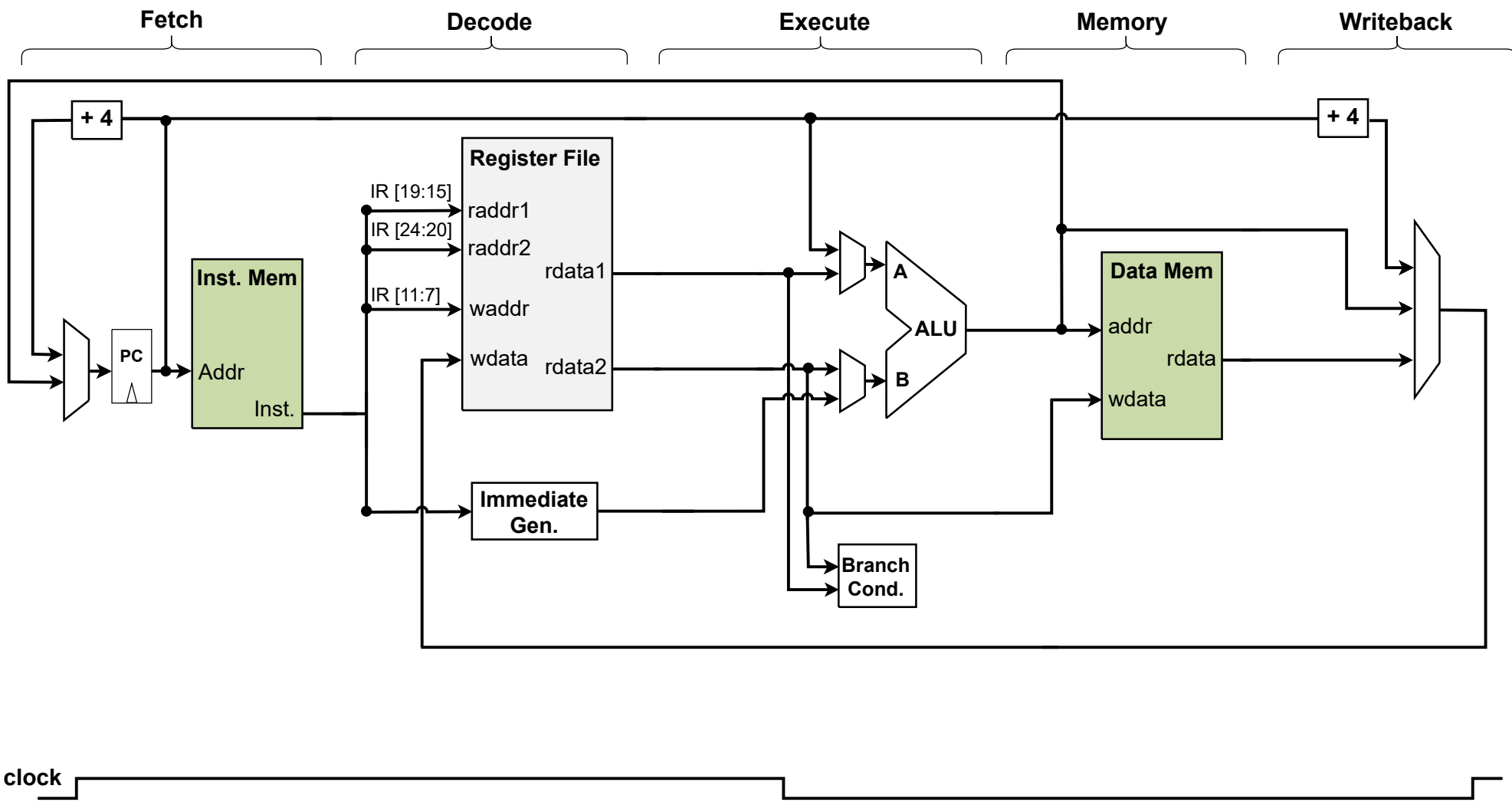
Datapath for R-, I-, S-, B-, U- and J-type



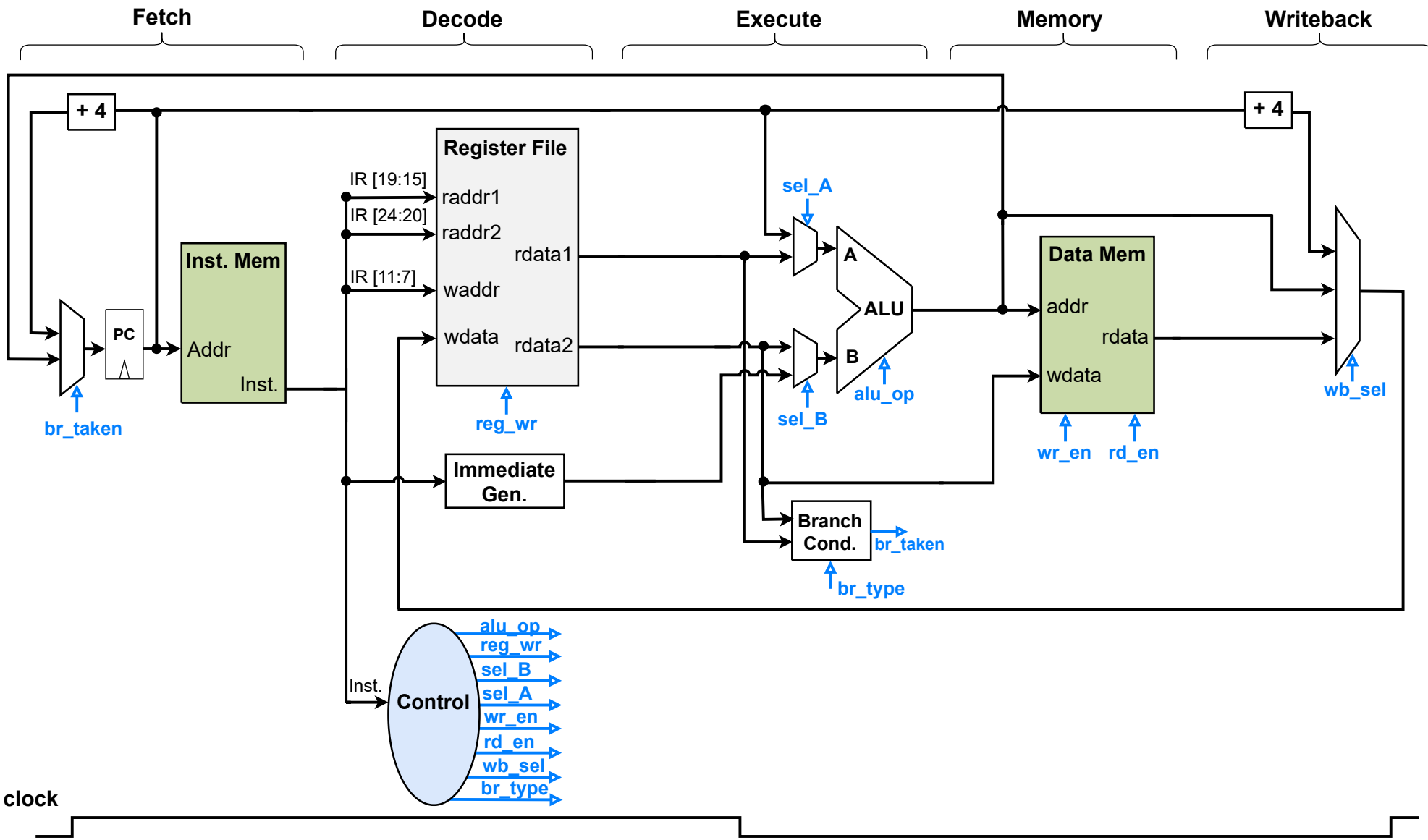
RISC-V ISA Supported by R-, I-, S-, B-, U- and J-type



Single Cycle Datapath



Single Cycle Datapath and Controller



Suggested Reading

- Read relevant sections of Chapters 2 and 4 of [Patterson and Hennessy, 2017].

Acknowledgment

- Preparation of this material was partly supported by Lampro Mellon Pakistan.

References

Patterson, D. and Hennessy, J. (2017).

Computer Organization and Design RISC-V Edition: The Hardware Software Interface.

Morgan Kaufmann.