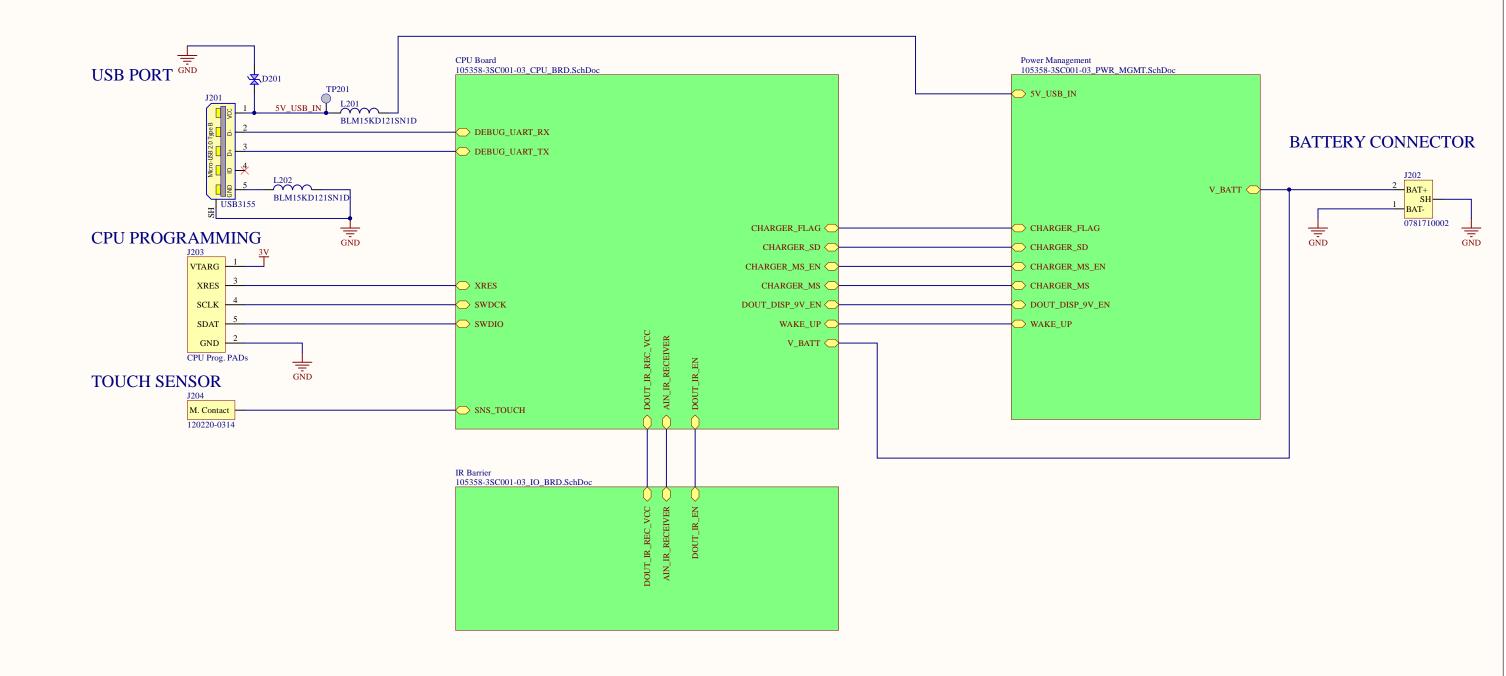
## Electronics Field Prototype 1 Schematic version 105358-3SC001-03-E

Block diagram 105358-3SC001-03\_BlockDiagram.SchDoc

- 2 Block Diagram
- 3 Power Management
- 4 CPU
- 5 IR Barrier

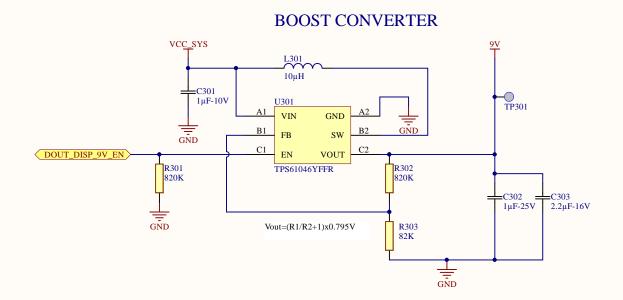
## Block Diagram

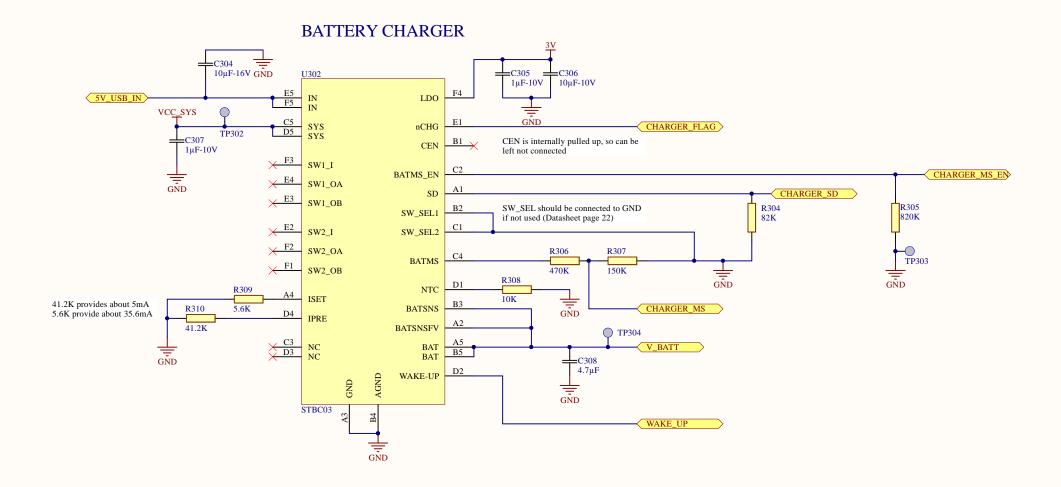






## Power Management





		Customer, project			Boa	rd			
	- HOTSWAP	Innovation Zed				EFP1			
	- HOLOWAP	Title			Dra	wn By		Si	ize
	LIFELOOIENIOE	Power Management				Kartik Karuna			<b>A</b> 3
	LIFE+SUIENCE	Document Number	Sheet	of	Last modified	Rev	Build		7
		105358-3SC001-03	3	5	2018-03-0	5 E	209 [Out	01	D

GND GND GND R401 P25 43R AUX\_CONTROL DOUT\_DISP\_RESET P07 (SWDCK) BLM21PG331SN1D BLE\_VDD VDD TP401 I2C\_SDA DEBUG\_UART\_TX P04 (RX, i2cSDA) **RESET SWITCH** PTS830GG140 =C401 0.1μF-10V -GND 6 LXES15AAA1-133 RESET\_SWITCH SW401 Bounce time: 10 ms using 41.2 KOhm and  $0.1 \mu F$ Do Not Place I2C\_SCL TP402 **MOUNTING SWITCH** R406 One Pad of R406 is used as a test point for PCBA testing Do Not Place TP403 ESE-16J001 **D**403 MOUNT\_SWITCH Q401 Ę GND \* CSD23382F4 VCC\_SYS Q402 CSD13380F3T AUX\_3V R410 5.6K 22μF CHARGER\_SD Ę GND I2C R412 AUX\_CONTROL CSD23382F4 C404 2.2μF-16V R413 I2C\_SCL IREF TP405 SCL SDA SCI DOUT\_DISP\_RESET RES# AUX\_3V TP406 DOUT\_DISP\_3V enabled from 9V input VDD Write protection disabled  $\overline{\text{WC}}$ VSS Ū GND VDDB **I2C EEPROM** C1N Device select code when addressing the memory array (b101 0000) Device select code when accessing the Identification page (b101 1000) I2C DISPLAY (b111 1000) C2N  $\Xi$  C2P  $\longrightarrow$ 5034801400 EFP1 **HOTSWAP** Drawn By Kartik Karuna 

## IR Barrier

