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Exp. 9

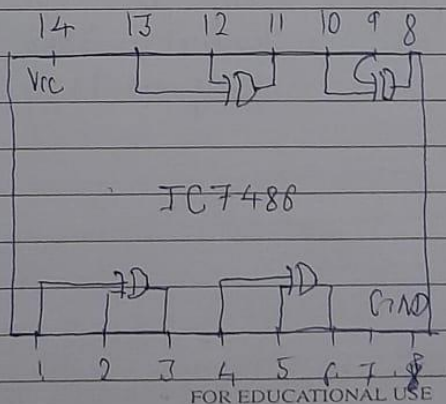
Aim: To design 2 bit synchronous counter using D flip-flop (MOD 4)

Apparatus: Breadboard, connecting with Led board, power supply, IC 7474, IC 7486

Theory:-

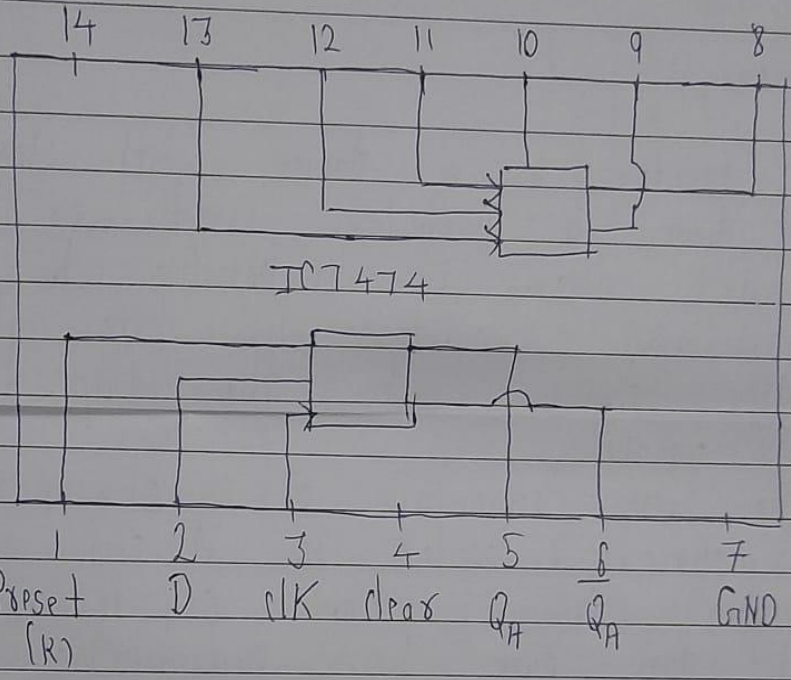
A counter is a device which stores the number of times a particular event or process has occured, often in relationship to a clock signal. Synchronous counter has one global clock which drives each flip-flop so output changes in parallel.
The one advantage of synchronous counter over asynchronous counter is, it can operate on higher frequency than asynchronous counter as it does not have cummulative delay.

Pin diagram:-



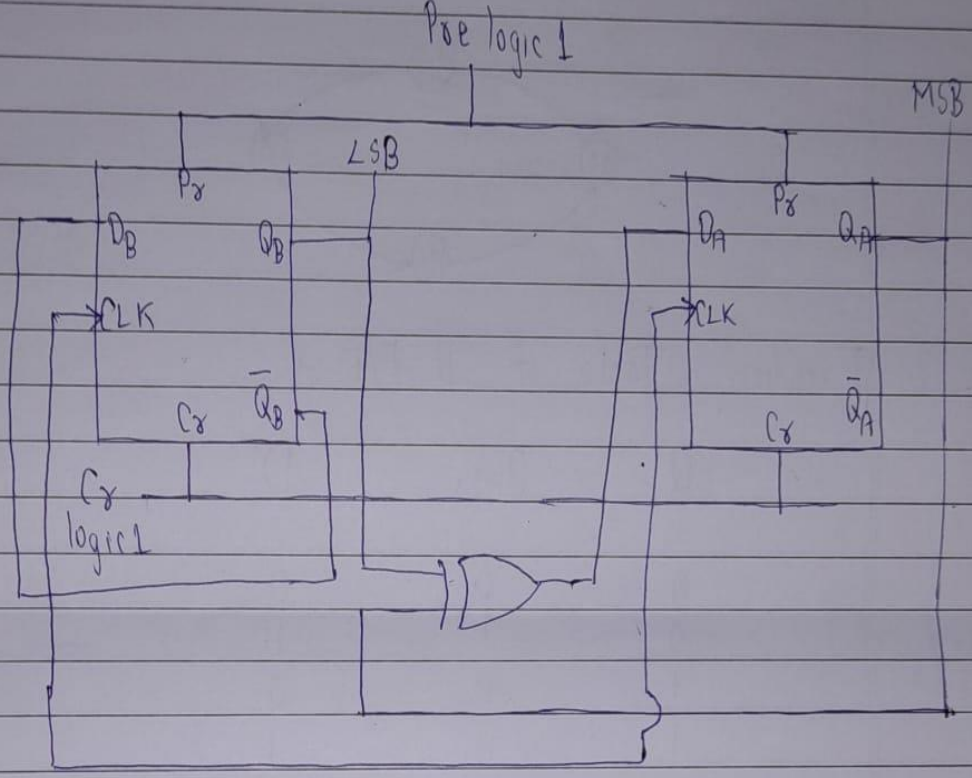
Quad 2 - Input Exclusive - OR gate :-

This device contains four independent gates each of which performs the logic exclusive - OR fraction.

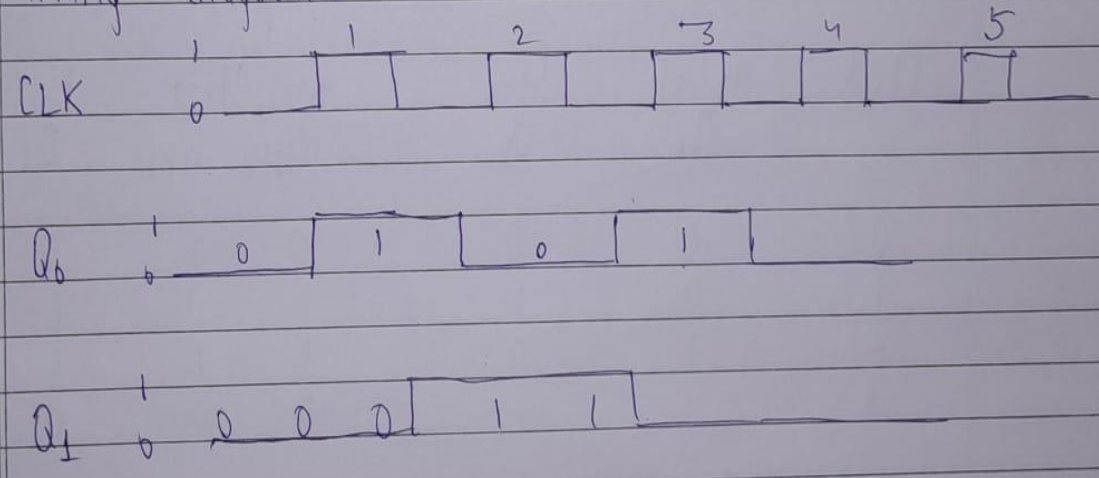


The dual edge triggered flip-flop utilizes circuitry to produce high speed D-type flip-flops. Each flip-flops has individual clear and not set inputs and also compumentary Q and $\overline{Q}$

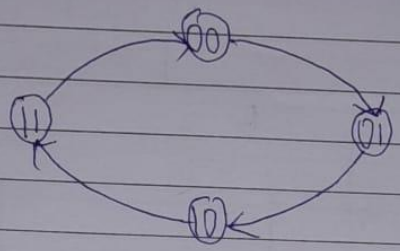
Circuit diagram :-



Timing diagram :-



Exact state diagram :-



Execution Table of D F/F :-

Q	Q_{t+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

State Transition table :

Clock	Present State Q_A	Q_B	Next State Q_{A+1}	Q_{B+1}	F/F control D_A	D_B
0	0	0	0	1	0	1
1	0	1	1	0	1	0
2	1	0	1	1	1	1
3	1	1	0	0	0	0

D_A

Q_B / D_A	0	1
0	0	1
1	1	0

$D_A = Q_A \oplus Q_B$

$Q_A \rightarrow MSB$
$Q_B \rightarrow LSB$

D_B

Q_B / Q_A	0	1
0	1	1
1	0	0

$D_A = \overline{Q_B}$

Conclusion:
I have understood the concept of synchronous counter using D flip-flops.

Synchronous counter using D flip flop