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I011

Exp: 2 LDCA

Aim : Realization of logic gates using NAND and NOR Gates

Components : IC 7400, 7402

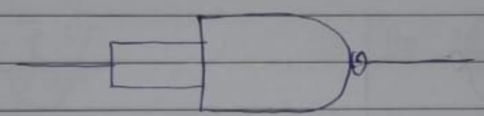
Apparatus : Digital trainer, wire, etc

Theory :

The NAND and NOR gates are called as universal gates, because it is possible to implement any Boolean expression with the help of only NAND or NOR gates.

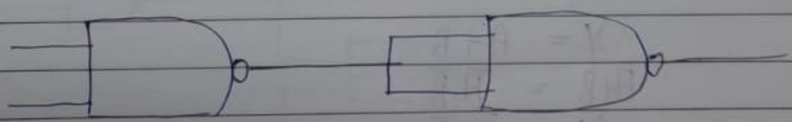
All gates using NAND Gates →

1 NOT using NAND



$\therefore Y = \overline{A}$

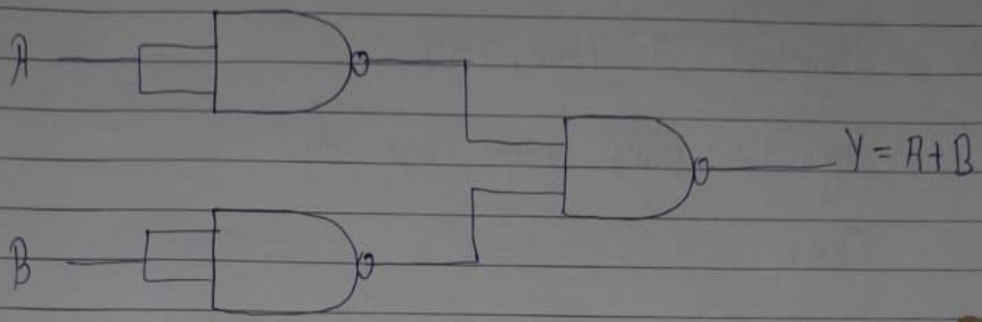
2 AND using NAND



$Y = \overline{\overline{A.B}}$ $\because \overline{\overline{A}} = A$

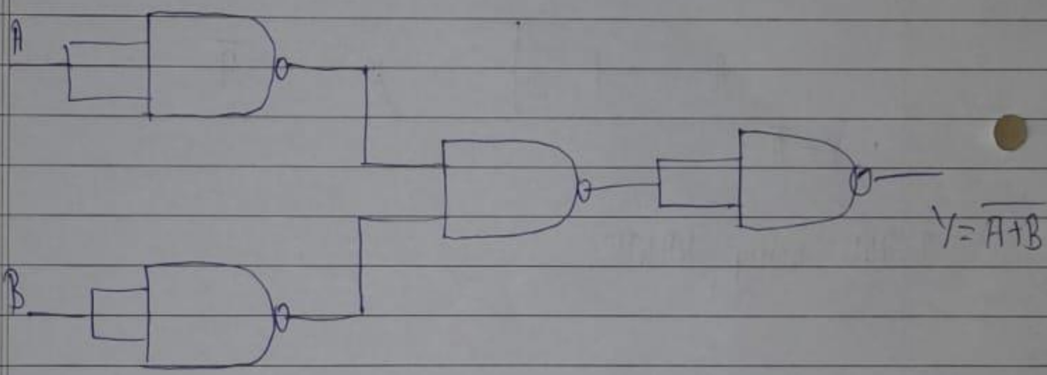
$Y = A.B$

3 OR using NAND



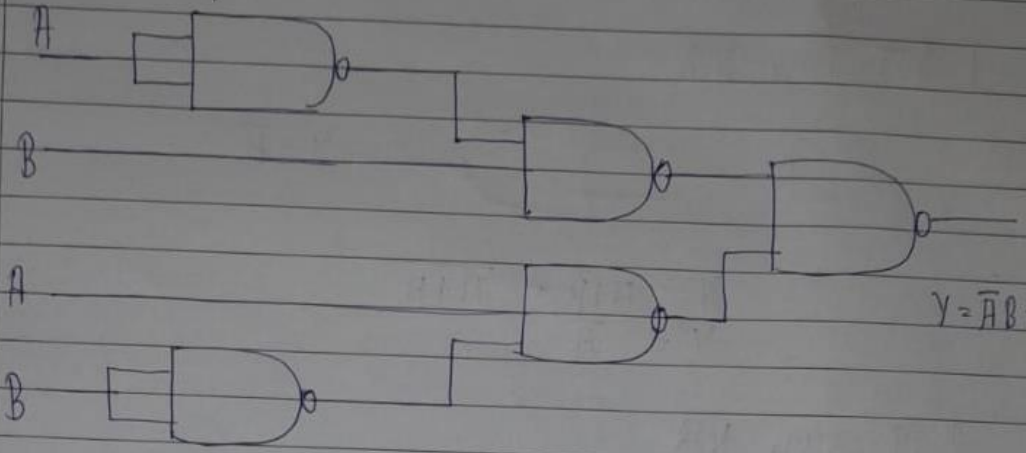
$$Y = \overline{A+B}$$
$$\overline{A+B} = \bar{A}\cdot\bar{B} \quad \text{—— (De - Morgan's Theorem)}$$
$$Y = \overline{\bar{A}\cdot\bar{B}}$$

4 NOR using NAND



$$Y = \overline{A+B}$$
$$\overline{A+B} = \bar{A}\cdot\bar{B}$$
$$Y = \overline{\overline{\bar{A}\cdot\bar{B}}}$$
$$Y = \bar{A}\cdot\bar{B}$$

5 EX-OR using NAND



$Y = \bar{A}B + A\bar{B}$

$Y = A \oplus B = \bar{A}\cdot B + A\bar{B}$

$Y = \overline{\overline{\bar{A}\cdot B + A\cdot\bar{B}}}$

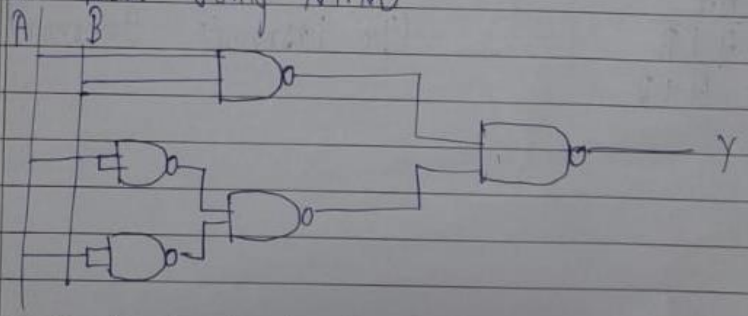
$Y = \overline{\overline{X+Z}}$ ——— $(\bar{A}\cdot B = X\ ,\ A\cdot\bar{B} = Z)$

$\overline{X+Z} = \bar{X}\cdot\bar{Z}$ ——— (De Morgan's Theorem)

$Y = \overline{\bar{X}\,\bar{Z}}$

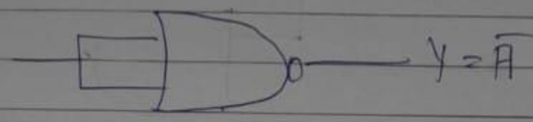
$Y = \overline{(\overline{\bar{A}B})\cdot(\overline{A\cdot\bar{B}})}$

6 EX-NOR Using NAND



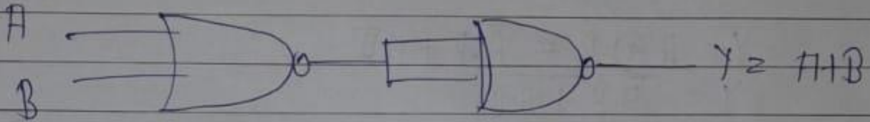
All gates using NOR Gates

1 NOT using NOR



$$Y = \overline{A+B} = \overline{A+A}$$
$$Y = \overline{A}$$

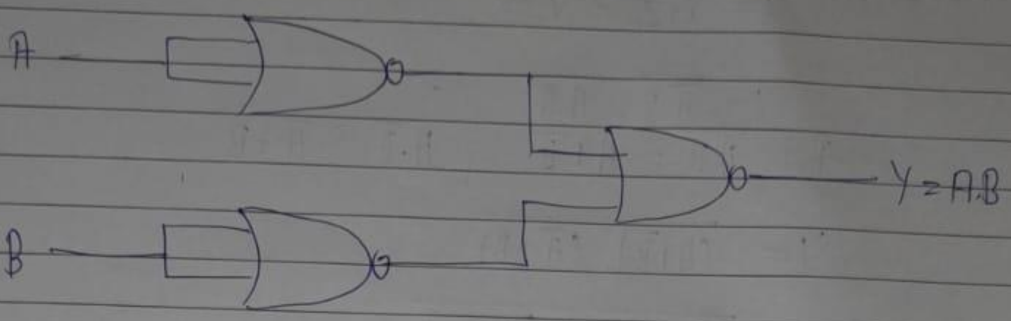
2 OR using NOR



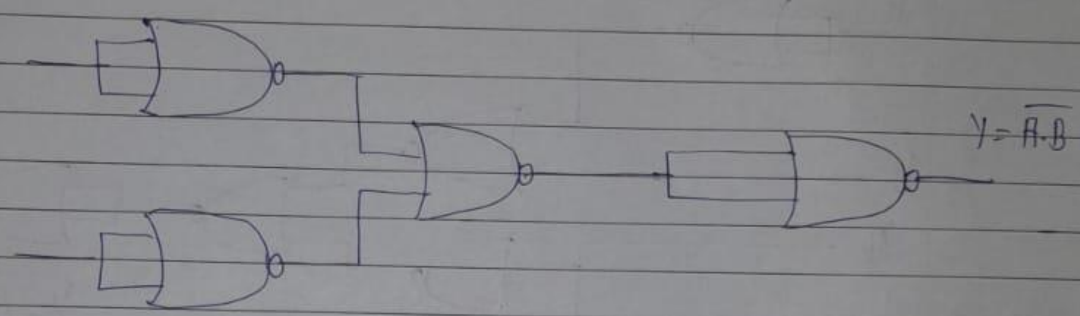
$$Y = \overline{\overline{A+B}}$$
$$\text{But } \overline{\overline{A}} = A$$
$$Y = A+B$$

3 AND using NOR

$$Y = \overline{\overline{A.B}}$$
$$\overline{A.B} = \overline{A} + \overline{B} \quad \text{— (De Morgan's Theorem)}$$
$$Y = \overline{\overline{A} + \overline{B}}$$



4 NAND using NOR



$$Y = \overline{A \cdot B}$$
$$\overline{A \cdot B} = \bar{A} + \bar{B} \quad \text{—— (De Morgan's)}$$
$$Y = \overline{\bar{A} + \bar{B}}$$

5 EX-OR using NOR

$Y = A \oplus B$

$Y = \bar{A} \cdot B + A \cdot \bar{B}$

Let $X = \bar{A} \cdot B$, $Y = A \cdot \bar{B}$

$Y = \overline{X + Z}$

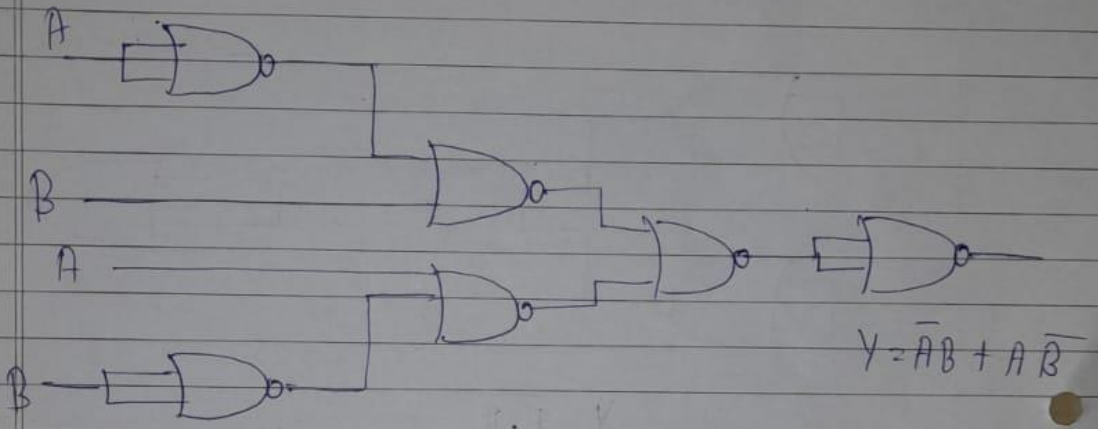
$$Y = \overline{X+Z} = \bar{X} \cdot \bar{Z}$$

$$Y = \overline{\bar{A} \cdot B} \cdot \overline{A \cdot \bar{B}}$$

But $\overline{\bar{A} \cdot B} = A + \bar{B}$, $\overline{A \cdot \bar{B}} = \bar{A} + B$

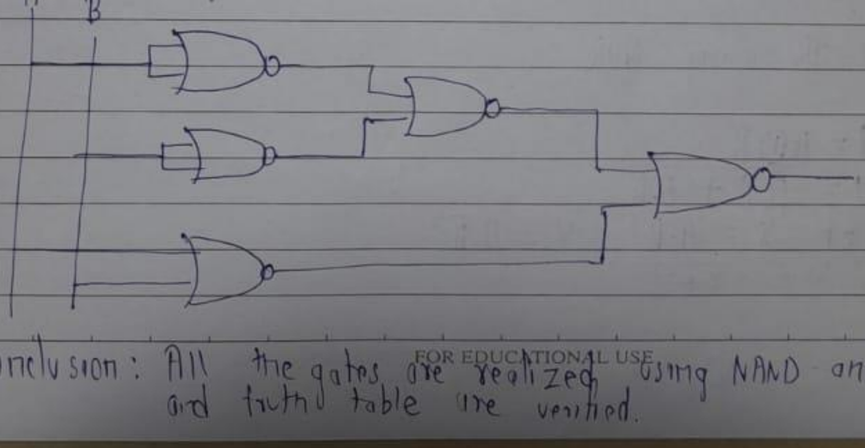
$$Y = \overline{(A+\bar{B}) \cdot (\bar{A}+B)}$$

$$Y = \overline{\overline{(A+\bar{B})} + \overline{(\bar{A}+B)}}$$

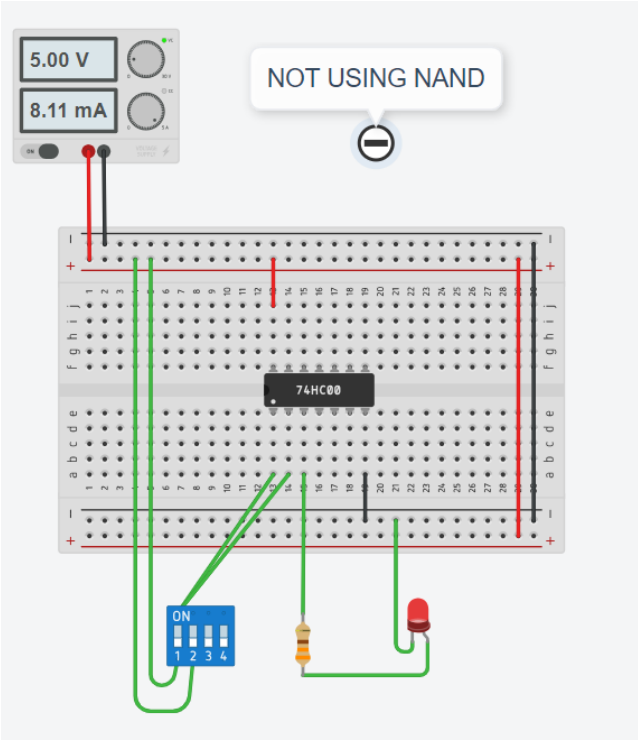


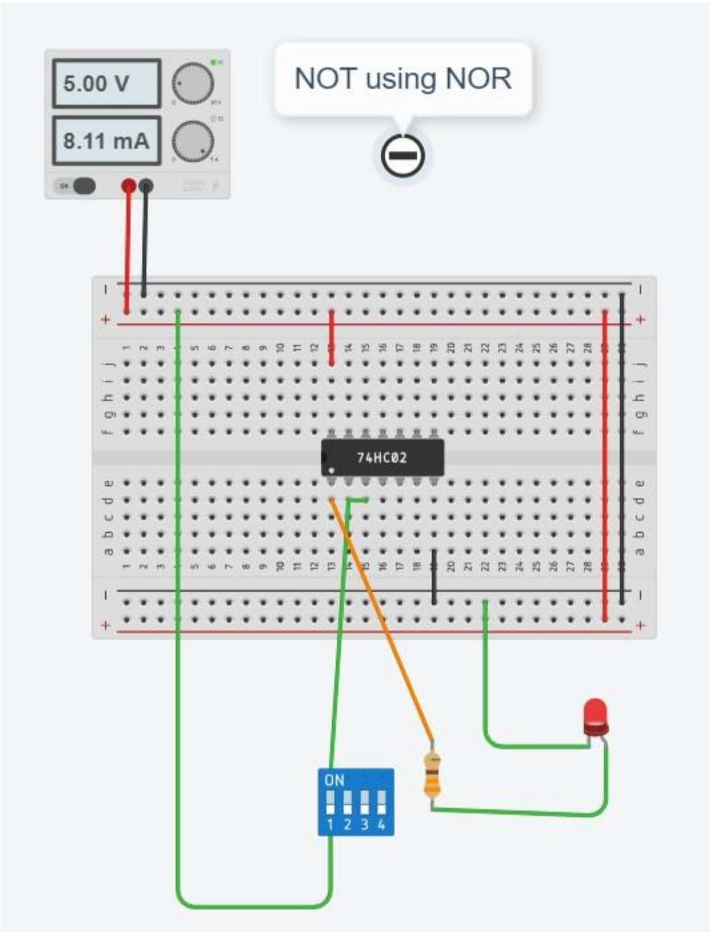
$Y = \bar{A}B + A\bar{B}$

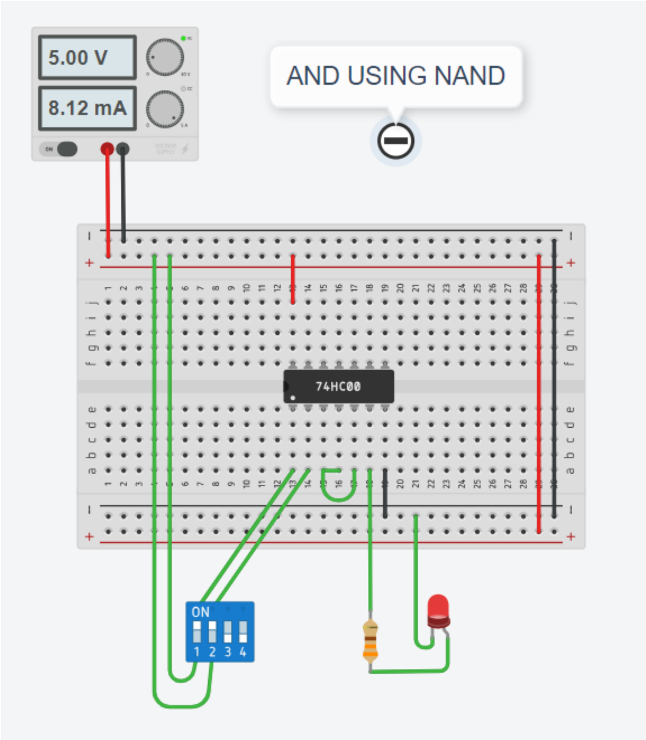
6 EX-NOR using NOR

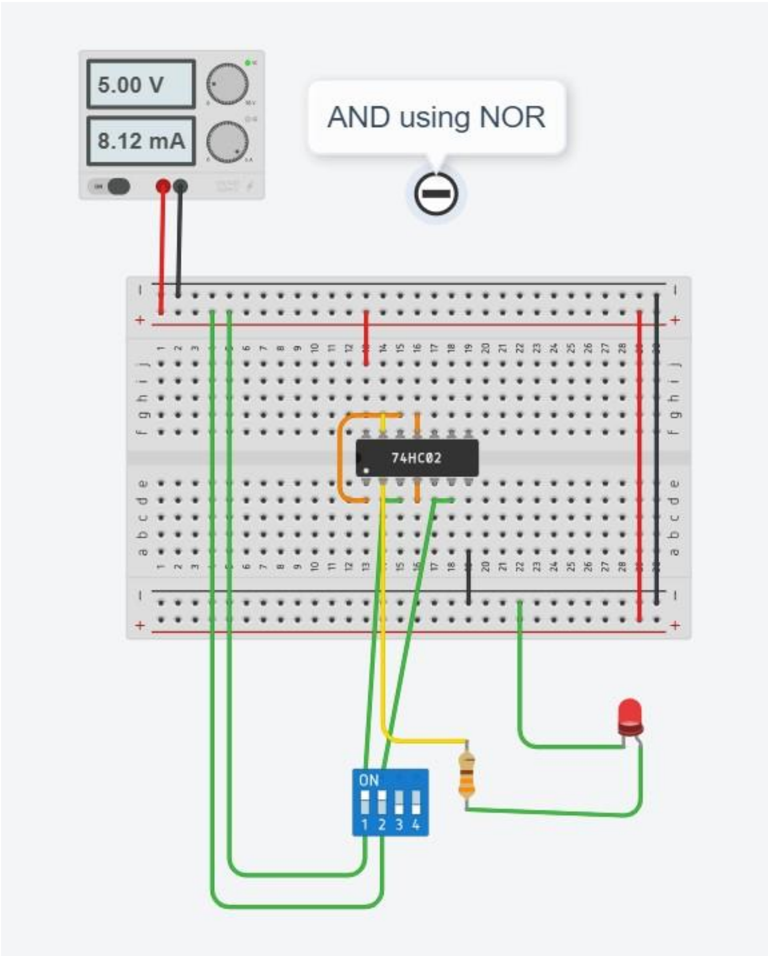


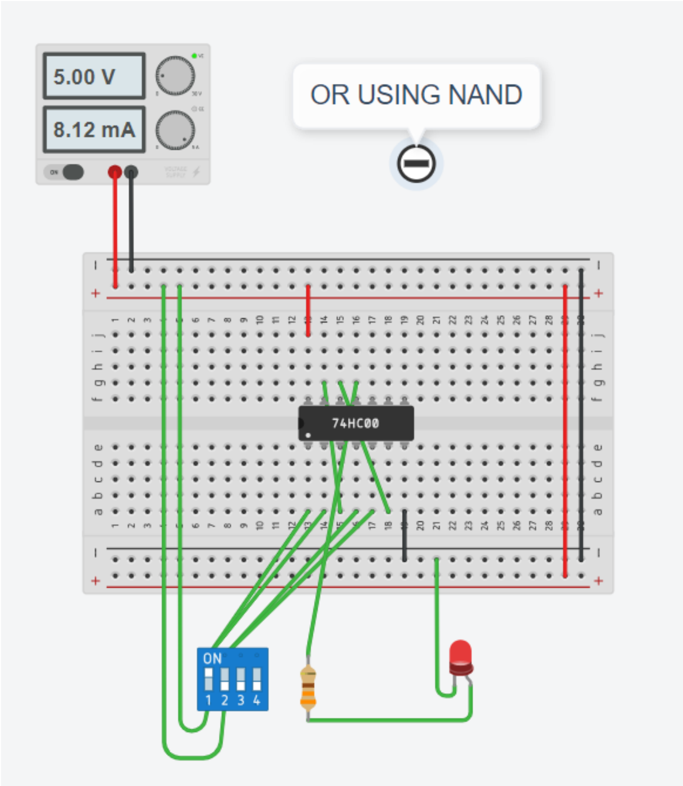
Conclusion: All the gates are realized using NAND and NOR and truth table are verified.

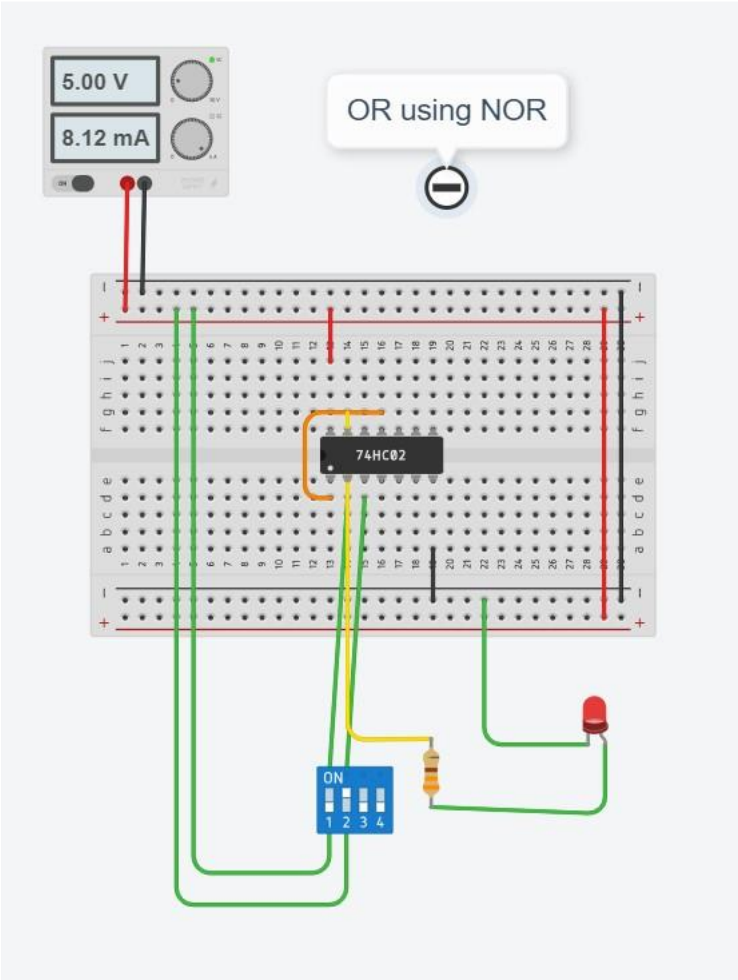

5.00 V
8.11 mA
NOT USING NAND
74HC00
ON
1 2 3 4

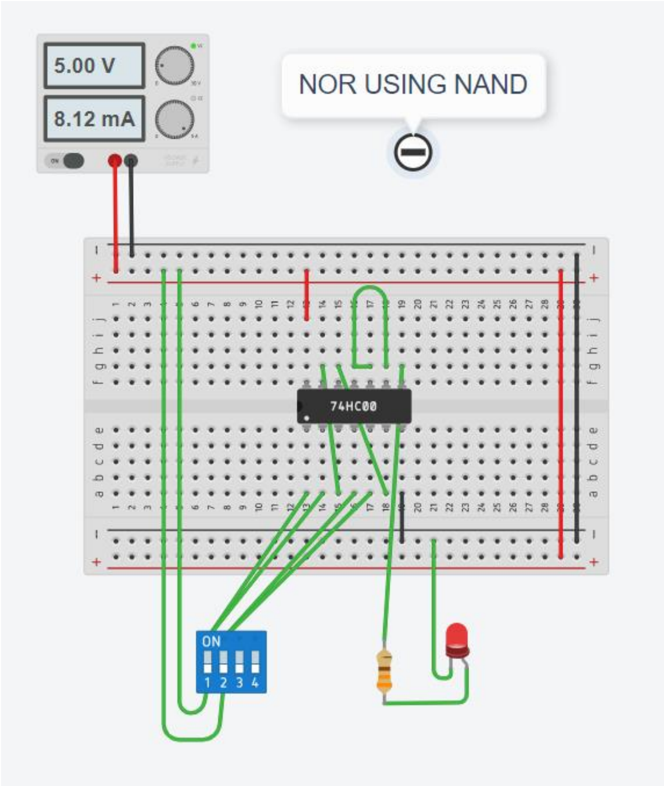

5.00 V
8.11 mA
NOT using NOR
74HC02
ON
1 2 3 4

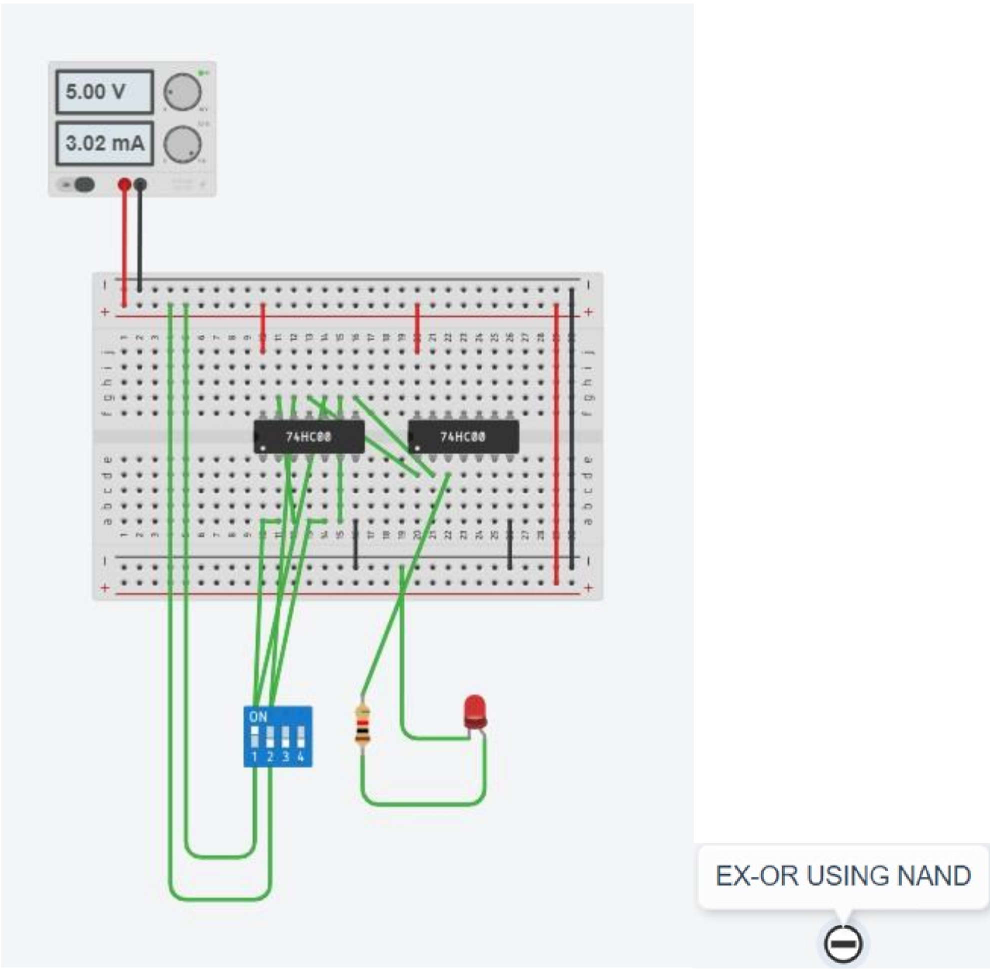

5.00 V
8.12 mA
AND USING NAND
74HC00
ON
1 2 3 4

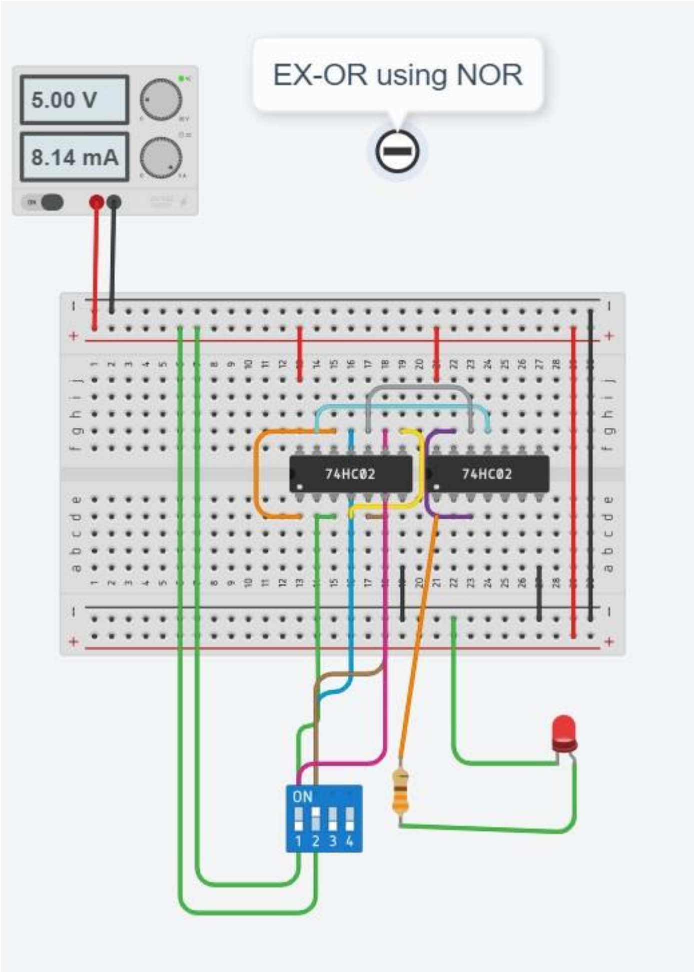

5.00 V
8.12 mA
AND using NOR
74HC02
ON
1 2 3 4

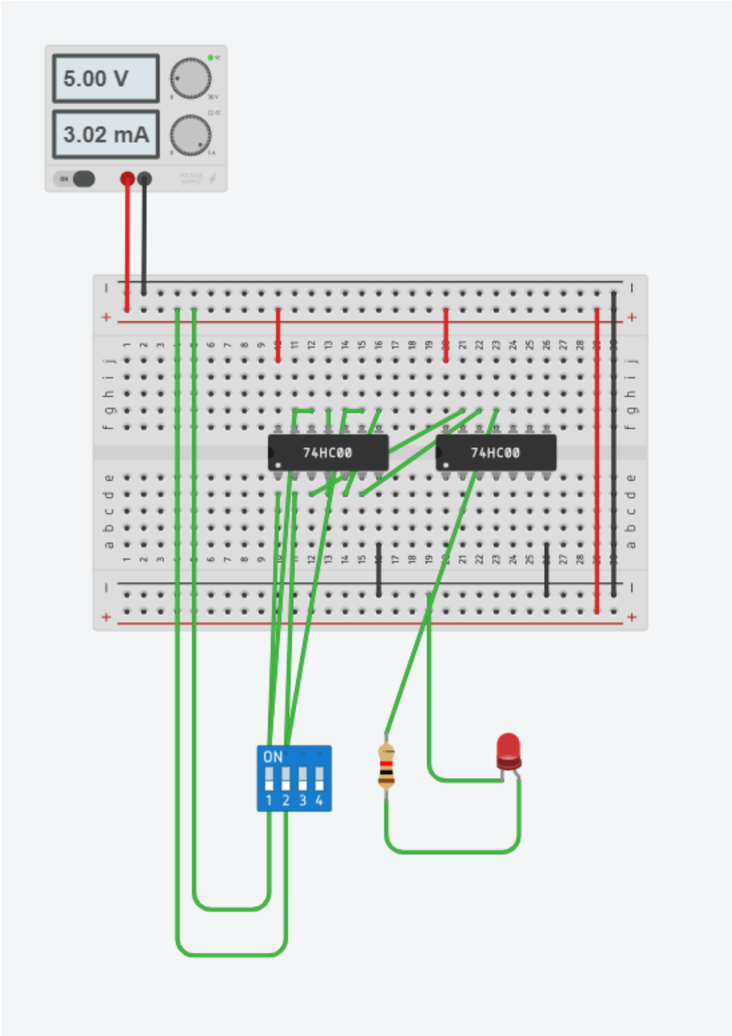

5.00 V
8.12 mA
OR USING NAND
74HC00
ON
1 2 3 4


5.00 V
8.12 mA
OR using NOR
74HC02
ON
1 2 3 4

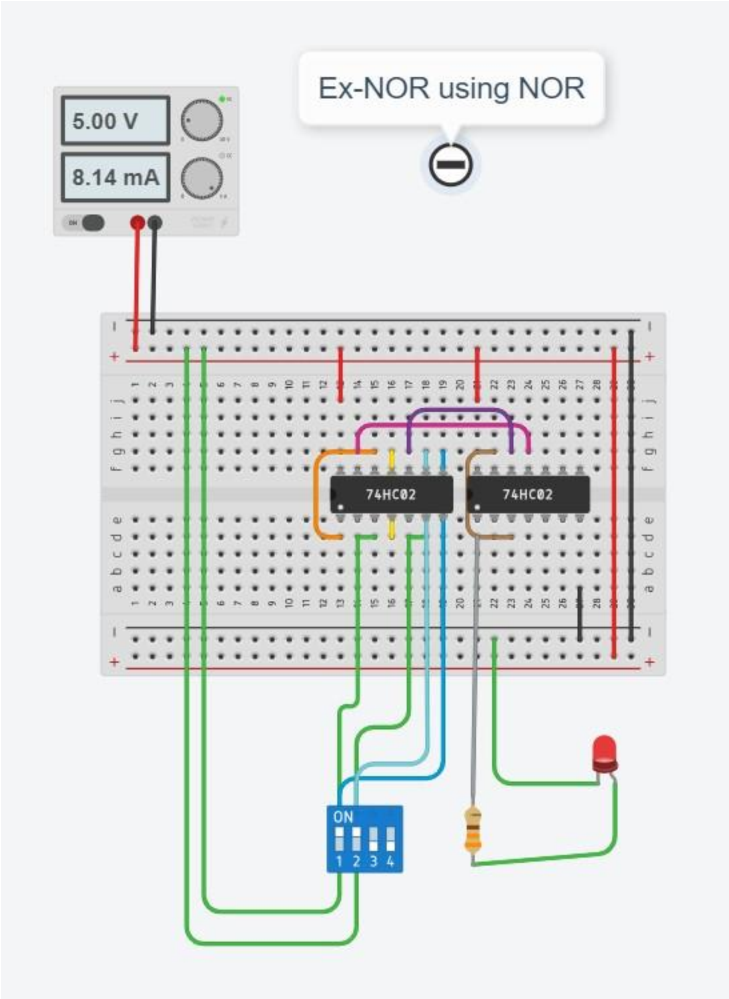

5.00 V
8.12 mA
NOR USING NAND
74HC00
ON
1 2 3 4

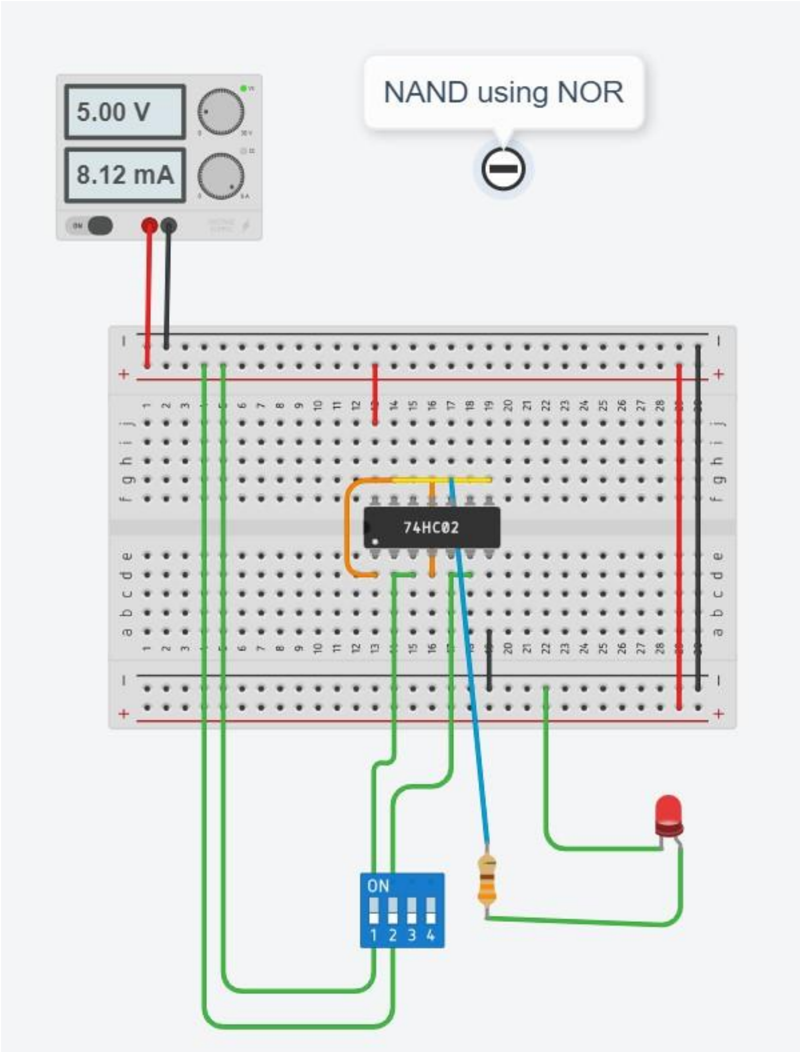

5.00 V
3.02 mA
74HC00
74HC00
ON
1 2 3 4
EX-OR USING NAND


EX-OR using NOR
5.00 V
8.14 mA
74HC02
74HC02
ON
1 2 3 4



EX-NOR USING NAND


Ex-NOR using NOR
5.00 V
8.14 mA
74HC02
74HC02
ON
1 2 3 4



5.00 V
8.12 mA
NAND using NOR
74HC02
ON
1 2 3 4