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I011

Exp:6 LDCA

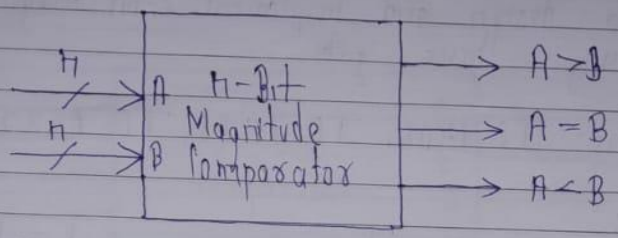
Aim: To design and implement 2-bit magnitude comparator using basic gates.

Apparatus: IC 7408, IC 7486, IC 7432, IC 7404

Theory:
Magnitude comparator is a combinational circuit that compare two number A and B. It determines the relative magnitude according to the comparison. Digital or binary comparators are made up from standard AND, NOR, NOT gates that compare the digital signals present at their input terminals and produce an output depending upon the condition of those inputs.

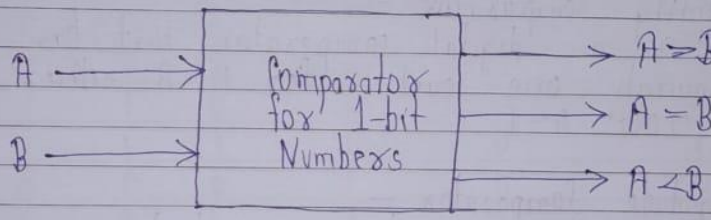
Identity Comparator –
It is a digital comparator that has three output terminals, one each for A=B either 'HIGH' A=B or 'LOW" A=1

Magnitude Comparator –
A magnitude comparator is a digital comparator that has three output terminals, one each for equality. A=B, A>B, A<B.



* 1-Bit magnitude comparator

A comparator used to compare two bits is called a single bit comparator. It consists of two input each for two single bit numbers and three outputs to generate less than, equal to and greater between two binary numbers

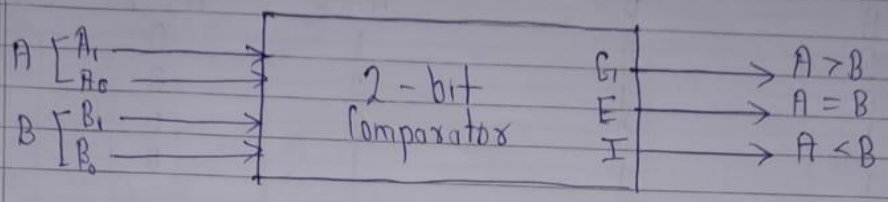


$\overline{A\bar{B} + \bar{A}B} = AB + \bar{A}\bar{B}$

$(A+\bar{B}).(\bar{A}+B) = A\bar{A} + AB + \bar{A}\bar{B} + B\bar{B}$

$= AB + \bar{A}\bar{B}$

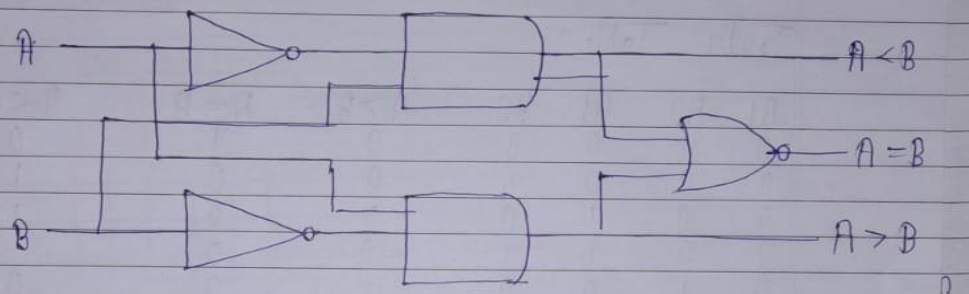
* 2 Bit Magnitude Comparator



Truth Table :-

A1	A0	B1	B0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Input		Output		
A	B	A = B	A > B	A < B
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0



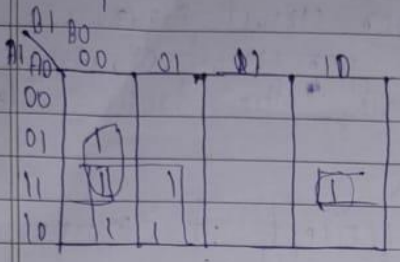
B

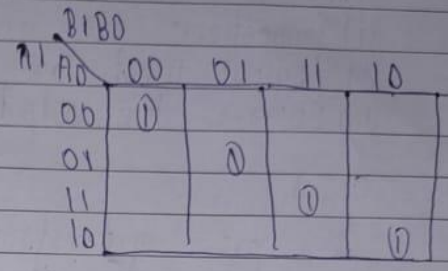
$\therefore (A < B) = A'B$

$(A = B) = A'B' + AB = (A \oplus B)'$

$(A > B) = AB'$

Kmap

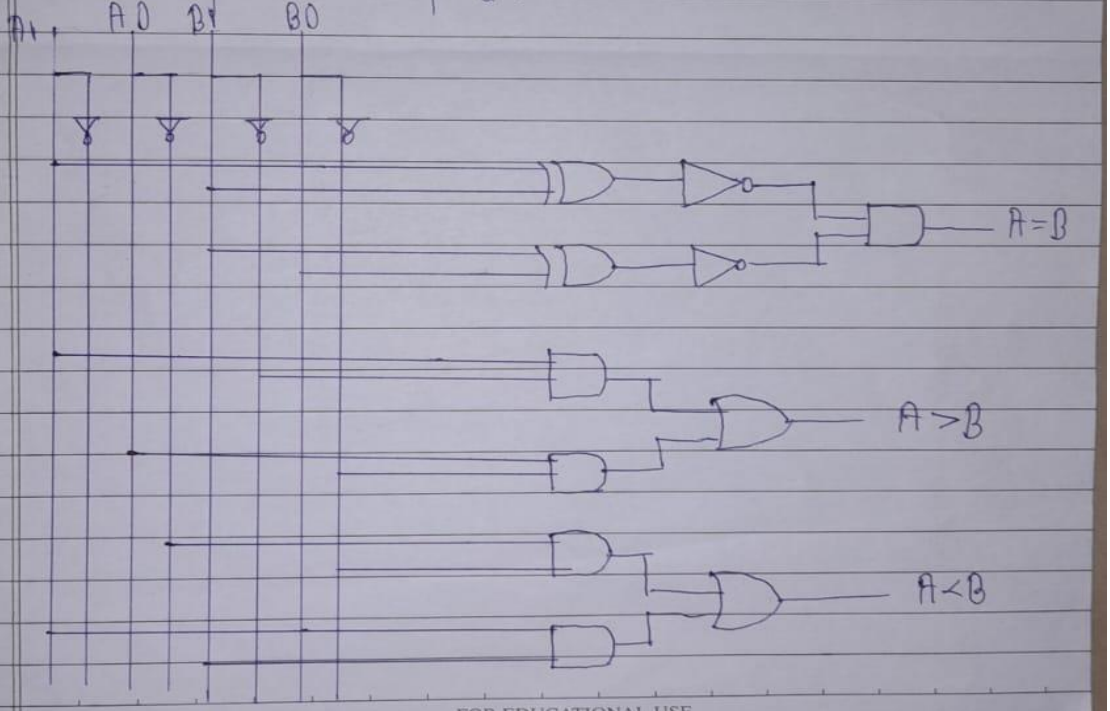




$A>B = A_0\overline{B_0}\,\overline{B_1} + A_1\overline{B_1} + A_1A_0\overline{B_0}$ $A=B = (A_0 \oplus B_0)(A_1 \oplus B_1)$

Logic Diagram:-

2 Bit Magnitude Comparator

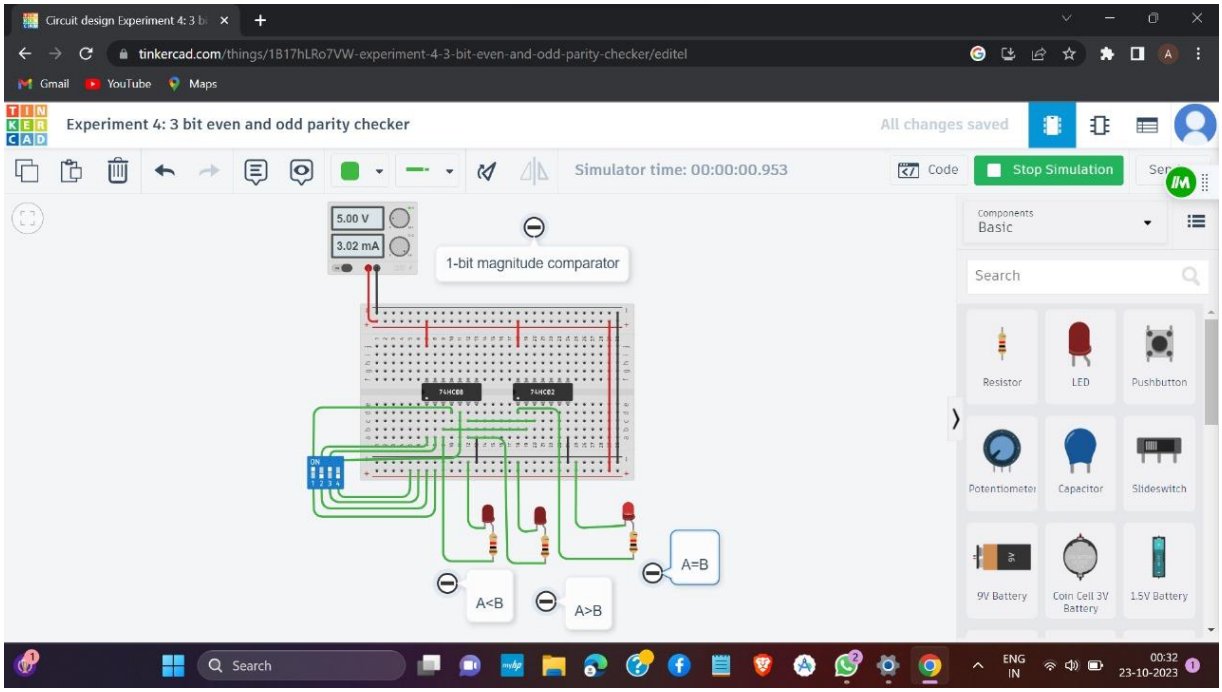


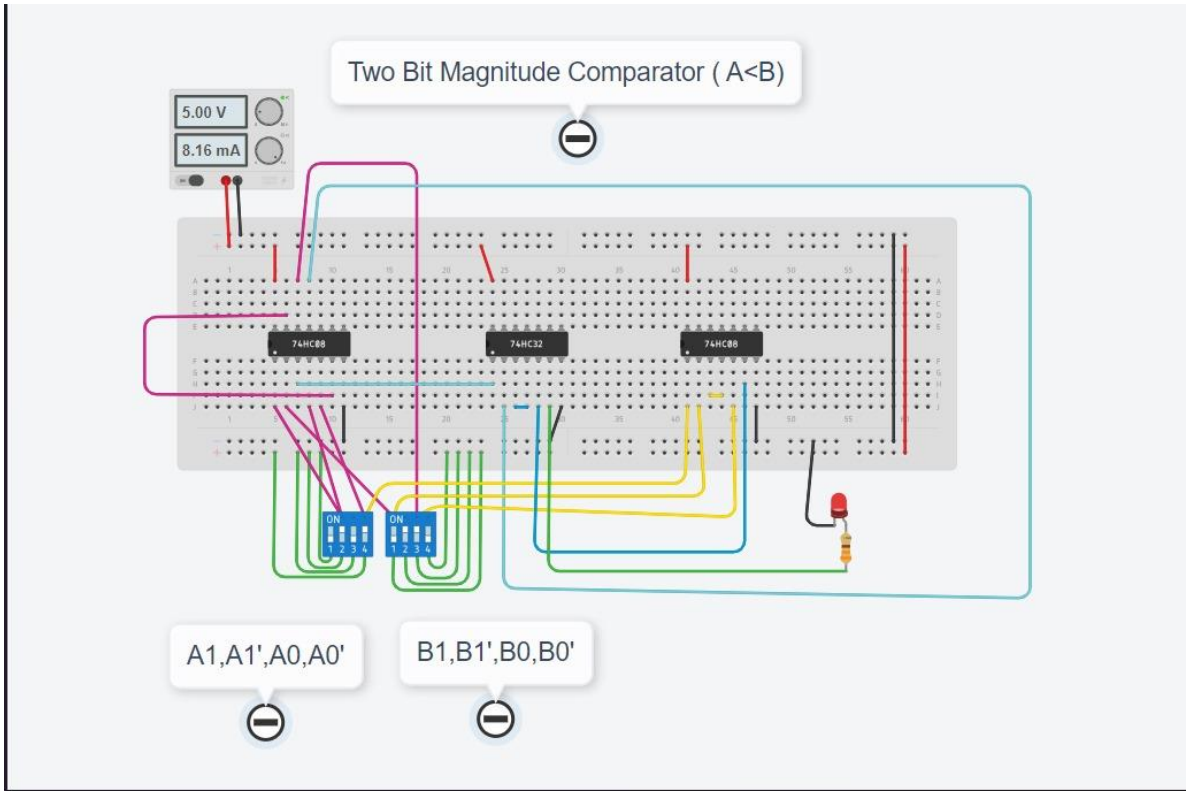
Procedure :-

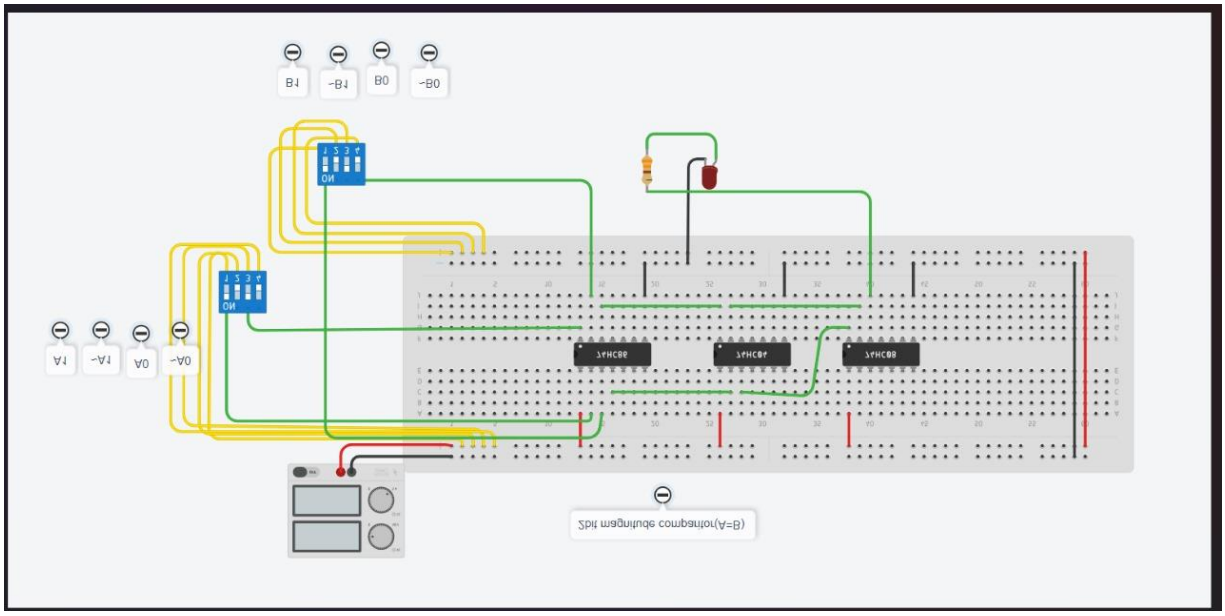
(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the outputs and verify the truth table.

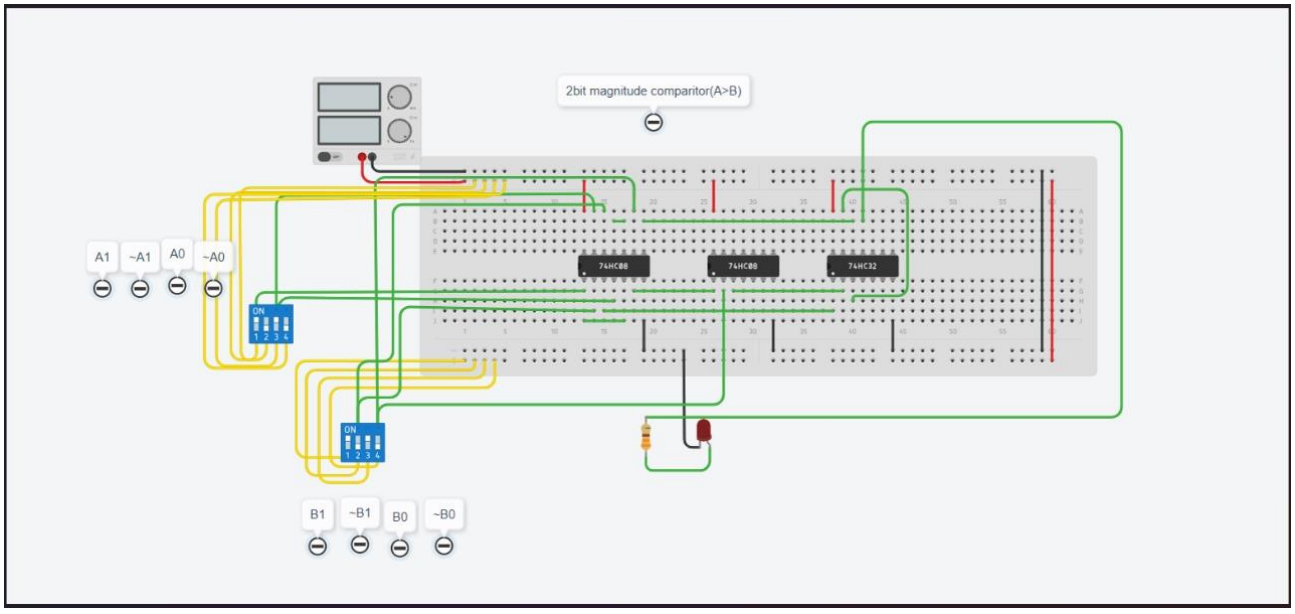
Conclusion :

I have understood the concept of comparator magnitude with its logical circuit.


Circuit design Experiment 4: 3 bi
tinkercad.com/things/1B17hLRo7VW-experiment-4-3-bit-even-and-odd-parity-checker/editel
Gmail
YouTube
Maps
Experiment 4: 3 bit even and odd parity checker
All changes saved
Simulator time: 00:00:00.953
Code
Stop Simulation
5.00 V
3.02 mA
1-bit magnitude comparator
A=B
A<B
A>B
Components
Basic
Search
Resistor
LED
Pushbutton
Potentiometer
Capacitor
Slideswitch
9V Battery
Coin Cell 3V Battery
1.5V Battery
Search
ENG
IN
00:32
23-10-2023


Two Bit Magnitude Comparator (A<B)
5.00 V
8.16 mA
74HC08
74HC32
74HC08
A1,A1',A0,A0'
B1,B1',B0,B0'


B1
~B1
B0
~B0
A1
~A1
A0
~A0
74HC08
74HC08
74HC32
2bit magnitude comparitor(A>B)


2bit magnitude comparitor(A>B)
A1
~A1
A0
~A0
B1
~B1
B0
~B0
74HC08
74HC08
74HC32