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I011

Exp - 4 (LO(A)

Aim: To study even and odd parity generator and checker

Parity generator:
It is a combinational circuit that accepts n-1 bit data and generates the additional bit that is to be transmitted with the bit stream. This additional bit is called parity bit.

Even parity generator

A	B	C	P
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Odd parity generator

A	B	C	P
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

K-map for 3 bits

A \ BC	00	01	11	10
0	0	1	0	1
1	1	0	1	0

K-map for 3 bits

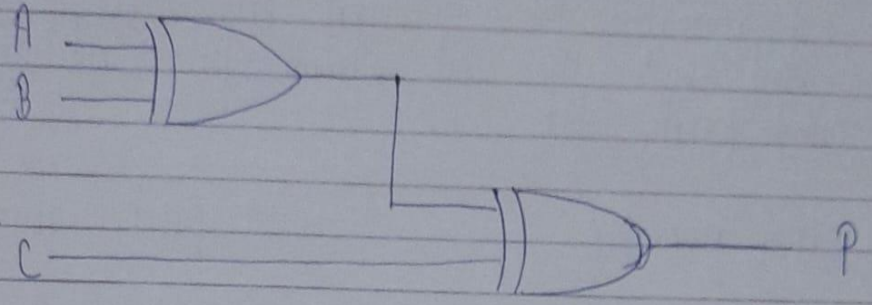
A \ BC	00	01	11	10
0	1	0	1	0
1	0	1	0	1

$P = \bar{A}BC + A\bar{B}\bar{C} + AB\bar{C} + ABC$

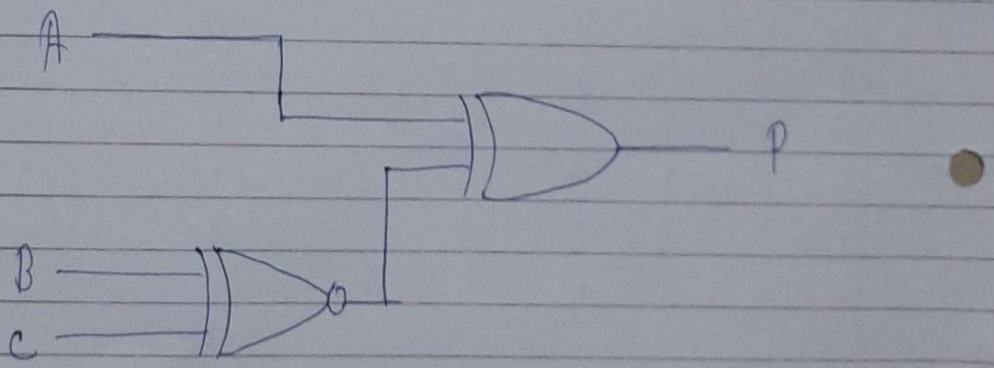
$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$

$= A(\bar{B} + C) + A(B \oplus \bar{C})$

$P = A \oplus B \oplus C$



Even-parity generator



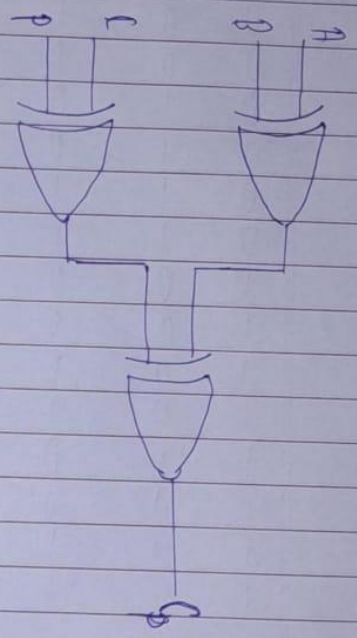
Odd-parity generator

Parity Checker :-

It is a logic circuit that checks for possible errors in transmission. When it is used as an even parity checker, the number of input bits must always be even.

Even-parity checker -

A	B	C	P	Cp
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0



AB \ CP

AB \ CP	00	01	11	10
00	0	1	0	1
01	1	0	1	0
11	0	1	0	1
10	1	0	1	0

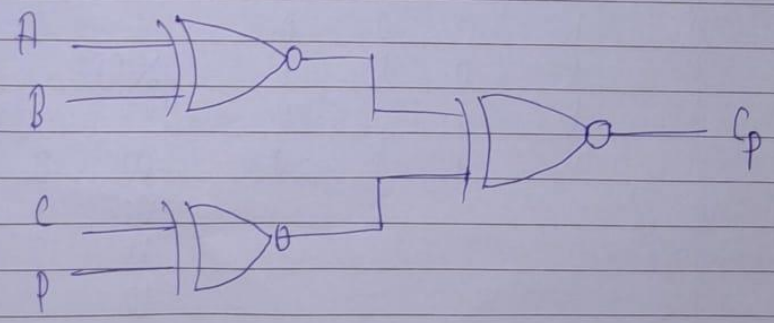
$= (A \oplus B) \oplus (C \oplus P)$

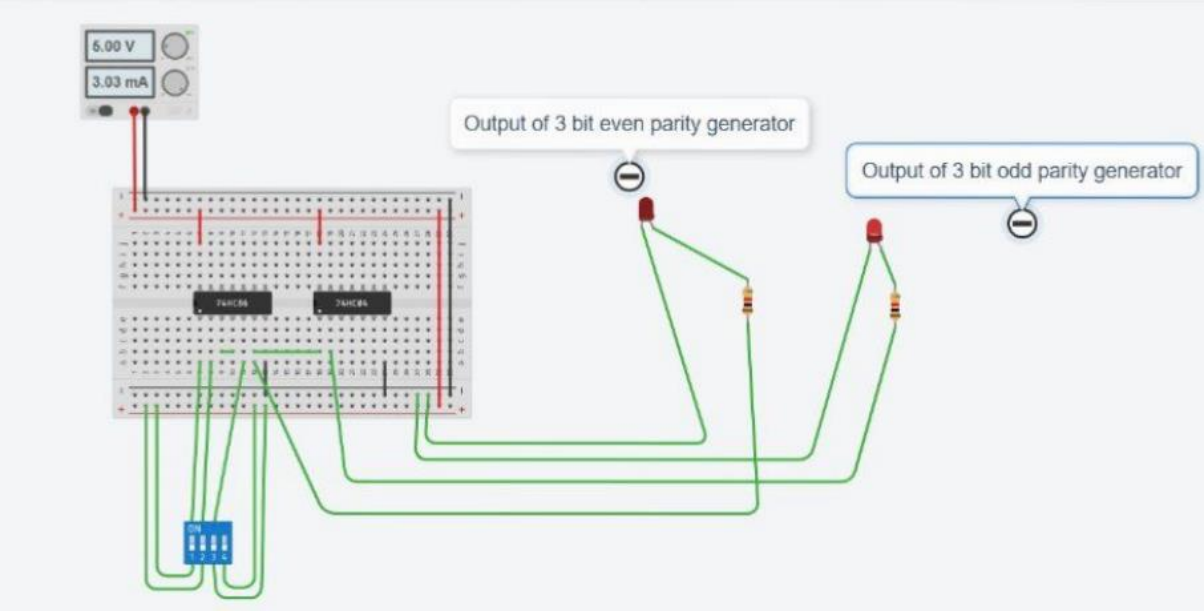
Odd-Parity Checker -

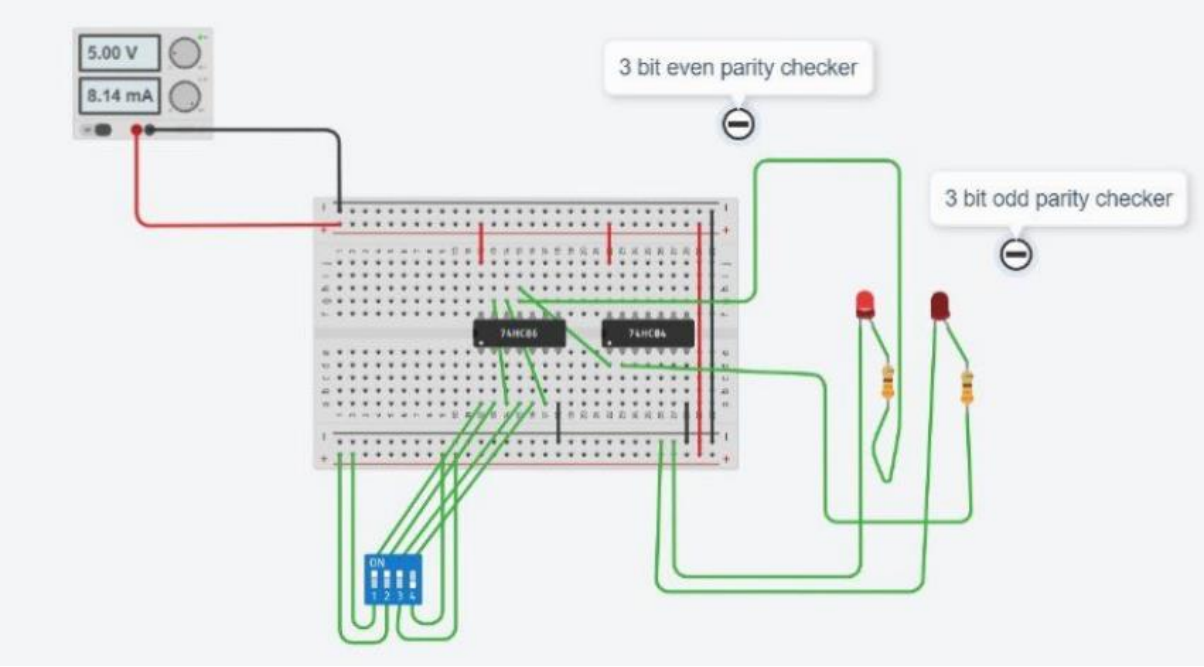
A	B	C	P	C_p
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

AB \ CP	00	01	11	10
00	1	0	1	0
01	0	1	0	1
11	1	0	1	0
10	0	1	0	1

$= (A \text{ Ex-NOR } B) \text{ Ex-NOR } (C \text{ Ex-NOR } P)$




5.00 V
3.03 mA
Output of 3 bit even parity generator
Output of 3 bit odd parity generator


5.00 V
8.14 mA
3 bit even parity checker
3 bit odd parity checker