

Your name and ID please:

We have completed our study of the CPU, and looked at 3 different sample architectures. *To show that you understand what each part does, please answer question 1 with numbered steps each containing bulleted sub-steps, just as we did in class many, many times.* I have left areas for your answers, and a diagram of the 3-bus architecture is attached for your convenience.

Question 1(a): You can assume that the ALU is sophisticated and has the ability simply to increment or decrement “A” (or “B” if you wish). Write “set ALU to increment ‘A’”, etc.

Write out the steps necessary to fetch an instruction using the three bus architecture. Use column 1 first, continue in column 2.

1. •	
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Question 1(b) Assume that the instruction you have just “fetched” is:

“ADD -(R1), (R2)+”

for your execution process. **Important:** Again, it would be crazy to include the auto-increment direct and auto-decrement direct addressing modes *and not provide increment and decrement ALU functions so although this cannot be indicated on the 3-bus diagram, assume that these ALU functions exist and are invoked using the function select lines.* What is a suitable execution sequence? Start in column 1, continue as necessary in column 2

[illegible]

Question 2: Importance – all modern computers employ microcoding.

Explain the essential difference between *horizontal micro-code* and *vertical micro-code*.

Question 3: Importance – all modern computers use 2's complement arithmetic *and* at the hardware level, if statements use the flags.

Using a 5-bit two's complement system, set up below the sum $+15 + (-16)$. Do the addition.

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Interpret the answer in decimal: _____

Which of the following ALU flags would be set to a "1" by this addition?

V **Yes** ☐ **No** ☐
C **Yes** ☐ **No** ☐
N **Yes** ☐ **No** ☐
Z **Yes** ☐ **No** ☐

Question 4(a). Importance – without these mechanisms and phenomena, we wouldn't be able to use the architecture of current main memory sub-system hierarchy.

Briefly explain the process of “paging”. And why do we do it? What is a “page fault”?

(b) What two phenomena make this system workable? Use a sentence or two to explain them.

Question 5(a). Importance – without certain fields in the page table, memory management would be impossible.

In the left column, name as many fields which exist in each line of a page table, and in the right column explain what the field is for. What's its purpose, briefly?

(b) What is cache? What type of memory hardware is it? What is its function and why does each block need a tag?

Question 7. Importance: the use of pipelining techniques improves the performance of a system by using parallelism. CPU control units generally are pipelined.

A 5 stage pipeline implements a task T which would normally take “n” seconds. Each of the stages of the pipeline are constructed to execute in “n/5” seconds. 21 tasks are waiting at the input to this pipeline. How many seconds will be required to finish all of these 21 tasks?

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Question 8. Importance: DMA is a general technique for improving computer system performance.

A dedicated DMA unit is connected to a hard drive. Describe the steps taken in copying pages into memory, and particularly identify what problematic issues are solved by the use of DMA.

Generic three-bus C.P.U. architecture

