

Name: Dominic Geneau ID number: 3675144 Date: Dec 6th 2019

EE2701 Experiment 5

Summary of Results

Op Amp:

1. Record the values of the resistors provided for this experiment in Table 5-1.

Table 5-1. Resistor Values.

Nominal	Measured (kΩ)
10 kΩ	9.73
200 kΩ	200.8

2. Record the range of offset voltages observed in step 2 of the procedure in Table 5-2.

Table 5-2. Offset Voltages

	Offset Voltage (mV)
Minimum	-3818 V
Maximum	3788 V

3. Record the measured amplitudes of v_{in} and v_{out} obtained in step 4 of the procedure in Table 5-3.

Table 5-3. Gain Data and Calculations

Circuit of	Amplitudes (V _{pp})		Voltage Gain A _v (V/V)		
	v_{in}	v_{out}	Nominal	Measured	% Difference
Step 2	500 mV	10.3 V	20.64	20.60	0.19%

$$\begin{aligned} \% \text{ Diff} &= \left| \frac{\text{measured} - \text{calculated}}{\text{calculated}} \right| \times 100 \\ &= \left| \frac{20.6 - 20.64}{20.64} \right| \times 100 \\ &= 0.19\% \end{aligned}$$

Calculate the nominal gains of the amplifiers of step 2 of the procedure from the measured values of R_1 and R_2 recorded in Table 5-1 and record the results in Table 5-3.

Calculate the measured gains of the amplifiers of step 2 of the procedure from the values of v_{in} and v_{out} recorded in Table 5-3 and record the results in Table 5-3 and Table 5-5.

Compare the nominal and measured gains of the amplifiers of step 2 of the procedure and record the results in Table 5-3.

Comment on the results of the gain comparisons.

The gains are extremely close ($> 1\%$ difference). This makes sense, because the approximation of $v_{in} \approx 0$ but not exactly 0 ($V_{in} \approx 0 \ll V_{out}$). So, the theoretical gain is naturally a bit higher than the measured (nominal) voltage gain.

4. Record the maximum positive and negative output voltages observed in step 6 of the procedure in Table 5-4.

Table 5-4. Output Voltage Limits

Clipping Voltage (V)	
Positive	+12.0 V
Negative	-10.4 V

12.0 V
-10.4 V

Does the op amp meet the specification for a ± 10 V output voltage range?

Yes, clipping occurs when peaks reach a max amplitude of 10 V (clipping started on positive amplitude around +10V)

5. Record the measured voltage gains from step 4 of the procedure in Table 5-5.

Record the measured values of f_{3dB} from step 7 of the procedure in Table 5-5.

Table 5-5. Gain Bandwidth.

Measured Values		
	A_v (V/V)	f_{3dB} (Hz)
Step 2	20.6	121.2×10^3 Hz

Bipolar Junction Transistors:

1. Record values you obtained for Task A) of the pre-lab and attach the worksheets showing the work you did to obtain the values.

Table 5-6. Biasing of common emitter circuit without R_E .

	V_{CC}	V_{th}	V_B	V_C	V_E	V_{CE}	V_{BE}	I_B	I_E	I_C	β
Calculated	12V	0.706V	0.65V	8.4V	0V	8.4V	0.65V	10 μ A	201 μ A	2mA	200

Is the transistor operating in the active mode? Why?

Yes, because the load line (Output) intersects the active region of the I_E - V_{CE} characteristics curve.

2. Record values you obtained for Task B) of the pre-lab and attach the worksheets showing the work you did to obtain the values.

Table 5-7. Biasing of common emitter circuit with $R_E = R_C = 1.8 \text{ k}\Omega$.

	V_{CC}	V_{th}	V_B	V_C	V_E	V_{CE}	V_{BE}	I_B	I_E	I_C	β
Calculated	12V	4.306V	4.25V	8.4V	3.6V	4.8V	0.65V	10 μ A	2.01 μ A	2mA	200

Is the transistor operating in the active mode? Why?

Yes, because the load line, albeit less steep than the previous one, still intersects the active region of the I_E - V_{CE} characteristics curve.

3. Record values you obtained for Task C) of the pre-lab and attach the worksheets showing the work you did to obtain the values. Then record values you obtained for Step 1 of Task B) of the BJT procedure.

Table 5-8. Biasing of common emitter circuit with $R_E = R_C = 1.8 \text{ k}\Omega$.

	V_{CC}	V_{RB2}	V_B	V_C	V_E	V_{CE}	V_{BE}	I_B	I_E	I_C	β
Calculated	12V	4.53V	4.47V	8.18V	3.82V	4.36V	0.65V	10.61 μ A	2.13mA	2.12mA	200
Measured	11.9V	4.45V	4.45V	8.16V	3.82V	4.34V	0.63V	12.7 μ A	2.15mA	2.14mA	167
% Difference	0.17%	1.80%	0.45%	0.24%	0.00%	0.46%	3.08%	2.00%	0.93%	0.94%	16.5%
Calculated	$R_{B1} = 15\text{k}\Omega$		$R_{B2} = 9.1\text{k}\Omega$		21.68V	$R_{th} = 5.66 \text{ k}\Omega$					
Measured	Measured $R_{B1} = 14.96 \text{ k}\Omega$		Measured $R_{B2} = 9.07 \text{ k}\Omega$		Actual $R_{th} = 5.647 \text{ k}\Omega$						
% Difference	0.27%		0.33%		0.23%						

Note: Use a multimeter to measure the resistance and record actual values. Recall currents can be obtained from voltages using Ohm's Law.

Is this circuit equivalent to the circuit described in Task B) above? Yes (although with slight deviations $\approx 5\%$, which is considered).

Is the transistor operating in the active mode? Why? Yes, the output voltage waveform is not distorted, indicating uninterrupted current flow from the Q-point and its max/min voltage from all values are extremely close. Save for β & I_E . The power source and resistors are reliable, but the transistor can vary in value, causing β and I_E to vary as well.

Compare the measured values with the calculated ones. Discuss the differences. V_B .

Identify the sources causing the differences. Calculate the relative differences with respect to the calculated ones. If the difference is significant, what is the reason and how to avoid it? The only considerably large difference is β & I_E (16.5% and 21.58%, respectively). BJT transistors vary sometimes from the factory value which could also change the requested β constant and base current.

4. Record values you obtained for Step 1 of Task A) of the BJT procedure.

Table 5-9. Base terminal of BJT.

Multimeter Leads connected to BJT		Diode Check value (reading or 0.L)
+ Terminal	Gnd Terminal	—
1	2	0.L
2	1	0.644V
1	3	0.L
3	1	0.L
2	3	0.626V
3	2	0.L

Explain why the remaining terminal is the base when the other two terminals give overload O.L with both polarities of the multimeter applied.

In the case of O.L., this means there is no current flowing through the diode (reversed biased). Thus, the two other terminals (diodes inverted to each other) should show O.L. since, as one of them is forward biased, the other inhibits current flow and is reversed biased (i.e. O.L.).

5. Record values you obtained for Step 2 and Step 3 of Task A) of the BJT procedure.

Table 5-10. Base terminal of BJT.

Transistor Type	NPN
Base Terminal	2
Emitter Terminal	1
Collector Terminal	3

Explain why Step 2 can be used to determine whether the transistor is 'NPN' or 'PNP'.
Since the base terminal defines forward or reversed biased current flow, we can verify the polarity of the base in reference to the other terminals. If the base has positive polarity and the DMM displays voltage across both terminals, then the transistor is NPN (negative-positive-negative).

When forward biased, the base-emitter voltage drop should represent an approximate $\sim 0.65V$ drop and should be higher than the base collector voltage drop.

6. Record values you obtained for Step 2 of Task B) of the BJT procedure.

Table 5-11. Base terminal of BJT.

	Peak-to peak voltages	
	v_B	v_C
Distorted	7.76 V	6.00 V
Non-distorted	4.16 V	4.08 V

Include in your lab report plots showing the distorted v_C along with v_B .

The BJT is operating in which mode if a distorted positive or negative output is observed?

Explain why. In the cutoff mode, this means the sinusoidal voltage source is high enough that it causes I_B to reduce to zero.

Clips at negative amplitude.
For the maximum undistorted output signal, include in the lab report the following waveforms obtained using the oscilloscope display printout: base voltage v_B , collector voltage v_C . Plot all waveforms on a common time scale using 2 to 3 sinusoidal cycles. For a negative output, I_B is high enough to cause v_C to approach an approximate voltage drop of $\approx 0.2V$. This means the transistor is in saturation mode.

Determine from the waveforms, what is the phase relation (phase angle) between the input and the output signals? Explain why. The phase angle is zero, since the input voltage directly correlates to the output current (I_C). Thus,

current (I_B) voltage directly correlates to the output current (I_C). Thus, no delay should occur between waveforms.

The capacitor acts as a half-wave rectifier circuit with smoothing similar to capacitor. It discharges a voltage as the sinusoidal input decreases its voltage. In doing so, it supplies a constant DC Voltage to the base current, I_B . This, in turn

makes a reliable current flow in I_C and a good amplification.

Name: Abdul Wasey ID number: 3609233 Date: Dec. 6. 2019

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Step 2	500 mV	10.3 V	20.64	20.60	0.19%

$$\begin{aligned} \% \text{ Difference} = & \\ & \frac{| \text{measured} - \text{calculated} |}{\text{calculated}} \\ & \times 100\% \end{aligned}$$

Calculate the nominal gains of the amplifiers of step 2 of the procedure from the measured values of R_1 and R_2 recorded in Table 5-1 and record the results in Table 5-3.

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The gains are extremely close ($> 1\%$ difference). This makes sense because the approximation of $V \approx 0$ but not exactly 0 ($v_{in} \approx 0 \ll v_{out}$). So, the theoretical gain is naturally about higher than the measured ~~gains~~ voltage gain.

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Record the measured values of f_{3dB} from step 7 of the procedure in Table 5-5.

Table 5-5. Gain Bandwidth.

	Measured Values	
	A_v (V/V)	f_{3dB} (Hz)
Step 2	20.6	121.2×10^3 Hz

* Please see the other Sheet *

Explain why the remaining terminal is the base when the other two terminals give overload 0.L with both polarities of the multimeter applied.

5. Record values you obtained for Step 2 and Step 3 of Task A) of the BJT procedure.

Table 5-10. Base terminal of BJT.

Transistor Type	NPN
Base Terminal	2
Emitter Terminal	1
Collector Terminal	3

Explain why Step 2 can be used to determine whether the transistor is 'NPN' or 'PNP'.

NPN because when transistor is reverse bias, the DMM reads 0.L.

Explain why Step 3 can be used to determine the collector and the emitter terminals.

The lower of the 2 readings indicates the base as a collector and so meaning b the other is emitter.

6. Record values you obtained for Step 2 of Task B) of the BJT procedure.

Table 5-11. Base terminal of BJT.

	Peak-to peak voltages	
	v_B	v_C
Distorted	7.60	6.80
Non-distorted	4.60	5.20

Include in your lab report plots showing the distorted v_C along with v_B .

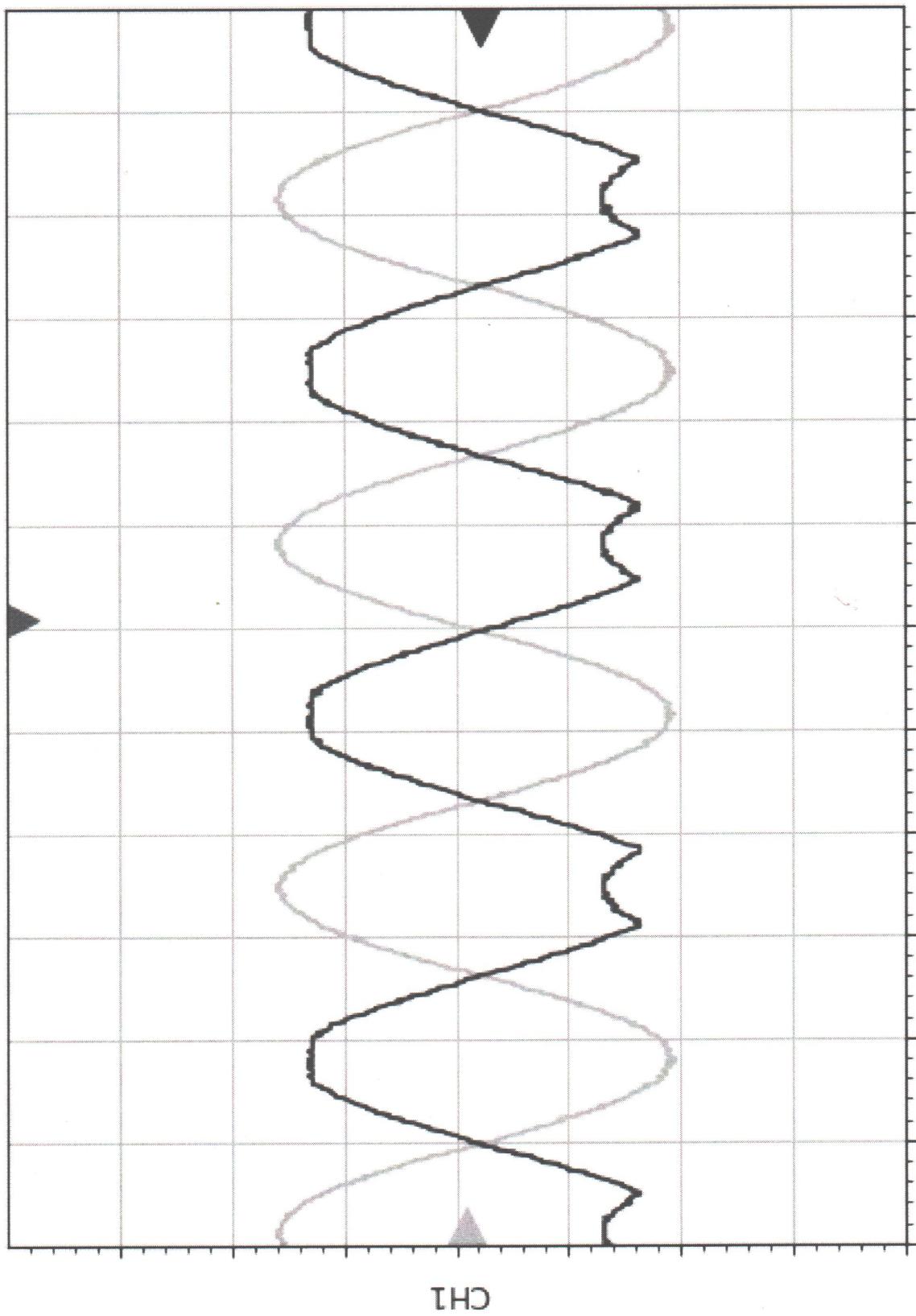
The BJT is operating in which mode if a distorted positive or negative output is observed?
Explain why.

For the maximum undistorted output signal, include in the lab report the following waveforms obtained using the oscilloscope display printout: base voltage v_B , collector voltage v_C . Plot all waveforms on a common time scale using 2 to 3 sinusoidal cycles.

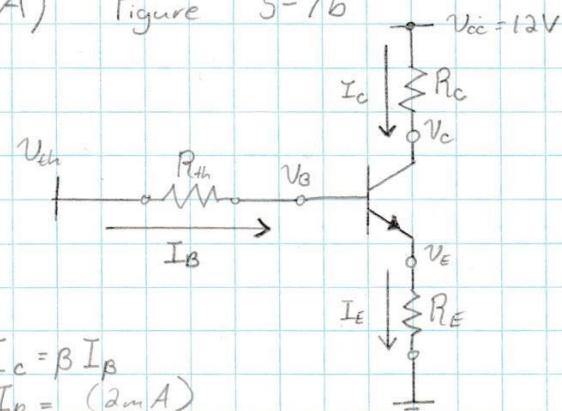
Determine from the waveforms, what is the phase relation (phase angle) between the input and the output signals? Explain why.

Explain why the $10\mu F$ capacitor in the circuit is necessary.

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A) Figure 5-7b

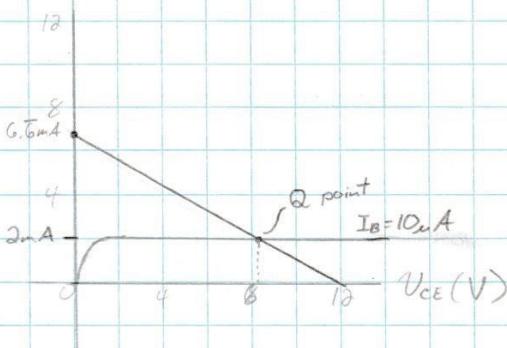


$$I_c = \beta I_B$$

$$I_B = \frac{(2\text{mA})}{200}$$

= $10\mu\text{A}$ (in active mode)

$I_c(\text{mA})$ for $I_c = 2\text{mA}$



$$Q = (8\text{V}, 2\text{mA})$$

$$V_{CE} = V_C - V_E$$

$$V_E = 0\text{V}$$

$$V_{th} = I_B R_{th} + (V_B - V_E)$$

$$V_C = (8.4\text{V}) + (0\text{V}) \Rightarrow V_C = 8.4\text{V}$$

$$V_{th} = I_B R_{th} + (V_B - V_E)$$

$$V_B = 0.706\text{V} - (10\mu\text{A})(5.6\text{k}\Omega)$$

$$V_B = 0.65\text{V}$$

→ Transistor operates in active mode, since load line intersects with active region ($I_c = 2\text{mA}$, $I_B = 10\mu\text{A}$)

$$V_{CC} = 12\text{V} \quad i_c = 2\text{mA}$$

$$R_C = 1.8\text{k}\Omega \quad \beta = 200$$

$$R_{th} = 5.6\text{k}\Omega$$

$$R_E = 0\text{k}\Omega \quad V_{BE} \approx 0.65\text{V}$$

KVL Input

$$V_{th} = I_B R_{th} + V_{BE} + I_E R_E$$

$$V_{th} = (10\mu\text{A})(5.6\text{k}\Omega) + (0.65\text{V})$$

$$V_{th} = 0.706\text{V}$$

KVL Output

$$\approx I_c$$

$$12\text{V} = I_c R_C + V_{CE} + I_E R_E$$

$$12\text{V} = I_c (R_C + R_E) + V_{CE}$$

$$I_c = \frac{12\text{V}}{(1.8\text{k}\Omega)} = 6.6\text{mA} @ V_{CE} = 0\text{V}$$

$$V_{CG} = 12\text{V} @ I_c = 0\text{mA}$$

@ $I_c = 2\text{mA}$:

$$12\text{V} = I_c (1.8\text{k}\Omega) + V_{CE}$$

$$V_{CE} = 12 - (2\text{mA})(1.8\text{k}\Omega)$$

$$V_{CE} = 8.4\text{V}$$

$$I_B = 10\mu\text{A}$$

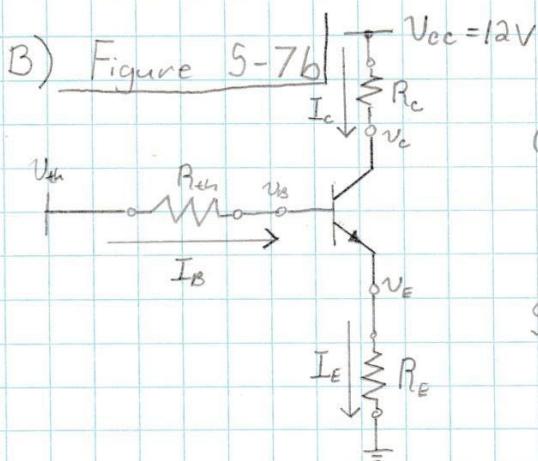
$$I_E = I_B + I_c \approx I_c$$

$$= (10\mu\text{A}) + (2\text{mA})$$

$$I_E = 2.01\text{mA} \approx 2\text{mA}$$

Pre-Lab

By: Dominic Geneau (3675144)



Given

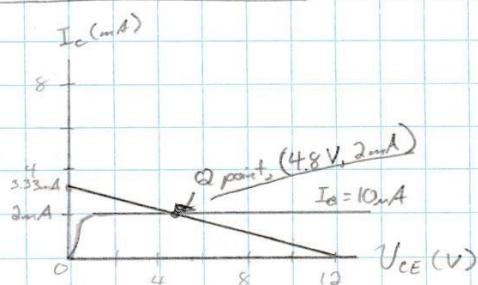
$$\begin{aligned} V_{cc} &= 12V \\ R_c &= 1.8 \text{ k}\Omega \\ R_E &= 1.8 \text{ k}\Omega \\ R_{th} &= 5.6 \text{ k}\Omega \end{aligned}$$

$$\begin{aligned} I_c &= 2 \text{ mA} \\ \beta &= 200 \\ V_{BE} &\approx 0.65V \end{aligned}$$

Solve for

$$\begin{cases} V_B = 4.25V \\ V_C = 8.4V \\ V_E = 3.6V \\ V_{CE} = 4.8V \end{cases}$$

$$\begin{cases} I_B = 10 \mu\text{A} \\ I_E \approx 2 \text{ mA} \\ V_{th} = 4.306V \\ Q\text{-point: } (4.8V, 2 \text{ mA}) \end{cases}$$

SolutionLoad line Analysis

$$12V = (2 \text{ mA})(3.6 \text{ k}\Omega) + V_{CE}$$

$$V_{CE} = 4.8V$$

$$\begin{aligned} V_B &= V_{th} - I_B R_{th} \\ &= 4.306 - (10 \mu\text{A})(5.6 \text{ k}\Omega) \end{aligned}$$

$$V_B = 4.25V$$

$$V_{BE} = 0.65 = V_B - V_E$$

$$\begin{aligned} V_E &= V_B - V_{BE} \\ &= (4.25V) - (0.65) \end{aligned}$$

$$V_E = 3.6V$$

$$V_{CE} = 4.8V = V_C - V_E$$

$$\begin{aligned} V_C &= V_{CE} + V_E \\ &= (4.8V) + (3.6V) \end{aligned}$$

$$V_C = 8.4V$$

KCL

$$I_E = \frac{I_B + I_C}{2.01 \text{ mA}} \approx I_C = 2.00 \text{ mA}$$

KVL - Input

$$= 2 \text{ mA} = I_C$$

$$V_{th} = I_B R_{th} + V_{BE} + I_E R_E$$

$$\begin{aligned} V_{th} &= (10 \mu\text{A})(5.6 \text{ k}\Omega) + (0.65V) + (2 \text{ mA})(1.8 \text{ k}\Omega) \\ V_{th} &= 4.306V \end{aligned}$$

KVL - Output

$$= 2 \text{ mA} = I_C$$

$$\begin{aligned} V_{cc} &= I_C R_C + V_{CE} + I_E R_E \\ 12V &= I_C (1.8 \text{ k}\Omega + 1.8 \text{ k}\Omega) + V_{CE} \end{aligned}$$

$$I_C = \frac{12V}{3.6 \text{ k}\Omega} = 3.33 \text{ mA} @ V_{CE} = 0$$

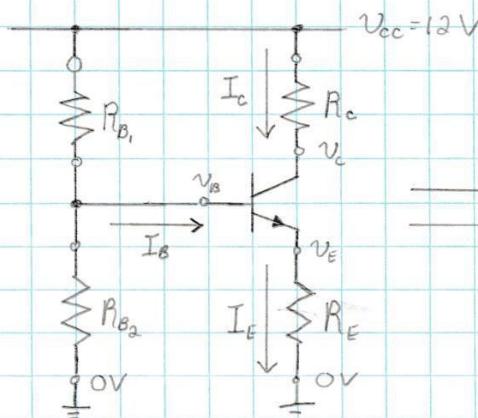
$$V_{CE} = 12V @ I_C = 0$$

\rightarrow Transistor operates in active mode
since load line crosses active
region at $I_C = 2 \text{ mA}$ and $I_B = 10 \mu\text{A}$
($V_{CE} = 4.8V$)

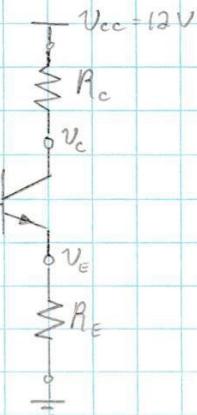
Pre-Lab

By: Dominic Geneau (3675144)

c) Figure 5.7a



$$\rightarrow V_{th} = 4.53 \text{ V}$$



$$\left. \begin{array}{l} V_{cc} = 12 \text{ V} \\ R_c = R_E = 1.8 \text{ k}\Omega \\ R_{B_1} = 15 \text{ k}\Omega \\ R_{B_2} = 9.1 \text{ k}\Omega \end{array} \right\} \text{ Given } \quad \left. \begin{array}{l} V_{BE} \approx 0.65 \text{ V} \\ \beta = 200 \end{array} \right\}$$

Parallel resistance

$$\frac{1}{R_{th}} = \frac{1}{R_{B_1}} + \frac{1}{R_{B_2}} \Rightarrow R_{th} = \frac{R_{B_1} R_{B_2}}{(R_{B_1} + R_{B_2})}$$

$$R_{th} = \frac{(15 \text{ k}\Omega)(9.1 \text{ k}\Omega)}{(15 \text{ k}\Omega) + (9.1 \text{ k}\Omega)} = 5.664 \text{ k}\Omega$$

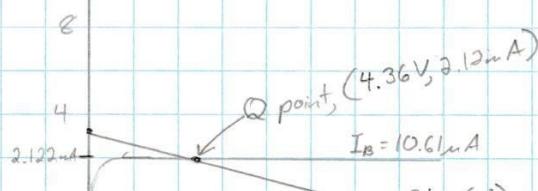
$$R_{th} = 5.7 \text{ k}\Omega \approx 5.6 \text{ k}\Omega$$

$$V_{AB_2} = V_{th} = V_{cc} - \frac{R_{B_2}}{R_{B_1} + R_{B_2}} = (12 \text{ V}) - \frac{(9.1 \text{ m}\Omega)}{(15 \text{ k}\Omega) + (9.1 \text{ k}\Omega)}$$

$$\boxed{V_{th} = 4.531 \text{ V}}$$

KVL Input ($V_{BE} \approx 0.65 \text{ V}$)

$$I_E \approx I_c = \beta I_B \text{ in active region}$$

 I_c (mA)

$$12 \text{ V} = (2.122 \text{ mA})(2.6 \text{ k}\Omega) + V_{ce}$$

$$\boxed{V_{ce} = 4.361 \text{ V}}$$

$$\boxed{I_c = 2.122 \text{ mA}}$$

$$I_E = I_B + I_c = (10.61 \mu\text{A}) + (2.122 \text{ mA})$$

$$\boxed{I_E = 2.133 \approx 2.122 \text{ mA} = I_c}$$

$$V_B = V_{th} - I_B R_{th} = (4.53) - (10.61 \mu\text{A})(5.664 \text{ k}\Omega)$$

$$\boxed{V_B = 4.471 \text{ V}}$$

$$V_E = V_B - V_{BE} = (4.471 - 0.65) \Rightarrow \boxed{V_E = 3.821 \text{ V}}$$

$$V_C = V_{ce} + V_E = (4.361 + 3.821)$$

$$\boxed{V_C = 8.182 \text{ V}}$$