

**MUHAMMAD SOHRAB**

PROFESSIONAL EMBEDDED DESIGN ENGINEER

Email/Skype: sohrabchhofficial@gmail.com

Phone/WhatsApp: +92-349-0359740

LinkedIn: [muhammad-sohrab-00a120282/](https://www.linkedin.com/in/muhammad-sohrab-00a120282/)

Address: Islamabad Pakistan.

SKILLS:

- HDLs (Hardware Description Languages): Verilog, VHDL (VHSIC Hardware Description Language), SystemVerilog(Basics).
- FPGA Synthesis Tools: Xilinx Vivado Altera Quartus
- Hardware Platforms: Xilinx Zynq and Ultrascale Intel (formerly Altera) Arria and Cyclone series.
- High-Level Synthesis (HLS) Tools: Vivado HLS (Xilinx).
- IP Cores: Xilinx IP Cores and Intel IP Cores.
- Documentation and Design Entry: Doxygen, Microsoft Word.
- Schematic Entry Tools: Xilinx Vivado and Altium Designer
- JTAG Debuggers: Xilinx Chipscope, Intel SignalTap
- Tools: Xilinx ISE, Xilinx Vivado, MATLAB/Simulink, LabVIEW, PSIM, Altium Designer, ModelSIM, Arduino IDE.
- Languages: English (C1), Urdu (Native), German (Basic)

EXPERIENCE:**FPGA/EMBEDDED SYSTEM DESIGN PROJECTS**

- DAC (Digital to Analog Converter) interfacing with FPGA using SPARTAN 3.
- ADC (Analog to Digital Converter) interfacing with FPGA using SPARTAN 3.
- Implementation of Digital Filter on FPGA using Verilog.
- 32-bit -5 stage Pipe-lined MIPS Processor in Verilog.
- UART-Based Temperature Monitor implementation on Artix-7 Board.
- SPI-Based Digital Dice implementation on Artix-7 Board.
- 32-bit RISC Processor in Verilog.
- Programmable Digital Delay Timer in Verilog HDL.
- Plate License Recognition in Verilog HDL.
- 7-Segment Display Controller on Basys 3 FPGA.

PROGRAMMING LANGUAGES:

- Verilog, VHDL, System Verilog, Embedded C, MATLAB, C/C++, ARDUINO, Python(Basic).

SEMESTER/RESEARCH PROJECTS

- Three level neutral point clamped inverter with MPPT & automatic cleaning of solar panels with MATLAB SIMULINK. (Published at PAS)
- FPGA based smart Home Automation System.
- Implementing Finite State Machine (FSM) on HDL.
- Schematic and PCB design of ESP32 using Altium Designer.
- Design of single stage DC/DC boost Converter. (MATLAB SIMULINK, Hardware).

RESEARCH PUBLICATIONS/REVIEWS**❖ Design of Three Level Neutral Point Clamped Inverter with Fuzzy Logic based MPPT for PV Applications**

(Proceedings of the Pakistan Academy of Sciences): A Physical and Computational Sciences 59(3): 69-80 (2022)

[https://doi.org/10.53560/PPASA\(59-3\)775](https://doi.org/10.53560/PPASA(59-3)775)**COURSES/CERTIFICATIONS:**

Introduction to FPGA Design for Embedded Systems.

HDL for FPGA Design.(Coursera-Enrolled)

Learning Verilog for FPGA development.

Building FPGA Projects.(Coursera)

FPGA Softcore Processors and IP Acquisition.(Coursera)

Intro to ESG: Environmental, Social & Governance.

Development of technical teams & execution of Project.

EDUCATION:

- **BE/BSC ELECTRONIC ENGINEERING [2016 – 2020]**

ELECTRONIC ENGINEERING DEPARTMENT, UNIVERSITY OF ENGINEERING & TECHNOLOGY (UET) PESHAWAR, PAKISTAN**Thesis:** Precise Control of Stepper and Servo Motor and their Comparative Analysis using FPGA (SPARTAN 3E).