数字电路实验报告

实验题目:	FPGA 实验平台及 IP 核使用
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1 实验题目

FPGA 实验平台及 IP 核使用

2 实验目的

1. 熟悉 FPGAOL 在线实验平台结构及使用
2. 掌握 FPGA 开发各关键环节
3. 学会使用 IP 核（知识产权核）

3 实验环境

(1) vlab.ustc.edu.cn

(2) fpagol.ustc.edu.cn

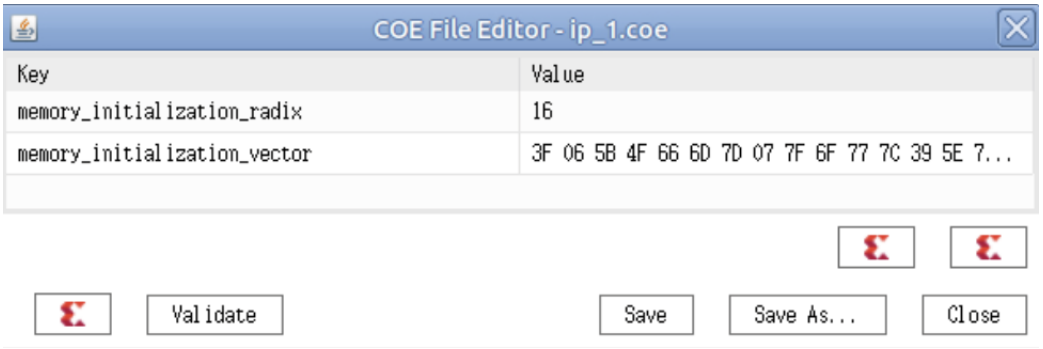
(3) Logisim

(4) Vivado

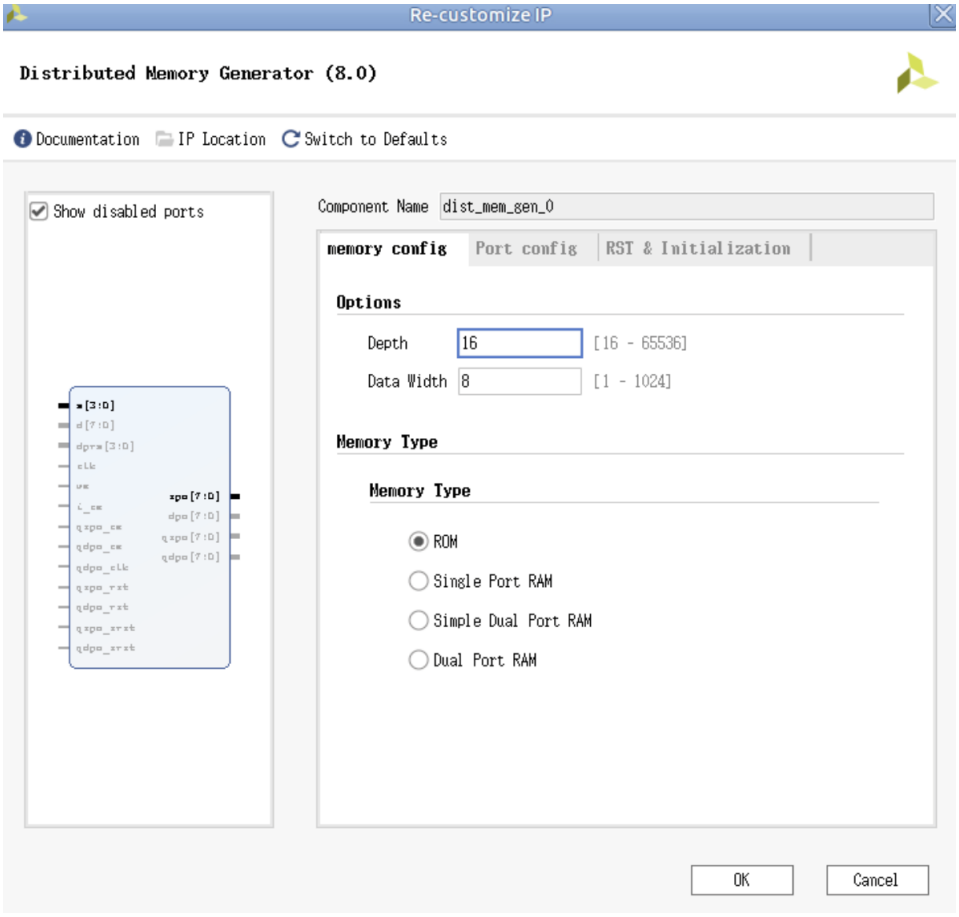
4 实验练习

题目 1

COE 文件如图



存储器设置如图



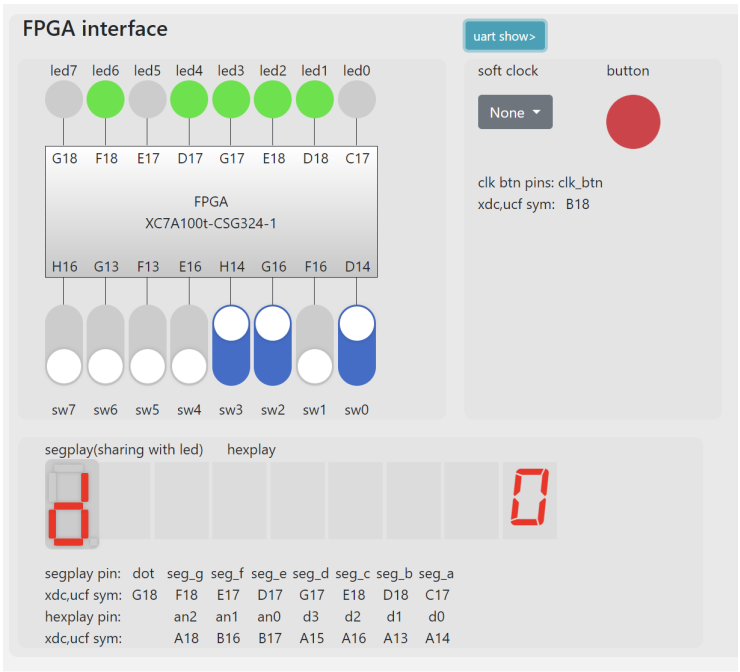
设计文件如图

```
module T1(
    input [3:0]sw,
    output [7:0]led
    );
    dist_mem_gen_0 dist_mem_gen_0(
    .a(sw),
    .spo(led)
    );
endmodule
```

约束文件如图

```
## FPGAOL LED (signle-digit-SEGPLAY)

set_property -dict { PACKAGE_PIN C17   IOSTANDARD LVCMOS33 } [get_ports { led[0] }];
set_property -dict { PACKAGE_PIN D18   IOSTANDARD LVCMOS33 } [get_ports { led[1] }];
set_property -dict { PACKAGE_PIN E18   IOSTANDARD LVCMOS33 } [get_ports { led[2] }];
set_property -dict { PACKAGE_PIN G17   IOSTANDARD LVCMOS33 } [get_ports { led[3] }];
set_property -dict { PACKAGE_PIN D17   IOSTANDARD LVCMOS33 } [get_ports { led[4] }];
set_property -dict { PACKAGE_PIN E17   IOSTANDARD LVCMOS33 } [get_ports { led[5] }];
set_property -dict { PACKAGE_PIN F18   IOSTANDARD LVCMOS33 } [get_ports { led[6] }];
set_property -dict { PACKAGE_PIN G18   IOSTANDARD LVCMOS33 } [get_ports { led[7] }];


## FPGAOL SWITCH

set_property -dict { PACKAGE_PIN D14   IOSTANDARD LVCMOS33 } [get_ports { sw[0] }];
set_property -dict { PACKAGE_PIN F16   IOSTANDARD LVCMOS33 } [get_ports { sw[1] }];
set_property -dict { PACKAGE_PIN G16   IOSTANDARD LVCMOS33 } [get_ports { sw[2] }];
set_property -dict { PACKAGE_PIN H14   IOSTANDARD LVCMOS33 } [get_ports { sw[3] }];
```

运行结果如图



题目 2

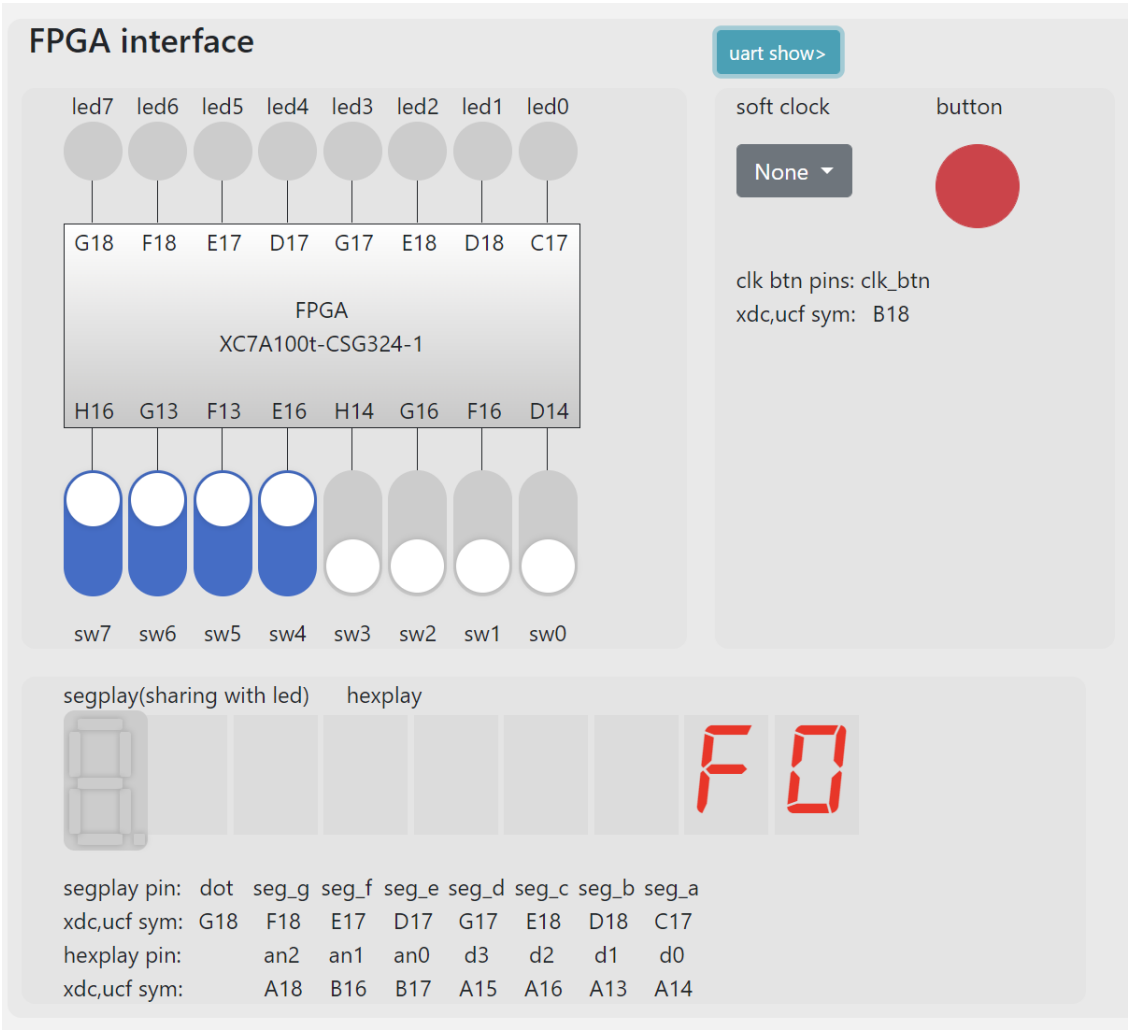
设计文件如图

```
module t2(
    input clk,
    input [7:0]sw,
    output reg [3:0]h,
    output reg An
    );
    reg [19:0] cnt;
    wire clk_100hz;
    assign clk_100hz= (cnt>=500000);
    always@(posedge clk)
    begin
        if(cnt>=999999) cnt<=0;
        else cnt<= cnt+1;
    end
    always@(posedge clk)
    begin
        if(clk_100hz)begin
            An<=1'b1;
            h<=sw[7:4];
        end
        else begin
            An<=1'b0;
            h<=sw[3:0];
        end
    end
endmodule
```

约束文件如图

```
# Clock signal
set_property -dict { PACKAGE_PIN E3    IOSTANDARD LVCMOS33 } [get_ports { clk }]; #
#create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports {CLK1
## FPGAOL BUTTON & SOFT_CLOCK
#set_property -dict { PACKAGE_PIN B18   IOSTANDARD LVCMOS33 } [get_ports { rst }];

## FPGAOL HEXPLAY

set_property -dict { PACKAGE_PIN A14   IOSTANDARD LVCMOS33 } [get_ports { h[0] }];
set_property -dict { PACKAGE_PIN A13   IOSTANDARD LVCMOS33 } [get_ports { h[1] }];
set_property -dict { PACKAGE_PIN A16   IOSTANDARD LVCMOS33 } [get_ports { h[2] }];
set_property -dict { PACKAGE_PIN A15   IOSTANDARD LVCMOS33 } [get_ports { h[3] }];
set_property -dict { PACKAGE_PIN B17   IOSTANDARD LVCMOS33 } [get_ports { An }];


## FPGAOL SWITCH

set_property -dict { PACKAGE_PIN D14   IOSTANDARD LVCMOS33 } [get_ports { sw[0] }];
set_property -dict { PACKAGE_PIN F16   IOSTANDARD LVCMOS33 } [get_ports { sw[1] }];
set_property -dict { PACKAGE_PIN G16   IOSTANDARD LVCMOS33 } [get_ports { sw[2] }];
set_property -dict { PACKAGE_PIN H14   IOSTANDARD LVCMOS33 } [get_ports { sw[3] }];
set_property -dict { PACKAGE_PIN E16   IOSTANDARD LVCMOS33 } [get_ports { sw[4] }];
set_property -dict { PACKAGE_PIN F13   IOSTANDARD LVCMOS33 } [get_ports { sw[5] }];
set_property -dict { PACKAGE_PIN G13   IOSTANDARD LVCMOS33 } [get_ports { sw[6] }];
set_property -dict { PACKAGE_PIN H16   IOSTANDARD LVCMOS33 } [get_ports { sw[7] }];
```

运行结果如图


FPGA interface
uart show>
led7 led6 led5 led4 led3 led2 led1 led0
G18 F18 E17 D17 G17 E18 D18 C17
FPGA
XC7A100t-CSG324-1
H16 G13 F13 E16 H14 G16 F16 D14
sw7 sw6 sw5 sw4 sw3 sw2 sw1 sw0
soft clock
None
button
clk btn pins: clk_btn
xdc,ucf sym: B18
segplay(sharing with led)
hexplay
F 0
segplay pin: dot seg_g seg_f seg_e seg_d seg_c seg_b seg_a
xdc,ucf sym: G18 F18 E17 D17 G17 E18 D18 C17
hexplay pin: an2 an1 an0 d3 d2 d1 d0
xdc,ucf sym: A18 B16 B17 A15 A16 A13 A14

题目 3

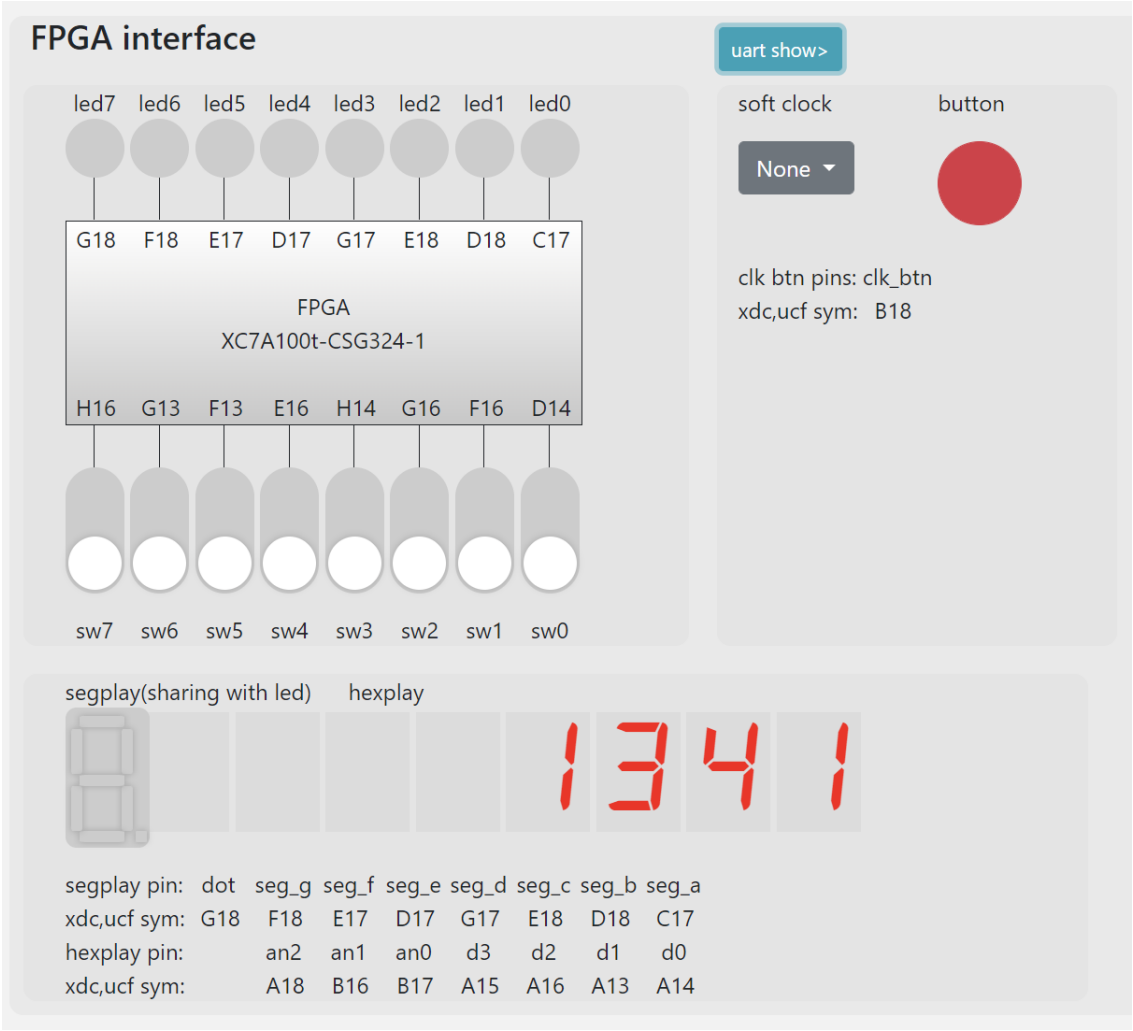
设计文件如图

```
module T3(
        input clk,rst,
        output reg[3:0] h,
        reg [1:0]An
    );
    wire clk_10hz,clk_200hz;
    reg[23:0] cnt_1;
    reg[19:0] cnt_2;
    assign clk_10hz= (cnt_1 == 24'h1);
    assign clk_200hz= (cnt_2 == 20'h1);
    always@(posedge clk)
    begin
        if(rst) cnt_1 <= 0;
        else if(cnt_1 >= 9999999) cnt_1 <= 0;
        else cnt_1 <= cnt_1+1;
    end
    always@(posedge clk)
    begin
        if(rst) cnt_2 <= 0;
        else if(cnt_2 >= 499999) cnt_2 <= 0;
        else cnt_2 <= cnt_2+1;
    end
    reg [3:0] deca_sec , sec, ten_sec , min;
    always @(posedge clk)
    begin
        if (rst)
        begin
            min <= 4'h1;
            ten_sec <= 4'h2;
            sec <= 4'h3;
            deca_sec <= 4'h4;
        end
        else if (clk_10hz)
        begin
        if (deca_sec >= 4'h9)
        begin
            deca_sec <= 4'h0;
            if (sec >= 4'h9)
            begin
                sec <= 4'h0;
                if (ten_sec >= 4'h5)
                begin
                    ten_sec <= 4'h0;
                    if (min >= 4'h9) min <= 4'h0;
                    else min <= min + 1;
                end
                else ten_sec <= ten_sec + 1;
            end
        else sec <= sec + 1;
        end
        else deca_sec <= deca_sec + 1;
        end
    end
    always @(posedge clk)
    begin
        if (clk_200hz)
        begin
            if (An >= 2'h3) An <= 2'h0;
            else An <= An + 1;
        end
    end
    always @(posedge clk)
    begin
        case(An)
        2'h0: h <= deca_sec;
        2'h1: h <= sec;
        2'h2: h <= ten_sec;
        2'h3: h <= min;
        endcase
    end
endmodule
```

约束文件如图

```
# Clock signal
set_property -dict { PACKAGE_PIN E3    IOSTANDARD LVCMOS33 } [get_ports { clk }]; #
#create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports {CLK1
## FPGAOL BUTTON & SOFT_CLOCK
set_property -dict { PACKAGE_PIN B18   IOSTANDARD LVCMOS33 } [get_ports { rst }];

## FPGAOL HEXPLAY

set_property -dict { PACKAGE_PIN A14   IOSTANDARD LVCMOS33 } [get_ports { h[0] }];
set_property -dict { PACKAGE_PIN A13   IOSTANDARD LVCMOS33 } [get_ports { h[1] }];
set_property -dict { PACKAGE_PIN A16   IOSTANDARD LVCMOS33 } [get_ports { h[2] }];
set_property -dict { PACKAGE_PIN A15   IOSTANDARD LVCMOS33 } [get_ports { h[3] }];
set_property -dict { PACKAGE_PIN B17   IOSTANDARD LVCMOS33 } [get_ports { An[0] }];
set_property -dict { PACKAGE_PIN B16   IOSTANDARD LVCMOS33 } [get_ports { An[1] }];
```

运行结果如图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uart show>
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G18 F18 E17 D17 G17 E18 D18 C17
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H16 G13 F13 E16 H14 G16 F16 D14
sw7 sw6 sw5 sw4 sw3 sw2 sw1 sw0
soft clock
button
None
clk btn pins: clk_btn
xdc,ucf sym: B18
segplay(sharing with led)
hexplay
1341
segplay pin: dot seg_g seg_f seg_e seg_d seg_c seg_b seg_a
xdc,ucf sym: G18 F18 E17 D17 G17 E18 D18 C17
hexplay pin: an2 an1 an0 d3 d2 d1 d0
xdc,ucf sym: A18 B16 B17 A15 A16 A13 A14

5 总结与思考

1. 学会了在 vivado 中使用 ip 核和生成时钟
2. 本次实验难度较大
3. 本次实验任务量非常重
4. 好迷，完全不知道在搞什么