Bellman-Ford on FPGA

The Single-Source Shortest Path (SSSP) algorithms are a fundamental class of algorithms in computer science and graph theory. Specifically, the algorithms find the shortest paths from a source vertex to all other vertices in a graph. Perhaps the most popular algorithm in the class is the Bellman-Ford algorithm, which not only finds all the shortest paths in O(VE) time, but also can be used to determine if the graph contains a negative weight cycle. Pseudo-code for the algorithm follows below:

```
for each vertex x in V do
        if x is source then
                w(x) = 0
        else
                w(x) = INFINITY
        end if
end for
for i = 1 to v - 1 do
        for each edge(i, j) in E do
                if w(i) + w(i, j) < w(j) then
                        w(j) = w(i) + w(i, j)
                        p(j) = i //predecessor
                end if
        end for
end for
for each edge(i, j) in E do
        if w(j) > w(i) + w(i, j) then
                return false //negative weight cycle
        end if
end for
return true
```

In order to speed-up the Bellman-Ford algorithm, we seek to implement the algorithm on a field-programmable gate array (FPGA) and in parallel. Several research papers have been devoted to the topic and we will base our further discussion on insights realized in “Accelerating Large-Scale Single-Source Shortest Path on FPGA.” The two principal components of the algorithm are a sorting block and relaxation module. The sorting block takes p amount of edges and determines which edge should be considered for its associated destination vertex during relaxation. The relaxation module takes the processed edges and compares them to the weight of the destination vertex. If the processed edge weight plus the source vertex is less than the current weight of the destination vertex then the destination vertex is updated. Further descriptions of these two modules follow in the schematics below and to the right:

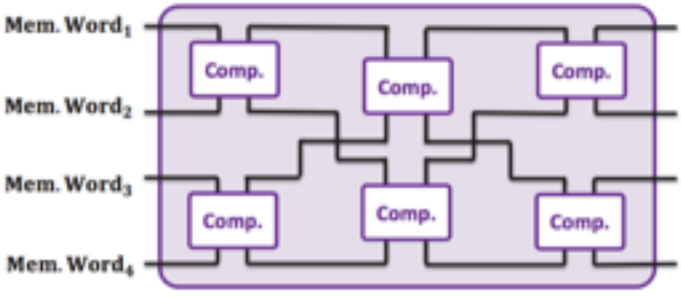

Fig. 2: Sorting block for $p = 4$

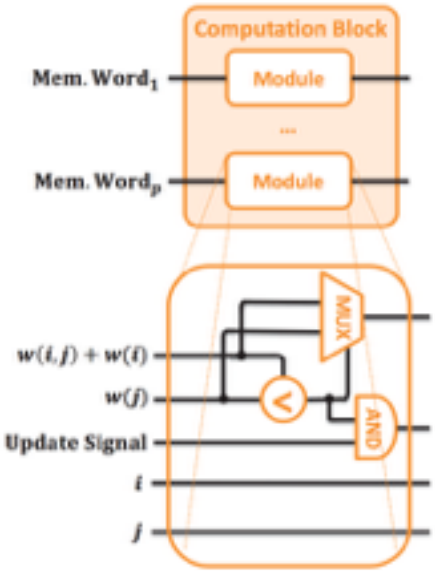

Fig. 3: Comparison Module