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Cpre 288 – Five Why's Extra Credit

Five Why's Exam 2 – Question 6

1. *Why was this question marked incorrect?*

   I didn't answer the question correctly.

2. *Why did I do it incorrectly?*

   a. I didn't realize that the parity bit is always set to 0 by default for the UART Line Control register.

   b. I misunderstood the what the question was asking me.

3. *Why didn't I realize that the UART Line Control Register's parity bit is always set to 0 by default?*

   a. I misread what the register map and the ULCR's description was saying the datasheet.

3. *Why did I misunderstand the question?*

   a. I did take my time to fully read the question, I rushed through it.

4. *Why did I misread what the register map and the UCLR's description was saying?*

   a. I thought the description was telling me that the register's parity bit was always set to 1 and that the user would have to personally set it to 0 for even parity.

4. *Why didn't I take my time to fully read the question?*

   a. I was on a time crunch and I wanted to give myself enough time to put some thought into Part B of the exam.

5. *Why did I think the description was telling me that the register's parity bit was always set to 1 and that the user would have to personally set it to 0 for even parity?*

    a. I didn't do a good enough job reviewing how the registers we used in lab were initialized. I also could've done a better job of understanding what the parity bit did in the UCLR.

5. *Why was I on a time crunch and I wanted to give myself enough time to put some thought into Part B of the exam?*

    a. I took too much time on earlier parts of Part A and I also spent too much time looking for information in the datasheet. I should have a quick reference guide on me so that I would have known exactly where to go look for the information that I needed.

Root Cause: Ultimately, the bulk of my problems came from the fact I didn't do a good job of reading what the question was asking me when it came to minimum number of bits required for the parity bit in the UCLR. This was mainly because I had wasted a lot of time on the earlier questions in the exam, so I began to rush through the remaining questions to get to Part B quicker, and this was because I spent a lot of time looking for stuff in the datasheet. If I had followed the advice of the TA's and spent some time reviewing how we set the UARTs up in lab then I might have known instinctively that for the UCLR the minimum amount of bits for the parity bit was 0.