Sound Analysis Synthesis and Processing: SSSP Homework

May 30, 2024

The topic of this homework is Wave Digital Filter (WDF) modeling. You will be required to model a section of the famous MXR Distortion+ guitar pedal in the Wave Digital (WD) domain starting from a reference analog circuit.

The circuit consists of three main sections: the op-amp stage, the clipping stage, and the power supply stage. The first stage consists of a non-inverting op-amp that provides high input impedance, amplitude gain, and filtering. The op-amp output is then passed through a decoupling capacitor to the clipping stage, which contains two antiparallel diodes that contribute to the pedal's distinctive sound. This stage distorts the signal by clipping it within an upper and lower threshold [1]. The complete circuit schematic of the MXR Distortion+ is shown in Fig. 1.

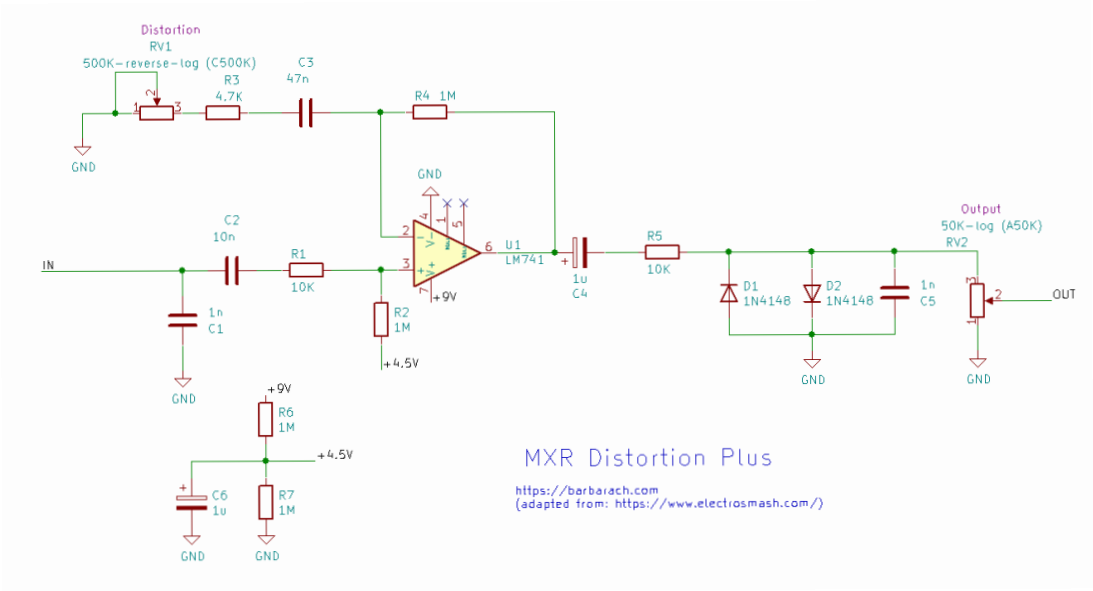

Figure 1: MXR Distortion+ schematic.

1 Reference Circuit

The analog circuit that we will consider as a reference for designing the WD structure is reported in Fig. 2. We assume that the signal fed from the first stage can be represented by a resistive voltage source V_{in}, which is AC coupled to the rest of the circuit through capacitor C_1. Resistor R_1 limits the amount of current into the diodes, while the capacitor C_2 placed in parallel to the diodes D_1 and D_2 filters out higher frequency harmonics. Resistor R_{out} is a potentiometer controlling the output volume: in our analysis, we are going to assume that its resistance value is fixed. The circuit parameters are summarized in Table 1, while the D_1 and D_2 diode parameters are reported in Table 2.

R_{in}	R_1	R_{out}	C_1	C_2
1 Ω	10 kΩ	10 kΩ	1 µF	1 nF

Table 1: Values of the parameters of the MXR Distortion+ Clipping Stage circuit shown in Fig.2

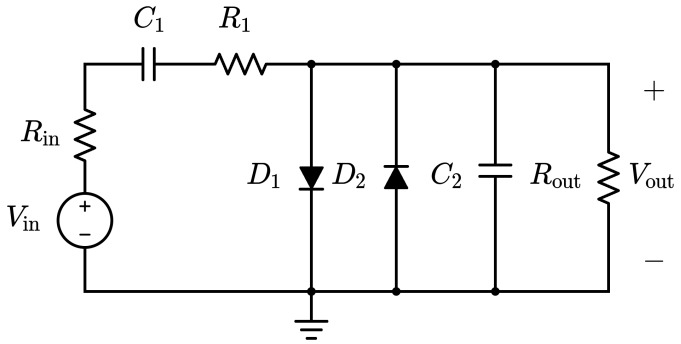

Figure 2: Reference Circuit: MXR Distortion+ Clipping Stage.

I_{s}	V_{t}	η
2.52nA	25.864mV	1.752

Table 2: Shockley diode model parameters (1N914 diodes).

1.1 Simscape Implementation of the Reference Circuit (optional)

You are not expected or required to download Simscape and to install it in order to complete this homework and achieve the maximum grade. The output signal of the reference circuit will be provided to you such that you can use it as a ground truth when you implement the required WDF. However, Simscape could help you to analyze the behavior of the reference circuit and search for a smart solution in designing the corresponding WDF structure. A file containing the Simscape implementation of the reference circuit (`diode_clipper_SSC.slx`) is provided. If you think that it can be useful, you can download Simscape for free, using your student license, at the following link: `https://it.mathworks.com/products/simscape.html`.

1.2 Input Signal

The input signal $V_{\text{in}}(t)$ is a synthesized sine wave with fundamental frequency $f_0 = 440$ Hz and sampling frequency $f_{\text{s}} = 96$ kHz. The amplitude $A = 1.5$ V is chosen to be comparable with the amplitude of a guitar signal being amplified by the first stage of the circuit. Such an input signal is modeled as a resistive voltage generator, with resistance $R_{\text{in}} = 1\ \Omega$.

1.3 Output Signal

The output signal $V_{\text{out}}(t)$ of the reference circuit is the voltage measured at the output volume potentiometer, which is modeled as a fixed resistor $R_{\text{out}} = 10$ kΩ.

The ground truth output signal obtained by the Simscape simulation is provided and can be imported in MATLAB using the command (already implemented in the script)

```
load('output_ssc.mat');
```

In this way, you can compare the output signal of the implemented WDF with a ground-truth.

2 Port-wise Definition of Wave Variables

The port-wise definition of wave variables considered in this homework is the same definition of voltage waves we have already seen in class. Therefore, Kirchhoff variables in the discrete-time domain at one

port of an element are expressed in terms of wave variables as

$$v[k] = \frac{a[k] + b[k]}{2} \ , \quad i[k] = \frac{a[k] - b[k]}{2Z[k]} \ , \tag{1}$$

where $v[k]$ is the port voltage, $i[k]$ is the port current, $a[k]$ is the wave incident to the element, $b[k]$ is the wave reflected by the element and $Z[k]$ is a scalar free parameter different from zero.

3 WD Model of the Diode Pair

The nonlinear part of the circuit consists of two antiparallel diodes. In this WD implementation, both diodes are modeled as a single one-port nonlinear element. In order to derive the scattering relation of an antiparallel diode pair, we start from the commonly used Shockley diode model, which expresses the constitutive equation of a diode as

$$i(t) = I_\mathrm{s} \left(e^{\frac{v(t)}{\eta V_\mathrm{t}}} - 1 \right), \tag{2}$$

where I_s is the saturation current, V_t is the thermal voltage, η is the ideality factor, while $v(t)$ and $i(t)$ are the voltage across and the current through the diode, respectively. As we have seen in class, it is possible to express the scattering relation of a single diode in the WD domain as an explicit mapping $b[k] = f(a[k], Z[k], I_\mathrm{s}, V_\mathrm{t}, \eta)$, expressed in terms of the Lambert $\mathcal{W}$ function as

$$\begin{aligned} b[k] &= f(a[k], Z[k], I_\mathrm{s}, V_\mathrm{t}, \eta) \\ &= a[k] + 2Z[k]I_\mathrm{s} - 2\eta V_\mathrm{t} \mathcal{W} \left(-\frac{Z[k] I_\mathrm{s}}{\eta V_\mathrm{t}} e^{\frac{a[k] + Z[k] I_\mathrm{s}}{\eta V_\mathrm{t}}} \right). \end{aligned} \tag{3}$$

Assuming that the two antiparallel diodes are identical and that only one diode conducts at a time (i.e., the reverse current of the diode is negligible w.r.t. its forward current), we can model the antiparallel diode pair in the WD domain as a single one-port nonlinear element characterized by the following scattering relation

$$b = \mathrm{sgn}(a[k]) f(|a[k]|, Z[k], I_\mathrm{s}, V_\mathrm{t}, \eta), \tag{4}$$

where $\mathrm{sgn}(\cdot)$ is the sign function [2].

Note that for this assignment, the MATLAB function `antiparallel_diodes.m` implementing the above scattering relation is already provided.

4 WDF Design

There are many possible ways of representing the reference circuit of Fig. 2 as a WDF structure, all leading to equally accurate results.

You are asked to choose one valid WDF representation of the reference circuit and draw the corresponding WDF scheme. For your convenience, you are encouraged to choose the WDF representation that, according to you, minimizes computational complexity. However, the only constraint on the required WD structure is that it must be computable in a fully explicit fashion; this means that no iterative solvers can be used to implement it in the WD domain.

You have to propose a WDF based on one connection tree characterized by:

- a root (hint - the root should be an element that cannot be adapted);
- one or more nodes (WD topological junctions called adaptors);
- many leaves (linear one-port elements that can be adapted).

As far as nodes of connection trees are concerned, you can use

- N-port series adaptors with $N \geq 3$.
  Remember that one port of a series adaptor, e.g. port 1, can be made reflection-free by setting

$$Z_1 = \sum_{n=2}^{N} Z_n$$

- N-port parallel adaptors with $N \geq 3$.
  Remember that one port of a parallel adaptor, e.g. port 1, can be made reflection-free by setting

$$Z_1 = \frac{1}{\sum_{n=2}^{N} Z_n^{-1}}$$

- N-port arbitrary topological junctions (adaptors) with $N \geq 3$.
  In this general case, the adaptation condition for making, e.g., port 1 reflection-free can be found using the symbolic environment in MATLAB. As an example, here follows a MATLAB-like pseudocode for finding the value of Z_1 that makes a generic 5-port topological junction reflection free at port 1

```
syms Z1 Z2 Z3 Z4 Z5 real

Z=diag([Z1,Z2,Z3,Z4,Z5]);

...

S = eye(5) - 2*Z*B'*inv(B*Z*B')*B;

Z1 = solve(S(1,1)==0,Z1)
```

  where `S` is the scattering matrix of the topological junction and `B` is the corresponding fundamental-loop matrix that maps the subset of independent port currents to all port currents. Matrix `B` depends on the specific topological junction you are considering, as we have seen in class. Additional details on how to compute the fundamental loop matrix $\mathbf{B}$ or the fundamental cut-set matrix $\mathbf{Q}$ of a given directed graph corresponding to a connection network can be found at the following link: `https://www.tutorialspoint.com/network_theory/network_theory_topology_matrices.htm`.

In summary, you are asked to:

1. Draw the proposed WDF scheme including T-shaped stubs at all ports of WD elements and WD junctions that are adapted (reflection-free ports). Please provide a figure created using a drawing software of your choice or a photo of a clear and legible drawing you made on paper. (Note that if we cannot understand something in your drawing, it will be counted as an error).

2. Assign numbers or names to all ports of topological junctions (adaptors).

3. Write down in symbolic form how to set each free parameter of the WDF.
   As an example, if an adapted resistor with resistance R_1 is connected to a port whose free parameter is called Z_4, you will write $Z_4 = R_1$.
   As another example, if a 3-port series adaptor is characterized by free parameters Z_1, Z_2, Z_3 and port 1 is made reflection-free, you will write $Z_1 = Z_2 + Z_3$.

5 WDF Implementation

You are asked to implement the WDF you designed according to the instructions presented in the previous section. You will do this by completing the MATLAB script `diode_clipper_WD.m` that we are providing.

The WD models that you can use for implementing the one-port elements of the reference circuit (apart from the already discussed nonlinear antiparallel diodes) are summarized in Table 3 for your convenience.

As a check of the correctness of your implementation, you are invited to compare the output signal of the WDF structure (i.e., the voltage across R_{out}) with the ground-truth audio signal `output_ssc.mat`, described in Subsection 1.3. You are also required to plot the error signal defined as the difference between the three ground-truth audio signal and the output signal of the WDF.

In the script `diode_clipper_WD.m`, the input signal V_{in} has already been defined, the ground-truth output signal has already been imported, the parameters of the circuit have already been set and the figures plotting the output signal and the error signal are already set up. The only missing parts concern the actual implementation of the WDF.

Table 3: Wave mappings of common WD linear one-port elements.

Constitutive Eq.	**Wave Mapping**	**Adaptation Condition**
$v(t) = V_{\mathrm{g}}(t) + R_{\mathrm{g}} i(t)$	$b[k] = V_{\mathrm{g}}[k]$	$Z[k] = R_{\mathrm{g}}$
$v(t) = Ri(t)$	$b[k] = 0$	$Z[k] = R$
$i(t) = C\frac{dv(t)}{dt}$	$b[k] = a[k-1]$	$Z[k] = \frac{T_{\mathrm{s}}}{2C}$
$v(t) = L\frac{di(t)}{dt}$	$b[k] = -a[k-1]$	$Z[k] = \frac{2L}{T_{\mathrm{s}}}$

Files to be delivered

You are required to deliver the following files:

1. A short **report** (max. 2 pages) in pdf format including
   - the picture of the WDF scheme following the recommendations discussed in Section 4
   - a description of the WDF scheme in words, in case you believe that your scheme requires some further explanation
   - the setting of free parameters due to adaptation conditions (please define the free parameters at each port coherently to the WDF scheme and specify how to set each free parameter using symbolic expressions as indicated in Section 4)
   - the plots of the output signal and of the error signal described in Section 5;
   - the value of the Mean Squared Error (MSE) between the output signal of the WDF structure and the ground-truth.
2. The folder containing the completed MATLAB script named `diode_clipper_WD.m` along with all the other files already provided (namely, the ground truth signal `output_ssc.mat` and the provided MATLAB functions), such that we can directly execute the script in that folder. Please, **deliver just one MATLAB script and avoid producing auxiliary files such as MATLAB functions**.

Remember to write your names both in the report and at the beginning of the MATLAB script as a comment. Put both the report and the folder containing the MATLAB script in another folder called 'SSSP_HW2_Surname' (where 'Surname' is your surname) in case you are doing the homework individually, or called 'SSSP_HW2_Surname1_Surname2' (where your surnames 'Surname1' and 'Surname2' are in alphabetical order) in case you are doing the homework in groups of 2. Finally, compress the folder in a zip file and upload it using the WeBeep platform in the delivery folder. One student will submit a zip file for the entire group; **do not upload the same HW twice**.

References

[1] Electrosmash. "MXR Distortion + Analysis". Available at `https://www.electrosmash.com/mxr-distortion-plus-analysis`. accessed May 28, 2024.

[2] Rafael C. D. Paiva et al. "Emulation of Operational Amplifiers and Diodes in Audio Distortion Circuits". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 59.10 (2012), pp. 688–692. DOI: 10.1109/TCSII.2012.2213358.