POLITECNICO
MILANO 1863

Sound Analysis, Synthesis And Processing

Module 2: Sound Synthesis and Spatial Processing

Wave Digital Filter Modelling

Academic Year 2023/2024

Enrico Dalla Mora - 10937966, Michele Murciano - 10883559

June 27, 2024

Contents

1 - Introduction **2**

2 - WDF scheme **2**

3 - Free parameters **3**

4 - Results **3**

1 - Introduction

Wave Digital Filters (WDFs) are a type of digital filter designed using principles from analog filter theory, specifically wave scattering and transmission lines. They translate analog filter circuits into digital counterparts, preserving properties like stability and passivity. This assignment requires to model the clipping stage of a famous distortion guitar pedal in the Wave Digital (WD) domain starting from a reference analog circuit.

2 - WDF scheme

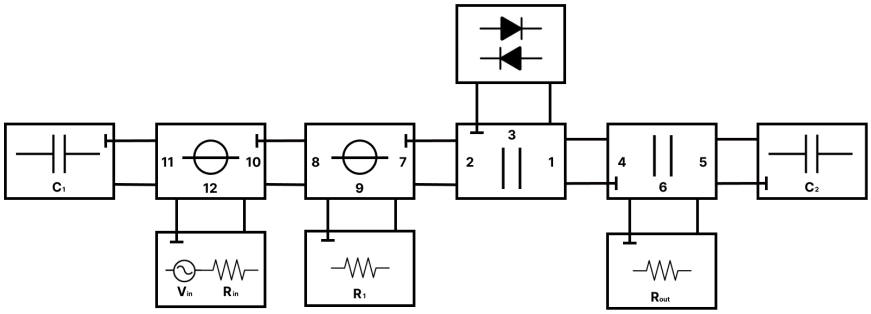

Figure 1: WDF scheme of the reference circuit.

The scheme in figure (1) models the circuit provided by the assignment. As specified, the two antiparallel diodes are modelled as a single one-port nonlinear element which will constitute the *root* of the *binary connection tree*. 3-port WD junctions, constituting the *nodes*, allow to model the connections of the *root* with the linear WD one-port elements, i.e. the *leaves*. In particular, parallel adaptors connect the diodes with the capacitor C_2 and the output resistance R_{out}, where the output voltage V_{out} will be measured. On the left side, series adaptors model the series of R_1, C_1 and the resistive voltage source V_{in}, R_{in}; this portion of network is then connected to the diodes by means of one of the parallel adaptors aforementioned. Note that, the same results could be achieved with different configurations. For example the two 3-port parallel junctions could be replaced by a 4-port parallel junction. The same goes for the two 3-port series adaptors, leading to the following scheme:

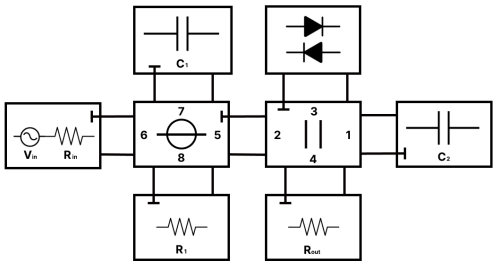

Figure 2: WDF alternative scheme of the reference circuit.

This second configuration (figure 2) was actually tested, providing the exact same results as the first scheme but with significant improvements in the computation time. Its implementation can be found in the file `"diode_clipper_WD_4_port_version.m"`. Moreover, another configuration of the tree could be implemented with a single 6-port generic topological junction. In this case the characteristic scattering matrix should be computed employing the *symbolic environment* and solving for the adaptation condition of the free parameter correspondent to the diodes port. Nonetheless, it was chosen to adopt the first connection tree (figure 1) in order to express the forward and backward scans in a more explicit fashion.

3 - Free parameters

The setting of free parameters is crucial in implementing the wave digital filter. Each element or junction port is defined by wave variables (incident wave $a[k]$ and reflected wave $b[k]$) and a free parameter Z_n, called the *reference port resistance*. Properly setting Z_n avoids the instantaneous dependency of $b[k]$ on $a[k]$, creating a reflection-free port.
Linear elements, represented by one-port blocks in the WDF scheme (leaves of the WDF tree), have been adapted according to the adaptation conditions specified in Table 3 of the assignment, leading to the free parameters values specified in the table on the right. For junctions instead, each port has been made reflection-free using the two well-know equations for series and parallel connections coming from Kirchhoff's theory. Once this is done, scattering matrices are computed with the following relations:

$$Parallel: \ S = 2Q^T(QZ^{-1}Q^T)^{-1}QZ^{-1} - I$$

$$Series: \ S = I - 2ZB^T(BZB^T)^{-1}B$$

and wave variables are set accordingly to the following table:

Voltage Source	Resistor	Capacitor
$b[k] = V_g[k]$	$b[k] = 0$	$b[k] = a[k-1]$

Table 1: Wave mapping of linear one-port elements.

Capacitors
$Z_{11} = \frac{T_s}{2C_1}$
$Z_5 = \frac{T_s}{2C_2}$
Resistances
$Z_9 = R_1$
$Z_6 = R_{\text{out}}$
$Z_{12} = R_{\text{in}}$
Series Junctions
$Z_{10} = Z_{11} + Z_{12}$
$Z_7 = Z_8 + Z_9$
Parallel Junctions
$Z_4 = \left(Z_5^{-1} + Z_6^{-1}\right)^{-1}$
$Z_3 = \left(Z_1^{-1} + Z_2^{-1}\right)^{-1}$
Topological Connections
$Z_8 = Z_{10}$
$Z_2 = Z_7$
$Z_1 = Z_4$

The `"antiparallel_diodes.m"` function computes the wave mapping relation for the anti-parallel diodes. Finally, forward and backward paths are evaluated.

4 - Results

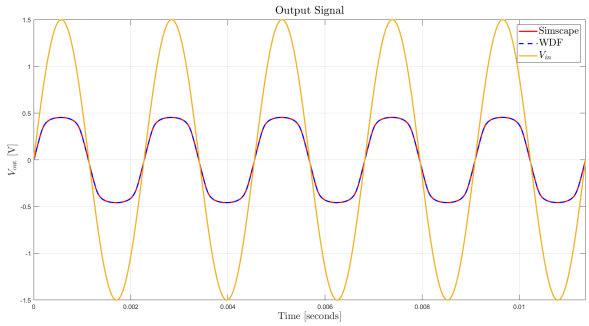

Figure 3: Output voltage compared to reference one and input voltage.

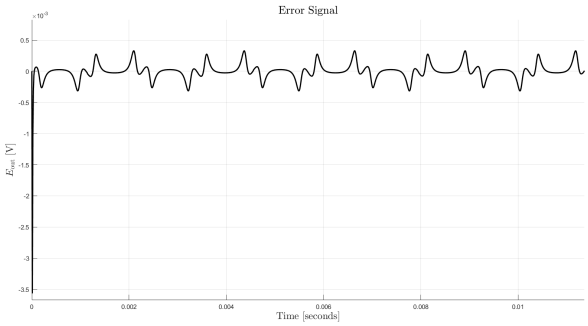

Figure 4: Error - difference between estimated and reference output voltages.

As depicted in figures 3 and 4, the algorithm simulates the analog circuit with very high fidelty. In particular, the obtained *Mean Squared Error* is equal to $MSE = 2.0941 \cdot 10^{-7}$ and this verifies the accuracy of the model. Some considerable differences between the computed output and the ground truth can be seen in the very first time instants. This is probably due to initial conditions and relative variables initialization. Nonetheless, this discrepancy is in the order of 10^{-3} V and quickly disappears therefore it does not compromise the reliability of the model.