TCL 华星

MODEL: ST6451D08-6

Ver. 2.1

Date: 16.Feb.2023

Customer's Approval	CSOT
Signature Date	Approved By Product Director Date Name: Yuming Mo Signature:
	Reviewed By PDT Manager Date Name: Tony Signature: Tony 2023.2.17
	Reviewed By Project Leader Date Name: Huaiyu Wang Signature: 2023.2.16
	Reviewed By PM Date Name: Jinshi Wang Signature: 2023.2.16

Contents

Revision History

Version	Date	Page (New)	Section	Description	Revision by
Ver. 1.0	5.Aug.2022	All	All	TentativeSpecification was First Issued	Huaiyu Wang
Ver. 1.1	22.Nov.2022	22	All	Update driver EQ setting	Huaiyu Wang
Ver. 2.1	16.Feb.2023	ALL	All	Final Specification was Issued	Huaiyu Wang

1. General Description

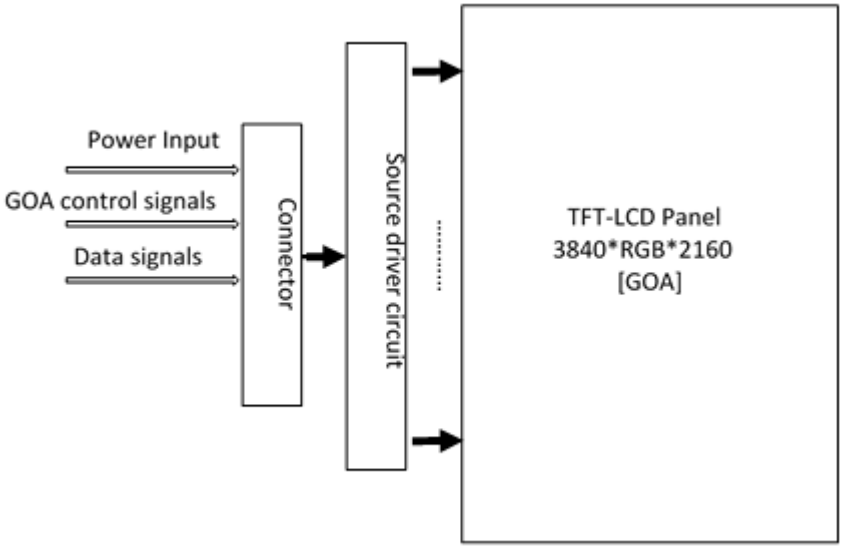
1.1 Product Features

- **QFHD Resolution (3840 x 2160)**
- **Very High Contrast Ratio:7000:1**
- **Fast Response Time**
- **High Color Saturation: 72% NTSC**
- **Ultra Wide Viewing Angle: 178° (H)/178° (V)(CR≥10)**
- **DLG function**
- **CSPI4.0B interface**

1.2 Overview

ST6451D08-6 is a diagonal 64.5”color active matrix open cell. This open cell is a trans missive type display operating in the normally black mode. It supports 3840x2160 QFHD resolution and can display up to 1.07G colors (8bit+FRC). Each pixel is divided into Red, Green and Blue sub-pixels which are arranged in vertical stripe.

This open cell dedicates for LCD TV products and provides excellent performance which includes high brightness, ultra wide viewing angle, high color saturation and high color depth. CSOT open cell comply with ROHS for identification.



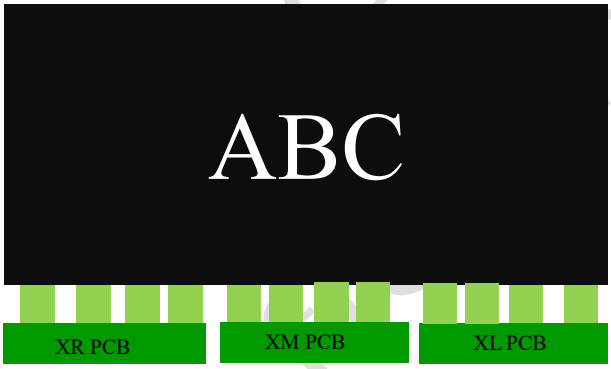
1.3 General Information

Item	Specification	Unit	Note
Cell Size	1440.48H)x 816.02(V)	mm	
Active Area	1428.48 (H)x803.52 (V)	mm	
Weight	3.70	kg	
Driving Scheme	a-Si TFT Active Matrix	-	
Number of Pixels	3840x2160	pixel	
Pixel Pitch (Sub Pixel)	0.124(H)x 0.372(V)	mm	
Pixel Arrangement	RGB Vertical Stripe	-	

Display Colors	1.07G	color	8bit+FRC
Display Mode	Transmissive Mode, Normally Black	-	
Glass Thickness (Array/CF)	0.5/0.5	mm	
Color Chromaticity	Red(0.646,0.335) Green(0.309,0.615) Blue(0.153,0.057) White(0.273,0.281)		Typical value measured at CSOT's module BLU
Contrast Ratio	7000:1 (Typ.)		
Cell Transmittance	5.15% typ,4.64%min	%	
View Angle(CR≥10)	178 °(H)/178 °(V) (Typ.)		
Surface Treatment	Anti-Glare, Haze 2%， Hard Coating(3H) –CF POL		
Display Orientation	Signal input with "ABC"		（1）

Note(1)：LCD display as below illustrated when signal input with "ABC"

Front side



2. Absolute Maximum Ratings

2.1 Absolute Maximum Ratings (Ta = 25 ± 2 °C)

The followings are maximum values which, if exceeded, may cause damage to the unit.

Item	Symbol	Value		Unit
		Min.	Max.	
Digital Supply Voltage	VDD1V8	-0.3	2.5	V
Digital Supply Voltage	VDD3V3	-0.3	3.6	V
Analog Supply Voltage	AVDD	-0.3	19.8	V

2.2 Environment Requirement

(1) Temperature and relative humidity range are shown as below

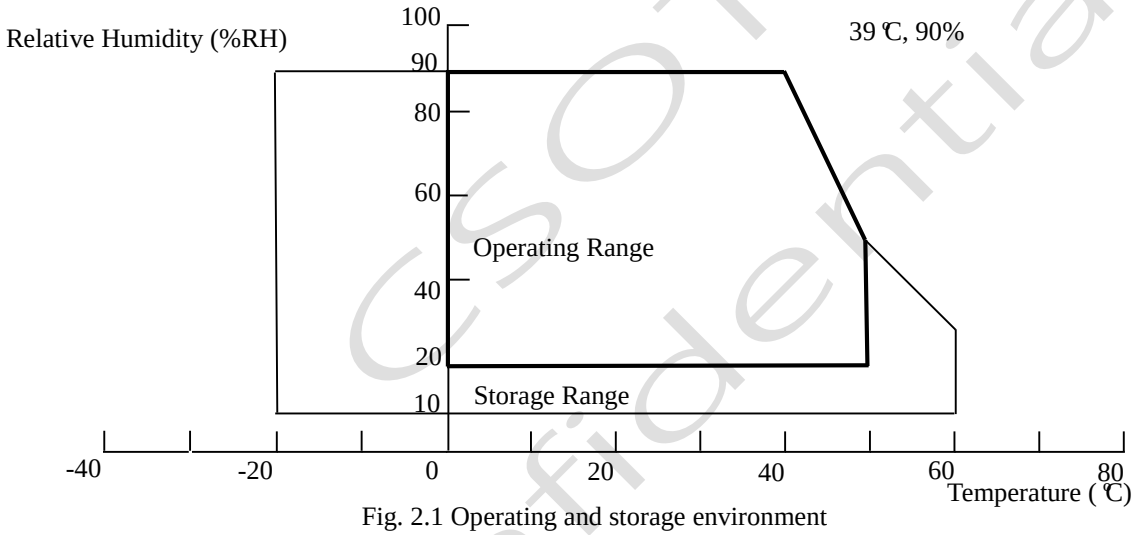


Fig. 2.1 Operating and storage environment

(a) 90%RH maximum (Ta ≤39 ℃).

(b) Wet-bulb temperature should be 39 ℃maximum (Ta>39 ℃).

(c) No condensation.

(2) The storage temperature is between -20 ℃ to 60 ℃, and the operating ambient temperature is between 0 ℃to50 ℃.

The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ℃ with LCD module in a temperature controlled chamber alone. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ℃. The range of operating temperature may degrade in case of improper thermal management in the end product design.

(3) The rating of environment is based on LCD module. Leave LCD cell alone, this environment condition can't be guaranteed. Except LCD cell, the customer has to consider the ability of other parts of LCD module and LCD module process.

2.3 Package Storage

When storing open cell as spares for a long time, please follow the precaution instructions:

(1) Do not store the open cell in high temperature and high humidity for a long time. It is highly recommended to store the open cell with temperature from5 ℃ ~ 40 ℃ and humidity from 35%RH~75%RH with shipping package.

(2)The open cell should be keep at a circumstance shown below:

0-2months	2-3months	3-6months
No baking	50℃、10%RH，24hr	50℃、10%RH，48hr

3. Electrical Specification

3.1 Electrical Characteristics

3.1.1 Open Cell DC voltage and ripple (Ta =25 ± 2ºC)

Parameter	Symbol	Value			Ripple	Note
		Min.(V)	Typ.(V)	Max.(V)	Pk-Pk (mV)	
Analog power supply	VAA	16.9	17.20	17.5	1720	(1)
Digital power supply	VDD1V8	1.65	1.80	1.95	180	
Digital power supply	VDD1V9	1.65	1.80	1.95	200	
Power supply for Gate on output	VGH	30.00	30.54	31.00	3000	(3)
Power supply for Gate off output	VGL	-9.70	-10.00	-10.30	1000	
Power voltage for GOA circuit	VSSQ	-9.70	-10.00	-10.30		(1)
Power voltage for GOA circuit	VSSG	-5.70	-6.00	-6.30		
Power supply for flash	VDD33	3.15	3.30	3.45	330	
Power supply for cell Vcom	CFVCM	6.35	6.50	6.65	70	
Power supply for cell Vcom	AVCM	6.35	6.53	6.65	70	
Power supply for cell Vcom	SVCM	8.35	8.50	8.65	85	
Power supply for source IC	HVAA	7.65	7.93	8.25	800	
Gamma voltage	GM_UH~GM_UL	HVAA+0.2	-	VAA-0.2		(2)
	GM_LH~GM_LL	0.2	-	HVAA-0.2		
	GM_UH	15.85	16.00	16.15	150	(1)
	GM_UL	8.5	8.65	8.8	150	
	GM_LH	7.1	7.25	7.4	/	
	GM_LL	0.13	0.215	0.33	/	

Note:

（1）Measurement condition : Ta = 25 ±2 ℃, F = 120Hz. The test patterns are shown as below. All the value and ripple voltage is measured on XB PCBA.

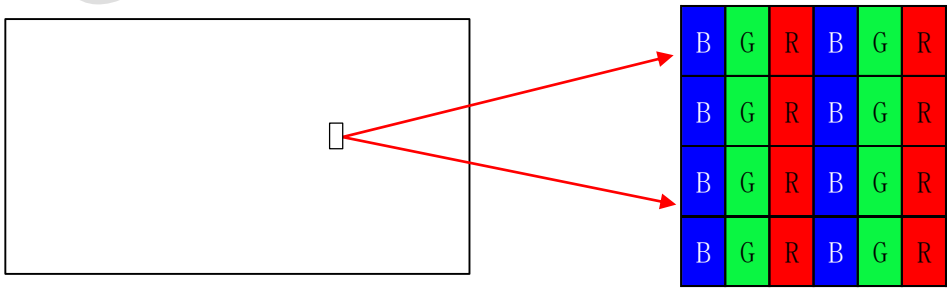


Fig. 3.1 White pattern

(1) HVAA must be: GM_LH+0.2V<HVAA<GM_UL-0.2V

(2) The value of VGHF,VGL ripple just refer to CSOT design.

3.1.2 Power design current demand

Symbol	RMS Value （Unit：mA）	Symbol	RMS Value （Unit：mA）	Symbol	RMS Value （Unit：mA）
120Hz		DLG 240Hz		144 Hz	
I_{VAA}	1981	I_{VAA}	1989	I_{VAA}	2160
I_{VDD1V8}	286	I_{VDD1V8}	286	I_{VDD1V8}	295
I_{VDD1V9}	503	I_{VDD1V9}	504	I_{VDD1V9}	507
I_{VGH}	105	I_{VGH}	194	I_{VGH}	130
I_{VGL}	93.6	I_{VGL}	144	I_{VGL}	98
$I_{VOFF(GOA)VSSQ}$	4.3	$I_{VOFF(GOA)}$	10	$I_{VOFF(GOA)}$	8.6
$I_{VSS(TFT)VSSG}$	3	$I_{VSS(TFT)}$	5.5	$I_{VSS(TFT)}$	2.6
I_{VDD33}	62	I_{VDD33}	63	I_{VDD33}	60
I_{CFVCM}	13	I_{CFVCM}	13	I_{CFVCM}	13
I_{AVCM}	6.5	I_{AVCM}	6.5	I_{AVCM}	6.5
I_{SVCM}	13	I_{SVCM}	13	I_{SVCM}	13
I_{HVAA}	41	I_{HVAA}	36	I_{HVAA}	41

Note:

(1) The above data are recommended values for your reference only

3.1.3 CSPI Differential Signal Characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Driver IC Clock frequency	Freq	1.2	-	3. 5	Gbps	-
input offset voltage	VCM_{CSPI}	0.3	-	0.7	V	(1)
SSCG Modulation Ratio	SS%	-1	-	+1	%	(2)
SSCG Modulation Frequency	f_{SS}	-	-	100	KHz	(2)
Parameter	Symbol	Normalized Time		Differential Amplitude		
Absolute Eye-Diagram Mask	A	0.25	UI	0	mV	CDR Bandwidth = 4MHz Damping factor = 0.7
	B	0.5	UI	60	mV	
	C	0.75	UI	0	mV	
	D	0.5	UI	-60	mV	

Note:

(1) $VCMcspi=(V_{CSPI(P)}+ V_{CSPI(N)})/2$

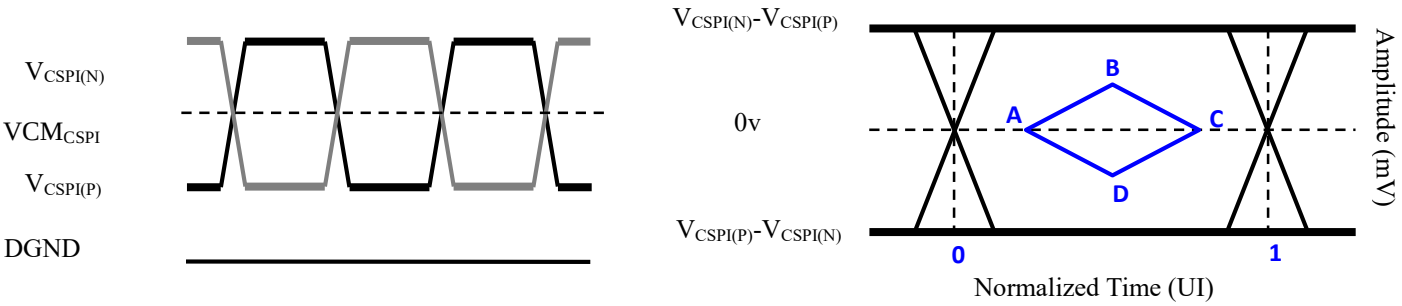


Fig. 3.2 CSPI signal definition

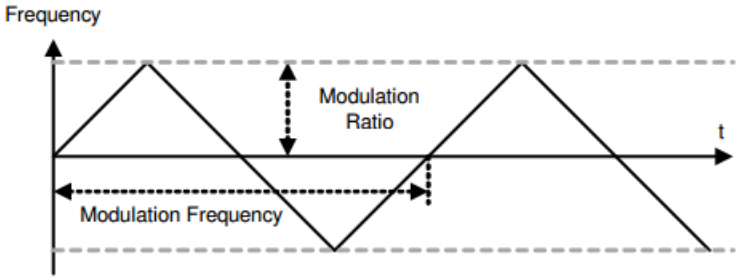


Fig. 3.3 SSCG modulation by modulating clock period

Note:

(2) Recommend SSCG M/R & SSCG MF as follow：

SSCG Modulation Ratio	+/- 0.8%
SSCG Modulation Frequency	33 KHz

3.2 Driver IC ESD spec

The Electro-Static Discharge tolerance of Source COF IC is +-2KV tested by ESD Gun. Especially if the LCD module is designed with the Plastic Bezel, ESD protection solutions should be applied to avoid damaged, as shown in Fig.3.4.

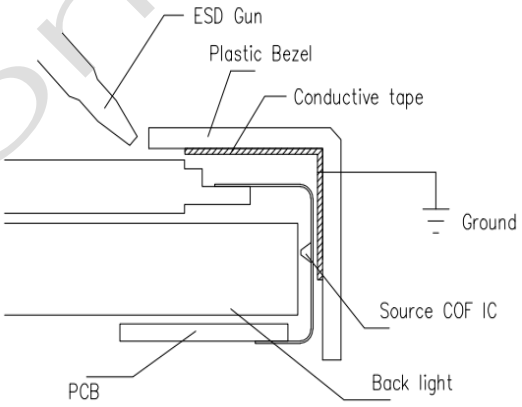


Fig. 3.4 Source COF IC ESD protection

3.3 Driver IC Temperature spec

Parameter	Symbol	SPEC			Unit	Note
		Min.	Typ.	Max.		
Surface temperature	Tc	-	-	120	℃	(1)

Note:

Any point on the IC surface must be less than maximum spec under any conditions, If the surface temperature is out of the spec, thermal solutions should be applied to avoid the damage. CSOT measured IC's surface temperature at room temperature of 25℃.

4. Input Terminal Pin Assignment

4.1 Interface Pin Assignment

CN1: 9-05582101-6 (XDYT) or equivalent

Pin No.	Symbol	Description	Note
1	VAA	Analog power supply	-
2	VAA	Analog power supply	-
3	VAA	Analog power supply	-
4	VAA	Analog power supply	-
5	VAA	Analog power supply	-
6	VAA	Analog power supply	-
7	VAA	Analog power supply	-
8	VAA	Analog power supply	-
9	GM_UH	Gamma Voltage	-
10	GM_UL	Gamma Voltage	-
11	HVAA	Analog power supply	-
12	HVAA	Analog power supply	-
13	GM_LH	Gamma Voltage	-
14	GM_LL	Gamma Voltage	-
15	NC	No Connection	(2)
16	GND	Ground	-
17	LOCK_LS	LOCK signal for source IC	(1)
18	GND	Ground	-
19	CSP12N	CSPI Data Input (12-)	-
20	CSP12P	CSPI Data Input (12+)	-
21	GND	Ground	-
22	CSP11N	CSPI Data Input (11-)	-
23	CSP11P	CSPI Data Input (11+)	-
24	GND	Ground	-
25	CSP10N	CSPI Data Input (10-)	-
26	CSP10P	CSPI Data Input (10+)	-
27	GND	Ground	-
28	CSP9N	CSPI Data Input (9-)	-
29	CSP9P	CSPI Data Input (9+)	-
30	GND	Ground	-
31	CSP8N	CSPI Data Input (8-)	-
32	CSP8P	CSPI Data Input (8+)	-

33	GND	Ground	-
34	CSP7N	CSPI Data Input (7-)	-
35	CSP7P	CSPI Data Input (7+)	-
36	GND	Ground	-
37	CSP6N	CSPI Data Input (6-)	-
38	CSP6P	CSPI Data Input (6+)	-
39	GND	Ground	-
40	CSP5N	CSPI Data Input (5-)	-
41	CSP5P	CSPI Data Input (5+)	-
42	GND	Ground	-
43	CSP4N	CSPI Data Input (4-)	-
44	CSP4P	CSPI Data Input (4+)	-
45	GND	Ground	-
46	CSP3N	CSPI Data Input (3-)	-
47	CSP3P	CSPI Data Input (3+)	-
48	GND	Ground	-
49	CSP2N	CSPI Data Input (2-)	-
50	CSP2P	CSPI Data Input (2+)	-
51	GND	Ground	-
52	CSP1N	CSPI Data Input (1-)	-
53	CSP1P	CSPI Data Input (1+)	-
54	GND	Ground	-
55	NC	No Connection	(2)
56	NC	No Connection	(2)
57	VDD18	Digital power supply for source driver	-
58	VDD18	Digital power supply for source driver	-
59	VDD19	Digital power supply for source driver	-
60	VDD19	Digital power supply for source driver	-
61	IO3(HOLD)	Demura Flash Hold input	(3)
62	SCK	CLK Signal of SPI	(3)
63	CS	CS Signal of SPI	(4)
64	IO0(DI)	Demura Flash data input/output	(3)
65	IO1(DO)	Demura Flash data input/output	(3)
66	IO2(WP)	Demura Flash Write Protection	(3)
67	VDD33	Digital power supply	-
68	NC	No Connection	(2)

69	VSSG	VSS Signal of TFT	-
70	VSSQ	VSS Signal of GOA	-
71	VSSQ	VSS Signal of GOA	-
72	LC2	LC2 Signal of GOA	-
73	LC1	LC1 Signal of GOA	-
74	NC	No Connection	(2)
75	NC	No Connection	(2)
76	NC	No Connection	(2)
77	NC	No Connection	(2)
78	CK8	CK8 Signal of GOA	-
79	CK7	CK7 Signal of GOA	-
80	CK6	CK6 Signal of GOA	-
81	CK5	CK5 Signal of GOA	-
82	CK4	CK4 Signal of GOA	-
83	CK3	CK3 Signal of GOA	-
84	CK2	CK2 Signal of GOA	-
85	CK1	CK1 Signal of GOA	-
86	ST	ST Signal of GOA	-
87	Reset	RESET Signal of GOA	-
88	SVCOM	Power supply for Share Bar VCOM	-
89	AVCOM	Power supply for Array VCOM	-
90	AVCOM	Power supply for Array VCOM	-
91	CFCOM	Power supply for CF VCOM	-
92	CFCOM	Power supply for CF VCOM	-
93	NC	No Connection	(2)
94	NC	No Connection	(2)
95	GND	Ground	-
96	NC	No Connection	(2)

Note:

The direction of pin assignment is shown as below:

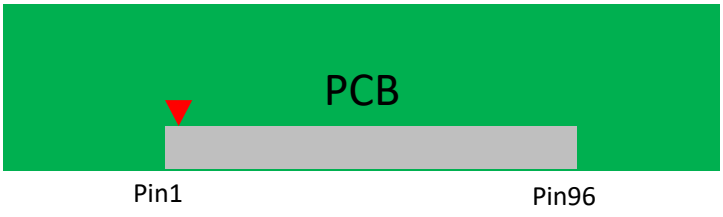


Fig. 4.1 Connector direction sketch map

(1) A.LOCK_LS pin need to pull High 1.8V with 10KΩ on SoC board.

B. LOCK_LS = 'H', Normal Display

LOCK_LS = 'L', T-con re-send training pattern

(2) This pin (NC) is for CSOT use only, please let it open

(3) The SPI signal pin define are named according to XB Flash IC.

(4) This pin (SPI_CS) need to Default Pull High(3.3V) on Master TCON/SOC

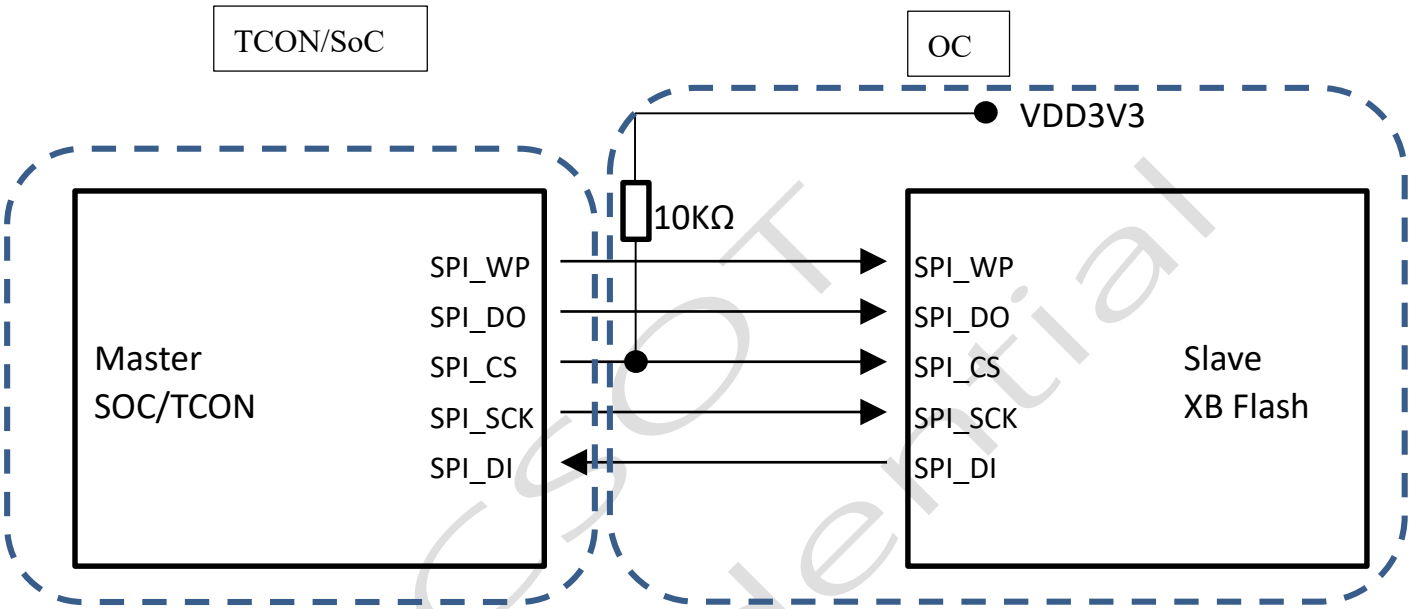


Fig. 4.2 SPI circuit connection diagram

5. Power On/off Sequence

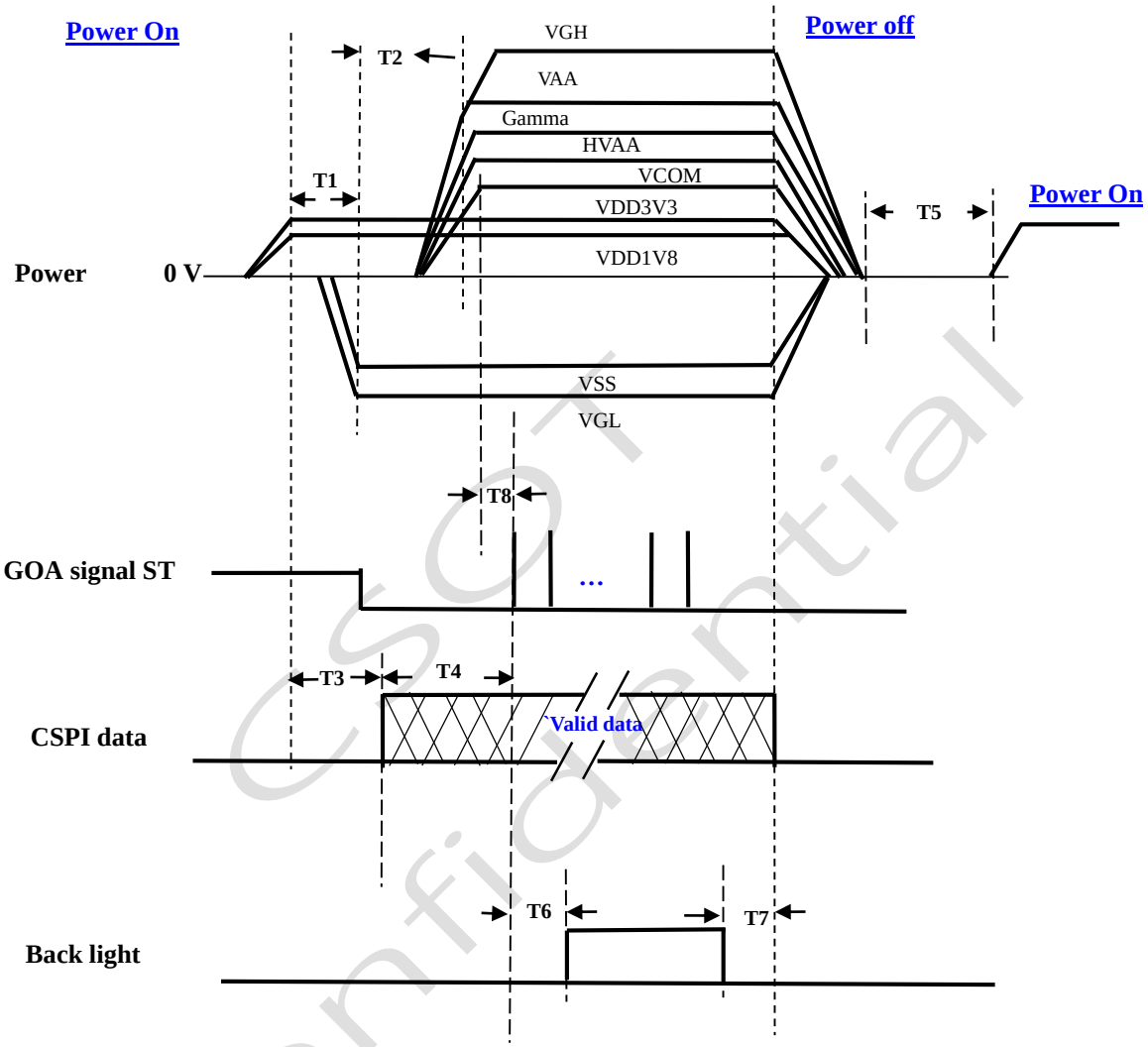


Fig. 5.1 Power sequence

Parameter	Values			Unit
	Min.	Typ.	Max.	
T1	0	-	-	ms
T2	0	-	-	ms
T3	1	-	-	ms
T4	0	-	-	ms
T5	1000	-	-	ms
T6	>0	-	-	ms
T7	>0	-	-	ms
T8	>0	-	-	ms

Note:

(1) please keep these condition: HVAA+0.2V<(GAMA_UH&GAMA_UL)<VAA-0.2V;
0.2V<(GAMA_LH&GAMA_LL)<HVAA-0.2V.

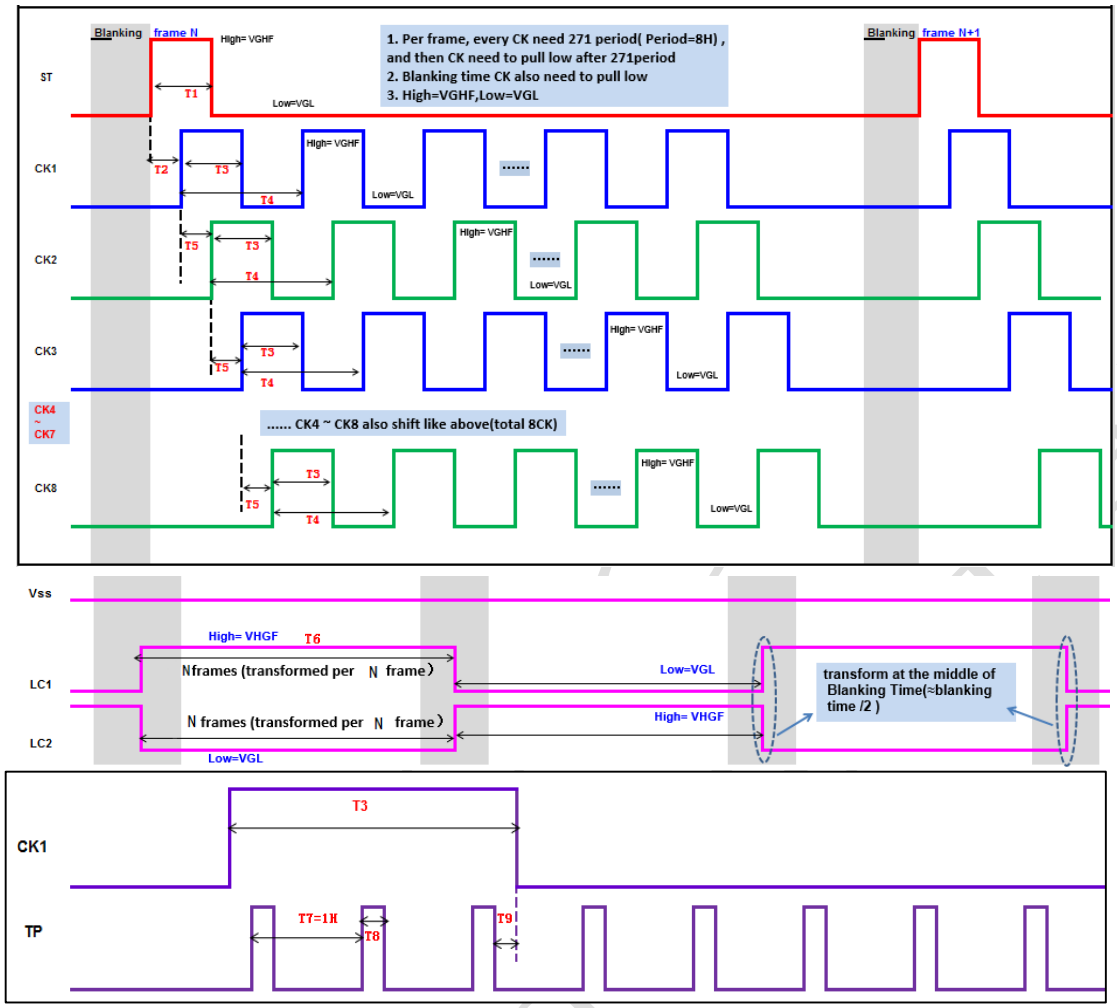
(2) The VAA voltage must be higher than HVAA& gamma all the time.

(3) Please ensure that all the signals are stable before BL on.

(4) VDD1V8 setting time(Max. 10 ms), VAA&HVAA Setting time(max.10ms).

6. Appendix

6.1.1 GOA timing chart



condition: H-total=4400 V-total=2250 Frame rate=60Hz

Parameter	Description	Value	unit	Note
T1	STV Width	37	us	
T2	STV raising to CK1 raising(2H)	14.8	us	
T3	CK High Width	23.68	us	
T4	CK Width	59.2	us	
T5	CK1 falling to CK2 falling(1H)	7.4	us	
T6	LC High/Low Width(100 Frame)	1.67	s	
T7	TP width(1H)	7.4	us	
T8	TP high Width	300	ns	
T9	TP falling to CK1 falling	3.6	us	

Table 6.1.0 60Hz GOA timing table

condition: H-total=4400 V-total=2250 Frame rate=120Hz

Parameter	Description	Value	unit	Note
T1	STV Width	22.2	us	
T2	STV raising to CK1 raising(3H)	11.1	us	
T3	CK High Width	11.84	us	
T4	CK Width	29.6	us	
T5	CK1 falling to CK2 falling(1H)	3.7	us	
T6	LC High/Low Width(200 Frame)	1.67	s	
T7	TP width(1H)	3.7	us	
T8	TP high Width	300	ns	
T9	TP falling to CK1 falling	1.5	us	

Table 6.1.1 120Hz GOA timing table

condition: H-total=4192 V-total=2250 Frame rate=144Hz

Parameter	Description	Value	unit	Note
T1	STV Width	18.54	us	
T2	STV raising to CK1 raising(3H)	9.27	us	
T3	CK High Width	9.89	us	
T4	CK Width	24.72	us	
T5	CK1 falling to CK2 falling(1H)	3.09	us	
T6	LC High/Low Width(240 Frame)	1.67	s	
T7	TP width(1H)	3.09	us	
T8	TP high Width	300	ns	
T9	TP falling to CK1 falling	1.28	us	

Table 6.1.2 144Hz GOA timing table

condition: H-total=4400 V-total=1125 Frame rate=240Hz

Parameter	Description	Value	unit	Note
T1	STV Width	14.8	us	
T2	STV raising to CK1 raising(2.5H)	9.25	us	
T3	CK High Width	5.92	us	
T4	CK Width	14.8	us	
T5	CK1 falling to CK2 falling(0.5H)	1.85	us	
T6	LC High/Low Width(400 Frame)	1.67	s	
T7	TP width(1H)	3.7	us	
T8	TP high Width	300	ns	
T9	TP falling to CK1 falling	0.9	us	

Table 6.1.3 240Hz GOA timing table

6.1.2 GOA OCP setting

Note: The data is the CSOT CS602 recommend setting

OCP Setting	Setting Current		delay time	
	Value	Unit	Value	Unit
STV	40	mA	4	us
CK1-CK8	40	mA	4	us
LC1-LC2	40	mA	4	us
VSS	50	mA	/	/

Table 6.1.2 OCP setting table

6.2. VCOM Adjustment pattern

(1) The CSOT Flicker adjusted the pattern was show as below. This pattern needs column inversion in vertical direction. if customer need below pattern please directly contact with account

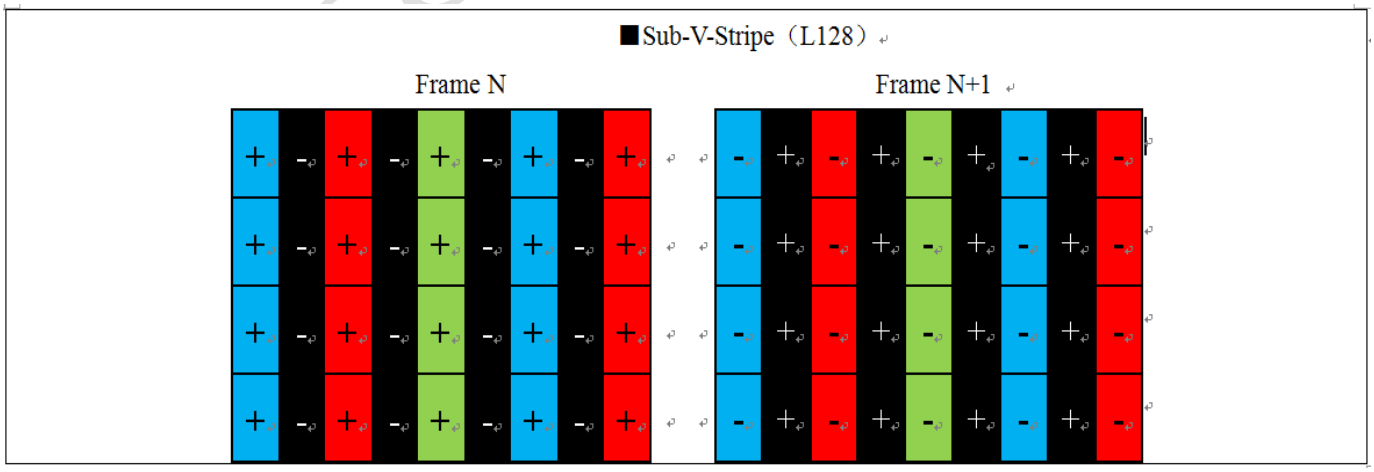


Fig. 6.2.1 Flicker pattern

6.3 Source Driver register setting & EQ setting

REG	reg0	reg1	reg2	reg3	reg4	reg5	reg6	Reg 7	Reg 8~13
8B LSB-> MSB	00000000	11100110	00000100	11101100	01000001	10000110	00000000	00000111	00000000
9B LSB-> MSB	110010110	011100110	100000100	011101100	101000001	010000110	110010110	110010001	110010110
DEC	0	103	32	55	130	97	0	224	0
REG	Reg14	reg15	Reg16	Reg17	Reg18	Reg19	Reg20	Reg 21-22	Reg 23
8B LSB-> MSB	11010000	10010110	10001110	01101001	10100101	11100101	01001101	00000000	10100000
9B LSB-> MSB	001000110	010010110	010001110	101101001	010100101	011100101	101001101	110010110	110101101
DEC	11	105	113	150	165	167	178	0	5
REG	Reg24	Reg25	Reg26	Reg27	Reg28	Reg29	Others		
8B LSB-> MSB	11101010	11010010	11010110	11010001	10001101	00101111	00000000		
9B LSB-> MSB	011101010	011010010	011010110	011010001	010001101	110111001	110010110		
DEC	87	75	107	139	177	244	0		

Driver	Driver1	Driver2	Driver3	Driver4	Driver5	Driver6	Driver7	Driver8	Driver9	Driver10	Driver11	Driver12
EQ	3db	3db	3db	3db	0db	0db	0db	0db	3db	3db	3db	3db

Table 6.3.2 Driver EQ setting

6.4 Cell structure & data mapping

6.4.1 Cell structure

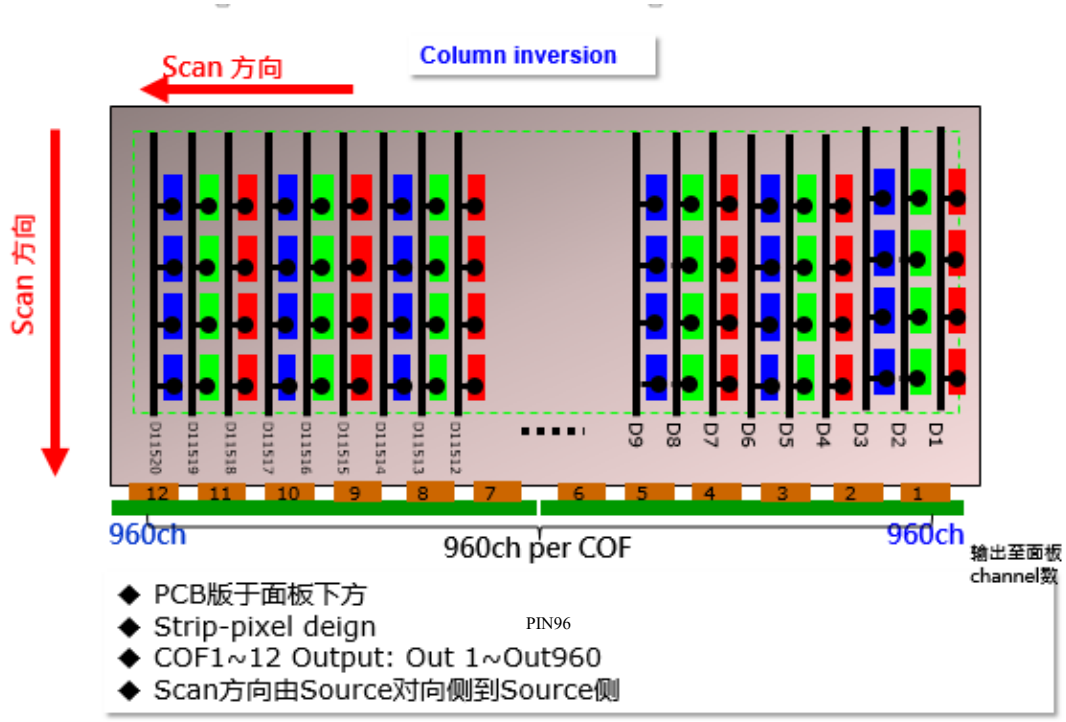


Fig. 6.4.1 Cell structure

6.4.2 Source driver data mapping

Register setting：REG1 [1]= 0, REG2 [5][6]= 01, mode : 8bit-1Pair 960CH, output direction : CH1→ CH960

DR NO.	Data CH NO.				
DR1	1	2	3	……	960
DR2	961	962	963	……	1920
DR3	1921	1922	1923	……	2880
DR4	2881	2882	2883	……	3840
DR5	3841	3842	3843	……	4800
DR6	4801	4802	4803	……	5760
DR7	5761	5762	5763	……	6720
DR8	6721	6722	6723	……	7680
DR9	7681	7682	7683	……	8640
DR10	8641	8642	8643	……	9600
DR11	9601	9602	9603	……	10560
DR12	10561	10562	10563	……	11520

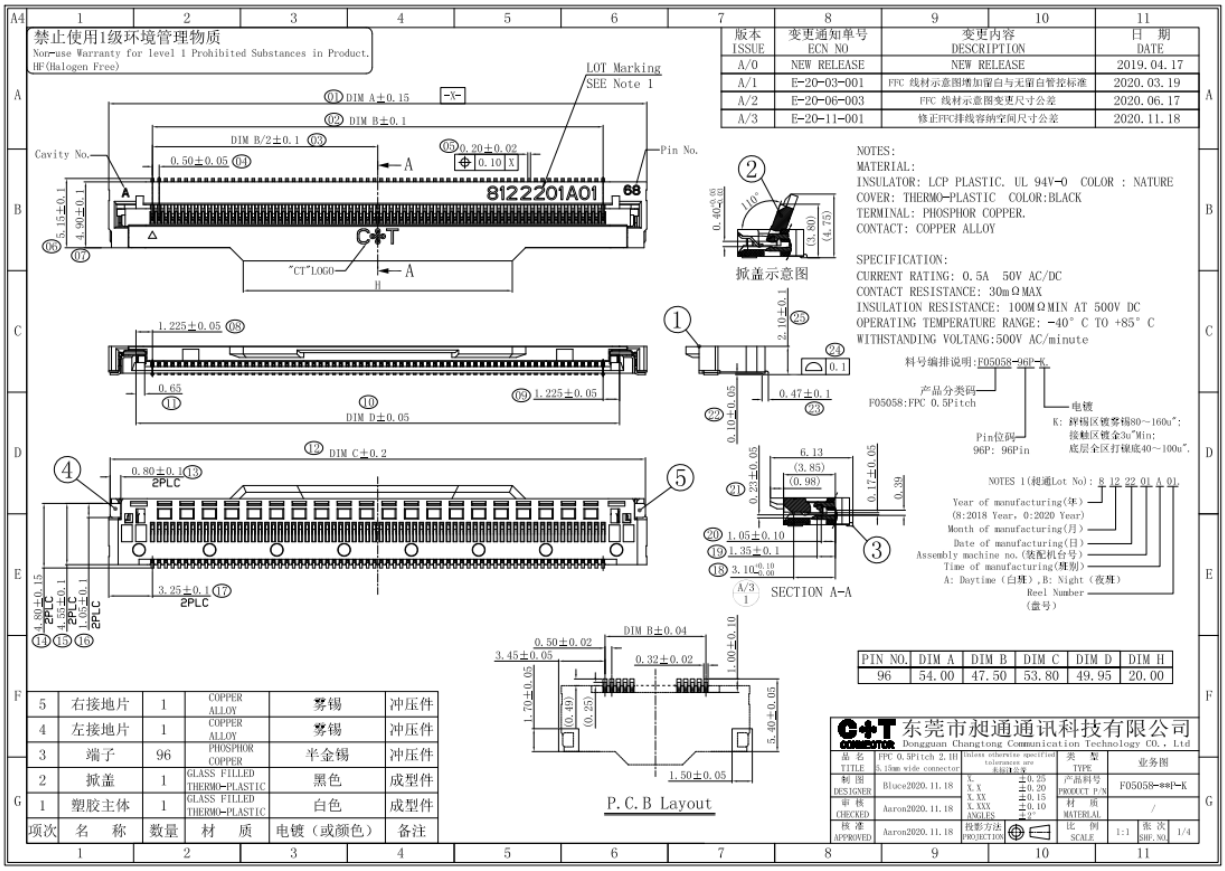
Table 6.4.2.1 Driver data output number

Fig. 6.4.2 input data mapping

Output	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8	CH9	CH10	CH11	CH12
Order	1st data	2nd data	3rd data	4th data	5th data	6th data	7th data	8th data	9th data	10th data	11th data	12th data
Data	R1[0~7]	G1[0~7]	B1[0~7]	R2[0~7]	G2[0~7]	B2[0~7]	R3[0~7]	G3[0~7]	B3[0~7]	R4[0~7]	G4[0~7]	B4[0~7]
Output	CH949	CH950	CH951	CH952	CH953	CH954	CH955	CH956	CH957	CH958	CH959	CH960
Order	949th data	950th data	951th data	952th data	953th data	954th data	955th data	956th data	957th data	958th data	959th data	960th data
Data	R317[0~7]	G317[0~7]	B317[0~7]	R318[0~7]	G318[0~7]	B318[0~7]	R319[0~7]	G319[0~7]	B319[0~7]	R320[0~7]	G320[0~7]	B320[0~7]

Table 6.4.2.2 Each Driver data mapping

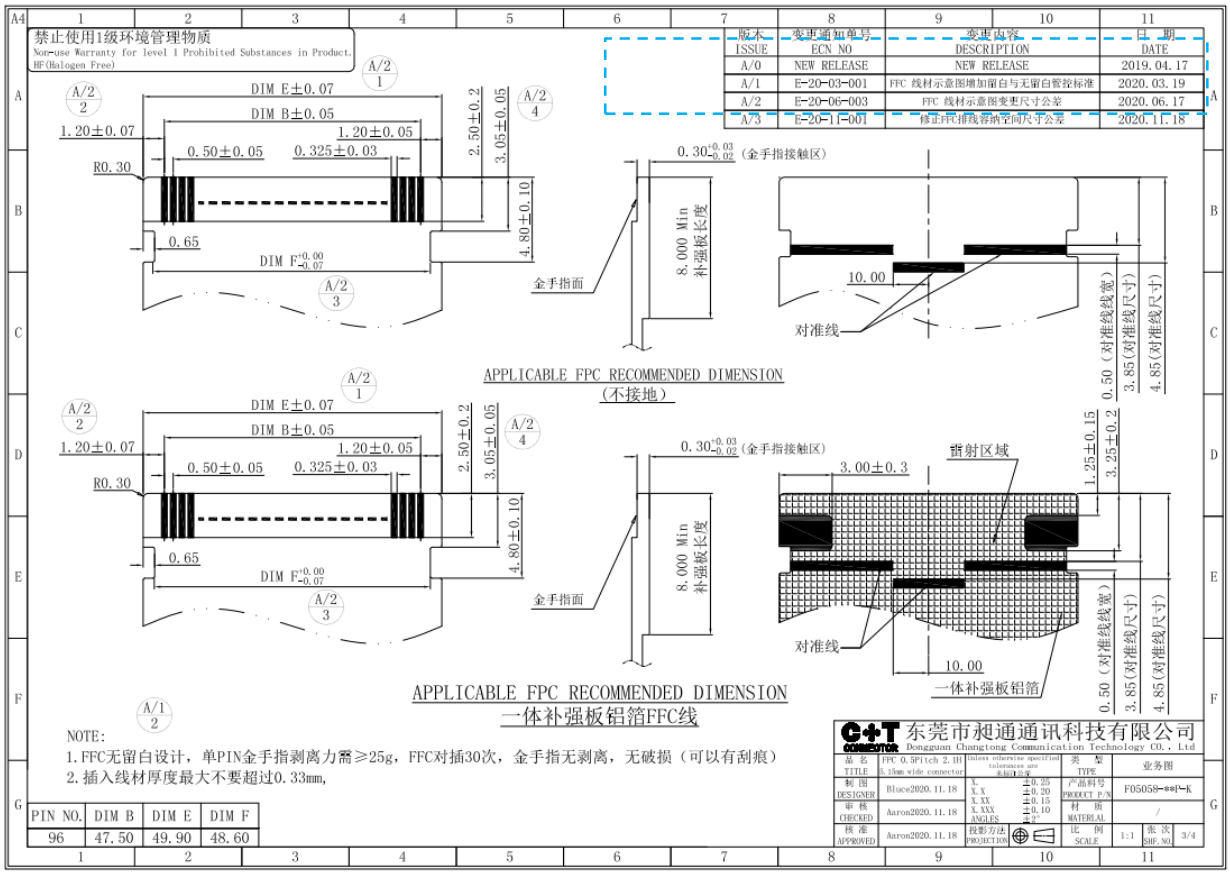
6.5 Input Connector& FFC Drawing



版本 ISSUE	变更通知单号 ECN NO	变更内容 DESCRIPTION	日 期 DATE
A/0	NEW RELEASE	NEW RELEASE	2019.04.17
A/1	E-20-03-001	FFC 线材示意图增加留白与无留白管控标准	2020.03.19
A/2	E-20-06-003	FFC 线材示意图变更尺寸公差	2020.06.17
A/3	E-20-11-001	修正FFC排线容纳空间尺寸公差	2020.11.18

PIN NO.	DIM A	DIM B	DIM C	DIM D	DIM H
96	54.00	47.50	53.80	49.95	20.00

项次	名 称	数量	材 质	电镀（或颜色）	备注
5	右接地片	1	COPPER ALLOY	雾锡	冲压件
4	左接地片	1	COPPER ALLOY	雾锡	冲压件
3	端子	96	PHOSPHOR COPPER	半金锡	冲压件
2	掀盖	1	GLASS FILLED THERMO-PLASTIC	黑色	成型件
1	塑胶主体	1	GLASS FILLED THERMO-PLASTIC	白色	成型件



Note：FFC’s impedance matching recommended to be controlled within 100±10% Ohm.

7 Optical Characteristics

7.1Measurement Conditions

The table below is the test condition of optical measurement.

Item	Symbol	Value	Unit
Ambient Temperature	T_A	25±2	℃
Ambient Humidity	H_A	50±10	%RH
Driving Signal	Refer to the typical value in Chapter 3: Electrical Specification		

To avoid abrupt temperature change during optical measurement, it's suggested to warm up the LCD module more than 60 minutes after lighting the backlight and in the windless environment.

To measure the LCD module, it is suggested to set up the standard measurement system as Fig. 7.1. The measuring area S should contain at least 500 pixels of the LCD module as illustrated in Fig.7.2(A means the area allocated to one pixel).In this model, for example, the minimum measuring distance Z is 370mm when θ is 2 degree. Hence, 500mm is the typical measuring distance. This measuring condition is referred to 301-2H of VESA FPDM 2.0 about viewing distance, angle, and angular field of view definition.

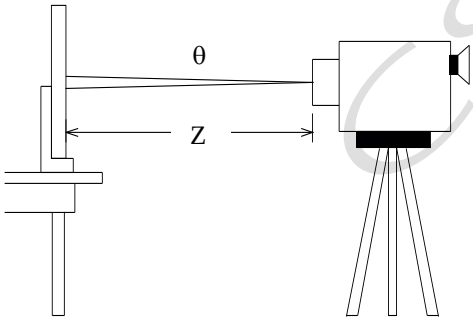


Fig. 7.1The standard set-up system of measurement

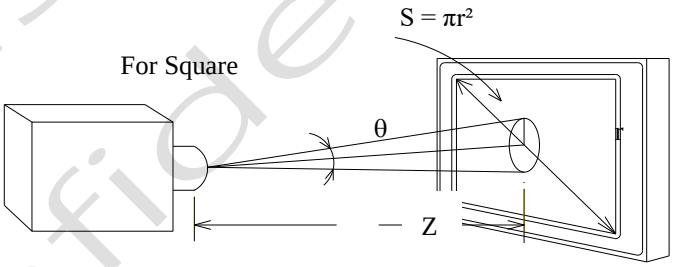


Fig. 7.2The area S contains at least 500 pixels to be measured

$$N = \frac{S}{A} \geqslant 500\text{pixels}$$

N means the actual number of the pixels in the area S.

7.2 Optical Specifications

The table below of optical characteristics is measured by MINOLTA CS2000,MINOLTA CA310,ELDIM OPTIScope-SAand ELDIM EZContrast in dark room.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Static Contrast Ratio		CR	θ_H=0°, θ_V=0° Normal direction at center point CSOT's module	5250	7000	-	-	(1)(2)
Response Time		T_L		-	6.5	12	ms	(3)OPTIScope-SA
Center Transmittance		T%		4.64%	5.15%			(2) (4)
Crosstalk		CT		-	-	4%	-	(2) (5)
Color Chromaticity (CIE1931)	Red	R_X		Typ. -0.03	0.646	Typ. +0.03	-	(2) (6)
		R_Y			0.335		-	
	Green	G_X			0.309		-	
		G_Y			0.615		-	
	Blue	B_X			0.153		-	
		B_Y			0.057		-	
	White	W_X			0.273		-	
		W_Y			0.281		-	
	Color Gamut	CG		68	72	-	% NTSC	(2) (6)
Viewing Angle	Horizontal	θ_{H+}	CR≥ 10	-	89	-	Deg.	(7)
		θ_{H-}		-	89	-		
	Vertical	θ_{V+}		-	89	-		
		θ_{V-}		-	89	-		

Note:

(1)Definition of static contrast ratio (CR):

It's necessary to switch off all the dynamic and dimming function when measuring the static contrast ratio.

$$\text{Static Contrast Ratio (CR)} = \frac{\text{CR-W}}{\text{CR-D}}$$

CR-W is the luminance measured by LMD (light-measuring device)at the center point of the LCD module with full-screen displaying white. The standard setup of measurement is illustrated in Fig. 7.3; CR-D is the luminance measured by LMD at the center point of the LCD module with full-screen displaying black.

(2) The LMD in the item could be a spectroradiometer such as (KONICA MINOLTA) CS2000, CS1000,(TOPCON) SR-UL2 or the same level spectroradiometer. Other display color analyzer (KONICA MINOLTA) CA210, CA310 or (TOPCON) BM-7 could be involved after being calibrated with a spectroradiometer on each stage of a product.

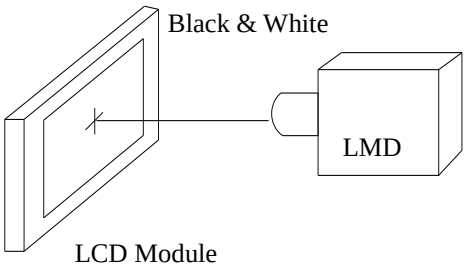


Fig. 7.3 The standard setup of CR measurement

(3) Response time T_L is defined as the average transition time in the response time matrix. The table below is the response time matrix in which each element $t_{X\ to\ Y}$ is the transition time from gray level X to Y. X and Yare two different gray level among0%,25%,50%,75%, and 100% gray level. The transition time $t_{X\ to\ Y}$ is defined as the time taken from 10% to 90% of the luminance difference between X and Y (X<Y) as illustrated in Fig7.4. When X>Y, the definition of $t_{X\ to\ Y}$ is the time taken from 90% to 10% of the luminance difference between X and Y. The response time is optimized on refresh rate F_R=120Hz.

Measured Transition Time		luminance ratio of Previous Frame				
		0%	25%	50%	75%	100%
luminance ratio of Current Frame	0%		$t_{25\%\ to\ 0\%}$	$t_{50\%\ to\ 0\%}$	$t_{75\%\ to\ 0\%}$	$t_{100\%\ to\ 0\%}$
	25%	$t_{0\%\ to\ 25\%}$		$t_{50\%\ to\ 25\%}$	$t_{75\%\ to\ 25\%}$	$t_{100\%\ to\ 25\%}$
	50%	$t_{0\%\ to\ 50\%}$	$t_{25\%\ to\ 50\%}$		$t_{75\%\ to\ 50\%}$	$t_{100\%\ to\ 50\%}$
	75%	$t_{0\%\ to\ 75\%}$	$t_{25\%\ to\ 75\%}$	$t_{50\%\ to\ 75\%}$		$t_{100\%\ to\ 75\%}$
	100%	$t_{0\%\ to\ 100\%}$	$t_{25\%\ to\ 100\%}$	$t_{50\%\ to\ 100\%}$	$t_{75\%\ to\ 100\%}$	

$t_{X\ to\ Y}$ means the transition time from gray level X to Y.

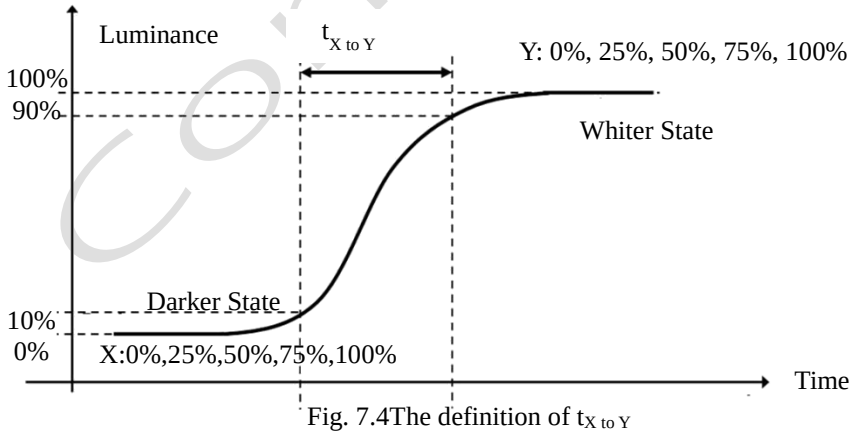


Fig. 7.4The definition of $t_{X\ to\ Y}$

All the transition time is measured at the center point of the LCD module by ELDIM OPTI Scope-SA.

(4) Definition of center Transmittance (T %):

The transmittance is measured with full white pattern (Gray 255)

$$\text{Transmittance(T\%)} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backlight}}$$

(5) Definition of the crosstalk:

$$\text{CT-2D} = \frac{|Y_B - Y_A|}{YA} \times 100\ (\%)$$

YA = Luminance of measured location without gray level 255pattern (cd/m^2)

YB = Luminance of measured location with gray level 255 pattern (cd/m^2)

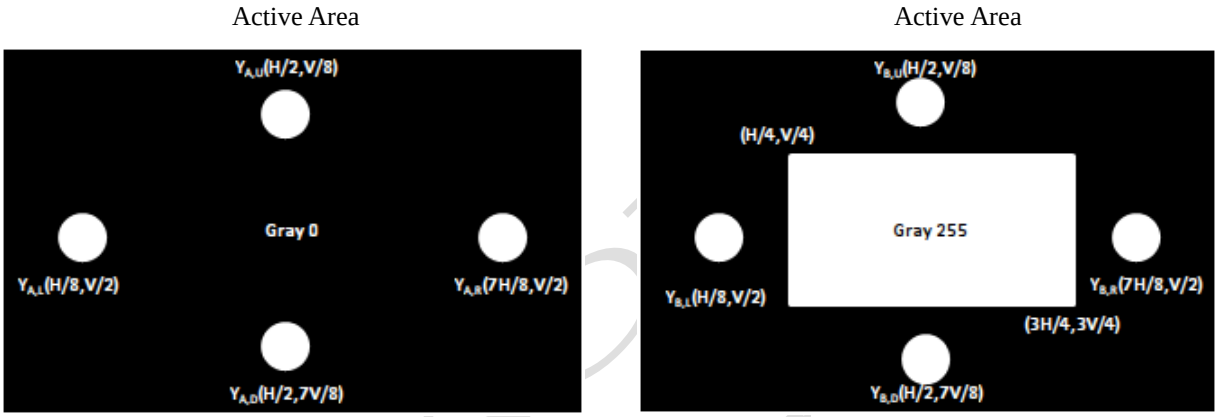


Fig. 7.5 The definition of crosstalk

(6) Definition of color chromaticity:

Each chromaticity coordinates (x, y) are measured in CIE1931 color space when full-screen displaying primary color R, G, B and white. The color gamut is defined as the fraction in percent of the area of the triangle bounded by R, G, B coordinates and the area is defined by NTSC 1953 color standard in the CIE color space. Chromaticity coordinates are measured by CS2000 and the standard setup of measurement is shown in Fig. 7.6.

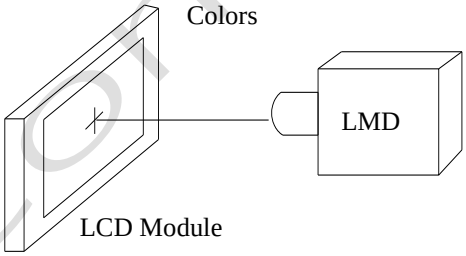


Fig. 7.6 The standard setup of color chromaticity measurement

(7)Definition of viewing angle coordinate system (θ_H,θ_V):

The contrast ratio is measured at the center point of the LCD module. The viewing angles are defined at the angle that the contrast ratio is larger than 10 at four directions relative to the perpendicular direction of the LCD module(two vertical angles:up θ_{V+} and downθ_{V-}; and two horizontal angles:right θ_{H+} and leftθ_{H-}) as illustrated in Fig. 7.7. The contrast ratio is measured by ELDIM EZ Contrast.

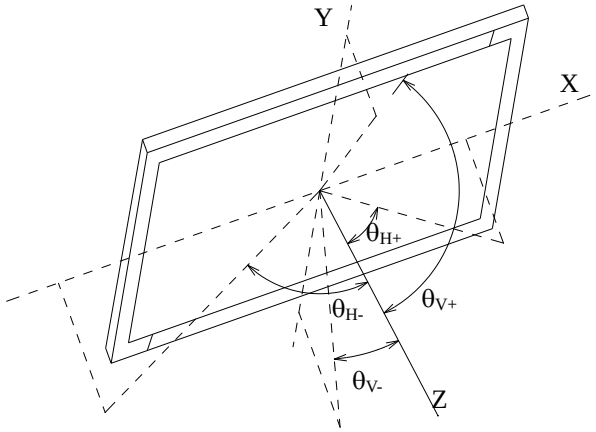
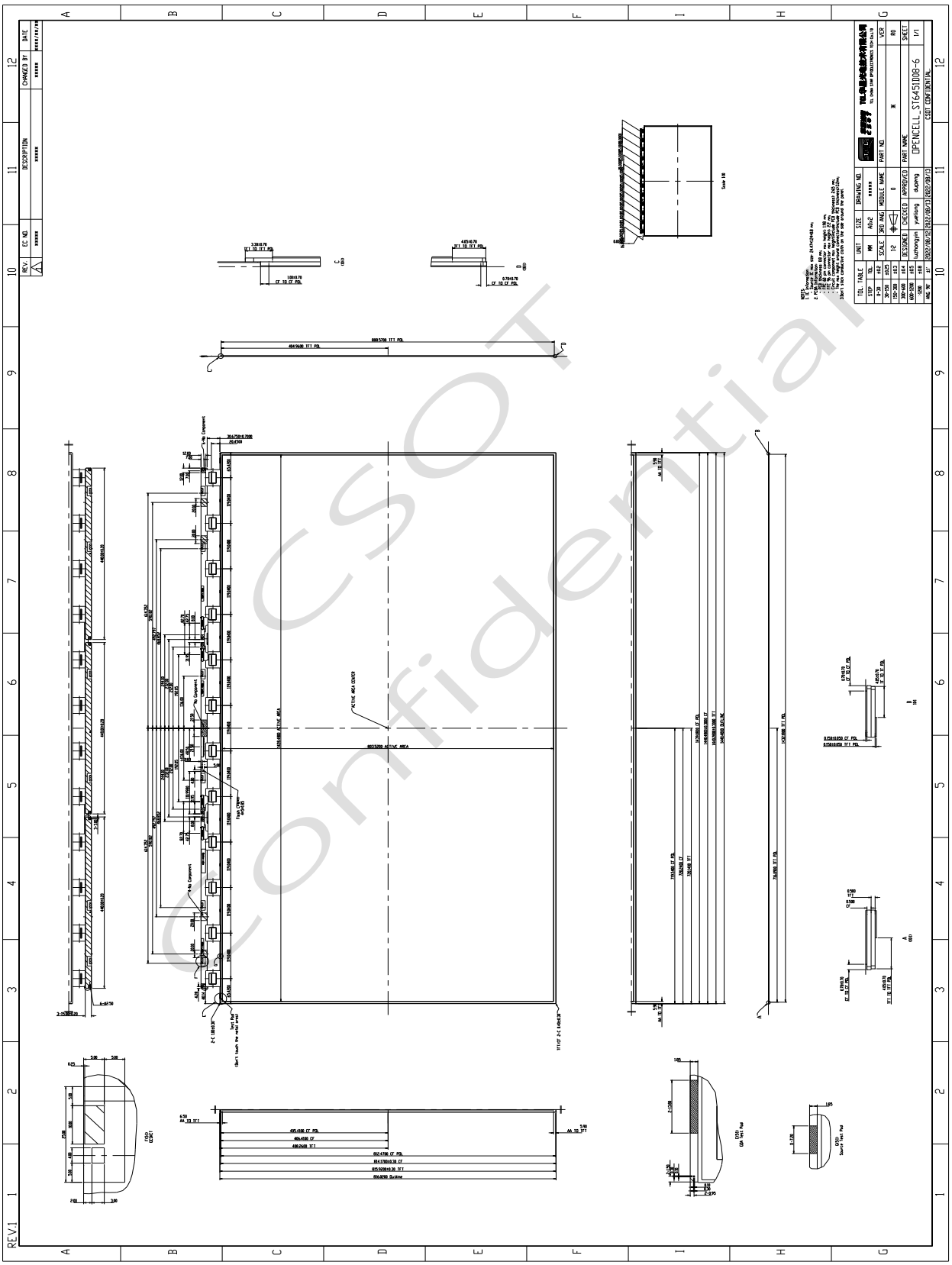


Fig. 7.7Viewing angle coordination system

8. Mechanical Characteristics

8.1 Mechanical Specification

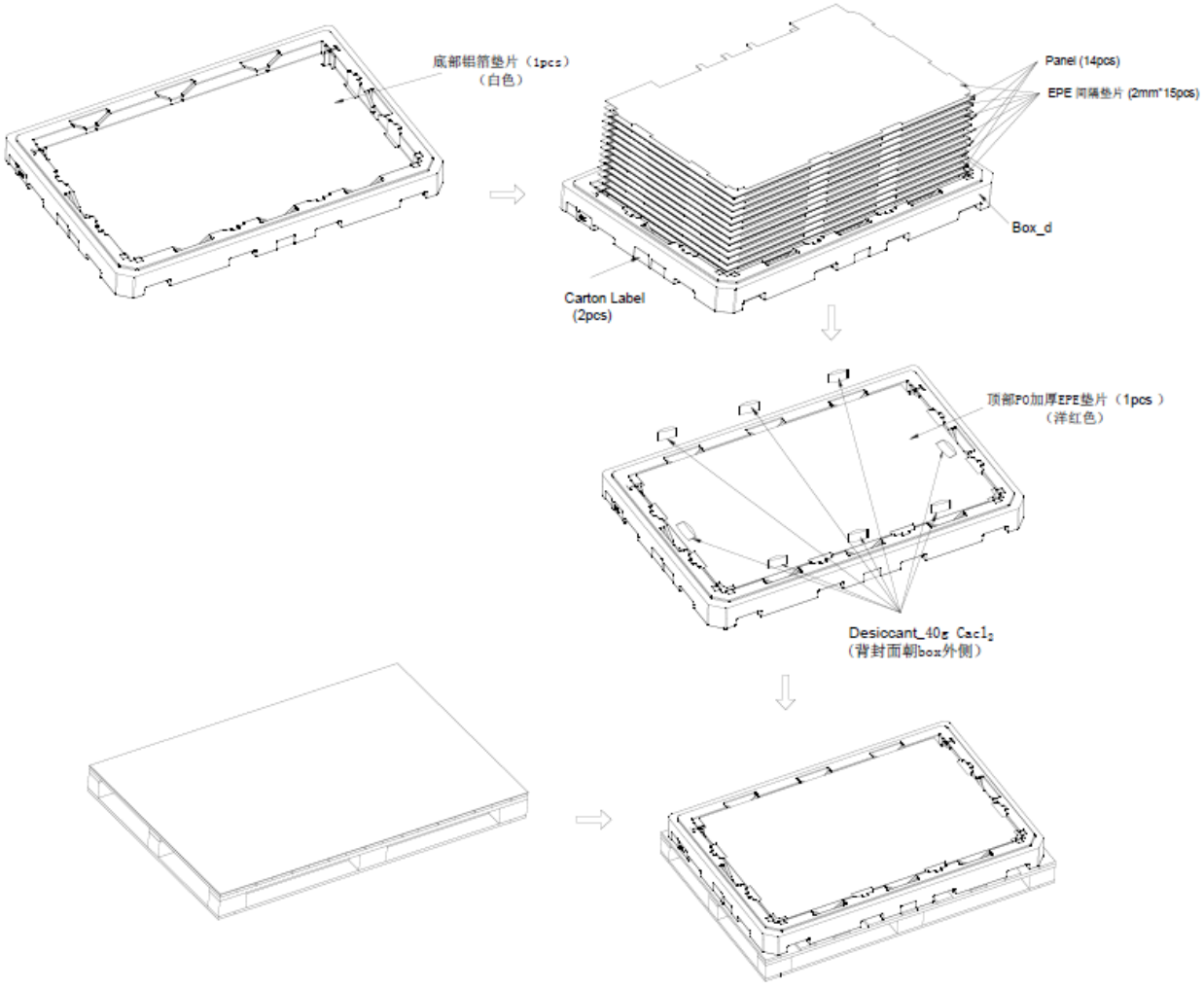


8.2 Packing

8.2.1 Packing Specifications

Item	Specification		
	Quantity	Dimension (mm)	Weight (kg)
Packing Box	14pcs/box	1650.00(L) x 1100.00(W) x136.50 (H)	Gross Weight: 59.8
Stack Layer	8		
Boxes per Pallet	8		
Pallet after Packing	112pcs/pallet	1700.00 (L) x 1130.00 (W) x 1197.00(H)	Gross Weight: 500.1
Pallet Stack Layer	2 layers/Warehouse, 2 layer/40HQ.		

8.2.2 Packing Method



9. Definition of Labels

9.1Open Cell Label

XXXXXXXXXXXXXXXXXXXXXXXXST6451D08-6 Ver. X.X

- Model Version Code
- Model Name
- Week Code
- Serial Number

Serial Number: XXXXXXXXXXXXXXXXXXX

- CSOT Internal Use
- Panel ID

Week Code: XXXX

- Week
- Year

Year: 2010 =10, 2011 = 11 …2020= 20, 2021= 21…

Week: 01, 02, 03 …

Model Name: ST6451D08-6

Ver.X.X: Version, for example: 0.1, 0.2, … , 1.1, 1.2, …, 2.1, 2.2, …

9.2 Carton Label

For RoHS compliant products, CSOT will add RoHS for identification.

Serial Number: XXXXXXXXXXXXXXXXXXX

- CSOT Internal Use
- Year, Month, Date
- Model Version Code
- CSOT Internal Use

Manufactured Date:

Year: 2010 =10, 2011 = 11…2020= 20, 2021= 21…

Month: 1~9, A~C, for Jan. ~ Dec.

Date: 01~31, for 1st to 31st

Model Version Code: Version of product, for example: 01, 02, 11, 12…

9.3 Pallet Label

Model Name: ST6451D08-6

Serial Number: XXXXXXXXXXXXXXXXXX

- CSOT Internal Use
- Year, Month, Date
- Model Version Code
- CSOT Internal Use

10. Precautions

10.1 Assembly and Handling Precautions

(1) The device listed in the product specification sheets was designed and manufactured for TV application only.

(2) Do not apply rough force such as bending or twisting to the open cell during assembly.

(3) It is recommended to assemble or install a open cell into the user's system in clean working areas. The dust and oil may cause electrical shorter damage the polarizer.

(4) Any attachment on polarizer of open-cell，such as tape，is forbidden and not recommend，especially under the high temperature and high humidity environment.

(5) Do not apply pressure or impulse to the open cell to prevent the damage to the open cell.

(6) Always follow the correct power-on sequence. This can prevent the damage and latch-up to the LSI chips.

(7) Do not plug in or pull out the interface connector while the open cell is in operation.

(8) Use soft dry cloth without chemicals for cleaning because the surface of polarizer is very soft and easily be scratched.

(9) Moisture can easily penetrate into the open cell and may cause the damage during operation.

(10) High temperature or humidity may deteriorate the performance of the open cell. Please store open cell in the specified storage conditions.

(11) When ambient temperature is lower than 10℃, the display quality might be deteriorated. For example, the response time will become slow.

(12) POL Protective film peeling Precautions：peeling from source side to the opposite; peeling speed：≤30m/min

10.2 Safety Precautions

(1) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(2) After the open cell end of life, it is not harmful in case of normal operation and storage.

(3) Any attachment on polarizer of open-cell，such as tape，is forbidden and not recommend，especially under the high temperature and high humidity environment.

Appendix I- VGH temperature compensation function suggestion

When switching to DLG240Hz，VGH temperature compensation function was suggested. The relationship between VGH voltage and temperature is as below.

Temperature	NCT voltage	VGH voltage
Above 5℃	1.6V	30.5V
Between -3℃ to 5℃	Varies linearly between 1.6V and 1.8V	Varies linearly between 30.5V and 36.5V
Below -3℃	1.8V	36.5V

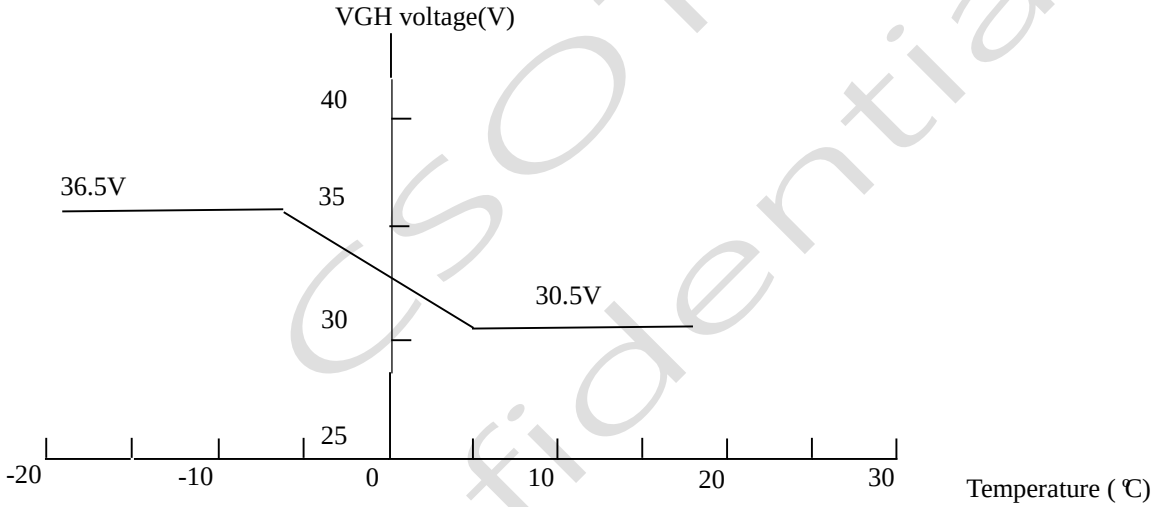


Fig. I.1 relationship between VGH voltage and temperature