Grupo: Los futuros jalados
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Cycle	reset	PC	Instr	SrcA	SrcB	Branch	ALUResult	ALUFlags[NZCV]	CondEx	WriteData	MemWrite	ReadData
1	1	00	SUB R0, R15, R15 (E04F000F)	8	0	0	0	?	1	8	0	X
2	0	04	ADD R2, R0, #5 (E2802005)	0	0	0	5	?	1	X	0	X
3	0	08	ADD R3, R0, #12 (E280300C)	0	C	0	C	?	1	X	0	X
4	0	0C	SUB R7, R3, #9 (E2437009)	C	9	0	3	?	1	X	0	X
5	0	10	ORR R4, R7,	3	5	0	7	0	1	5	0	X

			R2 (E1874 002)									
6	0	14	AND R5, R3, R4 (E0035 004)	C	7	0	4	0	1	7	0	X
7	0	18	ADD R5, R5, R4 (E0855 004)	4	7	0	B	?	1	7	0	X
8	0	1C	SUBS R8, R5, R7 (E0558 007)	B	3	0	8	?	1	3	0	X
9	0	20	BEQ END (0A000 00C)	28	30	1	58	?	0	0	0	X
10	0	24	SUBS R8, R3, R4 (E0538 004)	C	7	0	5	?	1	7	0	X
11	0	28	BGE AROU ND (AA000 000)	30	0	1	30	?	1	0	0	X

12	0	2C	ADD R5, R0, #0 (E2805000)									
13	0	30	AROUND SUBS R8, R7, R2 (E0578002)	3	5	0	FFFFFFFE	?	1	5	0	X
14	0	34	ADDLT R7, R5, #1 (B2857001)	B	1	0	C	?	1	X	0	X
15	0	38	SUB R7, R7, R2 (E0477002)	C	5	0	7	?	1	5	0	X
16	0	3C	STR R7, [R3, #84] (E5837054)	C	54	0	60	?	1	7	1	X
17	0	40	LDR R2, [R0, #96] (E5902060)	0	60	0	60	?	1	0	0	7

19	0	44	ADD R15, R15, R0 (E08FF000)	4C	0	0	4C	?	1	0	0	X
19	0	48	ADD R2, R0, #14 (E280200E)					?				
20	0	4C	B END (EA000001)	54	4	1	58	?	1	X	0	X
21	0	50	ADD R2, R0, #13 (E280200D)					?				
22	0	54	ADD R2, R0, #10 (E280200A)					?				
23	0	58	END STR R2, [R0, #100] (E5802064)	0	64	0	64	?	1	7	1	X

2. An image of the simulation waveforms showing correct operation of the processor. Does it write the
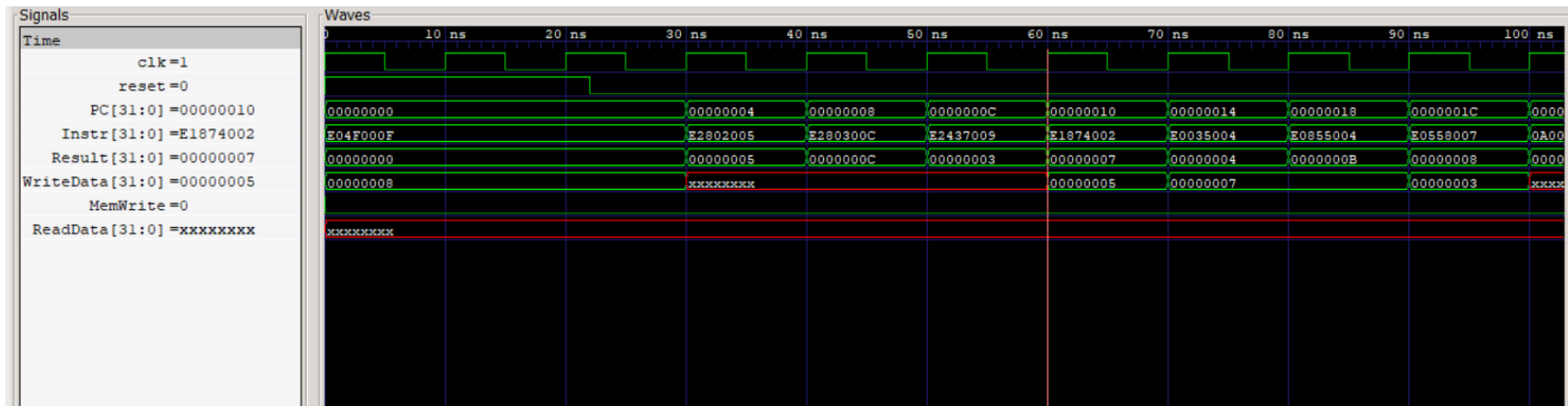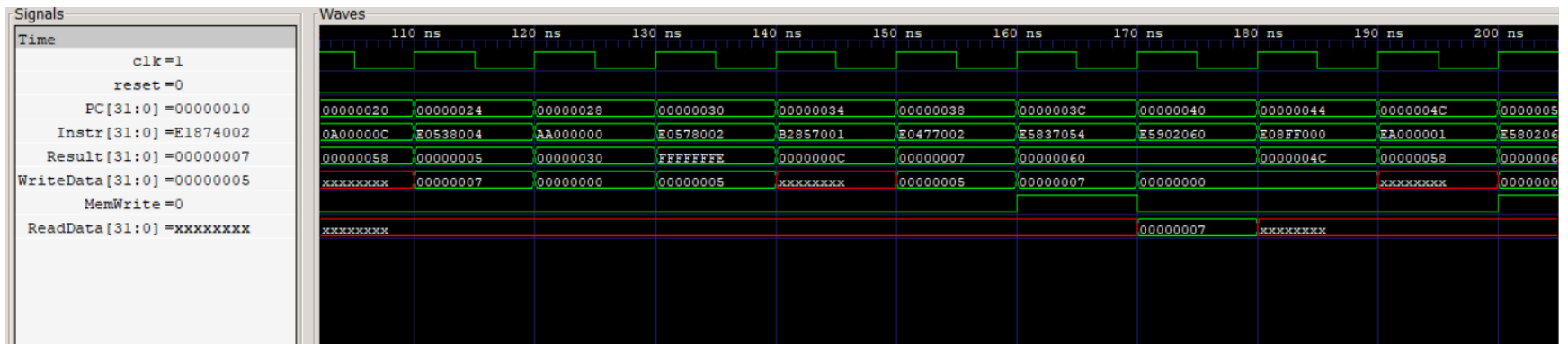
correct value to address 100?

Sí escribe los valores correctos, en la última instrucción se cumple:

```
58 END        STR R2, [R0, #100] ; mem[100] = 7
```

Lo cual está escrito en el libro. Para comprobar que el resultado es el correcto, mostraremos las siguientes capturas de pantalla del waveform a través de IcariusVerilog y GTKwave.

Simulation considering only the 8 signals

Vemos que el resultado final es el correcto.