Manual

for CCD - line scan camera system FL30xx

series FL3001 is for slow speed systems with 1 MHz pixel clock
series FL3010 is for mid speed systems with 10 MHz pixel clock
series FL3030 is for high speed systems with 30 MHz pixel clock
series FLC is a fiber link camera
series FLCC is a fiber link camera with camera control unit
series FLPC is a fiber link camera with peltier cooling
series FLIO is a fiber link input and output control unit

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Berlin, den 17.1.2017

Gerhard Stresing

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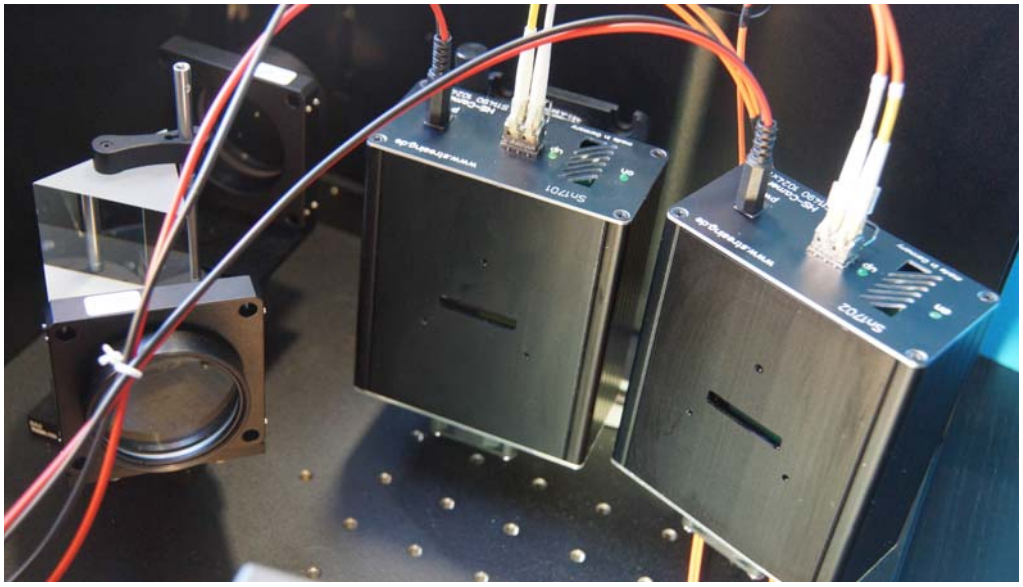
1 Introduction

Our cameras are delivered with 1024 pixel (pixel = “picture elements”) sensors. The pixel are **set up in one line** and so you get a one-dimensional optical multi channel detector. The optic signal can be coupled directly or focused with a lens to the sensor.

The series FL3000 cameras use a fiber link interface with standard components available for ethernet connections, but do not use an ethernet protocol. Here a data speed of 2.5Gbit/s is achievable where the effective data rate is up to 250 Mbyte/s. This interface is used to connect the camera with our PCIE board type Gen1 with 1 lane (simplest version) where here this data rate limits the camera speed to 200kHz line rate. In fact additional delays in software, DMA controller and operating system limits the speed of our camera to about 55kHz for two 1024 pixel sensors running parallel.

picture-1.1: Our Double line prism spectrometer kit



1.1 Camera Series 3000

We can offer 3 camera families with different speed / noise performance:
Table 1.1: Camera family parameters

series	AD res	trms [counts]	DR	max. lr line rate	
3001	16 (65k)	< 6	> 10000:1	2 kHz	
3010	16 (65k)	< 13	> 5000:1	8 kHz	
3030	14 (16k)	< 6	> 3000:1	50 kHz	

for more camera infos see:
series 3001 chapter-3.1, series 3010 chapter-3.2, series 3030 chapter-3.3

1.2 Double Line (DL) Function

All cameras and the Camera Control can be used with 2 parallel working A/D converter using the same clock. Here 2 sensors can be sampled absolutely parallel in high speed. So an easy way of simultaneous reading is accomplished, where the signals can be further calculated afterwards (i.e.: divided for I/I0 measurements). The sensors can be located close together behind one spectrometer (if they have a small case that they fit there) or they can be located behind 2 separated spectrometers (if their case is too big). For most spectrometers the vertical distance between the 2 spectra may not be more then 14mm.

1.2.1 Double Line Board

The 2 sensors can be located on one double line sensor board as shown in picture-1.2 mounted behind one spectrometer (only the PDAs are small enough for that option). Advantage: both rays use the same optical components.

picture-1.2: Double Line sensor board

Only big spectrometers with flat field function can be used with the 2 sensors on one board function:

picture-1.3: Setup with one Spectrometer

1.2.2 Two separated Single Line Boards

It is also possible to mount 2 single line sensor boards (picture-1.4) behind 2 separated spectrometers, if the case of the sensor is too big to place them beneath each other.

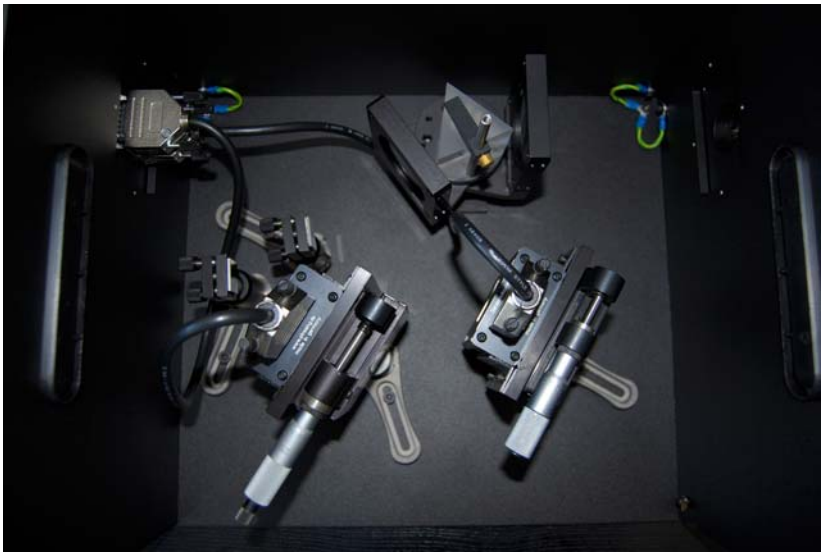
picture-1.4: Single Line Sensor Board

picture-1.5: Setup with two sensor heads FLCC

Here two sensor heads are shown. They can be used with one CamControl. If cooled cameras are needed, the CamControl cannot be used. Here only two separate cooled cameras can be used.

We offer a prism spectrometer kit for a 2 beam system with separated sensor heads.

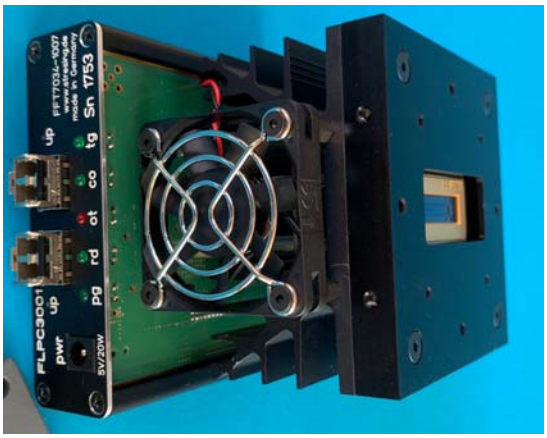
picture-1.6: Prism spectrometer with 2 single line sensor boards.



Here two laser beams are sent trough one prism (higher beam and lower beam with 20mm distance). The signals are reflected to 2 different sensor boards.

This system can also be used if 2 cooled camera systems are needed.

picture-1.7: Cooled camera FLPC3001



1.3 Sensors

The sensor reacts similar to a chemical film: the light is integrated in the sensor cells, until the read out sequence is started. The exposure time is determined by the distance between two reads and as a result the sensitivity can be increased by raising that interval.
The simplest way to use the camera is a continuous read of the line with a constant repetition rate. Here it is important to pay attention to a constant frequency, considering that the oscillation of the read-out frequency leads to an immediate oscillation of the signal.

The increasing of the sensitivity is restricted by darkness noise and read-out time of the registers.
For bright light condition a short exposure time has to be chosen. Since the deleting of the storage cells is only possible by a read of the complete line, the shortest exposure time is determined by the read sequence of one entire line.
An overexposured signal can be dimmed only with optical filters, whereby such a signal does not lead to the destruction of the sensor - unless you evaporate the chip!

For low light levels you should choose a long exposure time. According to the sensor the thermal darkness noise reaches saturation after about 5 to 50 seconds at room temperature. A cooling to -20 °C can reduce this noise about 100-1000 times.

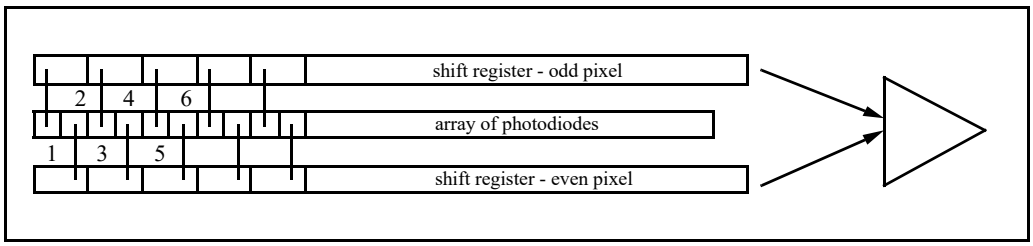
There are three main classes of sensors available:

Table 1.2: Sensor types

	Advantage	Disadvantage
CCD- sensor	price tiny pixel size	asymmetrical even/odd pixel
PDA (photo diode sensor)	good dynamic range uv-sensitive anti blooming not asymmetrical	expensive read-out at different times
FFT-sensor (full frame transfer) also called TDI (time delayed integration)	30..100 times more sensitive	expensive read-out at different times not uv-sensitive no anti blooming

a) CCD line-scan sensor (manufactured by Th, So, HA S11490)
These 'charged coupled devices' (CCD's), suit especially for opto electronic picture sensors. Picture sensors of this kind contain a sensor area assembled with photo diodes, as well as two (S11490: one) parallel CCD-shift registers. The registers consist of side by side lying storage cells (MOS-capacitors), which can store charges through connecting to an outer voltage. Through the linkage of the individual storage cells a CCD-shift register is formed, which transports the electrons with several clocks to the output amplifier. There is one register for the even and one for the odd storage cells:

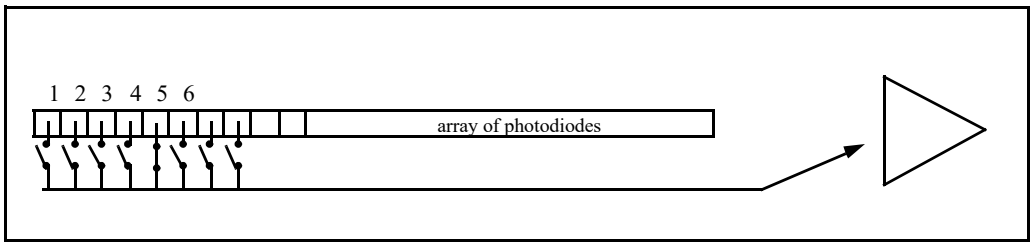
picture-1.8: CCD-sensor



After the start signal all electrons collected in the photo diode area are simultaneously submitted to the shift-registers. They were transported afterwards serial to the output. There they are translated into a voltage signal and yield to a video-signal corresponding to the exposure of the cell.
Between two read-out sequences, as well as during the transport through the shift registers, the newly arriving photons will already be integrated in the photo diode area.

b) Videoline-sensor (manufactured by Hamamatsu only applicable in series 2000)
This sensor type contains no CCD-shift registers. Instead there are switches implemented, whicsh connects respectively one photo diode after the other to the output amplifier.

picture-1.9: Videoline-sensor



After the start signal the switch control is reseted and the diodes are connected successively to the output amplifier. Light which falls on the diodes during read-out is determined at different times, depending on the pixel number.

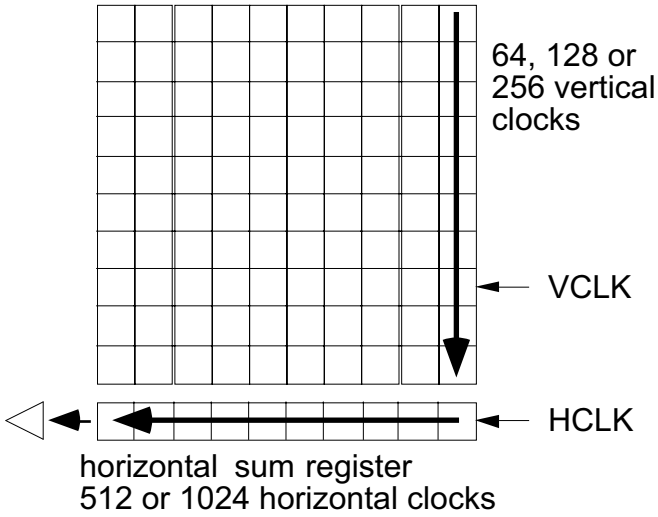
c) FFT-CCD-Array sensor (manufactured by Ha, Dalsa only series 2000)
This array sensor is operated like a line sensors. Because of its construction the sensor reaches a higher sensitivity as standard sensors. ‘FFT’ stands for ‘full frame transfer’ (is also designated TDI).
The FFT sensor has no extra memory on the chip and therefore the entire space is filled with photosensitive cells (100% fill factor).

Also available are Interline arrays, with several standard lines on the chip, that means a complete shift register beside each line. These sensors obtain gaps between the sensor cells (fill factor 10-90%) but they can store the complete picture at a giv-

en trigger.

Like the video line sensors, the FFT's are read out at different points of time. This vertical clock phase is about 64/ 128/ 256 x 10 µs = 0.64/ 1.28/ 2.56 ms long and starts directly after triggering.

picture-1.10: FFT-sensors



First all vertical pixels are transported to the sum register and are added there. The horizontal register is read afterwards like a line sensor. This operation mode is called 'binning mode'. The improvement of the noise reduction is $\sqrt{64}$, 128 or 256. The resolution of the following analog/ digital converter is now limited only through the read-out noise.

Since these sensors use the pixel cells for storing and transferring of the data they need no extra registers on the chip. The advantage is a 100% fill factor, but the disadvantage is a need for a mechanical shutter for cw signals. Otherwise the transferred data is smeared vertically with the new accumulated light data.
For pulsed signals (< data read time) the sensor can be used without a shutter.

Like the video line sensors, the temperature dependent dark noise of FFT sensors can be reduced with a cooler up to 1000 times. At high line rates like 1kHz, the dark noise effect can be neglected as the main factor here is the read noise. Only at rep. rates below 100Hz a cooling has a benefit.

2 Operation with computer

2.1 Before starting

The cameras are delivered presetted and there are no further adjustments necessary.
The power supply of the camera has to be connected to the power connector.

!Before installation of the interface board you have to remove the SFP modules. Otherwise the interface-board does not fit in the slot**! (see picture-2.1)**

Please read chapter-2.3 before starting.

2.2 Interface board

For the PC we offer a PCIE- interface board with additional connectors for external trigger input and output.

picture-2.1: PCIE interface

PCIE board with removed SFP module

The standard SFP modules can be used for distances up to 100m.

The SMB connections are:

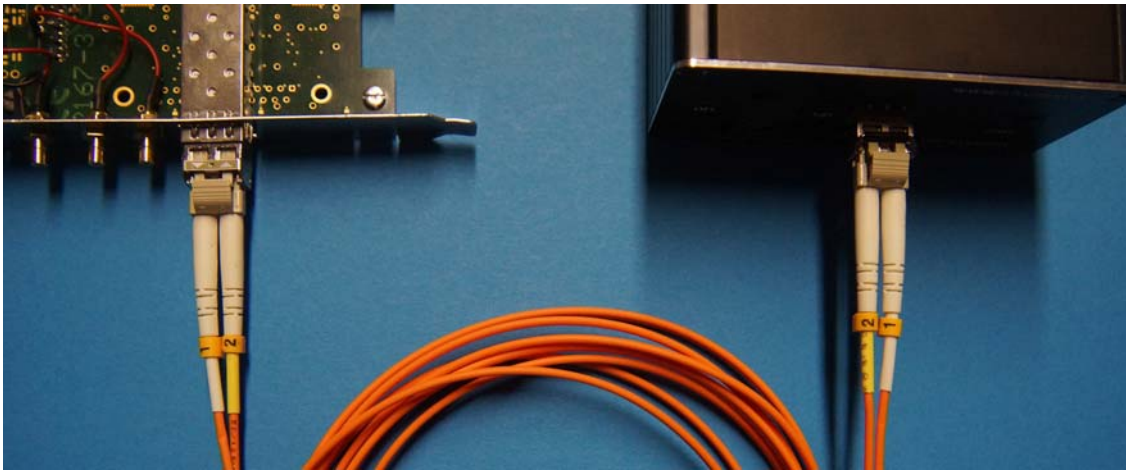
S1: Shutter (Chopper) Input1 or additional trigger input
S2: Shutter (Chopper) Input2 or additional trigger input
I: External Trigger Input
O: Trigger Output

The max. trigger rate for I is 1 MHz.
The max. trigger rate for S1 and S2 is 300kHz.

deeper infos at chapter-6.1

2.3 Connections and Indicators

picture-2.2: Wiring with computer



be sure to cross over the fiber cables as seen in picture-2.2. One side is for sending, the other for receiving. So a sender must connect to a receiver and not to another sender.

Setup
Switch on by connecting the pwr plug with the external power supply.
Now the **on** LED (front side) should be lightened and the **up** LED should indicate that the fiber link has synchronized.
The camera is ready now and the software can be started.

2.4 Error Indicators

up LED is not on
If the green up LED is not on, please unplug the fiber link by pushing the two LC levers. Remove the plug, wait a second and plug it in again. The two fibers should insert with a click. Now the interface should have got a reset and the LED should turn on. If not, please try again or try to swap or turn over the cables.

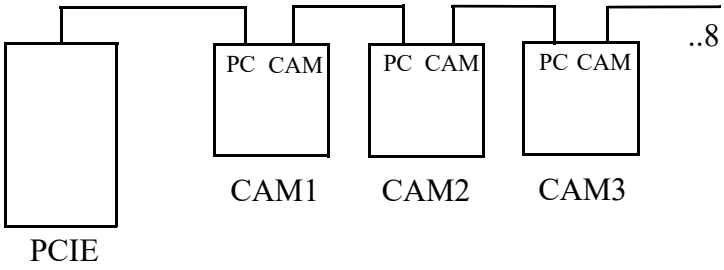
ot LED
The red ot LED (rear) indicates that an over temperature state occurred.
As the camera has a fan, this state should not occur and if so it indicates an error. In this case try it again after unplugging and replugging the power. Look if the fan is running. If the problem persists the camera should be send in for maintenance.

2.5 Double/Multiple Line Cameras

2.5.1 Setup for Double Line Function of series FL30xx

The lower speed cameras can be linked in a queue connected to one PCIE interface board. At one end must be the interface board. It is possible to link up to 8 cameras in a line. All cameras are exposed with the same trigger, so that they run exactly parallel (see next chapter). The number of chained cameras must be entered in register R7 (see chapter-6.2.4.8).

picture-2.3: Fiber Link connection for several cameras in a chain



2.5.1.1 Parallel exposure

All cameras in a chain are exposured parallel with one trigger which is inserted in the PCIE boards “I” input. The trigger is send over the fiber link connection. Here a slight delay occurs:

picture-2.4: Read Delay of 4 cameras in a chain

trigger delay with 4 cameras

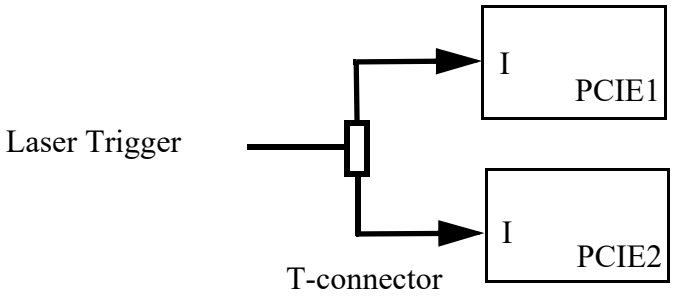
bl: ext. Trigger Input
rd: read starts on PCIE board after 150ns
gn: read start of cam1 after 1.4µs
ye: read start of cam4 after 2.5µs

So be sure to set your laser shot 3 µs before the camera trigger occurs.

2.5.2 Setup for Double Line Function of series FL3030(50kHz line rate)

In case you setup a Double Line System for I/I0 calculations with line rates up to 50kHz, you must use 2 PCIE interface boards to reach the maximum speed of 50 kHz.
The trigger input of both interface boards must be wired together (see picture-2.5) and the software has to be set to external trigger mode:

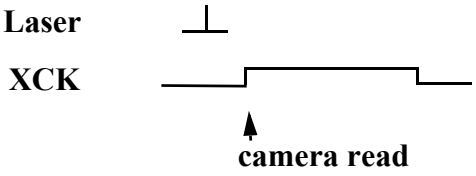
picture-2.5: Double Line trigger connection



only in this case it is guaranteed that both cameras exposure exactly at the same time.

The O connector can be used to monitor the read sequence (XCK) to see if an additional delay is needed. The laser pulse should occur directly before XCK goes high, as here all pixel values are transferred to the output register (see picture-2.6).

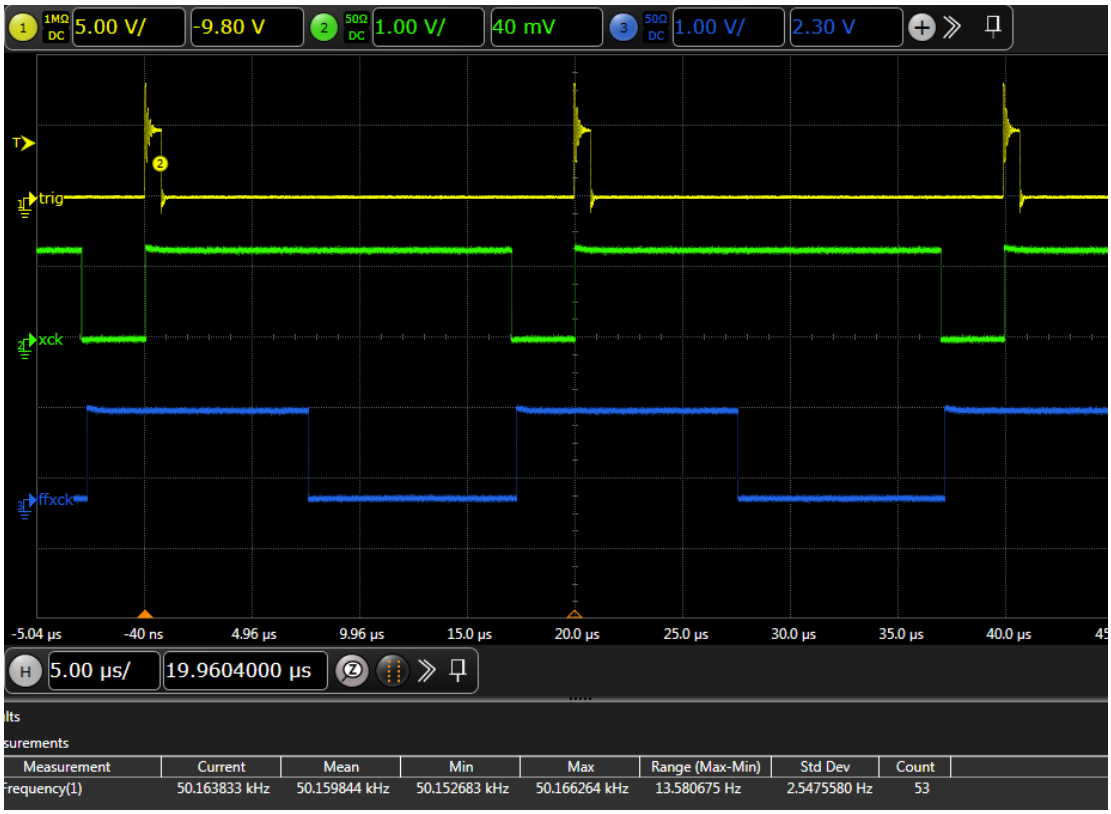
picture-2.6: Laser Trigger and XCK signal



The Laser pulse should not occur during the XCK=high phase.

Be sure not to trigger too fast, or computer could crash!
Always keep the trigger < 51 kHz.

picture-2.7: 50 kHz trigger signals



yellow: external trigger input
green: XCK signal (TrigO set to 0) - is high during the sensor read
blue: FFXCK signal (TrigO set to 4) - is high during PCIE transfer

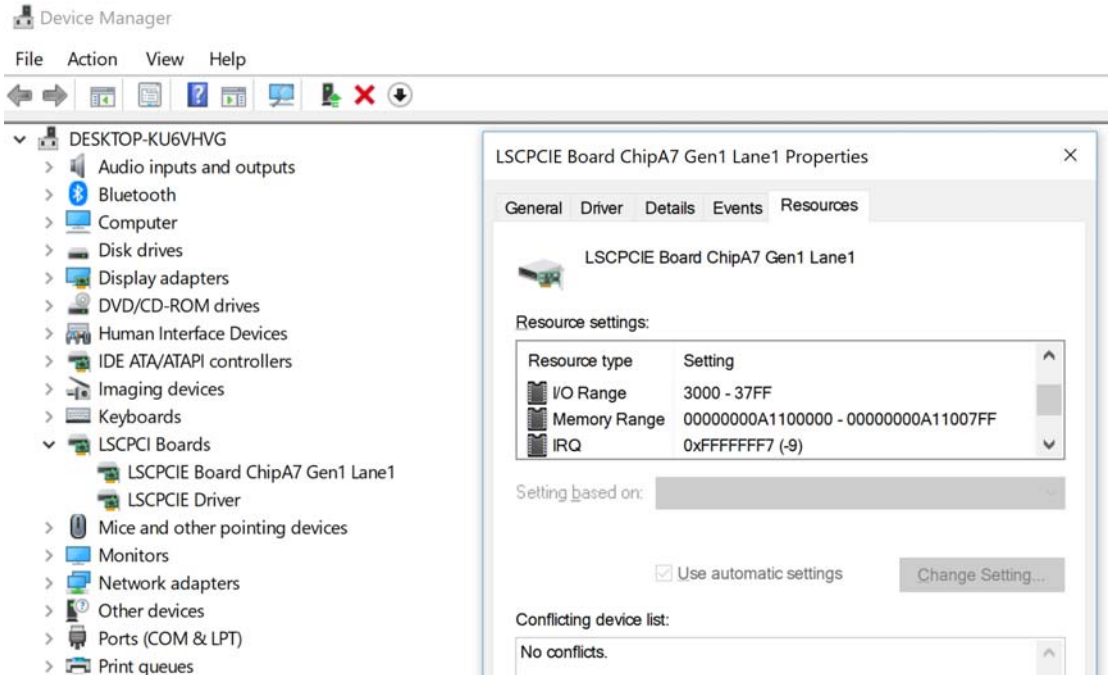
The external trigger starts the sensor read (XCK). When XCK was done, the transfer to the PC is started. To reach the max. line rate, both functions overlap. During the PC transfer, the next sensor read is already running. The sensor read needs 17 µs, the data transfer needs 10 µs. The sensors shutter function is closed at XCK goes high for about 1 µs. The laser should occur at XCK=low.

2.6 Driver install

If you have problems have a look at chapter-2.6.1.
The folder Stresing14.00_Driver_Distribution_Package contains all necessary files. The file: install_run_as_admin.bat mus be executed as administrator (right click on file and choose: run as administrator). Only here all necessary files are copied.

With success the drivers LSCPCIE Board and LSCPCIE Driver can be seen in the device manager:

picture-2.8: installed driver in device manager view



2.6.1 Driver Trouble Shooting

Run the setup batch file like shown in chapter-2.6 before you start Labview. This file is located in the Stresing14.00_Driver_Distribution_Package folder.

If it was not installed as admin, you can get the following errors:

- „Failed to initialize the WDC library...“
- Broken arrows because of the wrong path for the ESLSCDLL
- the labview vi started but nothing happened

possible reasons:
- The wdapi1400.dll was not copied to the system32 folder
- ESLSCDLL.DLL is not located in the bord.vi subfolder
- The debug version of the ESLSCDLL was used -> use the release version (size: 64kB instead of 240kB).

Our DLL is written with visual 2017. You get the source code to adopt own routines.

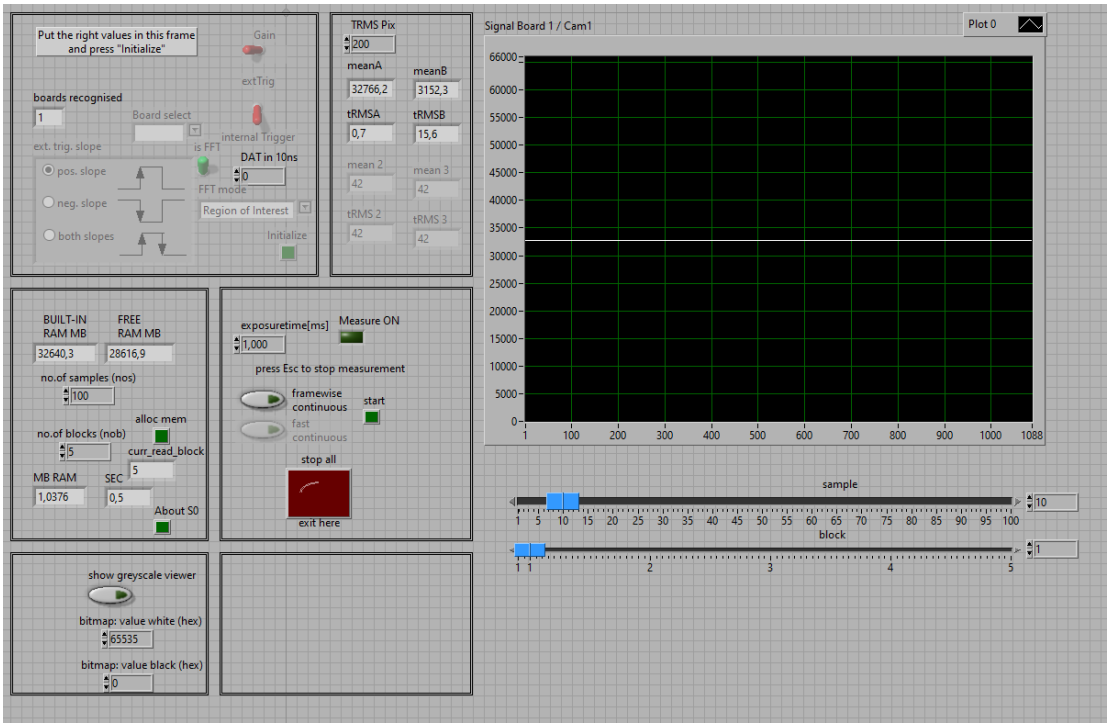
In some cases the resource entry: LSCPCIE Board ChipA7 Gen1 Lane1 is missing. This happens if the board is not recognized.
Some Computers have a special BIOS setup option which could lead to that.
In this case look for an option like: Early PCIe delay. Try to change that option in the BIOS and try again.

In general it is good to know in case of windows problems:
Press the key „shift“ and click restart. Windows is starting now with a blue screen and some options. Choose „Troubleshoot“, in the next screen „Advanced options“, then „Startup Settings“ and then click „Restart“. Now Windows is restarting in a next blue screen with 9 different options.

2.7 First start of Labview example

The labview example is individually setup for every camera system which is delivered. So here all parameters are already set as needed. To test the camera please first power up the camera and start the labview program. Start the FL30XX.vi.

picture-2.9: labview example



Now press the initialize button, then the alloc mem button and then start.
With every start hit he should assemble nobs * nos scans. If you need it to run continuously, hit the framewise continuous button and start again.
In case there is an error, you should hit the stop all button to leave the vi. Then start all over again. In case you need a master reset, you should switch off the camera, on again and start the vi. Please be aware: the initialize function must be called after every switch off. The alloc mem button must be called after changing the nos and nob values.

The standard select for a FFT sensor is full binning.

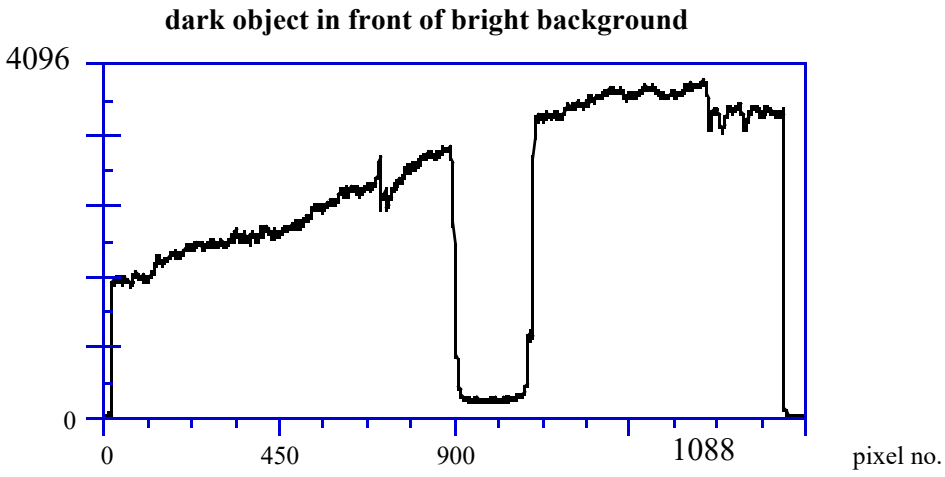
After running with internal timer, you should try the external trigger. This signal must be inserted in SMB plug marked “I” of the PCIE board (see picture-2.1).

2.8 First simple experiments

As first step the following attempts may be made to get familiar with the functions:

1. Darken the camera mounting hole - now all sensor signals should be near zero.
2. If stray light falls on the sensor -all values are 4096 (14 bit).
3. Now darken up only a part of the lens hole with your hand. You should be able to produce a brightness distribution similar to the picture-2.10 (without object in the middle). All function values between 0 and full scale must be achievable.
4. Produce stray light and perhaps change the exposure time to produce a background level at a value of about 4000. Now take an object, i.e. a pen and darken carefully some of the pixels of the sensor. Move the pen over the line. It should emerge a picture similar to picture-2.10, whereby the edges are less steep in this case, because in picture-2.10 a dark object has been scanned with a lens sharply focused.

picture-2.10: Example scan of an object



3 Cameras Series FL3000

Implemented in the camera are some registers to control the camera, the AD converter, the IO_Control and some special features like the DA offset alignment in series FL3030.

The write registers can be set by function:
SendFLCam(uint32 drv,uint8 maddr, uint8 adadr, uint16 data);
SendFLCam.vi

drv: interface board no. = 1
maddr: address of sub device in the camera
= 0 -> camera
= 1 -> AD converter
= 2 -> IO Ctrl
= 3 ->DAC in series FL3030

adadr: address inside the sub device
data: value to be transferred

The read register (only one register) can be read by function:
UINT32 ReadLongS0(drv, *data, port); // ReadL.vi
drv: interface board (=1), data: returned data, port=0
data is 32bit, where the lower word and the upper word are mirrored.
The data contains information about the number of connected cameras. The least significant bit is filled first. Example: 3 cameras are connected -> data = 00000111
The higher byte is filled with the TG signals (TG: temperature good of cooled cameras).
Example: 4 cameras / camera 2 has no TG -> data = 0000110100001111

3.1 Camera series 3001

Here a set of sensors is available, as there are PDAs (photo diode array), FFTs (‚full frame transfer' CCDs) or IR(infra red) sensors.

The possible sensors are (all from Hamamatsu):
FFT S7030-x
PDA S390x or S838x
IR G11608, G920x

3.1.1 Camera registers series 3001

3.1.1.1 Camera Register: Gain Select

maddr=0, adadr = 0;
some sensors have an internal gain select function where a build in capacitor can be switched (IR sensors -> to see the gain factor of the switch have a look at the data sheet of the sensor).
Bit0 = 0 sensor gain is set to standard (SENGAIN)
Bit0 = 1 sensor gain is set to high gain (SENGAIN)

3.1.1.2 Camera Register: PIXEL

The value for PIXEL must be send to the camera at initialization.
The PIXEL register is at maddr=0, adadr = 1;
the default setup for the camera is: SendFLCam(1,0, 1, 1088);

3.1.1.3 Camera Register: Trigger mode (Camera Control (CC) only)

maddr=0, adadr = 2;
CCs have an external trigger input which can be activated here.

Bit210 = 000 CC is triggered internal by XCK
Bit210 = 001 CC is triggered by external trigger input of Cam Control
Bit210 = 010 CC is triggered by external trigger input with CCs DAT function

3.1.1.4 Camera Register: Channel select

maddr=0, adadr = 3;
Bit0 = 1 CHA is enabled
Bit1 = 1 CHB is enabled
double line systems have activated both, single cameras have activated CHA by default.

3.1.1.5 Camera Register: VCLKs active

maddr=0, adadr = 4;
Bit0 = 1 VCLKs is enabled (for FFT and area sensors)

3.1.1.6 Camera Register: LED off (Cameras only)

maddr=0, adadr = 5;
Bit0 = 1 disables the cameras control LEDs for avoiding stray light.

3.1.2 AD Converter register series 3001

maddr=1 has no function
uses the converter ADS8422 (16 bit, 1 channel, 1MHz)
It has no programmable feature.

3.2 Camera series 3010

The sensor S12198 is a CMOS sensor with 10MHz pixel clock which can reach 8kHz line rate.

3.2.1 Camera registers series 3010

3.2.1.1 Camera Register: Gain Select

maddr=0, adadr = 0;
some sensors have an internal gain select function (see data sheet of sensor).
Bit0 = 0 sensor gain is set to standard (SENGAIN)
Bit0 = 1 sensor gain is set to high gain (SENGAIN)

3.2.1.2 Camera Register: PIXEL

The value for PIXEL must be send to the camera at initialization.
The PIXEL register is at maddr=0; adadr = 1;

the default setup for the camera is: SendFLCam(1,0, 1, 1088);

3.2.1.3 Camera Register: Trigger mode (Camera Control (CC) only)

maddr=0, adadr = 2;
CCs have an external trigger input which can be activated here.

Bit210 = 000 CC is triggered internal by XCK
Bit210 = 010 CC is triggered by external trigger input with CCs DAT function

3.2.1.4 Camera Register: Channel select

maddr=0, adadr = 3;
Bit0 = 1 CHA is enabled - is also set by SW1
Bit1 = 1 CHB is enabled - is also set by SW2
double line systems have activated both, single cameras have activated CHA by default.

3.2.1.5 Camera Register: VCLKs active

maddr=0, adadr = 3;
Bit0 = 1 VCLKs is enabled (for FFT and area sensors)

3.2.1.6 Camera Register: LED off (Cameras only)

maddr=0, adadr = 5;
Bit0 = 1 disables the cameras control LEDs for avoiding stray light.

3.2.2 AD Converter register series 3010

maddr=1
uses the converter LTC2271 (16 bit, 2 channel, 10MHz)
the default setup for this converter is:
SendFLCam(1,1, 0, 0x80); // reset
SendFLCam(1,1, 2, 0x1); // set output mode register to 4 lane
Additional filter functions could be activated here. Please refer to the data sheet of this converter for detailed infos.

3.3 Camera series 3030

The sensor Hamamatsu S11490 is a back thinned CCD sensor with high speed, capable to run with up to 50kHz line rate, even in a double line system.
It has 8 channels for parallel read out. The AD converter ADS5294 is a 14bit 8 channel converter with quite some programmable features. Please see data sheet for more details. The gain for each of the 8 channels can be set by software. Other functions are not implemented, but can be added by own programmings. Please see commented source code of the DLL and the sheet of the AD converter in that case.

3.3.1 Camera registers series 3030

3.3.1.1 Camera Register: Gain Select

maddr=0, adadr = 0; (not for S11490, here see chapter-3.3.2.1)
some sensors have an internal gain select function (see data sheet of sensor).
Bit0 = 0 sensor gain is set to standard (SENGAIN)
Bit0 = 1 sensor gain is set to high gain (SENGAIN)

3.3.1.2 Camera Register: PIXEL

The value for PIXEL must be send to the camera at initialization.
The PIXEL register is at maddr=0; adadr = 1;

the default setup for the camera is: SendFLCam(1,0, 1, 1088);

3.3.1.3 Camera Register: Trigger mode (Camera Control (CC) only)

maddr=0, adadr = 2;
CCs have an external trigger input which can be activated here.

Bit210 = 000 CC is triggered internal by XCK
Bit210 = 001 CC is triggered by external trigger input of Cam Control
Bit210 = 010 CC is triggered by external trigger input with CCs DAT function

3.3.1.4 Camera Register: Channel select

maddr=0, adadr = 3;
Bit0 = 1 CHA is enabled - is also set by SW1
Bit1 = 1 CHB is enabled - is also set by SW2
double line systems have activated both, single cameras have activated CHA by default.

3.3.1.5 Camera Register: VCLKs active

maddr=0, adadr = 4;
Bit0 = 1 VCLKs is enabled (for FFT and area sensors)

3.3.1.6 Camera Register: LED off (Cameras only)

maddr=0, adadr = 5;
Bit0 = 1 disables the cameras control LEDs for avoiding stray light.

3.3.2 AD Converter register series 3030

uses the converter ADS5294 (14 bit, 8 channel, 20MHz)
the default setup for this converter is:
SendFLCam(1,1, 0x2A, gain1_4); //set internal gain
SendFLCam(1,1, 0x2B, gain5_8); //set internal gain
Additional filter functions could be activated here. Please refer to the data sheet of this converter for detailed infos.

3.3.2.1 Software Gain for FL3030

The function we have implemented is the SetAdGain(). Here the gain for each of the 8 channels can be set by software in bigger steps. A fine adjust could be achieved with the potentiometers (see chapter-8.4.1) after the software gain was set. The **default value should be set to 5**. You can improve that, but you will increase the noise as well and the zero offset must be readjusted again. Also with a **gain >= 6 , no odd values** are generated. Here the build in amplifier of the AD converter is used. The range is 0..12. Usually here the dynamic range of the AD converter is set to the dynamic range of the sensor (see chapter-8.4.2).

3.3.3 DAC register for series 3030

maddr=3, adadr = 0;
For the HS_Camera series FL3030 an DAC8568 is implemented to adjust the 8 pixel ranges (see chapter-8.4.1). The values can be set by an own call:
SendFLCam_DAC(drv,ctrl,adr,data,feature);

the DAC is used with an external reference. That is the default setup of the converter, so no extra call is necessary. Please refer to the data sheet of this converter for detailed infos.

to set the zero level to value: data, call:
SendFLCam_DAC(1,3,0..7,data,0); data is the offset in 16bit, 0..7 is the range.

3.3.4 Power supply

The camera uses an external power supply with 18V and 11W power consumption. To avoid too much heating, a fan is implemented.

3.4 Cooled Camera FLPC 30xx

The temperature difference, which the Peltier Elements can generate is about 40°C. As the Peltier Elements can only generate a difference to the room temperature, the lowest achievable cold side temperature depends on the temperature of the warm side, that means of the ambient temperature. If the cold side temperature is specified to-20 °C at 20 °C ambient temperature the cooling cannot reach the -20 °C at an ambient temperature of 30°C. In that case the front panel indicator signal tg will never turn on and the regulation cannot reach a stable temperature.
On the other hand a lower ambient temperature can lead to a lower temperature of the sensor (for example with water cooling).

The linearization of the temperature sensor is optimized for the low temperature region (-40 ºC < T< -10 ºC) here a good precision is reached. Measurement errors leads to max. 1 K for temperatures under -10 ºC. In the range from 0 to +20ºC the measurement errors can reach up to 10 K.

3.4.1 Camera registers series FLPC 30xx

The series FLPC stands for peltier cooled camera. Here the sensors can be cooled down to -10 or -40 degrees celcius - depending on sensor type with one or two peltier elements.

3.4.1.1 Camera Write Register: Cooling Level (cooled cameras only)

The cooled cameras have an additional register to set the cooling level.
maddr=0, adadr = 6;

Bit 210 = 000 cooling is off.
Bit 210 = 1-7 cooling level

level = 0 (P10) -> OFF
level = 1 (P11) -> 0ºC
level = 2 (P12) -> -10ºC
level = 3 (P13) -> -20ºC
level = 4 (P14) -> -25ºC
level = 5 (P15) -> -30ºC
level = 6 (P16) -> -40ºC
level = 7 (P17) -> minºC

For the FFT series S7031 min=-15ºC as this is the achievable level with one peltier.
For the IR series G1147x min=-25ºC as this is the achievable level with two peltiers.

3.4.2 Camera Read Register

The read register (only one register) can be read by function:
UINT32 ReadLongS0(drv, *data, port); // ReadL.vi
drv: interface board (=1), data: returned data, port=0
data is 32bit, where the lower word and the upper word are mirrored.
The data contains information about the number of connected cameras. The least significant bit is filled first. Example: 3 cameras are connected -> data = 00000111
The higher byte is filled with the tg signals (tg: temperature good of cooled cameras). Example: 4 cameras / camera 2 has no tg-> data = 0000110100001111.

The value is only updated during the XCK=low phase, means is only valid when the measurement is running.

3.4.3 Power supply

The cooled camera uses an external power supply with 6V and 60W power consumption. When running the max. consumption is about 20W, but at power on a bigger supply is needed. A fan is implemented to distribute the heat.

3.5 Camera Control (CC) FLCC 30xx

3.5.1 Camera registers series FLCC

The Camera Control can be delivered with an option of additional sensor inputs. Here up to 4 voltage or photo diode signals can be inserted in the data stream at the end of the pixel

values of the sensor - as if you have some additional pixels. The values are taken exactly when the spectra was assembled, so that the are absolutely synchronous to the spectra. These signals can be used for energy measurements or delay stage position values.

3.5.1.1 Camera Register: Trigger Select

maddr=0, adadr = 2;
CCs with integrator function have an external trigger input which can be activated here.

Bit210 = 000 CC is triggered internal by XCK
Bit210 = 001 CC is triggered by external trigger input of Cam Control
Bit210 = 010 CC is triggered by external trigger input with CCs DAT function

In fact there are 3 possible trigger modes (see chapter-7.3.6).
the simplest mode is the mode 000 (default). Here the camera read (XCK) starts the integrator and the start of the sensor read is delayed internally by register DLY of the PCIE board. This mode is called DDAT and is explained in chapter-7.3.8

A more precise version is to use the so called ADAT mode - with or without the DAT function (see chapter-7.3.7)
Here the integrator is started by the external trigger input of the CamControl (front side). The trigger starts the INT sequence and the low slope of this INT signal is used to start the camera reads XCK. Therefore the INT plug of the CC must be connected with the 'I' plug of the PCIE board.

The camera control is explained more deeply in chapter-7.

3.6 IO Control (IO) FLIO 30xx

maddr=2, adadr = n;
The IO control has several registers and is explained more deeply in chapter-9.

3.7 Internal switch

The cameras have an internal switch bank. Here some major functions are selected.

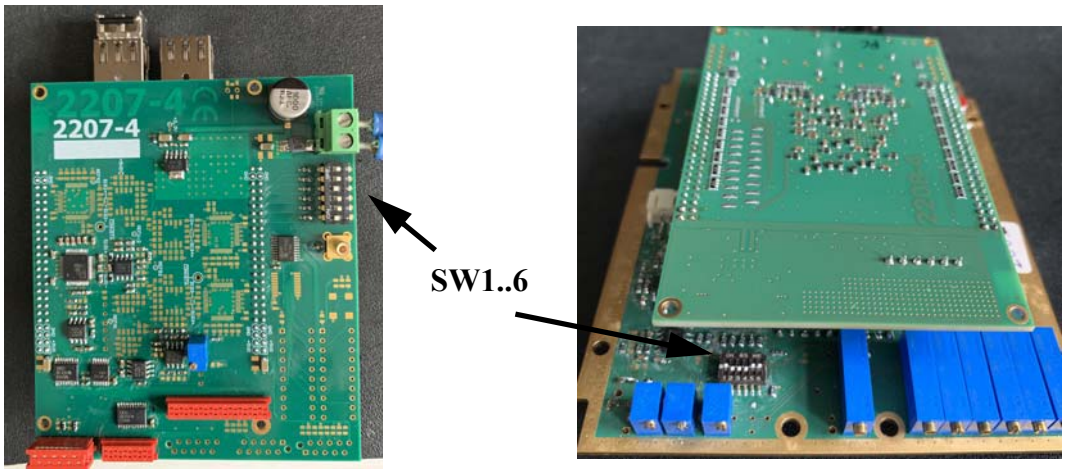
The switch SW has these functios:

SW2	SW1		
0	0	ENA	(default for 1 camera)
0	1	ENA + testramp	
1	0	ENA + ENB	(default for CC with 2 sensors)
1	1	ENA + ENB+ testramp	

SSW4	SW3:
0	0 - PDA
0	1 - IR
1	0 - FFT
1	1 - area

SW5:	IR	on = IR with 256 pixel off = IR with 512pixel
SW6:		on = AD with 3.33MHz off = AD with 2.5MHz (default)

picture-3.1: switch bank



FLCC3000 **FLPC3000**

SW6 can be used to speed up the IR camera.

Table 3.1: Speed up of sensor G11608

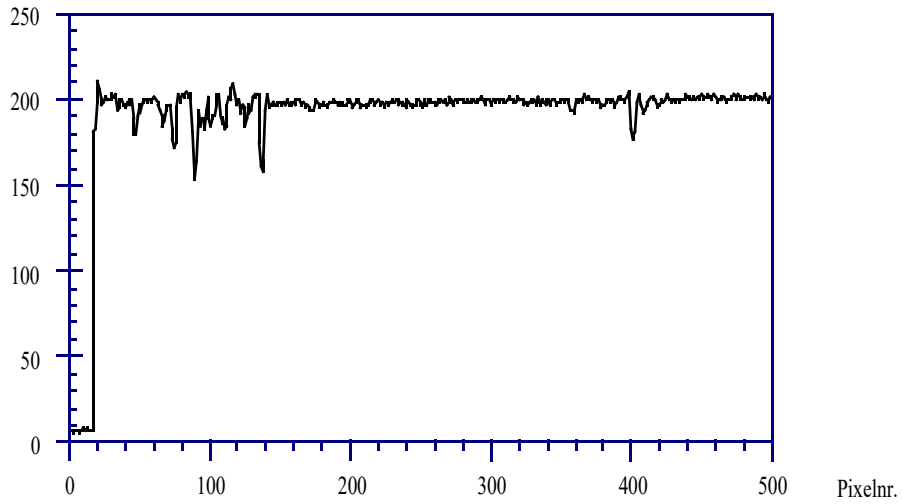
	mlr	noise
SW6=off	8 kHz	<4 cnts
SW6=on	10 kHz	< 8 cnts

4 Special sensor features

4.1 Dust on the window

With a spot light source it is possible to detect a signal caused by modulation structures on the measurement signal, which are caused by dust.

picture-4.1: Modulation caused by dust



These signals do not change their position if the camera is moved.

Because of this the sensor should be cleaned regularly with a special clearance paper.

4.2 Sensors without window

The window appropriate to the protection from dust on the sensor can lead at measurements with monochromatic light to interference phenomena, which falsify the measurements.

Besides the standard windows limit the spectral sensitivity in the UV region, since the standard window of the sensors (BK7) is not transparent underneath 400 nm. According to picture-10.12 the spectral range below 400nm is not available wit the standard sensor, but

- The Ha-sensors can be delivered with a quartz window.
- Also a version without window is available.

To avoid the interference- and UV-problems, some sensors without windows (o.F.), that means with a standard removable window, can be delivered. The window is fastened with a tape. To remove the tape, the cover of the camera should be disassembled.

Two modes of operation are possible:

- You can take off the window and close the cameras M42 mount with the in-

cluded body cap. The sensor is dust protected after each measurement again. For measurements in the lab this is the simplest solution.

- For measurements in harsh dusty industry environment it is advisable instead, to order a sensor with a specialized window, which is firmly positioned. For the interference problem the window can be covered with an anti reflex coating.
  For the expansion of the spectral range, quartz glass windows should be used. We can deliver quartz windows with and without coating on inquiry.

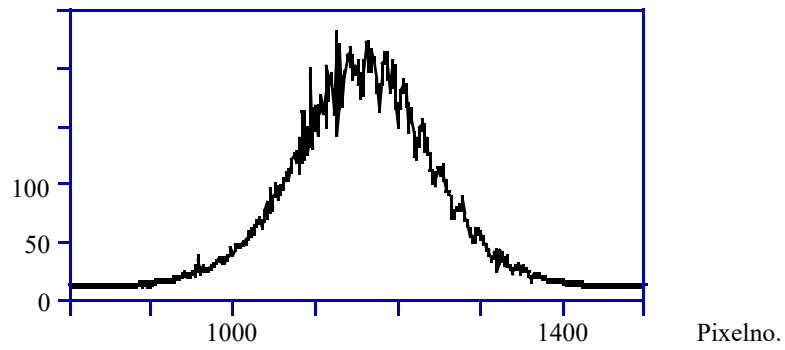
When sticking the window it must be paid attention to the humidity of the air! Otherwise condensation could happen on the inside of the sensor window.

IMPORTANT!
No guarantee for problems, which are caused through mechanical damage of a sensor without window!

4.2.1 Avoidance of interference with sensors without window

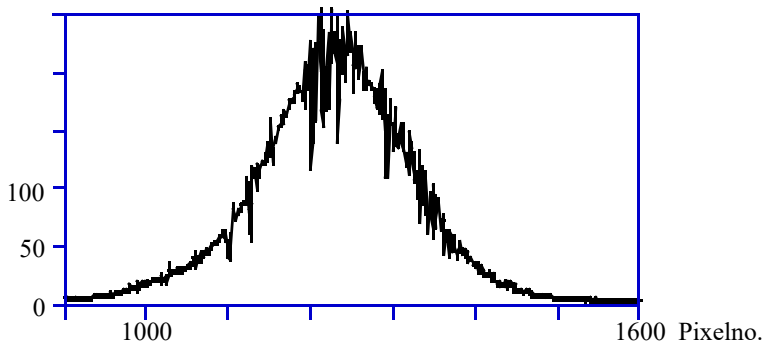
The measurement with coherent light is influenced by the window in front of the sensor which should protect the pixel of dust and mechanical damage. The window leads to interference. As an example tree measurements are shown of a He-Ne-laser beam profile, two taken with window and one without window.
Two modulations occur within the measurement signal: one is determined through the thickness of the window, the other through the distance of the lower rim of window to the highly reflectance surface of the chip. (picture-4.2).

picture-4.2: HeNe-Laser beam profile, sensor with window



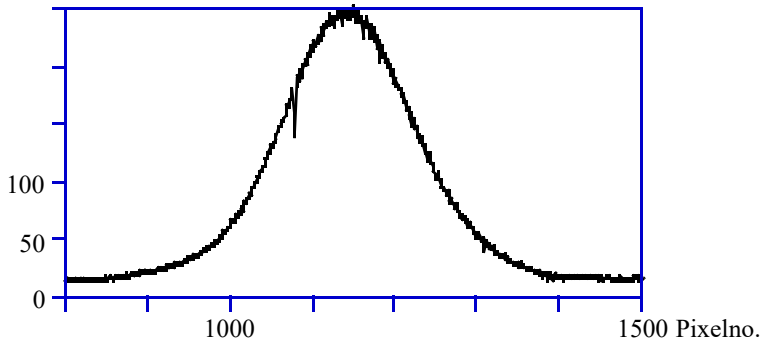
The modulation can be reduces by an angel within the light beam, however, this does not avoid the short wave beam (picture-4.3).

picture-4.3: HeNe-Laser beam profile, sensor angled



A picture without interferences can only be taken if the window was removed (picture-4.4).

picture-4.4: HeNe-Laser beam profile, sensor without window



A further advantage of using sensors without window could be the enlarged spectral range. The sensor itself could be sensitive down to 200 nm, but the window in front of the sensor selects the light only down to 400nm (depend also on sensor).

But be aware of the higher sensitivity of a sensor without window against dust and mechanical damage. In the example measurement (picture-4.4) a grain of dust is located at pixel number 1100 and eclipse the sensor at these pixel. These coverages might be disposed by a light blow but though a heavy expiration can destroy the tiny bonding connection. For laboratory measurements the window can be removed before each measurement. For measurement task in rough surrounding the window should be especially coated for the used wavelength.

Please ask for windows with special coating or quartz-windows for enlarged spectral range measurements.

Attention please!
No guarantee for damaged sensors without window due to mechanical damages.

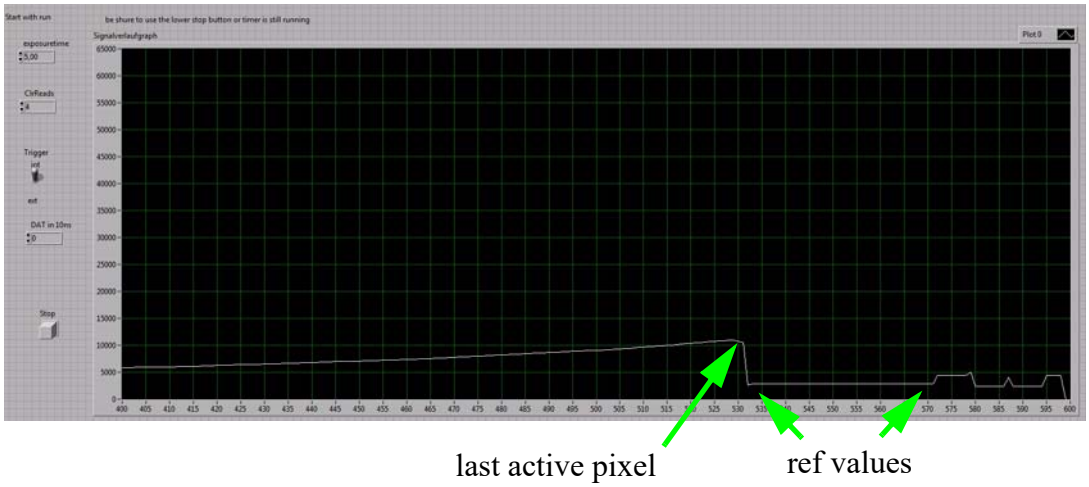
4.3 Temperature influence

The temperature influence in dark noise is quite big at longer exposure times, so cooling helps a lot here. For short exposure times this effect is not that big, so the costs for the cooling does not beat the benefit here.
There is a 2nd effect by temperature: the drift of the complete signal by warming up of the electronic circuits and the sensor itself. The first effect is made as low as possible, but the sensors self heating cannot be suppressed, especially when running in highest speed.

4.3.1 Drift of signal line

When the camera is switched on it needs a time for warming up (15 min.). Also when the measurement was stopped and the clock was not generated for a while, the buffers and driver ICs cool down a bit. This is especially true for high speed sensors like the IL-C6 sensor, but also cameras with 16 bit A/D can see this warming up effect. When the read loop starts again the video signal will begin to drift completely up or down. This effect can be up to 3000 counts (on a 16bit scale 0..65000 counts) for a S7030, where the IL-C6 and the G11608 and G11620 has a special compensation to suppress that (cds).
Trying to compensate that by hardware would only lead to additional errors, so the best solution here is to subtract this offset by software.

picture-4.5: video signal of S7030



To correct this shift of the complete video signal, a software routine can calculate the drift and subtract this constant from all pixel values. Therefore it makes sense to read some more then the active pixel (see picture-4.5 between pixel 535 and 570). These pixel are not real, but this floating voltage level can be used to measure the drift. The output transistor of the sensor itself is responsible for that and heats up the sensor at higher speeds. As this value is not really a zero it should be subtracted from all pixel values, but an additional offset value is necessary to stay always positive (the array is defined as unsigned words). Example: corval(pix) = val(pix)-ref+1000;

The ref value here can be calculated as mean value from 535 to 570

4.4 In terms of electrons

A good possibility to compare sensors is to calculate the amount of electrons they generate. Here the saturation values can be used and if they are divided by the dynamic range of the converter, the resolution of one count in electrons can be compared.
In Table 4.1 on page 28the values for different sensors are shown.

Qsat is taken from the data sheets.The FFT and IR sensors have a full well capacity.
One electron has the charge o f 1,6 x 10^{-19} C.
The number of electrons ne is calculated by Qsat/e.
The AD converter has a 16bit scale from zero up to 65000 (2^{16})counts.
The values for the read noise are measured and the rms value of a single darkened pixel over 400 scans is calculated as root mean square value trms. This is an over all value of sensor and electronics at 2MHz pixel clock (10/30 MHz for 3010/3030 sensors).
The trms value was measured at the specified linerate lr. It can vary ±0.5.
Values are measured for 512 pixel sensors, other lengths vary.
res shows the noise level in electrons. The dynamic range is 65k/trms or ne/res.
QE is taken from the data sheet.
If the res value is divided by the QE (wavelength of max. sensitivity), the res shows the noise level in counts of photons (phot).

Table 4.1: generated electrons for different sensors

Sensor	type	Qsat [pC]	ne [Me]	1count = [e]	trms [cnt]	lr [Hz]	res [e]	QE [%]	res [phot]
S3904	PDA	25	156	2.4k	4.5	3.4k	11k	50 (600)	22k
S7030	FFT		1	15	6	2k	90	92(650)	98
G11620	IR		75	1.1k	4	3.4k	4k	78(1600)	5k
S12198	CMOS		20	300	12	8k	5k	70(750)	3k5
S11490	CCD		0.5	30*	10	50k	300	84(700)	360
G10768	IR	0.25	1.6	100*	10	40k	1k	85(1350)	1k2

S3904, S8381 and S7030 are 1kHz sensors with 16bit AD converter.s
* HS- Sensor S11490 and G10768 have 14bit AD (0..16000 counts).

4.5 FFT sensor

The FFT (‘Full Frame Transfer’) sensors are area sensors which can be used in 3 different modes: Binning mode, Area mode, ROI mode. The modes are achieved just by generating different clock schemes.

4.5.1 Full Binning Mode

The Binning Mode is the standard mode for this sensor. Here it acts like a line sensor and uses its noise improvement function (see chapter-1.3).
Here all vertical clocks (vclks) are generated once before the horizontal clocks (hclks) appear. In this mode the highest line rate is achieved as the horizontal register is transferred only once. The hclks must occur pixel times.
Tread = vclks * 3µs + pixel (hclks) * 0.5µs

4.5.2 Area Mode

Beside the standard mode, this sensor can also be run as an area sensor.
Here for every line one vertical clock and all horizontal clocks are generated to read the complete sensor line by line. This is the slowest mode as all single pixel values must be transferred. All horizontal clocks appear vclks times.
Tread = vclks * 3µs + vclks * pixel * 0.5µs.

4.5.3 Range of Interest ROI Mode

In case you have 2 spectras on one area chip, the sensor can be divided in lower and upper half by clocking vclks/2, reading all pixel and then again for the lower half.
Tread = vclks * 3µs + 2 * pixel * 0.5µs.

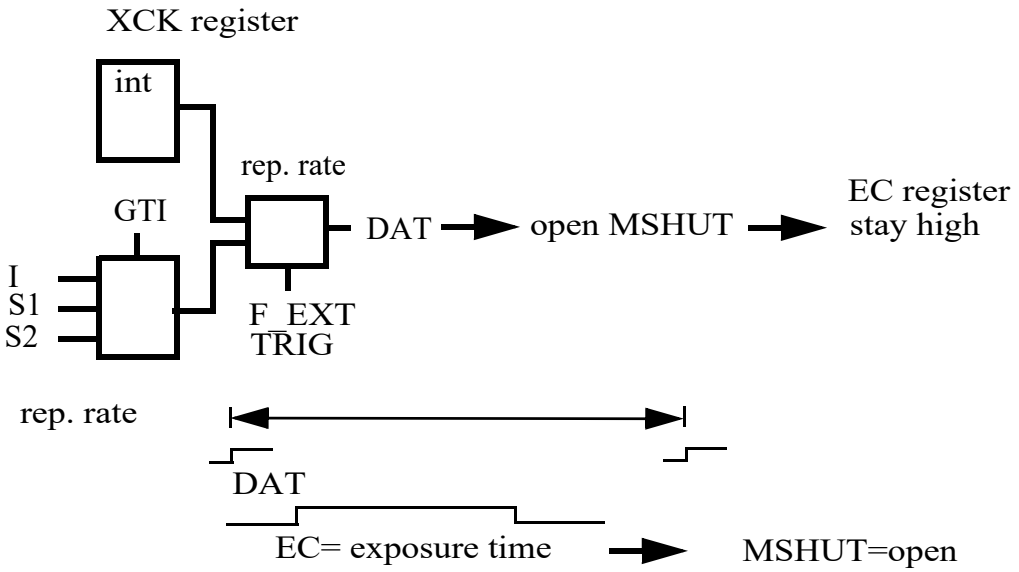
4.6 EC Exposure Control

Implemented in the software is a shutter function for switching the sensor sensitivity on and off. With some sensors (S11490) this can be accomplished electronically (these sensors have an extra gate to erase the photo diodes charge), other sensors (FFTs) must use a mechanical shutter if this function is needed (i.e. with cw signals).
For this purpose we have implemented a timing generator which can generate this “open shutter” pulse.
To disable this function, just set the value of the EC register (see chapter-6.2.3.11) to zero.

4.6.1 Working with a shutter

When a shutter is used, we need 2 control signals for this mode:
exposure time and repetition time.

picture-4.6: Trigger with shutter



The EC register (EC= Exposure Control) sets the shutter open time (in this case the exposure time) and the XCK register sets the repetition rate. The repetition can be triggered external or internal and can be delayed by the DAT register if needed.

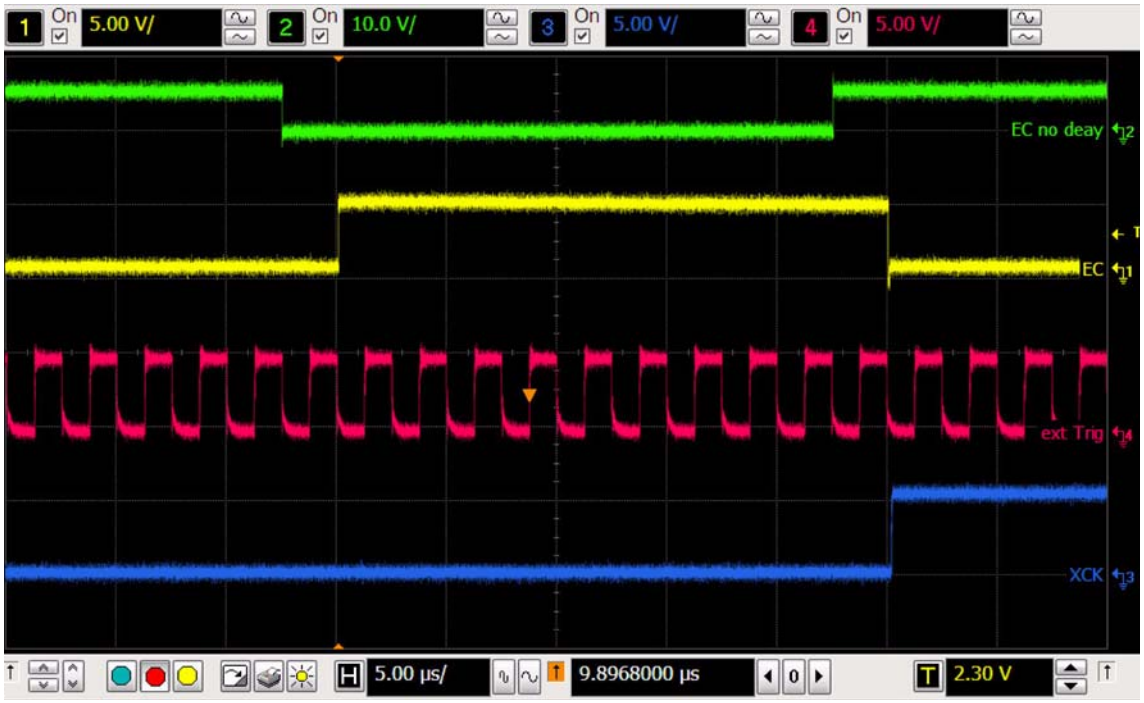
4.6.2 Mechanical SHUTter MSHUT

The shutter signal (EC) can be output with the TORReg (see chapter-6.2.3.12) on the PCIE boards output connector “O”. Here a mechanical shutter can be connected. This TTL signal must be connected with the shutters trigger input connector. The mechanical shutter control has to be set to open, if the shutter signal is high.
Be aware: the mechanical open/close reaction is delayed to the trigger signal. Some shutter controls have a monitor output to control the real open/close timing on a scope.
The shutter has a **maximal** allowed frequency. The uniblitz LS3 shutter has a 200Hz/50Hz limit. That means the shutter can switch with 200Hz for max. 4 seconds and with **50Hz** continuously. So the software is set to warn the user if the shutter time EC is set to < 20ms. The mechanics is delayed about 2ms to the EC pulse.

4.6.3 Exposure Control for high frequency pulsed lasers

For high repetition rates the camera read duration is too long to get one scan for every shot. But with the exposure control function (EC), it is possible to get a certain amount of n pulses on one scan. Here it is important to get really n pulses and not n±1 pulses or so. Here the exposure window (shutter open) can be placed very precisely to the laser pulses which trigger the PCI boards input.

picture-3.21: EC counts external pulses



the here shown example counts 10 laser pulses where the shutter is open. After counting to 10 the shutter is closed again. A scope can be used for control.

The number of counts must be written to the EC-Register (chapter-4.2.6.10). Here in the example we have set it to 10 pulses. To enable the external trigger input, the high bits must also be set.
WriteLongS0(1,0xE0000010,0x24); //set EC to 10 pulses, enable ext. trig input
(for labview: 0xE0000000 = 3758096384)
Also a delay is implemented (chapter-4.2.6.14), to get the EC window **fine adjusted** to the gap. The values are entered in 10ns steps.
example: WriteByteS0(1,0xff,0x36); //set fine adjust to 255*10ns pulses
WriteByteS0(1,0x80,0x37); //enable fine adjust
Don‘t use WriteLongS0(.,.,0x34) or you would change the DELAY value in the lower word.
To see exactly when the shutter is open, the PCI boards O plug can be used.

Here the TOR register must be set to
WriteByteS0(1,0x40,0x2B) //set TOR to show the EC (shutter open) signal
Instead of the PCI boards TrigIn input, the optional S1 and S2 can also be used as laser counter input. The flags in the EC register must be set accordingly

asymmetrical pulses have lower values.

4.7 Exposure Control (EC) Function for FL3030

The sensor has a control gate (ARG) to clear the internal CCD register. This can be used to implement an electronic shutter function. If ARG is high, the internal photo sensitive area is hold reset, if low, the sensor integrates the light.
The gate is controlled by the EC register (see chapter-6.2.3.11). If the EC register is set to a value >0, this phase starts immediately after the trigger. If it is set to zero, the electronic generates a clear signal at the end of the read phase.

The sensor S11490 is a high speed sensor and is not completely cleared by one read out. Therefore it may not be used without a reset signal, or following readouts have a crosstalk. Especially when used in a pulse on pulse off system. The sensor must be cleared after each read.
If the EC function is used (EC<>0) the shutter closed phase also resets the internal photo diodes.
If the EC function is not used (EC=0), an internally generated 800ns reset signal is generated automatically after each read (XCK goes low).

picture-4.7: Exposure Control Signal

red signal: shows the ARG signal when EC=0, is used to clear the sensor
green signal: shows ARG when EC is used (here EC=1000=10µs)
yellow signal: Shows XCK when the camera read is active.

In a **50kHz system with EC=0** the timing is shown in picture-4.8.

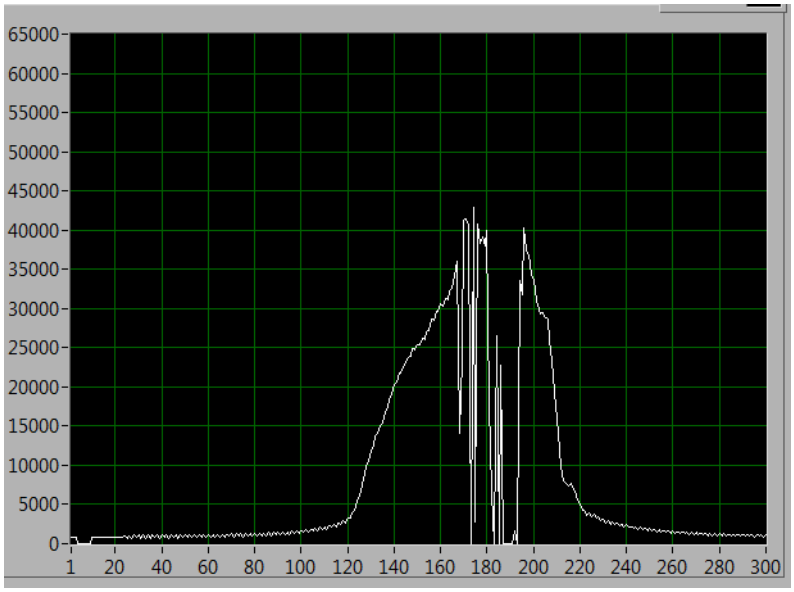
picture-4.8: 50kHz timing with EC=0

red signal: shows XCK (is high for 17µs).
yellow signal: shows TOR output -> shutter is open when high
-> so the light signal should occur within 2µs before XCK goes high.
The ‘O’output connector of the PCI board shows the shutter open periode if set to 3 (see chapter-6.2.3.12).

4.8 IR sensor

The IR sensors G11602 and G11608 as well as the cooled series G11475-G11478 are available with 256 or with 512 pixel. The 512 pixel versions have 2 separated output channels with own signal path: one for the even pixel and one for the odd ones. That means that each path has an own AD- converter with offset and amplification adjustment. In case you have a double line version of ir sensors with 512 pixel, you have over all 4 signals to adjust.
The ir sensors are about 100x less sensitive then the FFTs (see Table 4.1 on page 28). On the other hand they have a EC- function with better resistance against overexposure. They can be overexposured 100 times before the electrons flood the sensor and scrambles the signal.

picture-4.9: Overexposure of ir sensor



be sure to exposure the camera when XCK=low. If too much light hits the sensor during the XCK=high phase, the signal can be scrambled like shown in picture-4.9.

picture-4.10: IR exposure timing

5 Software functions

5.1 Control Functions

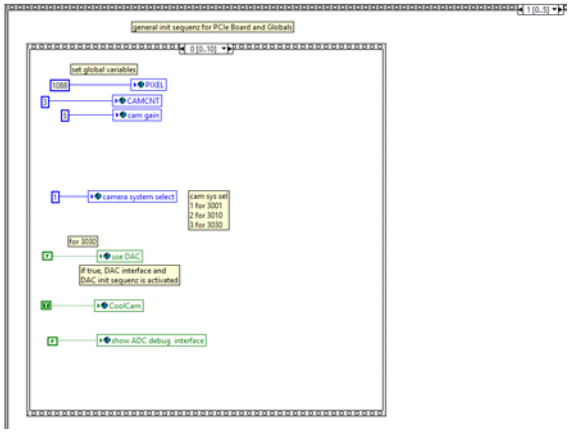
We supply a DLL: ESLSCDLL.DLL with source code where the necessary functions to control the camera are implemented. Mainly first the PCI boards registers must be setup correctly for the various functions of different sensors. After that the DMA transfer is started and the transfer runs automatically by hardware. So some functions are set by writing a specific value to a PCI board register and some functions must be set in the camera by writing a value to a camera register.

Therefore the main functions for setting up the camera are:

WriteLongSo0()	-	WriteL.vi
SendFLCam()	-	SendFLCam.vi

As the source code is commented, please have a look there for deeper explanations.
The examples show how to setup the cameras. They are written for all series: 3001, 3010 and 3030 and the target is selected by a global flag: camera system select. This is for easier maintenance. If you need only one camera type, you can erase all commands for the other series.

picture-5.1: Labview setup for different camera series



The CAMCNT parameter must be set to the value showing how many cameras are connected in the fiber link queue. The PIXEL value may only have discrete values. Please see chapter-5.2.CAM GAIN and use DAC is only valid for series 3030.

5.2 PIXEL value

The value for the parameter PIXEL sets the PCIE data transfer size and may only have discrete values greater then the active pixel of the sensor.

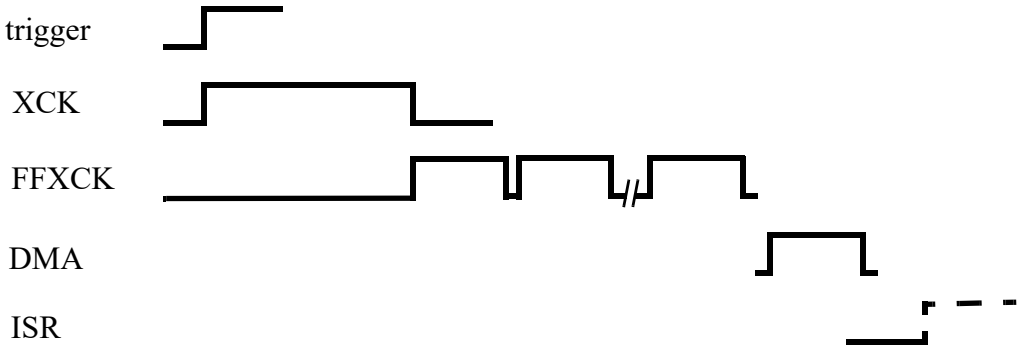
Table 5.1: allowed values for parameter PIXEL

active pixel	128	256	512	1024	2048
PIXEL val	192	320	576	1088	2112

5.3 Data transfer mechanism

The data transfer is a pipelined system between 2 FIFO memories (FIFO= First In First Out). One FIFO is in the camera, the 2nd FIFO is on the PCIE interface board. It is managed as shown in picture-5.2:

picture-5.2: Data Transfer for several cameras



XCK	the sensor is clocked and the data is written to the cameras FIFO
FFXCK	the data is transferred from the camera to the PCIE boards FIFO
DMA	the data is transferred from the PCIEs FIFO to the PCs RAM
ISR	each 500 scans the data is copied from the drivers memory space to the 64bit main RAM by the interrupt service routine (ISR).

5.3.1 Labview Functions

The data transfer is managed completely in hardware to reach the maximal speed. Therefore the main DLL calling functions are:

DLLSetupDMA -> vi: SetupDMA
DLLReadFFLoop -> vi: ReadFFFLoop

SetupDMA
This function receives the pointer of the data array. The array is allocated in labview and the address is passed to the DLL. It is intended that all data is packed in one big word array, but can be indexed by the parameter block(nob) and scans (nos).

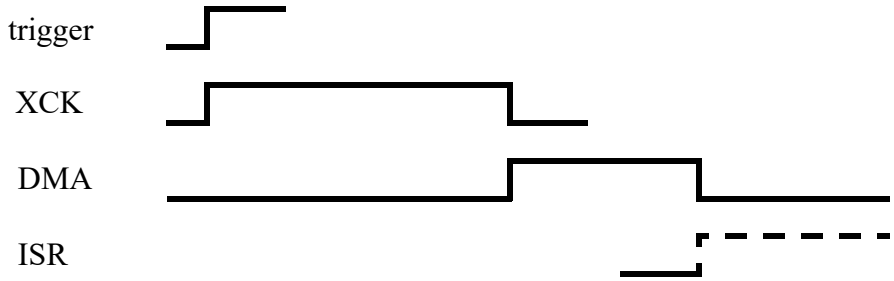
DLLReadFFLoop
This function starts the measure loop. It can be set to external or internal trigger. The internal trigger is set by the exposure time parameter. In external mode the parameter has no meaning.
The loop runs independent from the processor in hardware, as the external trigger can occur at any time. When all scans are assembled or when the ESC key was pressed, the ReadFFLoop returns.
The actual scan counter value (scanindex - chapter-6.2.4.3) or block counter value (blockindex - chapter-6.2.4.7) can be used to see how far the measure loop is in progress.

After the data was written to the RAM, it can be accessed by the pointer. With the labview tool: index array, you can access each scan individually.

5.4 DMA function

Implemented is a bus master DMA („Direct Memory Access“) engine for highest data transfer rates. The complete transfer is managed by hardware and must only be initiated once. The flow is accordingly picture-5.3.

picture-5.3: DMA Timing



The trigger starts a read sequence (XCK). With DREQ enabled, each DMA is started by the negative slope of XCK. The DMA buffer can accept 1000 scans. Every 500 scans an interrupt (ISR) sequence is generated to copy the DMA data to the main RAM. The 64bit bus master can handle the transfer to the complete in the PC available RAM without the need for additional ‘on board RAM’. Only a small FIFO (256kB) is implemented to de-couple the clock domains.

5.4.1 DREQ

The DMA transfer can be started by hardware. This is called Dma on REQuest. To enable this function the flag HWDREQ_EN in register IRQREG:30 (chapter-6.2.3.14) must be set.
If set, each camera read (XCK) starts a DMA when going low.
One DMA transfer has _PIXEL (1088) * 2 byte (words) = 2176 byte.

5.4.2 Interrupt Controller

The interface board claims one interrupt channel.
This interrupt is used to transfer smaller pieces of data blocks from the DMA range to the main RAM.
The DMA buffer claims DMABUFINSCANS * PIXEL * sizeof(USHORT).
Default is 1000 * 1088 * 2 = 2.1 MByte.
The DMABuffer is devided by 2, to copy the data in upper half / lower half order to the main RAM. When one half of the data is written to, the other half is transferred to the PC. When SCANSPERINTERRUPT = 500 (chapter-6.2.4.5) is reached, the higher and lower half is copied alternating to the main RAM by the interrupt service (ISR).

To enable the write interrupt, the flag „Write DMA Intr Disable“ in register DDMACR:7 (see chapter-6.2.2.2) must be set. If set, every DMA_done generates an interrupt if SCAN-SPERINTERRUPT is reached.

This high speed system can transfer more then 50 000 scans per second. If every scan would raise an interrupt, the PC would be blocked by an interrupt every 20 micro seconds

and could not do any other work. Therefore the scans are sampled until a certain amount is reached. Then the DMA is started and transfers this bigger block of scans to the main memory. The value can be programmed by the SCANSPERINTERRUPT register.

5.4.3 Block measure function

The hardware implements a block measure function. Here a trigger can start NOS scans several times.
If not needed set BLOCKS to 1.
If needed, set the BLOCKS register to the number of blocks needed and the NOS register to the number of scans for each block. Each block start can be triggered individually by the trigger inputs of the PCI board, or by pressing the space key.

picture-5.4: Block Trigger Function

The block trigger can be the „I“ input or one of the „S“ inputs of the PCIE board.
The NOS scans can be triggered by the internal timer, or by the „I“ input.

5.4.4 DMA mechanism

First the needed RAM is allocated by the application once. If this amount is huge, it can take a while until the calling function: Setup DMA comes back. So it is good practice to call this function only once at the first start and claim here the biggest amount which is ever needed. If your application needs smaller buffers later, you can just use smaller parts of the big buffer as well.
After the big RAM is allocated, the smaller DMA buffer is allocated by calling the function: SetupPCIE_DMA.
The measure is started by calling the function: DLLReadFFLoop.

When the DMA was started , the hole process is running in hardware. The PC is only used to setup all registers and the interrupt routines. An external or internal trigger starts each scan individually. After the start the scan counter is decremented until all scans are transferred to RAM. The hardware then stops automatically.
That means also that the hole measure process is running in an own time zone - like an own thread in an own core. It is not possible to synchronize other external processes to this as this transfer runs very fast.
In windows a so called time slice has a resolution of 1ms at the best. That means you can’t measure with different programs or PCIE boards with a better time relation then

1ms.
At a line rate of 50kHz, each scan comes with a 20µs distance. In a windows slice you have already assembled 50 scans.
So in case you need to get additional time synchronous signals, we have developed an IO-Control unit. Here we can pick up other signals with each trigger. The values are appended to the data stream of the image sensor, as if you have some extra pixels. Each scan has so the actual values stored in its data array. Please see chapter-9 for details.

Using more then one camera
The Fiber Link interface is implemented to connect several cameras in a line.

5.5 Data Structure

The data is stored directly in memory one by one, depending on how many cameras are in the queue:

1088 pixel words (16bit) of cam1	scan 1
1088 pixel words (16bit) of cam2	
..	
1088 pixel words (16bit) of cam_n	last of first block
1088 pixel words (16bit) of cam1	scan 2
1088 pixel words (16bit) of cam2	
...	

5.6 DLL ESLSCDLL

The DLL supplies all software functions which are necessary to run the cameras.

The compiler was set up for _stdcall and multithreaded DLL. If you need another interface, the source must be rebuilded with the new compiler settings. The standard settings are especially useful for linking the drivers to Labview.
The standard location for the DLL in labview is the subfolder: board.vi.

5.6.1 Own software extensions

The File LWLSC.DEF is necessary for the correct build and may not be omitted!
If you intend to add own routines, do not forget to enter the function here - just enter the name.

If the DLL should be linked to other C- programs you need to copy also the lib and exp files. The lib must be entered in the property->linker->input->additional dependencies entry of the project. The DLL file should be located in the same folder as the exe.

5.6.1.1 Linkage of DLL

The driver and the board must be initialized before using the interface from your own software.

The called software should at least look like this example:

```
DLLCCDDrvInit(1);    // searching the driver
DLLInitBoard(..)      // initialized the board
```

For simple testing here the called functions are:

```
DLLOutTrigHigh(1);
DLLOutTrigLow(1);
```

```
DLLCCDDrvExit();
```

Have a look at the About.vi example.

This signal can easily be controlled with an oscilloscope connected to the trigger out plug of the Interface board.

5.7 Labview

5.7.1 Labview Example

There is an example FL30xx.vi to show the calls of the DLL. The first 2 frames are used to initialize the camera for the specific sensor and camera type. Here all 3 camera types 3001, 3010 and 3030 have different setups. So you are free to delete the frames which are not intended for your system. The software is made to work with all versions.

Please set your parameter, like external trigger (the input is the connector marked ‘I’ of the PCIE board) or exposure time. Then enter nos and nob and start the vi.
now hit the alloc button and then the start button.
After all scans are sampled, the stored scans can be shown by moving the sliders. The scans are only stored in memory - not on the hard drive. So if you quit the program all data is lost.
When you selected the continuous mode, you can end the sequence by pressing the ESC key. Now you can walk trough the last data array with the slider.
Please use the exit button to leave the program. Otherwise you would get some error messages.

5.7.2 Labview Setup for FL3001

To adopt the software to the different sensor types and the Double Line System, some flags and sub vis must be set accordingly.

a) the HA FFT Sensor S703x
the sub vi IS_FFT must be called (if IS_PDA was called before, it must be reset)
and the vclk register has to be set to
lines = 64 (for 0906,1006)
vfeq = 12 (for 3µs vclk)

b) the HA PDA Sensor S390x
the sub vi IS_PDA must be called (if IS_FFT was called before, it must be reset)
and the vclk register has to be set to
lines = 0
vfeq = don‘t care

c) the HA IR Sensor G11608
same setting as b) PDA

d) the HA IR Sensor G920x
same setting as b) PDA

We deliver the camera systems with the correct setup for every sensor. So if you use the delivered setup as a guidance for your own needs. Functions which are set false by global flags can be deleted, as they are true only for special sensors.

5.7.3 Debugging the DLL in labview

The DLL can even be debugged within microsoft visual C when it is installed correctly. For that install the visual studio professional version, then the desktop development with C++ and after that the MFC x86 and x64 libraries.
The DLL must be compiled with the debug target selection and the DLL file must be replaced by the debug version in the board.vi folder.

6 PCIE Interface

For fastest operation of the camera our PCIE- Interface board can be used. With this board a transfer rate up to 250MByte/sec is possible.
Board P2167 is equipped with a Spartan S6 chip and implements a Gen1 Interface with 1 lane. The camera interface uses a standard fiber link cable and a send& receive module (SFP).

! Make sure to remove the SFP module before installation. The board does not fit into the computer with the attached module**!**

The following special functions have been added to the 4 SMB -connectors (picture-2.1):

S1,2: Shutter (chopper) state input
this state is written to every scan in pixel=4 when the camera read starts.

I: the trigger input synchronizes the read out to an external event. In the programs main menu the trigger source had to be chosen as external or single shot.

O: output for the synchronization of external events. That means the software can send any trigger sequence here. Default is the XCK signal which is high when the camera read is active.

Trigger functions
The O connector is a universal trigger output. The signals shown here can be programmed by a control register. (see chapter-6.2.3.12 for details). Default is XCK.
The digital signal voltage level is 3.3V.

The I connector can be used to trigger the read sequence by an external event (i.e. for single shot laser trigger).

The trigger pulse must last at least 2µs/400kHz and must be >1.3Vand <0.7V.
! The trigger input signal should have a maximum level of 30V!

The S connectors are additional trigger signals usually used to reflect the shutter (chopper) state signal. These states are written to the data stream in real time when the camera read is done.
They can also be used for additional functions like starting a block measure sequence or for measuring a time difference between the trigger and the camera read start. In that case we call it Opt1 and Opt2.
Signal level should be TTL (5V).

6.1 First pixel

6.1.1 Additional inputs and the first pixel

The first pixels are not valid and are sometimes used to store additional states or informations in each scan. The values are sampled at the begin of the camera read.

Table 6.1: Information of the first pixels

pixel	2	3	4	5	6	7
function	SSI+BLIh	BLIl	SCIh	SCIl	TDC1	TDC2

SSI (PIXEL=2)
The 2 optional opto coupled inputs S1 & S2(see chapter-2.2) can be used to write an additional external binary state to the data array at read time. This is for example useful if you need to know the state of a shutter or chopper signal when reading the camera (probe on/off). The hi / lo state is written at the beginning of the camera read (XCK goes high) to pixel = 4, which is usually 0 (high word of block counter). Here the state of S1 sets / resets bit 16=0x8000 and S2 sets / resets bit 15=0x4000 of the value of pixel = 4 (all other bits show the high word of the block counter).

Testing and finding the impact:
To test the signal attach a generator with 1Hz square wave 5V to the opt input and start measure in WCCD. Zoom to the first pixel and search the flipping data bit.

BLIh (PIXEL=2)
high word of Block Counter (see chapter-6.2.4.7).

BLIl (PIXEL=3)
low word of Block Counter.

SCIh (PIXEL=4)
high word of Scan Counter (see chapter-6.2.4.3).

SCIl (PIXEL=5)
low word of Scan Counter.

TDC1&TDC2 (PIXEL=6,7)
option: Time Delay Counter (see picture-6.2.4.9)

As the sensors have different dummy pixel in their line, the first active pixel differs from sensor to sensor.

Table 6.2: First active pixel of sensor

first active		PDA	FFT	IR G11608	
pixel		10	9	24	

6.2 Address range of PCIE board

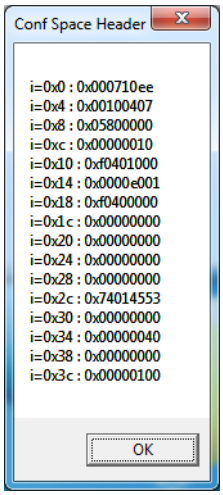
The driver can be found under the LSCPCI Boards entry in the device manager. Two drivers must be shown here: LSCPCIE Board Chip A7 Gen1 Lane1 and LSCPCIE Driver. The Version is 1400.
The PCIE board claims 3 address ranges in PCI space.

PCI space base0 in mem length=0x7ff
PCI space base1 in io length=0x7ff
Space0 base2 in mem length=0x7ff
and one IRQ

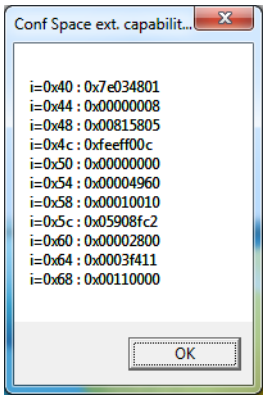
the range is devided in:
DMA = base2 + 0 functions: Read/WriteLongDMA()
space0 = base2 + 0x80 functions: Read/WriteLongS0()

6.2.1 PCI space

With the base0 address
picture-6.1: Configuration space



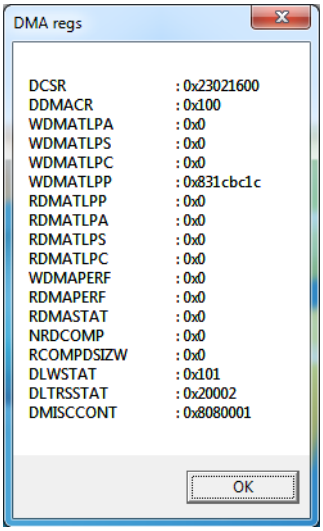
picture-6.2: Extended configuration space



6.2.2 DMA Controller

The DMA Controller can be accessed by 18 registers in base2, all 32bit wide.

picture-6.3: DMA registers



6.2.2.1 DCSR Device Control Status

This register is used to reset the DMA engine.

Bit	
0	reset, must be set and reset again to enable the DMA.
8:15	version number
16:19	data width: 1=32bit, 2=64bit and 3=128bit.
24:31	xilinx family 23=spartan6

6.2.2.2 DDMACR

Bit	Function
0	start write DMA
1	sets relaxed ordering on writes
2	sets no snoop bit on writes
3:6	reserved
7	sets write DMA done interrupt disable
8	DMA write operation done (cleared by initiator reset).
9:15	reserved
16	start read DMA
17	sets relaxed ordering on reads
18	sets no snoop bit on reads
19:22	reserved
23	sets read DMA done interrupt disable
24	DMA read operation done (cleared by initiator reset).
25:30	reserved
31	read error

6.2.2.3 DMA TLP Write Address WDMATLPA

This is the lower TLP address where the data is written. Here the hardware address is needed, not the virtual address. So this value must supply the driver.

6.2.2.4 DMA TLP WRITE Size WDMATLPS

Bit Function
0:12 TLP payload length in DWORDs <= 0x1FFF
13:15 reserved
16:18 TLP class field
19 64 bit enable for write address
20:23 reserved
24:31 upper TLP address (if 64bit) [39:32]

6.2.2.5 DMA TLP WRITE Count WDMATLPC

Number of TLPs to generate for write access. Only the lower word counts [15:0]. Upper word not used.

6.2.2.6 DMA TLP READ Address RDMATLPA

This is the lower TLP address where the data is read. Here the hardware address is needed, not the virtual address. So this value must supply the driver.

6.2.2.7 DMA TLP READ Count RDMATLPC

Number of TLPs to generate for write access. Only the lower word counts [15:0]. Upper word not used.

6.2.2.8 Device Link Width Status DLWSTAT

Bit
0:5 max. link capability
8:13 negotiated link width

6.2.2.9 Device Link Size Status DLTRSSTAT

Bit
0:2 max. payload capability
8:10 programmed max. payload size
16:18 max. read request size
the values are:

Table 6.3: Payload size values

val = 0	1	2	3	4	5
128 byte	256 byte	512 byte	1024 byte	2048 byte	4096 byte

6.2.3 Space0

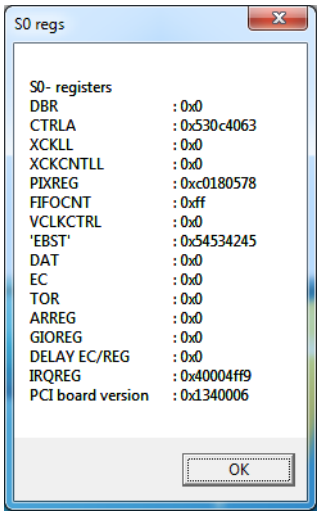
The board maps 0x7ff addresses of type long in the PCIE space0 of the computer (0..3f).
Table 6.4: Address list of PCIE Interface space S0

Longs in S0- range	Byte	Function
0	0	DBR
	1	0
	2	0
	3	0
1	4	CTRLA
	5	CTRLB
	6	CTRLC (Bit0=SyncTrigIn)
	7	0x53
2	8	XCKLL
	9	XCKLH
	0x0a=10	XCKHL
	0x0b=11	XCKMSB
3	0x0c=12	XCKCNTLL
	0x0d=13	XCKCNTLH
	0x0e=14	XCKCNTHL
	0x0f=15	XCKCNTMSB
4	0x10=16	PIXREG low
	0x11=17	PIXREG high
	0x12=18	FREQREG
	0x13=19	FF_FLAGS
5	0x14=20	FIFOCNT
6	0x18=24	VCLKCTRL
7	0x1C=28	„EBST“
8	0x20=32	DAT: delay after trigger
9	0x24=36	EC: exposure control (shutter)
A	0x28=40	TOR: Trigger options register
B	0x2C=44	ARREG
C	0x30=48	GIOREG
D	0x34=52	EC fine adj
E	0x38=56	IRQREG
F	0x3C=60	PCIE board version

Only 64 (0x1f) addresses are used for control functions which are described hereafter.

The registers in Space0 can only be accessed through the driver with the functions ReadLongS0 (ReadL.vi) or WriteLongS0 (WriteL.vi). The access is mapped in base2+0x80.

picture-6.4: S0 registers



6.2.3.1 DBR Data Bus Register

This register can be used to read data from the camera. It has a register where is written at XCK=low.

6.2.3.2 Control Registers

Table 6.5: Register CtrlA (0x04)

0x04	D7	D6	D5	D4	D3	D2	D1	D0
Read	TSTART	DIR TRIGIN	$\overline{\text{SLOPE}}$	$\overline{\text{BOTH SLOPE}}$	$\overline{\text{TRIG OUT}}$	XCK	IFC	VONOFF
Write		-	$\overline{\text{SLOPE}}$	$\overline{\text{BOTH SLOPE}}$	$\overline{\text{TRIG OUT}}$	XCK	IFC	VONOFF

TSTART: trigger signal after DAT&EC for software polling

DIRTRIGIN: trigger input combined with SLOPE.

SLOPE: set trigger to input slope (high = positive).

BOTH SLOPE: set trigger input to trigger on pos. and neg. slope

TRIGOUT: programmable trigger out signal set by software.

XCK: activate the read out of the camera data (high when reading).

IFC: control signal on data bus (used for vclks).

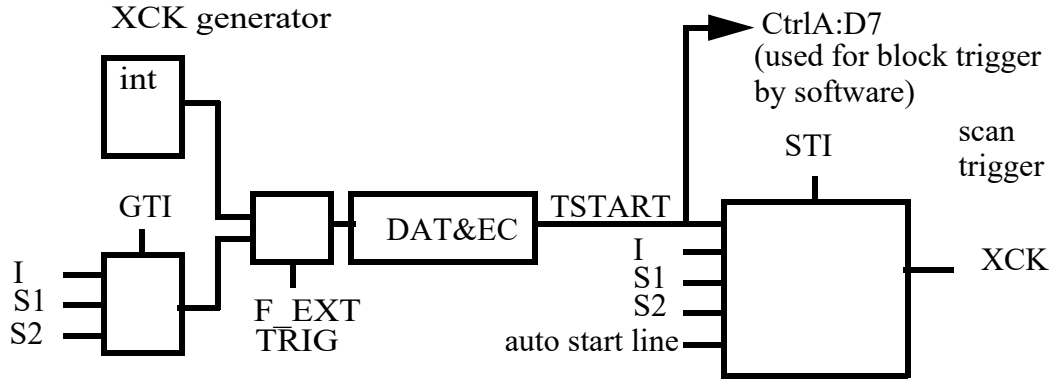
VONOFF: control signal on data bus (used for vclks).

Table 6.6: Register CtrlB (0x05)

0x05	D7	D6	D5	D4	D3	D2	D1	D0
Read/ Write			GTI1	GTI0	SHON	STI2	STI1	STI0

GTI1 general trigger input multiplexer
GTI0 00: “I”, 01: S1, 10: S2, 11:stop,
SHON Shutter on: keep shutter open - for adjusting purpose
STI2 scan trigger input multiplexer
STI1 scan trigger input multiplexer
STI0 000: TSTART, 001: auto start line, 100: “I”,101: S1, 110: S2, 111:gnd
the scans can be triggered independent from the block trigger

picture-6.5: Input Trigger Scheme



software polling with:

I → CtrlA:D6
S1 → CtrlC:D1
S2 → CtrlC:D2

Standard Setup
The default setup is that GTI (General Trigger Input) is set to internal and STI (Scan Trigger Input) to TSTART.

Area Mode
In Area Mode, the scans (number of lines) are triggered by auto start line and the GTI starts each block.

Table 6.7: Register CtrlC (0x06)

0x06	D7	D6	D5	D4	D3	D2	D1	D0
Read/ Write	0 -	1 -	$\overline{\text{EOI-CHB}}$ -	$\overline{\text{EOI}}$ -		$\overline{\text{S2}}$ S2	$\overline{\text{S1}}$ S1	$\overline{\text{STRIG}}$ -

EOI control signal on data bus
S 1,2 opto coupled trigger or chopper state inputs.

6.2.3.3 Register XCK (0x08)

XCK (exposure time) generator
Implemented is a 28 bit timer. The timer can be set with the XCK register and in XCKCNT the actual value can be read. Resolution is 1µs.
A pre divider sets resolution Res_ms=1 -> 1 ms resolution; Res_ns=1 -> 100ns

Table 6.8: Resolution of the timer

28 Bit	f in MHz	res. [µs]	max [sec]	max [min]	max [h]
Res_ns=1	10	0,1	26,8	0,45	0,007
268435456	1	1	268,44	4,47	0,07
Res_ms=1	0,001	1000	268435,46	4473,9	74,57

The MSB of the XCK register controls the timer

Table 6.9: XCKMSB Register

0x0b	D7(31)	D6(30)	D5(29)	D4(28)	D3(27)	D2(26)	D1(25)	D0(24)
Read/ Write	F_EXT TRIG	$\overline{\text{RS}}$	$\overline{\text{Res\_ms}}$	$\overline{\text{Res\_ns}}$	$\overline{\text{XCK-REG27}}$	$\overline{\text{XCK-REG26}}$	$\overline{\text{XCK-REG25}}$	$\overline{\text{XCK-REG24}}$

RS resets timer, must be =1 for free running.

F_EXT TRIG external Trigger (“I” plug), if 1. Each positive slope (or negative -> slope in CTRLA) starts a read sequence.

$\overline{\text{RS}}$ reset Timer, must be = 1 for starting the timer. (= TimerOn flag)

RES_MS Timer base = 1 ms
RES_NS Timer base = 100 ns

6.2.3.4 Register XCKCNT (0x0c)

here the timer state of the XCK timer can be read (28bit). example: the XCK reg is set to 1000 - that’s 1ms. So XCKCNT counts from 0..1000 and is reseted again.

6.2.3.5 Register PIXREG (0x10)

here the amount of words to transfer has to be entered. The register is type „word“ (bit 15:0). For correct PCI frame size only discrete values are allowed. These are: 192, 320, 576, 1088, 2112.

6.2.3.6 Register FREQREG (0x12)

0x12	D7(23)	D6(22)	D5(21)	D4(20)	D3(19)	D2(18)	D1(17)	D0(16)
Read/ Write	RS_FF	SWTrig						

SWTrig starts write to FIFO sequence by software (is ored to timer).
RS_FF reset the FIFO.

6.2.3.7 Register FF_FLAGS (0x13)

0x13	D7(31)	D6(30)	D5(29)	D4(28)	D3(27)	D2(26)	D1(25)	D0(24)
Read	VALID	$\overline{EF}$	$\overline{FF}$	$\overline{XCKI}$	$\overline{OVFL}$	-	-	-

VALID TRUE, if one or more complete lines in the FIFO.
EF TRUE, if FIFO is empty.
FF TRUE, if FIFO is full (the standard FIFO has 8kByte).
XCKI TRUE, if write to FIFO is active.
OVFL is set with FF=TRUE and keeps it until RS_FF.

6.2.3.8 Register FIFOCNT (0x14)

0x14	D7	D6	D5	D4	D3	D2	D1	D0
Read	$\overline{WRCN T7}$	$\overline{WRCN T6}$	$\overline{WRCN T5}$	$\overline{WRCN T4}$	$\overline{WRCN T3}$	$\overline{WRCN T2}$	$\overline{WRCN T1}$	$\overline{WRCNT 0}$

The „write to FIFO“ Register (bit7:0) counts the complete lines written to the FIFO. When the timer was startet, the counter is incremented with every line written to the FIFO. The DMA read of the FIFO decrements the counter. The Flag: FF_FLAGS:VALID is high if WRCNT>0.
This counter counts the read- and write cycles up to 255 independent of the capacity of the FIFO itself (FIFO default 32kByte)!
With FREQREG:RS_FF the WRCNT is set to 0,

6.2.3.9 Vertical Control Register VCLKCTRL (0x18)

The lower word of this register controls the vertical clocks which are generated before the start of the horizontal clocks is done. The upper byte of the upper word defines the frequency of the vertical clocks. This function is for FFT sensors only.

Register VCLKCNT (0x18) - word

This value (bit11:0) sets the number of vlk slopes. This means that this is 2* the number of vertical lines for an area Sensor (FFT). i.e. a sensor with 64 lines must set this register to 128, The value must be zero for line sensors. Value is 12bit, range is 0..4095.

Register VCLKFREQ (0x1b)
This value (bit31:24) sets the frequency for the vertical clocks, which usually has to be much lower then the horizontal clock frequency. Value set in 400ns steps +200.
val=0-> vclk = off, val=1 -> vclk = 600ns, val=2-> vclk = 1µs, val=7-> vclk = 3µs
value is 8bit = 0..255 (default = 7).

6.2.3.10 Delay After Trigger Register DAT (0x20)

The integration control DAT = delay after trigger function can be used to add a delay after an external trigger occurs.

DAT: delay after trigger (bit 31 = enable, bit 0..30 = val * 10ns).
can be used in all trigger modes.
must be 0 if not used.

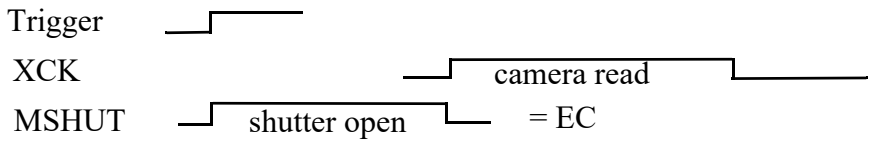
6.2.3.11 Exposure Control Register ECREG (0x24)

The integration control EC starts a “shutter open” signal after the trigger and keeps it active until the time is elapsed. After that the read sequence (XCK) is started.

EC: exposure control(bit 31 = enable, bit 0..30 = val * 10ns).
can be used in all trigger modes.
must be 0 if not used.

be aware: the max. line rate is limited by EC + XCK!

picture-6.6: Timing with EC



Some sensors with a shutter gate can use the EC signal directly (DALSA, S11490) , others must use a mechanical shutter (FFTs). If the mechanical shutter is used the signal can be output by setting the TOR register to 15. This signal must be connected to the input trigger of the mechanical shutter. These have a minimal pulse width, so please check the signal timing to keep the specs with a scope before connecting it to the shutter.
We use mostly the uniblitz LS3 which needs a minimum on time of 20 ms.
With the EC fine adjust register it is possible to keep the EC gate open for a specified number of pulses instead of just a certain time (see chapter-6.2.3.13).

6.2.3.12 TOR Register (0x28)

Here the signal which is send to the „O“ plug of the interface board can be set to show different internal signals. Default is XCK - what is high during the camera read.

Table 6.10: Trigger Options Register TOR (msb)

0x28	D31	D30	D29	D28	D27	D26	D25	D24
Read/ Write	TO3	TO2	TO1	TO0	RSLEVEL	no_RS	SEN-DRS	ISFFT

TOCNT (D23:16): trigger Out divider (bit 7 = enable, bit 0..6 = freq divider).
value = divider - 1
TICNT (D7:D0) : trigger In divider (bit 7 = enable, bit 0..6 = freq divider).
value = divider - 1

ISFFT high if FFT sensor (set IFC and VON to generate vclks and ENV)
SENDRS high if sensor needs a clear after read is done (PDA and S11490).
no_RS In high speed mode (2MHz) the PDA and S11490 are not completely cleared through read out. Therefore in default mode (bit = 0) a 800ns pulse is send via IFC to clear the diodes after read is done. To disable that pulse, set bit to 1.
RSLEVEL Level when SENDRS is send.

The **O- output of the PCI board** can be switched to show different signals.
Table 6.11: TO register

TO3..TO0	value	Function
0000	0	XCK
0001	1	REGO (TRIG OUT)
0010	2	TOCNTO
0011	3	RSMON
0100	4	DMAO (FFREAD)
0101	5	INTTRIGO
0110	6	DATO
0111	7	BTRIGO
1000	8	INTSRO
1001	9	OPT1(S1)
1010	10	OPT2(S2)
1011	11	BLOCKON
1100	12	MEASUREON
1101	13	XCKDLYON
1110	14	VON
1111	15	MSHUT

XCK Signal is high if camera is reading - default signal.

REGO Signal is programmable trough CtrlA-D3

TOCNTO	Signal is Trigger In - can be used in conjunction with TOCNT to divide trigger in frequency. Signal is enabled by TimerOn (XCK:RS - chapter-6.2.3.3).
RSMON	Reset signal monitor for some sensors (PDA, S11490)
MAO	FFREAR Signal is high during DMA read of Fifo - for test purposes.
INTTRIGO	Signal is Trigger In - can be used in conjunction with TOCNT to divide trigger in frequency. Signal is trigger in („I“) switched by flag ExtTrig (chapter-6.2.3.3)
DATO	Signal is high during DAT (delay after trigger) sequence (see chapter-6.2.3.10)
BTRIGO	Block trigger signal (pulse on each start of a block).
INTSRO	Signal is high during Interrupt service routine.
OPT1	Signal shows OPT1(S1) - max. freq=20kHz
OPT2	Signal shows OPT2(S2) - max. freq=20kHz
BLOCKON	Signal is high during TimerOn (is bit XCKMSB:D6 = XCK:30).
MEASUREON	Signal is high during the complete measure sequence (is bit R0:D5).
XCKDLYON	Signal is high during the XCK delay time.
VON	Signal monitors the VON function.
MSHUT	Signal is high during EC active.

6.2.3.13 EC fine adjust (0x34)

Here an internal fine adjust in terms of 10ns can be generated which is inserted after the EC signal goes high. That is useful if the EC function is used to count the pulses during EC open.
The highest bits are used to control the function.

Table 6.12: control bits EC fine adjust

0x37	D31	D30	D29	D28	D27	D16	D15:	D0
Read/ Write	ECFON	NOT	DIRT	TS2	-	-	fine	fine

ECFON	EC fine adjust on if high
NOT	if high the high time is set by clock pulses and not by the timer
DIRT	clock pulses come from “I” input of PCIE board if high, if low: S1 or S2
TS2	clock pulses come from S2 instead of S1
fine	fine adjust in steps of 10ns.

6.2.3.14 Register IRQREG (0x38)

Here 2 registers are implemented for the optional use with interrupt and a special bit for DREQ.

Bit function
0:15 IRQLAT (0x38) counts (bit 15:0) the time after read of FIFO starts in units of 25ns.
16:29 IRQCNT Count (byte) is incremented when one line was completely written to FIFO.
30 HWDREQ_EN enables DMA started by the low slope of XCK if set.
31 nc

6.2.4 Extended Registers

Table 6.13: extended Registers of PCIE Space0

Longs in S0- range	Byte	Register	Function
10	0x40=64	R0	PCIEFLAGS
11	0x44	R1	NOS
12	0x48	R2	SCANINDEX
13	0x4C	R3	DMABUFSIZEINSCANS
14	0x50	R4	DMASPERINTERRUPT
15	0x54	R5	BLOCKS
16	0x58	R6	BLOCKINDEX
17	0x5C	R7	CAMCNT
18	0x60	R8	GPX Control (TDC)
19	0x64	R9	GPX Data(TDC)
1A	0x68	R10	ROI0 (range of interest)
1B	0x6C	R11	ROI1
1C	0x70	R12	ROI2
1D	0x74	R13	TRIGCNT
1E	0x78	R14	XDLY
1F	0x7C	R15	

6.2.4.1 Register R0 (0x40) PCIEFLAGS

Single Bits here are used to show internal states of the PCIE board. Some bits read only (ro). These bits can be used to synchronize the software to the camera read.

D0: XCKI(ro) is high during the camera read.
D1: INTTRIG(ro) is high when input „I“ trigger is high
D2: ENRSTIMERHW enables the reset timer by hardware
if enabled (default) the timer is stopped when SCANINDEX reaches NOS

D3: INTRSR is high during the interrupt service (default: all 500 scans).
D4: BLOCKTRIG is high when a block of scans is started.
D5: MEASUREON is high during the complete measure sequence.
(Bit is set and reset by software only)

Fiber link signals
D26: lnk_up on SFP3 fiber module (SFP1=upper - used for CH3)
D27: Error on SFP3 fiber module (SFP1=upper - used for CH3)
D28: lnk_up on SFP2 fiber module (SFP2=lower - used for CH2)
D29: Error on SFP2 fiber module (SFP2=lower - used for CH2)
D30: lnk_up on SFP1 fiber module (SFP3=middle - used for CH1)
D31: Error on SFP1 fiber module (SFP3=middle - used for CH1)
lnk_up must be high if camera is linked, if low no camera connected.

6.2.4.2 Register R1 NOS

Here the over all number of scans to sample must be entered. The register is 31bit wide. max. value is 2^{31} = 2 147 483 648.

6.2.4.3 Register R2 SCANINDEX

This register counts the actual scan index. The value is also switched to pixel = 6.
If the ENRSTIMERHW(R0:b2) is set, the index is compared to the NOS value and if reached, the measurement is stopped. Counts from 0 to n-1 (is 1 less).
The counter is 31bit (D0-D30) wide, bit31 resets the counter.

6.2.4.4 Registers R3 DMABUFSIZEINSCANS

This register is set to the DMA Buffer length in scans. Should be NOS if one block is used. If set to 0, the DMA base address is reset after each transfer to the DMABaseAddr (TLPA). If set to the max. DMA Buflength, every transfer counts up the address until **DMABUFSIZE** is reached. Then it wraps around starts to use the DMA BaseAddr again.
DMABUFSIZEINSCANS is a 31bit (D0:D30)register (0.. 2 * 10^9).
bit31(D31) resets the actual block counter (must be set and reset before each start).

6.2.4.5 Registers R4 DMASPERINTERRUPT

If the Interrupts are too fast, they can be collected. So the INTR occurs only every DMASPERINTERRUPT scans (notice: with CAMCNT==2 each scan has 2 DMAs).
DMASPERINTERRUPT is a 31bit register. bit 31 resets the internal counter.

6.2.4.6 Register R5 BLOCKS

In case a block measure function is needed, here the number of blocks to sample can be entered. Each block consists of NOS scans (see chapter-5.4.3).

6.2.4.7 Register R6 BLOCKINDEX

Here the actual blocks are counted.

6.2.4.8 Register R7 CAMCNT

When more then one camera are connected in a queue, here the number of cameras must be entered. This value must be 1 for one camera and 2 for a double line system. In fact up to 16 cameras can be setup in a chain. All cameras in this chain are exposured and clocked synchronously (see chapter-2.5.1).
Only the lower 4 bit are valid (D3:D0).

6.2.4.9 Register R8 (0x60) GPX Control (TDC)

The PCIE board can be equipped with a daughter board which can measure the time between 2 pulses with sub nano second resolution. The Time Delay Counter (TDC) chip TDC-GPX is connected to registers R8 for control and R9 for the values.

6.2.4.10 Register R9 (0x64) GPX Data (TDC)

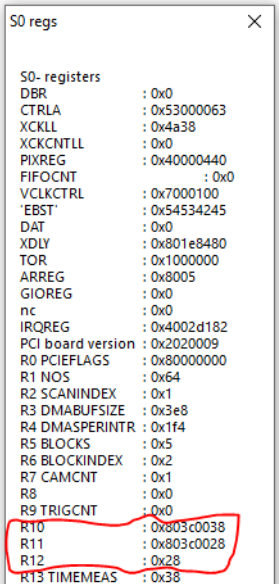
This register reads the measured delay data of the GPX chip. The values are also inserted in the data stream at pixel= 6 and 7 of each scan.

6.2.4.11 Range ROI Registers R10-12

The first 3 registers R10,R11 and R12 (6 words) implements the range of interest ROI registers for the partial binning of the FFT sensor. This sensor can be programmed to use a reduced binning. Here up to 5 ranges are programmable which store the number of lines (nol) *2 to bin. First the ARREG must be set with the number of ranges. Then each range register is set with the number of lines (*2) which should be binned together. The highest bit of each word decides if this scan should be kept or rejected. The functions SetupVPB() in UNIT BOARD or DLLSetupVPB() in the DLL can be used to setup the registers. The function automatically multiplies the nol by factor 2.

A 5 range scheme with 5 lines in range 1,2,3,4 and 10 lines in range 5 should look like this (CCDEXAMPLE -> Help -> Space0 / line 2 and 4 are kept) :

picture-6.7: 5 range Setup for partial line binning



As the scans are written to memory as they appear, its hard to find when which scan was sampled. For that the channel(C) and range(R) information is written to the dummy pixel number 2 in every scan. This value is written in the low byte.
The scheme is like 0xCR, example:

CHA range=1 pixel2 = 0x11 = 17
CHA range=5 pixel2 = 0x15 = 21
CHB range=3 pixel2 = 0x23 = 35

CHA and CHB (channel A or B) is for double line cameras.
note: only a range with keep active is written to memory.

6.2.4.12 Register R13 (0x74) TRIGCNT

For control how many pulses were used, here the trigger counts of the external input can be counted. This register counts the trigger pulses until a counter reset is done.
The reset function is on bit31 implemented. write 1 and 0 for reset.

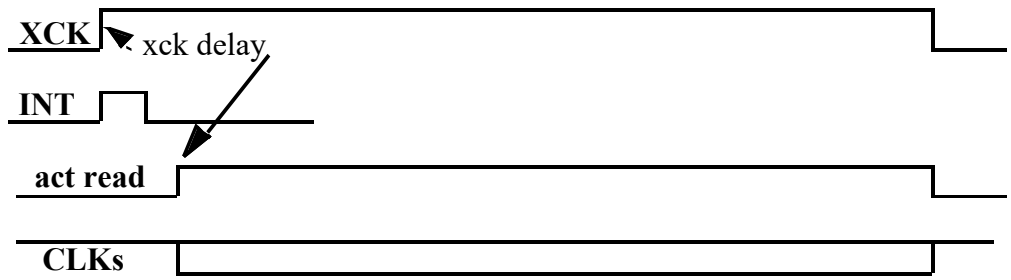
6.2.4.13 Register R14 (0x78 = 120) XDLY

This register can add a delay between camera on (XCK high slope) and start of ND or vclks clocks. Must be > 900ns for most sensors (value = 500ns + n * 10 ns; xckdelay = 50-> 1000 ns = 1µs). In the contrary DAT is intended to delay the high slope of XCK, but here the internal read sequence after the high slope of XCK is delayed.

This function can also be useful if the **Camera Control** is used and it starts an integration period for the external photo diodes. The integration INT is started with the high slope of XCK and the read must start after the integration period then. The signal if the read is active („act read“) can be monitored by a scope with the TOREG register (see chapter-6.2.3.12).

i.e. the PD integration periode is about 20µs.
xdly = 2200 (default)
Read starts after integration of the external photo diodes after 20 µs.

picture-6.8: Timing with XCK delay XDLY



If the Integrator is not used, it should be set to 0.

6.2.5 ID of Interface board

For Identification of the PCI board these registers can be used:

In the PCI- Configuration space the Vendor and SubVendor values:

Table 6.14: Vendor and SubVendor ID of the PCI- Board

	Vendor	Device	VendSubSys	VendSubID
Offset	0	2	0x2c	0x2e
ID	10EE	0007	4553	7401

ID Registers
In the S0 space are some type long registers with fixed values:
S0+0x04: value should start with 0x535n.
S0+0x1c has the „EBST“ value
S0+0x3c major and minor version of interface board

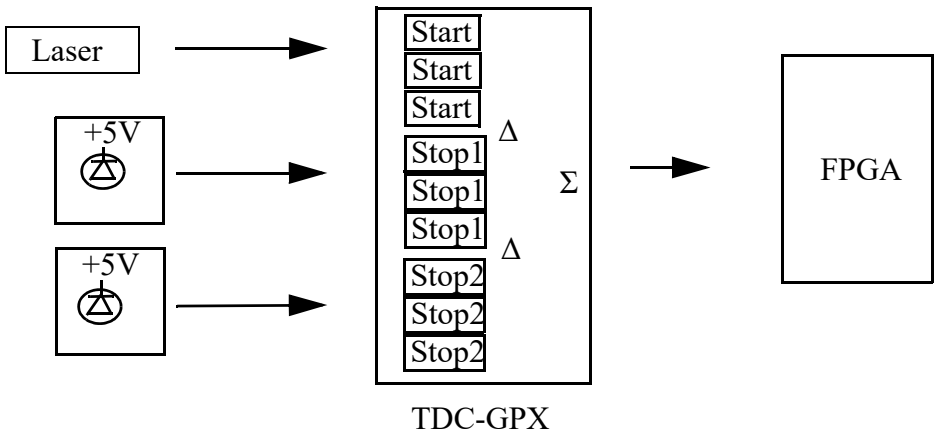
6.2.6 Jitter of external Input

The external Trigger Input to the Start of the camera read has a latency of 1.4µs.
This can be extended by the DAT (chapter-6.2.3.10) up to 21 seconds.
The Jitter is ±70ns(rms) and ±100ns (ptp).

6.3 TDC Time Delay Counter Option

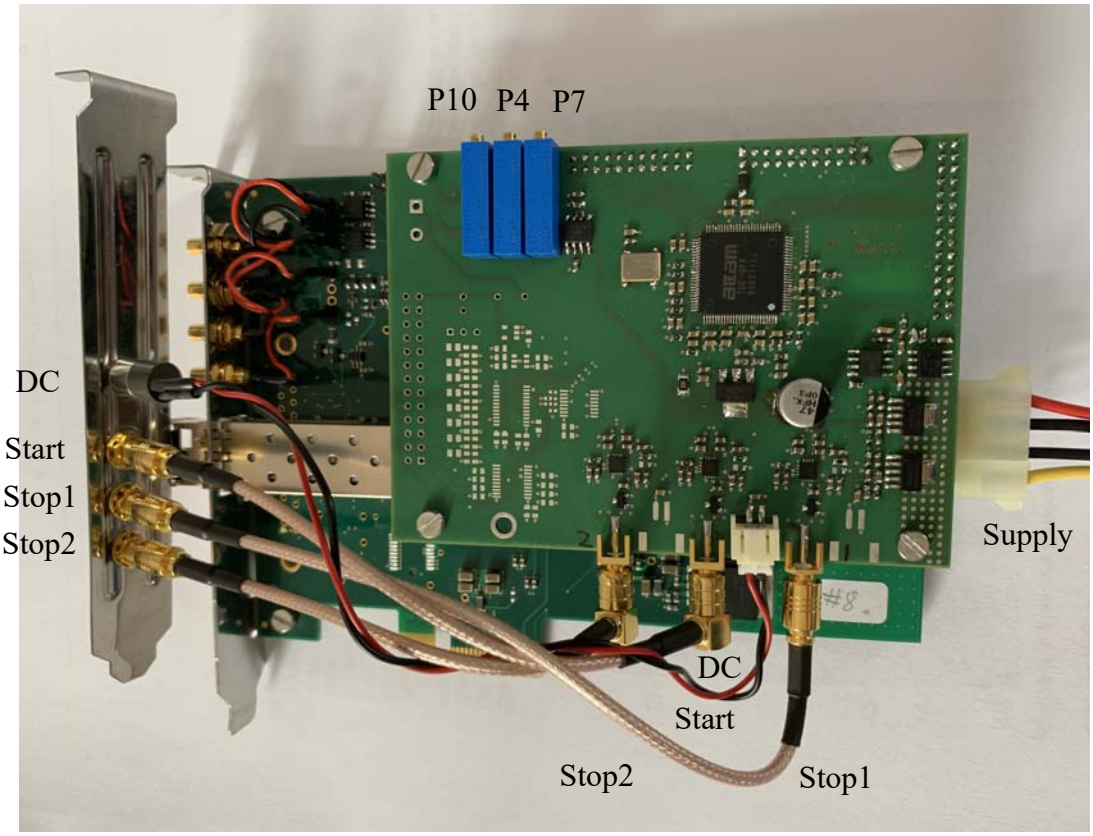
The PCI board can be delivered with a Time Delay Counter (TDC) function which can be used to measure the time between one start and two different stop signals with sub nano-second resolution. This option must be ordered separately. This option is located on the daughter board of the PCI Interface.

picture-6.9: TDC function



Each value for Start, Stop1 and Stop2 is sampled with 3 different timers. Each difference is calculated and the sum is then send to the interface board.

picture-6.10: TDC daughter board



Start: this signal gets the start pulse from the first photo diode
Stop1: this signal gets the stop pulse from the 2nd photo diode
Stop2: this signal gets the stop pulse from the 3nd photo diode
DC: Voltage supply for the photo diodes (5V)
Supply: The TDC board needs a +5V power supply. Therefore the board must be connected with the supply of the PC. At least the red and the black cable are needed.

We have 3potentiometer
P4: Start, P7: Stop1, P10:Stop2, which are used to align the comparators switching threshold of the start and the stop signals. Usually a photo diode signal is attached to Start and Stop and the threshold is set to 1V (or 0.5V). When the signal reaches this voltage level, the comparator generates a high pulse which is send to the TDC chip.
Changing the setting is usually not necessary when the diodes can generate a 0-1V signal or more (max. is 5V). In fact the inputs are not terminated, so the high impedance signals of a photo diode can be used here directly.

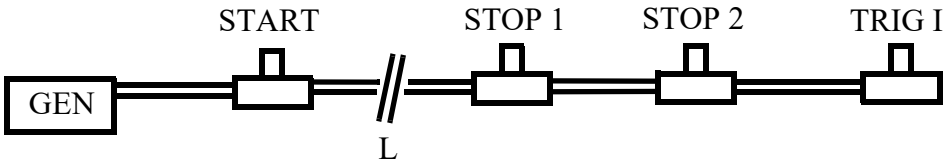
The range of the TDC is 30ps -580ns.

The rms Jitter of the delay is 2 counts, the ptp is 8 counts @ 30ns delay.
1 count is about 27ps
(see also chapter-6.2.4.9 for the software description).

6.3.1 TDC Test

The TDC counter must be synchronized to the camera read. So a simple test of the function would look like that:

picture-6.11: Setup for TDC test



Setup a chain of BNC cables with a generator (TTL signal). The signal path should be like picture-6.11 shows. Start and Stop are the plugs on the daughter board (picture-6.10). TrigI is the trigger input of the PCI board “I” (picture-2.1).
With that setup each trigger starts and stops the TDC (Time Delay Counter). The value is then displayed in pixel=6 and 7 after each shot.

The measured difference depends on the length of the cable L. Light speed is about 3ns for 1 meter length. If now the cable length L is changed to i.e. 2m, the mean value of pixel=6 and 7 should change accordingly.

These values should be noted and the mean value and rms value should be identified. The rms value is different for different delays.

As the values are added over 3 internal measurements, the value must be divided by 3.
Be aware that the value has also a constant offset to improve accuracy. Also differences in the signal path will have an effect here. Therefore the values for a zero delay should be measured with this setup here to get a calibration. You can use a scope to get the correct calibration delay values.
A complete description of the IC can be found at the inet. Search for TDC-GPX from ams.

7 Camera Control FLCC 30xx

7.1 Versions

The Cam Control can be ordered with 4 external inputs. These values are inserted in the video stream at the end of the line. Here an integrator (I-version) can be used or just a simple voltage input (V-version without hold).

The Cam Control is also available for single line systems and can be delivered with or without the integrator and voltage function.
The value is taken when signal INT is high, the voltage value when the camera read is active (end of XCK).

picture-7.1: CamControl with PD power supply

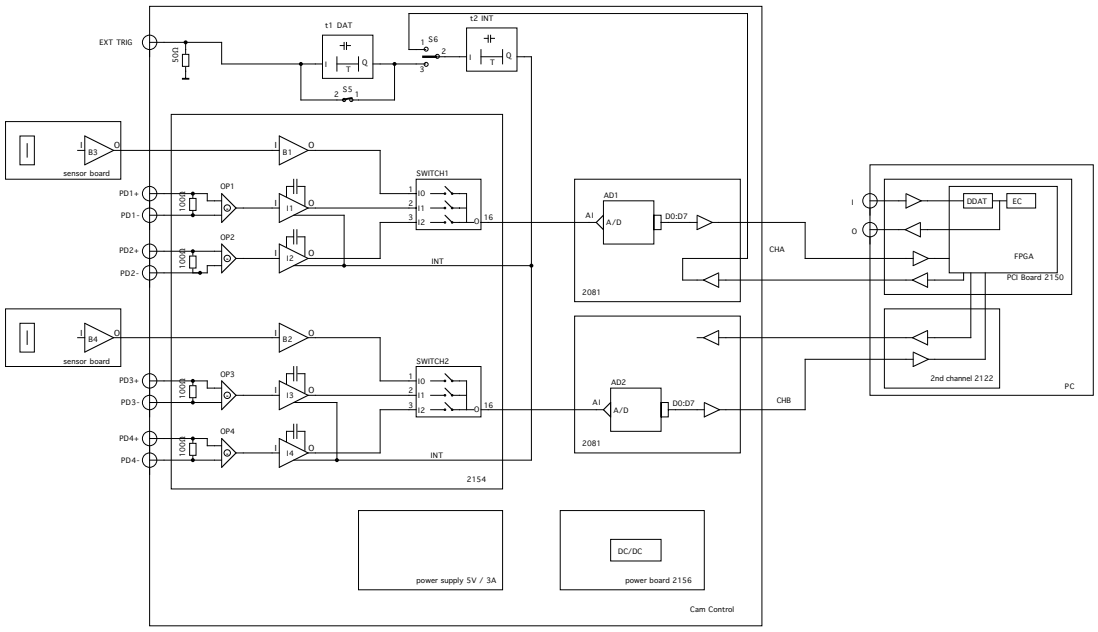
7.2 Schematic Function of Camera Control

The Cam Control can run up to 2 camera boards and 4 photo diodes. The power supply is also implemented here. Alternatively up to 4 voltage inputs are available.
The signal is integrated synchronous to the camera read and the values are inserted in the data stream (see chapter-7.3.3).

As seen in picture-7.2 there are 2 inputs possible for the external trigger input. These are explained deeper in chapter-7.3.6

The complete camera electronic and the A/D converter is mounted inside the control. So additional analog signals can be switched to the A/D converters input. The picture-7.2 shows the block diagram of the electronic.

picture-7.2: Block schematic of the Cam Control

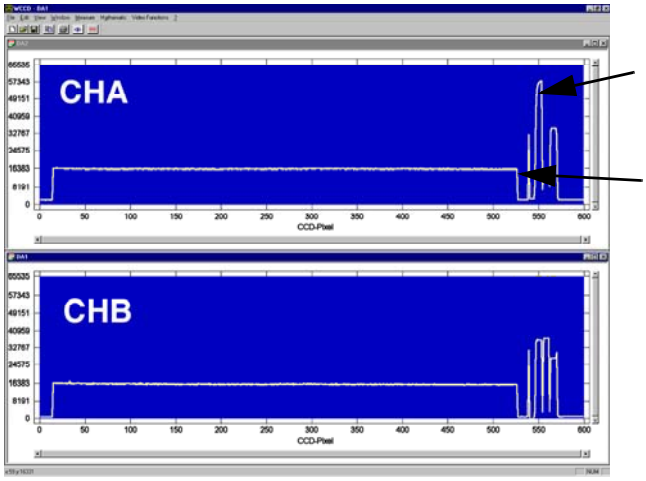


The integrator cycle can be started with different modes. After the adjustable integration time the values of the 4 channels are hold until they are switched to the output, when all active camera pixel have been read. So these values appear as additional pixel values at the end of the data stream (see picture-7.3).

7.3 Impact of additional signals

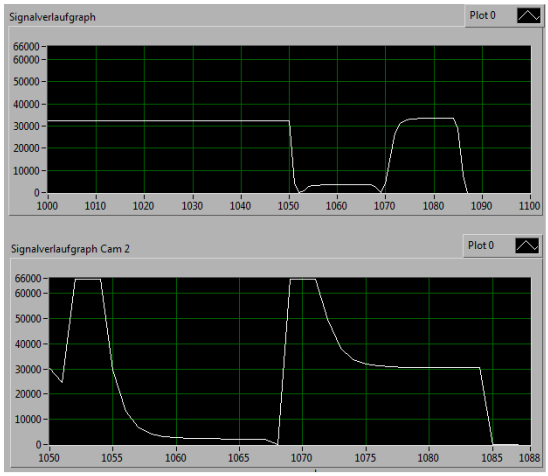
The external PDA- signals occurs at the end of the data array. In picture-7.3 the data stream is shown. First displayed are the values of the line camera (here pixel 20 to 532), then is a gap of non valid pixel. After that the 3 photo diode signals are shown on each channel (6 channel version) and a rest of non valid pixel values.

picture-7.3: Display of 2 channel data stream



Every PD signal consists of 16 pixel values (the A/D converter samples the integrator voltage 16times - could vary depending on sensor type). In case of a full scale value, an asymptotic slope can be seen at the first values. As the switch is not fast enough the first values should not be taken. The last values are stable and can be used. For additional noise improvements averaging of several values is recommended.

picture-7.4: Impact of PD signal in data stream (zoomed)

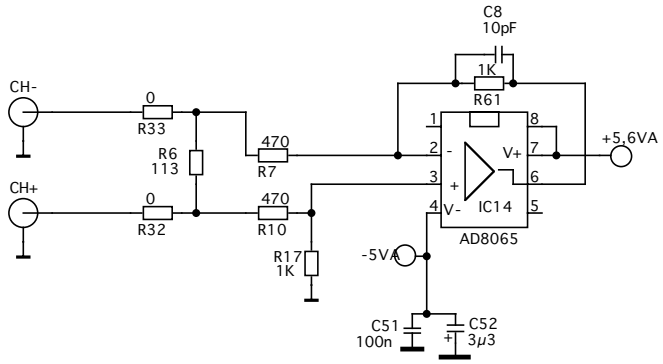


The voltage input has a big overshoot , so only the later values should be taken.

7.3.1 External Input

The 4 channels use differential signaling for better noise immunity. For ease of use standard BNC cables are used. Every signal has a pair of cables which should be twisted around each other and **must have the same length**! The input resistor is 100¾.

picture-7.5: PD Input schematic



The standard input voltage range is 2,5V±1V. This signal is amplificated before it connects to the integrator. A single ended output of the integrator input signal can easily be monitored on an oscilloscope with the PD1..4 BNC plugs on the rear. Here a 4V span shows that the signal is not overdriven (internal amplification = *2).

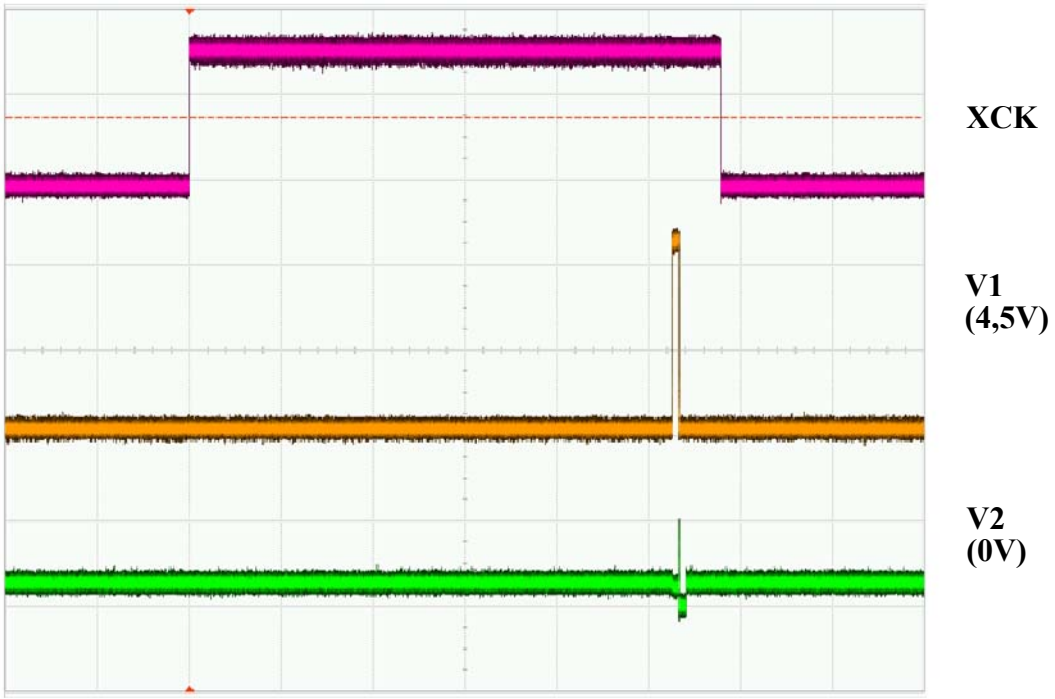
If needed the channel can also be made unidirectional by connecting the PD- input to GND. The input resistor is still 100 ¾ in that case. For correct 50¾ input, a parallel resistor of 100¾ should be connected parallel to the +input.

The low resistive input is not intended for direct use of a photo diode. Here an additional amplifier must be used (see chapter-7.5.1).
If an own PD amplifier is used, the signal must be adopted, so that the PD output monitors a 0 to 4V maximum signal (0..2V on 50¾). The peak width maximum is about 25µs (10µs for a square wave signal) which saturates the integrator. If the laser pulse is shorter, the signal should be stretched (Capacitor parallel to the photo diode).

7.3.2 Simple Voltage Input (V- Function)

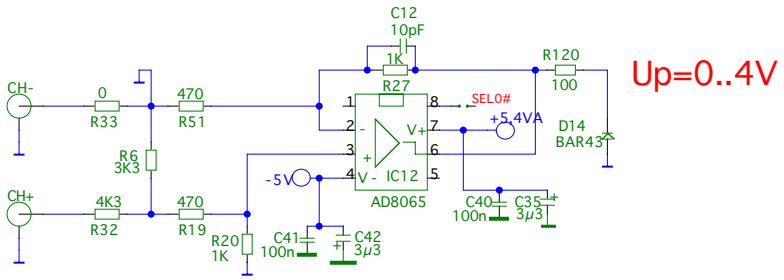
If the Voltage input function is used, the values are not integrated and stored. Instead the input is digitized when the read is done (xck=high). During this read the BNC output V1..V4 on the rear is active and shows the timing and voltage level(picture-7.6).

picture-7.6: Voltage Output



In fact here the A/D converter can be used like a sample scope.

picture-7.7: Voltage Input Schematic



The setup for an input voltage range of 0..10V is shown in picture-7.7.
With 10V at the input, a value of 4V is seen at the output PD1..4.
(be sure not to activate the 50Ω Input of a scope or the voltage will be lower).

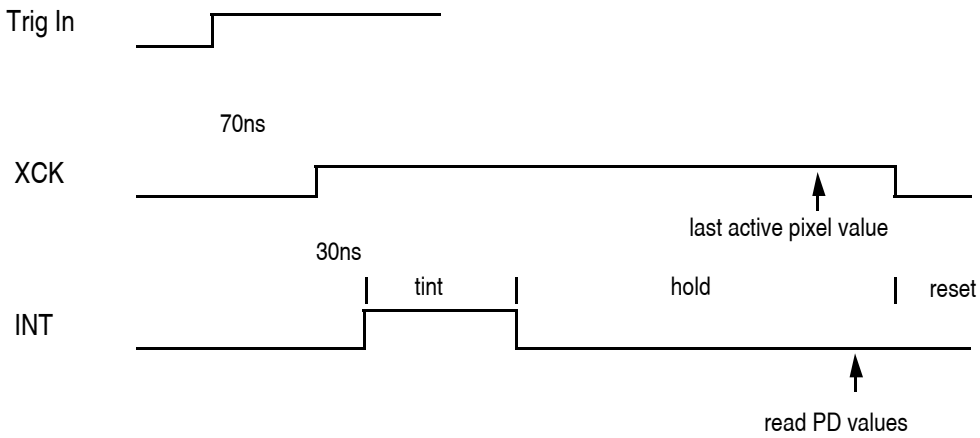
7.3.3 Photo Diode Integrator (I- Function)

The Camera Control can be equipped with 4 additional channels for external photo diodes. Every channel has an own integrator which is started at the beginning of the read sequence. The 4 integrated signals are held and switched to the data stream at the end of the read sequence after the sensor line was clocked out.

7.3.4 Integrator Timing

The Cam Control has an trigger input to start the integrate function with a very short and exact analog delay.

picture-7.8: Integrator Timing



The duration for the integration tint of the photo diode signals can be set with INT (picture-8.8) of the Cam Control (default = 20µs). DAT can insert an additional Delay After Trigger) if S5 in picture-7.10 is ON.

When tint goes low, the values are hold until they are switched to the A/D converter after the last active pixel of the sensor was transferred (usually after pixel*hclk, i.e. 600*1µs = 600µs). When XCK goes low the integrators capacitor is hold reset until the next trigger occurs.
The signals XCK and INT can be monitored by the BNC plugs on the rear.

7.3.5 Integrator Calibration

The full scale of the integrator is aligned for an input signal of 1.4V and tint= 20µs.

Alignment:
Start the measurement (XCK has a signal) and control with the INT BNC on the rear. Adjust „INT“ timer (INT on picture-8.8) to 20µs which starts when XCK goes high.
Apply a 1.4V constant Voltage at the + Input and connect - Input to GND (=case).
Align the supplied voltage that the BNC PD plug on the rear shows a constant 4V signal.
Now IV1, IV2, IV3 and IV4 are adjusted for maximum signal gain of the PD values (picture-7.3). The zero values are adjusted by IZ1/2 and IZ3/4 as a group, or by the IZ1 .. IZ4 potentiometers individually. After changing the gain, the zero values must be realigned again. First align IZ1/2 and IZ3/4. After that the IZ1..IZ4 are used to make the fine adjustment.
If a voltage input is implemented, use VZ1/2 and VZ3/4 instead of IZ1/2 and IZ3/4.

7.3.6 Trigger function

The Cam Control can be triggered in 3 different modes.
Default mode is the DDAT = digital delay = internal mode. The DDAT trigger uses 2 registers of the PCI Interface (DDAT= delay after trigger and EC/DLY = exposure control).
The ADAT = analog delay uses 2 monoflops which are build into the Cam Control (ADAT=P6 and INT=P5).
The DDAT internal mode is for easy running, but cannot reach the max. line rate.
The ADAT mode uses an external trigger lane and can reach the max. line rate. It also has a very low jitter.

The setup of the trigger modes is different and explained in the following chapters.

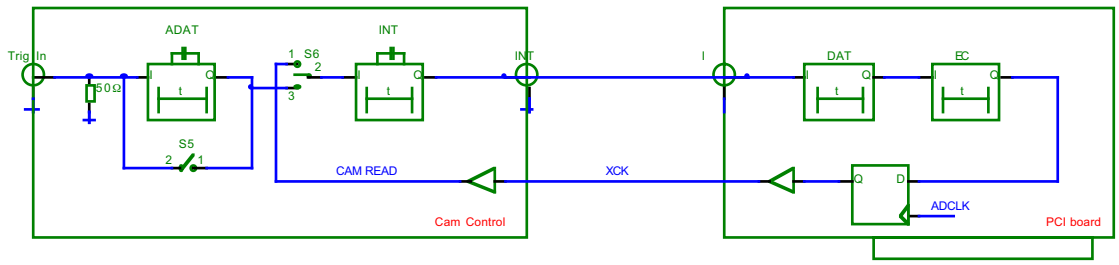
7.3.7 Analog Delay (ADAT)

The analog delay can be used to start the integrate before the camera read starts or when very short and accurate delay after trigger is needed.
This delay uses the ATrig Input on the front panel of the CamControl.

For very short delay the ADAT(P6) can be switched off by setting 001 in register Trigger select (TS- chapter-3.5.1.1). The (ADAT) of the Cam Control is disabled here, but there is still a minimal delay of 100ns coming from the input filter.

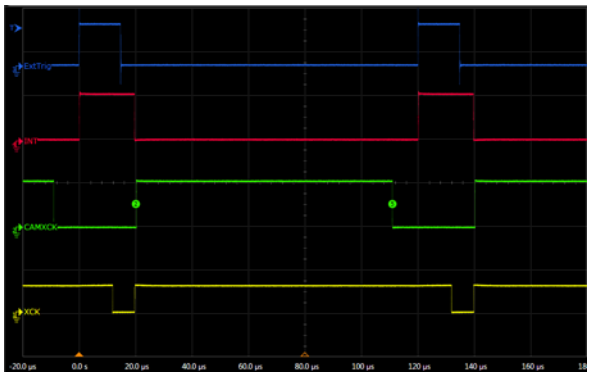
Setup for analog delay
setup a cable from INT connector of the CC to PCIE boards „I“ connector.
set PCIEs I- input to negative slope and to external trigger. The XCK signal is send via the fiber link.

picture-7.9: Setup for analog delay



S6 is in position 1 if TS is set to 000, S6 is in position 3 if TS is set to 001 or 010.
S5 is closed if TS = 001 and open if TS = 010.

picture-7.10: Timing when triggered with the ADAT signals



external trigger input of CamControl

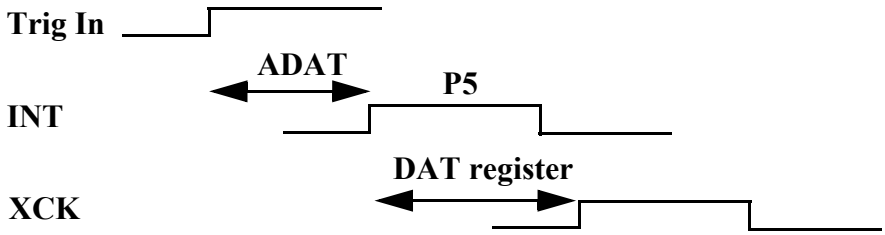
INT signal (20µs)

CAMXCK signal

XCK signal

CAMXCK is active during sensor read, XCK is active during sensor read + data transfer.

picture-7.11: Timing with analog delay



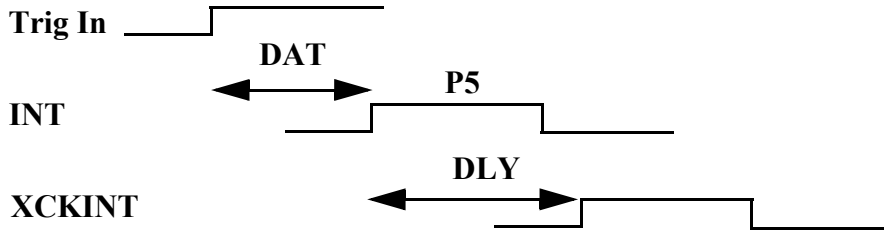
Alternative: the PCI Trigger Input (I) can also be connected directly to the trigger source and can be deayed by the DAT register of the PCIE board.

7.3.8 Digital Delay (DDAT)

Here the Trigger input is the BNC/Cinch plug marked I on the PCIE Interface board. The trigger starts the camera read directly. The DAT register can be used to delay the trigger before the integrator starts.
The duration of the integration is set by INT of the Cam Control. When all pixel values are sampled the additional 4 photo diode channels are switched to the A/D converter. The camera read can be delayed with the EC/DLY register to start after integrate is ready. All signals should be monitored with a scope during adjustment. The trigger can be set to external or internal.

Setup for digital delay
PCI board:
if external: ext. Trig In „I“ of PCI board starts sequence (DTrig)
DAT register sets the delay after trigger for starting INT
EC/DLY register sets the start of the camera read.
TOR register bit ECO must be set to = 0x30 -> trigger O is EC signal (chapter-6.2.3.12).

picture-7.12: Timing with digital delay



DAT is register 0x20 chapter-6.2.3.10
DLY is register 0x34 chapter-6.2.4.13
XCKINT is the internal read sequence.

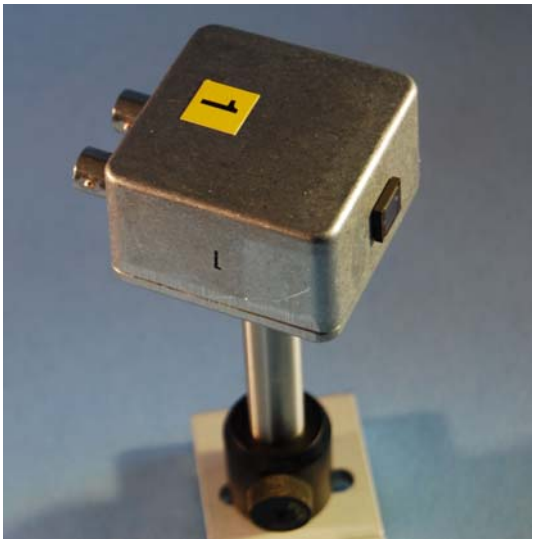
7.4 Power Supply

The main power switch is on the rear panel.
The power unit is a switching power supply with an input range of 110 - 240 V / 50-60 Hz with a voltage of 5V and 3A or 5A. All other voltages are derived by additional DC/DC - converters from these 5V. The power consumption is max. 10W.
The main fuses are beneath the power plug on the rear panel (2 items T1A). It can be reached after unplugging the cord and lifting the lid of the power connector.

7.5 Accessory

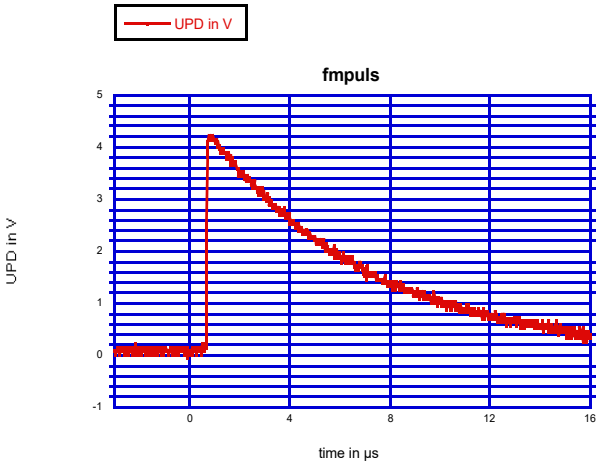
7.5.1 Photo diode (PD) Amplifier

We offer a well suited active photo diode amplifier for the Cam Control. Here the amplitude and the duration is optimized for the integrators input. The diode is especially a slow type with high capacity, to stretch the pulse to a time scale the integrator can handle. The power (6,8V) is supplied by the CamControl (no battery needed).
picture-7.13: PD Amplifier



Our PD amplifier supplies the signal which is best suited for the Integrators input (see chapter-7.3.6). That means the pulse is stretched and C-coupled to avoid dependencies of constant stray light. So it works best for short pulses <0.1µs.
The monitor BNC plug PD1..4 on the rear can be used to control the signal of each channel. The amplitude should not go beyond 4V and should be attenuated by optical filters if needed.

stretched femto second monitor pulse of PD amplifier



8 Maintenance

8.1 Maintenance Camera

After some time of running or after transportation, a realignment of the potentiometers (pots) , mainly the zero line ones, could be necessary.

Despite compensation of the electronic a disalignment of the zero line appears after turning on the camera. This effect reaches after about 15 minutes running time a stable final value. Therefore at critical measurements the camera should be given a warm up time of about 15 minutes.

After quite a time it can come however to a permanent displacement of the zero line.
In case of a shock or after changing a sensor the camera must be readjusted.

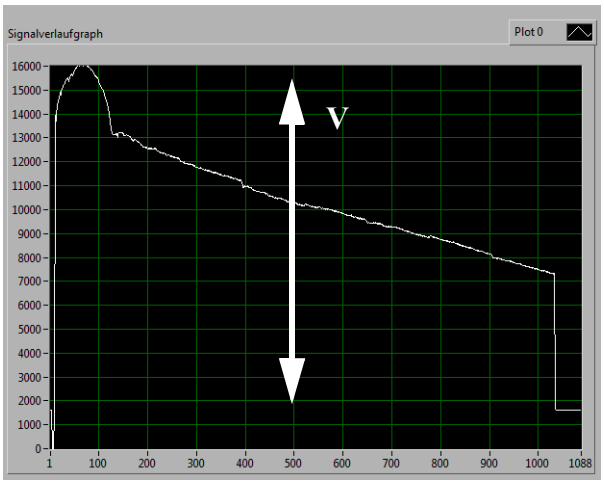
Basic adjustment
There are two main potentiometers in the camera:

Z This potentiometer is for calibrating the zero level.
The sensor should not be illuminated so that the ground level could be adjusted to a value close to zero, but positive(i.e. 500).

V After assessment of the zero line the amplification of the sensor signal can be aligned newly with the help of the potentiometer V. For this purpose, the saturation boundary of the sensor is searched first:
At a slight overexposure of the sensor, i.e.stray light, you can see a maximum level (full well limit of the sensor). You can turn at 1to get this limit level slighting under the value of 65536 (14bit = 16384).

In principle the sensor can be made more sensitive by raising the amplification with V. But by this adjustment also the dynamic range simultaneously is lowered. Therefore the sensitivity should be better varied by extension of the exposure time.

picture-8.1: Camera signal

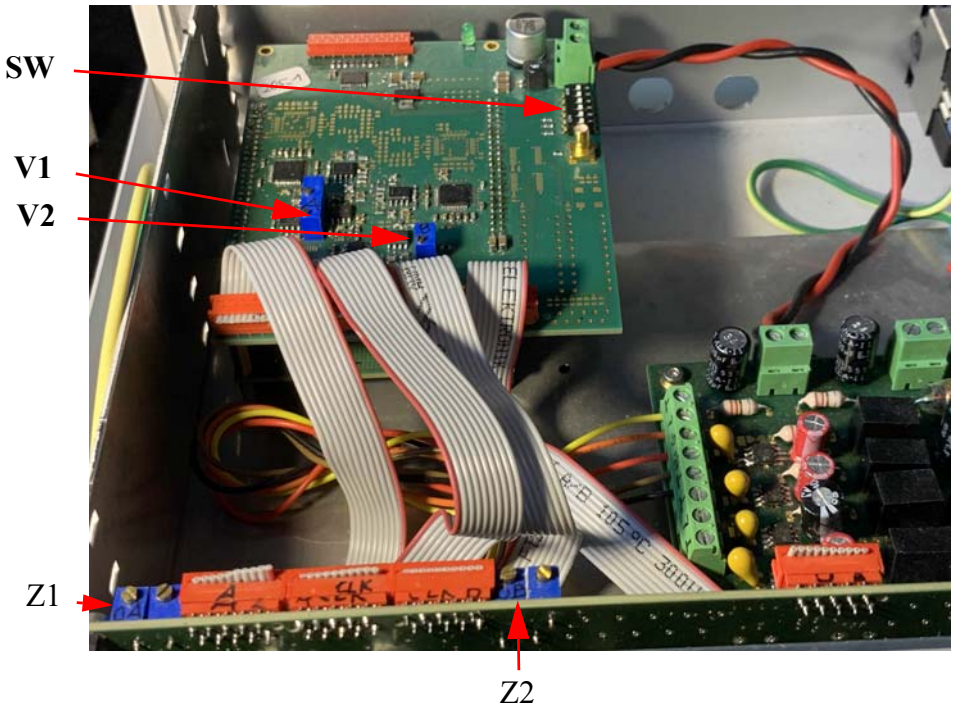


The Z pot moves the complete signal up and down, the V pot aligns the distance between max. signal and zero. As one pot influences the other, alternately alignment is necessary.

8.2 Camera Control FLCC3001

After opening the case some potentiometers can be reached like shown in picture-8.2

picture-8.2: Camera series 3001



The potentiometers are marked with Z1, V1, Z2, V2 and so forth. The Z1 adjusts the zero line of the first CHA, V1 adjusts the amplification of the first channel. In fact the Vn pots should not be misaligned and should be left as is, but the Zn pots are quite sensitive against temperature and mechanical shocks and therefore should be controlled from time to time.

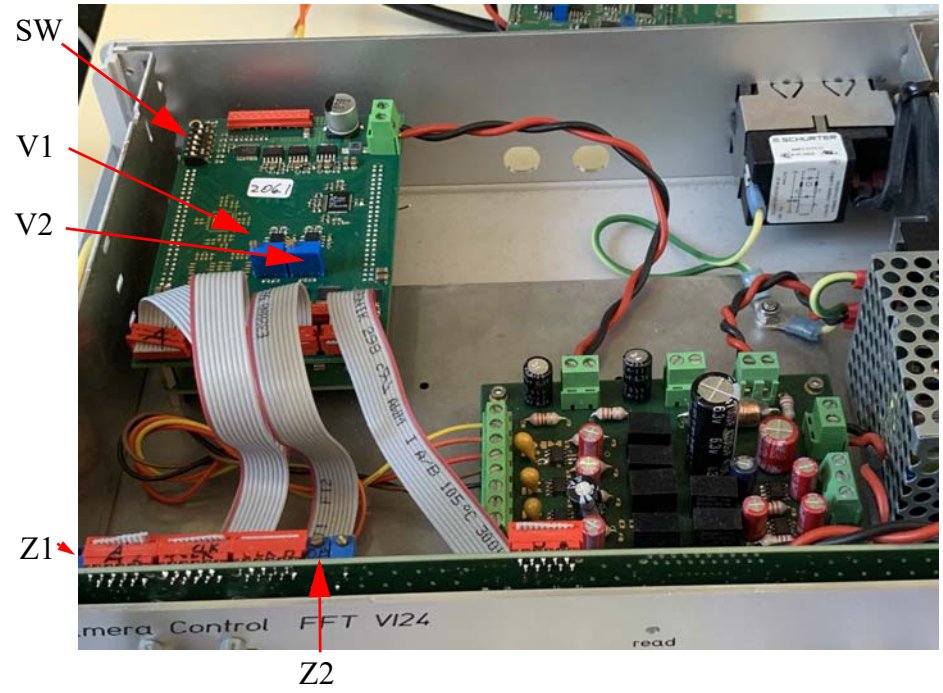
The switch SW has these functios:

SW1:	enable CHA	on
SW2:	enable CHB	on
SW3:	nc	off
SW4:	nc	off
SW5:	testramp on CHA	off
SW6:	testramp on CHB	off

8.3 Camera series 3010

After opening the case some potentiometers can be reached like shown in picture-8.3.

picture-8.3: Camera Control FLCC 3010



The potentiometers are marked with Z1, V1, Z2, V2 and so forth. The Z1 adjusts the zero line of the first CHA, V1 adjusts the amplification of the first channel. In fact the Vn pots should not be misaligned and should be left as is, but the Zn pots are quite sensitive against temperature and mechanical shocks and therefore should be controlled from time to time.

The switch SW has these functios:

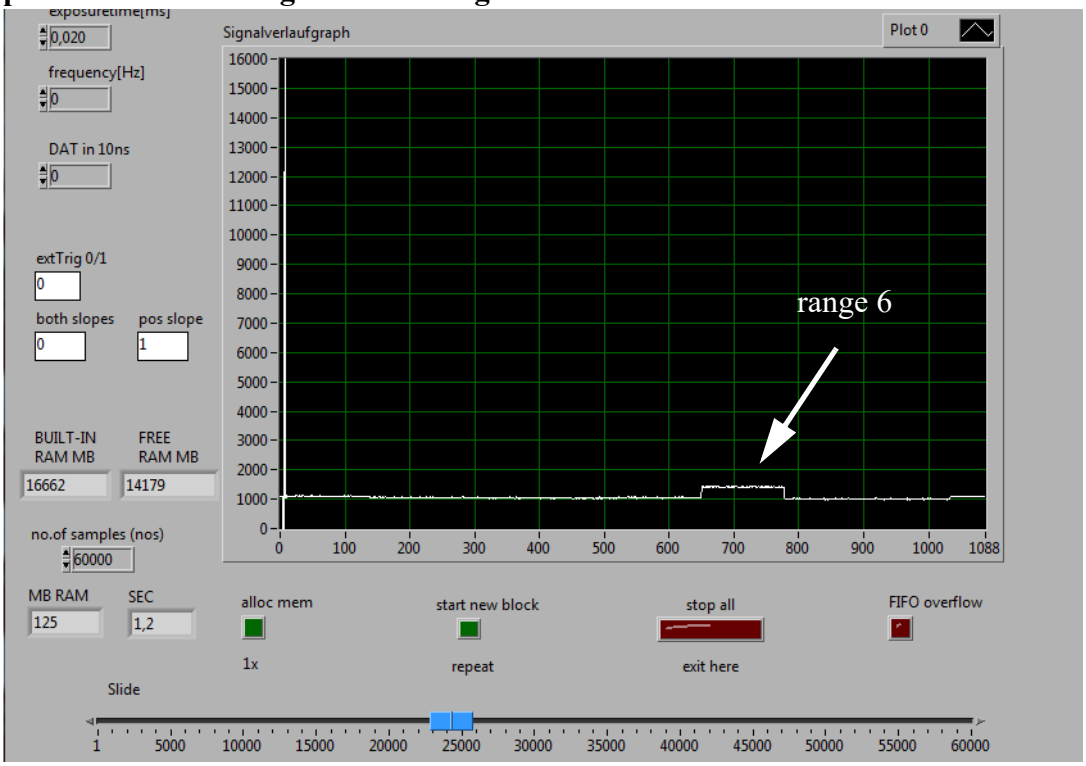
SW1:	enable CHA	on
SW2:	enable CHB	on
SW3:	nc	off
SW4:	nc	off
SW5:	testramp on CHA	off
SW6:	testramp on CHB	off

8.4 Camera series 3030

8.4.1 Alignment of the zero line Camera FL3030

The output signal consists of 8 separate channels which are sampled parallel. Therefore the signal has 8 ranges, each 128 pixel wide. The signal with no light should look like picture-8.4.

picture-8.4: Video signal with no light

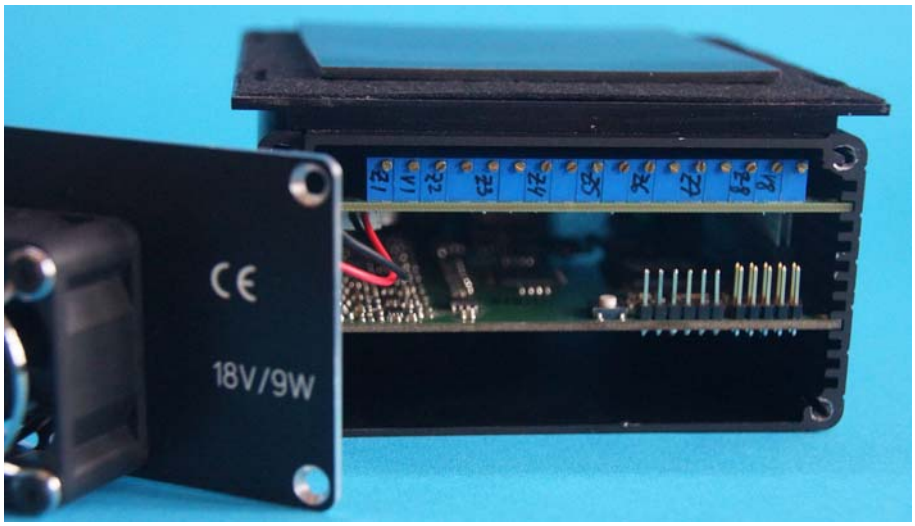


Y-scale in counts of a 14 bit converter, X-scale is pixel number
Here range 6 differs clearly from the main level and can be aligned by Z6.

Be sure to have set the gain by software to value=5 before adjustments (chapter-3.3.2.1). Also allow the camera to warm up by running for 15 minutes.Then cover the sensor that no light is passing. Now each of the 8 zero adjustment potentiometers can be set.

To reach the potentiometers you must open the case on the side of the fan. Carefully remove the plate without pulling the fan cable and without pushing the red OT LED like shown in picture-8.5.

picture-8.5: potentiometer of HS camera



The potentiometers are marked with Z1, V1, Z2, V2 and so forth counting from the left. The Z1 adjusts the zero line of the first pixel range, V1 adjusts the amplification of the first range. In fact the Vn pots should not be misaligned and should be left as is, but the Zn pots are quite sensitive against temperature and mechanical shocks and therefore should be controlled from time to time.

8.4.2 Alignment of the DynamicRange

The alignment is set in factory and usually you do not need to change that, as these values are not very critical.
The sensor has 2 saturation level. If the EC function is not used, the sensors full well level limits the max. signal. If the EC function is used, the saturation level is reduced. This level can be found by a weak saturation of the sensor with DC light (torch light). Standard electric light usually has a 100 Hz fluctuation which leads to heavy flickering signals.
Only the range from zero to ECsat is linear and should be used for the full scale of the AD converter. So the cameras internal gain should be set to gain=5 and the potentiometers V1-V8 are just set to max. signal.

picture-8.6: Adjustment for dynamic range

8.5 Alignment of the Cooled Camera series FLPC

The camera is delivered calibrated. No further adjustment is necessary. Only if the sensor was changed, a new calibration is necessary.

8.5.1 Calibration of the NTC sensor

In the sensor integrated is a NTC resistor. This resistor must be calibrated for the measurement of the temperature:
For adjustments the sensor must be removed and a resistor has to be connected to the pins #7=Gnd and #8=T_{Ist}).

Table 8.1: Calibrating values for temperature calibration

	IR Ha -S or -W series	IR Goodrich	FFT	IR G1147x
0 ºC	13,37 kΩ	16,34 kΩ	28,87 kΩ	32,10 kΩ
-10 ºC	20,87 kΩ	27,70 kΩ	46,68 kΩ	53 kΩ
-20 ºC	33,76 kΩ	48,63 kΩ	78,40 kΩ	88,8 kΩ
-30 ºC	56,82 kΩ	88,94 kΩ	137,40 kΩ	155 kΩ

The resistor value for 0 ºC will be connected and with P5 (see picture-8.7) the temperature display adjusted to 0 V (LED display=0). In the following the resister value for - 20 ºC (-30ºC) is taken and connected and with the help of P6 the temperature display is adjusted

to -20 (-30). Because both adjustments are related, the calibration must iteratively repeated several times.

picture-8.7: Potentiometer for NTC-sensor calibration

8.5.2 Cooling temperature

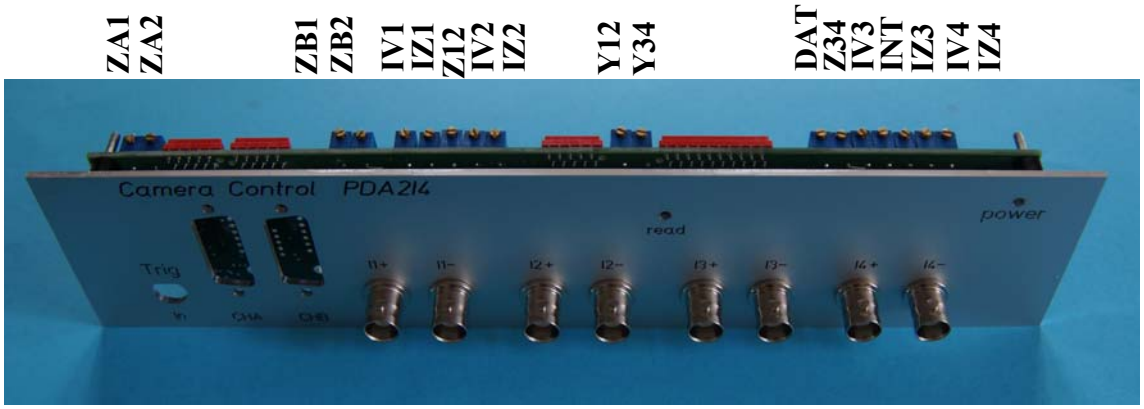
The picture-8.7 shows also the position of the potentiometers (P10-P17 = step 0..7) for the selectable temperature steps. These steps are selected by software and the related potentiometers adjusts the desired temperature. For every step the desired value must be adjusted separately by comparing the temperature display with the programmed step. As the regulation needs time to get the stable endpoint, the display value should not be reeded too short after changing the potentiometer position.
Potentiometer P10 is not assembled!

8.6 Camera Control FLIO

8.6.1 Top side PCB Potentiometers

Located on the front panel are the potentiometers for the alignment of the signal levels. They can be reached after opening the case.

picture-8.8: Locations of the potentiometer of front panel



ZA1: Zero offset of camera signal CHA
ZA2: Zero offset of camera signal C
ZA1: Zero offset of camera signal CHA
ZA2: Zero offset of camera signal C

ZA1: Zero offset of camera signal CHA
ZA2: Zero offset of camera signal CHA 2nd channel (only IR512)
ZB1: Zero offset of camera signal CHB
ZB2: Zero offset of camera signal CHB 2nd channel (only IR512)
IZ1: Zero offset of integrator signal CH1
IZ2: Zero offset of integrator signal CH2
IZ3: Zero offset of integrator signal CH3
IZ4: Zero offset of integrator signal CH4
Y12: Zero offset of integrator signal CH1 and CH2
Y34: Zero offset of integrator signal CH3 and CH4
INT: tint = integration time: when high, the integrator is active, low = hold
DAT: dat = delay after trigger - only for Cam Control trigger input
IV1: full scale of integrator signal PD1 CHA
IV2: full scale of integrator signal PD2 CHA
IV3: full scale of integrator signal PD3 CHB
IV4: full scale of integrator signal PD4 CHB
Z12: Zero offset of voltage signal V1/2
Z34: Zero offset of voltage signal V3/4

With the specific potentiometers each signal can be aligned.

After the zero levels are all set, the full scale integrators should be set:

Apply a 1.6V DC level to the ±inputs. Check that the PD output signal (I1..4) has now a constant 4.5V (2.25V if 50Ω Input) level. With an INT signal of 20µs the Pixel values of the tested channel should have a little less then the maximum value. This is aligned with IV1 to 4. With changing IVn the zero is also changing, so realign IZn too.
Be sure to have the INT signal triggered (external or internal ->chapter-7.3.6)!

8.7 IR Version

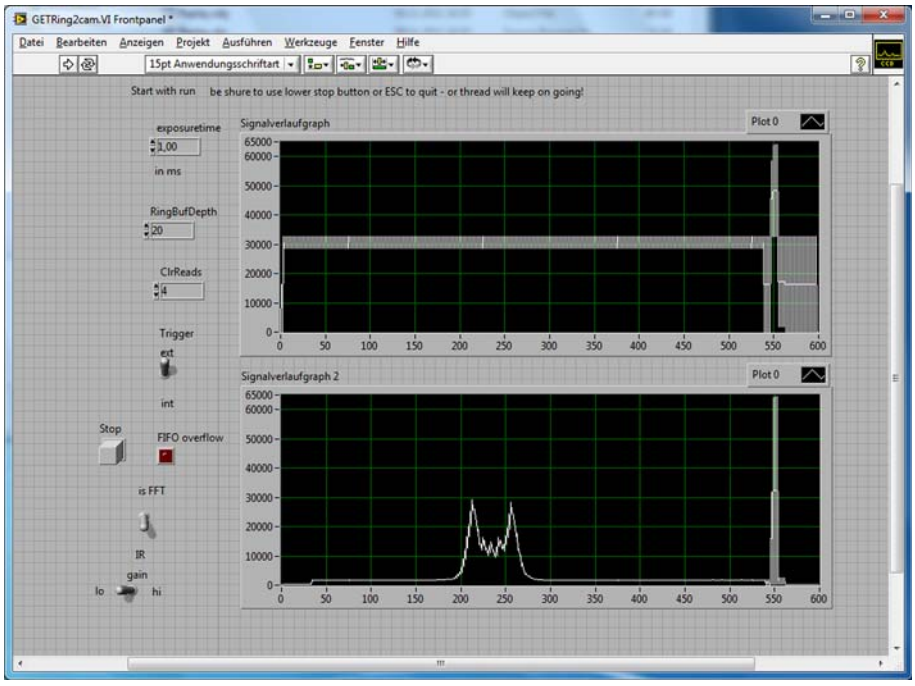
The IR sensor with 512 pixel consists of 2 completely separated channels, one for the even and one for the odd pixel. Therefore the Double Line Camera Control has 4 analog paths with 4 A/D converter sampling parallel.
The 256 pixel sensor has only one channel and acts as a standard sensor.

8.7.1 Even and odd asymmetry

Because of the double channel structure of the 512 pixel IR sensors, the signal of the even and odd pixels differ a little bit. Besides that the signals can be adjusted independently as shown in chapter-8.7.4, they are not equal in offset and amplification. Also their drift in time and temperature differs. For that reason a slight difference is seen in the signal. As this difference is static, it can be eliminated by mathematical corrections.

In picture-8.9 a double line system is shown, with only one IR sensor board connected to the lower channel. At pixel 550 also a signal from an external photo diode is applied. This signal can be used, even if the 2nd sensor is not used (see chapter-8.7.2).

picture-8.9: Labview plot of IR double line system

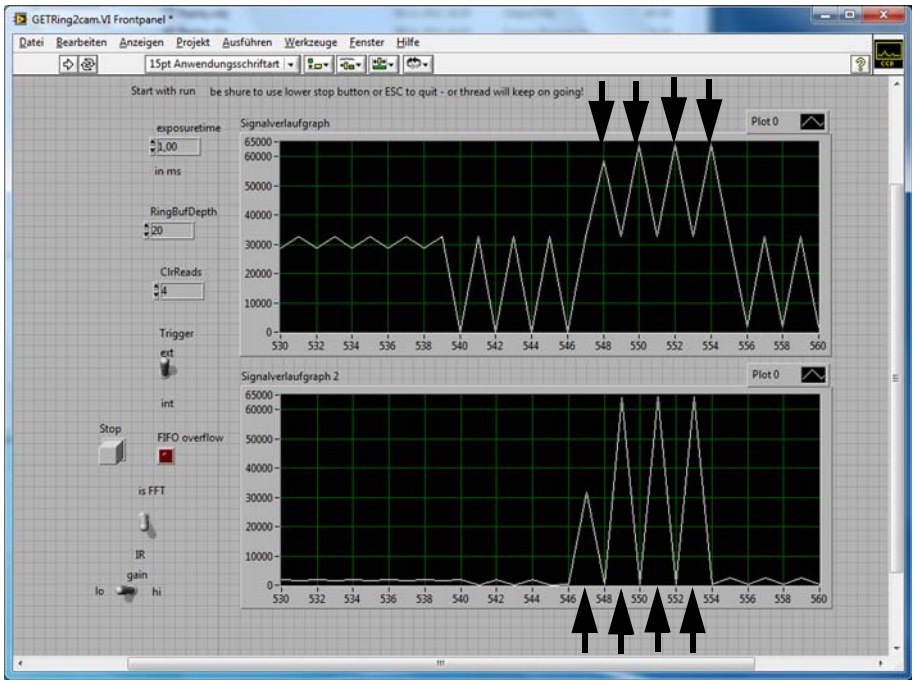


shown: Laser spot with only one sensor board connected.

8.7.2 Signal of the external Photo Diodes

Even if one sensor channel is not used, the external photo diodes are still switched to the data stream. If a 512 pixel sensor with even/odd data path is used, the diode signal is switched to one path only. So every 2nd value has no meaning here.

picture-8.10: Photo diode signal impact on IR version



valid signal

shown is a signal of two external photo diodes. One in channel A and one in channel B. Only each 2nd value is valid. The first value is not stable and should not be used. The 3 other signals could be averaged.
To find the values, apply a 2V DC signal to the integrator inputs with INT set as shown in picture-7.12.

8.7.3 Special Features of the IR Sensor

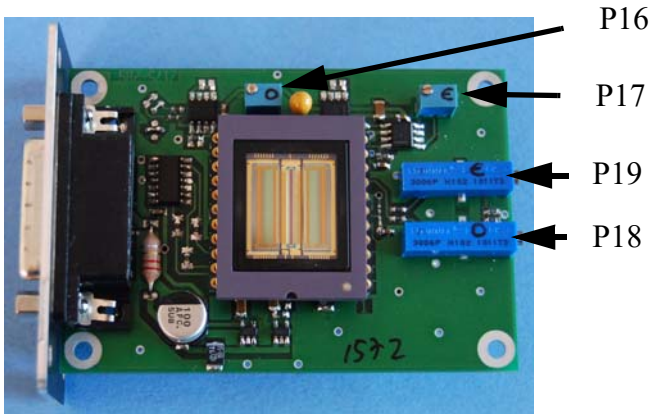
hi / lo gain
The IR sensor has a build in switch for changing the internal Capacitor. This changes the amplification by factor 10. This function is implemented with the VON signal of the interface. This signal can be set by the V_On and V_Off Function of BOARD.C

IR/FFT
The switchable Camera Control version is able to run up to 2 VIS sensor boards and alternatively 2 IR sensor boards. Therefore a switch on the front panel has to be set accordingly (picture-7.1). Also the software must set the flags of the TOREG register . Please have a look at chapter-6.2.3.12 for details. The software has 3 functions concerning this function: IS_PDA, IS_FFT and RsTOREG.
To avoid setting both flags, RsTOREG should be called before any set function.

8.7.4 Alignment of the IR Sensor Board

Also the sensor board has setup shown in picture-8.11.

picture-8.11: IR Sensor board



P16: full scale of camera signal odd
P17: full scale of camera signal even
P18: zero of camera signal odd
P19: zero of camera signal even

8.8 Changing the analogue range of DAT and INT

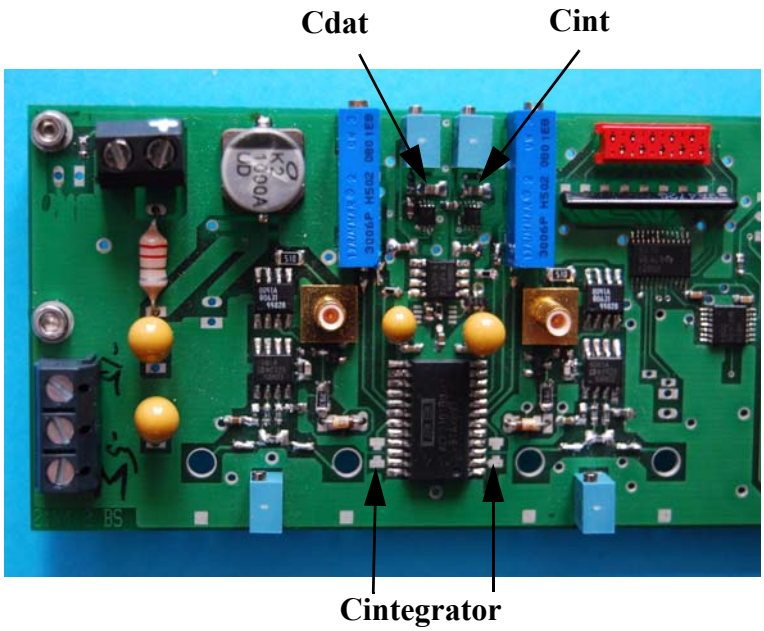
The monostable multi vibrator which sets the delay after trigger (DAT) and the integrating window (CINT) can be changed if necessary. The timing value is t = R * Cint. R is the potentiometer with 20k¾ + 1k¾ resistor and Cint is default 4.7nF. With these values the range is given:

default:
if Cint=4n7 delay range = 6-100µs

if Cint=22n the range is 8-450µs
if Cint=1n5 the range is 2-30µs

The SMD capacitor is mounted at the pcb as shown in picture-8.12. The Cs are mounted directly on the surface to guarantee very low Jitter. If they need to be replaced, a person with experience should do that, as the neighbor parts should not be damaged.

picture-8.12: Location of timing Capacitors



8.9 Changing the photo diode integrators range

It is also possible to change the range of the build in integrator of type ACF2101 (BB/TI) These ICs have a build in capacitor of 100pF. In some cases it might be necessary to change that. In those cases the empty Cintegrator pads (see picture-8.12)can be used. If so, a small connection between pin #2 , #3 and #22 , #23 must be removed.

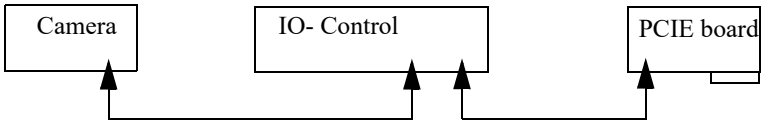
9 IO- Control FLIO

For time synchronous measurement of additional signals we have made an IO- Control. Here some data signals can be inserted in the data stream from camera to PC. The signals are measured exactly when the camera read is done. This is in example useful for signals of a delay stage or additional photo diodes. The IO-Control is available in different versions. P8 stands for 8 pulse outputs, V4 or 8 for voltage inputs and C2 for delay stage inputs.
The IO-Control cannot be used without a camera. The Camera - PCIE board communication must have been established.

picture-9.1: IO- Control front panel

This device is actually a pulse generator and a voltage Input sampler.
The fiber link should be connected in between the camera and the PC.

picture-9.2: wiring of the IO- Controls fiber link



picture-9.3: wiring of the IO- Control

If both fiber links are setup correctly, the LEDs pc-up and cam-up are on.
By problems try to reconnect or swap the cables.

9.1 Registers of the IO- Control

The IO- Control has 16 registers to setup the IO-Control.
To access and to differentiate between the Camera registers and the IO-Control registers, the function SendFLCam has the parameter maddr (master address). To access the IO_-Control, maddr must be set to 3.

The data width of every register is 16bit.

Table 9.1: Registers of IO- Control

ADR	reg	function
0	CTRLIO	Ctrl reg
1	TO2	delay of O2
2	DO2	duration of O2
3	TO3	delay of O3
4	DO3	duration of O3
5	TO4	delay of O4
6	DO4	duration of O4
7	TO5	delay of O5
8	DO5	duration of O5
9	TO6	delay of O6
10	DO6	duration of O6
11	TO7	delay of O7
12	DO7	duration of O7
13	TO8	delay of O8
14	DO8	duration of O8
15	TM0L	frequency of T0 generator
16	TM0H	frequency of T0 generator

9.2 Pulse Generator O8

The pulse generator runs independently of the camera function. It can be programmed to generate a stable main trigger for a complete timing sequence of several devices.
The pulses are generated as long as the power is on.

It has 8 outputs: O1..O8.
The Signal is 1.5V on 50Ω (3V if not terminated).

O1 is the TM0 main clock generator, the others have their own adjustable delay TO and duration DO relative to T0.

O2 up to O8 are 7 delay generator channels.

9.2.1 CTRLIO register

Bit0 of this register resets all pulse generator registers.

9.2.2 TOx registers

These registers set the delay relative to the T0 generators positive slope.
The time unit is 5ns, so the range is: 0..65536 -> 7ns .. 328µs.

9.2.3 DOx registers

These registers set the duration of each pulse.
The time unit is 5ns, so the range is: 0..65536 -> 0ns .. 328µs.
If set to 0, no pulse is generated:

9.2.4 T0ML and TM0H registers

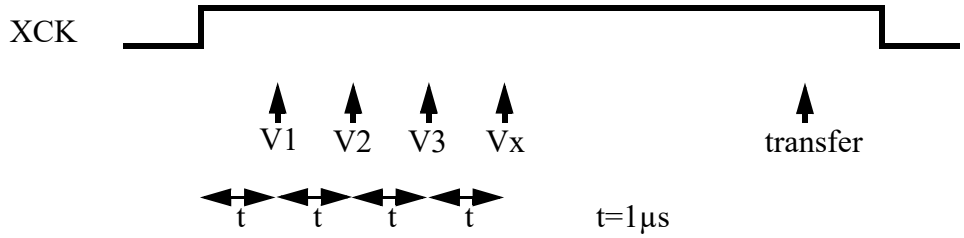
These registers set the master generators T0 frequency.
Here the TM0H is the high word and TM0L is the low word of the time generator.
A zero sets the generator to 100MHz. The pulse time can be set in 10ns steps. So a value of 100 sets a 1MHz frequency.

The time unit is 10ns,
so the range of TM0L is: 0..65536 -> 10ns .. 65µs -> 100MHz .. 1.5 kHz.
for lower frequencies TM0H must be >0.

9.3 Voltage Inputs V4 or V8

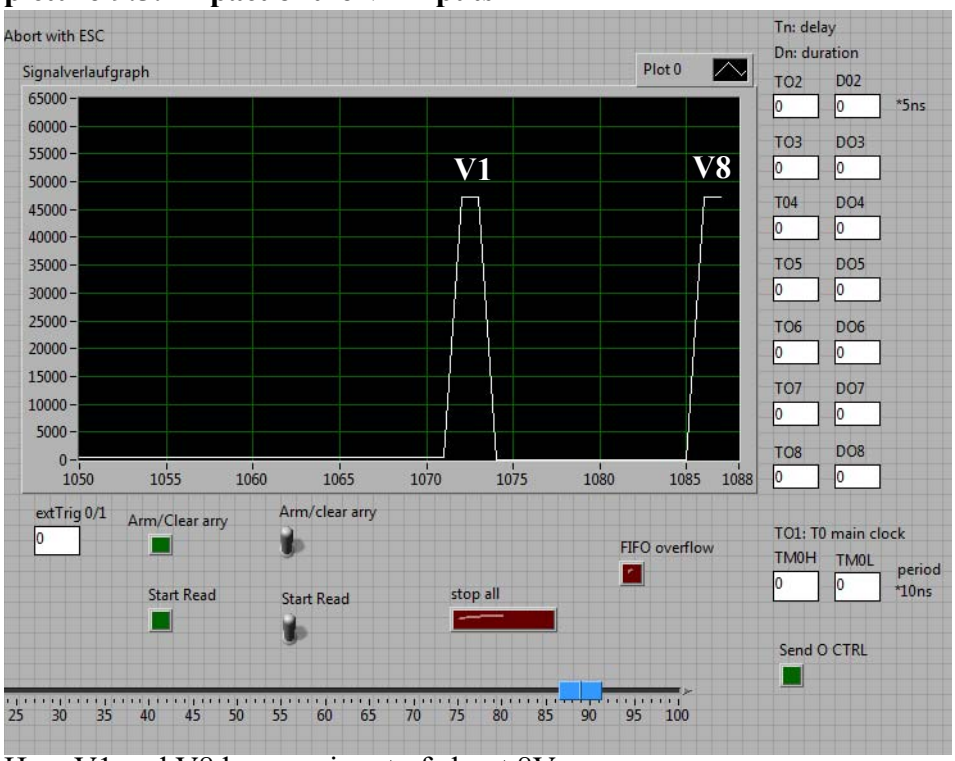
The voltage input function can sample up to 8 signals with a 16bit AD- converter. The input range is 0..10V what leads to values of up to 65536. This is different to the 14bit AD values of the camera which goes up to 4096!
This conversion is syncronously to the camera read cycle. When XCK goes high, the 8 inputs are sampled with 1µs distance. The sample time can be monitored on a scope with the XCK (SEL) signal on the rear. After the sample the values are kept in memory until the last camera values are transferred. Then these 8 values are appended to the stream as if they are additional pixel values.

picture-9.4: Trigger for AD inputs



To test the function, just apply a constant voltage to V1.. V8 and start the measure program. You should see the signal at the last pixels (see picture-9.5). Each value is transferred twice, so you get 2 equal values per channel. V1@pix=1072 and 1073 and so forth.

picture-9.5: Impact of the Vx inputs



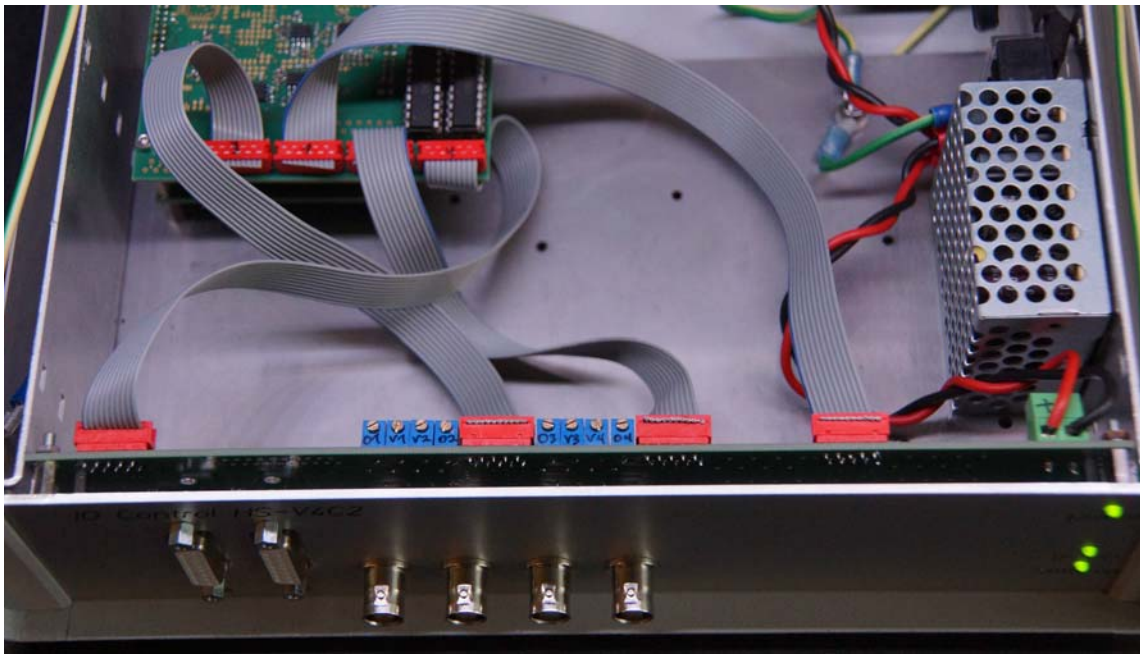
Here V1 and V8 have an input of about 8V.

9.3.1 Alignment for Voltage Input

The 8 Voltage inputs can be aligned individualy.

Apply a 10V DC Signal to the BNC input and align the 16bit AD value of 65000 with the potentiometers V1 to V8.
The zero values cannot be changed..

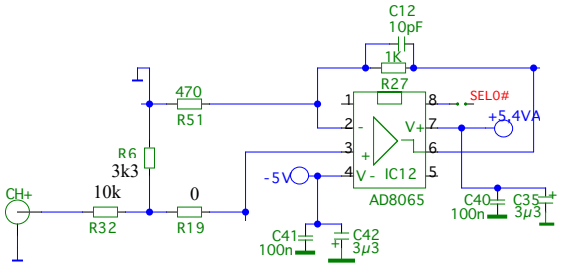
picture-9.6: Potentiometers



9.3.2 Voltage Input Characteristics

The voltage input range is 0..10V with an Input resistance of 13kΩ.

picture-9.7: Voltage Input Schematic

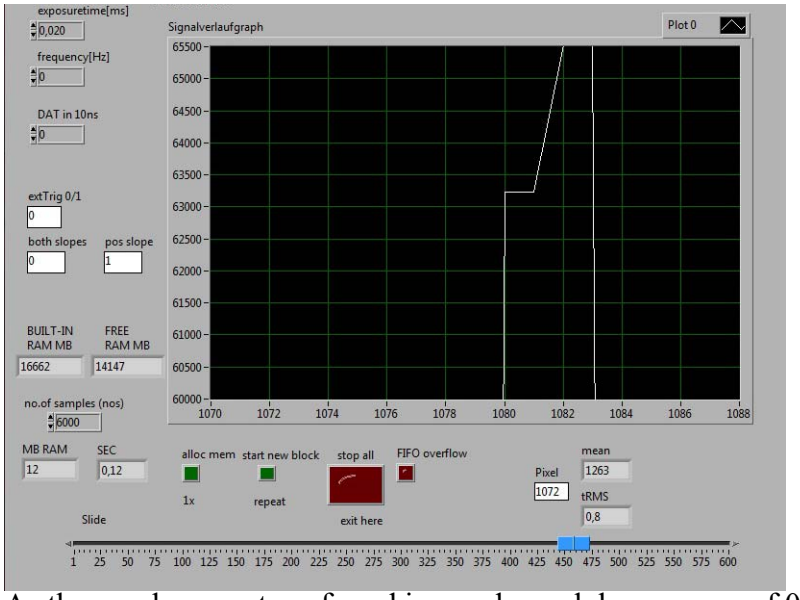


9.4 Counter Input C2

For keeping track of a delay stage 2 counter inputs are available. Here the position, means the counter stage is red when the camera data read is done. Two counter channels are implemented with 32bit resolution: CHA and CHB. At the end of the transfer these values are stored @ pixel

= 1080, 1081 CHA low word
= 1082, 1083 CHA high word
= 1084, 1085 CHB low word
= 1086, 1087 CHB high word

Screenshot of counter value



As these values are transferred in words, each has a range of 0..65535, where the 14bit values of the camera values have a range of 0.. 16384.

The interface can be configured as LVDS or „open collector“ version.

9.4.1 LVDS interface

The PI servo controller C-863 uses an RS-422 LVDS signal to decode the position. Here our IO-Control can be configured to decode that signal. The connection between controller and motor must be interrupted and the signal is looped through the 2 SubD15 plugs on the front panel.

Please ask for that option if needed.

9.4.2 Open collector input for TTL stepper motor controller

The newport motor controller XPS-Q8 has an interface AquadB which delivers the counter signals and expects an pull-up resistor of 470Ω, which is implemented in our electronic.
The LEMO connector FGG0B306 must be connected to the SubD-15 of the IO_Control as Table 9.2 on page 90 shows.

Table 9.2: Connection to PCO connector of XPS-Q8 controller

signal	AquadB	SubD	
+5VL	1	4	
A1	2	15	470Ω to +5VL
B1	3	14	470Ω to +5VL
B2	4	12	470Ω to +5VL
A2	5	13	470Ω to +5VL
GND	6	10	

9.5 Technical Data of IO-Control

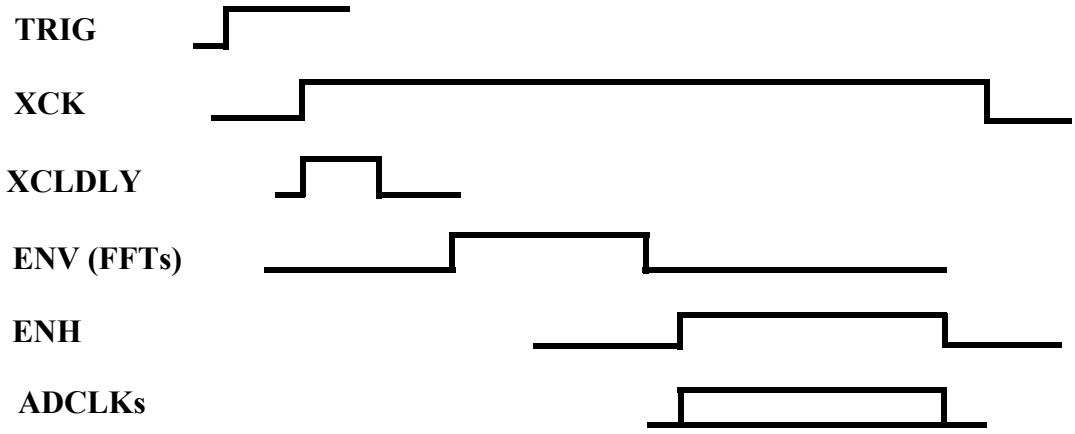
Main Power supply:	100-240V 350mA 50/60Hz
Max. input Power:	8W
Internal power supply(MW RS-15-5):	1.2A (max. 3A) @5V
Dimensions:	280 x 220 x 65 (L x W x H in mm)
Weight:	2.3 kg
data transfer rate :	250MByte/sec -> 2.5Gbit
max. line rate (1088 pixel):	50 kHz - even with 2 cameras parallel.

SFP module 2.5 GBit type Finisar 370-5211-01 FTRJ-8519A7D-2.5 850nm
fiber connector type: Duplex LC
fiber length up to 500m on 50/125µ or 300m on 62.5/125µm MMF
The standard camera fiber cable length is 3 m.

10 Technical Specifications Series FL

Our cameras are controlled with several control signals. The main control signal is the XCK- signal (eXposure ClocK). This signal is high during the read phase of the sensor. When this signal is output on the SMB plug "O" of the PCIE board, it can be used to monitor the timing of the camera on a scope.

picture-10.1: XCK timing



ENV	enable vertical clocks (during this time the vertical clocks (vclk) are on.
ENH	enable horizontal clocks
ADCLK	analog digital converter clocks = horizontal clocks (hclk)

10.1 Camera specifications FLCC30xx

weight FLCC control	2,2 kg
size	280 x 220 x 70 mm
input	100-220V 50/60 Hz
Type of power supply	RS-25-5
Fuse (T=slow blow)	T1A / 220V

SFP module type Finisar 370-5211-01 FTRJ-8519A7D-2.5 850nm
fiber connector type: Duplex LC
fiber length up to 500m on 50/125µ or 300m on 62.5/125µm MMF
The standard camera fiber cable length is 5m.

data transfer rate :	250MByte/sec
max. line rate:	50 kHz

10.2 Camera specifications FLCC3001

Power consumption:	13W
running @1kHz	2000mA @5V
AD clk	2.5 MHZ
noise@64bit AD (0..65536)	trms=< 6 counts
FPGA	P205

The camera timing for the FFT sensor with 1024 pixel is:

picture-10.2: Timing of FFT sensor

Table 10.1: Timing and max. line rate of series 3001

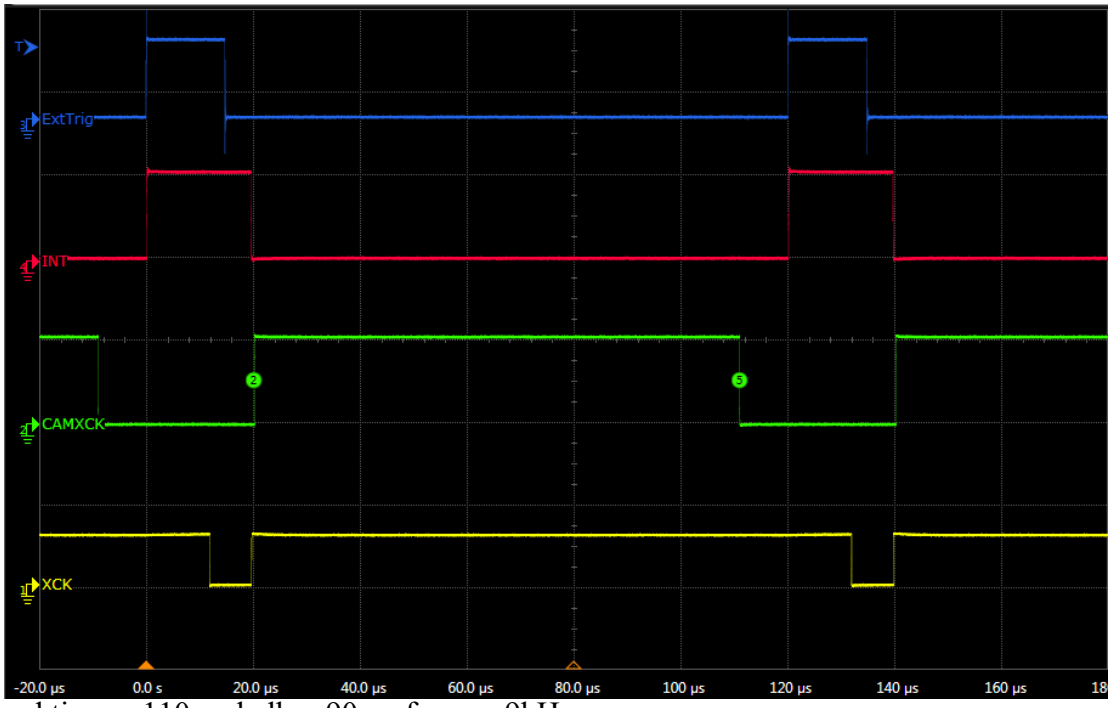
sensor	pixel	vlines	vclks	XCK	mlr.	noise
S838x-128Q	128	1	0	80 µs	12 kHz	<4 cnts
S838x-512Q	512	1	0	240 µs	4 kHz	<4 cnts
S838x-1024Q	1024	1	0	450µs	2 kHz	<4 cnts
S7030-0906	512	64	200µs	440 µs	2.2 kHz	<5 cnts
S7030-1006	1024	64	200µs	650 µs	1.5 kHz	<5 cnts
S7030-1007	1024	128	400µs	850 µs	1.1 kHz	<5 cnts
S7030-1007	area mode	128x1	BON =	60 ms	16 Hz	<5 cnts
G11608-256	256	1	0	68 µs	8 kHz	<4 cnts
G11608-512	512	1	0	121 µs	8 kHz	<4 cnts
G11608-512	512	1	0	93 µs	10 kHz	<8 cnts

mlr: max. line rate, XCK: complete sensor read time (vclks+hclks).

10.3 Camera specifications FLCC3010

Power consumption:	12 W
running @8kHz	1800mA @5V
AD clk	12 MHZ
noise@16bit AD (0..65536)	trms=< 12 counts
FPGA	P206

picture-10.3: Timing 8kHz camera with 1024 pixel



read time = 110µs, hclk = 90µs, fmax = 9kHz

10.4 Camera specifications FLC3030

Power consumption:	13W
not running	490mA @18V
running @50kHz	640mA @18V

power supply: Intertek 0055A-H 100-240V 800mA 50/60Hz

inner pin = plus	select = 18V , max. 2,1A
AD clk	20 MHZ
noise@14bit AD (0..16 384)	trms=< 6 counts @ gain=5
FPGA	P197
Dimensions:	125 x 104 x 54 (L x W x H in mm)
Weight:	460 g

10.5 Camera specifications FLPC3001

external power input:	max 3800 mA @6V = 24W
inner pin = plus	select = 6V , max. 5A
power supply:	HNP 60 UNI 100-240V 50/60Hz
FPGA	P208

Dimensions:	120 x 100 x 95(L x W x H in mm)
Weight:	1 kg

10.6 Technical Data of the Camera Control FLIO3000

Power consumption (max.):	9 W
Input voltage	110-250V/50-60Hz
Fuse (T=slow blow)	T1A / 220V
Type of power supply	RS-25-5
FPGA	P207
weight FLCC control	2,2 kg
size	280 x 220 x 70 mm

10.7 Integrator

10.7.1 DTrig (digital trigger)

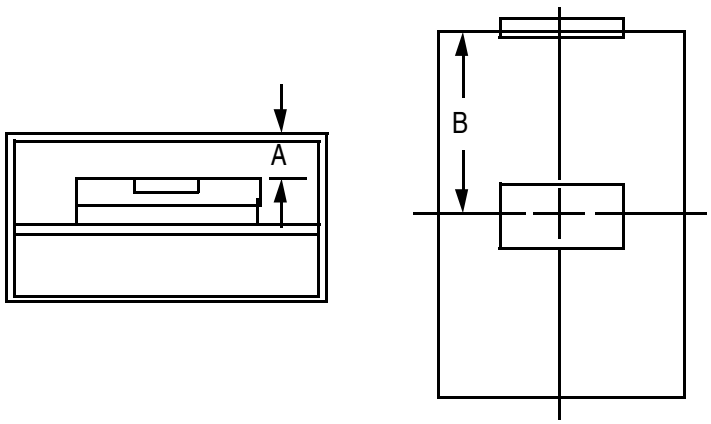
delay after XCK goes high	80ns
Integrator signal - INT (P5) Cint = 4n7	
int range =	6-100µs (default: 20µs)

10.7.2 ATrig (analog trigger)

ATrig In level	0-5V (TTL)
ATrig In restistance	1k5 to +5V
can be used with wire ored by connecting to GND	
no DAT, delay after trigger	70ns
with DAT, delay after trigger	6-100µs
Integrator signal - INT (P5) Cint = 4n7	
int range =	6-100µs
default =	20 µs

10.8 Sensor Head Size

picture-10.4: Case Size of Sensor Adapter



10.9 Technical Data of the FFT single channel sensor head- S7030

size with case	85x65x30 mm
pcb board size (2152)	78x55 mm

Sensor Distance A = 5.5 mm (+ inner sensor window <-> chip: 3.2mm),
B = center

10.10 Technical Data of the PDA double channel sensor head

size with case	85x65x30 mm
pcb board size (2128)	78x55 mm

sensor distance A = 6.3mm (+ inner sensor window <-> chip: 1.3mm),

one sensor version
B = center

double line version
sensor one B = center, sensor two B = center + 13.0 mm (distance mid - mid)

10.11 Technical Data of PD Amplifier

size	110x60x30 mm
Voltage (min.)	7V (6V)
Current	20 mA

10.12 Sensor specifications

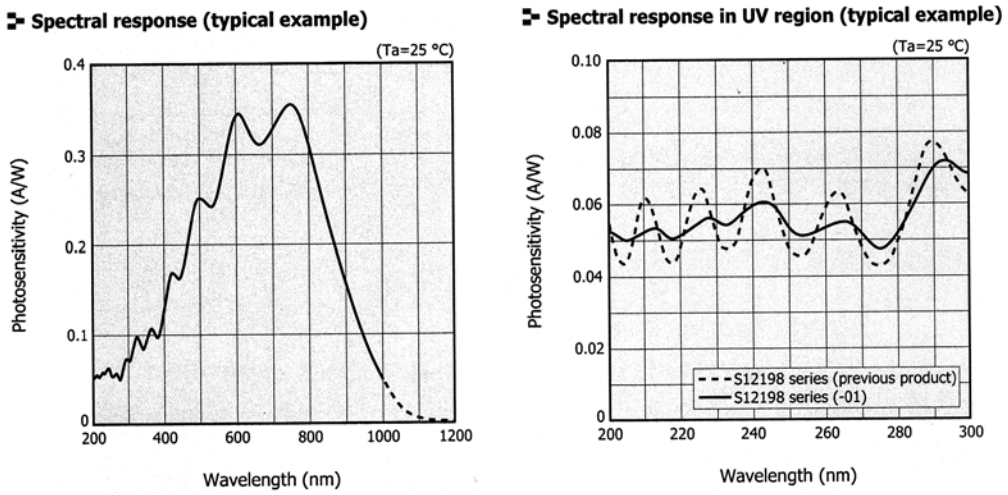
10.12.1 MID sensor S12198

The cameras are available with CMOS sensors from Hamamatsu (Ha):
Sensor S12198 with 1024 Pixel

active length:	25.6 mm
max. exposure time:	approx. 0.5sec. (25°C)
pixel size:	25 x 500 μm^2
Dyn. Range:	$5000:1_{rms}$
E_{SAT}(full well):	20 Me-
k	0.13 µV/e-
spectral range:	ca. 0,2 - 1,0 µm
Pclk	10 MHz

*

picture-10.5: Spectral response of Ha sensor S12198



taken from Hamamatsu data sheet S12198.

10.12.2 HS sensors S11490

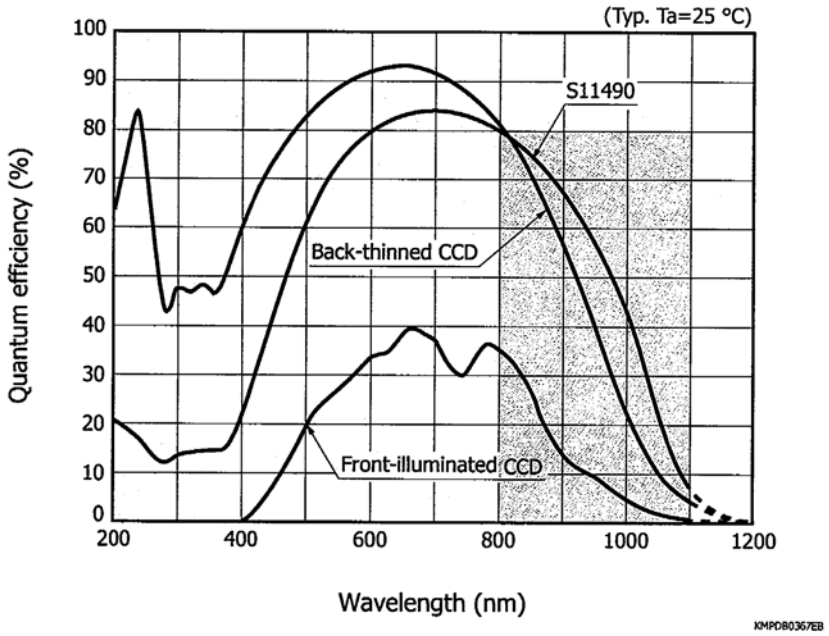
The cameras are available with CCD-line scan sensors from Hamamatsu (Ha):

Sensor S11490 with 1024 Pixel (Ha)	
active length:	24.576 mm
max. exposure time:	approx. 0.5sec. (25°C)
pixel size:	24 x 500 µm^2
Dyn. Range:	5000:1$_{rms}$
E_{SAT}(full well):	500000 e-
k	5 µV/e-
spectral range:	ca. 0,32 - 1,1 µm
Pclk	30 MHz

*

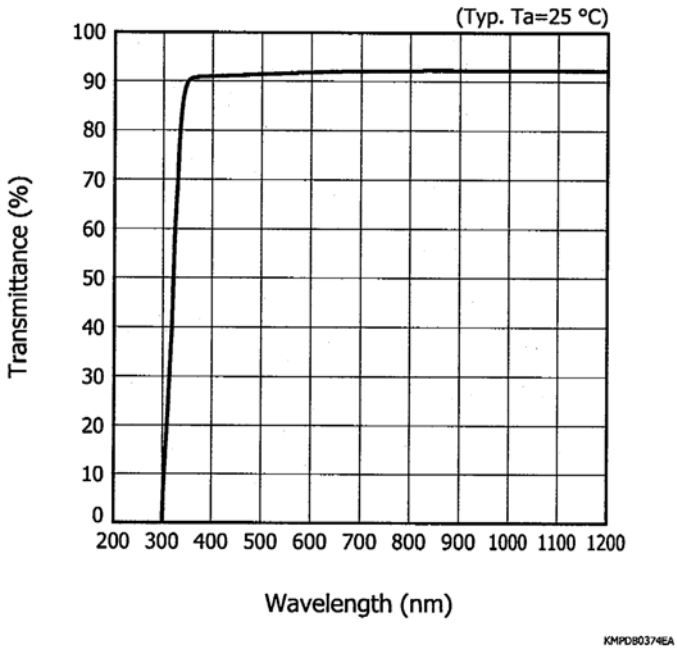
picture-10.6: Spectral response of the Ha- Sensor S11490(lin- Scale)

Spectral response (without window)*17



*17: Spectral response with borosilicate glass is decreased according to the spectral transmittance characteristics of

Spectral transmittance characteristics of window material



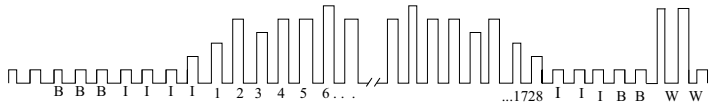
* taken from data sheet Hamamatsu S11490

10.13 Signals

10.13.1 Video signal

The video signal output of the line sensor contains additional informations which are saved to each scan.

picture-10.7: Video signal



Beside the active pixel signal it can contain additional elements (I: isolation, B: black reference) which can be used for additional data savings in every scan (ww).

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Table 10.2: Pixel of sensor signal S11490

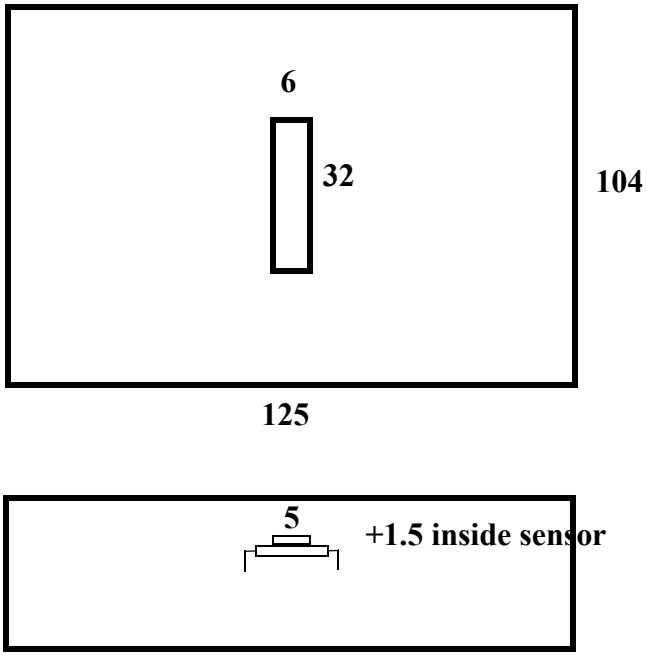
signal	pixel index	HA S11490	HA S12198
I			
shutter state & block cnt high	4	4	4
block cnt low	5	5	5
scan cnt high	6	6	6
scan cnt low	7	7	7
1st sensor pixel	1	11	16
last active pixel	1024	1034	1039
dark level		1035-1051	1040-1050
IO1	1061-1067	1052-1067	1052-1067
IO2	1078-1084	1069-1084	1069-1084

IO1: first impact of IO-Control (pixel index shows the usable range).
IO2: 2nd impact of IO-Control (pixel index shows the usable range).

10.14 Dimensions

picture-10.8: Camera Dimensions series 3030

All dimensions in mm



focal distance from outer case rim: 6.5 mm

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A
additional shutter state input 43
Area Mode 29
B
Binning Mode 29
BLOCKINDEX 56
BLOCKS 56
C
CAMCNT 57
CCD sensor 5
Chopper 8
chopper 42, 43
D
DAT 52
Dimensions 100
divider 53
DLLReadFFLoop 36
DMA 37
DMABUFSIZEINSCANS 56
DMASPERINTERRUPT 56
DOS- software 9
DREQ 37
driver install 13
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E
EC 30, 32, 52
EC fine adjust 54
ECREG 52
electrons 28
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Exposure Control 32, 52
external trigger 8, 11, 42
F
FFT sensor 6, 29, 92
first pixel 43
FLCC 21
FLIO 22
FLPC 21
G
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ID Registers 59
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IO- Control 84
IR sensor 34
IRQREG 55
J
Jitter of external Input 59
L
Labview 36
LED off 18
M
MSHUT 30
N
NOS 56
O
ot LED 9
P
Parallel exposure 10
partial line binning 57
potentiometers 72
Q
QE 28
R
range of interest 57
ReadL 48
Register CtrlA 48
Register CtrlB 49
Register CtrlC 50
Register FIFOCNT 51
Register PIXREG 51
Register VCLKCNT 51
Register VCLKCTRL 51
Register VCLKFREQ 52
Register XCK 50
Register XCKCNT 50
RegisterFF_FLAGS 51
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ROI Mode 29
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TimerOn 50
Trigger Options Register 53
Trigger Select 22
U
up LED 9
V
Vendor ID 59
W
Win software description 9
WriteL 48
X
XCKDELAY 58
Z
zero line 75

