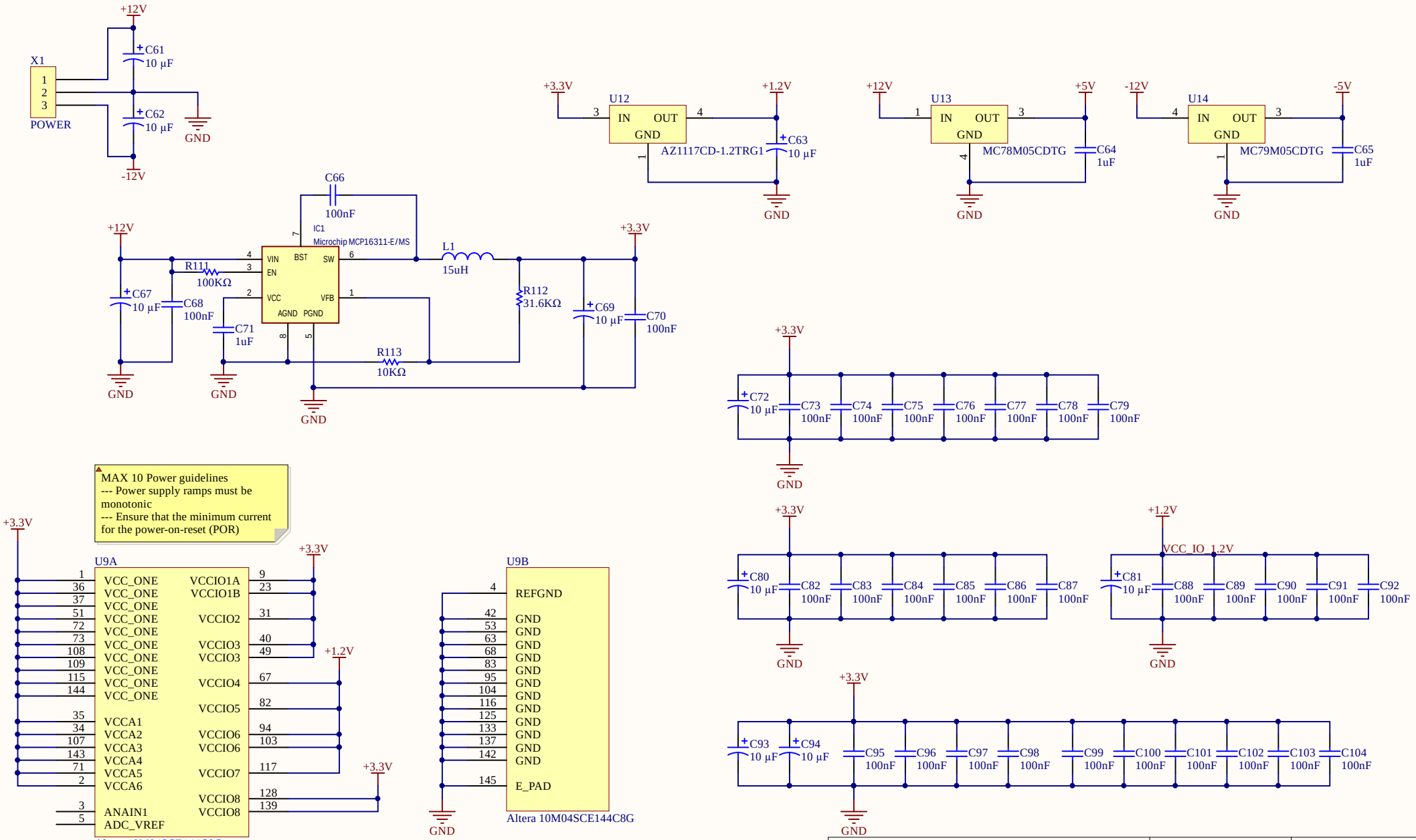
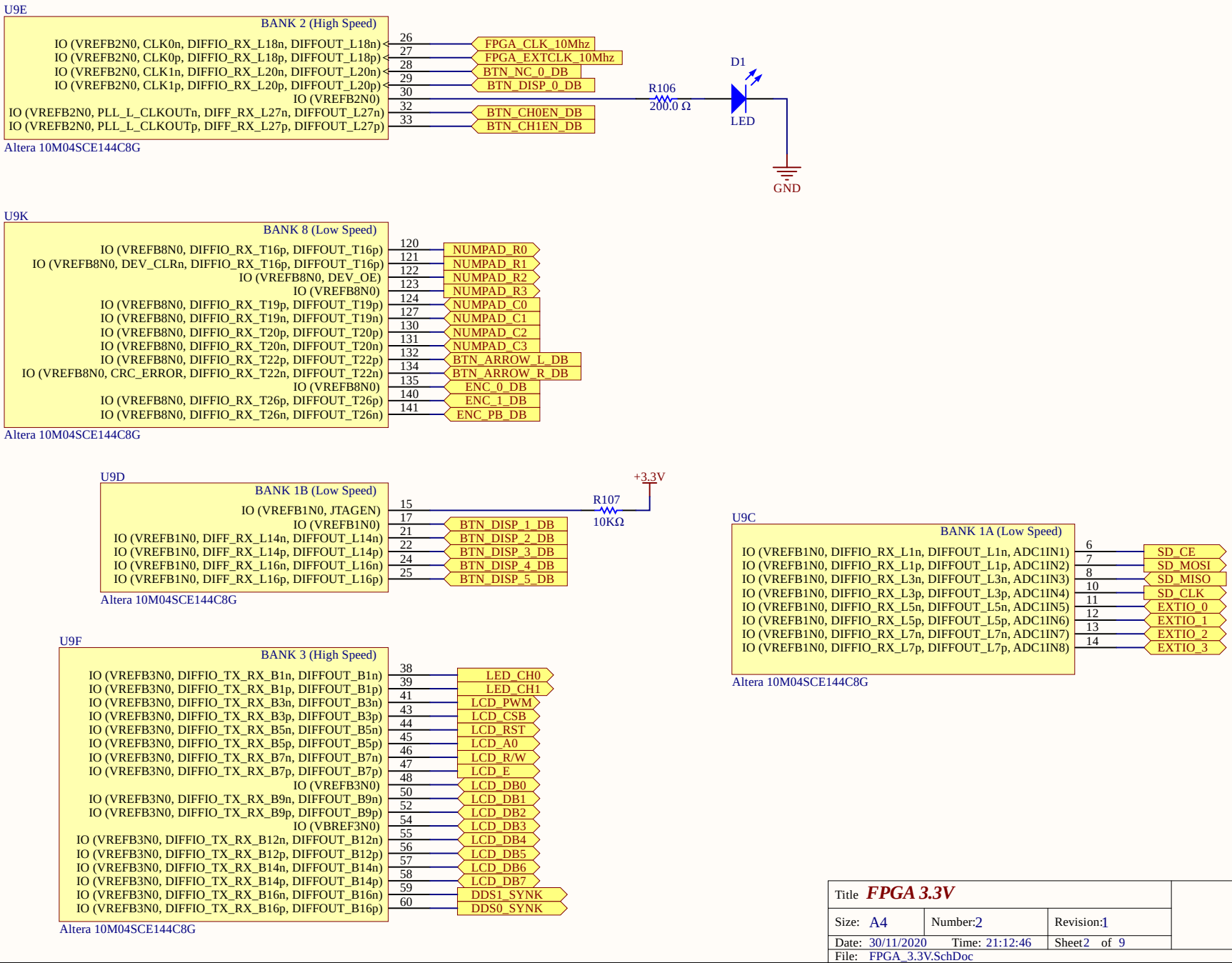
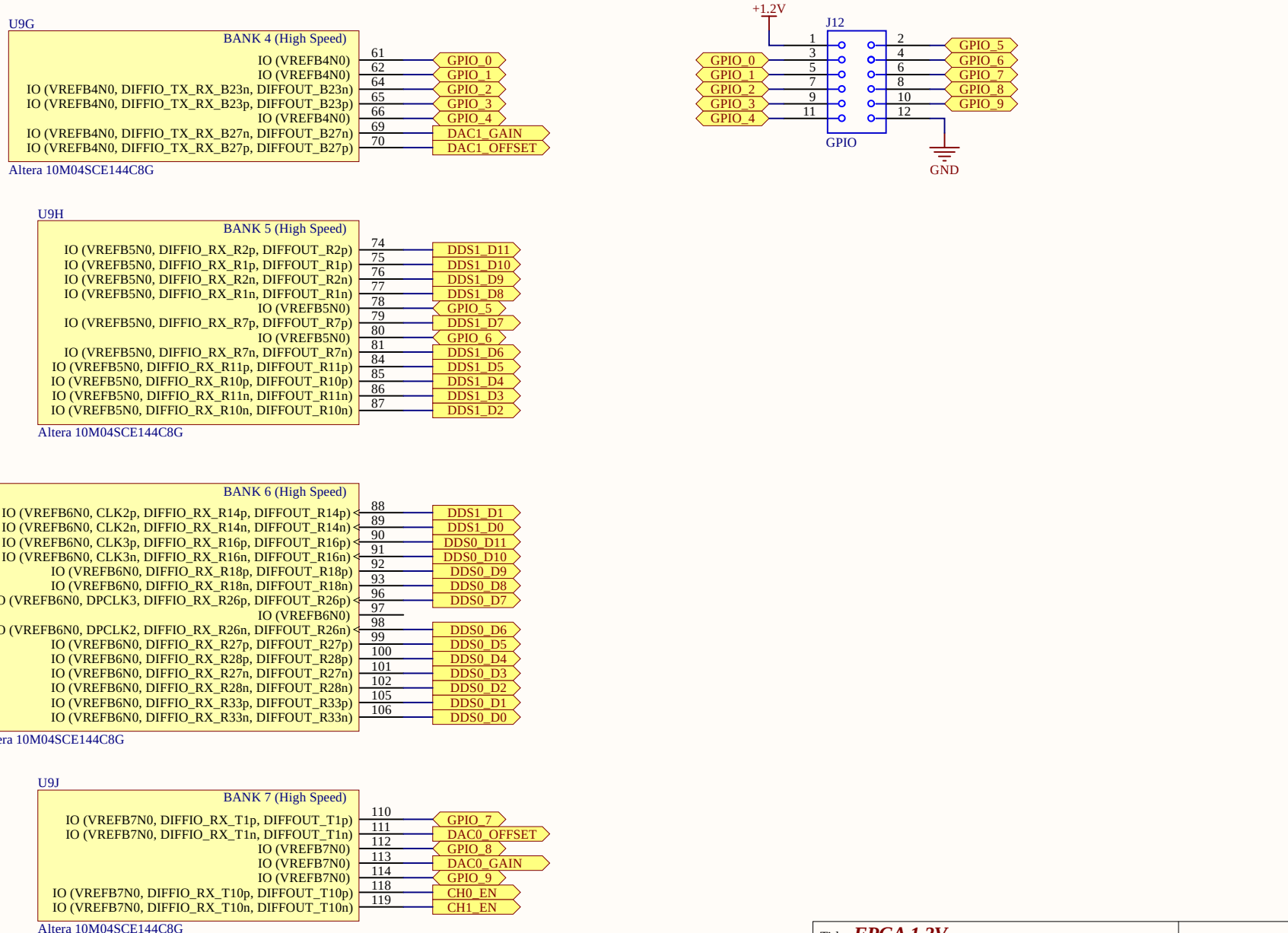
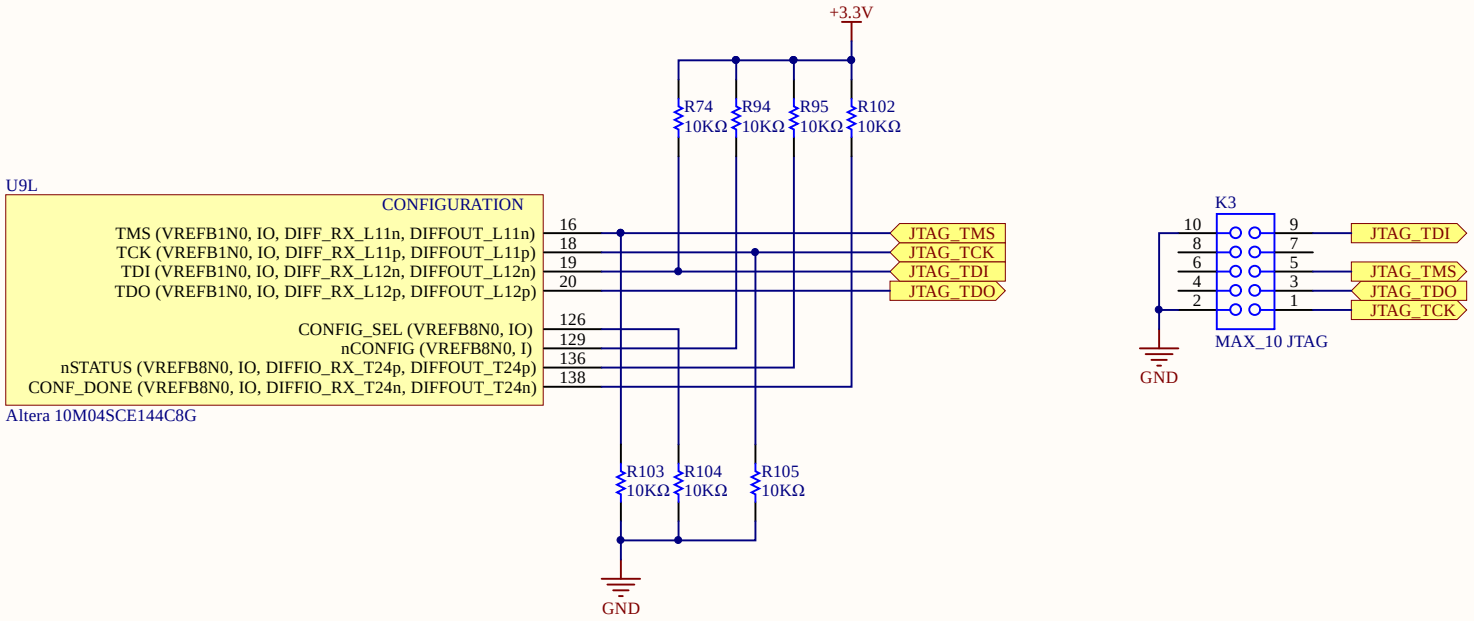
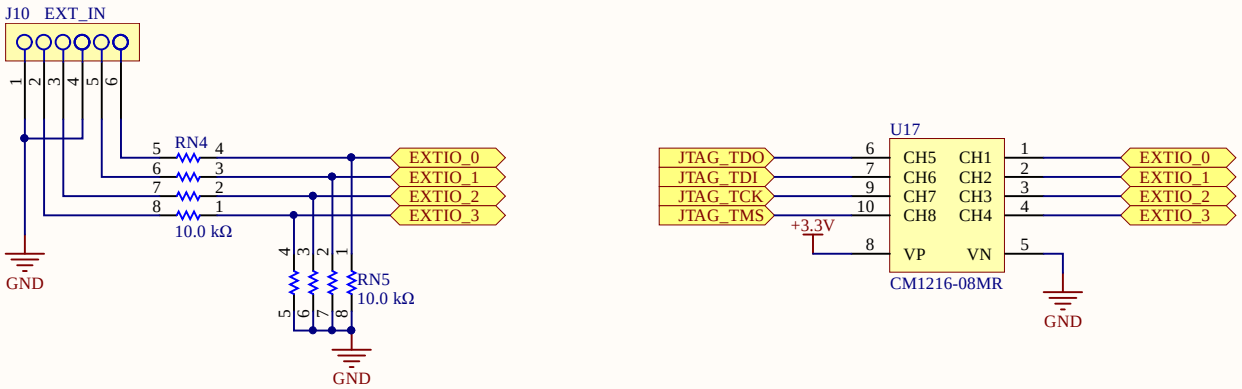

+12V
X1
1
2
3
POWER
C61
10 µF
C62
10 µF
GND
-12V
+3.3V
U12
IN
OUT
GND
AZ1117CD-1.2TRG1
+1.2V
C63
10 µF
GND
+12V
U13
IN
OUT
GND
MC78M05CDTG
+5V
C64
1uF
GND
-12V
U14
IN
OUT
GND
MC79M05CDTG
-5V
C65
1uF
GND
C66
100nF
IC1
Microchip MCP16311-E/MS
VIN
EN
VCC
AGND
PGND
BST
SW
VFB
+12V
R111
100KΩ
C67
10 µF
C68
100nF
C71
1uF
GND
GND
L1
15uH
R112
31.6KΩ
R113
10KΩ
+3.3V
C69
10 µF
C70
100nF
GND
+3.3V
C72
10 µF
C73
100nF
C74
100nF
C75
100nF
C76
100nF
C77
100nF
C78
100nF
C79
100nF
GND
MAX 10 Power guidelines
--- Power supply ramps must be monotonic
--- Ensure that the minimum current for the power-on-reset (POR)
+3.3V
U9A
VCC_ONE
VCCA1
VCCA2
VCCA3
VCCA4
VCCA5
VCCA6
ANAIN1
ADC_VREF
VCCIO1A
VCCIO1B
VCCIO2
VCCIO3
VCCIO4
VCCIO5
VCCIO6
VCCIO7
VCCIO8
+3.3V
+1.2V
+3.3V
Altera 10M04SCE144C8G
U9B
REFGND
GND
E_PAD
Altera 10M04SCE144C8G
GND
+3.3V
C80
10 µF
C82
100nF
C83
100nF
C84
100nF
C85
100nF
C86
100nF
C87
100nF
GND
+1.2V
VCC_IO_1.2V
C81
10 µF
C88
100nF
C89
100nF
C90
100nF
C91
100nF
C92
100nF
GND
+3.3V
C93
10 µF
C94
10 µF
C95
100nF
C96
100nF
C97
100nF
C98
100nF
C99
100nF
C100
100nF
C101
100nF
C102
100nF
C103
100nF
C104
100nF
GND
Title Power
Size: A4
Number:1
Revision:1
Date: 30/11/2020
Time: 21:12:45
Sheet1 of 9
File: Power.SchDoc
CIRCUITSTUDIO


U9E
BANK 2 (High Speed)
IO (VREFB2N0, CLK0n, DIFFIO_RX_L18n, DIFFOUT_L18n)
IO (VREFB2N0, CLK0p, DIFFIO_RX_L18p, DIFFOUT_L18p)
IO (VREFB2N0, CLK1n, DIFFIO_RX_L20n, DIFFOUT_L20n)
IO (VREFB2N0, CLK1p, DIFFIO_RX_L20p, DIFFOUT_L20p)
IO (VREFB2N0)
IO (VREFB2N0, PLL_L_CLKOUTn, DIFF_RX_L27n, DIFFOUT_L27n)
IO (VREFB2N0, PLL_L_CLKOUTp, DIFF_RX_L27p, DIFFOUT_L27p)
26
27
28
29
30
32
33
FPGA_CLK_10Mhz
FPGA_EXTCLK_10Mhz
BTN_NC_0_DB
BTN_DISP_0_DB
BTN_CH0EN_DB
BTN_CH1EN_DB
Altera 10M04SCE144C8G
R106
200.0 Ω
D1
LED
GND
U9K
BANK 8 (Low Speed)
IO (VREFB8N0, DIFFIO_RX_T16p, DIFFOUT_T16p)
IO (VREFB8N0, DEV_CLRn, DIFFIO_RX_T16p, DIFFOUT_T16p)
IO (VREFB8N0, DEV_OE)
IO (VREFB8N0)
IO (VREFB8N0, DIFFIO_RX_T19p, DIFFOUT_T19p)
IO (VREFB8N0, DIFFIO_RX_T19n, DIFFOUT_T19n)
IO (VREFB8N0, DIFFIO_RX_T20p, DIFFOUT_T20p)
IO (VREFB8N0, DIFFIO_RX_T20n, DIFFOUT_T20n)
IO (VREFB8N0, DIFFIO_RX_T22p, DIFFOUT_T22p)
IO (VREFB8N0, CRC_ERROR, DIFFIO_RX_T22n, DIFFOUT_T22n)
IO (VREFB8N0)
IO (VREFB8N0, DIFFIO_RX_T26p, DIFFOUT_T26p)
IO (VREFB8N0, DIFFIO_RX_T26n, DIFFOUT_T26n)
120
121
122
123
124
127
130
131
132
134
135
140
141
NUMPAD_R0
NUMPAD_R1
NUMPAD_R2
NUMPAD_R3
NUMPAD_C0
NUMPAD_C1
NUMPAD_C2
NUMPAD_C3
BTN_ARROW_L_DB
BTN_ARROW_R_DB
ENC_0_DB
ENC_1_DB
ENC_PB_DB
Altera 10M04SCE144C8G
U9D
BANK 1B (Low Speed)
IO (VREFB1N0, JTAGEN)
IO (VREFB1N0)
IO (VREFB1N0, DIFF_RX_L14n, DIFFOUT_L14n)
IO (VREFB1N0, DIFF_RX_L14p, DIFFOUT_L14p)
IO (VREFB1N0, DIFF_RX_L16n, DIFFOUT_L16n)
IO (VREFB1N0, DIFF_RX_L16p, DIFFOUT_L16p)
15
17
21
22
24
25
BTN_DISP_1_DB
BTN_DISP_2_DB
BTN_DISP_3_DB
BTN_DISP_4_DB
BTN_DISP_5_DB
Altera 10M04SCE144C8G
+3.3V
R107
10KΩ
U9C
BANK 1A (Low Speed)
IO (VREFB1N0, DIFFIO_RX_L1n, DIFFOUT_L1n, ADC1IN1)
IO (VREFB1N0, DIFFIO_RX_L1p, DIFFOUT_L1p, ADC1IN2)
IO (VREFB1N0, DIFFIO_RX_L3n, DIFFOUT_L3n, ADC1IN3)
IO (VREFB1N0, DIFFIO_RX_L3p, DIFFOUT_L3p, ADC1IN4)
IO (VREFB1N0, DIFFIO_RX_L5n, DIFFOUT_L5n, ADC1IN5)
IO (VREFB1N0, DIFFIO_RX_L5p, DIFFOUT_L5p, ADC1IN6)
IO (VREFB1N0, DIFFIO_RX_L7n, DIFFOUT_L7n, ADC1IN7)
IO (VREFB1N0, DIFFIO_RX_L7p, DIFFOUT_L7p, ADC1IN8)
6
7
8
10
11
12
13
14
SD_CE
SD_MOSI
SD_MISO
SD_CLK
EXTIO_0
EXTIO_1
EXTIO_2
EXTIO_3
Altera 10M04SCE144C8G
U9F
BANK 3 (High Speed)
IO (VREFB3N0, DIFFIO_TX_RX_B1n, DIFFOUT_B1n)
IO (VREFB3N0, DIFFIO_TX_RX_B1p, DIFFOUT_B1p)
IO (VREFB3N0, DIFFIO_TX_RX_B3n, DIFFOUT_B3n)
IO (VREFB3N0, DIFFIO_TX_RX_B3p, DIFFOUT_B3p)
IO (VREFB3N0, DIFFIO_TX_RX_B5n, DIFFOUT_B5n)
IO (VREFB3N0, DIFFIO_TX_RX_B5p, DIFFOUT_B5p)
IO (VREFB3N0, DIFFIO_TX_RX_B7n, DIFFOUT_B7n)
IO (VREFB3N0, DIFFIO_TX_RX_B7p, DIFFOUT_B7p)
IO (VREFB3N0)
IO (VREFB3N0, DIFFIO_TX_RX_B9n, DIFFOUT_B9n)
IO (VREFB3N0, DIFFIO_TX_RX_B9p, DIFFOUT_B9p)
IO (VBREF3N0)
IO (VREFB3N0, DIFFIO_TX_RX_B12n, DIFFOUT_B12n)
IO (VREFB3N0, DIFFIO_TX_RX_B12p, DIFFOUT_B12p)
IO (VREFB3N0, DIFFIO_TX_RX_B14n, DIFFOUT_B14n)
IO (VREFB3N0, DIFFIO_TX_RX_B14p, DIFFOUT_B14p)
IO (VREFB3N0, DIFFIO_TX_RX_B16n, DIFFOUT_B16n)
IO (VREFB3N0, DIFFIO_TX_RX_B16p, DIFFOUT_B16p)
38
39
41
43
44
45
46
47
48
50
52
54
55
56
57
58
59
60
LED_CH0
LED_CH1
LCD_PWM
LCD_CSB
LCD_RST
LCD_A0
LCD_R/W
LCD_E
LCD_DB0
LCD_DB1
LCD_DB2
LCD_DB3
LCD_DB4
LCD_DB5
LCD_DB6
LCD_DB7
DDS1_SYNK
DDS0_SYNK
Altera 10M04SCE144C8G
Title FPGA 3.3V
Size: A4
Number:2
Revision:1
Date: 30/11/2020
Time: 21:12:46
Sheet2 of 9
File: FPGA_3.3V.SchDoc
CIRCUITSTUDIO


U9G
BANK 4 (High Speed)
IO (VREFB4N0)
IO (VREFB4N0)
IO (VREFB4N0, DIFFIO_TX_RX_B23n, DIFFOUT_B23n)
IO (VREFB4N0, DIFFIO_TX_RX_B23p, DIFFOUT_B23p)
IO (VREFB4N0)
IO (VREFB4N0, DIFFIO_TX_RX_B27n, DIFFOUT_B27n)
IO (VREFB4N0, DIFFIO_TX_RX_B27p, DIFFOUT_B27p)
61
62
64
65
66
69
70
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
DAC1_GAIN
DAC1_OFFSET
Altera 10M04SCE144C8G
U9H
BANK 5 (High Speed)
IO (VREFB5N0, DIFFIO_RX_R2p, DIFFOUT_R2p)
IO (VREFB5N0, DIFFIO_RX_R1p, DIFFOUT_R1p)
IO (VREFB5N0, DIFFIO_RX_R2n, DIFFOUT_R2n)
IO (VREFB5N0, DIFFIO_RX_R1n, DIFFOUT_R1n)
IO (VREFB5N0)
IO (VREFB5N0, DIFFIO_RX_R7p, DIFFOUT_R7p)
IO (VREFB5N0)
IO (VREFB5N0, DIFFIO_RX_R7n, DIFFOUT_R7n)
IO (VREFB5N0, DIFFIO_RX_R11p, DIFFOUT_R11p)
IO (VREFB5N0, DIFFIO_RX_R10p, DIFFOUT_R10p)
IO (VREFB5N0, DIFFIO_RX_R11n, DIFFOUT_R11n)
IO (VREFB5N0, DIFFIO_RX_R10n, DIFFOUT_R10n)
74
75
76
77
78
79
80
81
84
85
86
87
DDS1_D11
DDS1_D10
DDS1_D9
DDS1_D8
GPIO_5
DDS1_D7
GPIO_6
DDS1_D6
DDS1_D5
DDS1_D4
DDS1_D3
DDS1_D2
Altera 10M04SCE144C8G
U9I
BANK 6 (High Speed)
IO (VREFB6N0, CLK2p, DIFFIO_RX_R14p, DIFFOUT_R14p)
IO (VREFB6N0, CLK2n, DIFFIO_RX_R14n, DIFFOUT_R14n)
IO (VREFB6N0, CLK3p, DIFFIO_RX_R16p, DIFFOUT_R16p)
IO (VREFB6N0, CLK3n, DIFFIO_RX_R16n, DIFFOUT_R16n)
IO (VREFB6N0, DIFFIO_RX_R18p, DIFFOUT_R18p)
IO (VREFB6N0, DIFFIO_RX_R18n, DIFFOUT_R18n)
IO (VREFB6N0, DPCLK3, DIFFIO_RX_R26p, DIFFOUT_R26p)
IO (VREFB6N0)
IO (VREFB6N0, DPCLK2, DIFFIO_RX_R26n, DIFFOUT_R26n)
IO (VREFB6N0, DIFFIO_RX_R27p, DIFFOUT_R27p)
IO (VREFB6N0, DIFFIO_RX_R28p, DIFFOUT_R28p)
IO (VREFB6N0, DIFFIO_RX_R27n, DIFFOUT_R27n)
IO (VREFB6N0, DIFFIO_RX_R28n, DIFFOUT_R28n)
IO (VREFB6N0, DIFFIO_RX_R33p, DIFFOUT_R33p)
IO (VREFB6N0, DIFFIO_RX_R33n, DIFFOUT_R33n)
88
89
90
91
92
93
96
97
98
99
100
101
102
105
106
DDS1_D1
DDS1_D0
DDS0_D11
DDS0_D10
DDS0_D9
DDS0_D8
DDS0_D7
DDS0_D6
DDS0_D5
DDS0_D4
DDS0_D3
DDS0_D2
DDS0_D1
DDS0_D0
Altera 10M04SCE144C8G
U9J
BANK 7 (High Speed)
IO (VREFB7N0, DIFFIO_RX_T1p, DIFFOUT_T1p)
IO (VREFB7N0, DIFFIO_RX_T1n, DIFFOUT_T1n)
IO (VREFB7N0)
IO (VREFB7N0)
IO (VREFB7N0)
IO (VREFB7N0, DIFFIO_RX_T10p, DIFFOUT_T10p)
IO (VREFB7N0, DIFFIO_RX_T10n, DIFFOUT_T10n)
110
111
112
113
114
118
119
GPIO_7
DAC0_OFFSET
GPIO_8
DAC0_GAIN
GPIO_9
CH0_EN
CH1_EN
Altera 10M04SCE144C8G
+1.2V
J12
1
3
5
7
9
11
2
4
6
8
10
12
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO
GND
Title FPGA 1.2V
Size: A4
Number:3
Revision:1
Date: 30/11/2020
Time: 21:12:46
Sheet3 of 9
File: FPGA_1.2v.SchDoc
CIRCUITSTUDIO

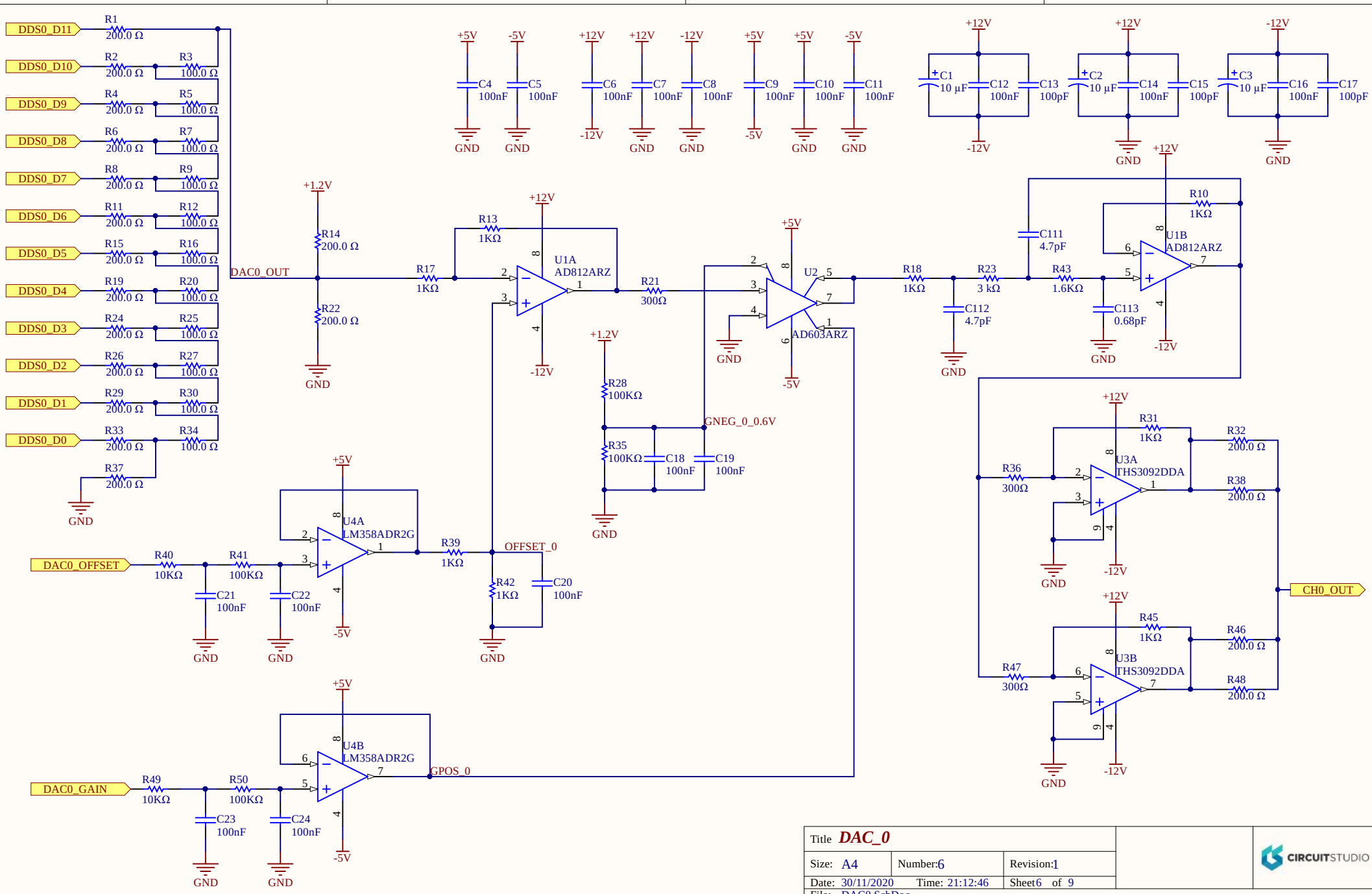


Title	***FPGA JTAG***		
Size: A4	Number:4	Revision:1	
Date: 30/11/2020	Time: 21:12:46	Sheet4 of 9	
File: FPGA_JTAG.SchDoc			



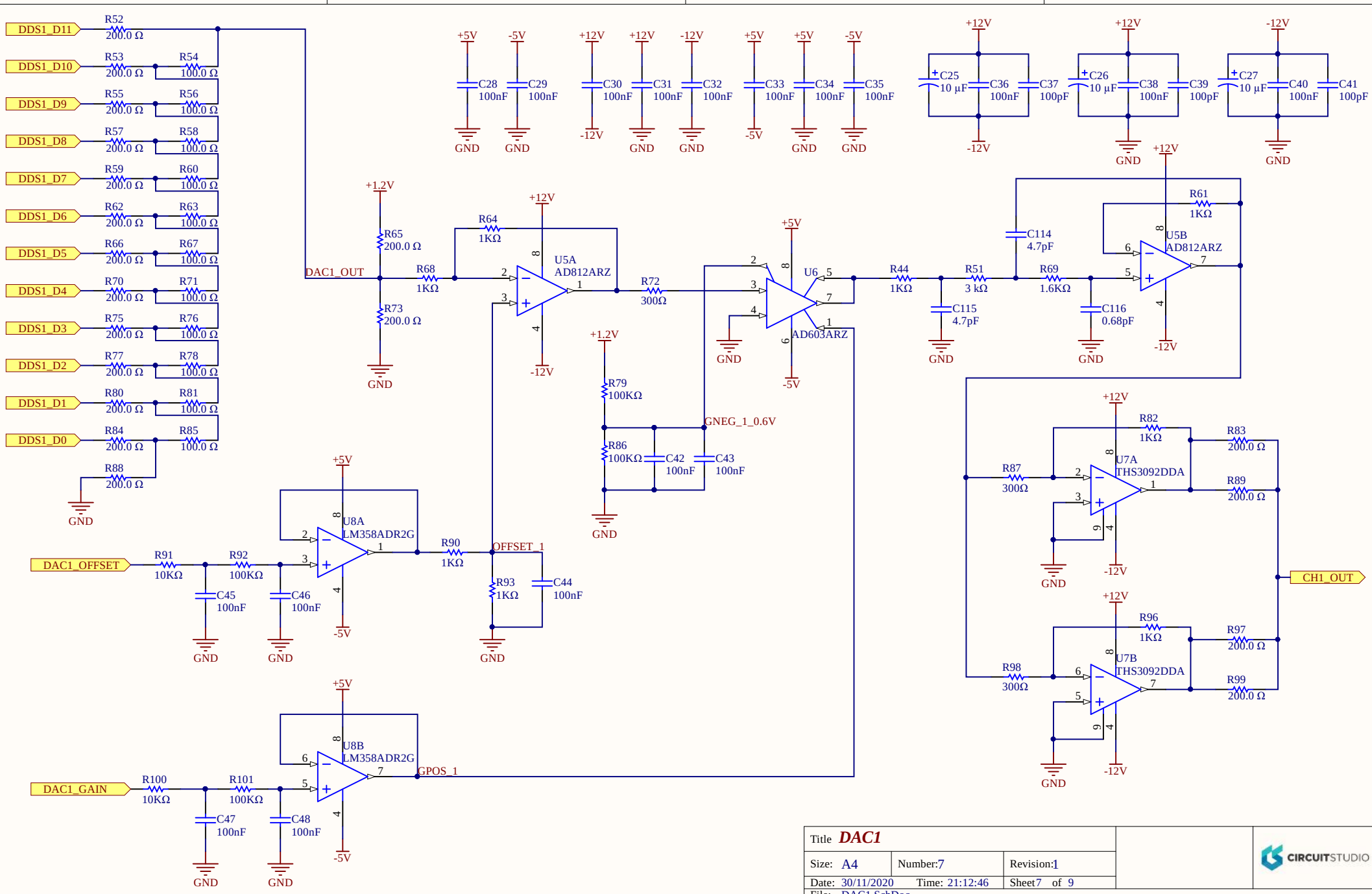
Title	***Analog***		
Size: A4	Number:5	Revision:1	
Date: 30/11/2020	Time: 21:12:46	Sheet5 of 9	
File: Analog.SchDoc			

CIRCUITSTUDIO



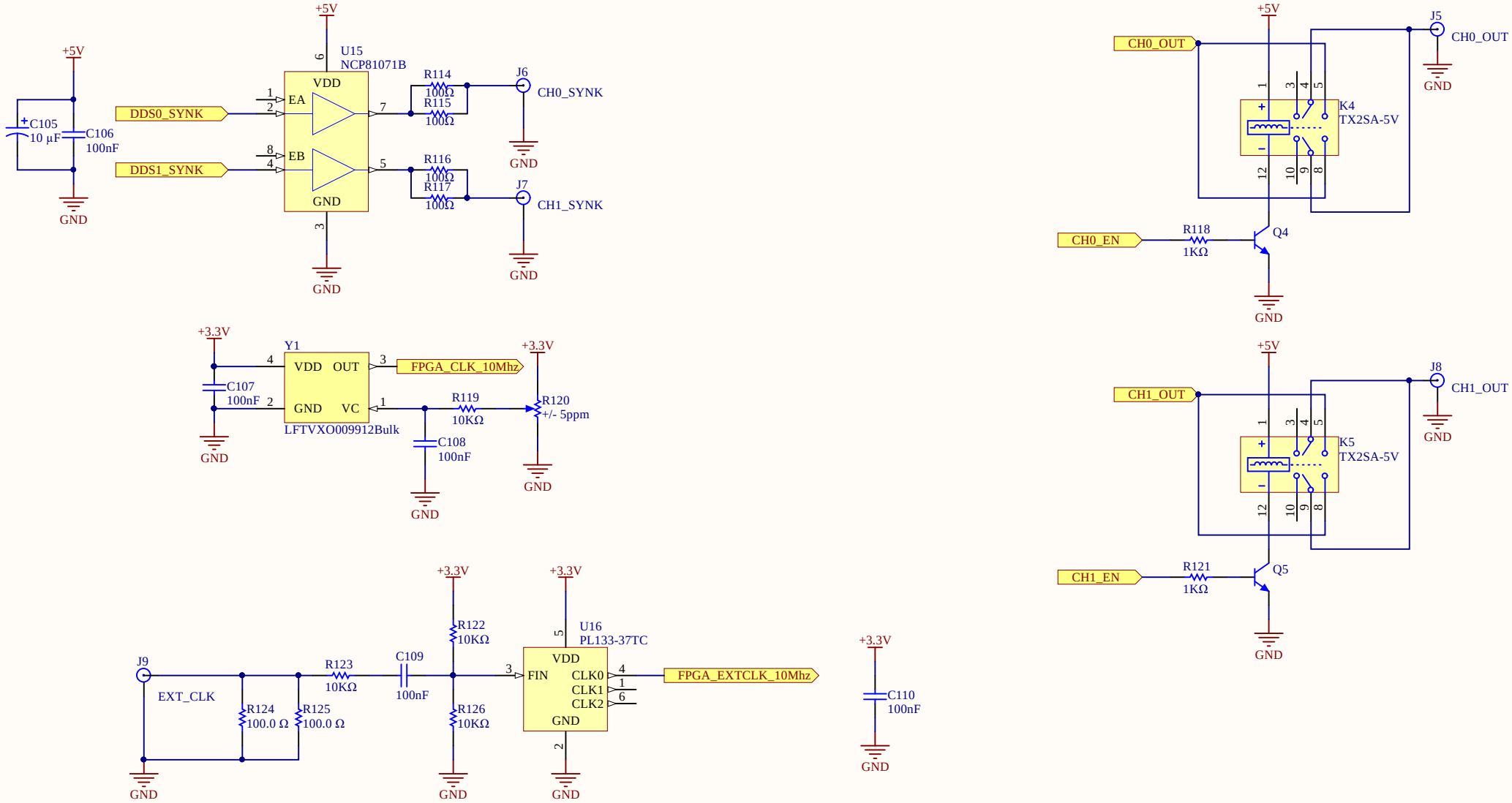
Title	***DAC_0***		
Size: A4	Number:6	Revision:1	
Date: 30/11/2020	Time: 21:12:46	Sheet6 of 9	
File: DAC0.SchDoc			

CIRCUITSTUDIO

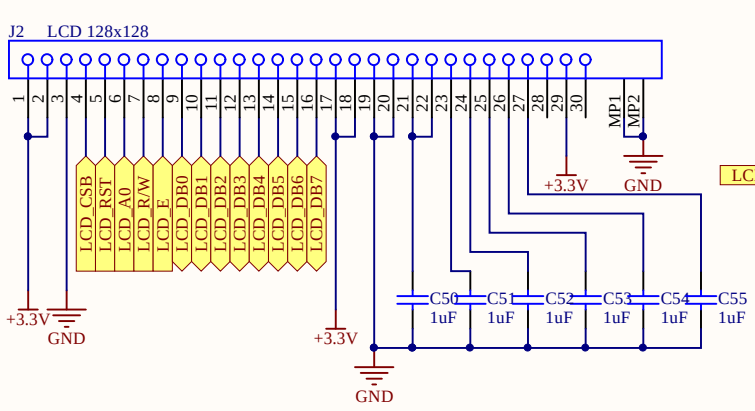


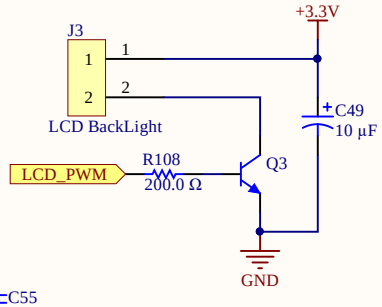
Title	***DAC1***		
Size: A4	Number:7	Revision:1	
Date: 30/11/2020	Time: 21:12:46	Sheet7 of 9	
File: DAC1.SchDoc			

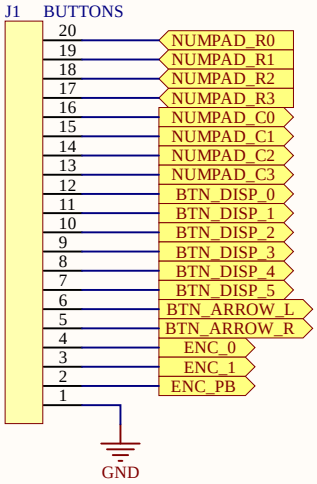
CIRCUITSTUDIO

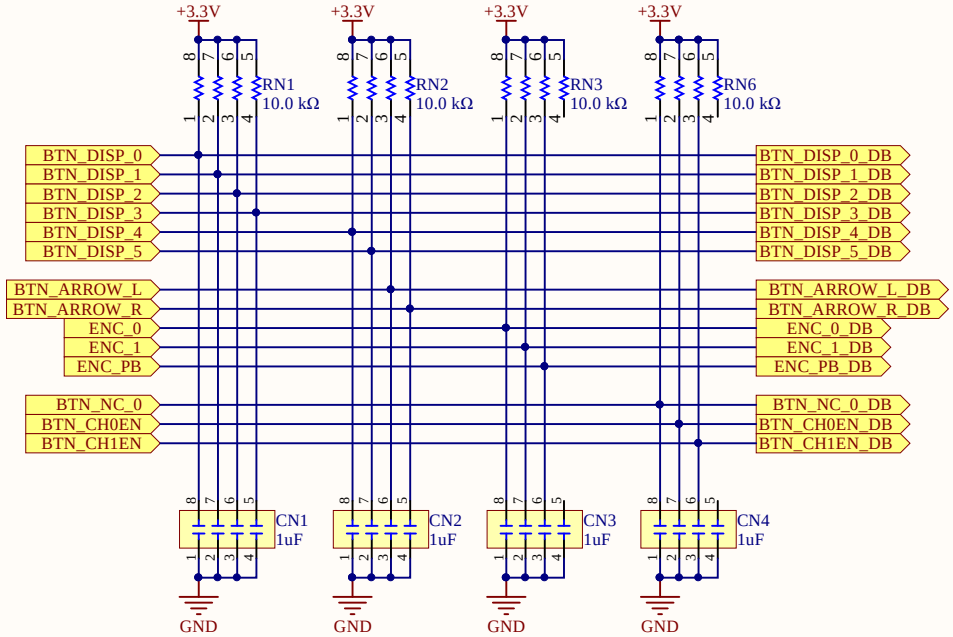


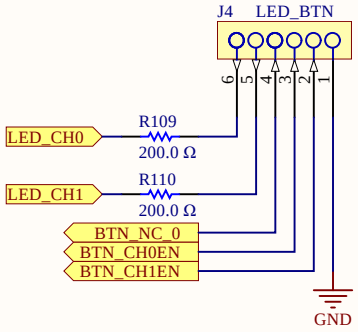
Title	***Clock and Buffers***		
Size: A4	Number:8	Revision:1	
Date: 30/11/2020	Time: 21:12:47	Sheet8 of 9	
File: ClockAndBuffers.SchDoc			

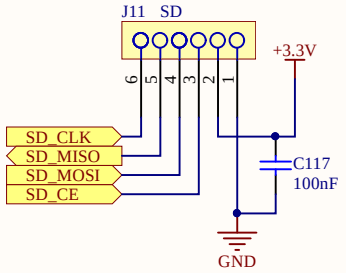












Title	***Front Pannel***		
Size: A4	Number:9	Revision:1	
Date: 30/11/2020	Time: 21:12:47	Sheet9 of 9	
File: FrontPannel.SchDoc			

CIRCUITSTUDIO