

Power and FPGA

Power.sch

Ethernet

Ethernet.sch

Clock

Clock.sch

RF Frontend

RFFrontend.sch

Input Output

InputOutput.sch

Filters

Filters.sch

PA

PA.sch

PCB
Pb1

CASE
EN1

PROG
PG1

KF70 Steve Haynal

SofterHardware

Sheet: /

File: hermeslite.sch

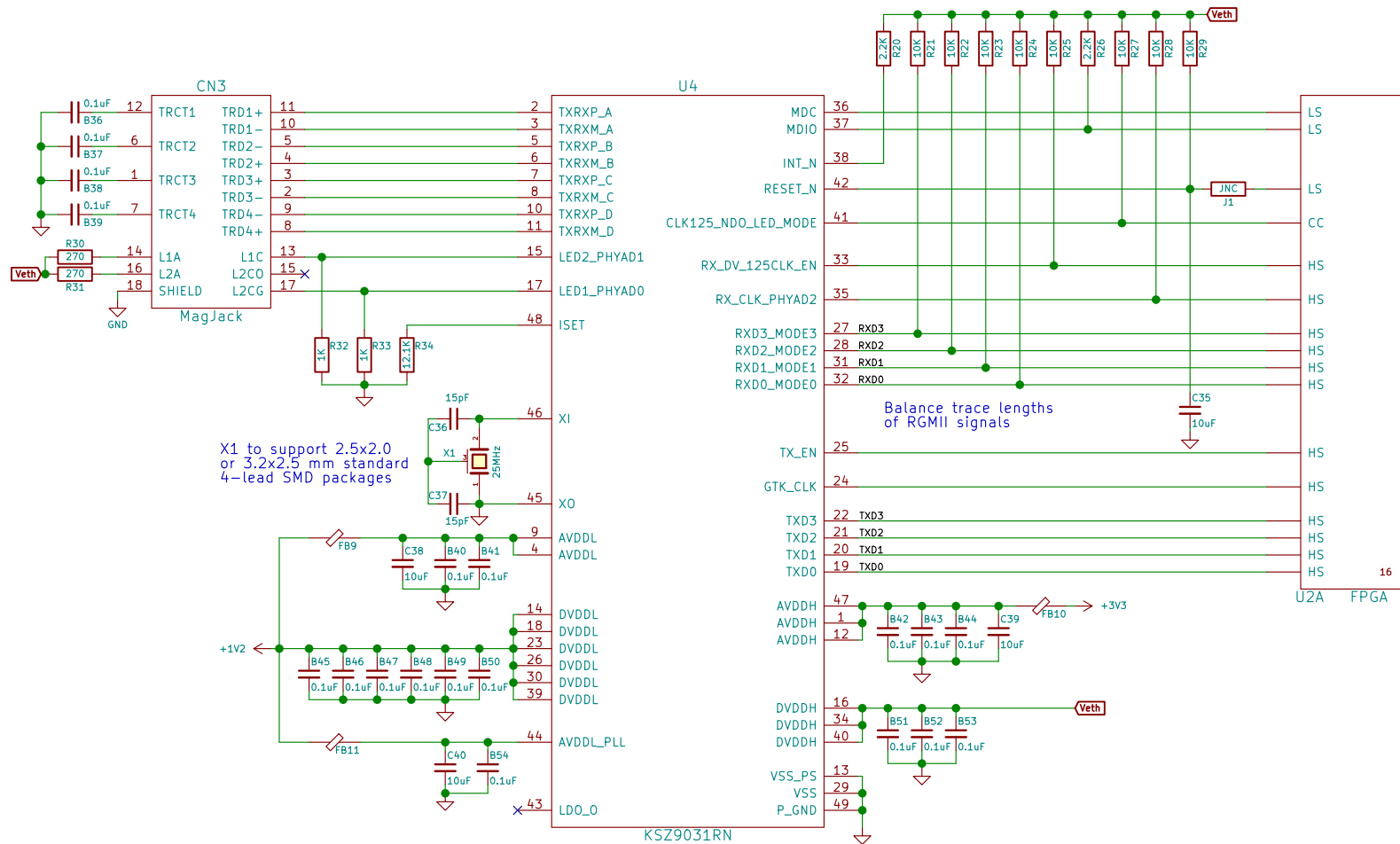
Title: **Hermes-Lite**

Size: USLetter Date: 2016-07-17

KiCad E.D.A. kicad 4.0.1-stable

Rev: **2.0-pre2**

Id: 1/8



KF70 Steve Haynal

SofterHardware

Sheet: /Ethernet/

File: Ethernet.sch

Title: Ethernet

Size: USLetter Date: 2016-07-10

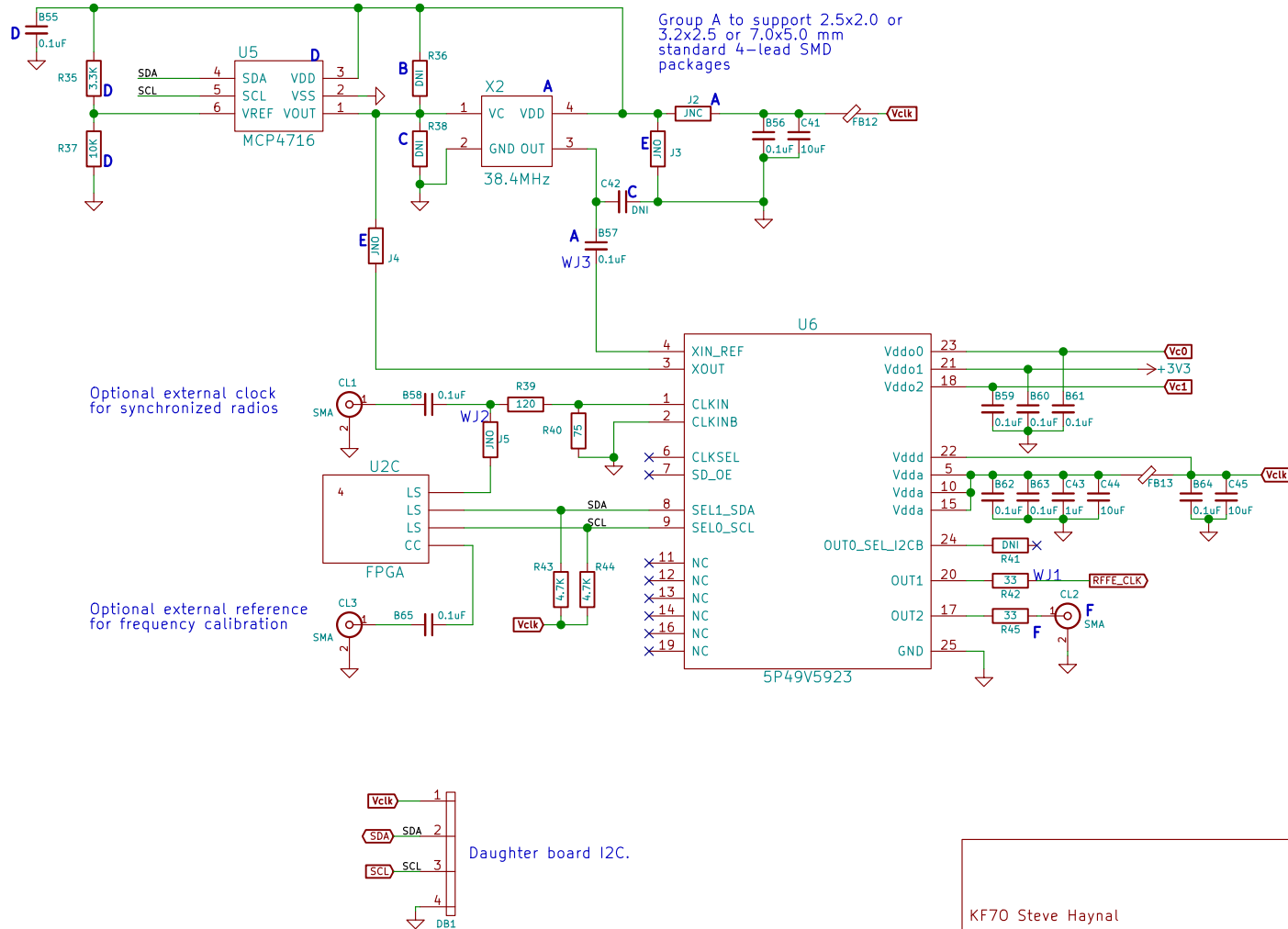
KiCad E.D.A. kicad 4.0.1-stable

Rev: 2.0-pre2

Id: 3/8

Build Options

Versa with oscillator: Include A, include B and/or C with adjusted values per oscillator's spec, exclude D and E
Versa with VCO: Include A and D, exclude B, C and E
Versa with crystal: Include E, E jumpers shorted, exclude A except oscillator footprint is now stuffed with crystal, include C as 15pF capacitor, exclude B and D
Versa with second output for synchronized slave: Build one of the Versa options above, include F
No Versa but oscillator to AD9866: Exclude all Versa components, build for oscillator, connect WJ3 to WJ1
No Versa but external clock to AD9866: Exclude all Versa components, A, B, C, D, and E, wire from WJ2 to WJ1
See RF Frontend sheet for additional AD9866 clock options



KF70 Steve Haynal

SofterHardware

Sheet: /Clock/

File: Clock.sch

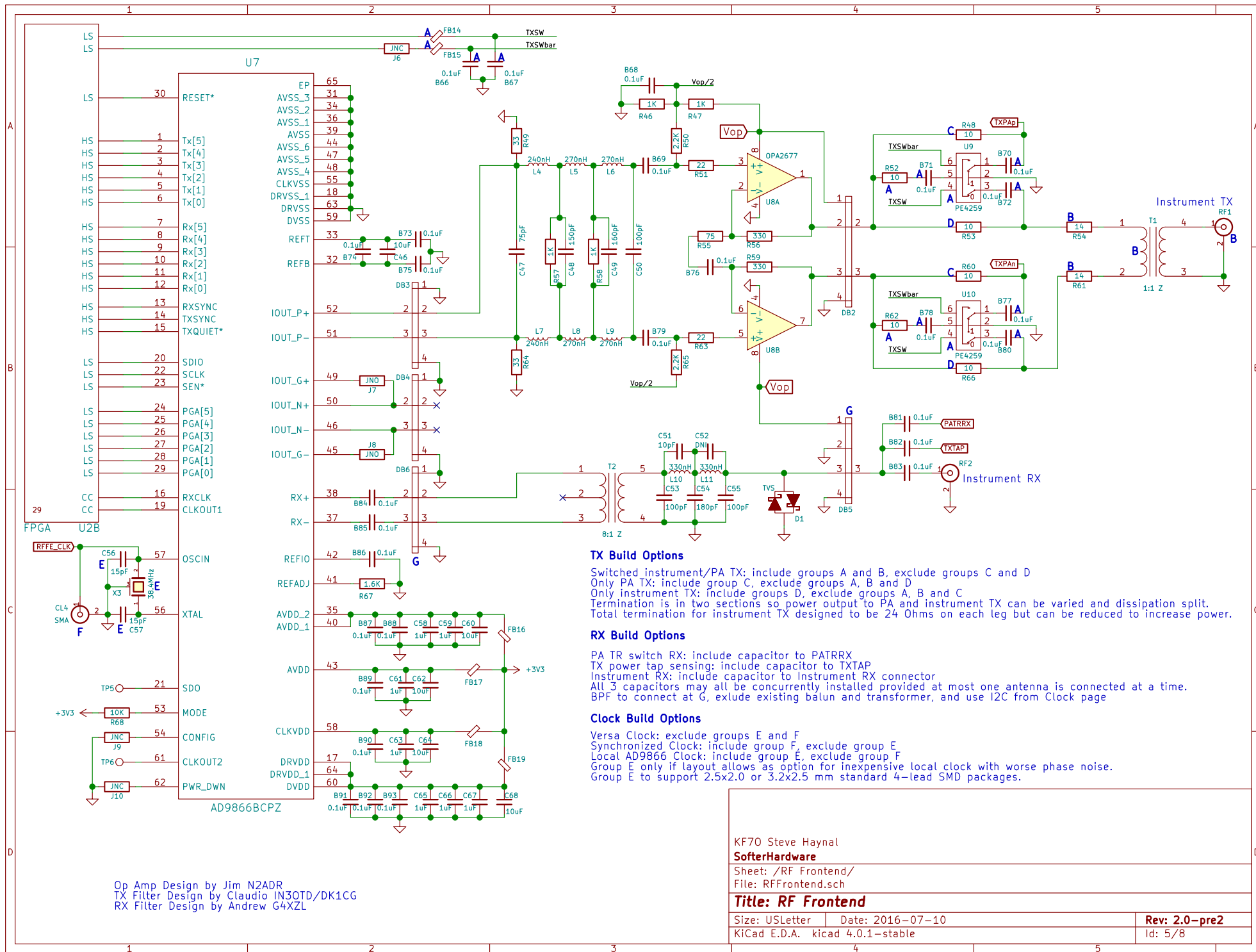
Title: Clock

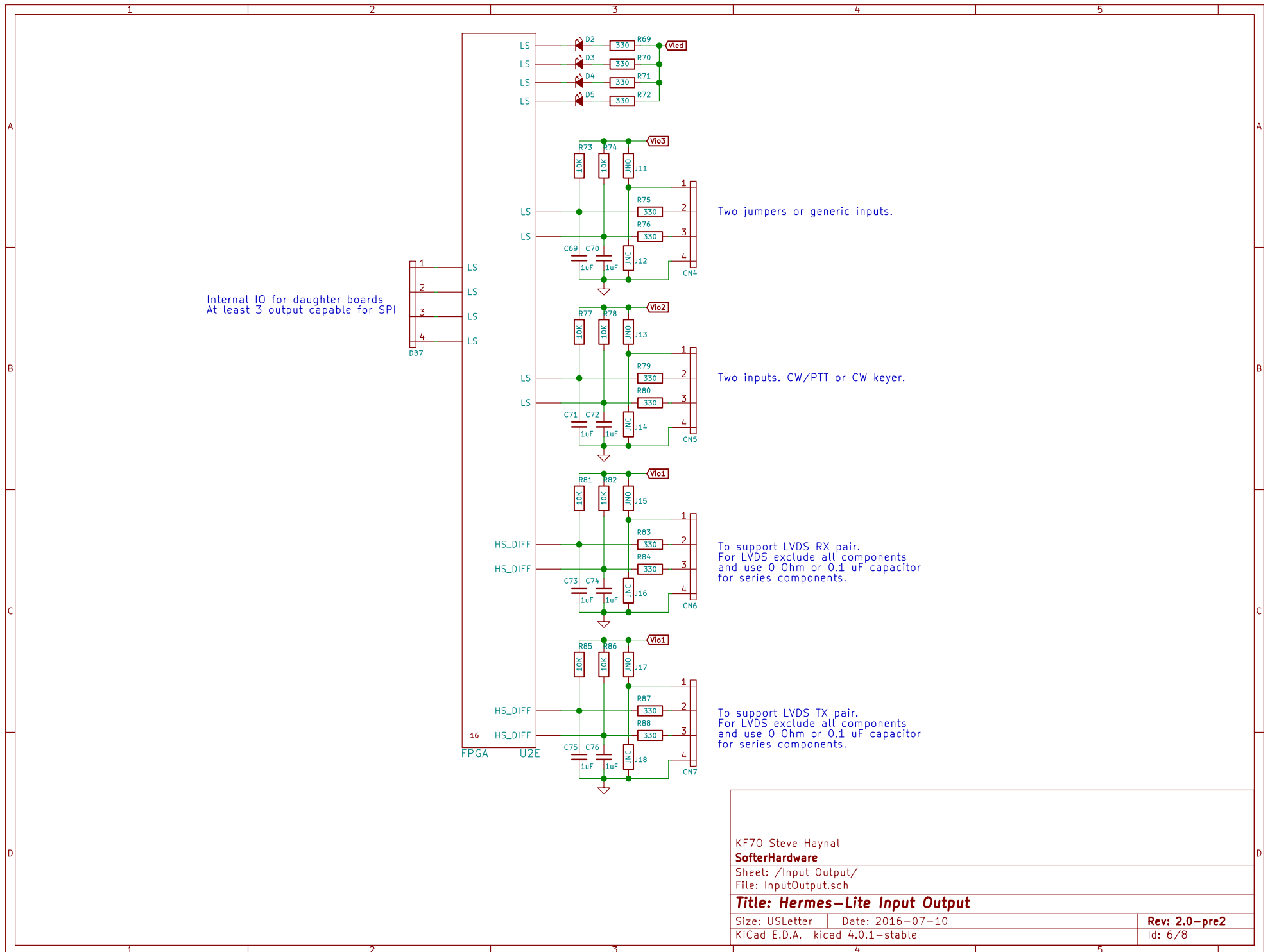
Size: USLetter Date: 2016-07-10

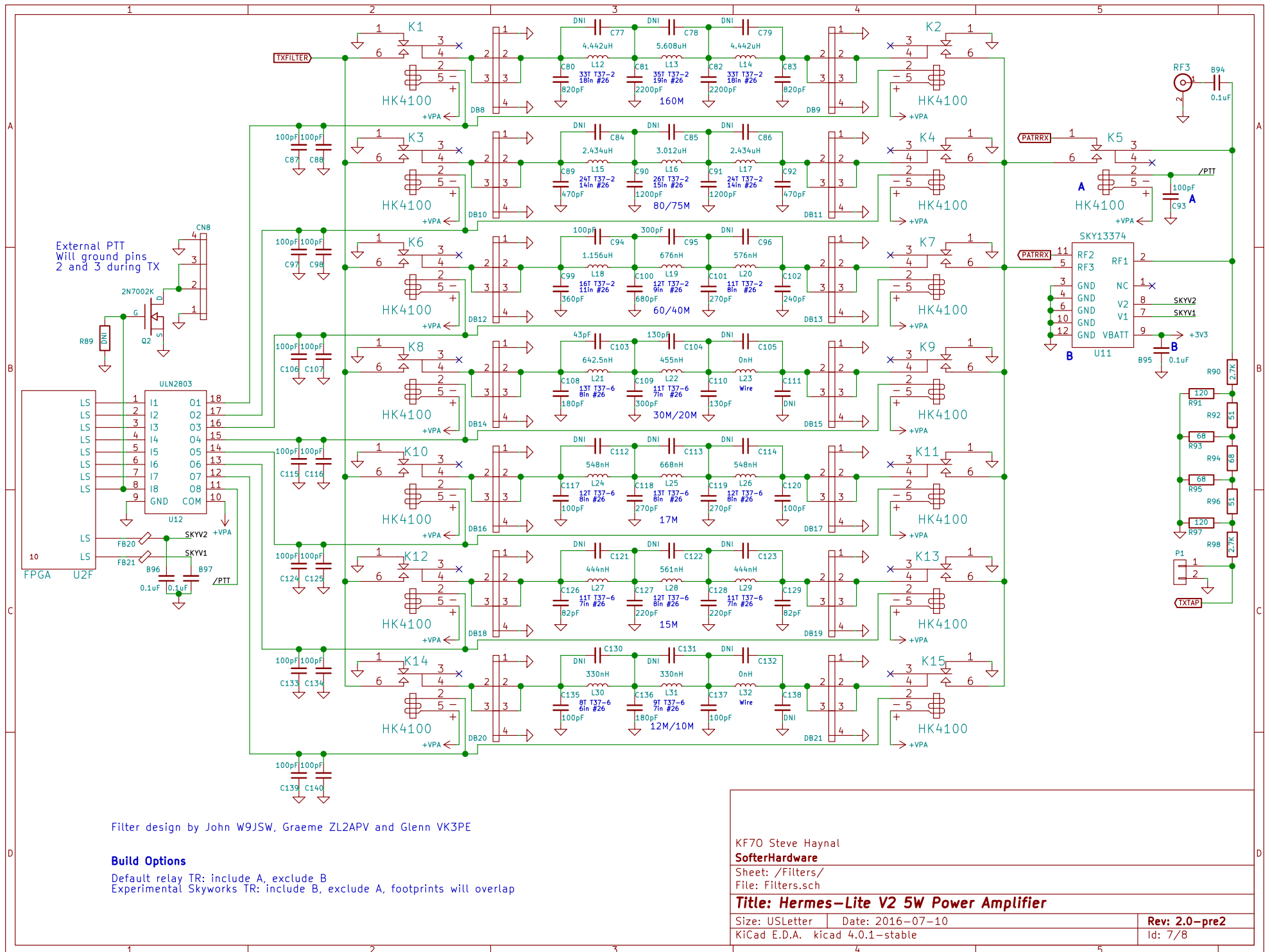
KiCad E.D.A. kicad 4.0.1-stable

Rev: 2.0-pre2

Id: 4/8





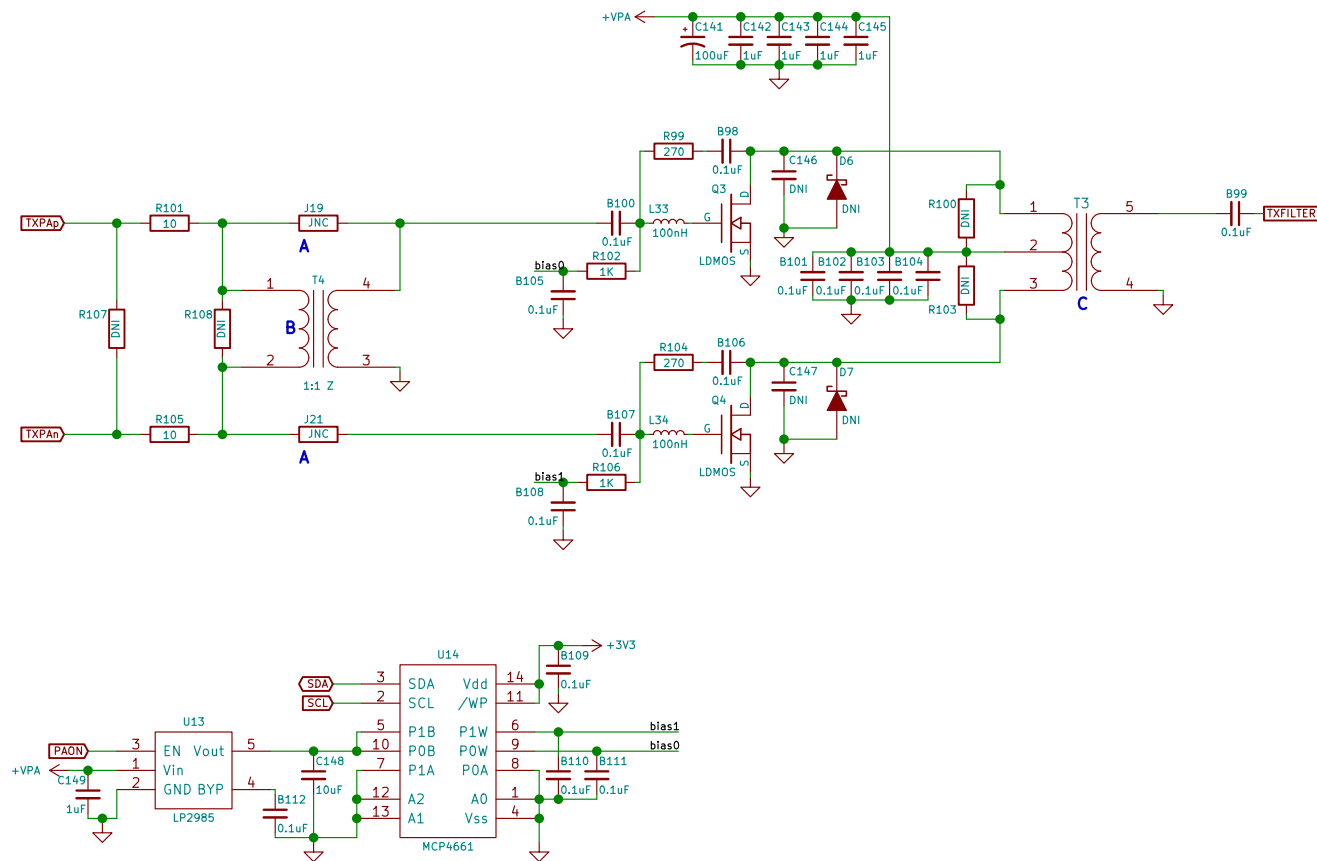


Build Options

Class AB Push Pull: include A, exclude B, C is BN43-202 4 turns primary, 1+1 turns secondary

Class A: include B, exclude A, exclude mirror PA using bias1, C is BN43-202 2 turns on pins 1/2, 4 turns on pins 4/5. C also supports SMT autotransformer or BN43-202 wound as 4:1Z autotransformer.

All values are first-cut place holders. To be refined with simulation and experimentation.



All I2C address to be checked for overlap!!
Position bias logic near digital logic, run long bias lines.

Design based on work by Claudio IN30TD/DK1CG, John W9JSW, and other LDMOS/MOSFET QRP PA designs

KF7O Steve Haynal

SofterHardware

Sheet: /PA/

File: PA.sch

Title: Hermes-Lite V2 5W Power Amplifier

Size: USLetter Date: 2016-07-10

KiCad E.D.A. kicad 4.0.1-stable

Rev: 2.0-pre2

Id: 8/8