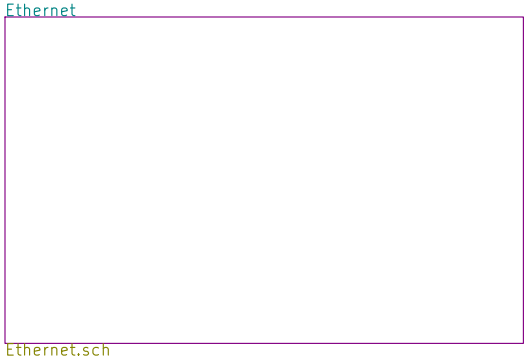
Power and FPGA

Power.sch

Ethernet

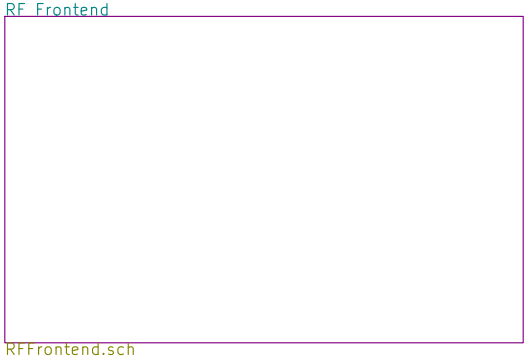


Ethernet.sch

Clock

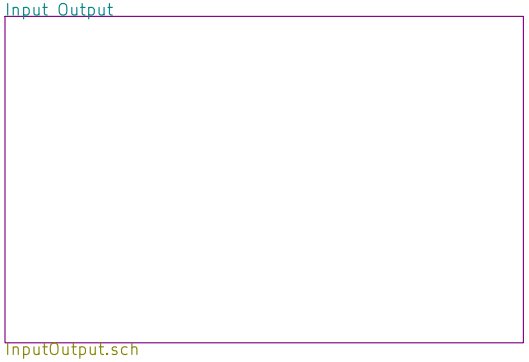
Clock.sch

RF Frontend



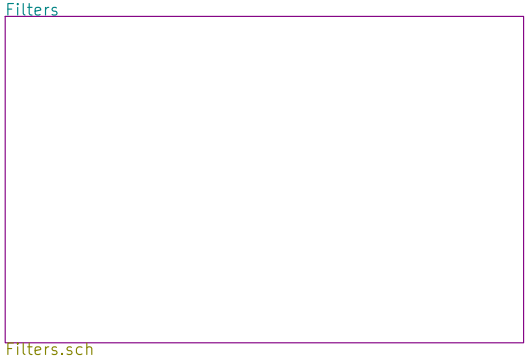
RFFrontend.sch

Input Output



InputOutput.sch

Filters



Filters.sch

PA

PA.sch

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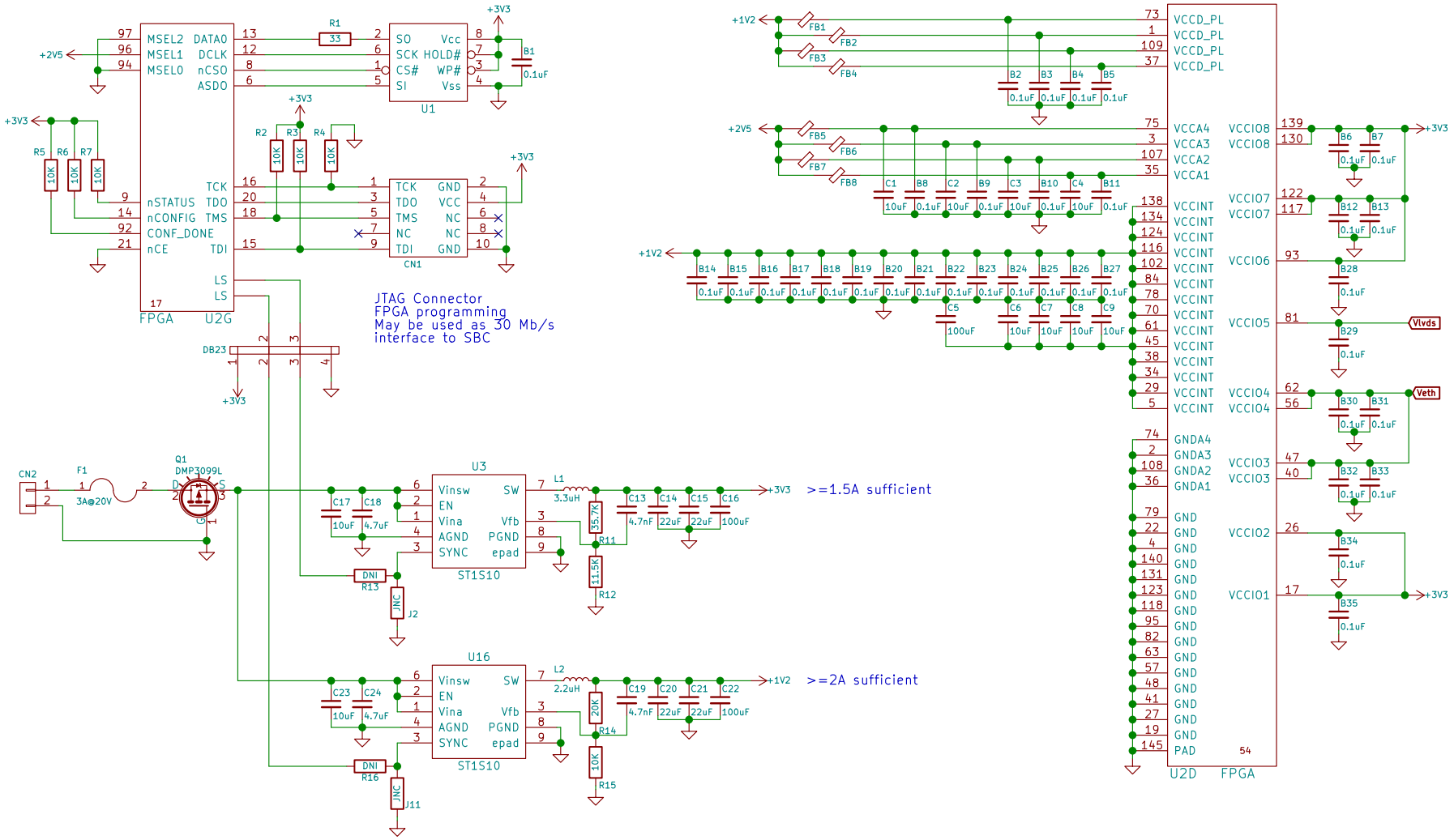
Sheet: /

File: hermeslite.sch

Title: Hermes-Lite

Size: USLetter	Date: 2016-07-17	**Rev: 2.0-pre2**
KiCad E.D.A. kicad 4.0.1-stable		Id: 1/8



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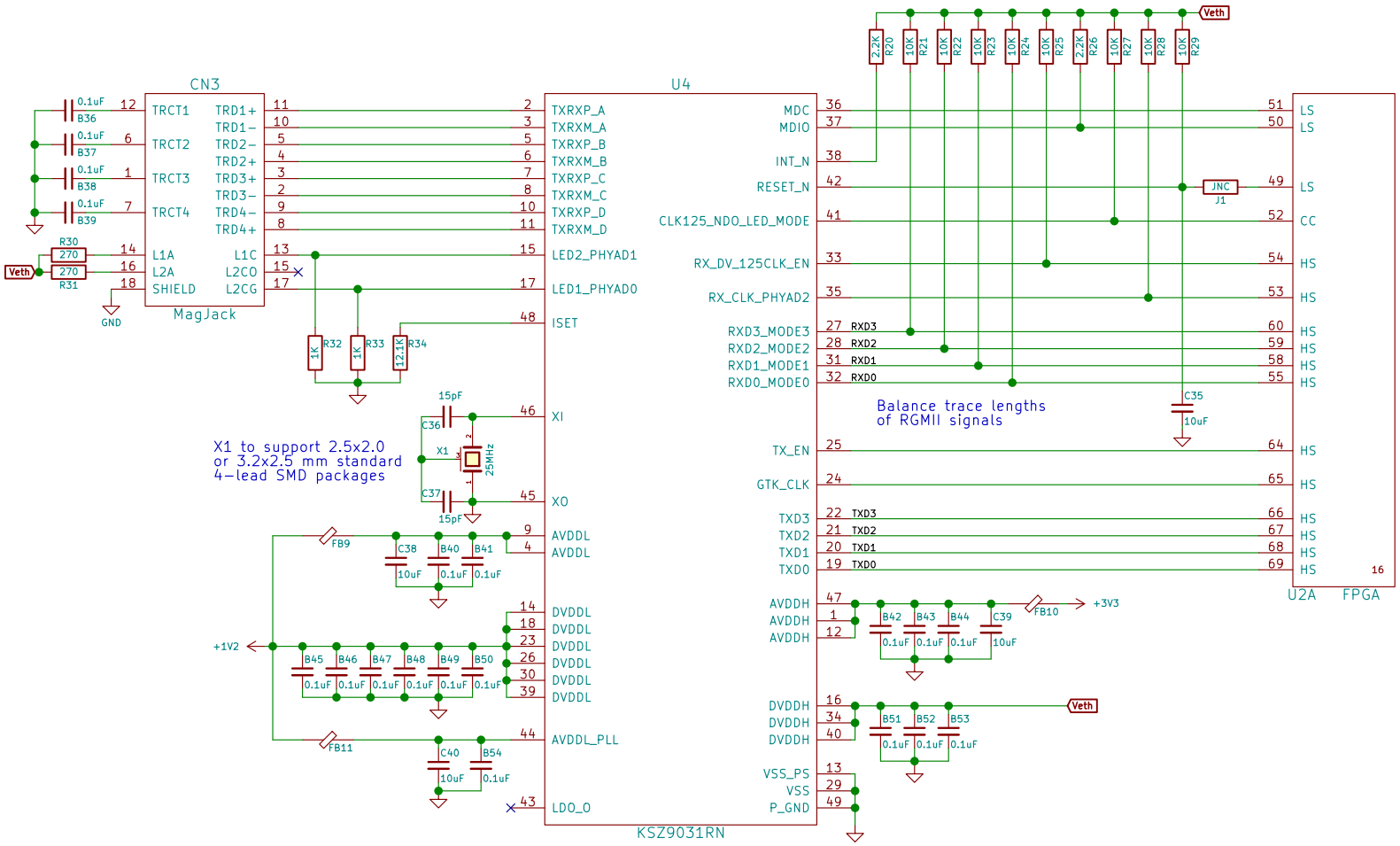
Sheet: /Power and FPGA/
File: Power.sch

Title: Power

Size: USLetter	Date: 2016-09-05	**Rev: 2.0-pre2**
KiCad E.D.A. kicad 4.0.1-stable		Id: 2/8



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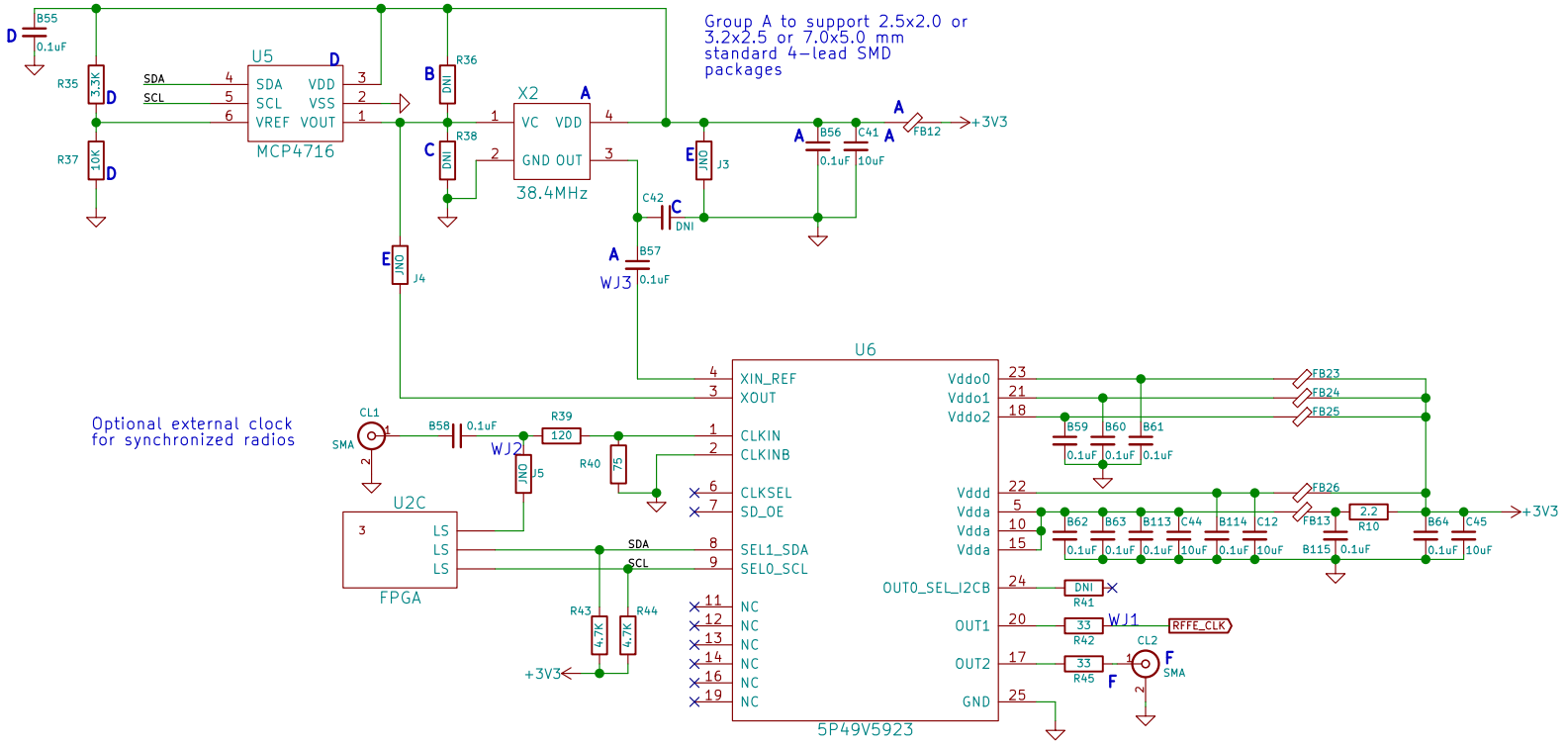
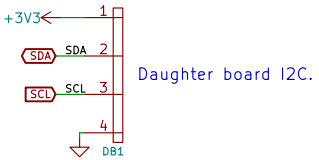
Sheet: /Ethernet/	
File: Ethernet.sch	
Title: Ethernet	
Size: USLetter | Date: 2016-09-05	**Rev: 2.0-pre2**
KiCad E.D.A. kicad 4.0.1-stable	Id: 3/8

Build Options

Versa with oscillator: Include A, include B and/or C with adjusted values per oscillator's spec, exclude D and E
Versa with VCO: Include A and D, exclude B, C and E
Versa with crystal: Include E, E jumpers shorted, exclude A except oscillator footprint is now stuffed with crystal, include C as 15pF capacitor, exclude B and D
Versa with second output for synchronized slave: Build one of the Versa options above, include F
No Versa but oscillator to AD9866: Exclude all Versa components, build for oscillator, connect WJ3 to WJ1
No Versa but external clock to AD9866: Exclude all Versa components, A, B, C, D, and E, wire from WJ2 to WJ1
See RF Frontend sheet for additional AD9866 clock options





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Sheet: /Clock/
File: Clock.sch

Title: Clock

Size: USLetter	Date: 2016-09-05	**Rev: 2.0-pre2**
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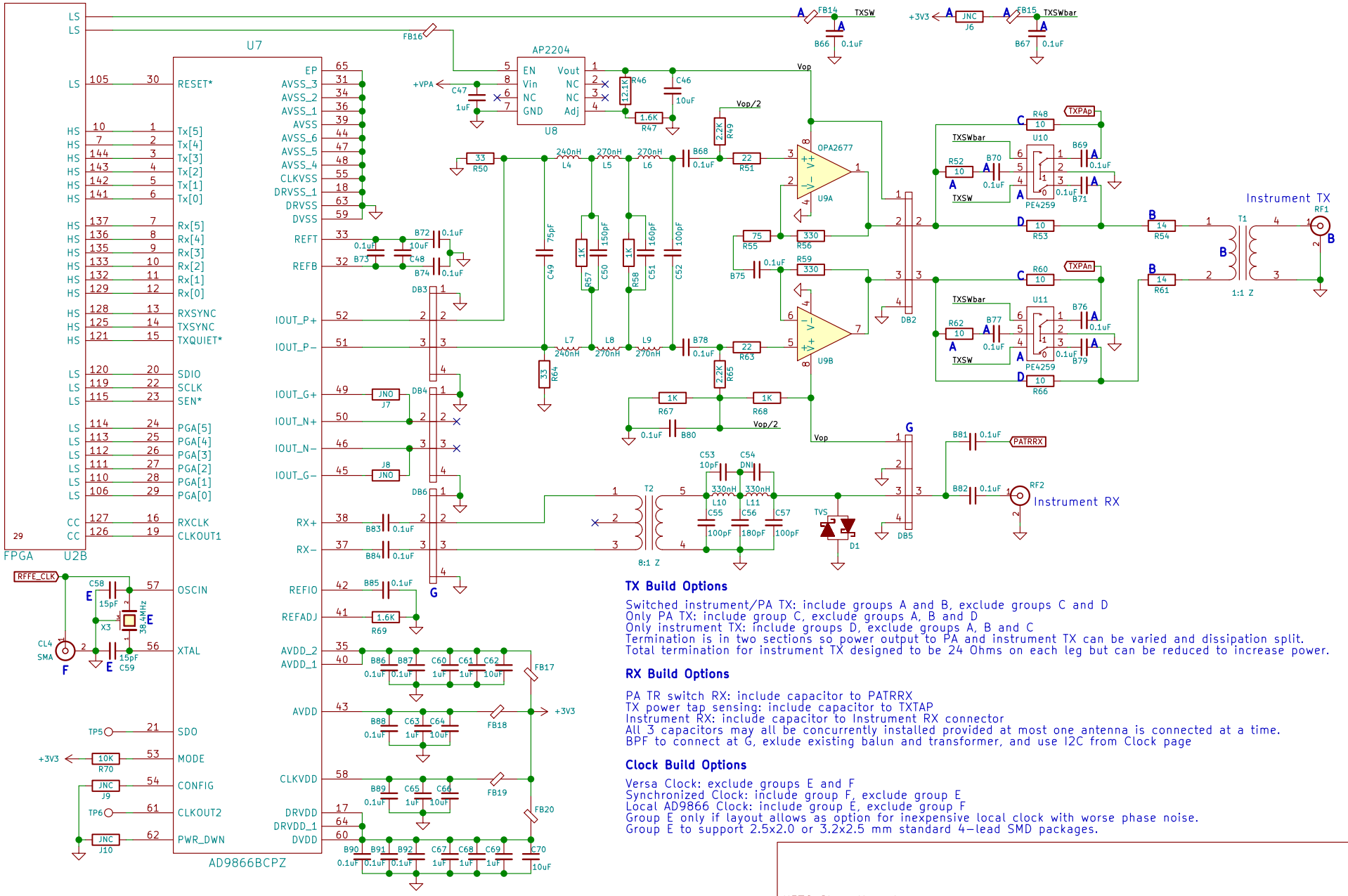

TX Build Options

Switched instrument/PA TX: include groups A and B, exclude groups C and D
Only PA TX: include group C, exclude groups A, B and D
Only instrument TX: include groups D, exclude groups A, B and C
Termination is in two sections so power output to PA and instrument TX can be varied and dissipation split.
Total termination for instrument TX designed to be 24 Ohms on each leg but can be reduced to increase power.

RX Build Options

PA TR switch RX: include capacitor to PATRRX
TX power tap sensing: include capacitor to TXTAP
Instrument RX: include capacitor to Instrument RX connector
All 3 capacitors may all be concurrently installed provided at most one antenna is connected at a time.
BPF to connect at G, exlude existing balun and transformer, and use I2C from Clock page

Clock Build Options

Versa Clock: exclude groups E and F
Synchronized Clock: include group F, exclude group E
Local AD9866 Clock: include group E, exclude group F
Group E only if layout allows as option for inexpensive local clock with worse phase noise.
Group E to support 2.5x2.0 or 3.2x2.5 mm standard 4-lead SMD packages.

Op Amp Design by Jim N2ADR
TX Filter Design by Claudio IN3OTD/DK1CG
RX Filter Design by Andrew G4XZL

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Sheet: /RF Frontend/
File: RFFrontend.sch

Title: RF Frontend

Size: USLetter	Date: 2016-09-05	**Rev: 2.0-pre2**
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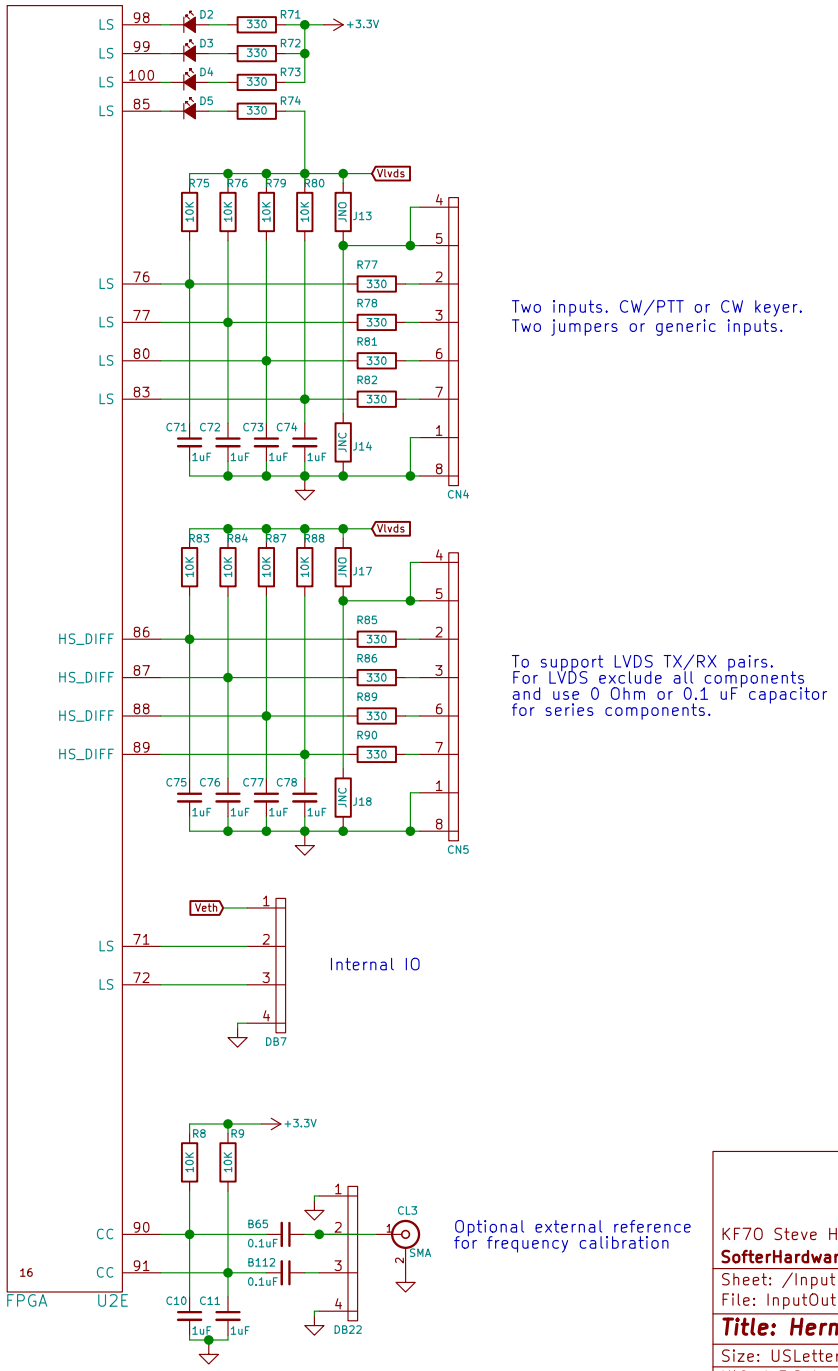

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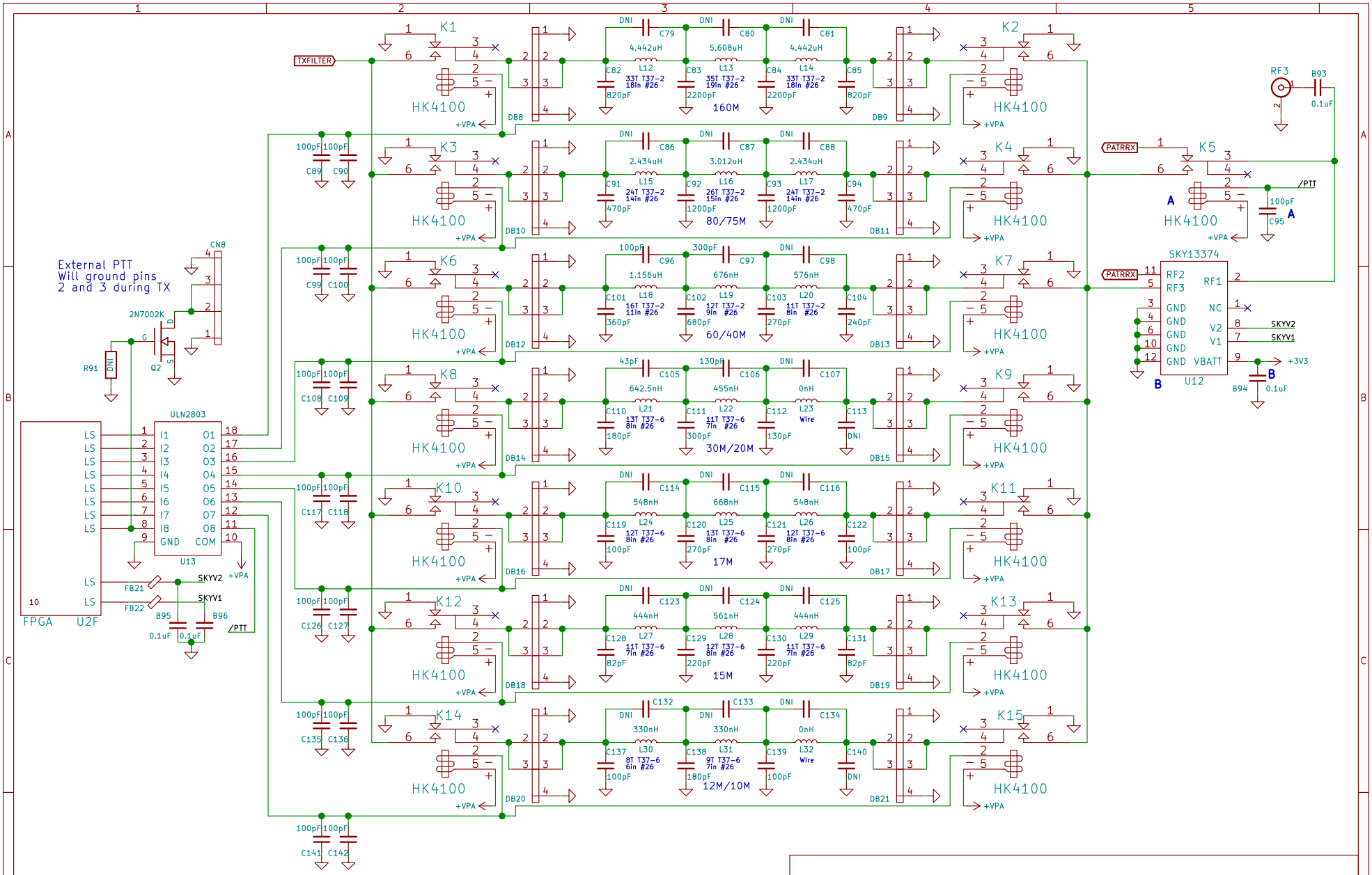
Sheet: /Input Output/
File: InputOutput.sch

Title: Hermes-Lite Input Output

Size: USLetter	Date: 2016-09-05	**Rev: 2.0-pre2**
KiCad E.D.A. kicad 4.0.1-stable		Id: 6/8


External PTT
Will ground pins
2 and 3 during TX
CN8
2N7002K
Q2
R91
DNI
ULN2803
U13
FPGA
U2F
FB21
FB22
B95
B96
0.1uF
/PTT
SKYV2
SKYV1
+VPA
TXFILTER
K1
K2
K3
K4
K5
K6
K7
K8
K9
K10
K11
K12
K13
K14
K15
HK4100
160M
80/75M
60/40M
30M/20M
17M
15M
12M/10M
RF3
B93
0.1uF
PATRRX
SKY13374
U12
RF1
RF2
RF3
GND
NC
V1
V2
VBATT
+3V3
B94
Filter design by John W9JSW, Graeme ZL2APV and Glenn VK3PE
Build Options
Default relay TR: include A, exclude B
Experimental Skyworks TR: include B, exclude A, footprints will overlap
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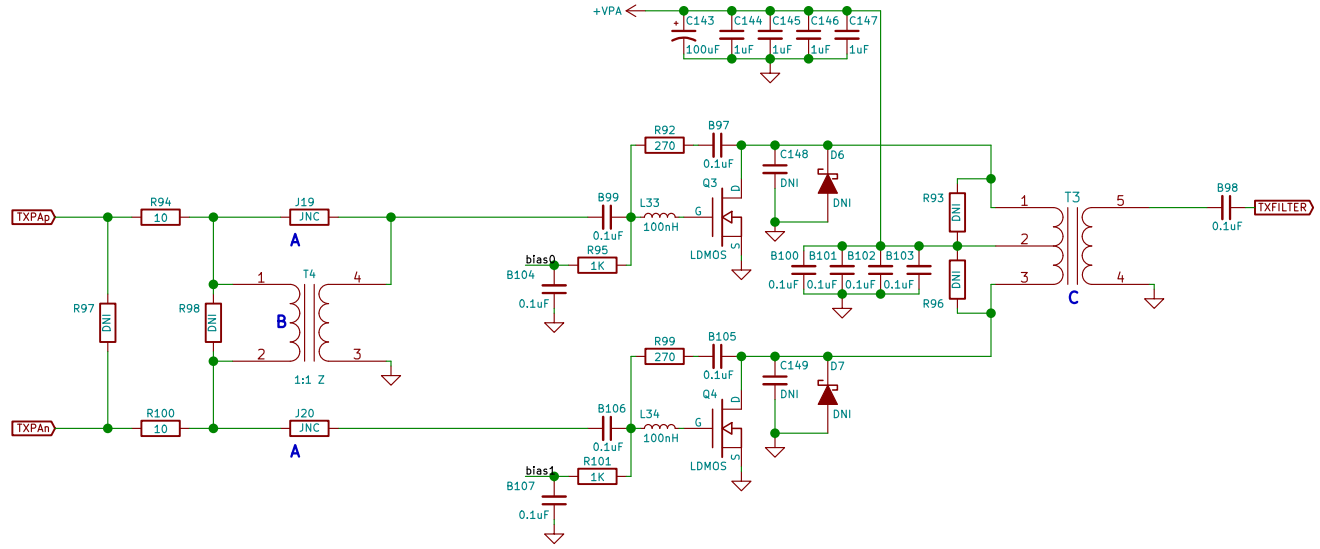
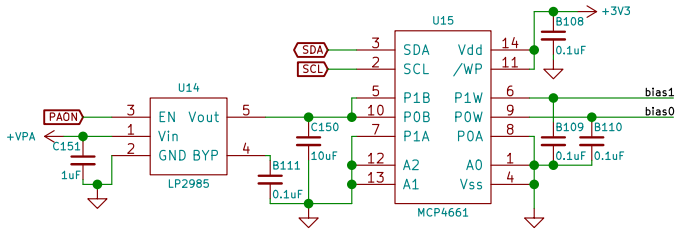
SofterHardware
Sheet: /Filters/
File: Filters.sch
Title: Hermes-Lite V2 5W Power Amplifier
Size: USLetter
Date: 2016-09-05
Rev: 2.0-pre2
KiCad E.D.A. kicad 4.0.1-stable
Id: 7/8

Build Options

Class AB Push Pull: include A, exclude B, C is BN43-202 4 turns primary, 1+1 turns secondary
Class A: include B, exclude A, exclude mirror PA using bias1, C is BN43-202 2 turns on pins 1/2, 4 turns on pins 4/5. C also supports SMT autotransformer or BN43-202 wound as 4:1Z autotransformer.

All values are first-cut place holders. To be refined with simulation and experimentation.





All I2C address to be checked for overlap!!
Position bias logic near digital logic, run long bias lines.

Design based on work by Claudio IN3OTD/DK1CG, John W9JSW, and other LDMOS/MOSFET QRP PA designs

KF7O Steve Haynal
SofterHardware
Sheet: /PA/
File: PA.sch

Title: Hermes-Lite V2 5W Power Amplifier

Size: USLetter	Date: 2016-09-05	**Rev: 2.0-pre2**
KiCad E.D.A. kicad 4.0.1-stable		Id: 8/8