Design1 analysed at 09/26/12 22:33:03

PLL Chip is ADF4351
VCO is ADF4351
Reference is custom

Advanced Design - VCO Divider is Outside loop and set as follows:

Start Freq	Stop Freq	VCO Divider	Channel Spacing
470MHz	550MHz	8	25.0kHz
550MHz	698MHz	4	50.0kHz

Loop Filter designed at a VCO frequency of 3.1113GHz with a Kv of 38.66MHz/V

Frequency Domain Analysis of PLL
Analysis at PLL output frequency of 572.75MHz

Phase Noise Table

Freq	Total	VCO	Ref	Chip	SDM	Filter
100	-96.65	-98.77	--	-100.8	-265.7	-154.3
1.00k	-93.70	-93.81	--	-110.0	-225.5	-134.4
10.0k	-94.71	-94.77	--	-114.1	-183.0	-120.9
100k	-125.6	-125.6	--	-151.9	-178.8	-150.8
1.00M	-145.5	-145.5	--	-209.0	-195.8	-189.1

Reference Spurious
Noise and Jitter Calculations include the first 10 ref spurs
First three spurs: -300 dBc -300 dBc -300 dBc

Fractional-N Spur Estimate (worst case)
Phase Detector mode is Dither OFF

Freq (Hz)	Spur Level (dBc)
100k	-90.2
200k	-106
300k	-116

Phase jitter using brick wall filter
from 10.0kHz to 100kHz
Phase Jitter **0.12 degrees rms**

ACP - Channel 1
Channel 1 is centred 25.0kHz from carrier with bandwidth 15.0kHz
Power in channel = **-62.4dBc**

---- End of Frequency Domain Results ----

Transient Analysis of PLL
Frequency change from 470MHz to 698MHz
Simulation run for 1.15ms

Frequency Locking
Time to lock to 1.00kHz is 294us
Time to lock to 10.0 Hz is 441us

Phase Locking (VCO Output Phase)
Time to lock to 10.0 deg is 298us
Time to lock to 1.00 deg is 372us

Lock Detect Threshold
Time to lock detect exceeds 2.50 V is 135us

---- End of Time Domain Results ----