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TECHNICAL UNIVERSITY
FACULTY OF ELECTRONICS
DEPARTMENT OF ELECTRONIC SYSTEMS

Max frequency signal generation

Embedded Systems
Intermediate Exam 1

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Work goal: using VHDL in DE0 development board generate maximum possible frequency periodical signal.

Algorithms used in tasks.

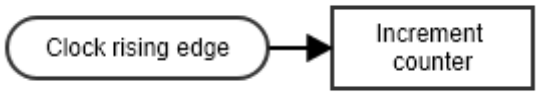


Fig. 1. "Algorithm" for signal generation.

Results analysis.

All in all it is simple operation: on each clock rising edge a counter is increased (Fig. 1) and that counter value is directly tied to output – when counter is an even number output is high, when an odd number output is low. Thus generating a periodic square-ish wave signal. In theory maximum frequency of a generated square wave is 25 MHz because FPGA clock is 50 MHz so due to there being two distinct states in the signal that needs to be switched between we get 25 MHz maximum. That is what the oscilloscope shows as well (Fig. 2).

Fig. 3. Example audio signal.

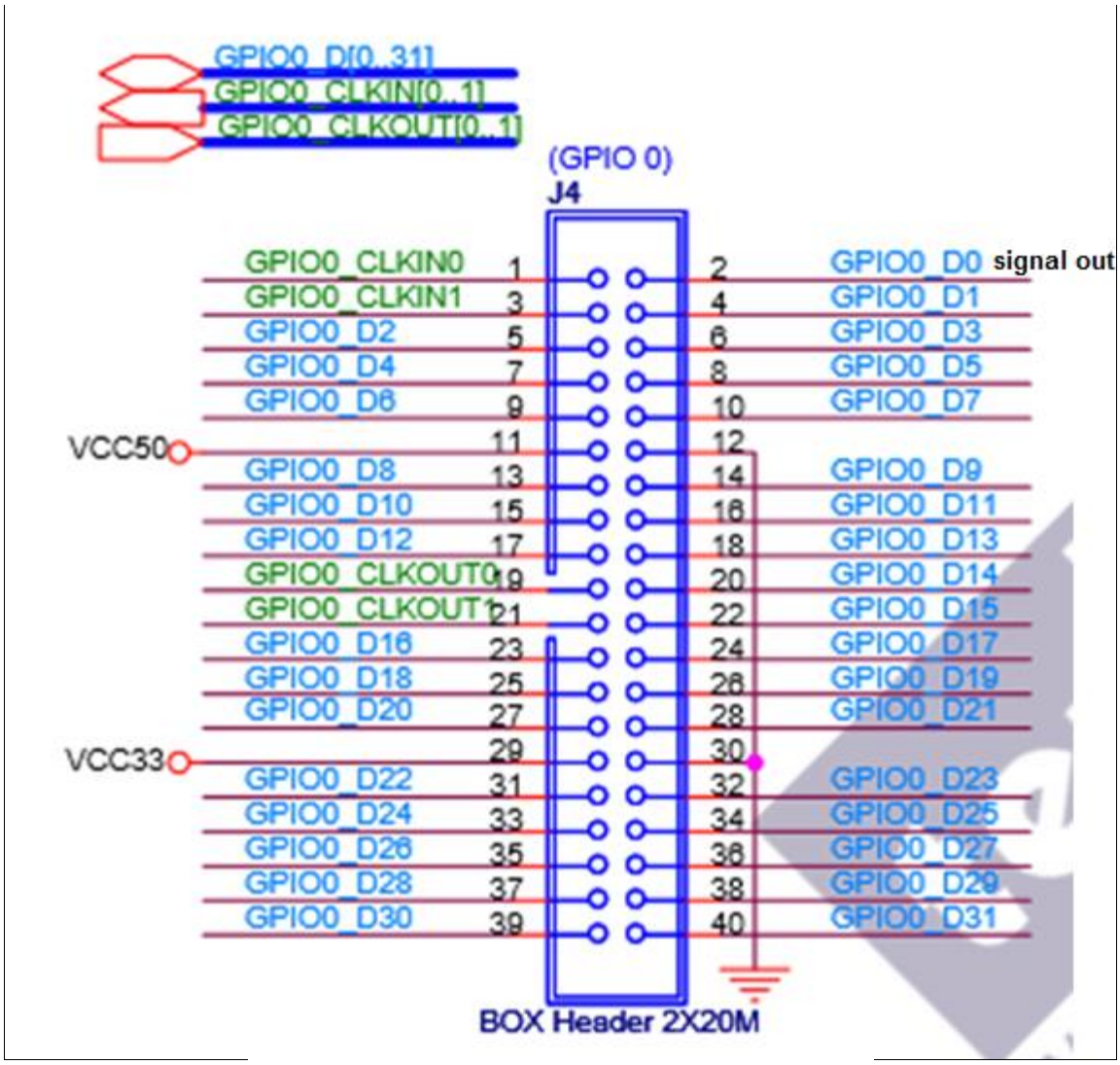
Conclusions.

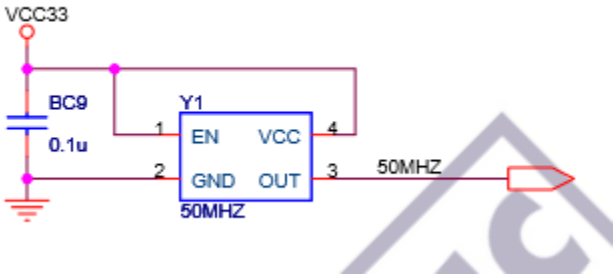
Simple VHDL script that switches the output voltage level on a single pin. Though the signal generated has significant rising and dropping edge noises and the end signal doesn't really seem like a square wave signal, which it should be. Though the frequency is correct.

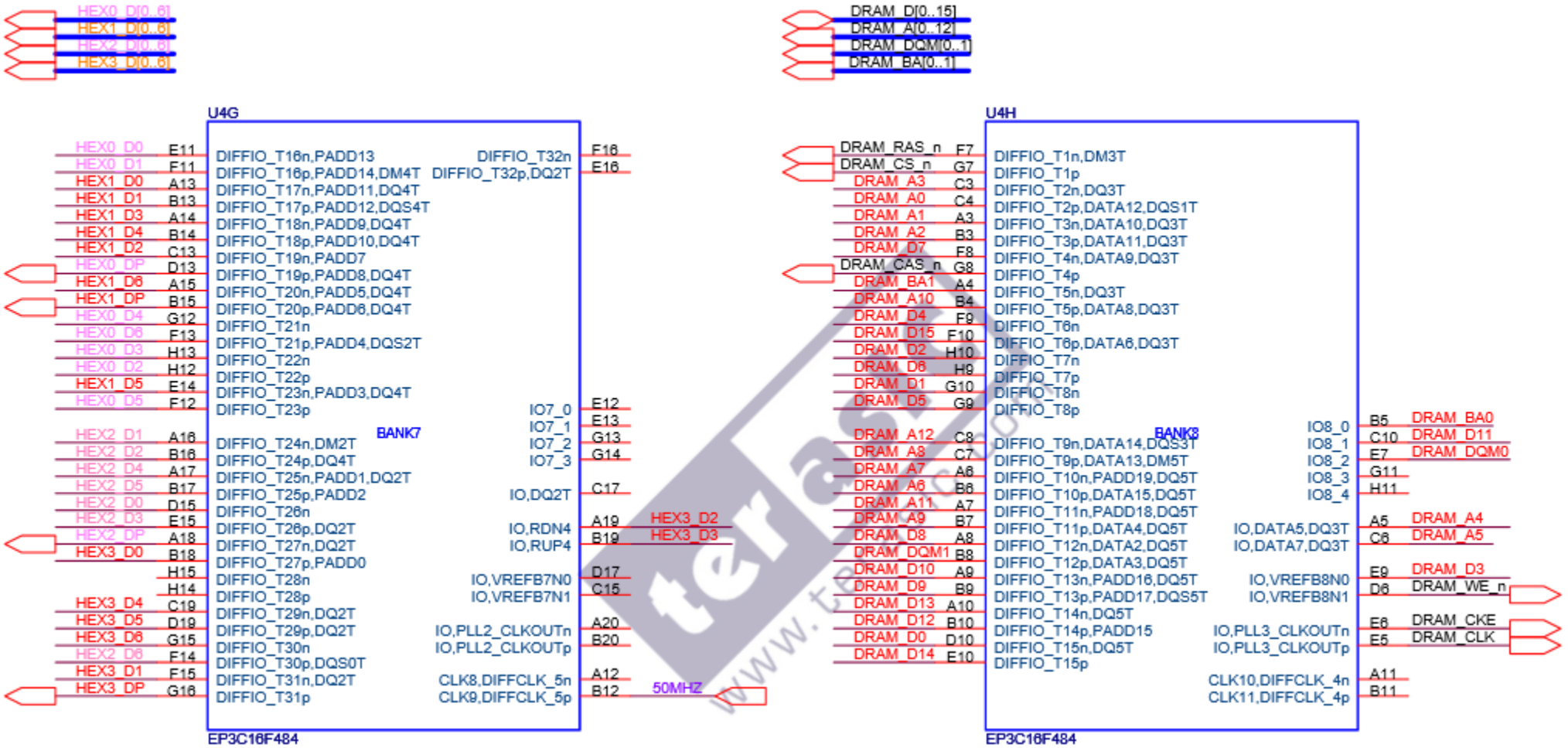
Source code.

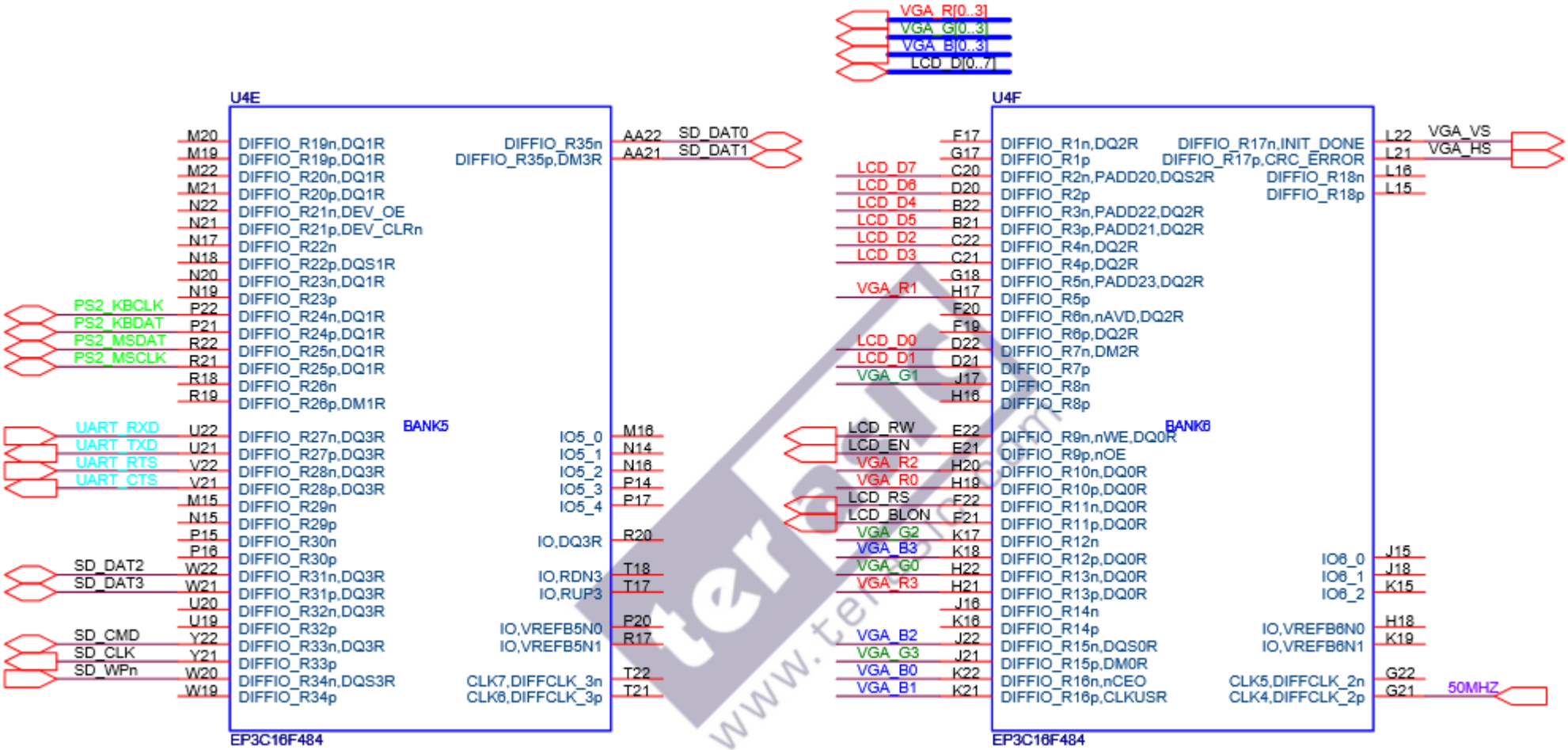
```
01 library ieee;
02 use ieee.std_logic_1164.all;
03
04 entity IESigGen is
05    Port (
06          CLOCK_50 : IN STD_LOGIC;
07          SW : IN STD LOGIC VECTOR(9 DOWNTO 0);
08          KEY : IN STD_LOGIC_VECTOR(2 DOWNTO 0);
09          HEX0 : OUT STD_LOGIC_VECTOR(7 DOWNTO 0);
10          HEX1 : OUT STD_LOGIC_VECTOR(7 DOWNTO 0);
11          HEX2 : OUT STD_LOGIC_VECTOR(7 DOWNTO 0);
12          HEX3 : OUT STD LOGIC VECTOR(7 DOWNTO 0);
13          LEDG : OUT STD_LOGIC_VECTOR(9 downto 0);
14          GPIO_0 : OUT STD_LOGIC_VECTOR(2 DOWNTO 0)
15    );
16 end IESigGen;
17
18 architecture Whatever of IESigGen is
19
20 signal timer_count  : INTEGER := 0;
21 signal counter       : INTEGER := 0;
22
23 begin
24
25    WITH timer_count MOD 2 SELECT GPIO_0 <=
26          "001" WHEN 0,
27          "000" WHEN OTHERS;
28
29    process(CLOCK_50)
30    begin
31          if rising_edge(CLOCK_50) then
32                timer_count <= timer_count + 1;
33                if (timer_count = TIMER_MAX) then
34                      counter <= counter + 1;
35                      timer_count <= 0;
36                end if;
37          end if;
38    end process;
39
40 end Whatever;
```

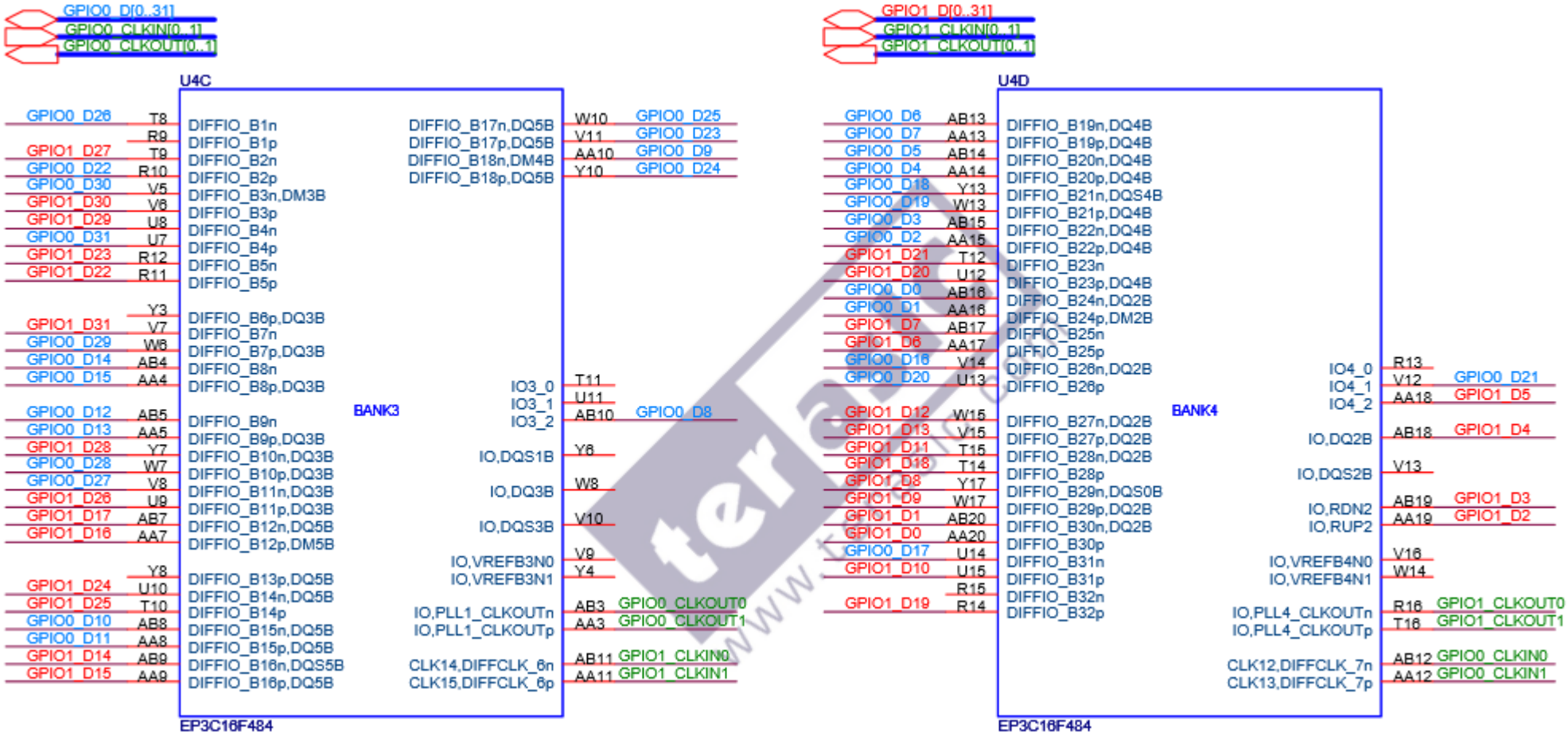
Electrical schemes:

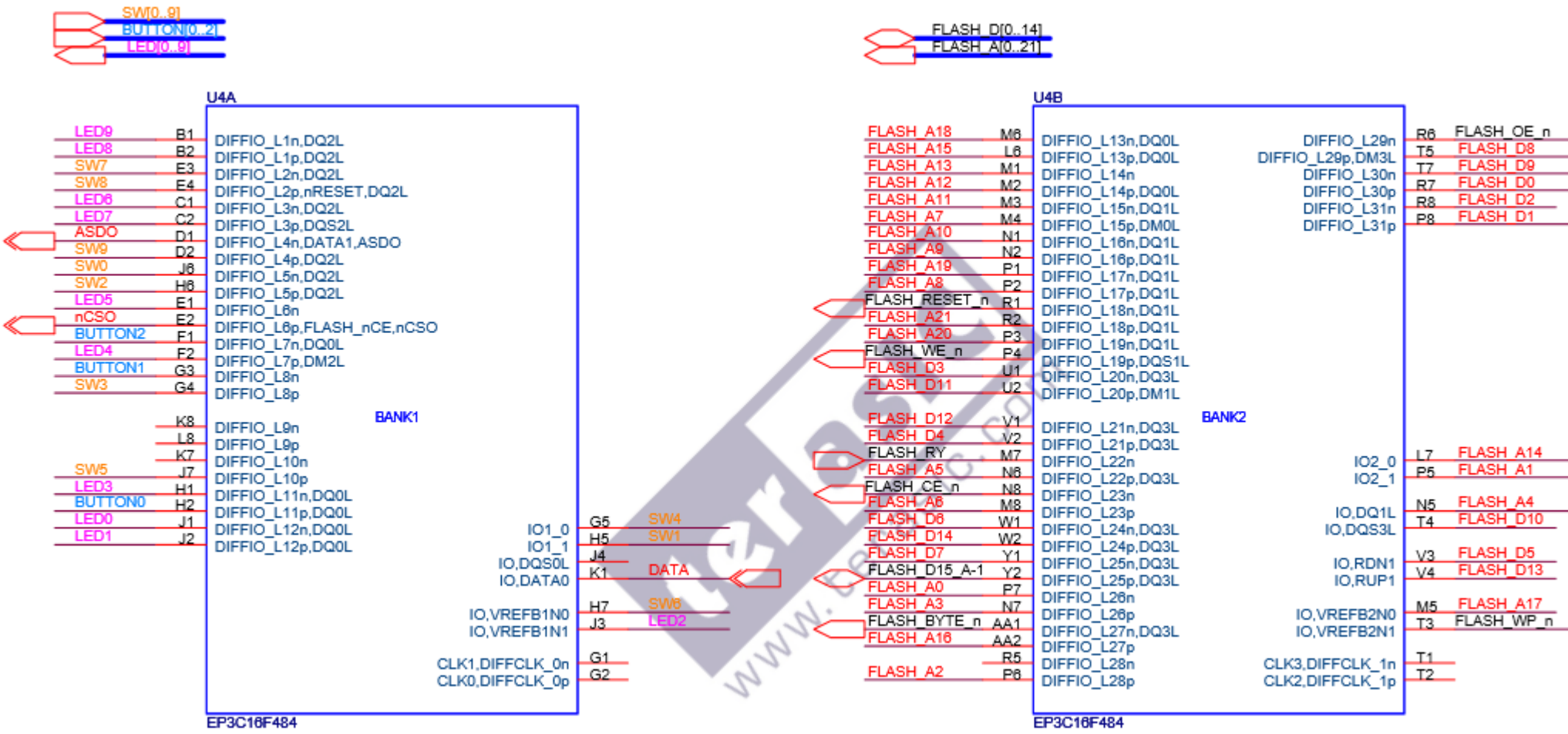





HEX0_D[0..6]
HEX1_D[0..6]
HEX2_D[0..6]
HEX3_D[0..6]
U4G
HEX0_D0 E11
HEX0_D1 F11
HEX1_D0 A13
HEX1_D1 B13
HEX1_D3 A14
HEX1_D4 B14
HEX1_D2 C13
HEX0_DP D13
HEX1_D6 A15
HEX1_DP B15
HEX0_D4 G12
HEX0_D6 F13
HEX0_D3 H13
HEX0_D2 H12
HEX1_D5 E14
HEX0_D5 F12
HEX2_D1 A16
HEX2_D2 B16
HEX2_D4 A17
HEX2_D5 B17
HEX2_D0 D15
HEX2_D3 E15
HEX2_DP A18
HEX3_D0 B18
H15
H14
HEX3_D4 C19
HEX3_D5 D19
HEX3_D6 G15
HEX2_D6 F14
HEX3_D1 F15
HEX3_DP G16
DIFFIO_T16n,PADD13
DIFFIO_T16p,PADD14,DM4T
DIFFIO_T17n,PADD11,DQ4T
DIFFIO_T17p,PADD12,DQS4T
DIFFIO_T18n,PADD9,DQ4T
DIFFIO_T18p,PADD10,DQ4T
DIFFIO_T19n,PADD7
DIFFIO_T19p,PADD8,DQ4T
DIFFIO_T20n,PADD5,DQ4T
DIFFIO_T20p,PADD6,DQ4T
DIFFIO_T21n
DIFFIO_T21p,PADD4,DQS2T
DIFFIO_T22n
DIFFIO_T22p
DIFFIO_T23n,PADD3,DQ4T
DIFFIO_T23p
BANK7
DIFFIO_T24n,DM2T
DIFFIO_T24p,DQ4T
DIFFIO_T25n,PADD1,DQ2T
DIFFIO_T25p,PADD2
DIFFIO_T26n
DIFFIO_T26p,DQ2T
DIFFIO_T27n,DQ2T
DIFFIO_T27p,PADD0
DIFFIO_T28n
DIFFIO_T28p
DIFFIO_T29n,DQ2T
DIFFIO_T29p,DQ2T
DIFFIO_T30n
DIFFIO_T30p,DQS0T
DIFFIO_T31n,DQ2T
DIFFIO_T31p
DIFFIO_T32n F16
DIFFIO_T32p,DQ2T E16
IO7_0 E12
IO7_1 E13
IO7_2 G13
IO7_3 G14
IO,DQ2T C17
IO,RDN4 A19
IO,RUP4 B19
IO,VREFB7N0 D17
IO,VREFB7N1 C15
IO,PLL2_CLKOUTn A20
IO,PLL2_CLKOUTp B20
CLK8,DIFFCLK_5n A12
CLK9,DIFFCLK_5p B12
HEX3_D2
HEX3_D3
50MHZ
EP3C16F484
DRAM_D[0..15]
DRAM_A[0..12]
DRAM_DQM[0..1]
DRAM_BA[0..1]
U4H
DRAM_RAS_n F7
DRAM_CS_n G7
DRAM_A3 C3
DRAM_A0 C4
DRAM_A1 A3
DRAM_A2 B3
DRAM_D7 F8
DRAM_CAS_n G8
DRAM_BA1 A4
DRAM_A10 B4
DRAM_D4 F9
DRAM_D15 F10
DRAM_D2 H10
DRAM_D6 H9
DRAM_D1 G10
DRAM_D5 G9
DRAM_A12 C8
DRAM_A8 C7
DRAM_A7 A6
DRAM_A6 B6
DRAM_A11 A7
DRAM_A9 B7
DRAM_D8 A8
DRAM_DQM1 B8
DRAM_D10 A9
DRAM_D9 B9
DRAM_D13 A10
DRAM_D12 B10
DRAM_D0 D10
DRAM_D14 E10
DIFFIO_T1n,DM3T
DIFFIO_T1p
DIFFIO_T2n,DQ3T
DIFFIO_T2p,DATA12,DQS1T
DIFFIO_T3n,DATA10,DQ3T
DIFFIO_T3p,DATA11,DQ3T
DIFFIO_T4n,DATA9,DQ3T
DIFFIO_T4p
DIFFIO_T5n,DQ3T
DIFFIO_T5p,DATA8,DQ3T
DIFFIO_T6n
DIFFIO_T6p,DATA6,DQ3T
DIFFIO_T7n
DIFFIO_T7p
DIFFIO_T8n
DIFFIO_T8p
BANK8
DIFFIO_T9n,DATA14,DQS3T
DIFFIO_T9p,DATA13,DM5T
DIFFIO_T10n,PADD19,DQ5T
DIFFIO_T10p,DATA15,DQ5T
DIFFIO_T11n,PADD18,DQ5T
DIFFIO_T11p,DATA4,DQ5T
DIFFIO_T12n,DATA2,DQ5T
DIFFIO_T12p,DATA3,DQ5T
DIFFIO_T13n,PADD16,DQ5T
DIFFIO_T13p,PADD17,DQS5T
DIFFIO_T14n,DQ5T
DIFFIO_T14p,PADD15
DIFFIO_T15n,DQ5T
DIFFIO_T15p
IO8_0 B5 DRAM_BA0
IO8_1 C10 DRAM_D11
IO8_2 E7 DRAM_DQM0
IO8_3 G11
IO8_4 H11
IO,DATA5,DQ3T A5 DRAM_A4
IO,DATA7,DQ3T C8 DRAM_A5
IO,VREFB8N0 E9 DRAM_D3
IO,VREFB8N1 D6 DRAM_WE_n
IO,PLL3_CLKOUTn E6 DRAM_CKE
IO,PLL3_CLKOUTp E5 DRAM_CLK
CLK10,DIFFCLK_4n A11
CLK11,DIFFCLK_4p B11
EP3C16F484


VGA_R[0..3]
VGA_G[0..3]
VGA_B[0..3]
LCD_D[0..7]
U4E
M20 DIFFIO_R19n,DQ1R
M19 DIFFIO_R19p,DQ1R
M22 DIFFIO_R20n,DQ1R
M21 DIFFIO_R20p,DQ1R
N22 DIFFIO_R21n,DEV_OE
N21 DIFFIO_R21p,DEV_CLRn
N17 DIFFIO_R22n
N18 DIFFIO_R22p,DQS1R
N20 DIFFIO_R23n,DQ1R
N19 DIFFIO_R23p
PS2_KBCLK P22 DIFFIO_R24n,DQ1R
PS2_KBDAT P21 DIFFIO_R24p,DQ1R
PS2_MSDAT R22 DIFFIO_R25n,DQ1R
PS2_MSCLK R21 DIFFIO_R25p,DQ1R
R18 DIFFIO_R26n
R19 DIFFIO_R26p,DM1R
BANK5
UART_RXD U22 DIFFIO_R27n,DQ3R
UART_TXD U21 DIFFIO_R27p,DQ3R
UART_RTS V22 DIFFIO_R28n,DQ3R
UART_CTS V21 DIFFIO_R28p,DQ3R
M15 DIFFIO_R29n
N15 DIFFIO_R29p
P15 DIFFIO_R30n
P16 DIFFIO_R30p
SD_DAT2 W22 DIFFIO_R31n,DQ3R
SD_DAT3 W21 DIFFIO_R31p,DQ3R
U20 DIFFIO_R32n,DQ3R
U19 DIFFIO_R32p
SD_CMD Y22 DIFFIO_R33n,DQ3R
SD_CLK Y21 DIFFIO_R33p
SD_WPn W20 DIFFIO_R34n,DQS3R
W19 DIFFIO_R34p
DIFFIO_R35n AA22 SD_DAT0
DIFFIO_R35p,DM3R AA21 SD_DAT1
IO5_0 M18
IO5_1 N14
IO5_2 N16
IO5_3 P14
IO5_4 P17
IO,DQ3R R20
IO,RDN3 T18
IO,RUP3 T17
IO,VREFB5N0 P20
IO,VREFB5N1 R17
CLK7,DIFFCLK_3n T22
CLK6,DIFFCLK_3p T21
EP3C16F484
U4F
F17 DIFFIO_R1n,DQ2R
G17 DIFFIO_R1p
LCD_D7 C20 DIFFIO_R2n,PADD20,DQS2R
LCD_D6 D20 DIFFIO_R2p
LCD_D4 B22 DIFFIO_R3n,PADD22,DQ2R
LCD_D5 B21 DIFFIO_R3p,PADD21,DQ2R
LCD_D2 C22 DIFFIO_R4n,DQ2R
LCD_D3 C21 DIFFIO_R4p,DQ2R
G18 DIFFIO_R5n,PADD23,DQ2R
VGA_R1 H17 DIFFIO_R5p
F20 DIFFIO_R6n,nAVD,DQ2R
F19 DIFFIO_R6p,DQ2R
LCD_D0 D22 DIFFIO_R7n,DM2R
LCD_D1 D21 DIFFIO_R7p
VGA_G1 J17 DIFFIO_R8n
H16 DIFFIO_R8p
BANK6
LCD_RW E22 DIFFIO_R9n,nWE,DQ0R
LCD_EN E21 DIFFIO_R9p,nOE
VGA_R2 H20 DIFFIO_R10n,DQ0R
VGA_R0 H19 DIFFIO_R10p,DQ0R
LCD_RS F22 DIFFIO_R11n,DQ0R
LCD_BLON F21 DIFFIO_R11p,DQ0R
VGA_G2 K17 DIFFIO_R12n
VGA_B3 K18 DIFFIO_R12p,DQ0R
VGA_G0 H22 DIFFIO_R13n,DQ0R
VGA_R3 H21 DIFFIO_R13p,DQ0R
J16 DIFFIO_R14n
K16 DIFFIO_R14p
VGA_B2 J22 DIFFIO_R15n,DQS0R
VGA_G3 J21 DIFFIO_R15p,DM0R
VGA_B0 K22 DIFFIO_R16n,nCEO
VGA_B1 K21 DIFFIO_R16p,CLKUSR
DIFFIO_R17n,INIT_DONE L22 VGA_VS
DIFFIO_R17p,CRC_ERROR L21 VGA_HS
DIFFIO_R18n L16
DIFFIO_R18p L15
IO6_0 J15
IO6_1 J18
IO6_2 K15
IO,VREFB6N0 H18
IO,VREFB6N1 K19
CLK5,DIFFCLK_2n G22
CLK4,DIFFCLK_2p G21 50MHZ
EP3C16F484


GPIO0_D[0..31]
GPIO0_CLKIN[0..1]
GPIO0_CLKOUT[0..1]
U4C
GPIO0_D26 T8
R9
GPIO1_D27 T9
GPIO0_D22 R10
GPIO0_D30 V5
GPIO1_D30 V6
GPIO1_D29 U8
GPIO0_D31 U7
GPIO1_D23 R12
GPIO1_D22 R11
Y3
GPIO1_D31 V7
GPIO0_D29 W6
GPIO0_D14 AB4
GPIO0_D15 AA4
GPIO0_D12 AB5
GPIO0_D13 AA5
GPIO1_D28 Y7
GPIO0_D28 W7
GPIO0_D27 V8
GPIO1_D26 U9
GPIO1_D17 AB7
GPIO1_D16 AA7
Y8
GPIO1_D24 U10
GPIO1_D25 T10
GPIO0_D10 AB8
GPIO0_D11 AA8
GPIO1_D14 AB9
GPIO1_D15 AA9
DIFFIO_B1n
DIFFIO_B1p
DIFFIO_B2n
DIFFIO_B2p
DIFFIO_B3n,DM3B
DIFFIO_B3p
DIFFIO_B4n
DIFFIO_B4p
DIFFIO_B5n
DIFFIO_B5p
DIFFIO_B6p,DQ3B
DIFFIO_B7n
DIFFIO_B7p,DQ3B
DIFFIO_B8n
DIFFIO_B8p,DQ3B
DIFFIO_B9n
DIFFIO_B9p,DQ3B
DIFFIO_B10n,DQ3B
DIFFIO_B10p,DQ3B
DIFFIO_B11n,DQ3B
DIFFIO_B11p,DQ3B
DIFFIO_B12n,DQ5B
DIFFIO_B12p,DM5B
DIFFIO_B13p,DQ5B
DIFFIO_B14n,DQ5B
DIFFIO_B14p
DIFFIO_B15n,DQ5B
DIFFIO_B15p,DQ5B
DIFFIO_B16n,DQS5B
DIFFIO_B16p,DQ5B
BANK3
DIFFIO_B17n,DQ5B W10 GPIO0_D25
DIFFIO_B17p,DQ5B V11 GPIO0_D23
DIFFIO_B18n,DM4B AA10 GPIO0_D9
DIFFIO_B18p,DQ5B Y10 GPIO0_D24
IO3_0 T11
IO3_1 U11
IO3_2 AB10 GPIO0_D8
IO,DQS1B Y6
IO,DQ3B W8
IO,DQS3B V10
IO,VREFB3N0 V9
IO,VREFB3N1 Y4
IO,PLL1_CLKOUTn AB3 GPIO0_CLKOUT0
IO,PLL1_CLKOUTp AA3 GPIO0_CLKOUT1
CLK14,DIFFCLK_6n AB11 GPIO1_CLKIN0
CLK15,DIFFCLK_6p AA11 GPIO1_CLKIN1
EP3C16F484
GPIO1_D[0..31]
GPIO1_CLKIN[0..1]
GPIO1_CLKOUT[0..1]
U4D
GPIO0_D6 AB13
GPIO0_D7 AA13
GPIO0_D5 AB14
GPIO0_D4 AA14
GPIO0_D18 Y13
GPIO0_D19 W13
GPIO0_D3 AB15
GPIO0_D2 AA15
GPIO1_D21 T12
GPIO1_D20 U12
GPIO0_D0 AB16
GPIO0_D1 AA16
GPIO1_D7 AB17
GPIO1_D6 AA17
GPIO0_D16 V14
GPIO0_D20 U13
GPIO1_D12 W15
GPIO1_D13 V15
GPIO1_D11 T15
GPIO1_D10 T14
GPIO1_D8 Y17
GPIO1_D9 W17
GPIO1_D1 AB20
GPIO1_D0 AA20
GPIO0_D17 U14
GPIO1_D10 U15
R15
GPIO1_D19 R14
DIFFIO_B19n,DQ4B
DIFFIO_B19p,DQ4B
DIFFIO_B20n,DQ4B
DIFFIO_B20p,DQ4B
DIFFIO_B21n,DQS4B
DIFFIO_B21p,DQ4B
DIFFIO_B22n,DQ4B
DIFFIO_B22p,DQ4B
DIFFIO_B23n
DIFFIO_B23p,DQ4B
DIFFIO_B24n,DQ2B
DIFFIO_B24p,DM2B
DIFFIO_B25n
DIFFIO_B25p
DIFFIO_B26n,DQ2B
DIFFIO_B26p
DIFFIO_B27n,DQ2B
DIFFIO_B27p,DQ2B
DIFFIO_B28n,DQ2B
DIFFIO_B28p
DIFFIO_B29n,DQS0B
DIFFIO_B29p,DQ2B
DIFFIO_B30n,DQ2B
DIFFIO_B30p
DIFFIO_B31n
DIFFIO_B31p
DIFFIO_B32n
DIFFIO_B32p
BANK4
IO4_0 R13
IO4_1 V12 GPIO0_D21
IO4_2 AA18 GPIO1_D5
IO,DQ2B AB18 GPIO1_D4
IO,DQS2B V13
IO,RDN2 AB19 GPIO1_D3
IO,RUP2 AA19 GPIO1_D2
IO,VREFB4N0 V16
IO,VREFB4N1 W14
IO,PLL4_CLKOUTn R16 GPIO1_CLKOUT0
IO,PLL4_CLKOUTp T16 GPIO1_CLKOUT1
CLK12,DIFFCLK_7n AB12 GPIO0_CLKIN0
CLK13,DIFFCLK_7p AA12 GPIO0_CLKIN1
EP3C16F484


SW[0..9]
BUTTON[0..2]
LED[0..9]
U4A
LED9 B1
LED8 B2
SW7 E3
SW8 E4
LED6 C1
LED7 C2
ASDO D1
SW9 D2
SW0 J6
SW2 H6
LED5 E1
nCSO E2
BUTTON2 F1
LED4 F2
BUTTON1 G3
SW3 G4
K8
L8
K7
SW5 J7
LED3 H1
BUTTON0 H2
LED0 J1
LED1 J2
DIFFIO_L1n,DQ2L
DIFFIO_L1p,DQ2L
DIFFIO_L2n,DQ2L
DIFFIO_L2p,nRESET,DQ2L
DIFFIO_L3n,DQ2L
DIFFIO_L3p,DQS2L
DIFFIO_L4n,DATA1,ASDO
DIFFIO_L4p,DQ2L
DIFFIO_L5n,DQ2L
DIFFIO_L5p,DQ2L
DIFFIO_L6n
DIFFIO_L6p,FLASH_nCE,nCSO
DIFFIO_L7n,DQ0L
DIFFIO_L7p,DM2L
DIFFIO_L8n
DIFFIO_L8p
BANK1
DIFFIO_L9n
DIFFIO_L9p
DIFFIO_L10n
DIFFIO_L10p
DIFFIO_L11n,DQ0L
DIFFIO_L11p,DQ0L
DIFFIO_L12n,DQ0L
DIFFIO_L12p,DQ0L
IO1_0 G5 SW4
IO1_1 H5 SW1
IO,DQS0L J4
IO,DATA0 K1 DATA
IO,VREFB1N0 H7 SW6
IO,VREFB1N1 J3 LED2
CLK1,DIFFCLK_0n G1
CLK0,DIFFCLK_0p G2
EP3C16F484
FLASH_D[0..14]
FLASH_A[0..21]
U4B
FLASH_A18 M6
FLASH_A15 L6
FLASH_A13 M1
FLASH_A12 M2
FLASH_A11 M3
FLASH_A7 M4
FLASH_A10 N1
FLASH_A9 N2
FLASH_A19 P1
FLASH_A8 P2
FLASH_RESET_n R1
FLASH_A21 R2
FLASH_A20 P3
FLASH_WE_n P4
FLASH_D3 U1
FLASH_D11 U2
FLASH_D12 V1
FLASH_D4 V2
FLASH_RY M7
FLASH_A5 N6
FLASH_CE_n N8
FLASH_A6 M8
FLASH_D6 W1
FLASH_D14 W2
FLASH_D7 Y1
FLASH_D15_A-1 Y2
FLASH_A0 P7
FLASH_A3 N7
FLASH_BYTE_n AA1
FLASH_A16 AA2
R5
FLASH_A2 P6
DIFFIO_L13n,DQ0L
DIFFIO_L13p,DQ0L
DIFFIO_L14n
DIFFIO_L14p,DQ0L
DIFFIO_L15n,DQ1L
DIFFIO_L15p,DM0L
DIFFIO_L16n,DQ1L
DIFFIO_L16p,DQ1L
DIFFIO_L17n,DQ1L
DIFFIO_L17p,DQ1L
DIFFIO_L18n,DQ1L
DIFFIO_L18p,DQ1L
DIFFIO_L19n,DQ1L
DIFFIO_L19p,DQS1L
DIFFIO_L20n,DQ3L
DIFFIO_L20p,DM1L
BANK2
DIFFIO_L21n,DQ3L
DIFFIO_L21p,DQ3L
DIFFIO_L22n
DIFFIO_L22p,DQ3L
DIFFIO_L23n
DIFFIO_L23p
DIFFIO_L24n,DQ3L
DIFFIO_L24p,DQ3L
DIFFIO_L25n,DQ3L
DIFFIO_L25p,DQ3L
DIFFIO_L26n
DIFFIO_L26p
DIFFIO_L27n,DQ3L
DIFFIO_L27p
DIFFIO_L28n
DIFFIO_L28p
DIFFIO_L29n R6 FLASH_OE_n
DIFFIO_L29p,DM3L T5 FLASH_D8
DIFFIO_L30n T7 FLASH_D9
DIFFIO_L30p R7 FLASH_D0
DIFFIO_L31n R8 FLASH_D2
DIFFIO_L31p P8 FLASH_D1
IO2_0 L7 FLASH_A14
IO2_1 P5 FLASH_A1
IO,DQ1L N5 FLASH_A4
IO,DQS3L T4 FLASH_D10
IO,RDN1 V3 FLASH_D5
IO,RUP1 V4 FLASH_D13
IO,VREFB2N0 M5 FLASH_A17
IO,VREFB2N1 T3 FLASH_WP_n
CLK3,DIFFCLK_1n T1
CLK2,DIFFCLK_1p T2
EP3C16F484