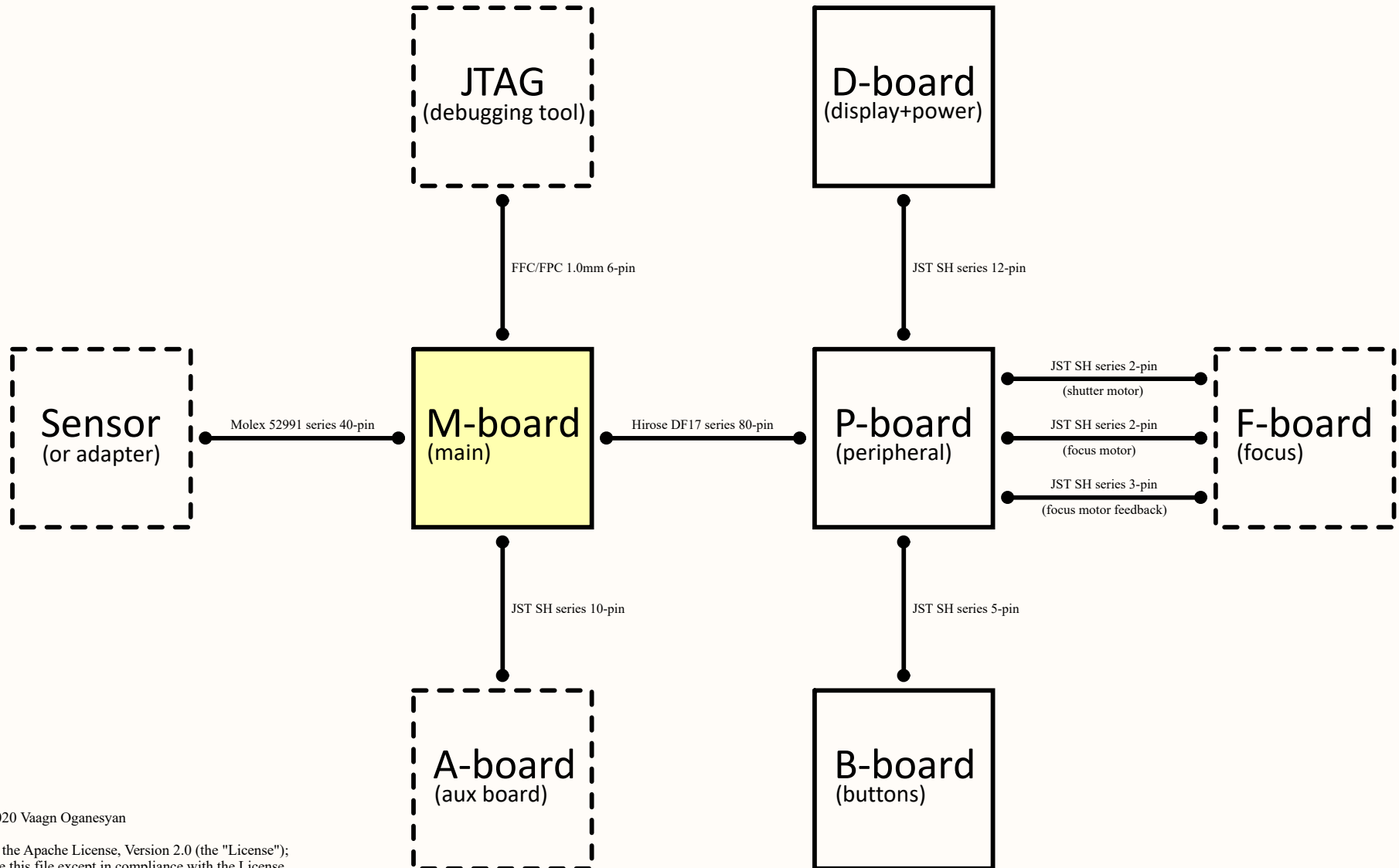
 - optional



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Title: M-board.Header		
File: 0_HEADER.SchDoc	Size: A4	
Drawn by: Vaagn Oganessian	Version: v0.2.0	
Date: 07.09.2020	Time: 16:43:13	Sheet: 1 of 6

OpenRV

Sensor connector

X1 connector reflects ISC0901B0 sensor pinout. ISC0901B0 uses 6 digital lines for control and 3 different power rails. Most of other connector pins are connected to ground.

To have an ability to support more different sensors, some backward compatible changes to original ISC0901B0 connector pinout were made:

1. NC pins are connected to VCC_SYS to provide additional power source.
2. All power rails, except VCC_SYS, are designed to be adjustable to meet individual sensor power requirements.
3. Ground pins 5, 6, 10, 12, 14, 15, 19, 25, 26, 28, 30, 34, 35, 36 were transformed into IO lines and connected to FPGA.

R6 resistor pull-up may be useful to detect if ISC0901B0 board is attached.

WARNING!

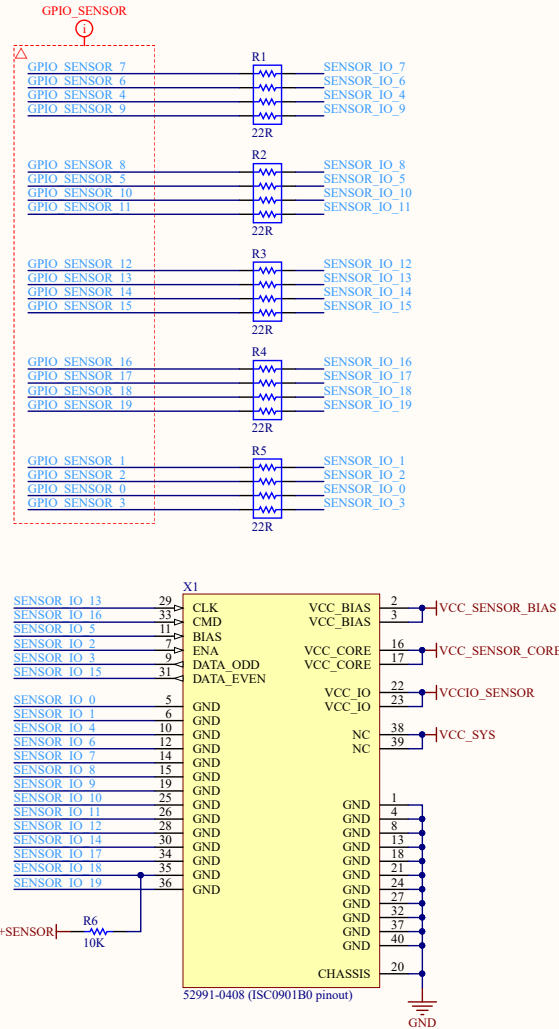
This warning is mostly for those users, who would like to use this hardware in their own way. You MUST BE EXTREMELY CAREFULL while matching different devices/adapters attached to X1 connector with different FPGA bitstreams and different power rail voltages at X1.

Bad scenario examples:

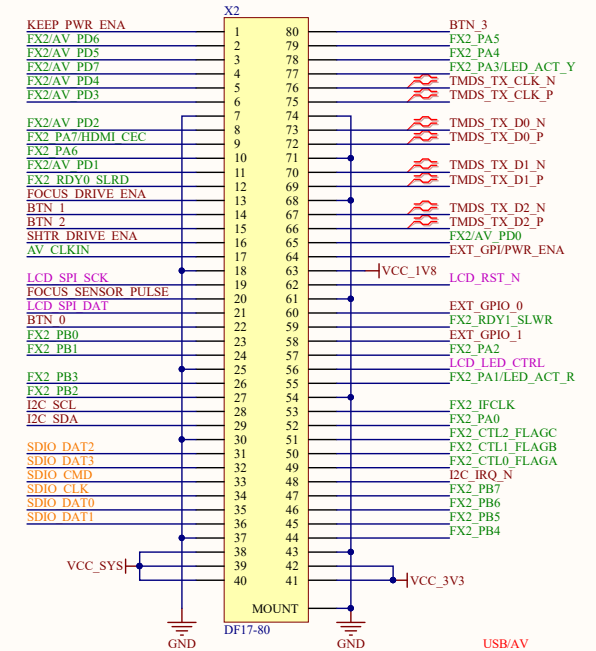
1. If you attach some custom board to X1, that, for example, expects 1V2 voltage at VCC_SENSOR_CORE lines, while there is actually 3V3, that may cause a damage to your attached device.
2. If you attach some custom board to X1 that drives digital IO lines with logic "High" levels higher than VCCIO_SENSOR, that will cause a damage to FPGA.
3. Loading FPGA with your custom bitstream, that drives IO lines that are shared with ground at X1 while ISC0901B0 sensor board is attached, will cause short circuit of these lines to ground. Shorted IO current will overdrive IO buffers, bank power, cause an overheat and possibly damage FPGA.

.....
N. Any other bad or non-thought-out idea.

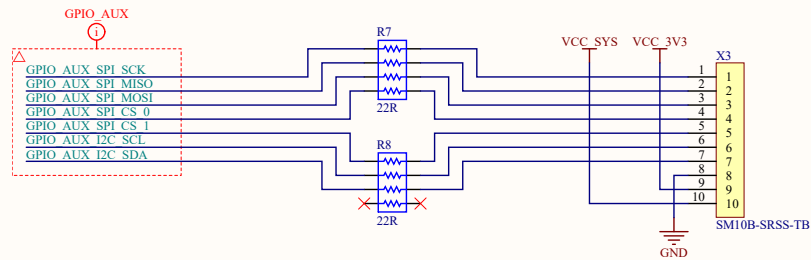
If you would like to develop your own custom HDL design on current hardware, consider to base it on a special safe "empty" project with all possible stubs, that will be provided later.



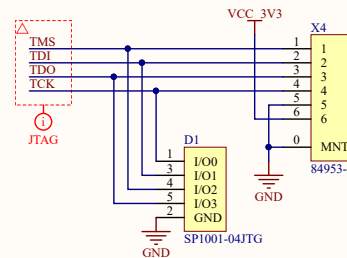
Peripheral board connector



AUX connector



JTAG



Title: M-board.Connectors

File: 1_CONNECTORS.SchDoc

Size: A3

Drawn by: Vaagn Oganessyan

Version: v0.2.0

Date: 07.09.2020 Time: 16:43:14

Sheet: 2 of 6

OpenIRV

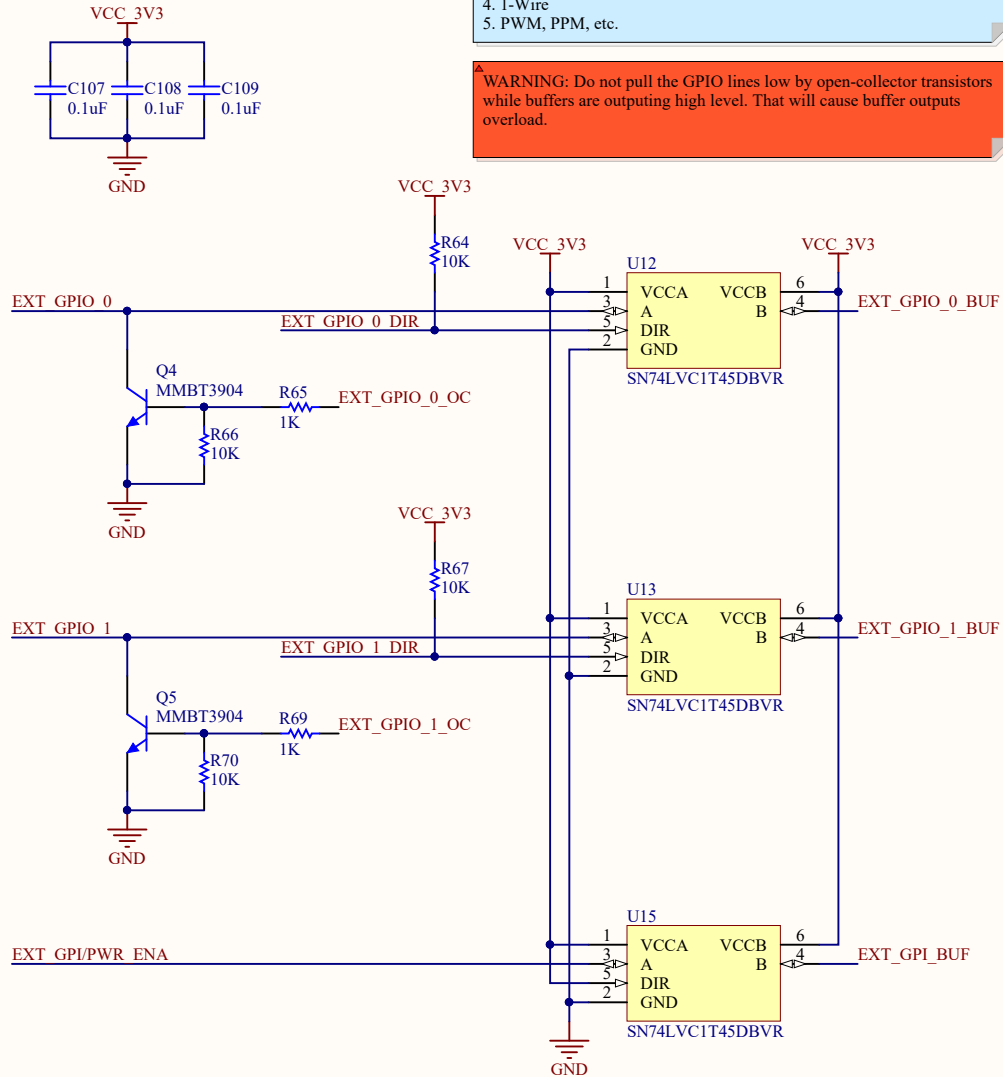
GPIO_EXT buffers

EXT_GPIO[1:0] are configurable input/output, push-pull/open-collector.
EXT_GPI is input only.

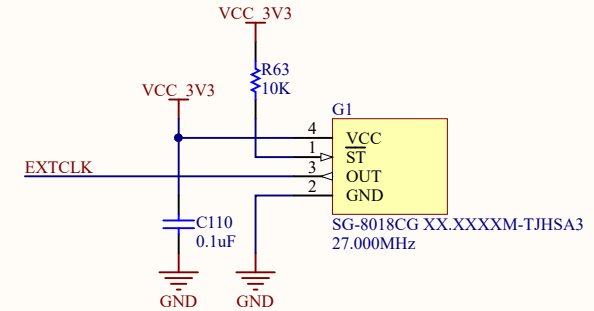
Supports master/slave interfaces:

1. SPI (3-wire)
2. UART
3. I2C
4. 1-Wire
5. PWM, PPM, etc.

WARNING: Do not pull the GPIO lines low by open-collector transistors while buffers are outputting high level. That will cause buffer outputs overload.

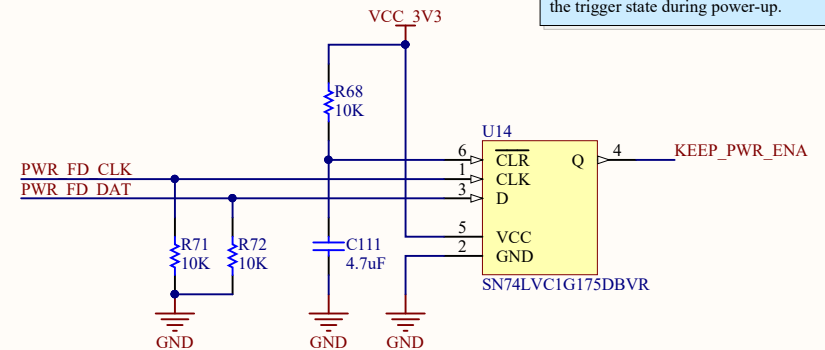


Clock generator



Power keep logic

This trigger keeps main power path enabled during FPGA (re)configuration. RC delay (47ms) at the CLR pin resets the trigger state during power-up.



Title: M-board.Miscellaneous

File: 2_MISC.SchDoc

Size: A4

Drawn by: Vaagn Oganessian

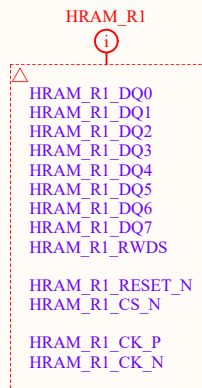
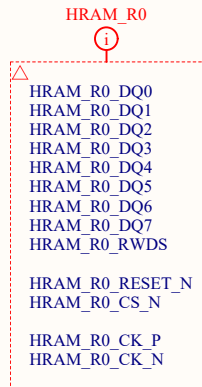
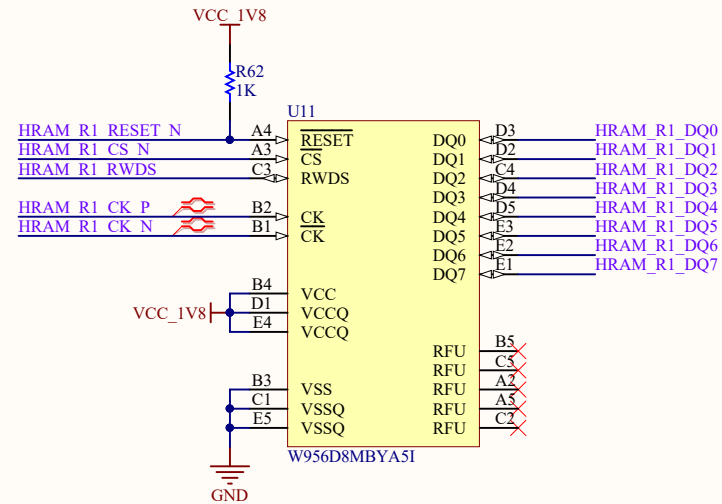
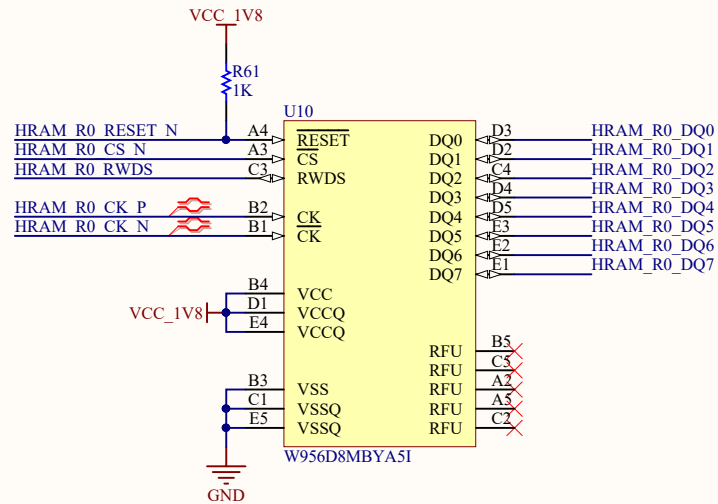
Version: v0.2.0

Date: 07.09.2020 Time: 16:43:14

Sheet: 3 of 6

OpenRV

RAM



Two HyperRAM memory ICs are connected to FPGA over two independent 8-bit HyperBUS interfaces. Depending on memory controller mode, both ranks may work fully independently even with different clock frequencies or can be combined in a single memory area with a 16-bit bus width, that will increase memory throughput twice.

Pull-ups at RESET_N inputs allow to keep HyperRAM memory in non-reseted state, while FPGA is being (re)configured. This feature allows to save memory content (i.e. internal MCU context), while switching from one FPGA configuration to another. Switching between different configurations may be useful if you can actually interleave your hardware in time, when all modules cannot be fitted in a single bitstream and you do not need to keep them working simultaneously.

Title: M-board.RAM	
File: 3_RAM.SchDoc	Size: A4
Drawn by: Vaagn Oganessian	Version: v0.2.0
Date: 07.09.2020	Time: 16:43:14
Sheet: 4	of 6

OpenRV

NK 16
C for 7S25)

I0_I2N_T0_VREF_16
I0_L11P_T1_SRCC_16
I0_L11N_T1_SRCC_16
I0_L12P_T1_MRCC_16
I0_L12N_T1_MRCC_16
I0_L13P_T2_MRCC_16
I0_L13N_T2_MRCC_16
I0_L14P_T2_SRCC_16
I0_L14N_T2_SRCC_16
I0_L19N_T3_VREF_16

I10
I11
I12
I13
I14
I15

GPIO_SENSOR_19
GPIO_SENSOR_2
GPIO_SENSOR_1
GPIO_SENSOR_3
GPIO_SENSOR_0
GPIO_SENSOR_0

0-ICSGA324C

FPGA I2C Master ID

I2C_SCL
I2C_SDA
I2C_S_SCL

FPGA I2C Slave ID

I2C_S_SCL
I2C_S_SDA

NT1
NT2

FPGA design contains both I2C master and slave modules on the same bus, along with other master/slave devices outside of the FPGA. To simplify HDL design, external connection to the common I2C signals was implemented rather than internal.

Diagram illustrating the configuration bank of an FPGA (Xilinx UGA70) connected to a flash memory (CNFG_FLASH).

The FPGA pins are connected to the flash memory pins as follows:

- FPGA Pin 15 (CS) is connected to Flash Pin 1 (CS).
- FPGA Pin 16 (CLK) is connected to Flash Pin 2 (CLK).
- FPGA Pin 19 (GND) is connected to Flash Pin 3 (GND).
- FPGA Pin 4 (GND) is connected to Flash Pin 4 (GND).
- FPGA Pin 8 (VCC) is connected to Flash Pin 5 (VCC).
- FPGA Pin 9 (DI000) is connected to Flash Pin 6 (MISO0).
- FPGA Pin 10 (DI001) is connected to Flash Pin 7 (MISO1).
- FPGA Pin 11 (WP/IO) is connected to Flash Pin 8 (MISO2).
- FPGA Pin 12 (HOLD RST/IO) is connected to Flash Pin 9 (MISO3).
- FPGA Pin 17 (MISO0) is connected to Flash Pin 10 (MISO0).
- FPGA Pin 18 (MISO1) is connected to Flash Pin 11 (MISO1).
- FPGA Pin 20 (MISO2) is connected to Flash Pin 12 (MISO2).
- FPGA Pin 21 (MISO3) is connected to Flash Pin 13 (MISO3).

Additional components shown include resistors (R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21) and a capacitor (C20).

Notes:

- Xilinx UGA70 user guide: Other density memories are supported, except those that cannot fit a single bitstream.
- Xilinx UGA70 user guide: At a max clock frequency of 65MHz in 4-bit mode bitstream can be reloaded in about 68ms.

U1F

BANK 0

TCK_0
TDO_0
TDI_0
TMS_0
DONE_0
INIT_B_0
PROGRAM_B_0
CCLK_0
M0_0
M1_0
M2_0
CFGBVS_0
VREFP_0
VREFN_0
VP_0
VN_0
DXP_0
DXN_0

D9
F8
F9
F9
V8
F8
F8
F8
F8
T10
T10
T9
V9
K10
J2
H10
F9
L10
L9

R22 4.7K
R23 4.7K
R24 10K
R25 4.7K
R26 4.7K

TCK
TDO
TDI
TMS
FPGA_DONE
FPGA_INIT_B
FPGA_PROG_B

CNFG_CLK

VCC_3V3
GND
VCC_3V3

M[2:0] = 001
(Master SPI boot mode)

XC7S50-1CSGA324C

Title: M-board.FPGA

