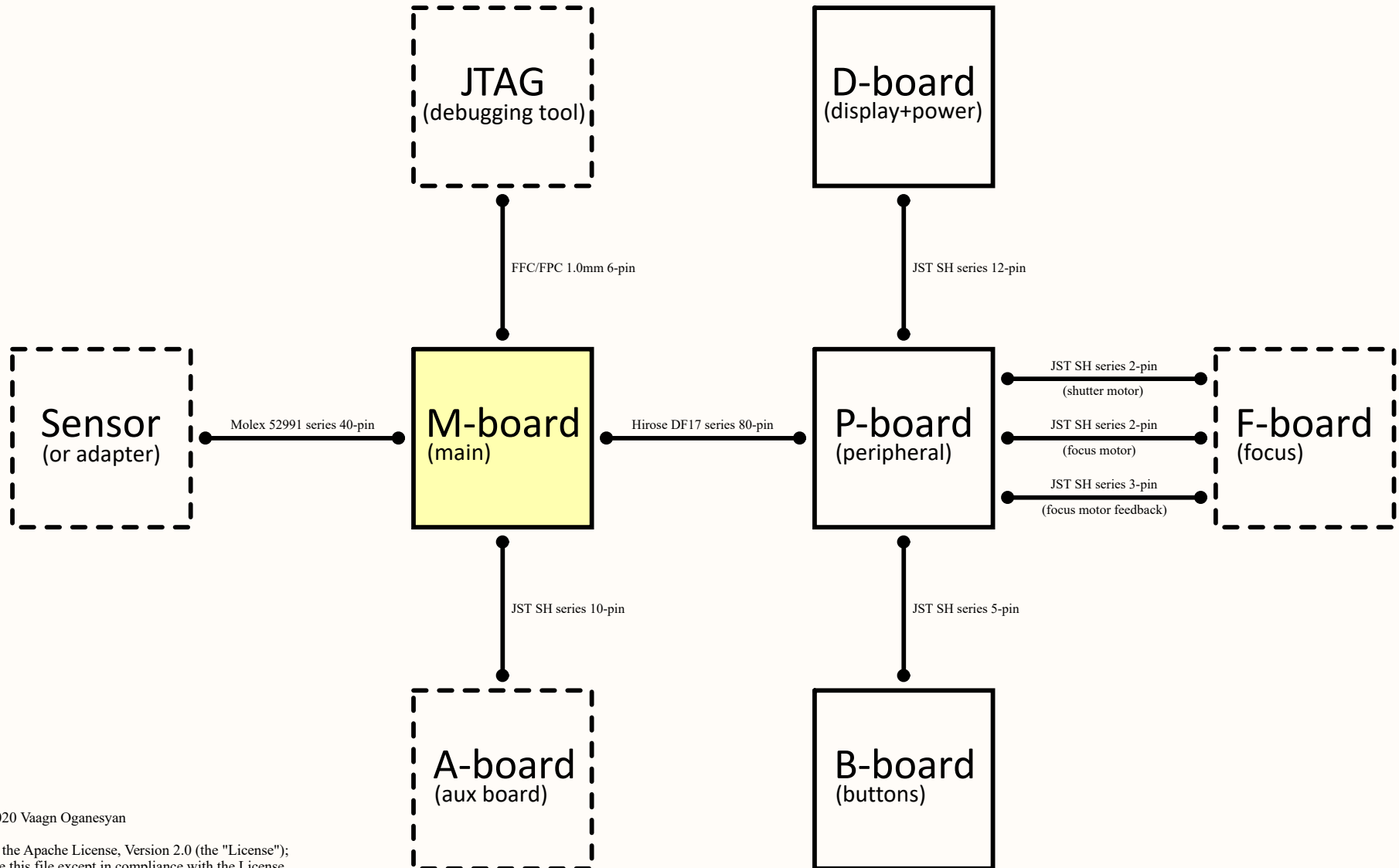
 - optional



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Title: M-board.Header	
File: 0_Header.SchDoc	Size: A4
Drawn by: Vaagn Oganessian	Version: v0.1.0
Date: 01.09.2020 Time: 0:31:16	Sheet: 1 of 6

OpenRV

Sensor connector

X1 connector reflects ISC0901B0 sensor pinout. ISC0901B0 uses 6 digital lines for control and 3 different power rails. Most of other connector pins are connected to ground.

To have an ability to support more different sensors, some backward compatible changes to original ISC0901B0 connector pinout were made:

1. NC pins are connected to VCC_SYS to provide additional power source.
2. All power rails, except VCC_SYS, are designed to be adjustable to meet individual sensor power requirements.
3. Ground pins 5, 10, 12, 14, 15, 19, 25, 26, 28, 34, 35, 36 were transformed into IO lines and connected to FPGA.

R6 resistor pull-up may be useful to detect if ISC0901B0 board is attached.

WARNING!

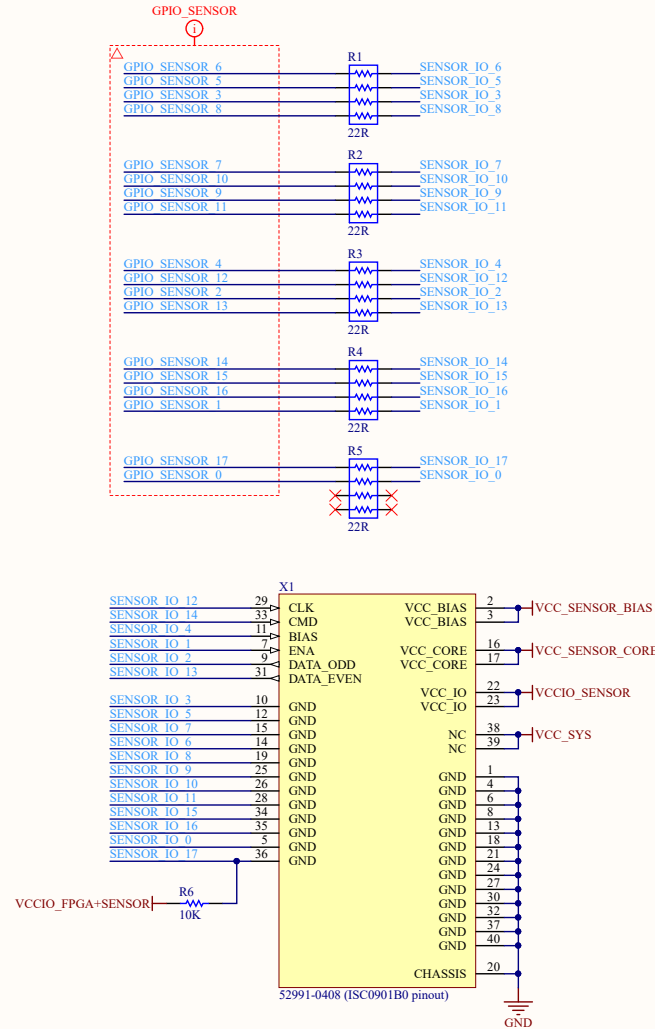
This warning is mostly for those users, who would like to use this hardware in their own way. You MUST BE EXTREMELY CAREFULL while matching different devices/adapters attached to X1 connector with different FPGA bitstreams and different power rail voltages at X1.

Bad scenario examples:

1. If you attach some custom board to X1, that, for example, expects 1V2 voltage at VCC_SENSOR_CORE lines, while there is actually 3V3, that may cause a damage to your attached device.
2. If you attach some custom board to X1 that drives digital IO lines with logic "High" levels higher than VCCIO_SENSOR, that will cause a damage to FPGA.
3. Loading FPGA with your custom bitstream, that drives IO lines that are shared with ground at X1 while ISC0901B0 sensor board is attached, will cause short circuit of these lines to ground. Shorted IO current will overdrive IO buffers, bank power, cause an overheat and possibly damage FPGA.

N. Any other bad or non-thought-out idea.

If you would like to develop your own custom HDL design on current hardware, consider to base it on a special safe "empty" project with all possible stubs, that will be provided later.



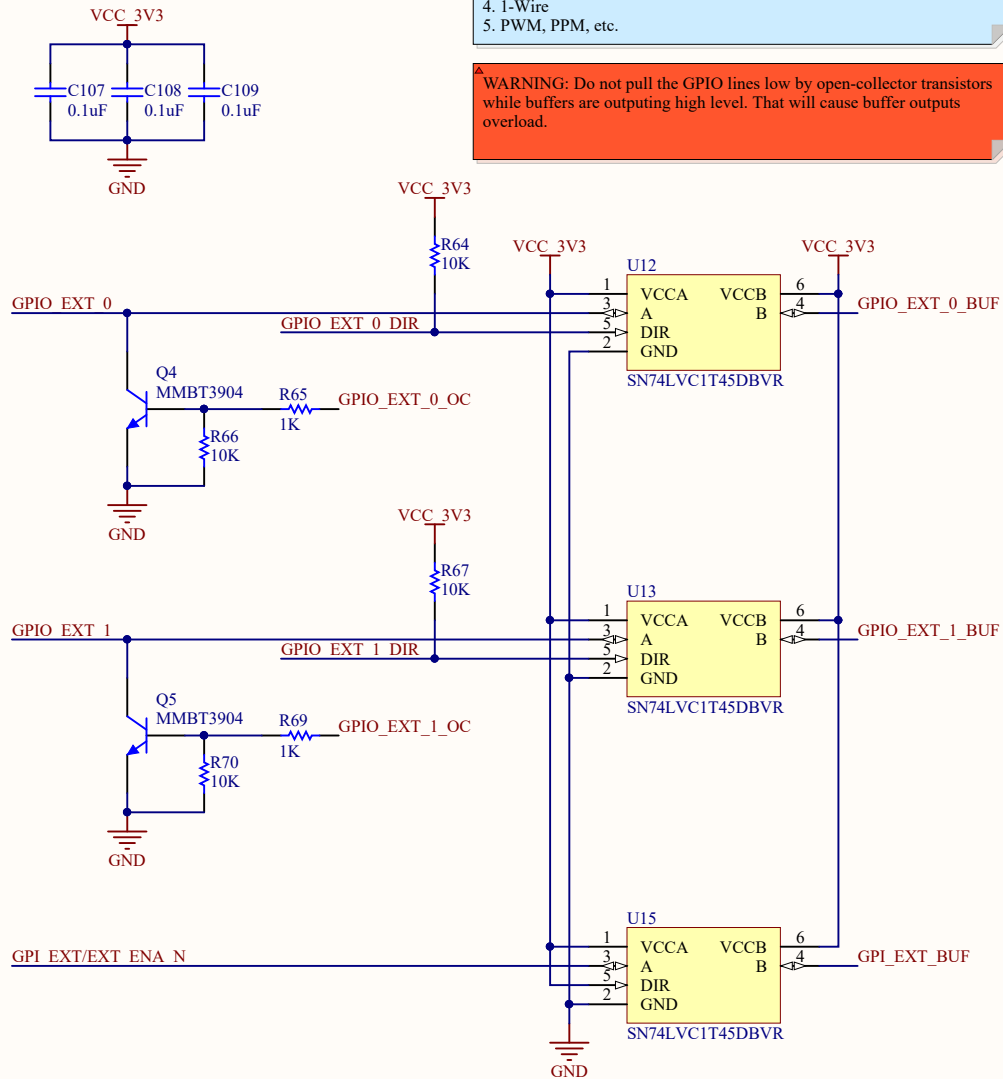
GPIO_EXT buffers

GPIO_EXT[1:0] are configurable input/output, push-pull/open-collector.
GPI_EXT is input only.

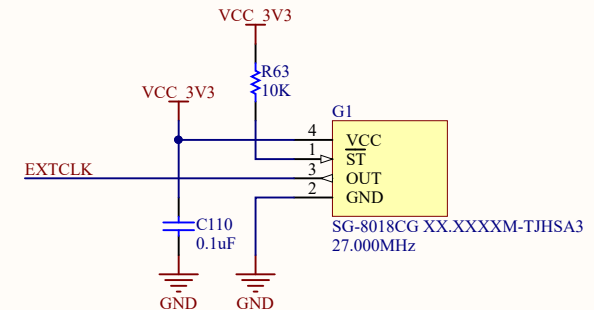
Supports master/slave interfaces:

1. SPI (3-wire)
2. UART
3. I2C
4. 1-Wire
5. PWM, PPM, etc.

WARNING: Do not pull the GPIO lines low by open-collector transistors while buffers are outputting high level. That will cause buffer outputs overload.

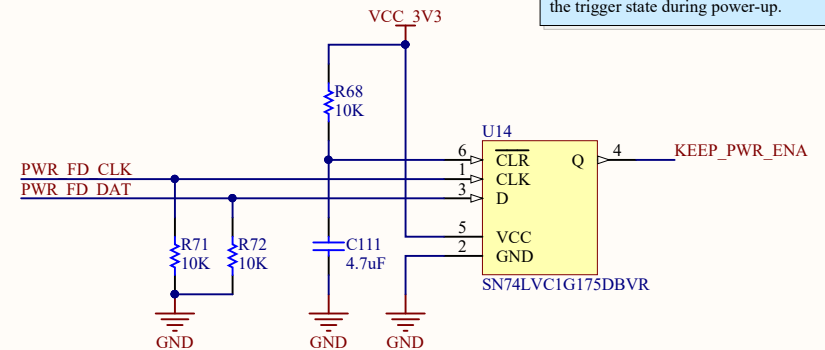


Clock generator



Power keep logic

This trigger keeps main power path enabled during FPGA (re)configuration. RC delay (47ms) at the CLR pin resets the trigger state during power-up.



Title: M-board.Miscellaneous

File: 2_MISC.SchDoc

Size: A4

Drawn by: Vaagn Oganessian

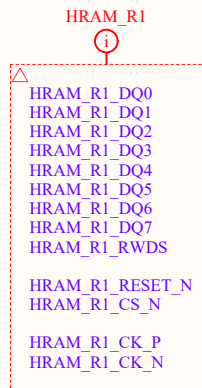
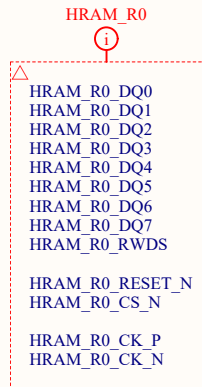
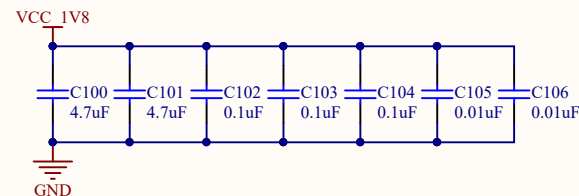
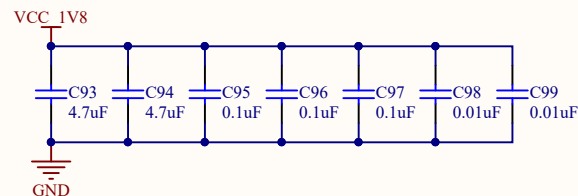
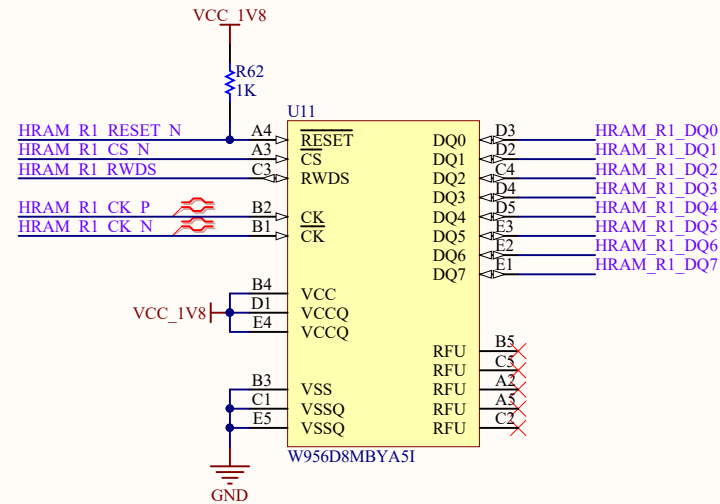
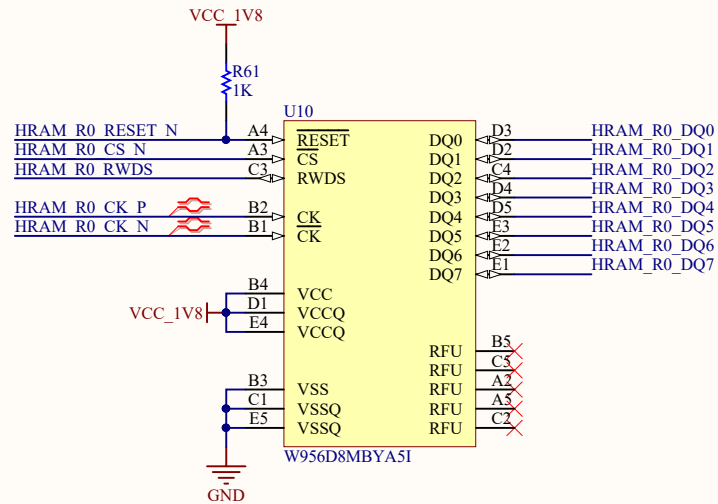
Version: v0.1.0

Date: 01.09.2020 Time: 0:31:16

Sheet: 3 of 6

OpenRV

RAM



Two HyperRAM memory ICs are connected to FPGA over two independent 8-bit HyperBUS interfaces. Depending on memory controller mode, both ranks may work fully independently even with different clock frequencies or can be combined in a single memory area with a 16-bit bus width, that will increase memory throughput twice.

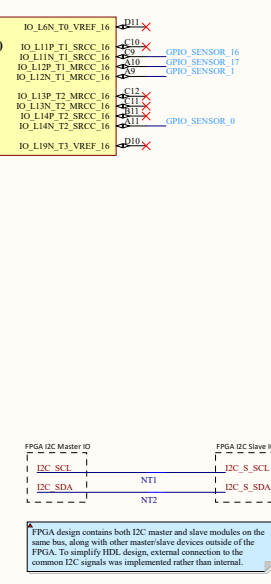
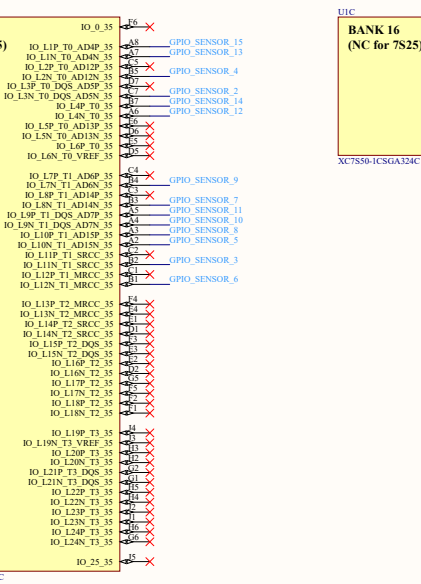
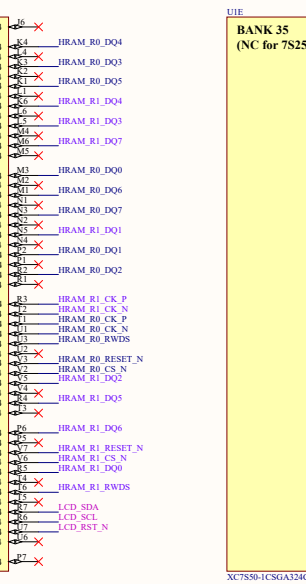
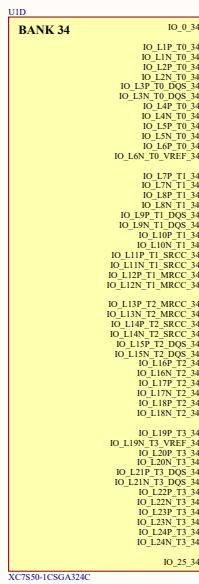
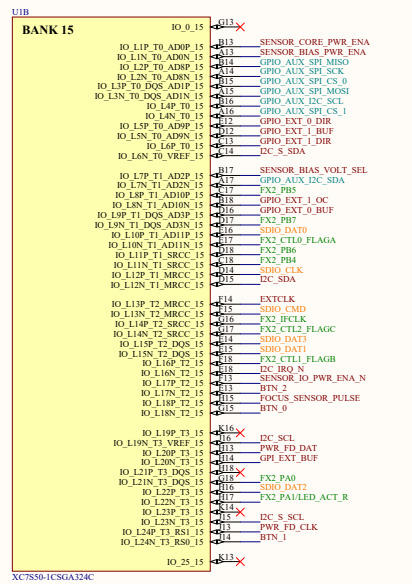
Pull-ups at RESET_N inputs allow to keep HyperRAM memory in non-reseted state, while FPGA is being (re)configured. This feature allows to save memory content (i.e. internal MCU context), while switching from one FPGA configuration to another. Switching between different configurations may be useful if you can actually interleave your hardware in time, when all modules cannot be fitted in a single bitstream and you do not need to keep them working simultaneously.

Title: M-board.RAM	
File: 3_RAM.SchDoc	Size: A4
Drawn by: Vaagn Oganessian	Version: v0.1.0
Date: 01.09.2020	Time: 0:31:16
Sheet: 4 of 6	

OpenRV

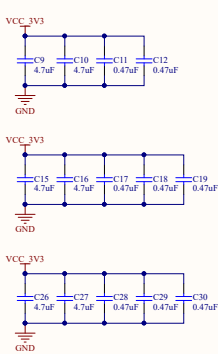
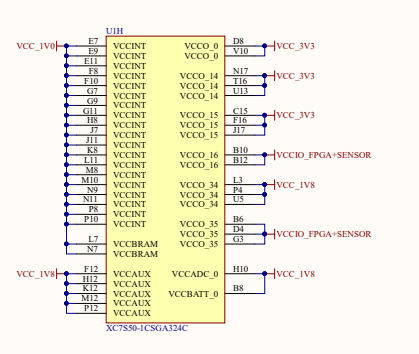
U1A	IO_24	
BANK 1		
IO_L1P_TO_D00_M0SI_14	X	R17 CNFG_M0SI/M0S0
IO_L1N_TO_D01_DIN_14	X	R18 CNFG_M0SI/M0S1
IO_L2P_TO_D02_14	X	R19 CNFG_M0S2
IO_L2N_TO_D03_14	X	R15 CNFG_M0S3
IO_L3P_TO_D05_PUDC_B_14	X	R9
IO_L3N_TO_D06_EMCC1_14	X	R16 FX2_P02 4.7k \rightarrow I-GND
IO_L4P_TO_D04_14	X	R17 FX2_P01
IO_L4N_TO_D05_14	X	R18 FX2_P01_CTRL
IO_L4P_TO_D06_14	X	R19 CNFG_CS_N
IO_L5N_TO_D07_14	X	
IO_L6P_TO_PCS_B_14	X	
IO_L6N_TO_D08_VREF_14	X	
IO_L7P_T1_D09_14	X	M16 FX2_P03
IO_L7N_T1_D10_14	X	R17 GPIO_EXT_0_OC
IO_L8P_T1_D11_14	X	R18 FX2_PA2
IO_L8N_T1_D12_14	X	R19 FX2_RDV1_SLWR
IO_L9P_T1_D05_14	X	R17 FX2AV_P00
IO_L9N_T1_D06_D13_14	X	R18 FOCUS_DRIVE_ENA
IO_L10P_T1_D14_14	X	R19 TMDX_TX_D2_P
IO_L10N_T1_D15_14	X	R17 TMDX_TX_D2_P
IO_L11P_T1_SRCC_14	X	R18 FX2_PA7
IO_L11N_T1_SRCC_14	X	R19 FX2AV_PD1
IO_L12P_T1_MRCC_14	X	R17 FX2_P00
IO_L12N_T1_MRCC_14	X	R18 FX2_RDV0_SLRD
IO_L13P_T2_MRCC_14	X	R14 TMDX_TX_CLK_P
IO_L13N_T2_MRCC_14	X	R15 TMDX_TX_CLK_N
IO_L14P_T2_SRCC_14	X	R17 SHTR_DRIVE_ENA
IO_L14N_T2_SRCC_14	X	R18 TMDX_TX_D1_P
IO_L15P_T2_DRDR_WB_14	X	R19 TMDX_TX_D1_P
IO_L15N_T2_DRDR_C01_14	X	R17 TMDX_TX_D0_P
IO_L16P_T2_CSI_B_14	X	R18 TMDX_TX_D0_P
IO_L16N_T2_D01_14	X	R19 TMDX_TX_D0_P
IO_L17P_T2_D30_14	X	R15 FX2_PA6
IO_L17N_T2_D29_14	X	
IO_L18P_T2_D28_14	X	
IO_L18N_T2_D27_14	X	
IO_L19P_T3_D26_14	X	R13 AV_CLKIN
IO_L19N_T3_D25_VREF_14	X	R14 FX2AV_PD2
IO_L20P_T3_D24_14	X	R15 FX2_P5
IO_L20N_T3_D23_14	X	R16 FX2_P0A
IO_L21P_T3_D08_14	X	R17 JUNKOR_HWS_BOOST_PWR_ENA
IO_L21N_T3_D06_D12_14	X	R18 BTN_3
IO_L22P_T3_D21_14	X	R19 FX2AV_PD5
IO_L22N_T3_D20_14	X	R17 FX2AV_PD4
IO_L23P_T3_D17_14	X	R18 FX2AV_PD6
IO_L23N_T3_D18_14	X	R19 FX2_PASILED_ACT_Y
IO_L24P_T3_D17_14	X	R17 FX2AV_PD7
IO_L24N_T3_D16_14	X	R18 FX2AV_PD3
IO_25_14		

XC7S50-ICSGA32C



The figure displays three circuit diagrams illustrating different decoupling capacitor topologies connected to a VCC supply and ground (GND):

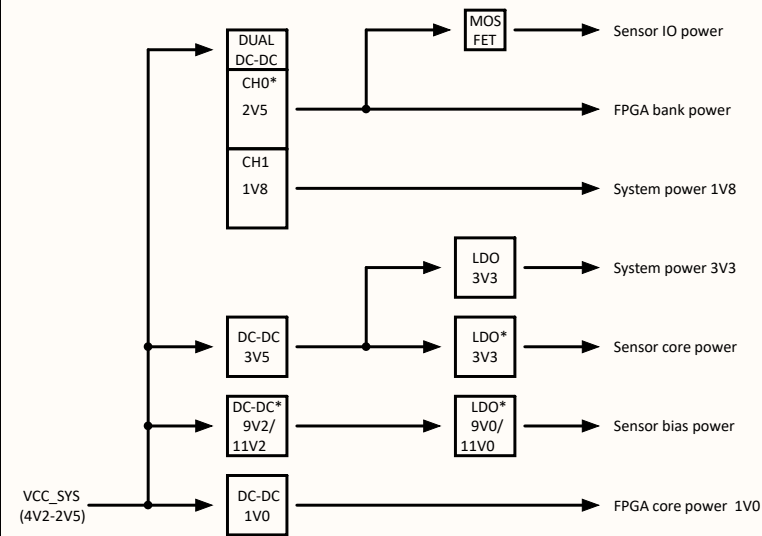
- Top Diagram:** A series chain of eight capacitors (C1 through C8) connected between VCC_I/V0 and GND. Each capacitor has a value of 4.7nF.
- Middle Diagram:** A parallel pair of capacitors (C13 and C14) connected between VCC_I/V0 and GND. Each capacitor has a value of 4.7nF.
- Bottom Diagram:** A parallel chain of five capacitors (C21 through C25) connected between VCC_I/V8 and GND. Each capacitor has a value of 4.7nF.

[illegible]

Title: M-board.FPGA	
File: 4_FPGA.SchDoc	Size: A2
Drawn by: Vaagn Ogenesyan	Version: v0.1.0
Date: 01.09.2020 Time: 0:31:17	Sheet: 5 of 6

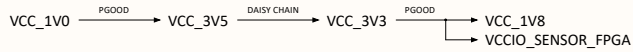
OpenIRV

Power delivery scheme



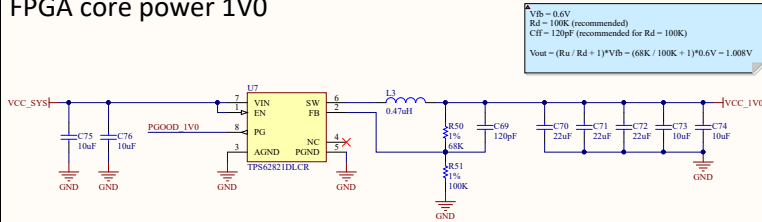
* only this regulator voltages can be modified to meet sensor's special power requirements if necessary

Power sequencing

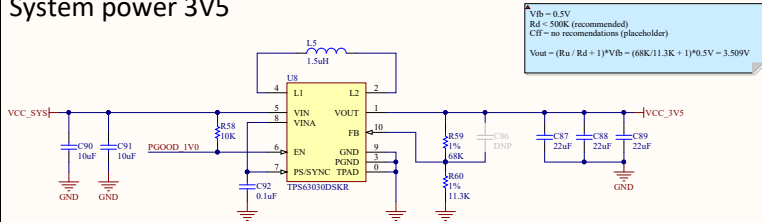


NOTE: All other power rails can be each enabled/disabled individually

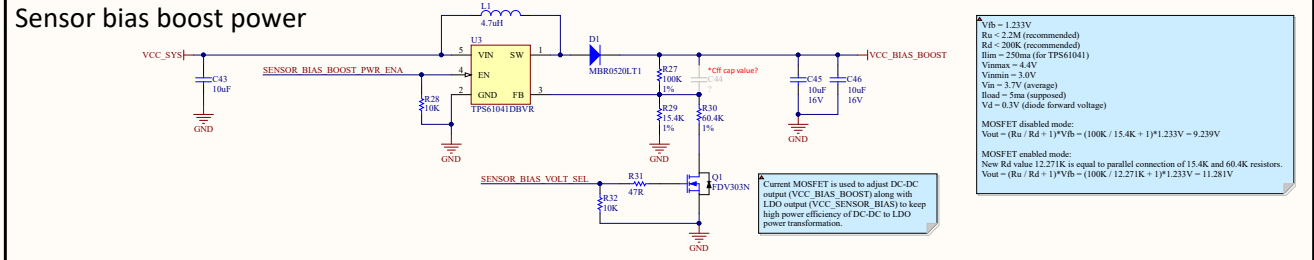
FPGA core power 1V0



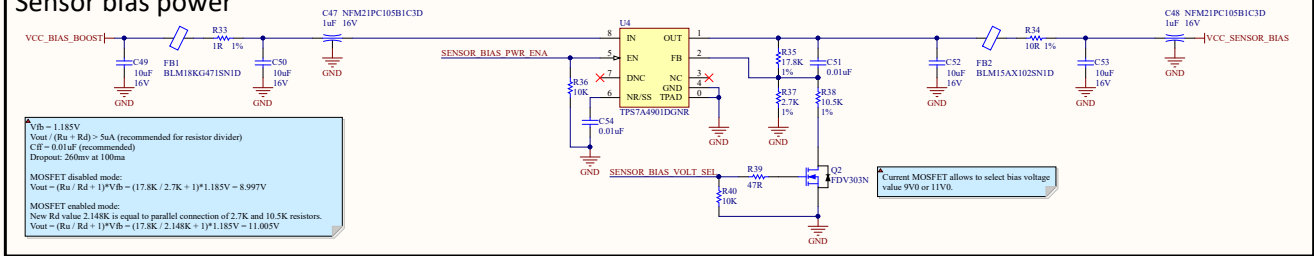
System power 3V5



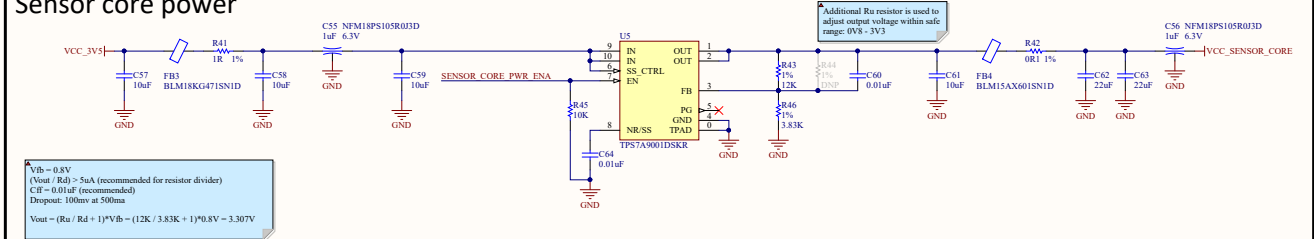
Sensor bias boost power



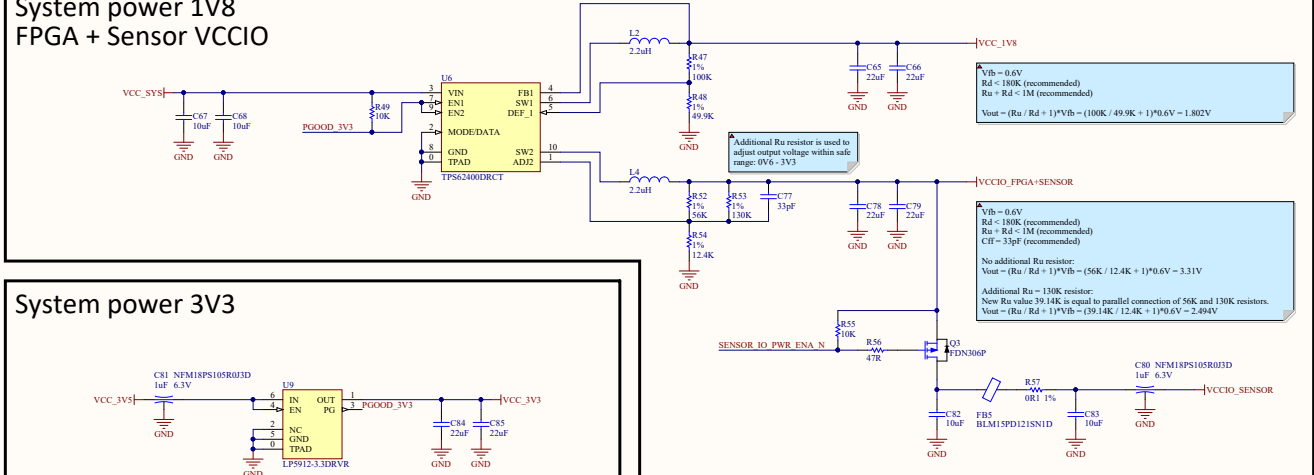
Sensor bias power



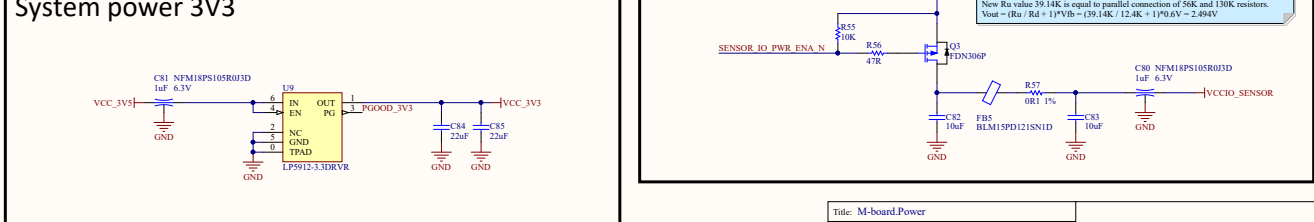
Sensor core power



System power 1V8 FPGA + Sensor VCCIO



System power 3V3



Title: M-board Power	Size: A2
File: 5_POWER_SchDoc	Version: v0.1.0
Drawn by: Vaagn Oganeyan	Sheet: 6 of 6
Date: 01.09.2020	Time: 0:31:17

OpenIRV