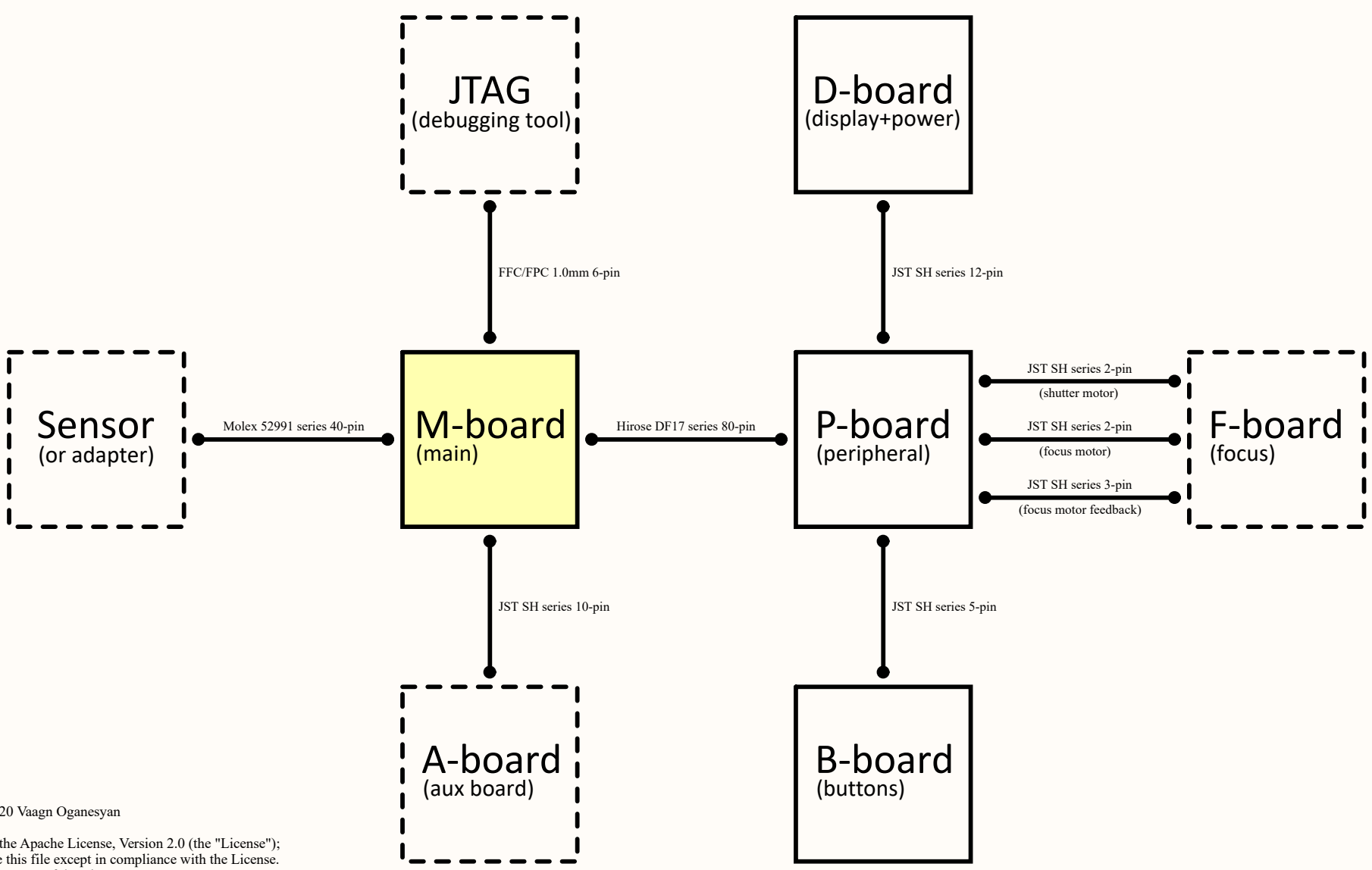


Title: M-board.Header		
File: 0_HEADER.SchDoc	Size: A4	OpenIRV
Drawn by: Vaagn Oganesyan	Version: v0.2.0	
Date: 07.09.2020 Time: 16:43:13	Sheet: 1 of 6	

Sensor connector

X1 connector reflects ISC0901B0 sensor pinout. ISC0901B0 uses 6 digital lines for control and 3 different power rails. Most of other connector pins are connected to ground.

To have an ability to support more different sensors, some backward compatible changes to original ISC0901B0 connector pinout were made:

1. NC pins are connected to VCC_SYS to provide additional power source.
2. All power rails, except VCC_SYS, are designed to be adjustable to meet individual sensor power requirements.
3. Ground pins 5, 6, 10, 12, 14, 15, 19, 25, 26, 28, 30, 34, 35, 36 were transformed into IO lines and connected to FPGA.

R6 resistor pull-up may be useful to detect if ISC0901B0 board is attached.

WARNING!

This warning is mostly for those users, who would like to use this hardware in their own way. You MUST BE EXTREMLY CAREFULL while matching different devices/adapters attached to X1 connector with different FPGA bitstreams and different power rail voltages at X1.

Bad scenario examples:

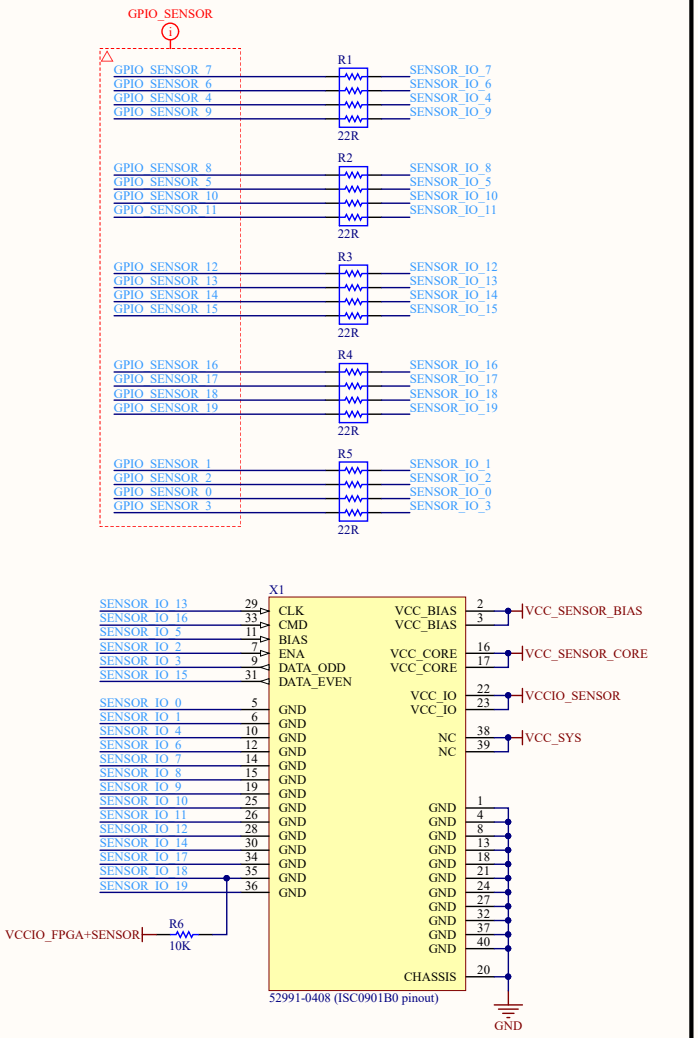
1. If you attach some custom board to X1, that, for example, expects 1V2 voltage at VCC_SENSOR_CORE lines, while there is actually 3V3, that may cause a damage to your attached device.

2. If you attach some custom board to X1 that drives digital IO lines with logic "High" levels higher than VCCIO_SENSOR, that will cause a damage to FPGA.

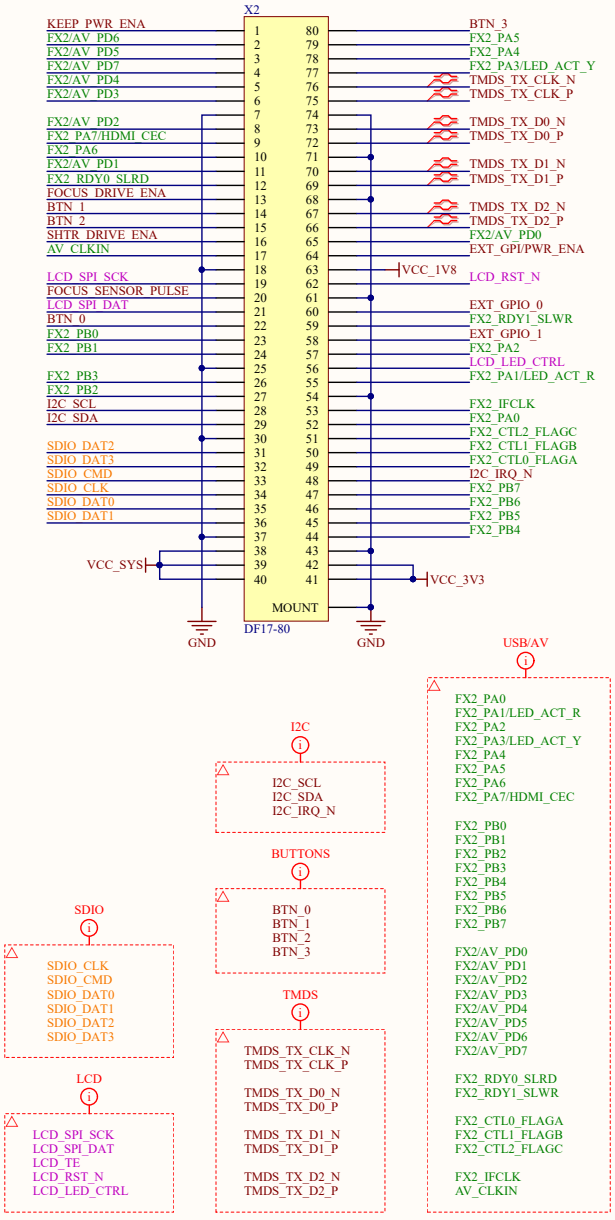
3. Loading FPGA with your custom bistream, that drives IO lines that are shared with ground at X1 while ISC0901B0 sensor board is attached, will cause short circuit of these lines to ground. Shorted IO current will overdrive IO buffers, bank power, cause an overheat and possibly damage FPGA.

.....
.....
.....
N. Any other bad or non-thought-out idea.

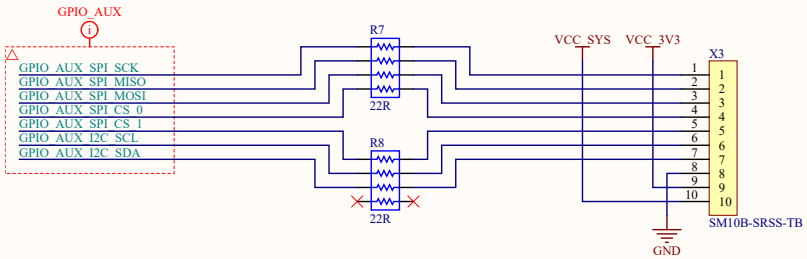
If you would like to develop your own custom HDL design on current hardware, consider to base it on a special safe "empty" project with all possible stubs, that will be provided later.



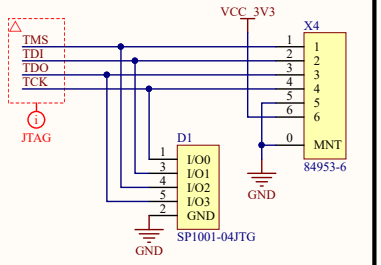
Peripheral board connector



AUX connector



JTAG



Title: M-board.Connectors			
File: 1_CONNECTORS.SchDoc		Size: A3	
Drawn by: Vaagn Oganesyan		Version: v0.2.0	
Date: 07.09.2020	Time: 16:43:14	Sheet: 2 of 6	

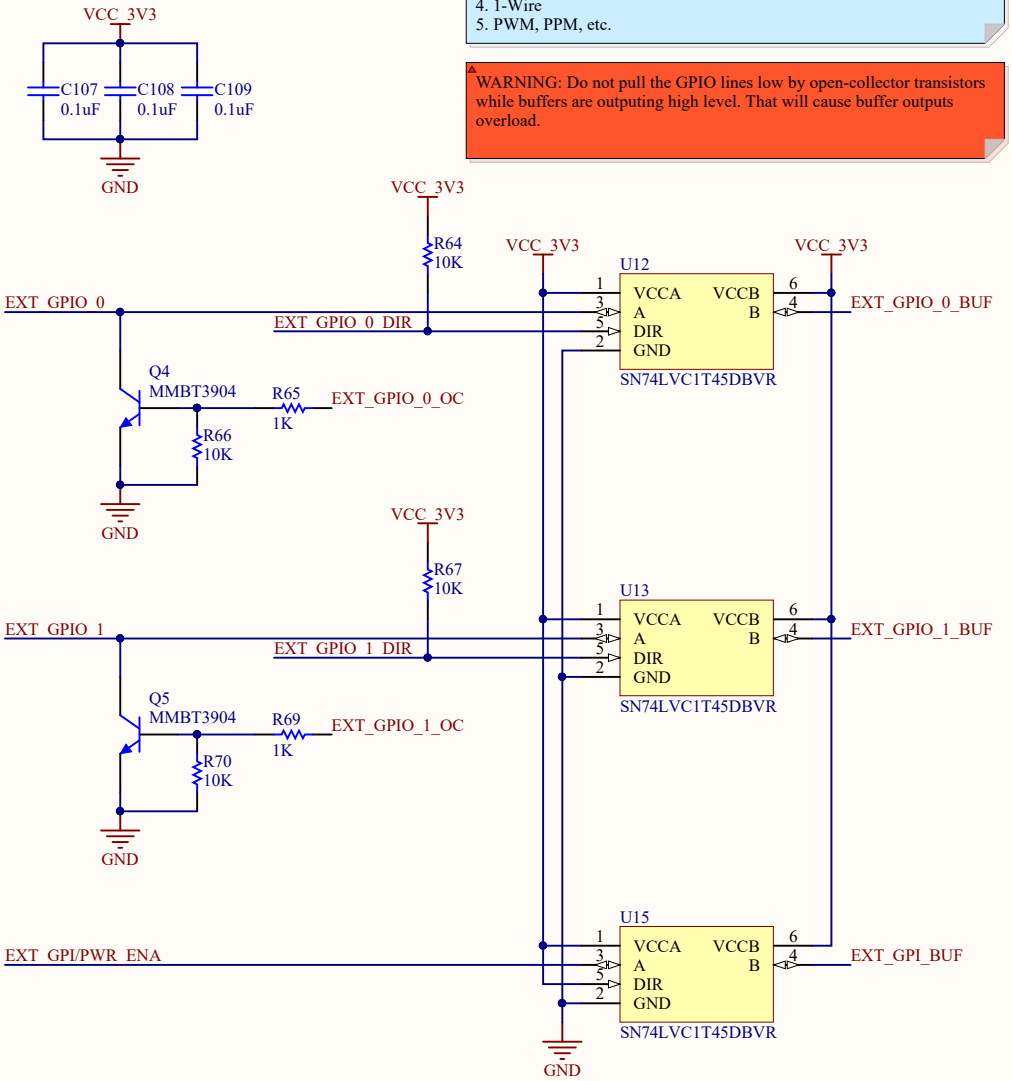
OpenIRV

GPIO_EXT buffers

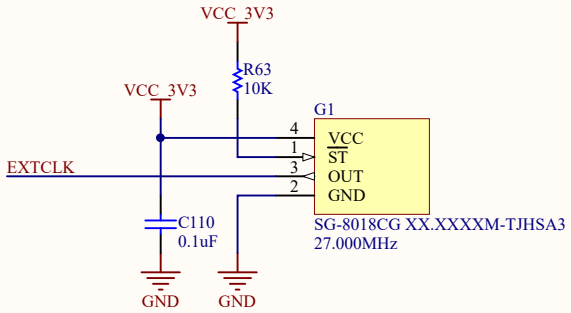
EXT_GPIO[1:0] are confugurable input/output, push-pull/open-collector.
EXT_GPI is input only.

Supports master/slave interfaces:
1. SPI (3-wire)
2. UART
3. I2C
4. 1-Wire
5. PWM, PPM, etc.

WARNING: Do not pull the GPIO lines low by open-collector transistors while buffers are outputing high level. That will cause buffer outputs overload.

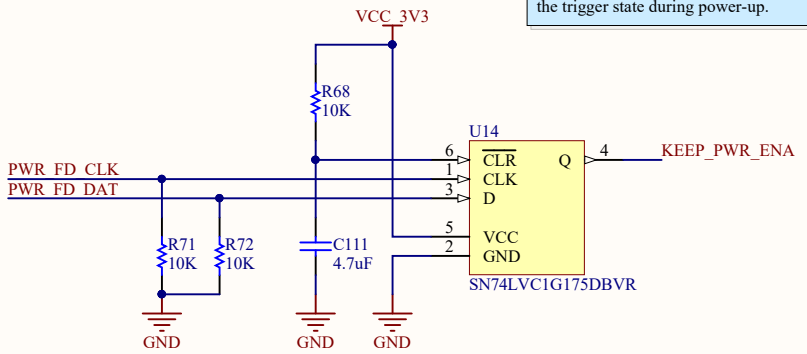


Clock generator



Power keep logic

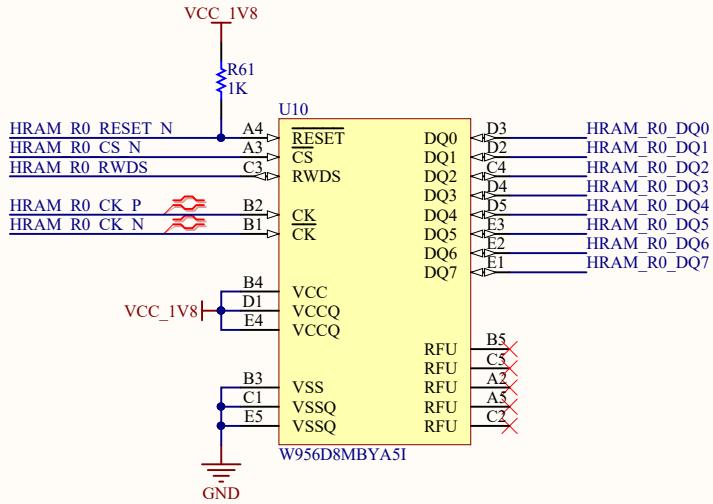
This trigger keeps main power path enabled during FPGA (re)configuration. RC delay (47ms) at the CLR pin resets the trigger state during power-up.

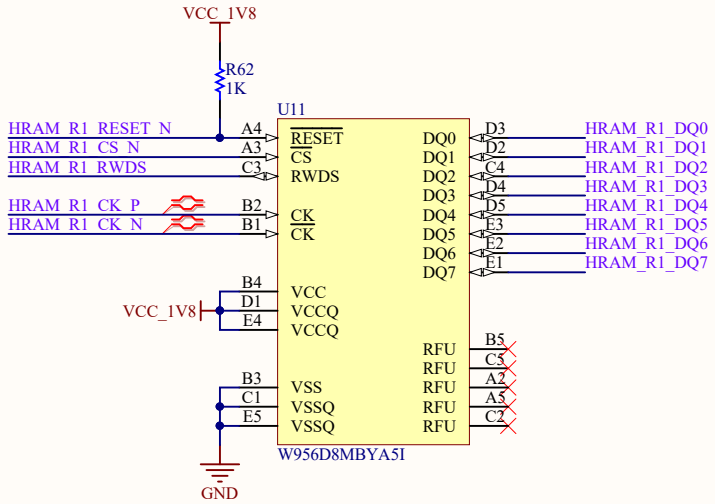


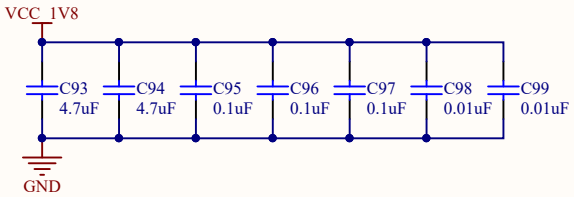
Title: M-board.Miscellaneous		
File: 2_MISC.SchDoc	Size: A4	
Drawn by: Vaagn Oganesyan	Version: v0.2.0	
Date: 07.09.2020 Time: 16:43:14	Sheet: 3 of 6	

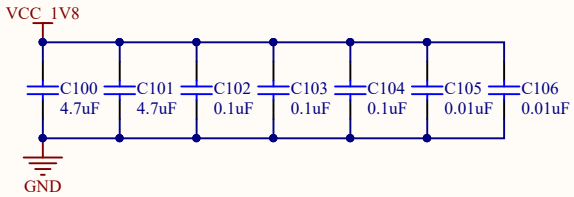
OpenIRV

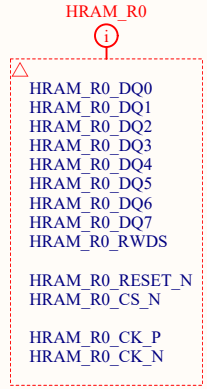
RAM

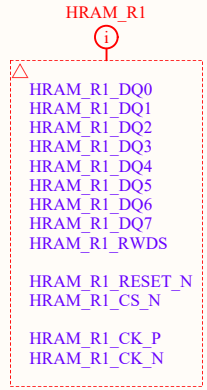












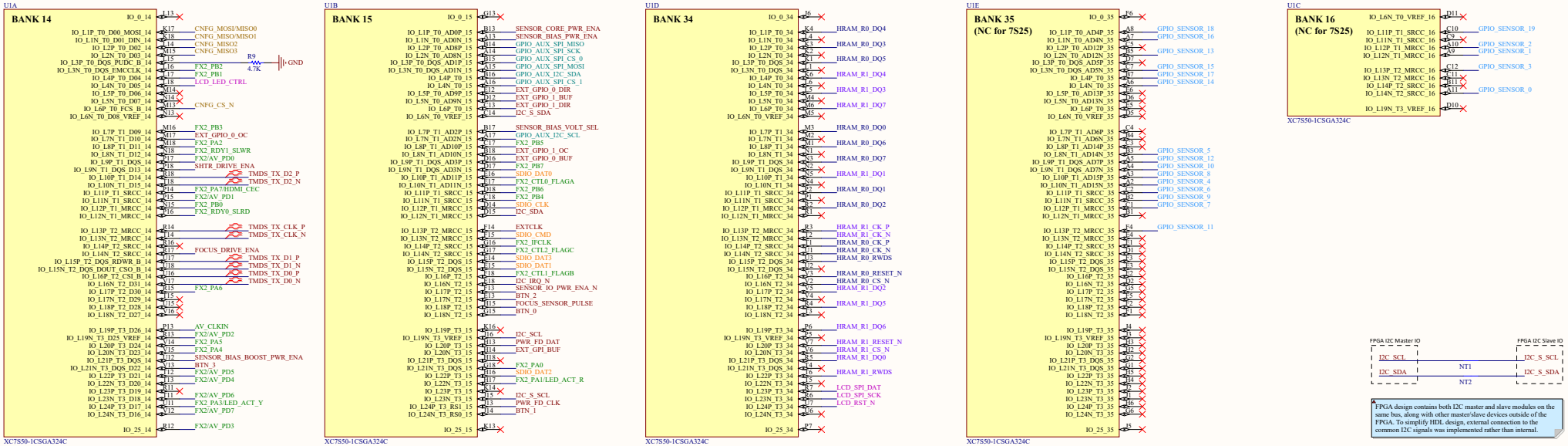
Two HyperRAM memory ICs are connected to FPGA over two independent 8-bit HyperBUS interfaces. Depending on memory controller mode, both ranks may work fully independently even with different clock frequencies or can be combined in a single memory area with a 16-bit bus width, that will increase memory throughput twice.

Pull-ups at RESET_N inputs allow to keep HyperRAM memory in non-reseted state, while FPGA is being (re)configurated. This feature allows to save memory content (i.e. internal MCU context), while switching from one FPGA configuration to another. Switching between different configurations may be useful if you can actually interleave your hardware in time, when all modules cannot be fitted in a single bitstream and you do not need to keep them working simultaneously.

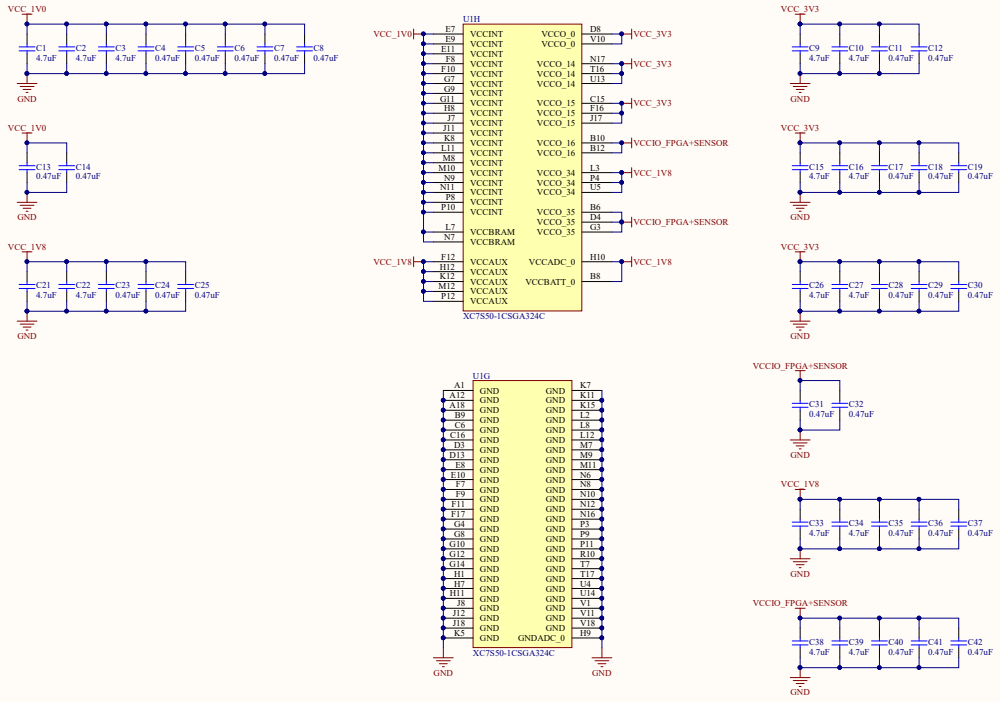
Title: M-board.RAM		
File: 3_RAM.SchDoc	Size: A4	
Drawn by: Vaagn Oganesyan	Version: v0.2.0	
Date: 07.09.2020 Time: 16:43:14	Sheet: 4 of 6	

OpenIRV

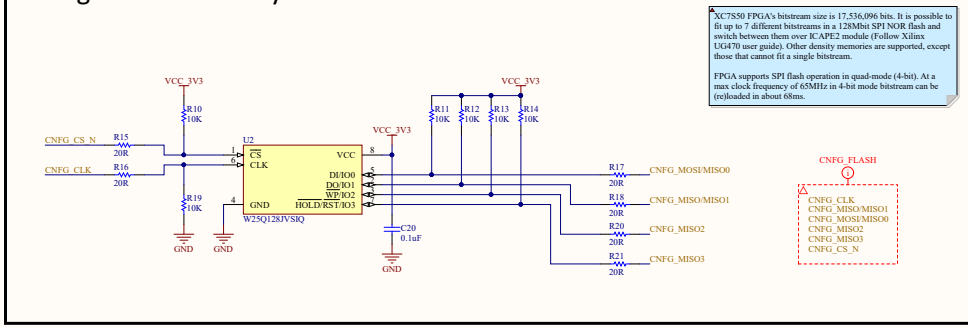
FPGA IO banks



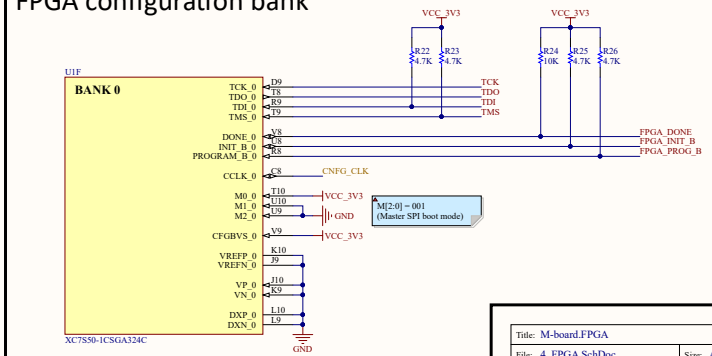
FPGA power



Configuration memory



FPGA configuration bank



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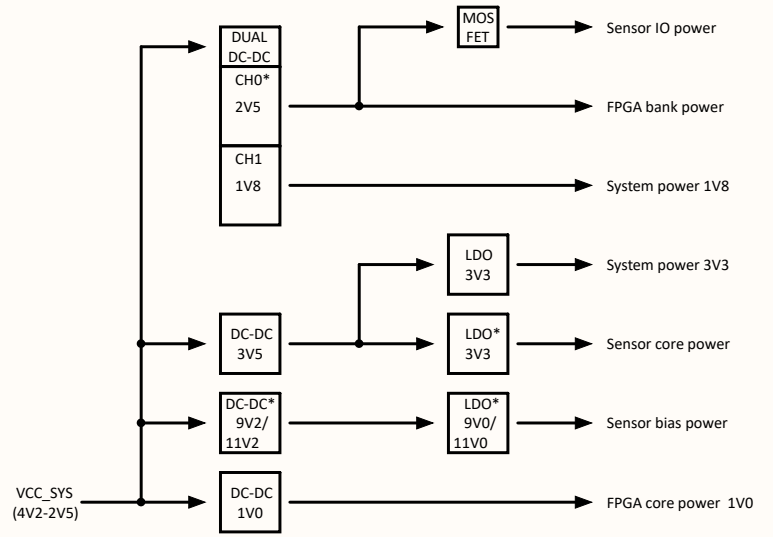
File: 4_FPGA.SchDoc		Size: A2	
Drawn by: Vaagn Oganesyan		Version: v0.2.0	
Date: 07.09.2020	Time: 16:43:14	Sheet: 5 of 6	

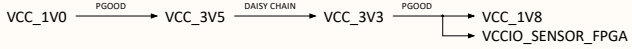
OpenIRV

Power delivery scheme



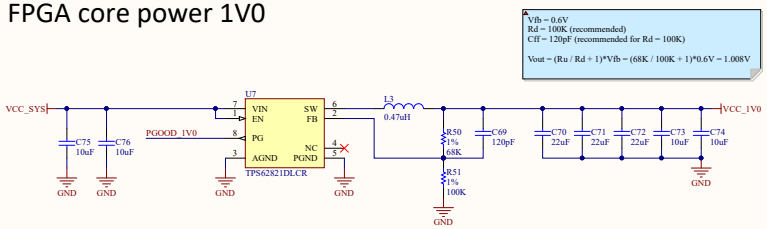
* only this regulator voltages can be modified to meet sensor's special power requirements if necessary

Power sequencing

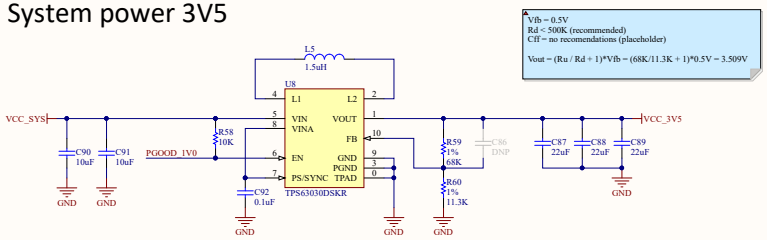


NOTE: All other power rails can be each enabled/disabled individually

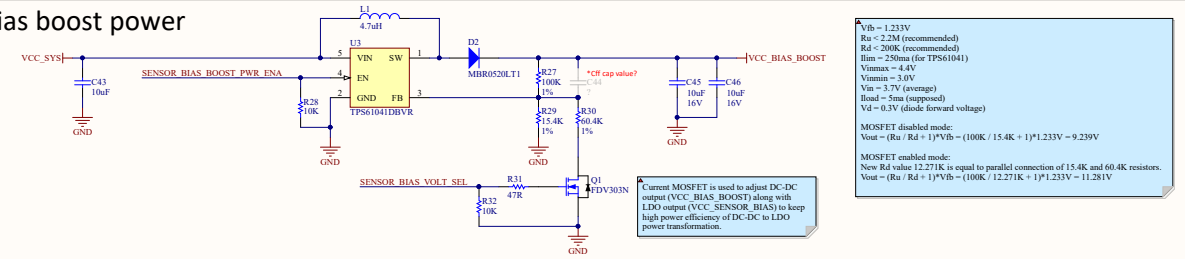
FPGA core power 1V0



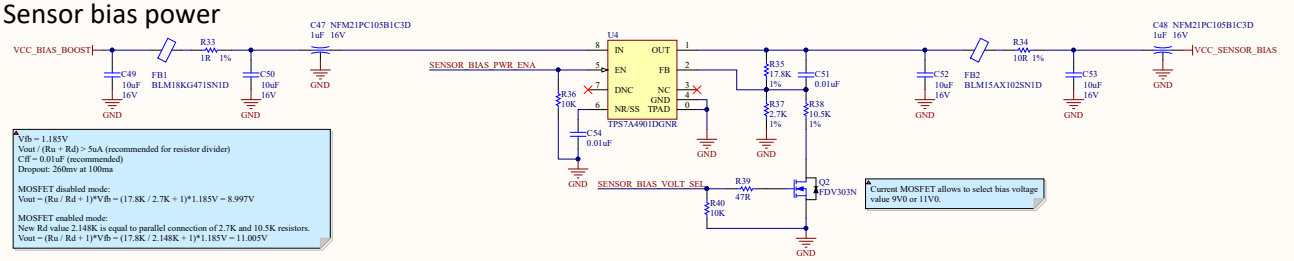
System power 3V5



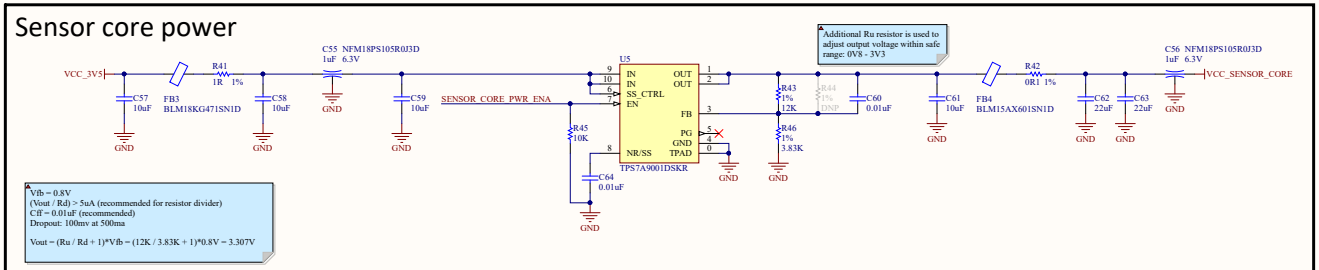
Sensor bias boost power



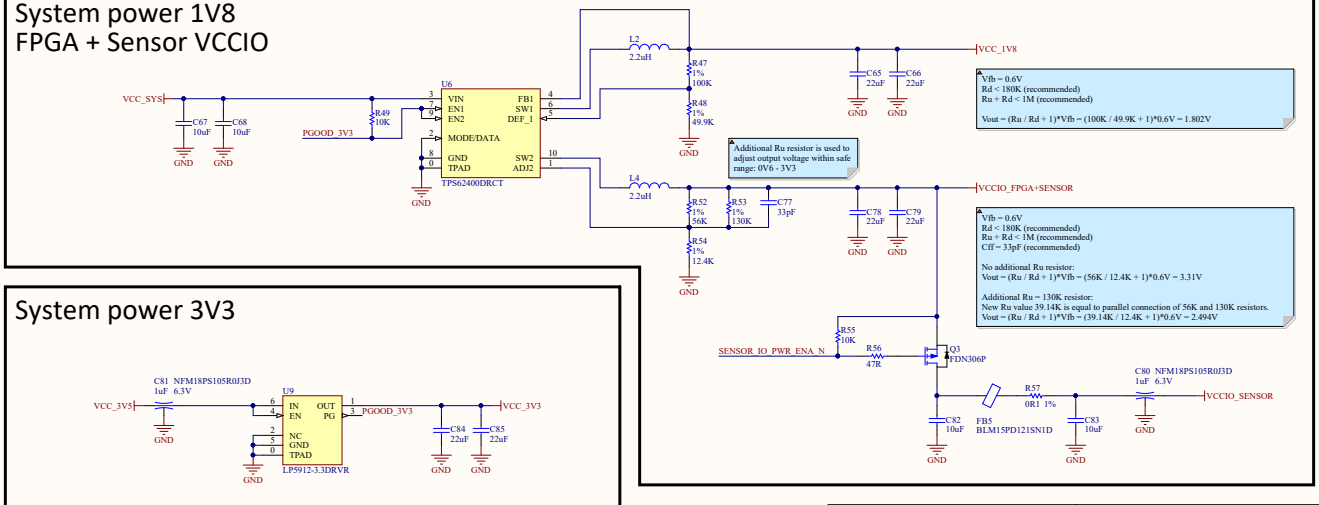
Sensor bias power



Sensor core power



System power 1V8
FPGA + Sensor VCCIO



System power 3V3

Title: M-board.Power	
File: 5_POWER.SchDoc	Size: A2
Drawn by: Vaagn Oganesyan	Version: v0.2.0
Date: 07.09.2020 Time: 16:43:15	Sheet: 6 of 6

OpenIRV