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Title: M-board.Header		
File: 0_HEADER.SchDoc	Size: A4	
Drawn by: Vaagn Oganessian	Version: v1.0.0	
Date: 09.12.2020	Time: 16:15:40	Sheet: 1 of 7

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Sensor connector

X1 connector reflects ISC0901B0 sensor pinout. ISC0901B0 uses 6 digital lines for control and 3 different power rails. Most of other connector pins are connected to ground.

To have an ability to support more different sensors, some backward compatible changes to original ISC0901B0 connector pinout were made:

1. NC pins are connected to VCC_SYS to provide additional power source.
2. All power rails, except VCC_SYS, are designed to be adjustable to meet individual sensor power requirements.
3. Ground pins 5, 6, 10, 12, 14, 15, 19, 25, 26, 28, 30, 34, 35, 36 were transformed into IO lines and connected to FPGA.

R6 resistor pull-up may be useful to detect if ISC0901B0 board is attached.

WARNING!

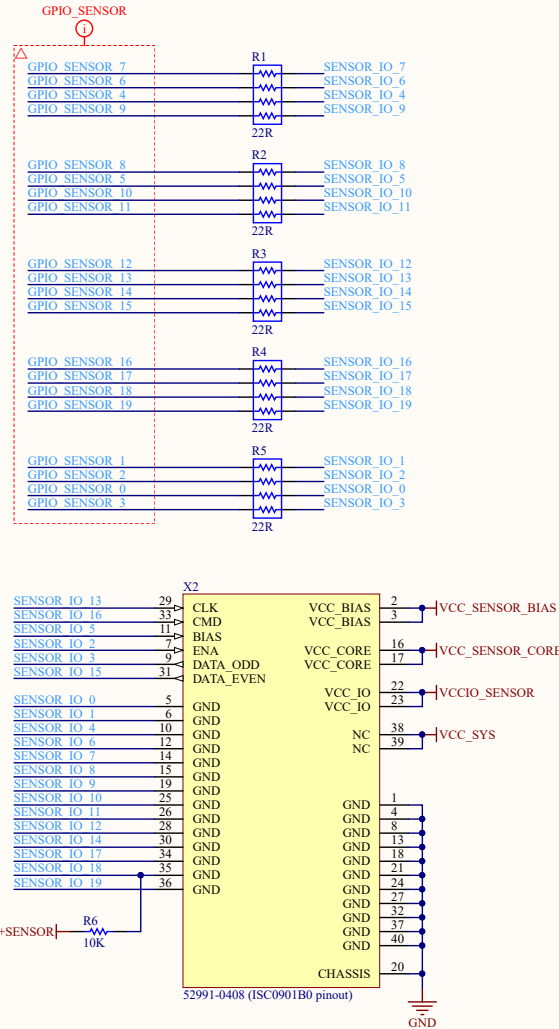
This warning is mostly for those users, who would like to use this hardware in their own way. You MUST BE EXTREMELY CAREFULL while matching different devices/adapters attached to X1 connector with different FPGA bitstreams and different power rail voltages at X1.

Bad scenario examples:

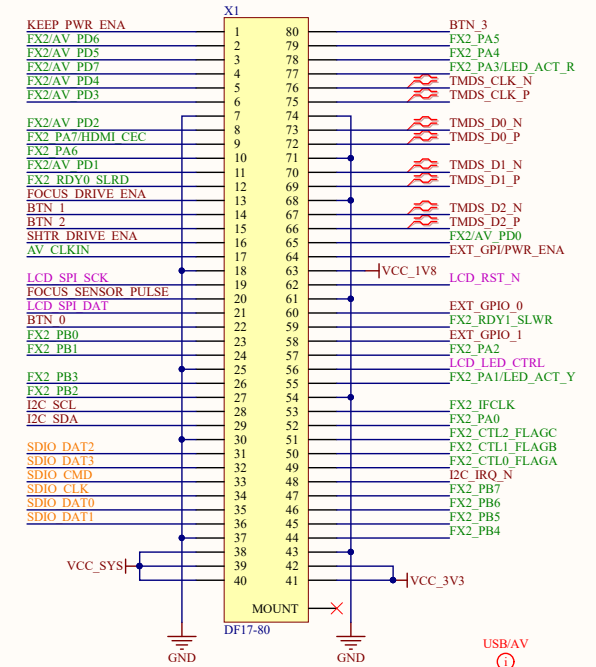
1. If you attach some custom board to X1, that, for example, expects 1V2 voltage at VCC_SENSOR_CORE lines, while there is actually 3V3, that may cause a damage to your attached device.
2. If you attach some custom board to X1 that drives digital IO lines with logic "High" levels higher than VCCIO_SENSOR, that will cause a damage to FPGA.
3. Loading FPGA with your custom bitstream, that drives IO lines that are shared with ground at X1 while ISC0901B0 sensor board is attached, will cause short circuit of these lines to ground. Shorted IO current will overdrive IO buffers, bank power, cause an overheat and possibly damage FPGA.

N. Any other bad or non-thought-out idea.

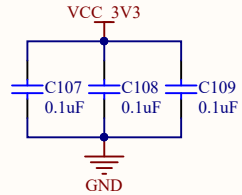
If you would like to develop your own custom HDL design on current hardware, consider to base it on a special safe "empty" project with all possible stubs, that will be provided later.



Peripheral board connector



GPIO_EXT buffers

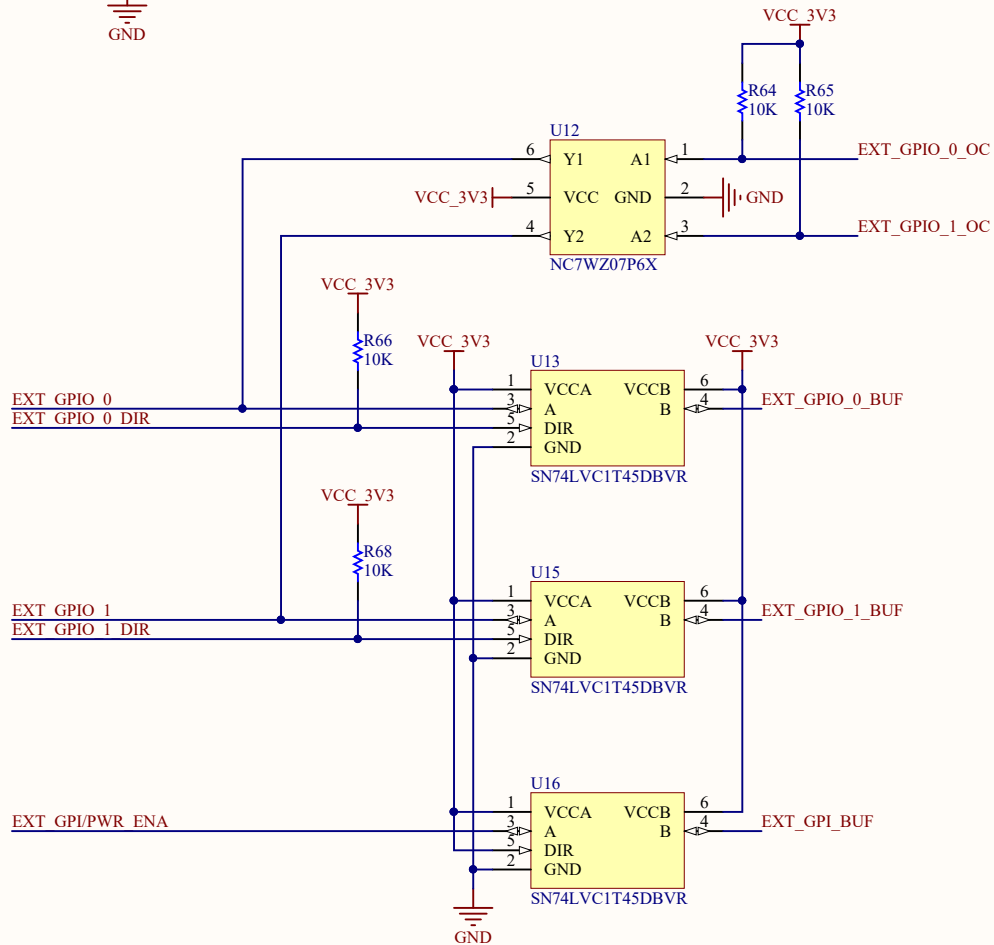


EXT_GPIO[1:0] are configurable input/output, push-pull/open-collector.
EXT_GPIO is input only.

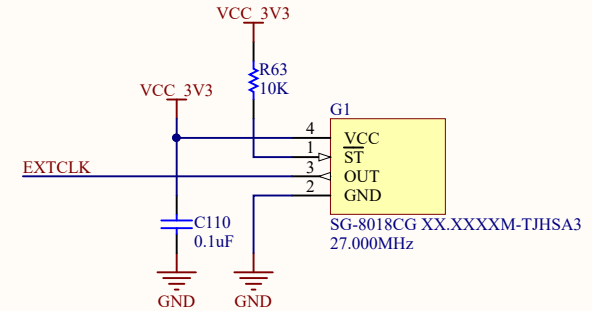
Supports master/slave interfaces:

1. SPI (3-wire)
2. UART
3. I2C
4. 1-Wire
5. PWM, PPM, etc.

WARNING: Do not pull the GPIO lines low by open-collector transistors while buffers are outputting high level. That will cause buffer outputs overload.

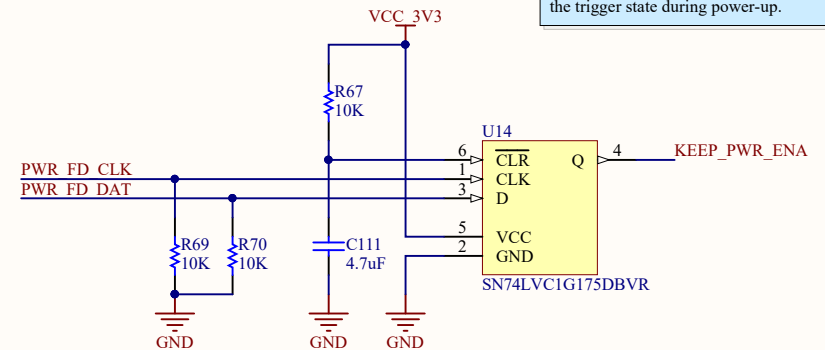


Clock generator



Power keep logic

This trigger keeps main power path enabled during FPGA (re)configuration. RC delay (47ms) at the CLR pin resets the trigger state during power-up.



Title: M-board.Miscellaneous

File: 2_MISC.SchDoc

Size: A4

Drawn by: Vaagn Oganessian

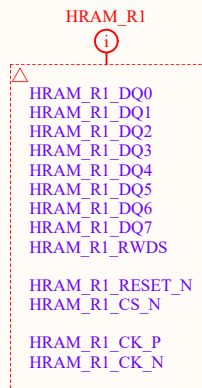
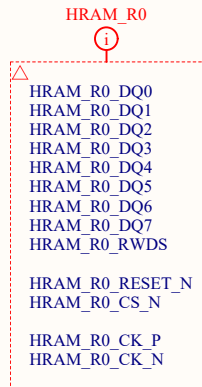
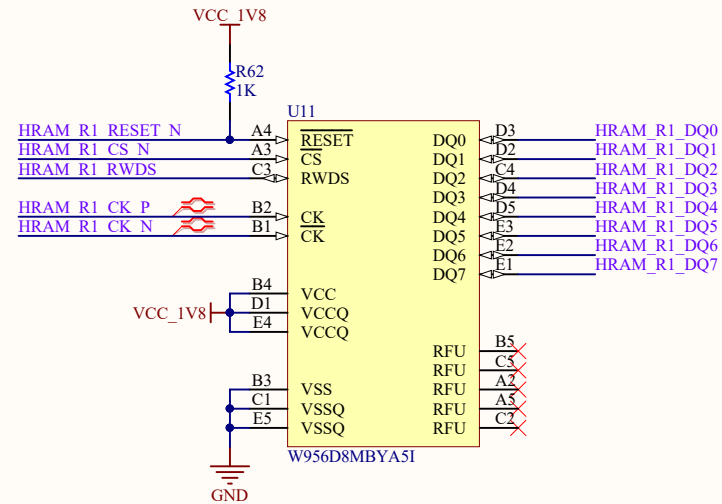
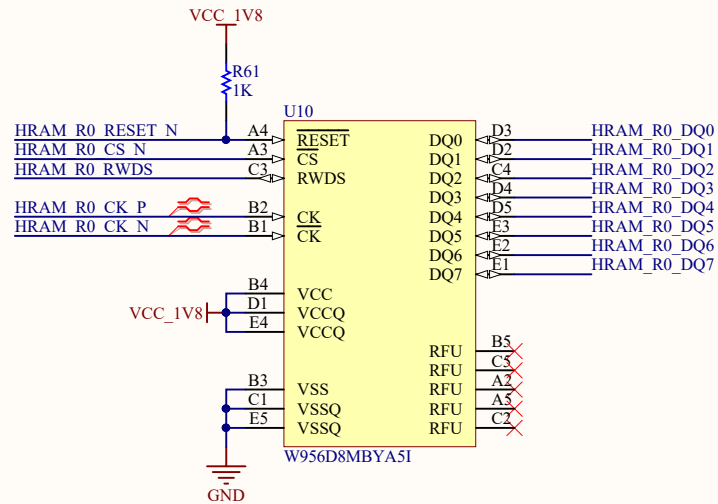
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RAM



Two HyperRAM memory ICs are connected to FPGA over two independent 8-bit HyperBUS interfaces. Depending on memory controller mode, both ranks may work fully independently even with different clock frequencies or can be combined in a single memory area with a 16-bit bus width, that will increase memory throughput twice.

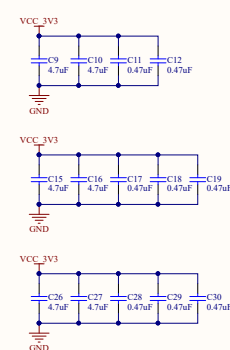
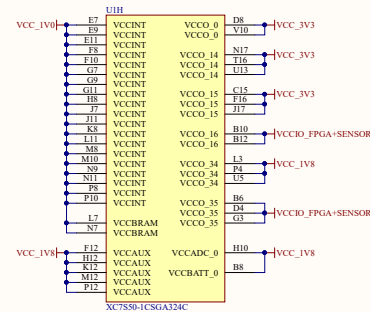
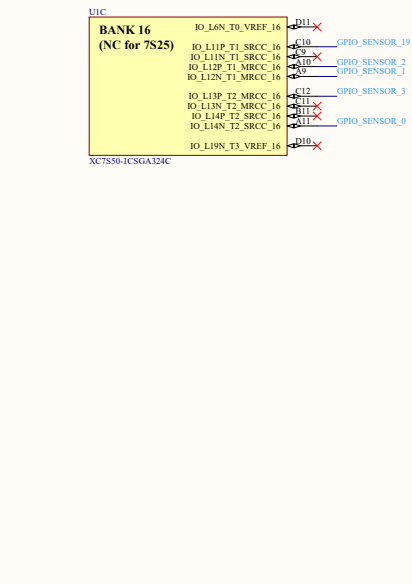
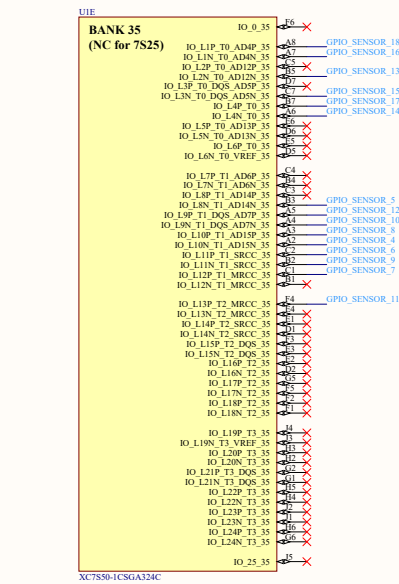
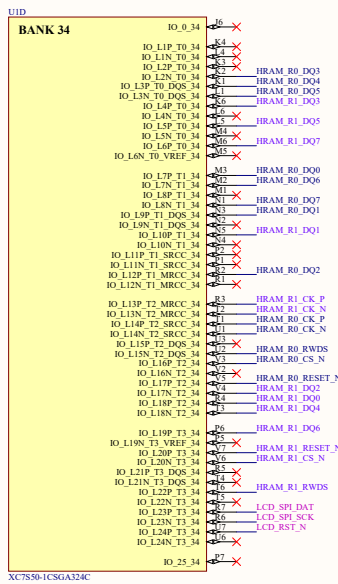
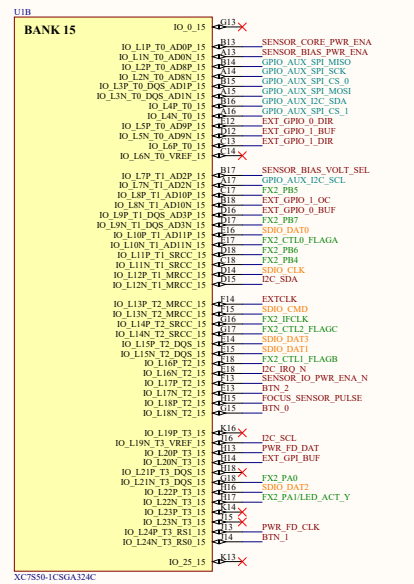
Pull-ups at RESET_N inputs allow to keep HyperRAM memory in non-reseted state, while FPGA is being (re)configured. This feature allows to save memory content (i.e. internal MCU context), while switching from one FPGA configuration to another. Switching between different configurations may be useful if you can actually interleave your hardware in time, when all modules cannot be fitted in a single bitstream and you do not need to keep them working simultaneously.

Title: M-board.RAM	
File: 3_RAM.SchDoc	Size: A4
Drawn by: Vaagn Oganessian	Version: v1.0.0
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U1A		IO_0_14	
BANK 14			
IO L1P TO D00_M0SI_L	117	CNFG_M0SI/M0SIO	
IO L1N TO D01_DN_L	118	CNFG_M0SI/M0SIO	
IO L2P TO D02_L	119	CNFG_M0SI/M0SIO	
IO L2N TO D03_D	120	CNFG_M0SI/M0SIO	
IO L3P TO D05_PUDC_B	121	CNFG_M0SI/M0SIO	
IO L3N TO D06_EMCC1_C	122		
IO L4P TO D04_L	123	FX2_P02	R9
IO L4N TO D05_L	124	FX2_P01	4.7K
IO L4P TO D06_C	125	FX2_AV_CTRL	
IO L5N TO D07_L	126		
IO L6P TO PCS_B	127	CNFG_CS_N	
IO L6N TO D08_VREF_L	128		
IO L7P T1 D09_L	129	FX2_P03	
IO L7N T1 D10_L	130	FX2_P02	
IO L8P T1 D11_L	131	FX2_OFIO_0_OC	
IO L8N T1 D12_L	132	FX2_DRV1_SLWR	
IO L9P T1 D05_L	133	FX2AV_P00	
IO L9N T1 D06_D13	134	SHTR_DRIVE_INA	
IO L10P T1 D14_L	135		TMD5_D1_P
IO L10N T1 D15_L	136		TMD5_D1_P
IO L11P T1 SRCC_C	137	FX2_P04/HDMI_CEL	
IO L11N T1 SRCC_L	138	FX2AV_P01	
IO L12P T1 MRCC_C	139	FX2_P00	
IO L12N T1 MRCC_L	140	FX2_RDV0_SLRD	
IO L13P T2 MRCC_C	141		TMD5_CLK_P
IO L13N T2 MRCC_L	142		TMD5_CLK_N
IO L14P T2 SRCC_C	143		
IO L14N T2 SRCC_L	144	FOCUS_DRIVE_INA	
IO L15P T2 D08_RDWR_B	145		TMD5_D1_P
IO L15N T2 D09_D07_C00_B	146		TMD5_D1_P
IO L16P T2 CSI_B	147		TMD5_D0_P
IO L16N T2 D01_L	148		TMD5_D0_P
IO L17P T2 D30_L	149	FX2_P06	
IO L17N T2 D29_L	150		
IO L18P T2 D28_L	151		
IO L18N T2 D27_L	152		
IO L19P T3 D26_L	153	AV_CLKIN	
IO L19N T3 D25_VREF_L	154	FX2AV_P02	
IO L20P T3 D24_L	155	FX2_P05	
IO L20N T3 D23_L	156	FX2_P06	
IO L21P T3 D08_L	157	SUN80R_H0ST_BOOST_FIRNA	
IO L21N T3 D06_D12	158	BTN_3	
IO L22P T3 D21_L	159	FX2_P05	
IO L22N T3 D20_L	160	FX2AV_P04	
IO L23P T3 D19_L	161		
IO L23N T3 D18_L	162	FX2AV_P06	
IO L24P T3 D17_L	163	FX2_P07/ACTR	
IO L24N T3 D16_L	164	FX2AV_P07	
IO 25_14	165	FX2AV_P03	

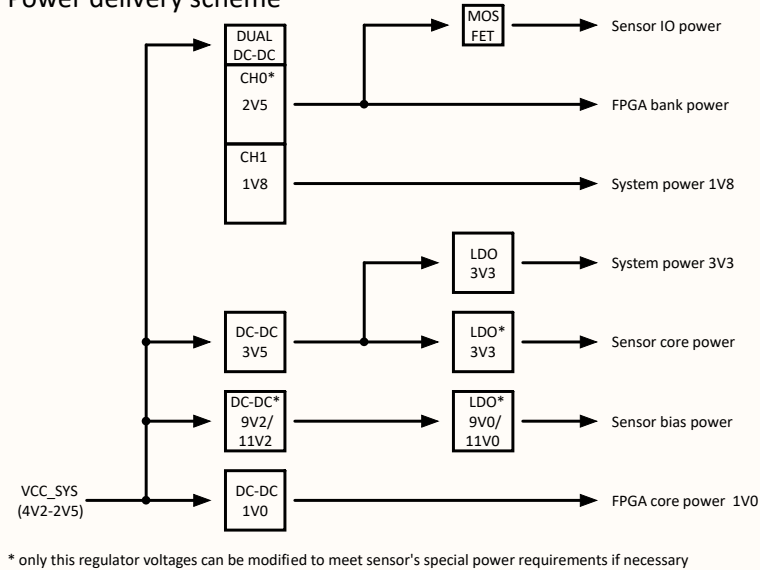
XC7S50-ICSGA324C

[illegible][illegible]

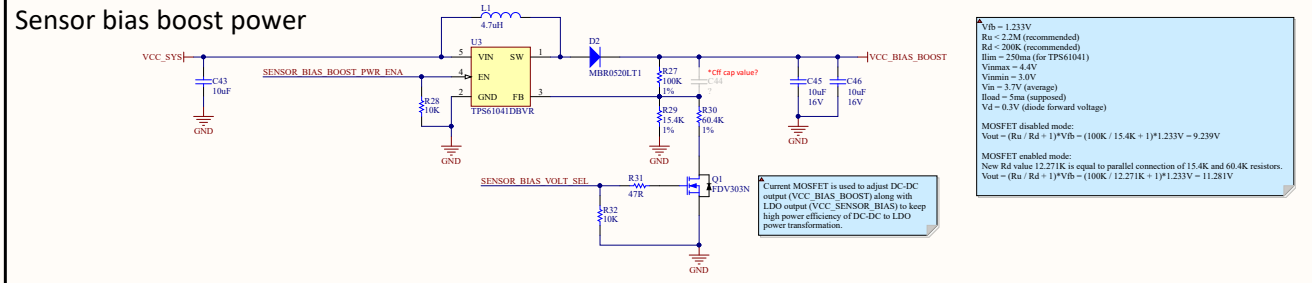
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File: 4_FPGA.SchDoc	Size: A2
Drawn by: Vaagn Oganesyan	Version: v1.0.0
Date: 09.12.2020 Time: 16:15:41	Sheet: 5 of 7

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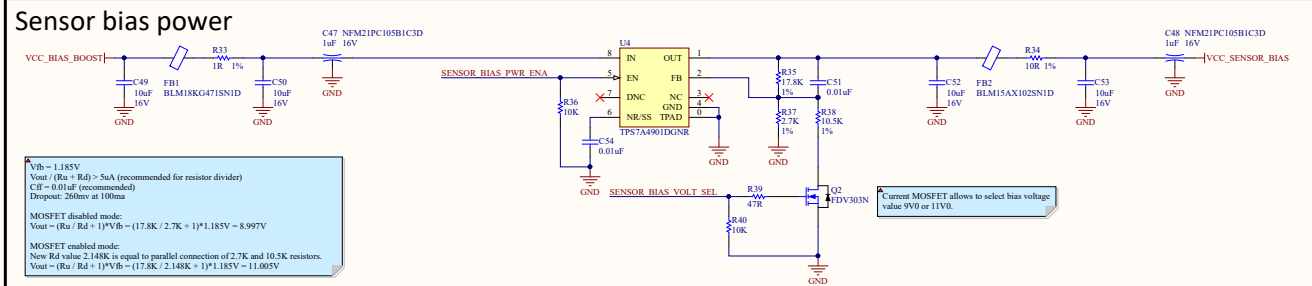
Power delivery scheme



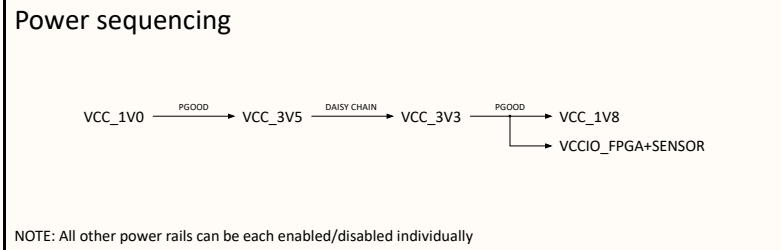
Sensor bias boost power



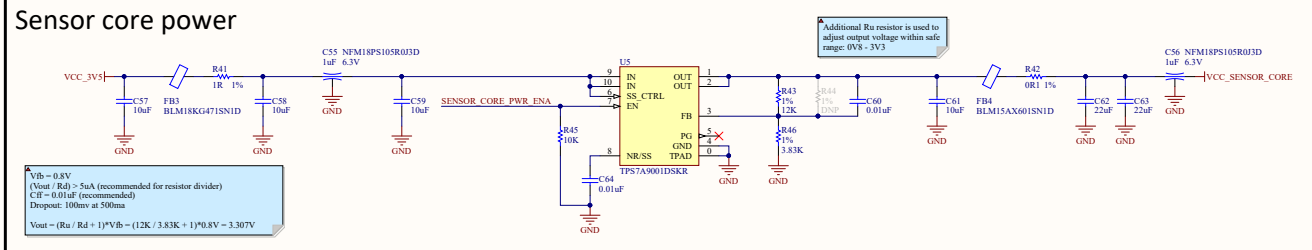
Sensor bias power



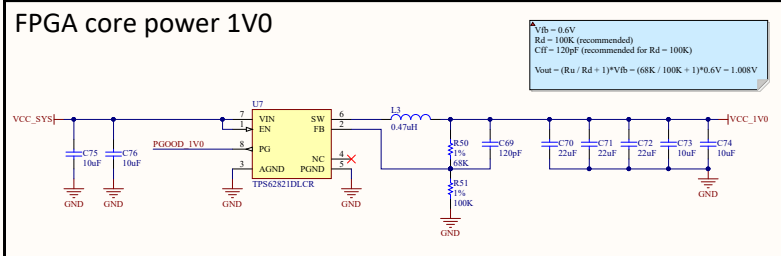
Power sequencing



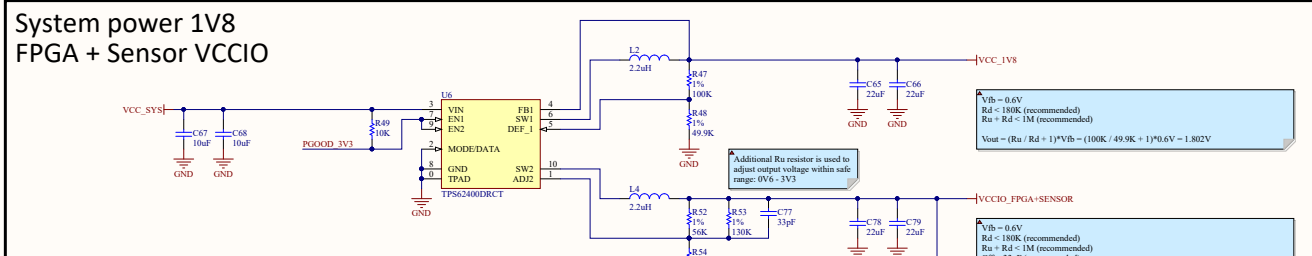
Sensor core power



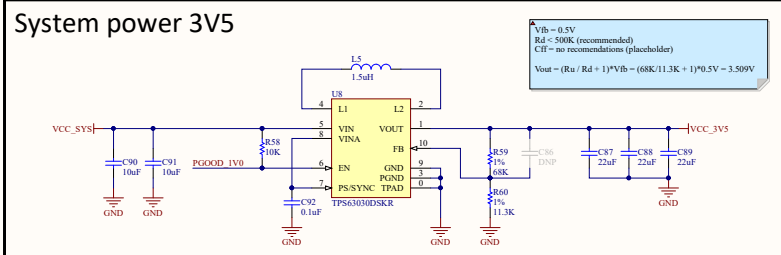
FPGA core power 1V0



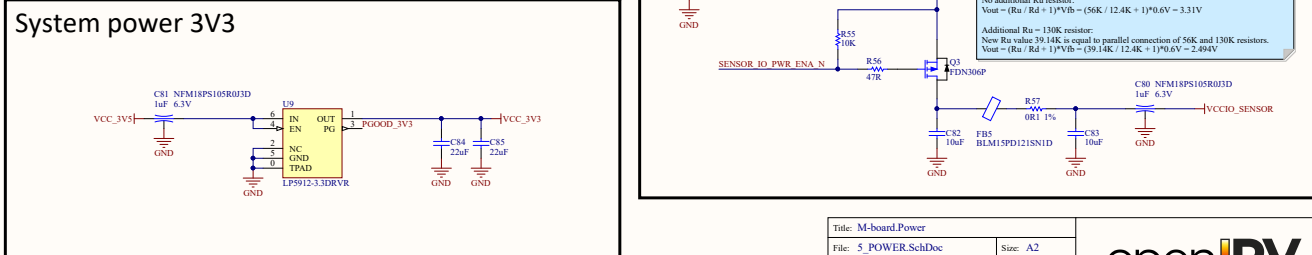
System power 1V8 FPGA + Sensor VCCIO



System power 3V5



System power 3V3



v1.0.0
- initial release

Title: M-board.ChangeLog		
File: 6_CHANGELOG.SchDoc	Size: A4	
Drawn by: Vaagn Oganessian	Version: v1.0.0	
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