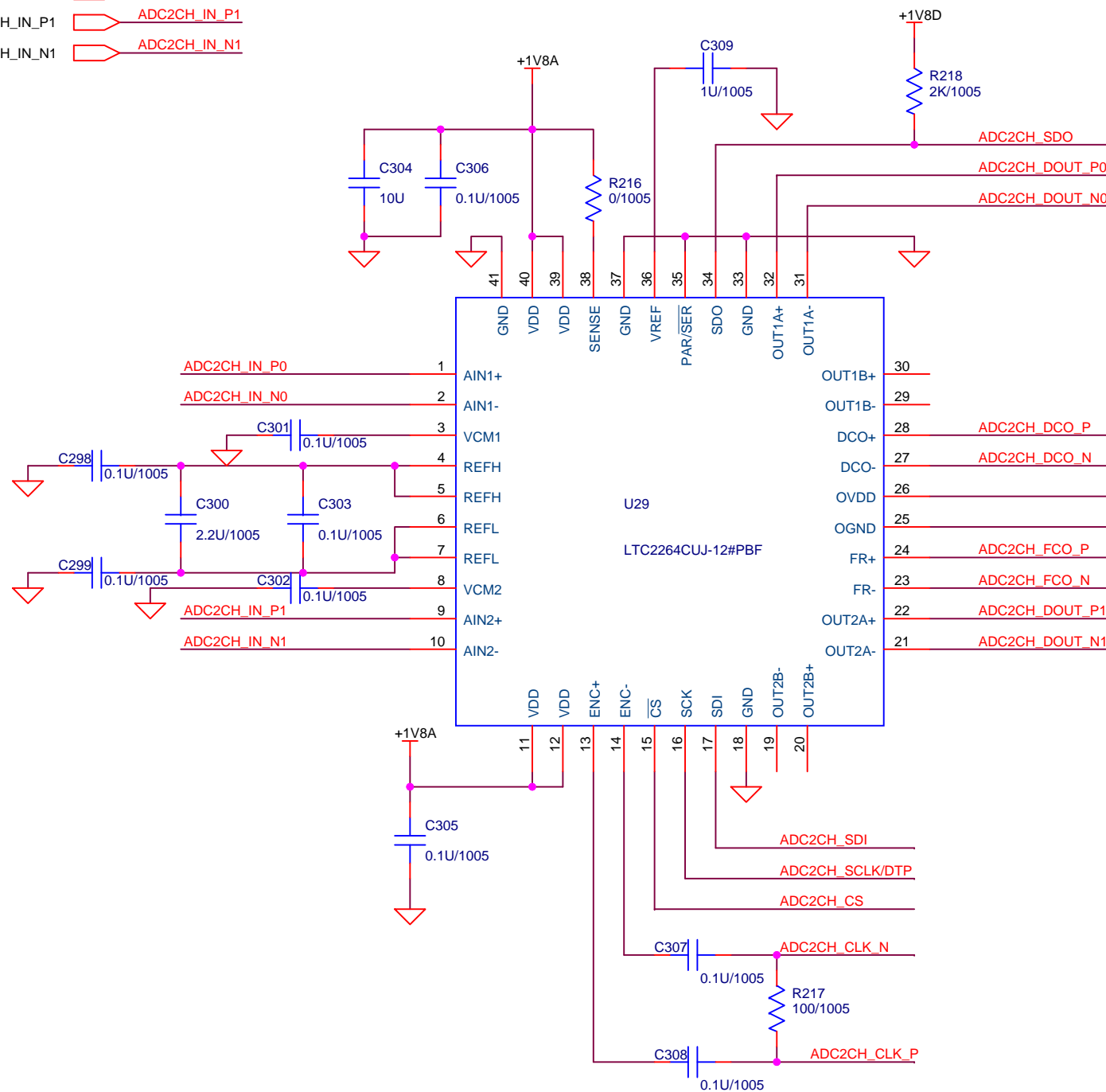


ADC2CH_IN_P0 ADC2CH_IN_P0
 ADC2CH_IN_N0 ADC2CH_IN_N0
 ADC2CH_IN_P1 ADC2CH_IN_P1
 ADC2CH_IN_N1 ADC2CH_IN_N1

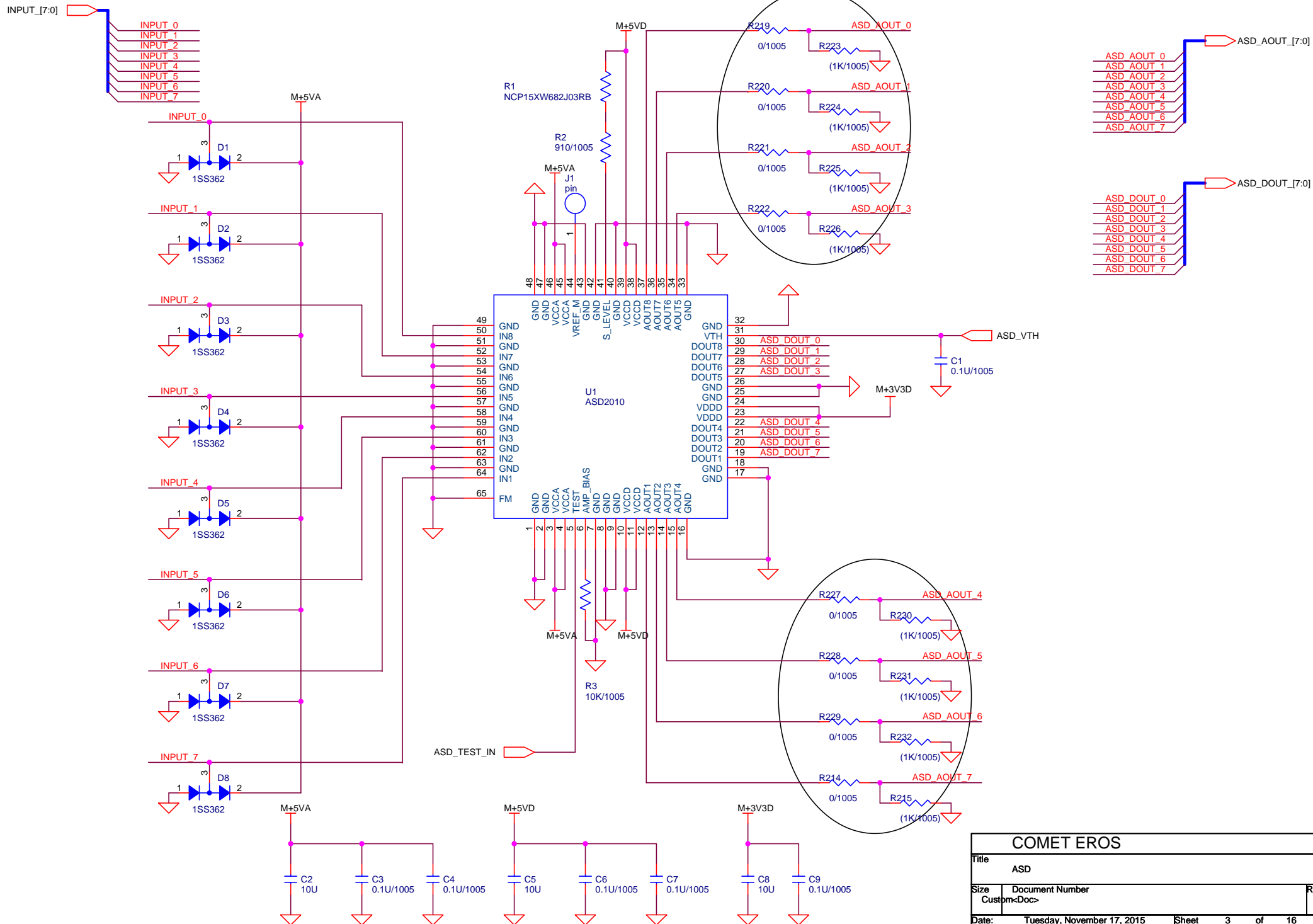
ADC2CH_DOUT_P0 ADC2CH_DOUT_P[1:0]
 ADC2CH_DOUT_P1
 ADC2CH_DOUT_N0 ADC2CH_DOUT_N[1:0]
 ADC2CH_DOUT_N1

ADC2CH_SDO ADC2CH_SDO
 ADC2CH_SDI ADC2CH_SDI
 ADC2CH_SCLK/DTP ADC2CH_SCLK/DTP
 ADC2CH_CS ADC2CH_CS
 ADC2CH_CLK_P ADC2CH_CLK_P
 ADC2CH_CLK_N ADC2CH_CLK_N
 ADC2CH_DCO_P ADC2CH_DCO_P
 ADC2CH_DCO_N ADC2CH_DCO_N
 ADC2CH_FCO_P ADC2CH_FCO_P
 ADC2CH_FCO_N ADC2CH_FCO_N

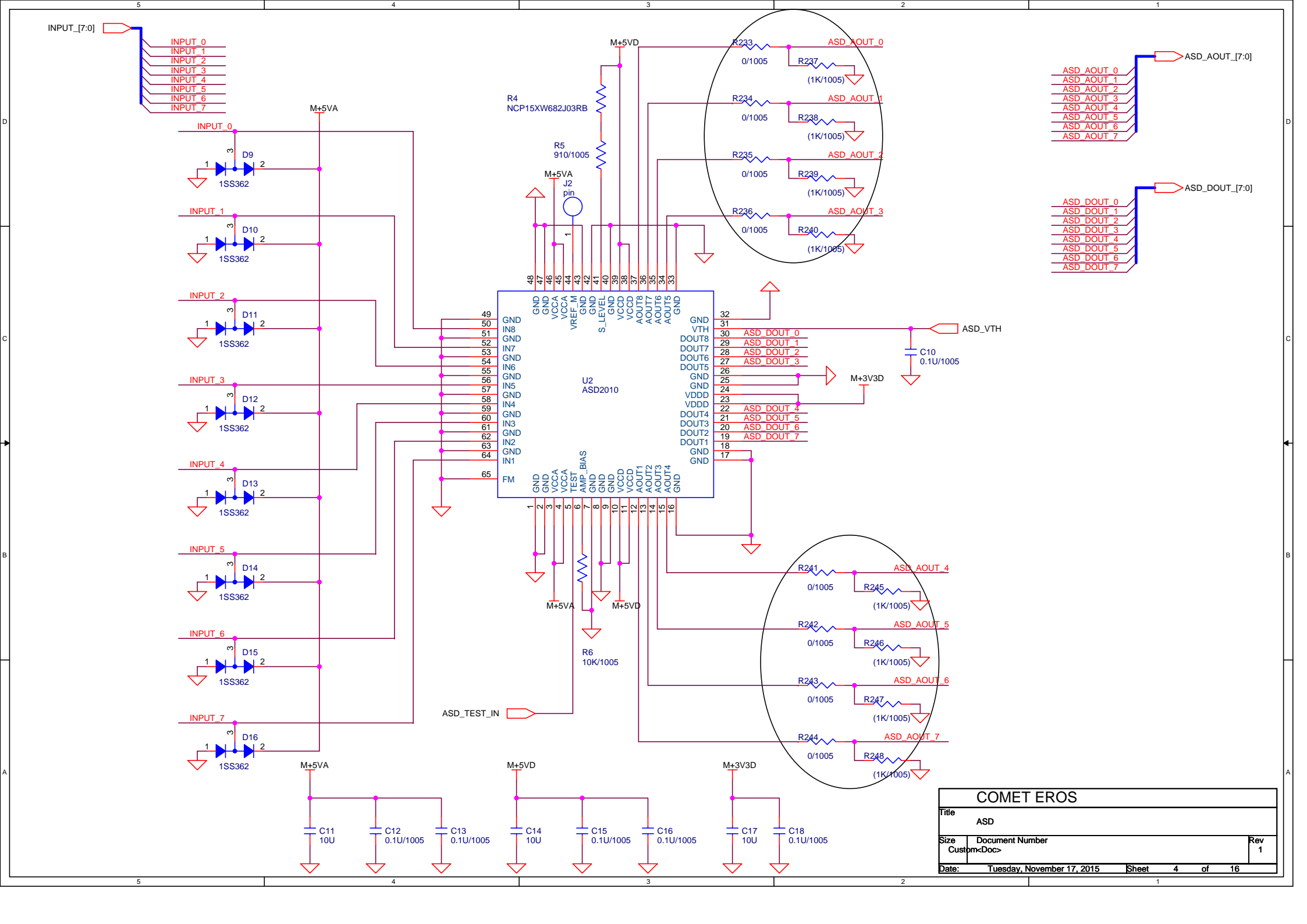


25番ピン周辺に複数のビアを使用して
GNDプレーンに繋ぐ

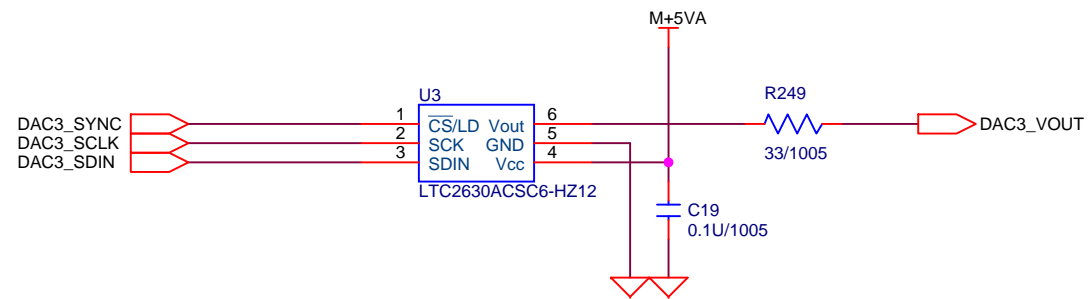
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Title ADC 2CH		
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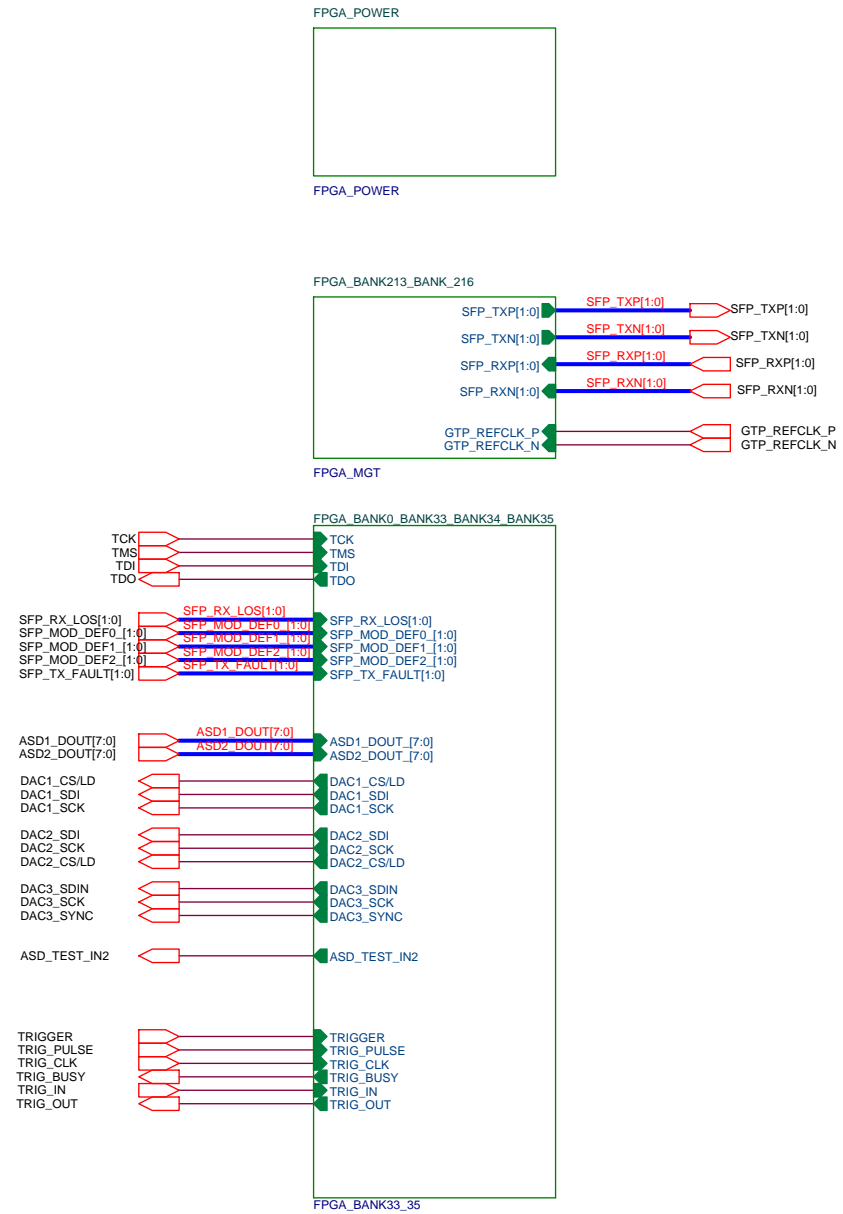
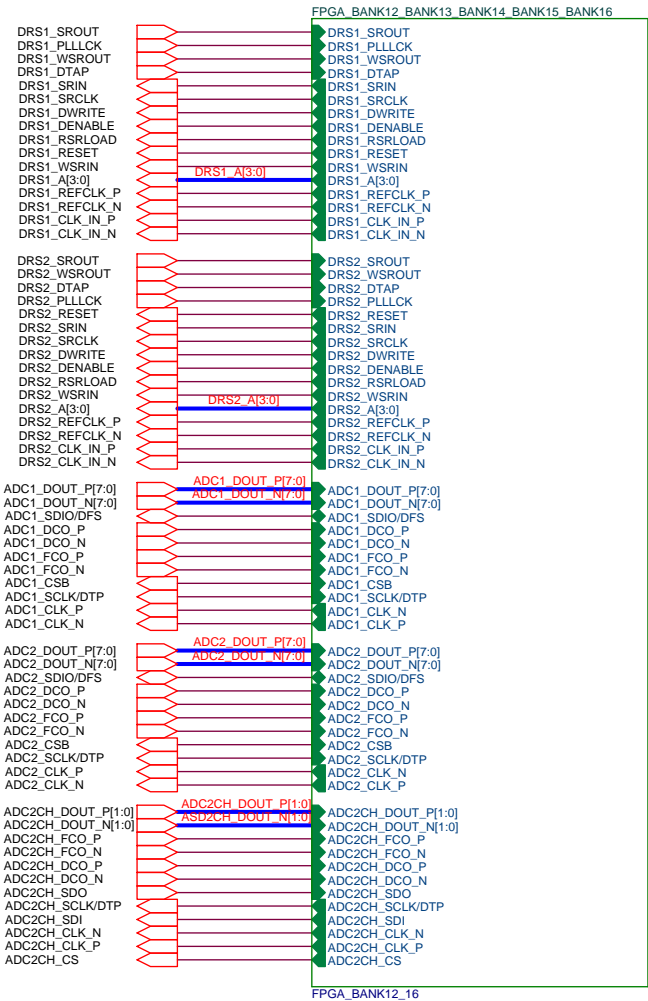
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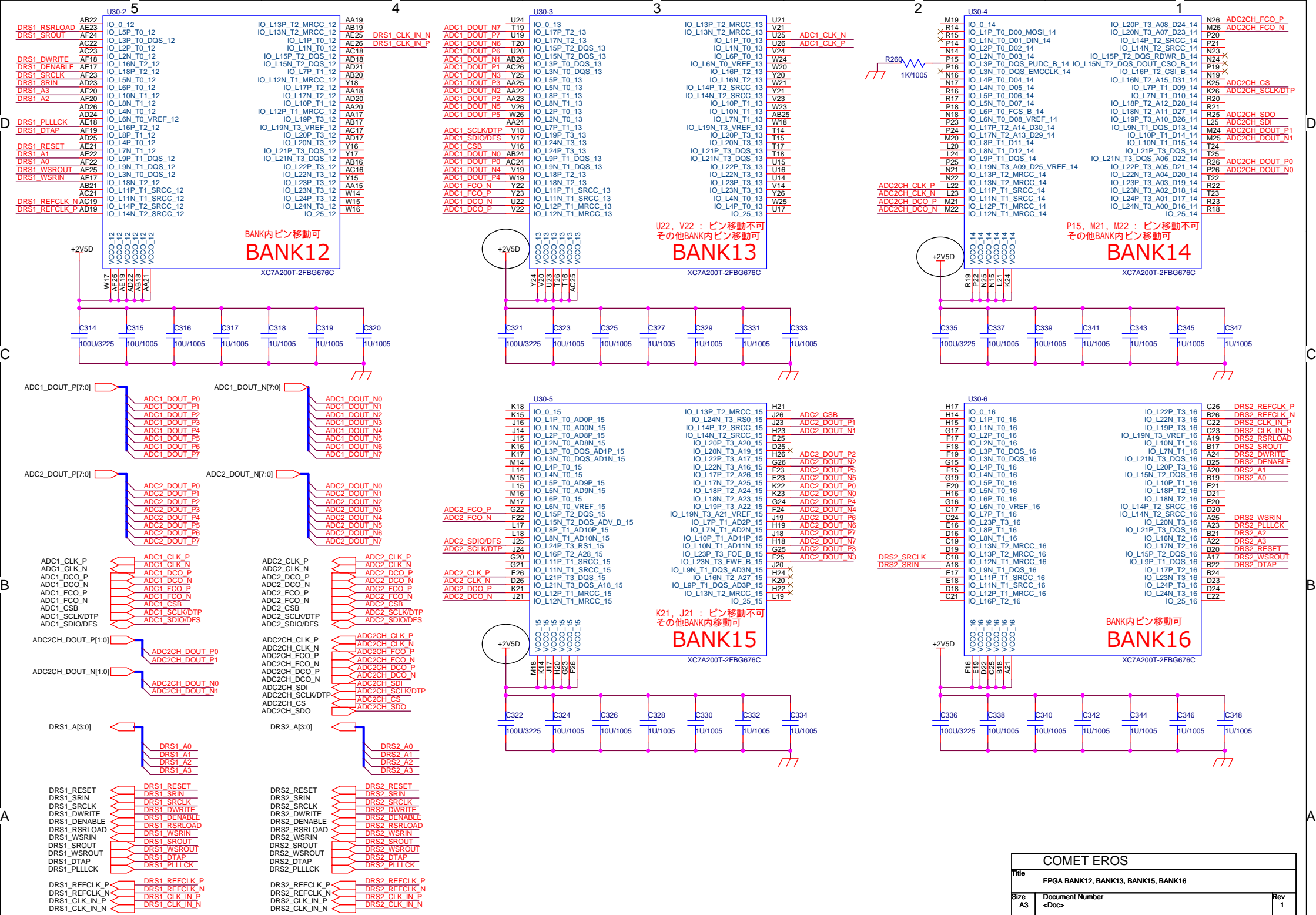


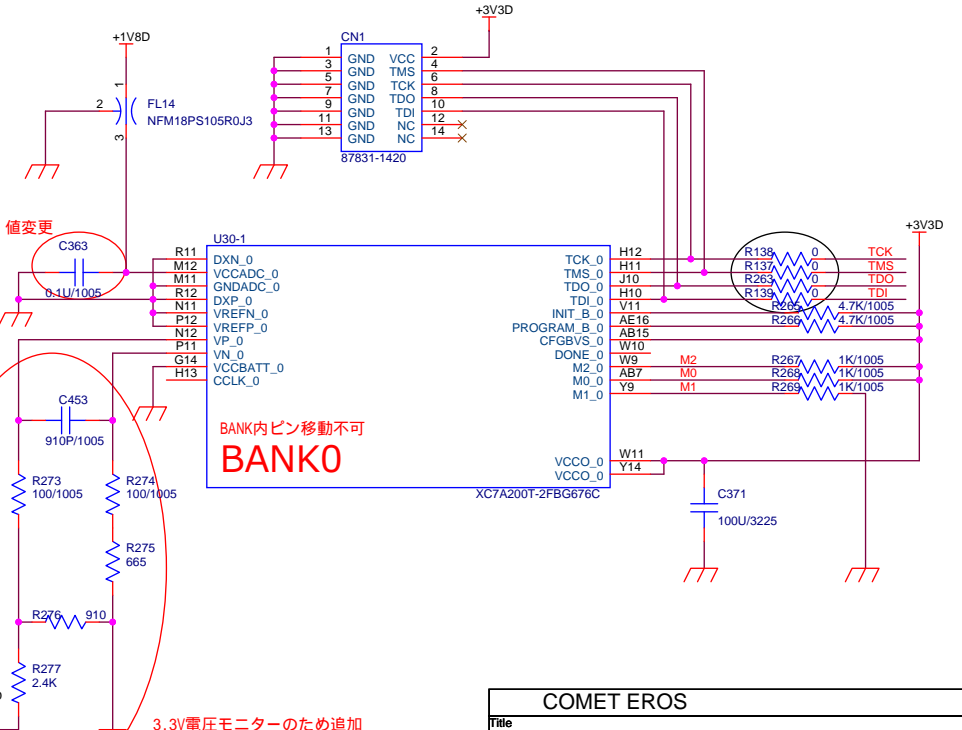
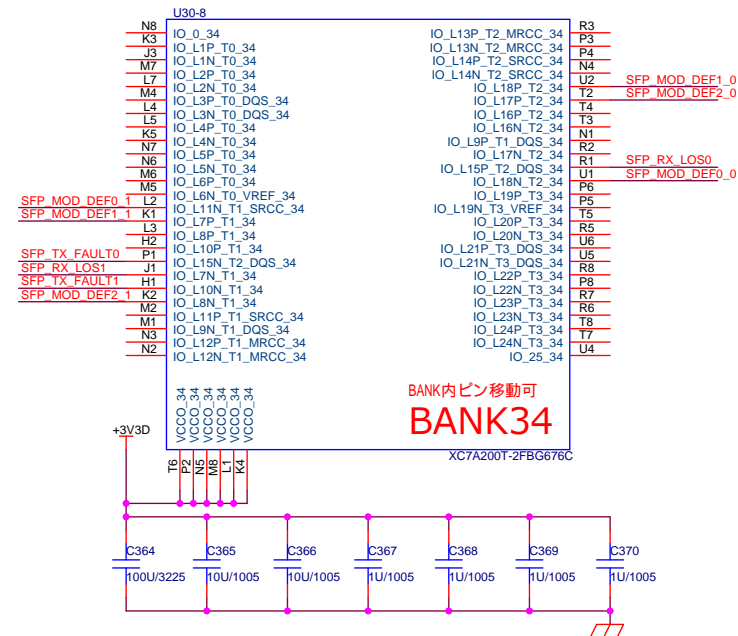
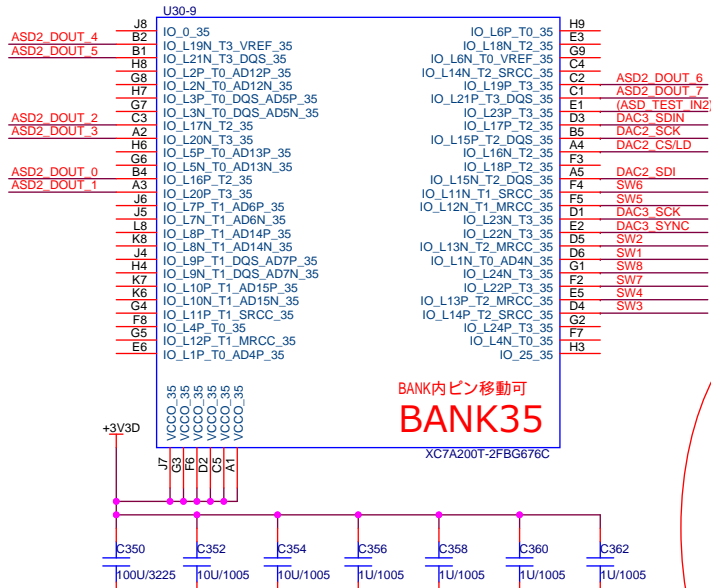
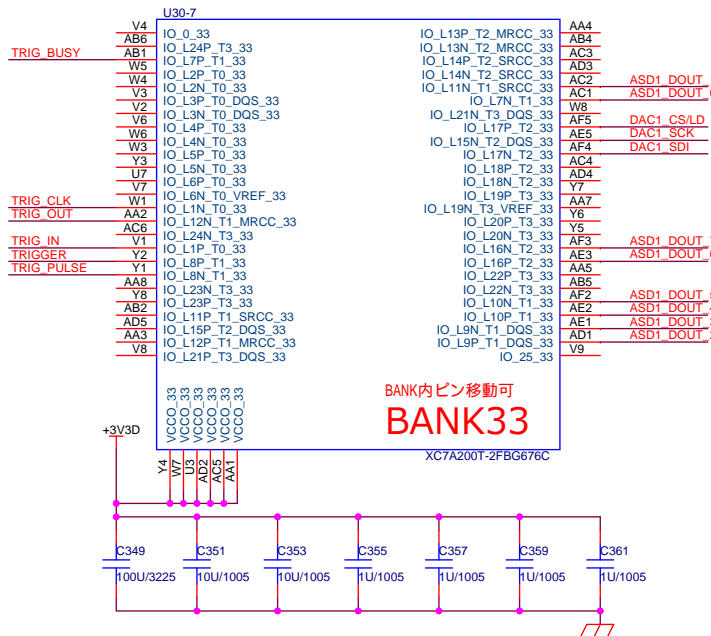
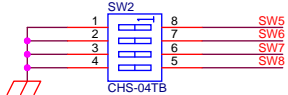
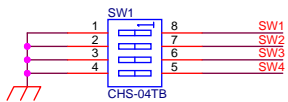
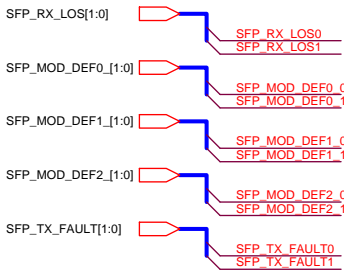
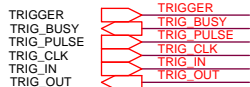
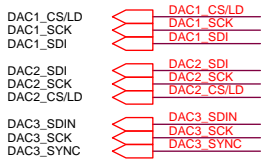
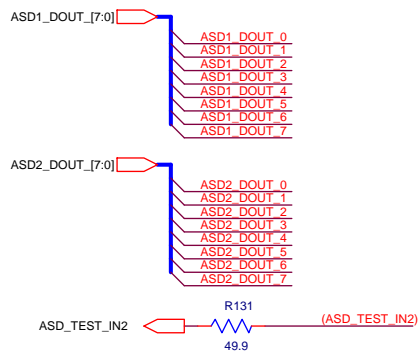
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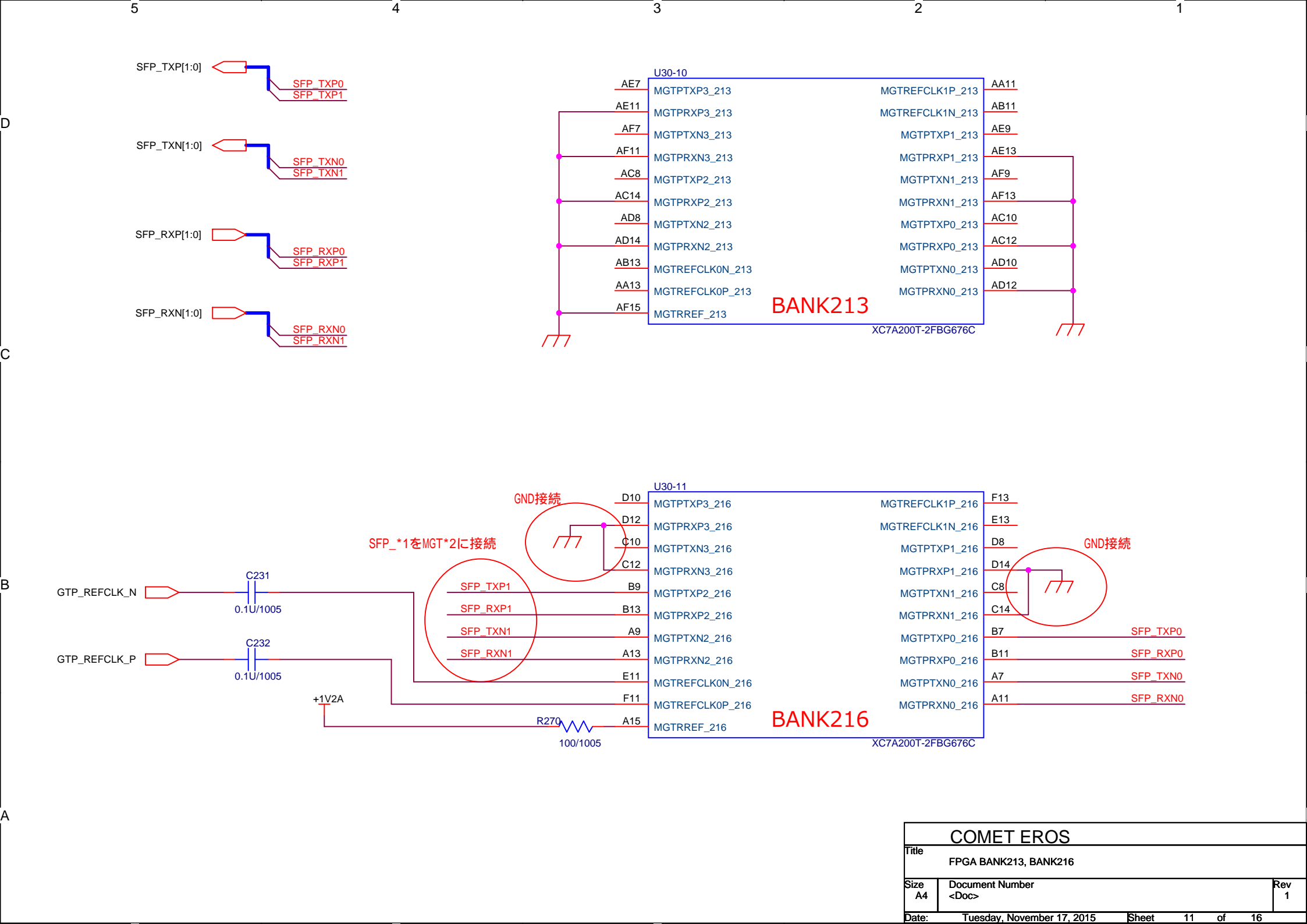
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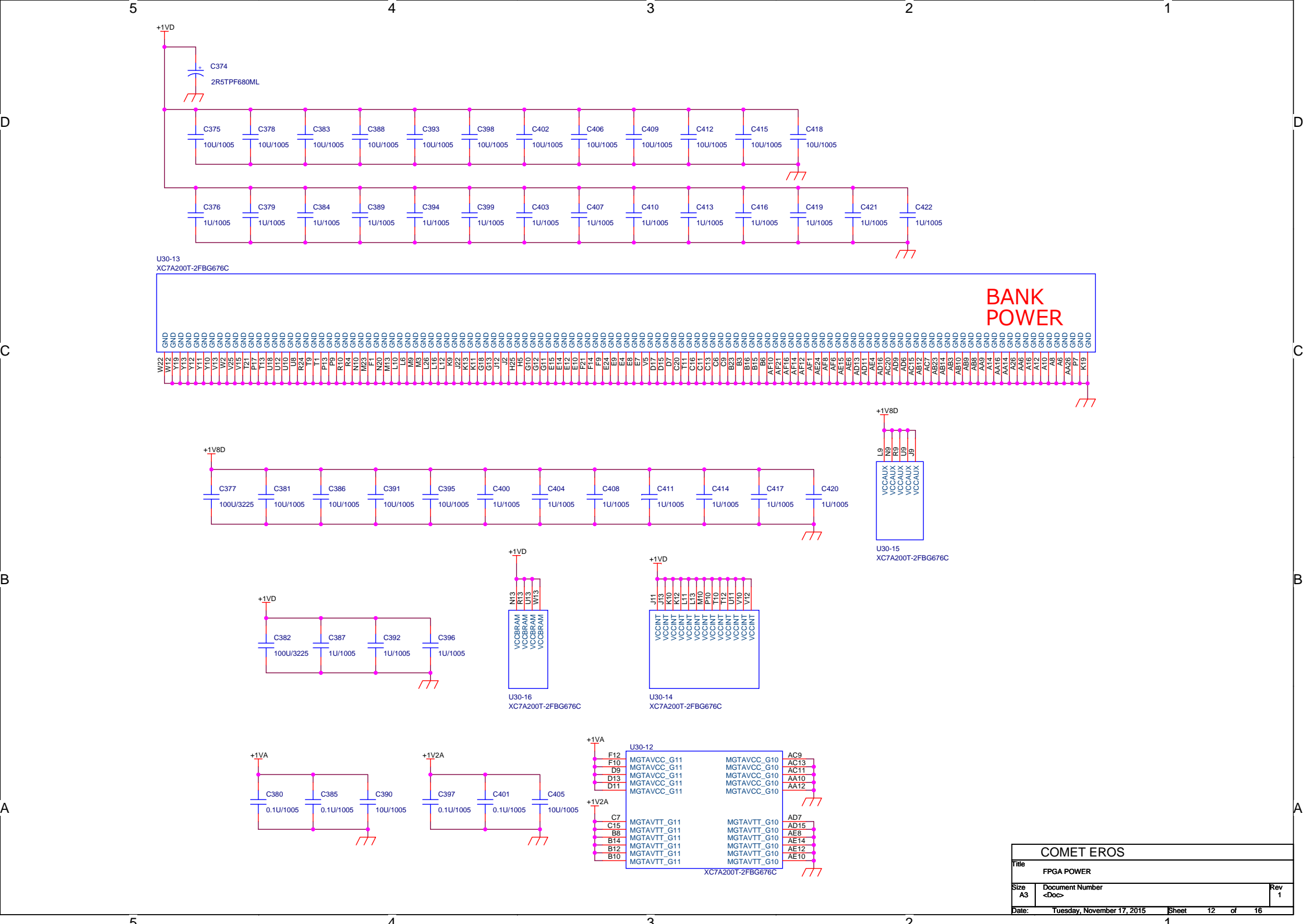


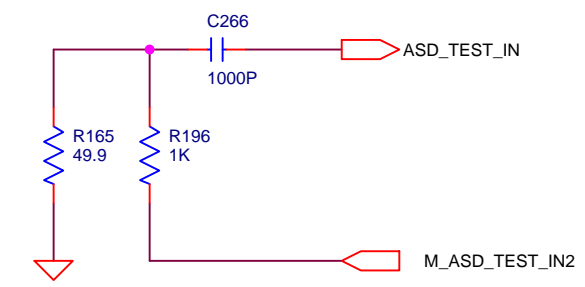
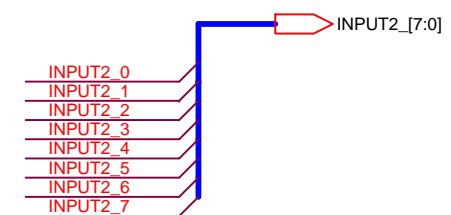
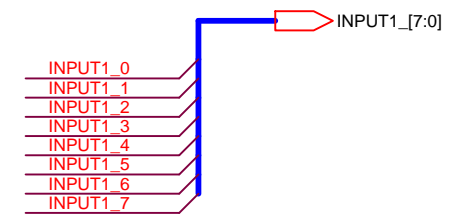
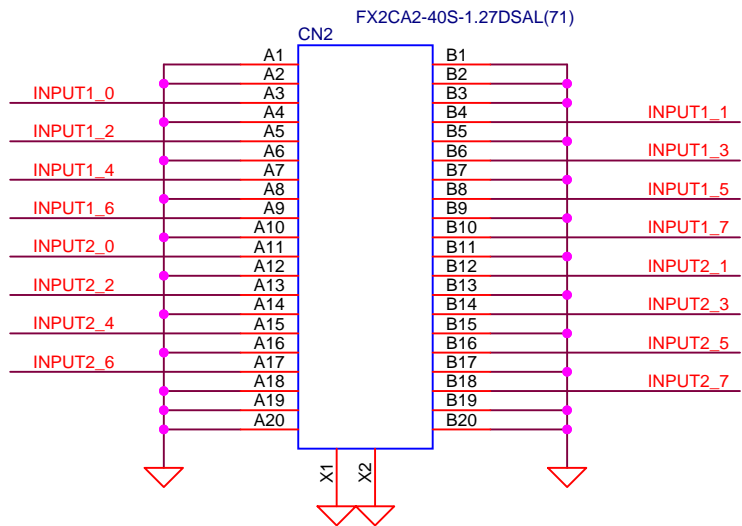




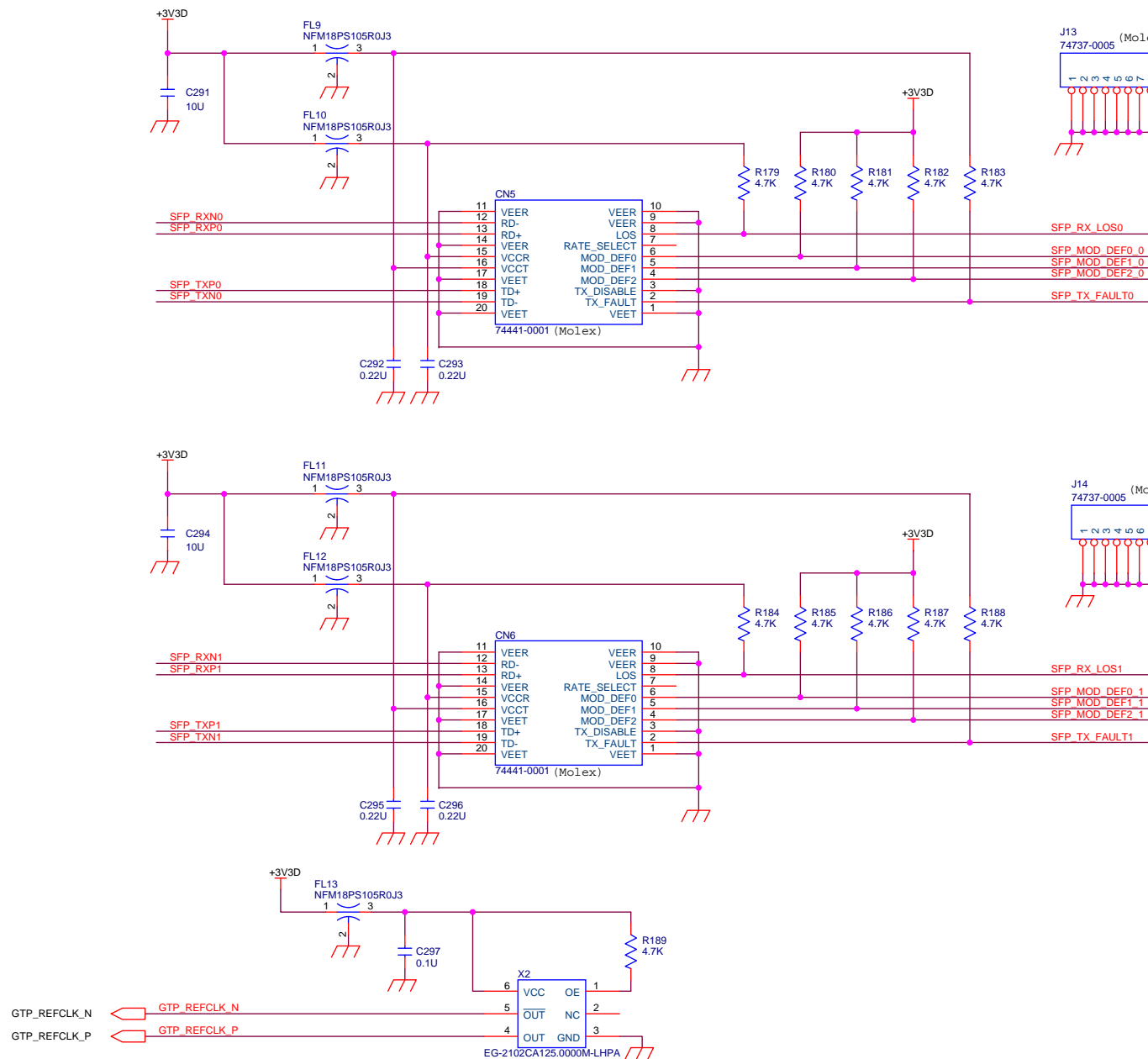
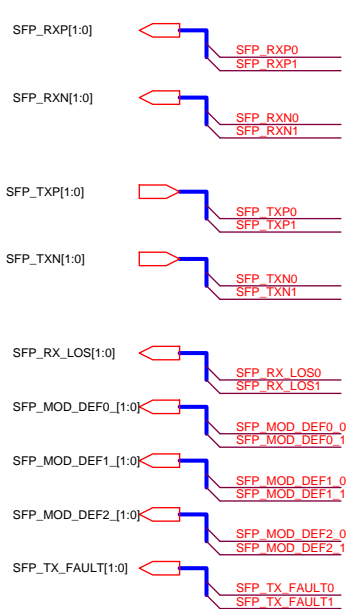
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FPGA BANK0, BANK33, BANK34, BANK35			
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COMET EROS			
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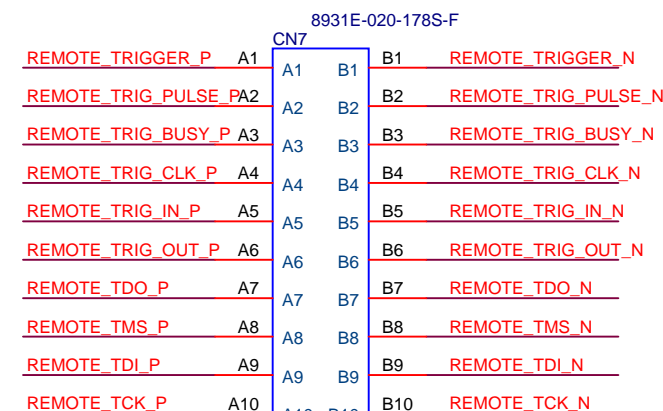
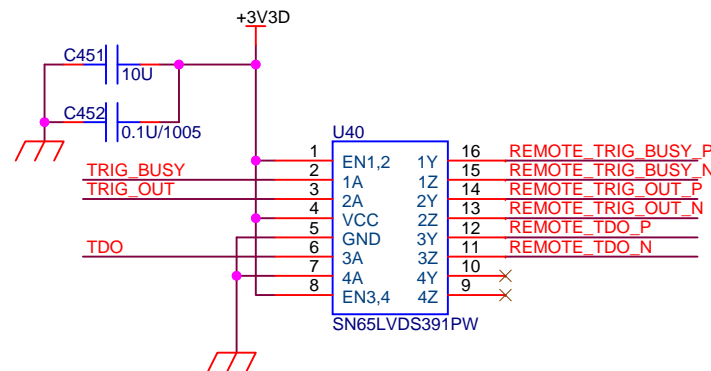
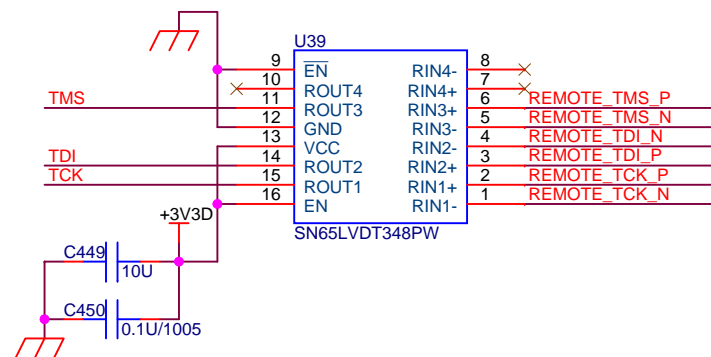
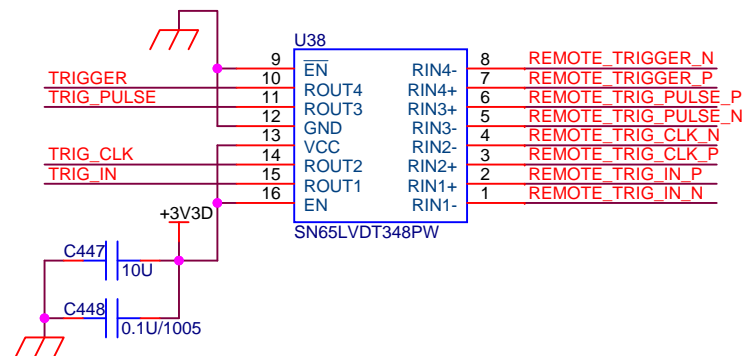
表面で等長配線、ペア配線、最短配線
インピーダンス100Ω、ペアのPとN間の配線長差は±0.5mm

COMET EROS		
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TRIGGER
TRIG_PULSE
TRIG_CLK
TRIG_IN

TRIG_BUSY
TRIG_OUT

TDO
TMS
TDI
TCK



ケーブルシールド用タブ端子
CN7の近くに配置