POWER

POWER

Input

INPUT1_[7:0]

ASD_TEST_IN

INPUT2_[7:0]

ASD_TEST_IN2

ASD1

INPUT_[7:0]

ASD_TEST_IN

ASD_AOUT_[7:0]

ASD_DOUT_[7:0]

ASD_VTH

ASD

ASD1_INPUT[7:0]

ASD1_AOUT[7:0]

ASD2

ASD_TEST_IN

INPUT_[7:0]

ASD_DOUT_[7:0]

ASD_AOUT_[7:0]

ASD_VTH

ASD

ASD2_INPUT[7:0]

ASD2_AOUT[7:0]

DACforASD

DAC3_VOUT

DAC3_SYNC

DAC3_SCLK

DAC3_SDIN

DACforASD

DRS-ADC

ASD_AOUT_[7:0]

ADC_DOUT_P[7:0]

ADC_DOUT_N[7:0]

ADC_FCO_P

ADC_FCO_N

ADC_DCO_P

ADC_DCO_N

ADC_CLK_P

ADC_CLK_N

ADC_SCLK/DTP

ADC_CSB

ADC_SDIO/ODM

DRS_RESET

DRS_SRIN

DRS_SROUT

DRS_SRCLK

DRS_RSRLOAD

DRS_DWRITE

DRS_DENABLE

DRS_WSRIN

DRS_WSROUT

DRS_REFCLK_P

DRS_REFCLK_N

DRS_DTAP

DRS_PLLLCK

DRS_A[3:0]

DAC_SDI

DAC_SCK

DAC_CS/LD

DRS-ADC

ADC1_DOUT_P[7:0]

ADC1_DOUT_N[7:0]

DRS1_A[3:0]

ASD1_DOUT[7:0]

ASD2_DOUT[7:0]

DRS-ADC2

ADC_DOUT_P[7:0]

ADC_DOUT_N[7:0]

ADC_FCO_P

ADC_FCO_N

ADC_DCO_P

ADC_DCO_N

ADC_CLK_P

ADC_CLK_N

ADC_SCLK/DTP

ADC_CSB

ADC_SDIO/ODM

DRS_RESET

DRS_SRIN

DRS_SROUT

DRS_SRCLK

DRS_RSRLOAD

DRS_DWRITE

DRS_DENABLE

DRS_WSRIN

DRS_WSROUT

DRS_REFCLK_P

DRS_REFCLK_N

DRS_DTAP

DRS_PLLLCK

DRS_A[3:0]

DAC_SDI

DAC_SCK

DAC_CS/LD

DRS-ADC

ADC2_DOUT_P[7:0]

ADC2_DOUT_N[7:0]

DRS2_A[3:0]

FPGA

ADC1_DOUT_P[7:0]

ADC1_DOUT_N[7:0]

ADC1_FCO_P

ADC1_FCO_N

ADC1_DCO_P

ADC1_DCO_N

ADC1_CLK_P

ADC1_CLK_N

ADC1_SCLK/DTP

ADC1_CSB

ADC1_SDIO/ODM

DRS1_RESET

DRS1_SRIN

DRS1_SROUT

DRS1_SRCLK

DRS1_RSRLOAD

DRS1_DWRITE

DRS1_DENABLE

DRS1_WSRIN

DRS1_WSROUT

DRS1_REFCLK_P

DRS1_REFCLK_N

DRS1_DTAP

DRS1_PLLLCK

DRS1_A[3:0]

DAC1_SDI

DAC1_SCK

DAC1_CS/LD

ASD1_DOUT[7:0]

ASD2_DOUT[7:0]

ADC2_DOUT_P[7:0]

ADC2_DOUT_N[7:0]

ADC2_FCO_P

ADC2_FCO_N

ADC2_DCO_P

ADC2_DCO_N

ADC2_CLK_P

ADC2_CLK_N

ADC2_SCLK/DTP

ADC2_CSB

ADC2_SDIO/ODM

DRS2_RESET

DRS2_SRIN

DRS2_SROUT

DRS2_SRCLK

DRS2_RSRLOAD

DRS2_DWRITE

DRS2_DENABLE

DRS2_WSRIN

DRS2_WSROUT

DRS2_REFCLK_P

DRS2_REFCLK_N

DRS2_DTAP

DRS2_PLLLCK

DRS2_A[3:0]

DAC2_SDI

DAC2_SCK

DAC2_CS/LD

DAC3_SYNC

DAC3_SCK

DAC3_DIN

ASD_TEST_IN2

FPGA

TRIG-IN

NIM_IN1

NIM_IN2

TRIG-IN

SFP

SFP_RXP[1:0]

SFP_RXN[1:0]

SFP_TXP[1:0]

SFP_TXN[1:0]

GTP_REFCLK_P

GTP_REFCLK_N

SFP

FPGA-PROM-SPI

CCLK

DIN

PROG_B

CSO_B

MOSI

DONE

INIT_B

TMS

TCK

TDI

TDO

FPGA-PROM

EEPROM

EEPROM_CS_[1:0]

EEPROM_SK_[1:0]

EEPROM_DI_[1:0]

EEPROM_DO_[1:0]

EEPROM

COMET Sread

ver2

Title	Top-Scheme	
Size A3	Document Number <Doc>	Rev 1.0
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INPUT_[7:0]

INPUT_0
INPUT_1
INPUT_2
INPUT_3
INPUT_4
INPUT_5
INPUT_6
INPUT_7

+5VA

D1 1SS362
D2 1SS362
D3 1SS362
D4 1SS362
D5 1SS362
D6 1SS362
D7 1SS362
D8 1SS362

+5VD

R1
NCP15XW682J03RB

R2
910/1005

+5VA

J1
pin

ASD_AOUT_[7:0]

ASD_AOUT_0
ASD_AOUT_1
ASD_AOUT_2
ASD_AOUT_3
ASD_AOUT_4
ASD_AOUT_5
ASD_AOUT_6
ASD_AOUT_7

ASD_DOUT_[7:0]

ASD_DOUT_0
ASD_DOUT_1
ASD_DOUT_2
ASD_DOUT_3
ASD_DOUT_4
ASD_DOUT_5
ASD_DOUT_6
ASD_DOUT_7

U1
ASD2010

49	GND	GND	32
50	IN8	VTH	31
51	GND	DOUT8	30 ASD_DOUT_0
52	IN7	DOUT7	29 ASD_DOUT_1
53	GND	DOUT6	28 ASD_DOUT_2
54	IN6	DOUT5	27 ASD_DOUT_3
55	GND	GND	26
56	IN5	GND	25
57	GND	VDDD	24
58	IN4	VDDD	23
59	GND	DOUT4	22 ASD_DOUT_4
60	IN3	DOUT3	21 ASD_DOUT_5
61	GND	DOUT2	20 ASD_DOUT_6
62	IN2	DOUT1	19 ASD_DOUT_7
63	GND	GND	18
64	IN1	GND	17
65	FM		

48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	
GND	GND	VCCA	VCCA	VREF_M	GND	GND	S_LEVEL	GND	VCCD	VCCD	AOUT8	AOUT7	AOUT6	AOUT5	GND	
											ASD_AOUT_0	ASD_AOUT_1	ASD_AOUT_2	ASD_AOUT_3		

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
GND	GND	VCCA	VCCA	TEST	AMP_BIAS	GND	GND	GND	VCCD	VCCD	AOUT1	AOUT2	AOUT3	AOUT4	GND	
											ASD_AOUT_7	ASD_AOUT_6	ASD_AOUT_5	ASD_AOUT_4		

+5VA
+5VD

R3
10K/1005

ASD_TEST_IN

ASD_VTH

C1
0.1U/1005

+3V3D

+5VA
C2 10U
C3 0.1U/1005
C4 0.1U/1005

+5VD
C5 10U
C6 0.1U/1005
C7 0.1U/1005

+3V3D
C8 10U
C9 0.1U/1005

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INPUT_[7:0]

INPUT_0
INPUT_1
INPUT_2
INPUT_3
INPUT_4
INPUT_5
INPUT_6
INPUT_7

+5VA

INPUT_0 — D9 — 1SS362
INPUT_1 — D10 — 1SS362
INPUT_2 — D11 — 1SS362
INPUT_3 — D12 — 1SS362
INPUT_4 — D13 — 1SS362
INPUT_5 — D14 — 1SS362
INPUT_6 — D15 — 1SS362
INPUT_7 — D16 — 1SS362

+5VD

R4
NCP15XW682J03RB

R5
910/1005

+5VA

J2
pin

ASD_AOUT_0
ASD_AOUT_1
ASD_AOUT_2
ASD_AOUT_3

U2
ASD2010

48	GND	GND	32
47	GND	VTH	31
46	VCCA	DOUT8	30
45	VCCA	DOUT7	29
44	VREF_M	DOUT6	28
43	GND	DOUT5	27
42	GND	GND	26
41	S_LEVEL	GND	25
40	GND	VDDD	24
39	VCCD	VDDD	23
38	VCCD	DOUT4	22
37	AOUT8	DOUT3	21
36	AOUT7	DOUT2	20
35	AOUT6	DOUT1	19
34	AOUT5	GND	18
33	GND	GND	17
49	GND		
50	IN8		
51	GND		
52	IN7		
53	GND		
54	IN6		
55	GND		
56	IN5		
57	GND		
58	IN4		
59	GND		
60	IN3		
61	GND		
62	IN2		
63	GND		
64	IN1		
65	FM		
1	GND		
2	GND		
3	VCCA		
4	VCCA		
5	TEST		
6	AMP_BIAS		
7	GND		
8	GND		
9	GND		
10	VCCD		
11	VCCD		
12	AOUT1		
13	AOUT2		
14	AOUT3		
15	AOUT4		
16	GND		

ASD_AOUT_[7:0]

ASD_AOUT_0
ASD_AOUT_1
ASD_AOUT_2
ASD_AOUT_3
ASD_AOUT_4
ASD_AOUT_5
ASD_AOUT_6
ASD_AOUT_7

ASD_DOUT_[7:0]

ASD_DOUT_0
ASD_DOUT_1
ASD_DOUT_2
ASD_DOUT_3
ASD_DOUT_4
ASD_DOUT_5
ASD_DOUT_6
ASD_DOUT_7

ASD_VTH

C10
0.1U/1005

+3V3D

R6
10K/1005

ASD_TEST_IN

+5VA
C11
10U
C12
0.1U/1005
C13
0.1U/1005

+5VD
C14
10U
C15
0.1U/1005
C16
0.1U/1005

+3V3D
C17
10U
C18
0.1U/1005

Title	ASD		
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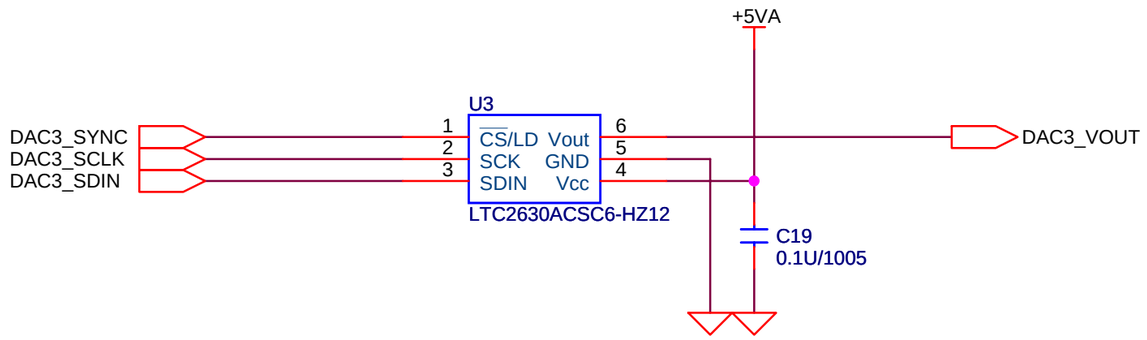

Title: DAC for ASD		
Size: A4	Document Number: <Doc>	Rev: 1.0
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ASD_AOUT_[7:0]

ASD_AOUT_0
ASD_AOUT_1
ASD_AOUT_2
ASD_AOUT_3
ASD_AOUT_4
ASD_AOUT_5
ASD_AOUT_6
ASD_AOUT_7

+2V5A
R8 1.8K
R9 1.8K

ASD_AOUT_0 — C24 0.1U/1005 — R10 15/1005 — DRS_IN_P0
R12 1K/1005 — C26 (10P/1005)
R14 15/1005 — DRS_IN_N0
C33 0.1U/1005 — C30 (10P/1005)

ASD_AOUT_1 — C35 0.1U/1005 — R17 15/1005 — DRS_IN_P1
R19 1K/1005 — C37 (10P/1005)
R23 15/1005 — DRS_IN_N1
C41 0.1U/1005 — C42 (10P/1005)

ASD_AOUT_2 — C46 0.1U/1005 — R26 15/1005 — DRS_IN_P2
R28 1K/1005 — C48 (10P/1005)
R32 15/1005 — DRS_IN_N2
C65 0.1U/1005 — C66 (10P/1005)

ASD_AOUT_3 — C70 0.1U/1005 — R34 15/1005 — DRS_IN_P3
R36 1K/1005 — C72 (10P/1005)
R44 15/1005 — DRS_IN_N3
C79 0.1U/1005 — C80 (10P/1005)

ASD_AOUT_4 — C25 0.1U/1005 — R11 15/1005 — DRS_IN_P4
R13 1K/1005 — C27 (10P/1005)
R15 15/1005 — DRS_IN_N4
C31 0.1U/1005 — C34 (10P/1005)

ASD_AOUT_5 — C36 0.1U/1005 — R18 15/1005 — DRS_IN_P5
R20 1K/1005 — C38 (10P/1005)
R24 15/1005 — DRS_IN_N5
C43 0.1U/1005 — C44 (10P/1005)

ASD_AOUT_6 — C47 0.1U/1005 — R27 15/1005 — DRS_IN_P6
R29 1K/1005 — C49 (10P/1005)
R33 15/1005 — DRS_IN_N6
C67 0.1U/1005 — C68 (10P/1005)

ASD_AOUT_7 — C71 0.1U/1005 — R35 15/1005 — DRS_IN_P7
R37 1K/1005 — C73 (10P/1005)
R45 15/1005 — DRS_IN_N7
C81 0.1U/1005 — C82 (10P/1005)

+5VA — C22 0.1U/1005 — U4 AD8061ARTZ
DRS_ROFS — R7 4.7 — pin J4
DAC_CS\LD
DAC_SCK

+5VA — C20 10U — C21 0.1U/1005
U5 LTC2634CMSE-LZ12
DRS_BIAS
DAC_CS\LD
DAC_SCK
DRS_OOFS
DAC_SDI — C23 0.1U/1005
J3 pin
pin J5

J6 pin — C28 100P/1005
DRS_PLLLCK
DRS_RESET
DRS_ROFS
+2V5A — R21 4.7K/1005
C39 0.1U/1005
C40 10U
C29 470P/1005
R16 249/1005
C32 0.047U/1005
R22 150/1005
J7 pin
DRS_DTAP — DRS_DTAP
DRS_REFCLK_P — DRS_REFCLK_P
R25 100/1005
DRS_REFCLK_N — DRS_REFCLK_N
C45 0.0047U/1005

U6 — DRS4

1 AGND	64 AGND	OUT0+ 57	DRS_OUT_P0
2 AGND	58 AGND	OUT0- 56	DRS_OUT_N0
DRS_IN_P0 3 IN0+	70 AGND	OUT1+ 54	DRS_OUT_P1
DRS_IN_N0 4 IN0-	72 BIAS	OUT1- 55	DRS_OUT_N1
DRS_IN_P1 5 IN1+	36 O-OFS	OUT2+ 52	DRS_OUT_P2
DRS_IN_N1 6 IN1-	30 R-OFS	OUT2- 51	DRS_OUT_N2
DRS_IN_P2 7 IN2+	35 RESET	OUT3+ 49	DRS_OUT_P3
DRS_IN_N2 8 IN2-	25 WSROUT	OUT3- 50	DRS_OUT_N3
DRS_IN_P3 9 IN3+	75 WSRIN	OUT4+ 48	DRS_OUT_P4
DRS_IN_N3 10 IN3-	63 PLLLCK	OUT4- 47	DRS_OUT_N4
DRS_IN_P4 11 IN4+	69 DSPEED	OUT5+ 45	DRS_OUT_P5
DRS_IN_N4 12 IN4-	68 PLLOUT	OUT5- 46	DRS_OUT_N5
DRS_IN_P5 13 IN5+	62 DTAP	OUT6+ 43	DRS_OUT_P6
DRS_IN_N5 14 IN5-	66 REFCLK+	OUT6- 42	DRS_OUT_N6
DRS_IN_P6 15 IN6+	67 REFCLK-	OUT7+ 40	DRS_OUT_P7
DRS_IN_N6 16 IN6-		OUT7- 41	DRS_OUT_N7
DRS_IN_P7 17 IN7+		OUT8+ 37	
DRS_IN_N7 18 IN7-		OUT8- 38	
R52 0/1005 — R55 0/1005 — 20 IN8+ — 21 IN8-		A0 31	DRS_A0
		A1 32	DRS_A1
		A2 60	DRS_A2
		A3 61	DRS_A3
59 AVDD — 71 AVDD — 65 AVDD — 76 AVDD			
39 DGND — 44 DGND — 19 DGND — 22 DGND — 53 DGND			
24 DVDD — 33 DVDD — 34 DVDD — 23 DVDD			
27 SRIN — 28 SRCLK — 29 SROUT — 74 RSRLOAD — 73 DENABLE — 77 DWRITE — EP			

+2V5A — C88 0.1U/1005 — C89 0.1U/1005 — C90 0.1U/1005 — C91 0.1U/1005 — C92 10U
FL2 NFM18PS105R0J3
C97 0.1U/1005 — C99 0.1U/1005 — C100 10U
C96 0.1U/1005 — C98 0.1U/1005

DRS_DWRITE — DRS_DWRITE
DRS_DENABLE — DRS_DENABLE
DRS_RSRLOAD — DRS_RSRLOAD
DRS_SROUT — DRS_SROUT
DRS_SRCLK — DRS_SRCLK
DRS_SRIN — DRS_SRIN

DRS_OUT_P0 — R30 22/1005 — ADC_VIN_P0
DRS_OUT_N0 — C64 2P/1005 — ADC_VIN_N0
R38 22/1005
DRS_OUT_P1 — R40 22/1005 — ADC_VIN_P1
DRS_OUT_N1 — C74 2P/1005 — ADC_VIN_N1
R42 22/1005
DRS_OUT_P2 — R46 22/1005 — ADC_VIN_P2
DRS_OUT_N2 — C84 2P/1005 — ADC_VIN_N2
R48 22/1005
DRS_OUT_P3 — R50 22/1005 — ADC_VIN_P3
DRS_OUT_N3 — C85 2P/1005 — ADC_VIN_N3
R53 22/1005

DRS_DWRITE — R56 4.7K/1005
DRS_DENABLE — R57 4.7K/1005

During power-up, care has to be taken that the DENABLE and DWRITE signals are low

DRS_OUT_P4 — R31 22/1005 — ADC_VIN_P4
DRS_OUT_N4 — C69 2P/1005 — ADC_VIN_N4
R39 22/1005
DRS_OUT_P5 — R41 22/1005 — ADC_VIN_P5
DRS_OUT_N5 — C75 2P/1005 — ADC_VIN_N5
R43 22/1005
DRS_OUT_P6 — R47 22/1005 — ADC_VIN_P6
DRS_OUT_N6 — C83 2P/1005 — ADC_VIN_N6
R49 22/1005
DRS_OUT_P7 — R51 22/1005 — ADC_VIN_P7
DRS_OUT_N7 — C86 2P/1005 — ADC_VIN_N7
R54 22/1005

ADC_CLK_N — C87 0.1U/1005 — R58 100/1005 — C93 0.1U/1005
ADC_CLK_P
C94 0.1U/1005 — C95 1U/1005
C101 0.1U/1005
ビン名変更
キャパシター削除
R59 10K(1%)/1005

DRS_A[3:0]
DRS_A0
DRS_A1
DRS_A2
DRS_A3

ADC_DOUT_P[7:0]
ADC_DOUT_P0
ADC_DOUT_P1
ADC_DOUT_P2
ADC_DOUT_P3
ADC_DOUT_P4
ADC_DOUT_P5
ADC_DOUT_P6
ADC_DOUT_P7

ADC_DOUT_N[7:0]
ADC_DOUT_N0
ADC_DOUT_N1
ADC_DOUT_N2
ADC_DOUT_N3
ADC_DOUT_N4
ADC_DOUT_N5
ADC_DOUT_N6
ADC_DOUT_N7

キャパシター2つ削除

C52 0.1U/1005 — C54 0.1U/1005 — C56 0.1U/1005 — C58 0.1U/1005 — C60 0.1U/1005 — C62 0.1U/1005
C53 0.1U/1005 — C55 0.1U/1005 — C57 0.1U/1005 — C59 0.1U/1005 — C61 0.1U/1005 — C63 10U

+1V8A — FL1 NFM18PS105R0J3 — C77 0.1U/1005 — C78 10U — C76 0.1U/1005

AD9637BCPZ-40

ADC_VIN_P0	43 VIN+A	D+H 16	ADC_DOUT_P7
ADC_VIN_N0	44 VIN-A	D-H 15	ADC_DOUT_N7
ADC_VIN_P1	47 VIN+B	D+G 18	ADC_DOUT_P6
ADC_VIN_N1	46 VIN-B	D-G 17	ADC_DOUT_N6
ADC_VIN_P2	49 VIN+C	D+F 20	ADC_DOUT_P5
ADC_VIN_N2	50 VIN-C	D-F 19	ADC_DOUT_N5
ADC_VIN_P3	53 VIN+D	D+E 22	ADC_DOUT_P4
ADC_VIN_N3	52 VIN-D	D-E 21	ADC_DOUT_N4
ADC_VIN_P4	60 VIN+E	D+D 28	ADC_DOUT_P3
ADC_VIN_N4	61 VIN-E	D-D 27	ADC_DOUT_N3
ADC_VIN_P5	64 VIN+F	D+C 30	ADC_DOUT_P2
ADC_VIN_N5	63 VIN-F	D-C 29	ADC_DOUT_N2
ADC_VIN_P6	2 VIN+G	D+B 32	ADC_DOUT_P1
ADC_VIN_N6	3 VIN-G	D-B 31	ADC_DOUT_N1
ADC_VIN_P7	6 VIN+H	D+A 34	ADC_DOUT_P0
ADC_VIN_N7	5 VIN-H	D-A 33	ADC_DOUT_N0
ADC_CLK_N	9 CLK-	FCO+ 26	ADC_FCO_P
ADC_CLK_P	10 CLK+	FCO- 25	ADC_FCO_N
	56 VREF	DCO+ 24	ADC_DCO_P
	55 SENSE	DCO- 23	ADC_DCO_N
	57 VCM	NC 13	
	58 SYNC	NC 36	
	54 RBIAS		
	EP 65		

CSB 40 — ADC_CSB
SCLK/DTP 38 — ADC_SCLK/DTP
SDIO/DFS 39 — ADC_SDIO/ODM
U27

Title	DRS ADC
Size	Document Number <Doc> — Rev 1.0
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ASD_AOUT_[7:0]
ASD_AOUT_0
ASD_AOUT_1
ASD_AOUT_2
ASD_AOUT_3
ASD_AOUT_4
ASD_AOUT_5
ASD_AOUT_6
ASD_AOUT_7

+2V5A
R61 1.8K
R62 1.8K

ASD_AOUT_0 → C109 0.1U/1005 → R63 15/1005 → DRS_IN_P0
R65 1K/1005 → C111 (10P/1005)
R67 15/1005 → DRS_IN_N0
C118 0.1U/1005 → C115 (10P/1005)

ASD_AOUT_1 → C120 0.1U/1005 → R70 15/1005 → DRS_IN_P1
R72 1K/1005 → C122 (10P/1005)
R76 15/1005 → DRS_IN_N1
C126 0.1U/1005 → C127 (10P/1005)

ASD_AOUT_2 → C131 0.1U/1005 → R79 15/1005 → DRS_IN_P2
R81 1K/1005 → C133 (10P/1005)
R85 15/1005 → DRS_IN_N2
C150 0.1U/1005 → C151 (10P/1005)

ASD_AOUT_3 → C155 0.1U/1005 → R87 15/1005 → DRS_IN_P3
R89 1K/1005 → C157 (10P/1005)
R97 15/1005 → DRS_IN_N3
C164 0.1U/1005 → C165 (10P/1005)

ASD_AOUT_4 → C110 0.1U/1005 → R64 15/1005 → DRS_IN_P4
R66 1K/1005 → C112 (10P/1005)
R68 15/1005 → DRS_IN_N4
C116 0.1U/1005 → C119 (10P/1005)

ASD_AOUT_5 → C121 0.1U/1005 → R71 15/1005 → DRS_IN_P5
R73 1K/1005 → C123 (10P/1005)
R77 15/1005 → DRS_IN_N5
C128 0.1U/1005 → C129 (10P/1005)

ASD_AOUT_6 → C132 0.1U/1005 → R80 15/1005 → DRS_IN_P6
R82 1K/1005 → C134 (10P/1005)
R86 15/1005 → DRS_IN_N6
C152 0.1U/1005 → C153 (10P/1005)

ASD_AOUT_7 → C156 0.1U/1005 → R88 15/1005 → DRS_IN_P7
R90 1K/1005 → C158 (10P/1005)
R98 15/1005 → DRS_IN_N7
C166 0.1U/1005 → C167 (10P/1005)

+5VA
C107 0.1U/1005
U8 AD8061ART
DRS_ROFS → R60 4.7 → U8 IN+
U8 OUT → DAC_BIAS
DAC_CS/LD
DAC_SCK
J9 pin

+5VA
C105 10U
C106 0.1U/1005
J8 pin
U9 LTC2634CMSE-LZ12
DAC_BIAS
DAC_CS/LD
DAC_SCK
DRS_OOFS
DAC_SDI
C108 0.1U/1005
J10 pin

J11 pin
C113 100P/1005
DRS_PLLLCK
DRS_RESET
DRS_ROFS
+2V5A
R74 4.7K/1005
C124 0.1U/1005
C125 10U
C114 470P/1005
R69 249/1005
C117 0.047U/1005
R75 150/1005
J12 pin
DRS_DTAP
DRS_REFCLK_P
R78 100/1005
DRS_REFCLK_N
C130 0.0047U/1005

U10 DRS4

1 AGND	64 AGND	57 OUT0+	DRS_OUT_P0
2 AGND	58 AGND	56 OUT0-	DRS_OUT_N0
DRS_IN_P0 3 IN0+	70 AGND	54 OUT1+	DRS_OUT_P1
DRS_IN_N0 4 IN0-	72 BIAS	55 OUT1-	DRS_OUT_N1
DRS_IN_P1 5 IN1+	36 O-OFS	52 OUT2+	DRS_OUT_P2
DRS_IN_N1 6 IN1-	30 R-OFS	51 OUT2-	DRS_OUT_N2
DRS_IN_P2 7 IN2+	35 RESET	49 OUT3+	DRS_OUT_P3
DRS_IN_N2 8 IN2-	25 WSROUT	50 OUT3-	DRS_OUT_N3
DRS_IN_P3 9 IN3+	75 WSRIN	48 OUT4+	DRS_OUT_P4
DRS_IN_N3 10 IN3-	63 PLLLCK	47 OUT4-	DRS_OUT_N4
DRS_IN_P4 11 IN4+	69 DSPEED	45 OUT5+	DRS_OUT_P5
DRS_IN_N4 12 IN4-	68 PLLOUT	46 OUT5-	DRS_OUT_N5
DRS_IN_P5 13 IN5+	62 DTAP	43 OUT6+	DRS_OUT_P6
DRS_IN_N5 14 IN5-	66 REFCLK+	42 OUT6-	DRS_OUT_N6
DRS_IN_P6 15 IN6+	67 REFCLK-	40 OUT7+	DRS_OUT_P7
DRS_IN_N6 16 IN6-		41 OUT7-	DRS_OUT_N7
DRS_IN_P7 17 IN7+		37 OUT8+	
DRS_IN_N7 18 IN7-		38 OUT8-	
R105 0/1005 20 IN8+		31 A0	DRS_A0
R108 0/1005 21 IN8-		32 A1	DRS_A1
59 AVDD		60 A2	DRS_A2
71 AVDD		61 A3	DRS_A3
65 AVDD			
76 AVDD			
39 DGND			
44 DGND			
19 DGND			
22 DGND			
53 DGND			
24 DVDD			
33 DVDD			
34 DVDD			
23 DVDD			
27 SRIN			
28 SRCLK			
29 SROUT			
74 RSRLOAD			
73 DENABLE			
77 DWRITE			
77 EP			

DRS_DWRITE → DRS_DWRITE
DRS_DENABLE → DRS_DENABLE
DRS_RSRLOAD → DRS_RSRLOAD
DRS_SROUT → DRS_SROUT
DRS_SRCLK → DRS_SRCLK
DRS_SRIN → DRS_SRIN

+2V5A
C173 0.1U/1005
C174 0.1U/1005
C175 0.1U/1005
C176 0.1U/1005
C177 10U
FL4 NFM18PS105R0J3
C182 0.1U/1005
C184 0.1U/1005
C181 0.1U/1005
C183 0.1U/1005
C185 10U

R83 22/1005 DRS_OUT_P0 → ADC_VIN_P0
C149 2P/1005
R91 22/1005 DRS_OUT_N0 → ADC_VIN_N0
R93 22/1005 DRS_OUT_P1 → ADC_VIN_P1
C159 2P/1005
R95 22/1005 DRS_OUT_N1 → ADC_VIN_N1
R99 22/1005 DRS_OUT_P2 → ADC_VIN_P2
C169 2P/1005
R101 22/1005 DRS_OUT_N2 → ADC_VIN_N2
R103 22/1005 DRS_OUT_P3 → ADC_VIN_P3
C170 2P/1005
R106 22/1005 DRS_OUT_N3 → ADC_VIN_N3

R84 22/1005 DRS_OUT_P4 → ADC_VIN_P4
C154 2P/1005
R92 22/1005 DRS_OUT_N4 → ADC_VIN_N4
R94 22/1005 DRS_OUT_P5 → ADC_VIN_P5
C160 2P/1005
R96 22/1005 DRS_OUT_N5 → ADC_VIN_N5
R100 22/1005 DRS_OUT_P6 → ADC_VIN_P6
C168 2P/1005
R102 22/1005 DRS_OUT_N6 → ADC_VIN_N6
R104 22/1005 DRS_OUT_P7 → ADC_VIN_P7
C171 2P/1005
R107 22/1005 DRS_OUT_N7 → ADC_VIN_N7

R109 4.7K/1005 DRS_DWRITE
R110 4.7K/1005 DRS_DENABLE

During power-up, care has to be taken that the DENABLE and DWRITE signals are low

DRS_A[3:0]
DRS_A0
DRS_A1
DRS_A2
DRS_A3

ADC_DOUT_P[7:0]
ADC_DOUT_P0
ADC_DOUT_P1
ADC_DOUT_P2
ADC_DOUT_P3
ADC_DOUT_P4
ADC_DOUT_P5
ADC_DOUT_P6
ADC_DOUT_P7

ADC_DOUT_N[7:0]
ADC_DOUT_N0
ADC_DOUT_N1
ADC_DOUT_N2
ADC_DOUT_N3
ADC_DOUT_N4
ADC_DOUT_N5
ADC_DOUT_N6
ADC_DOUT_N7

キャパシター2つ削除

C137 0.1U/1005
C139 0.1U/1005
C141 0.1U/1005
C143 0.1U/1005
C145 0.1U/1005
C147 0.1U/1005
C148 10U
C138 0.1U/1005
C140 0.1U/1005
C142 0.1U/1005
C144 0.1U/1005
C146 0.1U/1005

+1V8A
FL3 NFM18PS105R0J3
C162 0.1U/1005
C163 10U
C161 0.1U/1005

U28 AD9637BCPZ-40

ADC_VIN_P0 43	VIN+A	16	ADC_DOUT_P7
ADC_VIN_N0 44	VIN-A	15	ADC_DOUT_N7
ADC_VIN_P1 47	VIN+B	18	ADC_DOUT_P6
ADC_VIN_N1 46	VIN-B	17	ADC_DOUT_N6
ADC_VIN_P2 49	VIN+C	20	ADC_DOUT_P5
ADC_VIN_N2 50	VIN-C	19	ADC_DOUT_N5
ADC_VIN_P3 53	VIN+D	22	ADC_DOUT_P4
ADC_VIN_N3 52	VIN-D	21	ADC_DOUT_N4
ADC_VIN_P4 60	VIN+E	28	ADC_DOUT_P3
ADC_VIN_N4 61	VIN-E	27	ADC_DOUT_N3
ADC_VIN_P5 64	VIN+F	30	ADC_DOUT_P2
ADC_VIN_N5 63	VIN-F	29	ADC_DOUT_N2
ADC_VIN_P6 2	VIN+G	32	ADC_DOUT_P1
ADC_VIN_N6 3	VIN-G	31	ADC_DOUT_N1
ADC_VIN_P7 6	VIN+H	34	ADC_DOUT_P0
ADC_VIN_N7 5	VIN-H	33	ADC_DOUT_N0
ADC_CLK_N → R111 100/1005 → C172 0.1U/1005 → C178 0.1U/1005 → 9 CLK-		26	ADC_FCO_P
ADC_CLK_P → 10 CLK+		25	ADC_FCO_N
C179 0.1U/1005 → C180 1U/1005 → 56 VREF		24	ADC_DCO_P
55 SENSE		23	ADC_DCO_N
57 VCM		13	NC
58 SYNC		36	NC
54 RBIAS → R112 10K(1%)/1005			
65 EP			
41 PDWN			
1 3 8 11 12 27 35 45 48 51 62 AVDD			
14 35 DRVDD DVDD			
40 CSB			
38 SCLK/DTP			
39 SDIO/DFS			

ADC_SDIO/ODM → ADC_SDIO/ODM
ADC_SCLK/DTP → ADC_SCLK/DTP
ADC_CSB → ADC_CSB

ピン名変更
キャパシター削除

Title	DRS ADC		
Size	Document Number <Doc>		Rev 1.0
Date:	Monday, August 13, 2012	Sheet 6	of 20

EEPROM_CS_[1:0]

EEPROM_CS_0
EEPROM_CS_1

EEPROM_SK_[1:0]

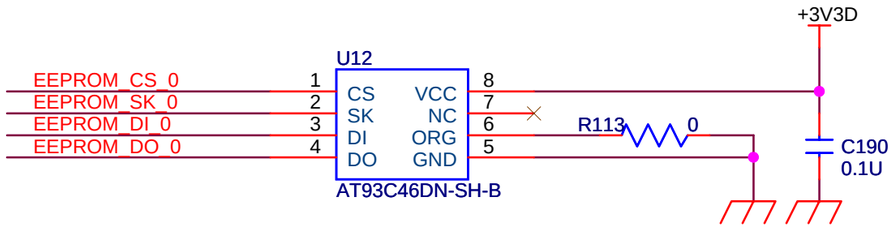
EEPROM_SK_0
EEPROM_SK_1

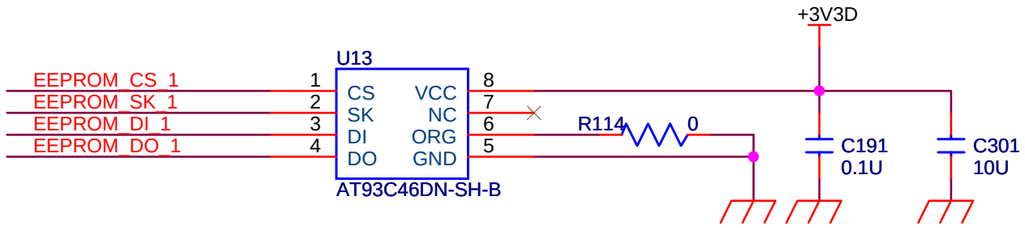
EEPROM_DI_[1:0]

EEPROM_DI_0
EEPROM_DI_1

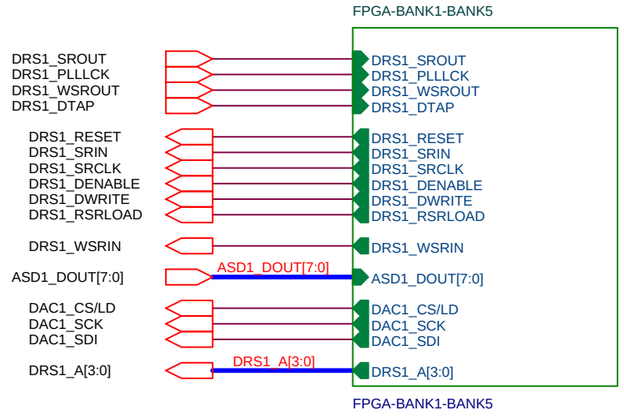
EEPROM_DO_[1:0]

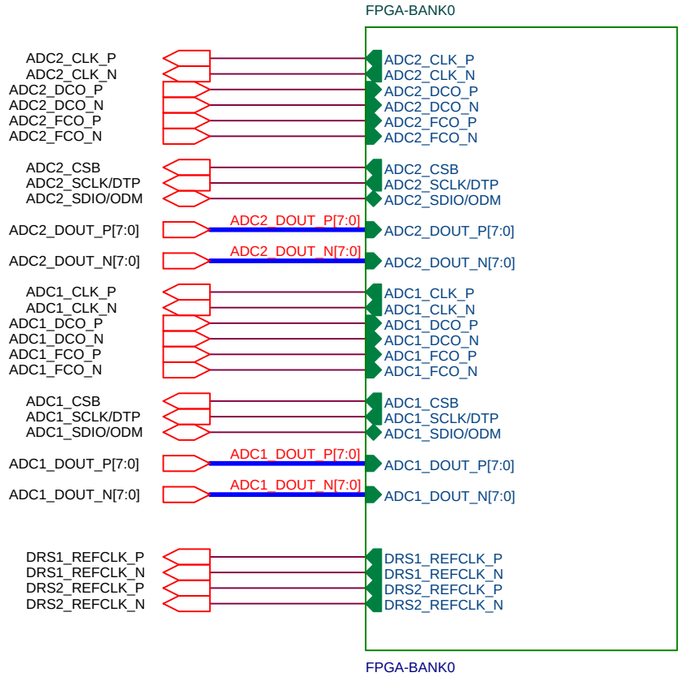
EEPROM_DO_0
EEPROM_DO_1

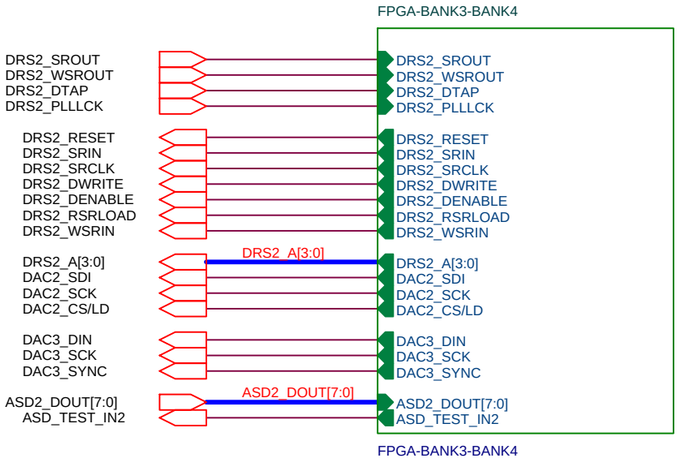


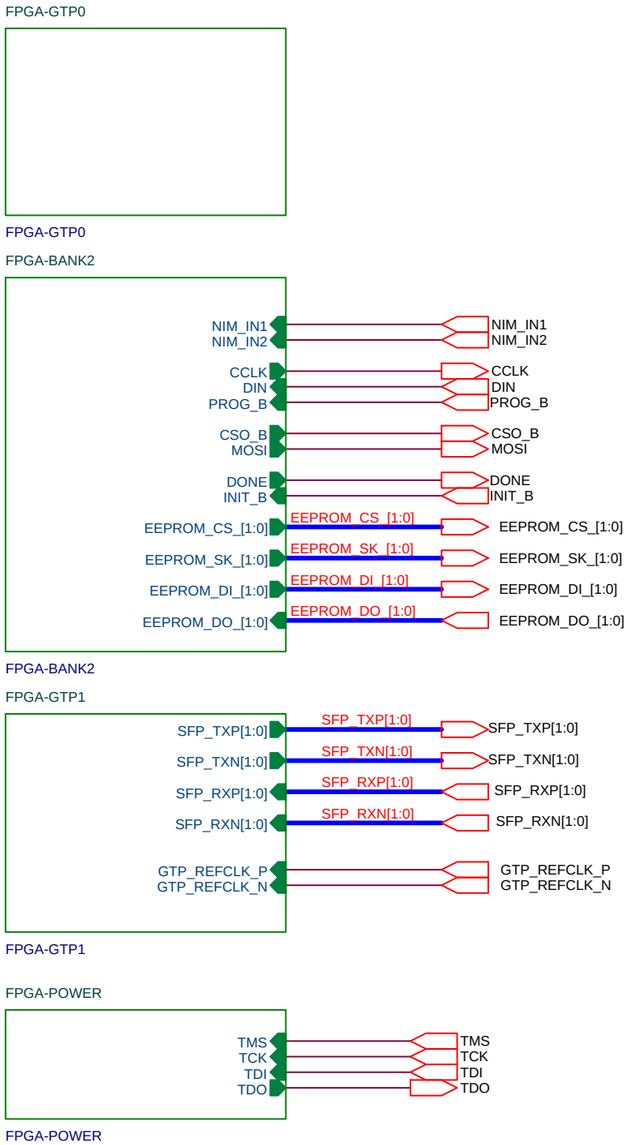


Title: EEPROM		
Size: A4	Document Number: <Doc>	Rev: 1.0
Date: Monday, August 13, 2012	Sheet 7 of 20	









Title: FPGA Spartan-6 LX150T		
Size: A3	Document Number: <Doc>	Rev: 1.0
Date: Monday, August 13, 2012	Sheet 8 of 20	

BANK0

ADC1_CLK_P
ADC1_CLK_N
ADC1_DCO_P
ADC1_DCO_N
ADC1_FCO_P
ADC1_FCO_N
ADC1_CSB
ADC1_SCLK/DTP
ADC1_SDIO/ODM

R198 1K/1005 (ADC1_CSB)
R200 1K/1005 (ADC1_SCLK/DTP)
R116 1K/1005 (ADC1_SDIO/ODM)

抵抗追加

ADC2_CLK_P
ADC2_CLK_N
ADC2_DCO_P
ADC2_DCO_N
ADC2_FCO_P
ADC2_FCO_N
ADC2_CSB
ADC2_SCLK/DTP
ADC2_SDIO/ODM

(ADC2_CSB) R197 1K/1005
(ADC2_SCLK/DTP) R199 1K/1005
(ADC2_SDIO/ODM) R115 1K/1005

抵抗追加

ADC1_DOUT_P[7:0]
ADC1_DOUT_P0
ADC1_DOUT_P1
ADC1_DOUT_P2
ADC1_DOUT_P3
ADC1_DOUT_P4
ADC1_DOUT_P5
ADC1_DOUT_P6
ADC1_DOUT_P7

ADC1_DOUT_N[7:0]
ADC1_DOUT_N0
ADC1_DOUT_N1
ADC1_DOUT_N2
ADC1_DOUT_N3
ADC1_DOUT_N4
ADC1_DOUT_N5
ADC1_DOUT_N6
ADC1_DOUT_N7

R117 0/1005

移動不可

U14-1

	H7	IO_L1P_HSWAPEN_0	IO_L34P_GCLK19_0/TL	E13	ADC2_DCO_P
	G7	IO_L1N_VREF_0	IO_L34N_GCLK18_0/TL	D13	ADC2_DCO_N
ADC2_DOUT_P2	H8	IO_L2P_0	IO_L35P_GCLK17_0/TL	C13	DRS2_REFCLK_P
ADC2_DOUT_N2	G8	IO_L2N_0	IO_L35N_GCLK16_0/TL	A13	DRS2_REFCLK_N
ADC2_DOUT_P3	F7	IO_L3P_0	IO_L36P_GCLK15_0/TR	B12	DRS1_REFCLK_P
ADC2_DOUT_N3	F6	IO_L3N_0	IO_L36N_GCLK14_0/TR	A12	DRS1_REFCLK_N
ADC2_DOUT_P7	C3	IO_L4P_0	IO_L37P_GCLK13_0/TR	B14	ADC1_DCO_P
ADC2_DOUT_N7	B3	IO_L4N_0	IO_L37N_GCLK12_0/TR	A14	ADC1_DCO_N
	G6	IO_L5P_0	IO_L38P_0	K12	
	F5	IO_L5N_0	IO_L38N_VREF_0	J12	
ADC2_FCO_P	E6	IO_L8P_0	IO_L39P_0	J13	
ADC2_FCO_N	E5	IO_L8N_VREF_0	IO_L39N_0	H13	
ADC2_DOUT_P1	H9	IO_L13P_0	IO_L40P_0	F14	ADC1_CLK_P
ADC2_DOUT_N1	G9	IO_L13N_0	IO_L40N_0	E14	ADC1_CLK_N
ADC2_CLK_P	A3	IO_L14P_0	IO_L41P_0	K14	
ADC2_CLK_N	A2	IO_L14N_0	IO_L41N_0	H14	
	F9	IO_L15P_0	IO_L43P_0	J15	
	E8	IO_L15N_0	IO_L43N_0	H15	
ADC2_DOUT_P4	D5	IO_L16P_0	IO_L48P_0	J16	
ADC2_DOUT_N4	C5	IO_L16N_0	IO_L48N_0	J17	
	H10	IO_L21P_0	IO_L49P_0	F16	ADC1_DOUT_P6
	G10	IO_L21N_0	IO_L49N_0	E16	ADC1_DOUT_N6
ADC2_DOUT_P6	B4	IO_L22P_0	IO_L50P_0	G15	ADC1_DOUT_P7
ADC2_DOUT_N6	A4	IO_L22N_0	IO_L50N_0	F15	ADC1_DOUT_N7
ADC2_DOUT_P0	F10	IO_L23P_0	IO_L51P_0	F18	ADC1_FCO_P
ADC2_DOUT_N0	E10	IO_L23N_0	IO_L51N_0	E18	ADC1_FCO_N
ADC2_DOUT_P5	B5	IO_L24P_0	IO_L56P_0	G16	ADC1_DOUT_P5
ADC2_DOUT_N5	A5	IO_L24N_0	IO_L56N_0	F17	ADC1_DOUT_N5
	G12	IO_L30P_0	IO_L57P_0	F20	ADC1_DOUT_P2
(ADC2_SDIO/ODM)	F11	IO_L30N_0	IO_L57N_0	E20	ADC1_DOUT_N2
(ADC2_CSB)	F12	IO_L31P_0	IO_L58P_0	H17	ADC1_DOUT_P4
	E12	IO_L31N_0	IO_L58N_0	G17	ADC1_DOUT_N4
	J11	IO_L32P_0	IO_L59P_0	C21	ADC1_DOUT_P1
(ADC2_SCLK/DTP)	G11	IO_L32N_0	IO_L59N_0	B21	ADC1_DOUT_N1
	H12	IO_L33P_0	IO_L62P_0	H18	
	G13	IO_L33N_0	IO_L62N_VREF_0	H19	
			IO_L63P_SCP7_0	B22	ADC1_DOUT_P0
			IO_L63N_SCP6_0	A22	ADC1_DOUT_N0
			IO_L64P_SCP5_0	G19	ADC1_DOUT_P3
			IO_L64N_SCP4_0	F19	ADC1_DOUT_N3
			IO_L65P_SCP3_0	B23	(ADC1_SDIO/ODM)
			IO_L65N_SCP2_0	A23	(ADC1_SCLK/DTP)
			IO_L66P_SCP1_0	D21	
			IO_L66N_SCP0_0	D22	(ADC1_CSB)

+2V5D

B13	VCCO_0
C22	VCCO_0
C4	VCCO_0
E21	VCCO_0
F13	VCCO_0
F8	VCCO_0
G18	VCCO_0
H11	VCCO_0
J14	VCCO_0
H16	VCCO_0

BANK0

XC6SLX150T-2FG(G)676

GCLKピンのみ可

ADC2_DOUT_P[7:0]
ADC2_DOUT_P0
ADC2_DOUT_P1
ADC2_DOUT_P2
ADC2_DOUT_P3
ADC2_DOUT_P4
ADC2_DOUT_P5
ADC2_DOUT_P6
ADC2_DOUT_P7

ADC2_DOUT_N[7:0]
ADC2_DOUT_N0
ADC2_DOUT_N1
ADC2_DOUT_N2
ADC2_DOUT_N3
ADC2_DOUT_N4
ADC2_DOUT_N5
ADC2_DOUT_N6
ADC2_DOUT_N7

DRS1_REFCLK_P
DRS1_REFCLK_N
DRS2_REFCLK_P
DRS2_REFCLK_N

BANK0の近くに置く

+2V5D C192 100U/3225
+2V5D C193 10U
+2V5D C194 1U/1005
+2V5D C195 1U/1005
+2V5D C196 1U/1005

Title	FPGA BANK0	
Size A3	Document Number <Doc>	Rev 1.0
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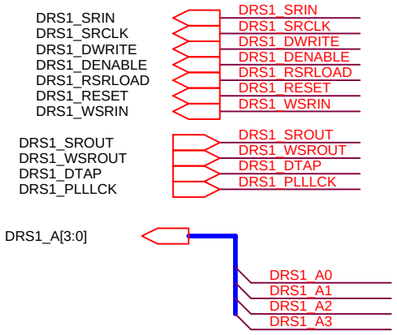
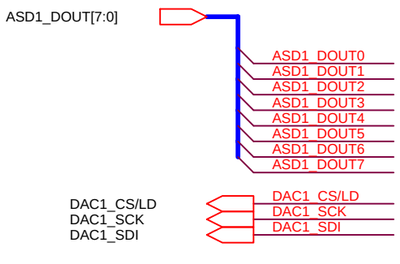
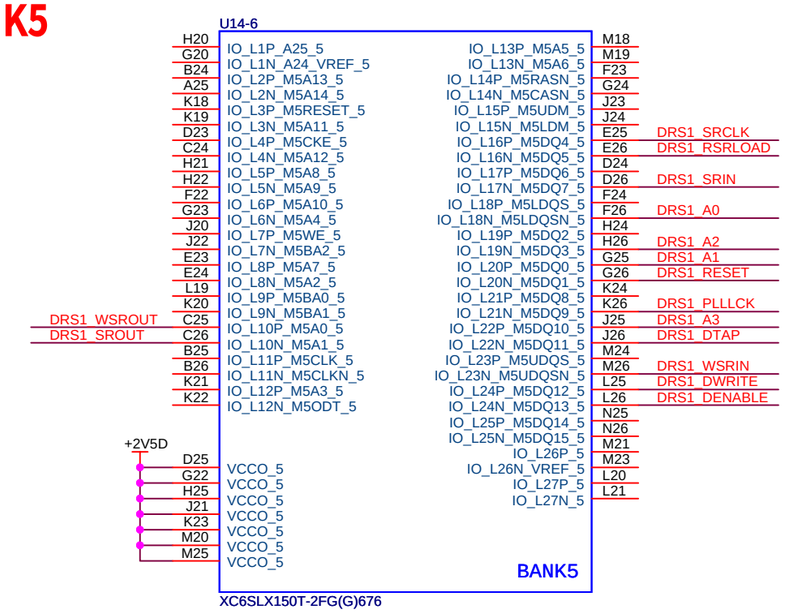
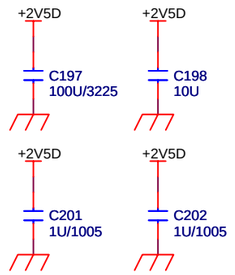
BANK5



DRS1の信号はBANK5のみ可

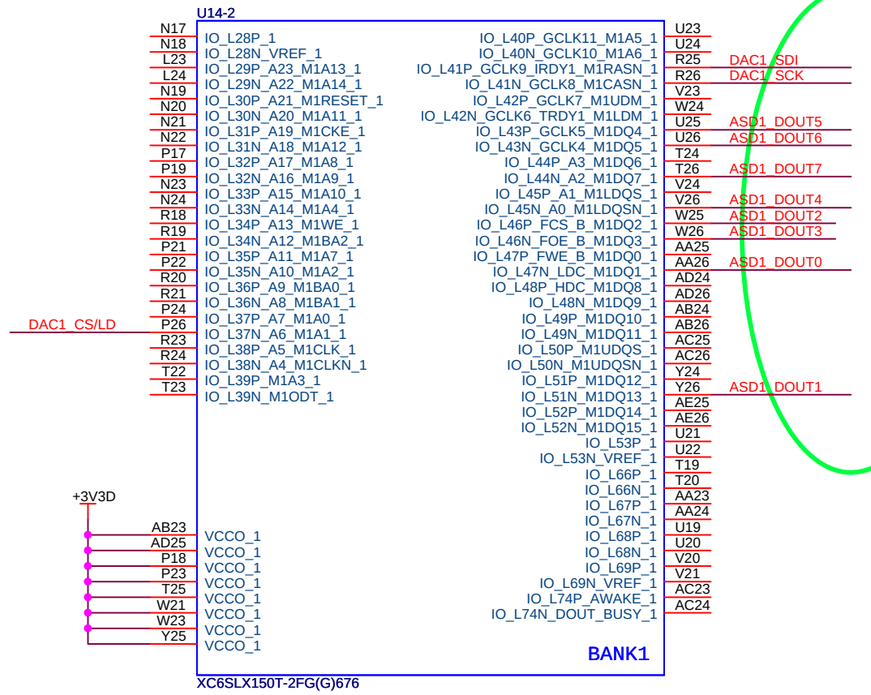


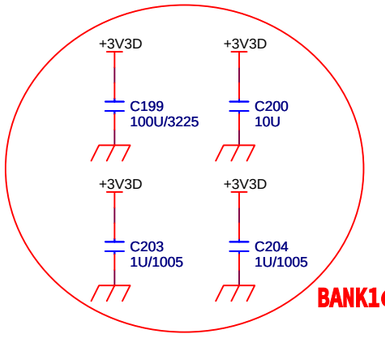




BANK5の近くに置く

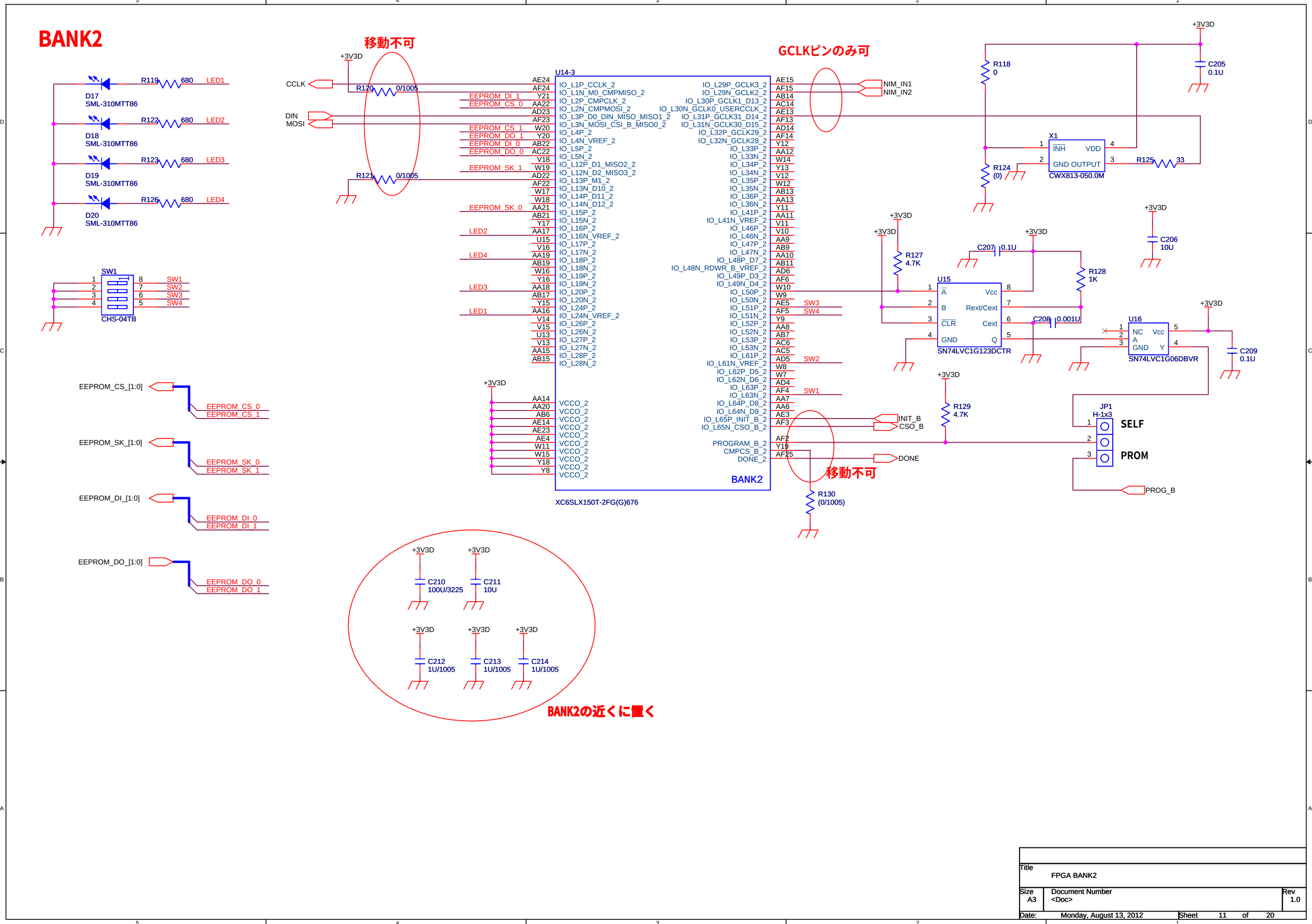
BANK1





BANK1の近くに置く

Title: FPGA BANK1 BANK5		
Size: A3	Document Number: <Doc>	Rev: 1.0
Date: Wednesday, August 15, 2012	Sheet 10 of 20	


BANK2
移動不可
GCLKピンのみ可
U14-3
XC6SLX150T-2FG(G)676
BANK2
CCLK
DIN
MOSI
NIM_IN1
NIM_IN2
INIT_B
CSO_B
DONE
PROGRAM_B_2
CMPCS_B_2
DONE_2
R120 0/1005
R121 0/1005
R119 680 LED1
R122 680 LED2
R123 680 LED3
R126 680 LED4
D17 SML-310MTT86
D18 SML-310MTT86
D19 SML-310MTT86
D20 SML-310MTT86
SW1 CHS-04TB
EEPROM_CS_[1:0]
EEPROM_SK_[1:0]
EEPROM_DI_[1:0]
EEPROM_DO_[1:0]
EEPROM_CS_0
EEPROM_CS_1
EEPROM_SK_0
EEPROM_SK_1
EEPROM_DI_0
EEPROM_DI_1
EEPROM_DO_0
EEPROM_DO_1
LED1
LED2
LED3
LED4
SW1
SW2
SW3
SW4
+3V3D
R118 0
R124 (0)
R125 33
X1 CWX813-050.0M
C205 0.1U
C206 10U
C207 0.1U
C208 0.001U
C209 0.1U
R127 4.7K
R128 1K
R129 4.7K
U15 SN74LVC1G123DCTR
U16 SN74LVC1G06DBVR
JP1 H-1x3
SELF
PROM
PROG_B
R130 (0/1005)
C210 100U/3225
C211 10U
C212 1U/1005
C213 1U/1005
C214 1U/1005
BANK2の近くに置く
Title FPGA BANK2
Size A3
Document Number <Doc>
Rev 1.0
Date: Monday, August 13, 2012
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BANK4

DRS2_RESET
DRS2_SRIN
DRS2_SRCLK
DRS2_DWRITE
DRS2_DENABLE
DRS2_RSRLOAD
DRS2_WSRIN
DRS2_SROUT
DRS2_WSROUT
DRS2_DTAP
DRS2_PLLLCK
DRS2_A[3:0]
DRS2_A0
DRS2_A1
DRS2_A2
DRS2_A3

DRS2の信号はBANK4のみ可

ASD2_DOUT[7:0]
ASD2_DOUT0
ASD2_DOUT1
ASD2_DOUT2
ASD2_DOUT3
ASD2_DOUT4
ASD2_DOUT5
ASD2_DOUT6
ASD2_DOUT7

DAC2_SDI
DAC2_SCK
DAC2_CS/LD
DAC3_DIN
DAC3_SCK
DAC3_SYNC

ASD_TEST_IN2
R131
49.9
(ASD_TEST_IN2)

U14-5

	M4	IO_L58P_4	IO_L69P_M4UDM_4	J4	
	N3	IO_L58N_VREF_4	IO_L69N_M4LDM_4	J3	
DRS2_WSROUT	N2	IO_L59P_M4DQ14_4	IO_L70P_M4RASN_4	L9	
(ASD_TEST_IN2)	N1	IO_L59N_M4DQ15_4	IO_L70N_M4CASN_4	L8	
	M3	IO_L60P_M4DQ12_4	IO_L71P_M4A5_4	L4	
DRS2_SROUT	M1	IO_L60N_M4DQ13_4	IO_L71N_M4A6_4	L3	
DRS2_SRCLK	L2	IO_L61P_M4UDQS_4	IO_L72P_M4A3_4	M8	
DRS2_SRIN	L1	IO_L61N_M4UDQSN_4	IO_L72N_M4ODT_4	M6	
	K3	IO_L62P_M4DQ10_4	IO_L73P_M4CLK_4	K5	
DRS2_RSRLOAD	K1	IO_L62N_M4DQ11_4	IO_L73N_M4CLKN_4	J5	
DRS2_A1	J2	IO_L63P_M4DQ8_4	IO_L74P_M4A0_4	L7	
DRS2_A0	J1	IO_L63N_M4DQ9_4	IO_L74N_M4A1_4	L6	
	H3	IO_L64P_M4DQ0_4	IO_L75P_M4BA0_4	B2	
DRS2_RESET	H1	IO_L64N_M4DQ1_4	IO_L75N_M4BA1_4	B1	
DRS2_A3	G2	IO_L65P_M4DQ2_4	IO_L76P_M4A7_4	L10	
DRS2_A2	G1	IO_L65N_M4DQ3_4	IO_L76N_M4A2_4	K10	
	F3	IO_L66P_M4LDQS_4	IO_L77P_M4WE_4	G4	
DRS2_DTAP	F1	IO_L66N_M4LDQSN_4	IO_L77N_M4BA2_4	G3	
DRS2_DWRITE	E2	IO_L67P_M4DQ6_4	IO_L78P_M4A10_4	J9	
DRS2_PLLLCK	E1	IO_L67N_M4DQ7_4	IO_L78N_M4A4_4	J7	
	D3	IO_L68P_M4DQ4_4	IO_L79P_M4A8_4	C2	
DRS2_DENABLE	D1	IO_L68N_M4DQ5_4	IO_L79N_M4A9_4	C1	DRS2_WSRIN
			IO_L80P_M4CKE_4	K9	
			IO_L80N_M4A12_4	K8	
			IO_L81P_M4RESET_4	E4	
	D2	VCCO_4	IO_L81N_M4A11_4	E3	
	F4	VCCO_4	IO_L82P_M4A13_4	K7	
	H2	VCCO_4	IO_L82N_M4A14_4	K6	
	J6	VCCO_4	IO_L83P_4	H6	
	K4	VCCO_4	IO_L83N_VREF_4	H5	
	M2	VCCO_4			
	M7	VCCO_4			

+2V5D

BANK4

XC6SLX150T-2FG(G)676

BANK3

U14-4

	AB5	IO_L1P_3	IO_L38P_M3DQ2_3	W2	DAC2_SDI
	AC4	IO_L1N_VREF_3	IO_L38N_M3DQ3_3	W1	ASD2_DOUT7
	AA4	IO_L2P_3	IO_L39P_M3LDQS_3	V3	
	AA3	IO_L2N_3	IO_L39N_M3LDQSN_3	V1	ASD2_DOUT6
	Y6	IO_L7P_3	IO_L40P_M3DQ6_3	U2	ASD2_DOUT5
	Y5	IO_L7N_3	IO_L40N_M3DQ7_3	U1	ASD2_DOUT4
	AB4	IO_L8P_3	IO_L41P_GCLK27_M3DQ4_3	T3	
	AC3	IO_L8N_3	IO_L41N_GCLK26_M3DQ5_3	T1	ASD2_DOUT3
	V7	IO_L9P_3	IO_L42P_GCLK25_TRDY2_M3UDM_3	V4	
	V6	IO_L9N_3	IO_L42N_GCLK24_M3LDM_3	W3	
	U4	IO_L10P_3	IO_L43P_GCLK23_M3RASN_3	R7	
	U3	IO_L10N_3	IO_L43N_GCLK22_IRDY2_M3CASN_3	R6	
	V5	IO_L17P_3	IO_L44P_GCLK21_M3A5_3	R2	ASD2_DOUT2
	W5	IO_L17N_VREF_3	IO_L44N_GCLK20_M3A6_3	R1	ASD2_DOUT1
	U9	IO_L18P_3	IO_L45P_M3A3_3	R8	
	U8	IO_L18N_3	IO_L45N_M3ODT_3	T8	
	U7	IO_L31P_3	IO_L46P_M3CLK_3	U5	
	T6	IO_L31N_VREF_3	IO_L46N_M3CLKN_3	T4	
	AB3	IO_L32P_M3DQ14_3	IO_L47P_M3A0_3	R10	
DAC3_SCK	AB1	IO_L32N_M3DQ15_3	IO_L47N_M3A1_3	T9	
	AD3	IO_L33P_M3DQ12_3	IO_L48P_M3BA0_3	P3	
	AD1	IO_L33N_M3DQ13_3	IO_L48N_M3BA1_3	P1	ASD2_DOUT0
	AC2	IO_L34P_M3UDQS_3	IO_L49P_M3A7_3	N6	
DAC3_SYNC	AC1	IO_L34N_M3UDQSN_3	IO_L49N_M3A2_3	P6	
	AE2	IO_L35P_M3DQ10_3	IO_L50P_M3WE_3	P5	
	AE1	IO_L35N_M3DQ11_3	IO_L50N_M3BA2_3	R5	
DAC3_DIN	AA2	IO_L36P_M3DQ8_3	IO_L51P_M3A10_3	N8	
DAC2_CS/LD	AA1	IO_L36N_M3DQ9_3	IO_L51N_M3A4_3	N7	
	Y3	IO_L37P_M3DQ0_3	IO_L52P_M3A8_3	R4	
DAC2_SCK	Y1	IO_L37N_M3DQ1_3	IO_L52N_M3A9_3	R3	
			IO_L53P_M3CKE_3	R9	
			IO_L53N_M3A12_3	P8	
			IO_L54P_M3RESET_3	N5	
	AD2	VCCO_3	IO_L54N_M3A11_3	N4	
	P4	VCCO_3	IO_L55P_M3A13_3	P10	
	P9	VCCO_3	IO_L55N_M3A14_3	N9	
	T2	VCCO_3	IO_L57P_3	M10	
	T7	VCCO_3	IO_L57N_VREF_3	M9	
	W4	VCCO_3			
	W6	VCCO_3			
	Y2	VCCO_3			

+3V3D

BANK3

XC6SLX150T-2FG(G)676

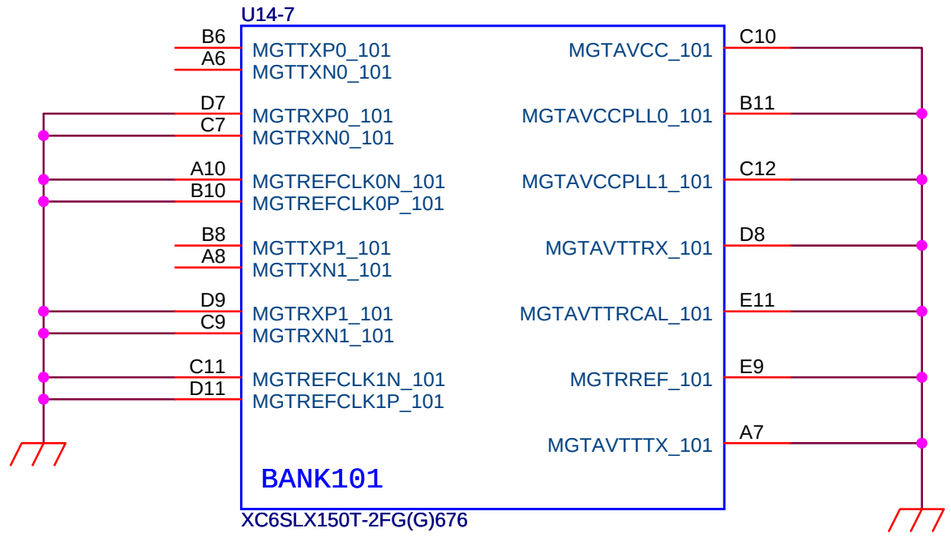
+2V5D
C215
100U/3225
+2V5D
C216
10U
+2V5D
C219
1U/1005
+2V5D
C220
1U/1005

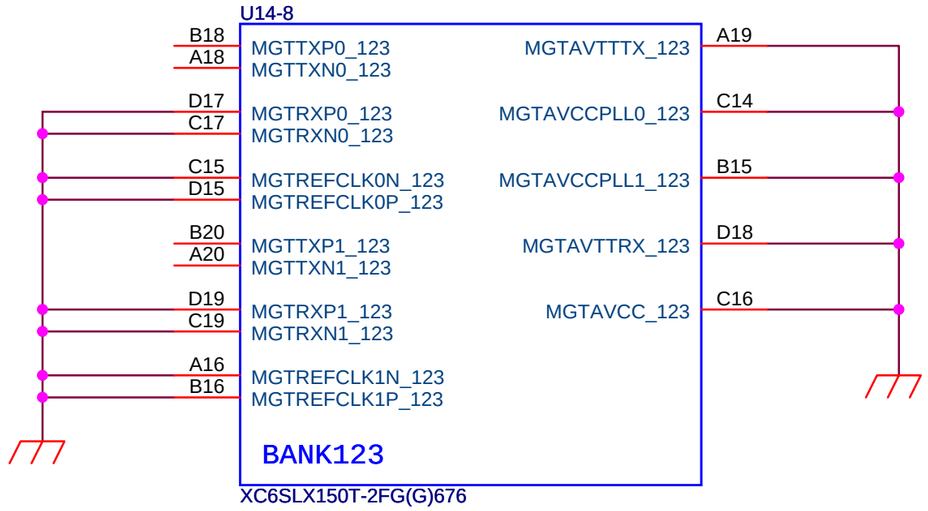
BANK4の近くに置く

+3V3D
C217
100U/3225
+3V3D
C218
10U
+3V3D
C221
1U/1005
+3V3D
C222
1U/1005

BANK3の近くに置く

Title	FPGA BANK3 BANK4	
Size A3	Document Number <Doc>	Rev 1.0
Date: Wednesday, August 15, 2012	Sheet 12 of 20	





Title	FPGA BANK101 BNAK123	
Size A4	Document Number <Doc>	Rev 1.0
Date: Monday, August 13, 2012	Sheet 13 of 20	

SFP_RXP[1:0]
SFP_RXP0
SFP_RXP1
SFP_RXN[1:0]
SFP_RXN0
SFP_RXN1
SFP_TXP[1:0]
SFP_TXP0
SFP_TXP1
SFP_TXN[1:0]
SFP_TXN0
SFP_TXN1

+2V5D

U17
LP3879SD-1.2
1 BYPASS
2 N/C
3 GROUND
4 INPUT
8 SHUTDOWN
7 N/C
6 SENSE
5 OUTPUT
9 GROUND (Pad)

C223 0.01U
C224 10U
C225 47U/3216
FL5 NFM18PS105R0J3
C226 10U

U14-10
XC6SLX150T-2FG(G)676

SFP_TXN0 AE9 MGTTXP1_245
SFP_TXP0 AF9 MGTTXN1_245
SFP_RXP0 AC10 MGTRXP1_245
SFP_RXN0 AD10 MGTRXN1_245
AD12 MGTREFCLK1N_245
AC12 MGTREFCLK1P_245
SFP_RXP1 AC8 MGTRXP0_245
SFP_RXN1 AD8 MGTRXN0_245
SFP_TXN1 AE7 MGTTXP0_245
SFP_TXP1 AF7 MGTTXN0_245
GTP_REFCLK_N C231 0.01U/1005 AF11 MGTREFCLK0N_245
GTP_REFCLK_P C232 0.01U/1005 AE11 MGTREFCLK0P_245

MGTAVCC_245 AD11
MGTAVCCPLL0_245 AE12
MGTAVCCPLL1_245 AD13
MGTAVTTRX_245 AC9
MGTAVTTTX_245 AF8
MGTAVTTRCAL_245 AB12
MGTRREF_245 AB10

C227 0.22U/1005
C228 0.22U/1005
C229 0.22U/1005
C230 0.22U/1005
C233 0.22U/1005
C234 0.22U/1005
R132 49.9
等長配線

BANK245

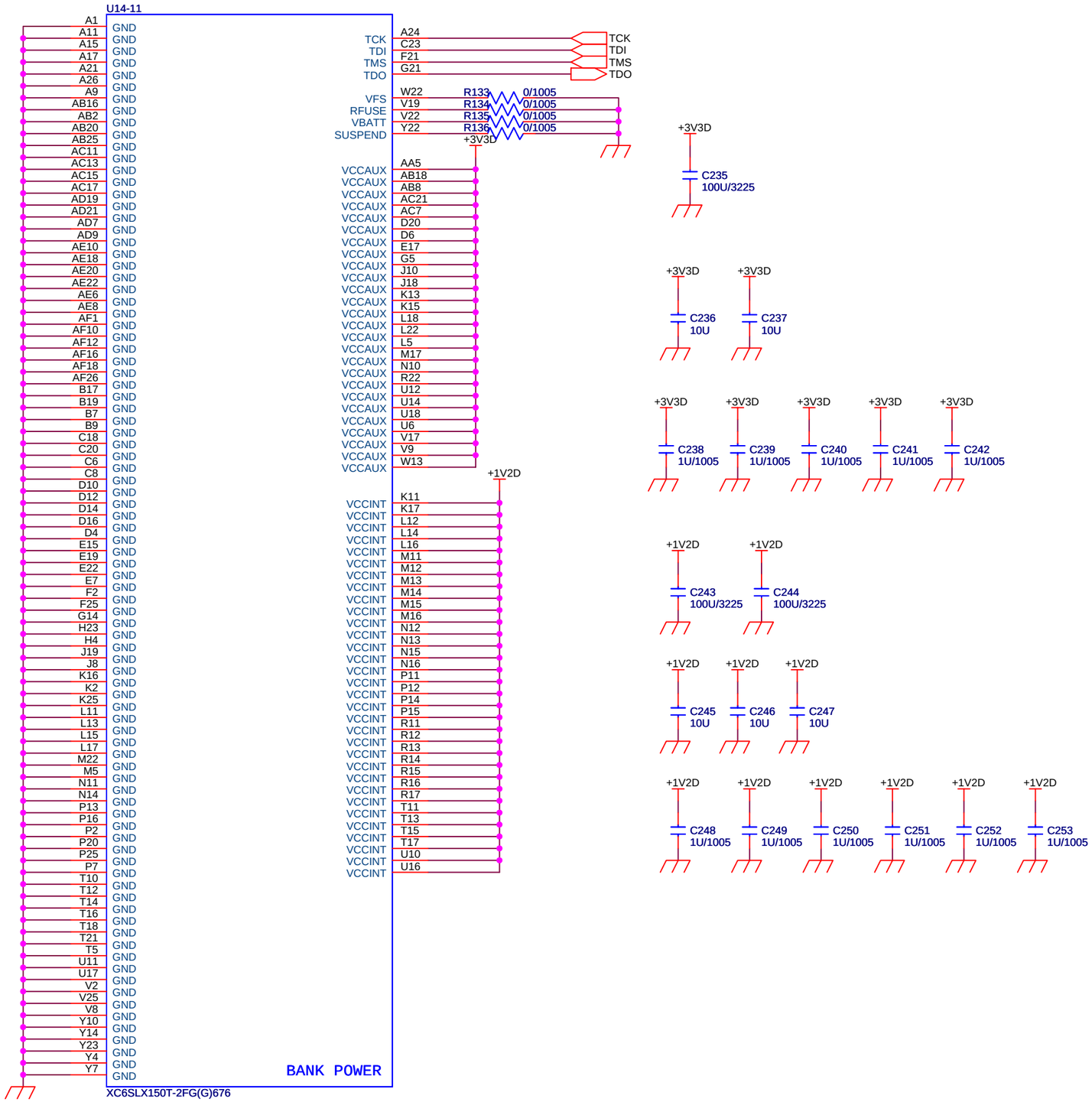
U14-9
XC6SLX150T-2FG(G)676

AE19 MGTTXP0_267
AF19 MGTTXN0_267
AC18 MGTRXP0_267
AD18 MGTRXN0_267
AD16 MGTREFCLK0N_267
AC16 MGTREFCLK0P_267
AE21 MGTTXP1_267
AF21 MGTTXN1_267
AC20 MGTRXP1_267
AD20 MGTRXN1_267
AF17 MGTREFCLK1N_267
AE17 MGTREFCLK1P_267

MGTAVTTTX_267 AF20
MGTAVCCPLL0_267 AD15
MGTAVCCPLL1_267 AE16
MGTAVTTRX_267 AC19
MGTAVCC_267 AD17

BANK267

Title	FPGA BANK243 BANK267	
Size A4	Document Number <Doc>	Rev 1.0
Date: Wednesday, August 15, 2012	Sheet 14 of 20	



Title	FPGA POWER	
Size A3	Document Number <Doc>	Rev 1.0
Date: Monday, August 13, 2012	Sheet 15 of 20	

CN1のすぐ近くに設置する

ICの近くに設置する

CN1
87331-1420

U19
XCF32PFSG48C

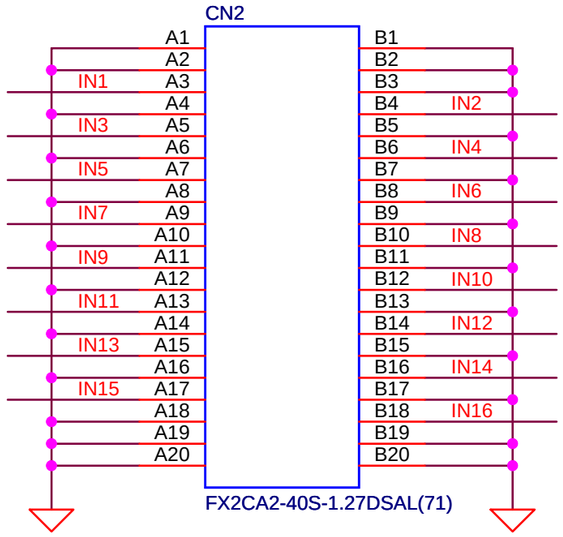
U18
LP3990MF-1.8

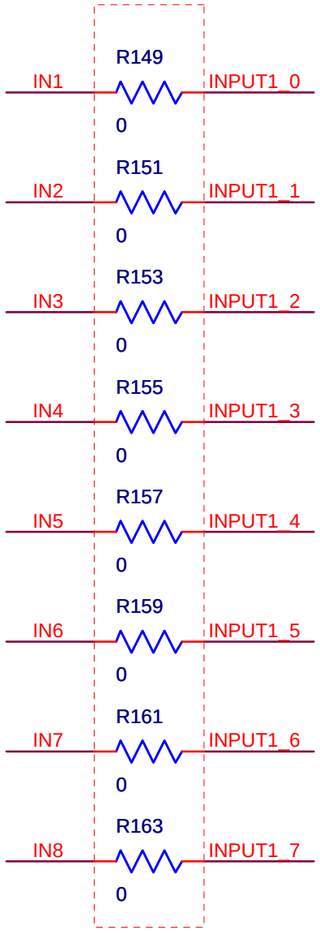
U20
M25P64-VME

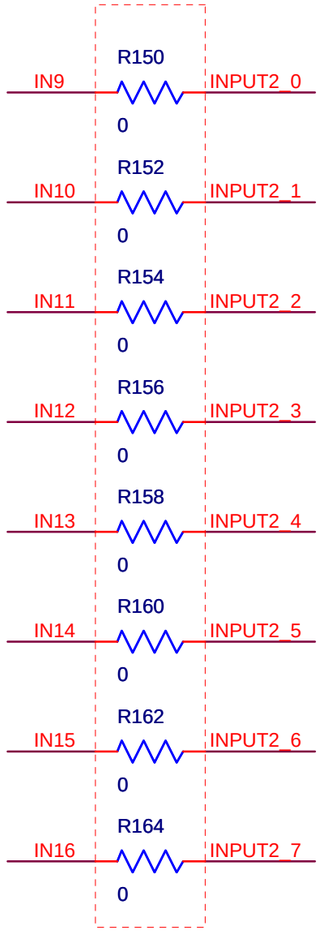
JP2 PROM
JP3 SPI

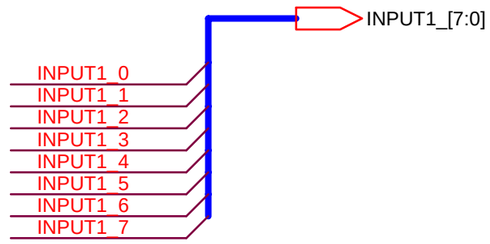
50Ω 一筆書配線

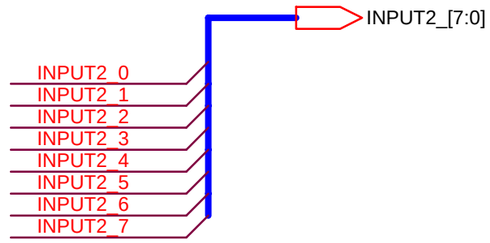
Title	PROM SPI
Size	A3
Document Number	<Doc>
Rev	1.0
Date:	Thursday, August 23, 2012
Sheet	16 of 20



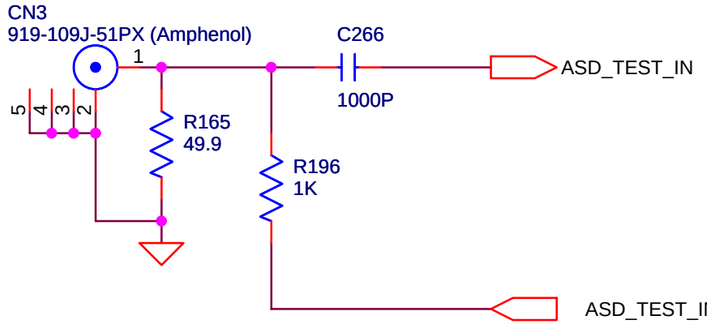




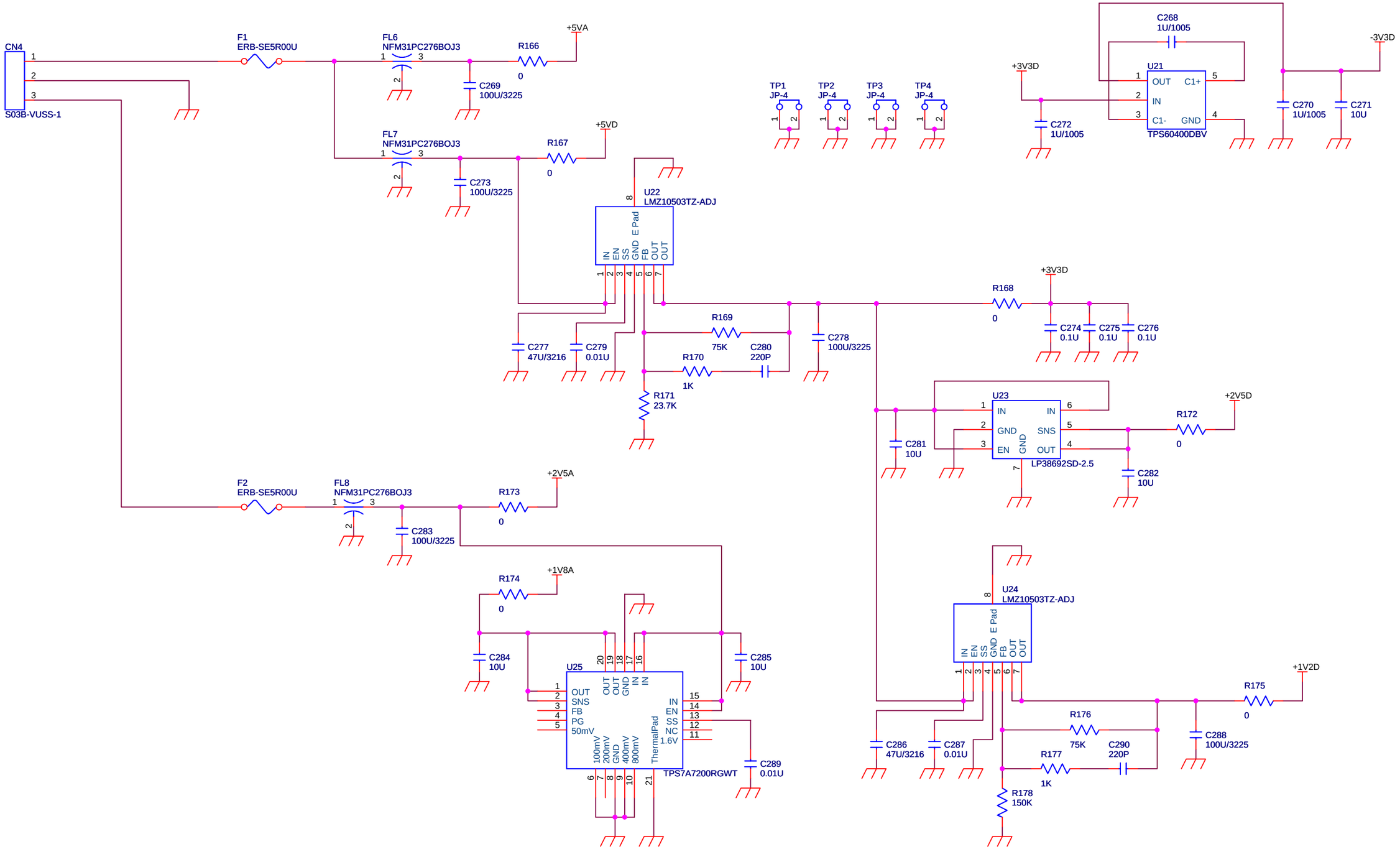




インピーダンス整合はここの抵抗で調整する



Title: Input		
Size: A4	Document Number: <Doc>	Rev: 1.0
Date: Monday, August 13, 2012	Sheet 17 of 20	



Title	Power Supply	
Size A3	Document Number <Doc>	Rev 1.0
Date: Monday, August 13, 2012	Sheet 18 of 20	

SFP_RXP[1:0]
SFP_RXP0
SFP_RXP1
SFP_RXN[1:0]
SFP_RXN0
SFP_RXN1
SFP_TXP[1:0]
SFP_TXP0
SFP_TXP1
SFP_TXN[1:0]
SFP_TXN0
SFP_TXN1

+3V3D
FL9
NFM18PS105R0J3
C291
10U
FL10
NFM18PS105R0J3
R179
4.7K
R180
4.7K
R181
4.7K
R182
4.7K
R183
4.7K
CN5
SFP_RXN0
SFP_RXP0
SFP_TXP0
SFP_TXN0
11 VEER
12 RD-
13 RD+
14 VEER
15 VCCR
16 VCCT
17 VEET
18 TD+
19 TD-
20 VEET
10 VEER
9 VEER
8 LOS
7 RATE_SELECT
6 MOD_DEF0
5 MOD_DEF1
4 MOD_DEF2
3 TX_DISABLE
2 TX_FAULT
1 VEET
74441-0001 (Molex)
C292
0.22U
C293
0.22U

J13
73927-0002 (Molex)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

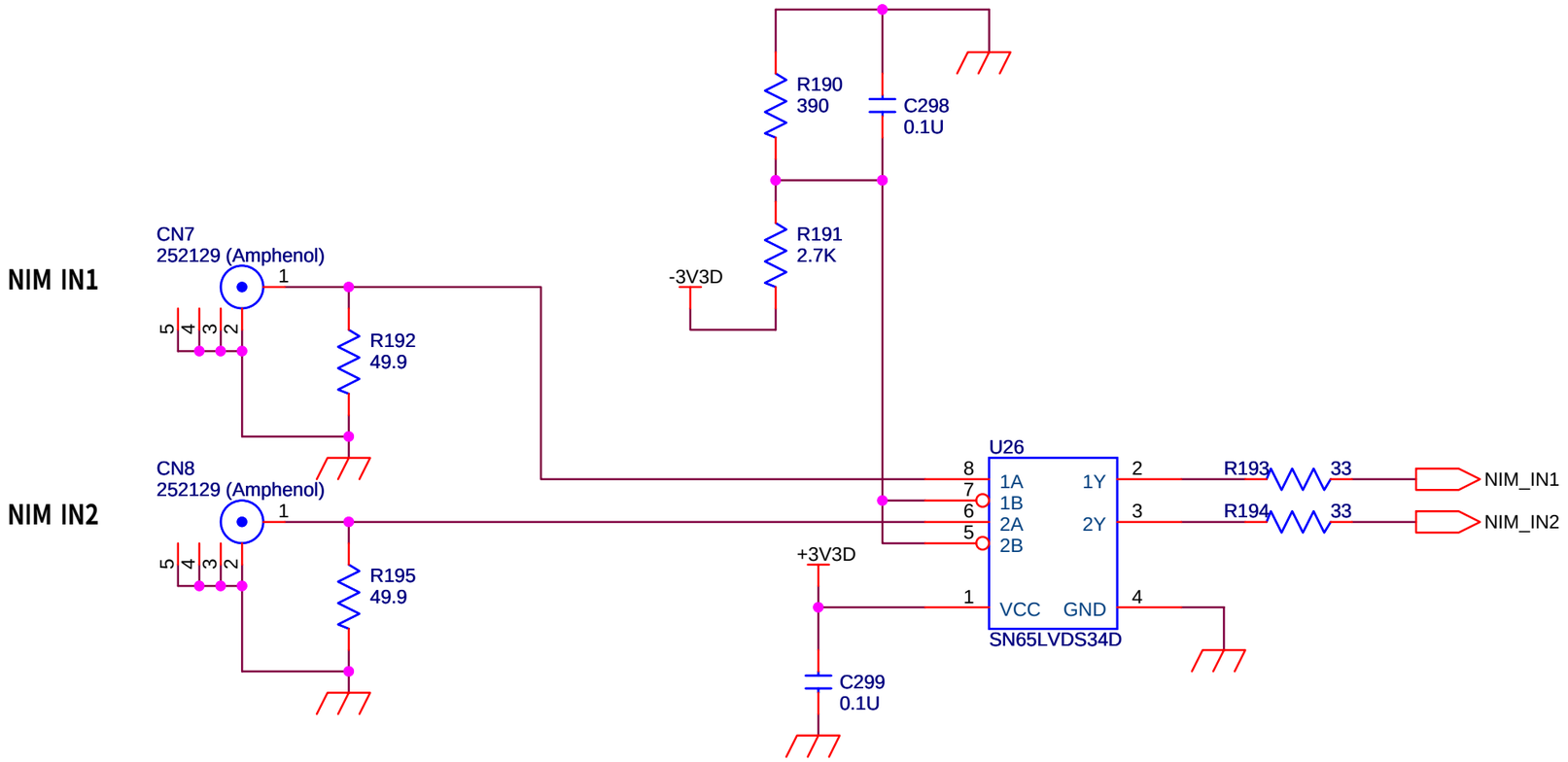
+3V3D
FL11
NFM18PS105R0J3
C294
10U
FL12
NFM18PS105R0J3
R184
4.7K
R185
4.7K
R186
4.7K
R187
4.7K
R188
4.7K
CN6
SFP_RXN1
SFP_RXP1
SFP_TXP1
SFP_TXN1
11 VEER
12 RD-
13 RD+
14 VEER
15 VCCR
16 VCCT
17 VEET
18 TD+
19 TD-
20 VEET
10 VEER
9 VEER
8 LOS
7 RATE_SELECT
6 MOD_DEF0
5 MOD_DEF1
4 MOD_DEF2
3 TX_DISABLE
2 TX_FAULT
1 VEET
74441-0001 (Molex)
C295
0.22U
C296
0.22U

J14
73927-0002 (Molex)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

+2V5D
FL13
NFM18PS105R0J3
C297
0.1U
R189
4.7K
X2
6 VCC
5 OUT
4 OUT
1 OE
2 NC
3 GND
EG-2121CA 125.0000M-LHPAB
GTP_REFCLK_N
GTP_REFCLK_P

表面で等長配線、ペア配線、最短配線
インピーダンス100Ω、ペアのPとN間の配線長差は±0.5mm

Title	SFP	
Size A3	Document Number <Doc>	Rev 1.0
Date: Monday, August 13, 2012	Sheet 19 of 20	



Title: Trigger		
Size: A4	Document Number: <Doc>	Rev: 1.0
Date: Monday, August 13, 2012	Sheet 20 of 20	