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**High-Frequency Sampling Alternative for Analyzing Circuit Failure**

**College of Engineering and Computing**

**Department of Electrical and Computer Engineering**

**ECE 449**

**Senior Design - Final Report**

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## 1 Introduction

Electronic circuits are ingrained in nearly every aspect of our lives providing us with systems such as lighting, communication, and transportation. Though this technology may increase efficiency and reduce human error, the reality is that electronics are fallible. Consequences of failed electronics can range from financial and temporal inconveniences to the extremes of injuries or loss of life. Ethical engineering practices call for designs to reflect a concern for human safety [1]. Additionally, it’s often in the best interest of companies to quickly detect and replace failing hardware to mitigate financial losses from extensive equipment downtimes. These are the motivations for our project.

The goal of our project is to establish a relatively inexpensive method to monitor a power electronic circuit’s health through the analysis of the similarity between specific measured waveforms of the circuit to the simulated waveform of a circuit’s “virtual twin” to quantifiably identify circuit failure within a given level of accuracy.

Our report begins with a discussion of previous findings in this field (Section 2, Project Background), followed by a section highlighting our research and developed theories. We then explain the experimental steps taken using a buck converter circuit as a case study, beginning with building a mathematical model of the circuit’s functionality, followed by an explanation of the simulated representation of the circuit using Matlab, and the processed results of the physical circuit (Section 3, Project Research). We then discuss some alternative data collection solutions researched and our final selection utilized to provide a basis for failure identification (Section 4, Solution Process). The report concludes with an analysis of our results and details what advancements could be made to the project in the future (Sections 5, 6, 7, and 8).

## 2 Project Background

Power electronic circuits are vital elements in industries including industrial automation, transportation, telecommunications, and power transmission. Due to their growing integration into systems, there has been much research into ensuring their health and examining their performance through a process known as condition monitoring.

Current condition monitoring methods can be sorted into three different types: degradation indicators monitoring, aging-based modeling, and software-based methods [2]. Degradation indicators monitoring and aging-based modeling consist of utilizing sensors. This type of hardware can be expensive and has its own need for maintenance and replacement after failure. This is why modern approaches often seek to fall into the third category of software-based solutions which include the virtual twin approach we utilize in our project.

Though modern condition monitoring for power converter systems can range in methods, the literature is consistent in the identification of capacitors and semiconductors as key devices to monitor for failure in power electronics hardware [2,3,4]. Failure often occurs in capacitors and semiconductor components due to their sensitivity to transient overvoltages or extreme temperatures [6]. For this project, we choose to assess a capacitor for failure due to its simplistic and passive nature. Additionally, the literature indicates that degradation indicators for electrolytic capacitors consist of a capacitor’s capacitance and resistance, as these impact the rate at which the capacitor charges and discharges [2]. This causes a change in shape and amplitude of the voltage across the capacitor.

The combination of this established knowledge in the literature led us to research the development of a software-based condition monitoring system for a buck-converter circuit. It would predict circuit failure by comparing the measured performance of the capacitor’s ripple voltage to its virtual twin values, represented by the mathematical model in [4]. In the following sections, we will develop a theory for virtual twin condition monitoring that has a balance of being simple, scalable, and inexpensive.

## 3 Project Research

Research for implementing this process falls into three main categories: understanding the selected power electronic circuit topology, implementation of a virtual twin or mathematical model of the circuit, and the process for accurately identifying whether the circuit operates without failure. We expand on our understanding of each of these concepts in the following sections with an additional section detailing any assumptions made in our report.

### 3.1 Buck Converter Circuit

In power electronics, buck converters are considered one of the simplest power electronic circuits that contain a capacitor component whose behavior can be studied. Additionally, it contains similar components to other commonly utilized power electronic circuits such as boost converters and buck-boost converters which means our research is scalable.

A DC-DC Buck converter is also known as a step-down converter because it reduces an input DC voltage to a lower DC voltage output. The topology of a buck converter can be seen below in Fig 1.

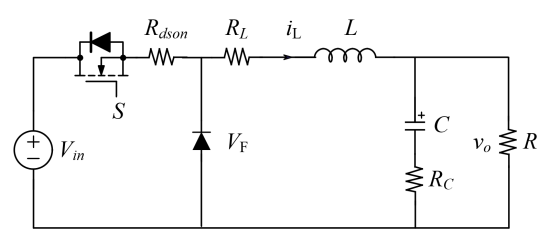


Fig. 1: Buck Converter Schematic

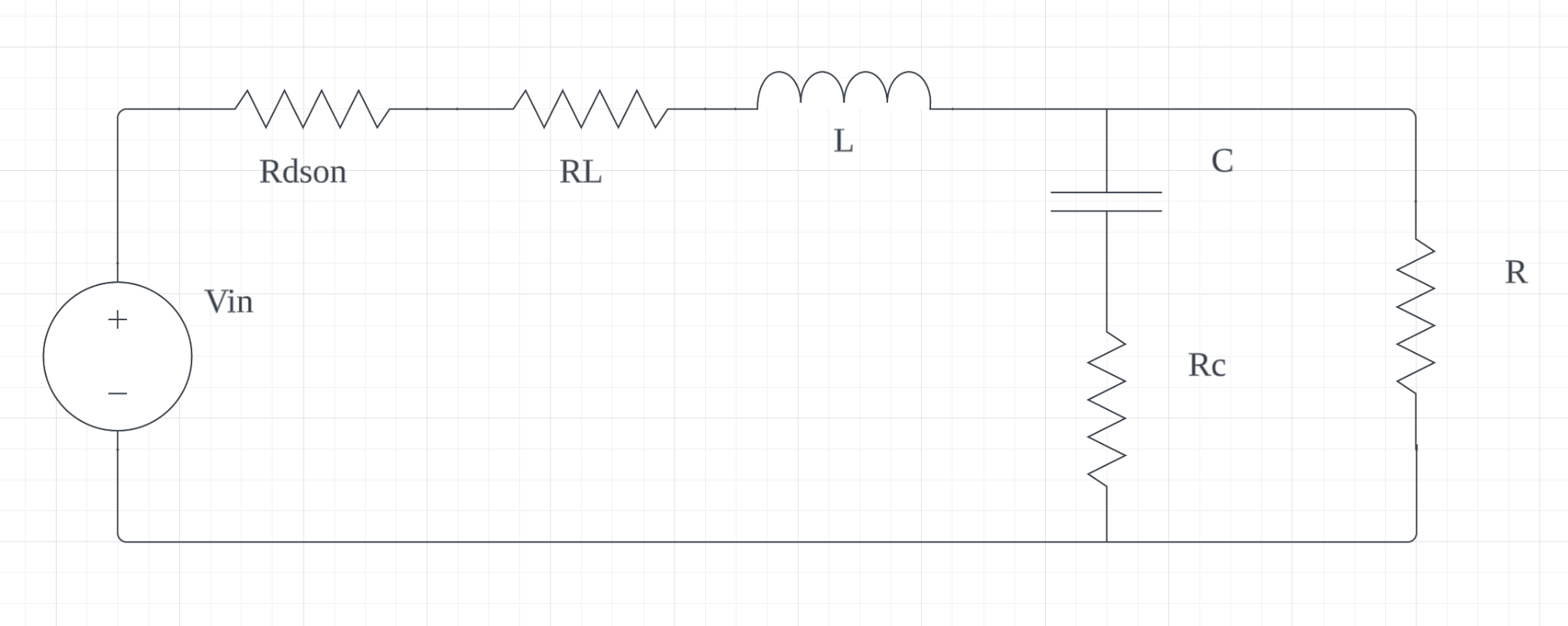
In this work, the parameters of the buck converter will be represented as follows:

* Vin is the input DC voltage value of the buck converter circuit
* is the switching state of the power semiconductor device (1 represents an “on” state, 0 represents an “off” state)
* is the internal resistance of the semiconductor device when it is on
* is the forward voltage of the diode
* is the internal resistance of the inductor, also known as equivalent series resistance (ESR) which has an inductance
* is the ESR of the capacitor which has a capacitance
* is the resistance of the load resistor in parallel with the capacitor whose response we will be focusing on during this report.
* Vo is the output voltage across the load resistor

In our test setup, the input Vin is a variable power supply set to 24 V. The duty cycle (*D*) represents the ratio of the amount of time the switch is on (tSon) to the total time of one period of the switching operation (TS). It determines the percentage of the input voltage that will be output by the circuit:

. (1)

Pulse width modulation (PWM) is the technical term for this voltage regulation method using the duty cycle. Under this operation, the buck converter has two states in which it performs: the “on” state and the “off” state. During the “on” state the circuit appears as seen below in Fig 2. The switch (S) is closed and the input voltage flows through the inductor to reach both the capacitor and load resistor. During this state, the diode is reverse-biased and acts as an inductor which allows the current to charge the capacitor.

Fig. 2: The Schematic of a Buck Converter During the“on” State

During the “off” state seen in Fig 3, the switch is opened and the input voltage is no longer provided to the circuit. At this time, the inductor releases its stored energy forcing current to flow through the load resistor and through the diode which is now in forward-bias mode. The capacitor begins to discharge and provides additional current to the load resistor [6].

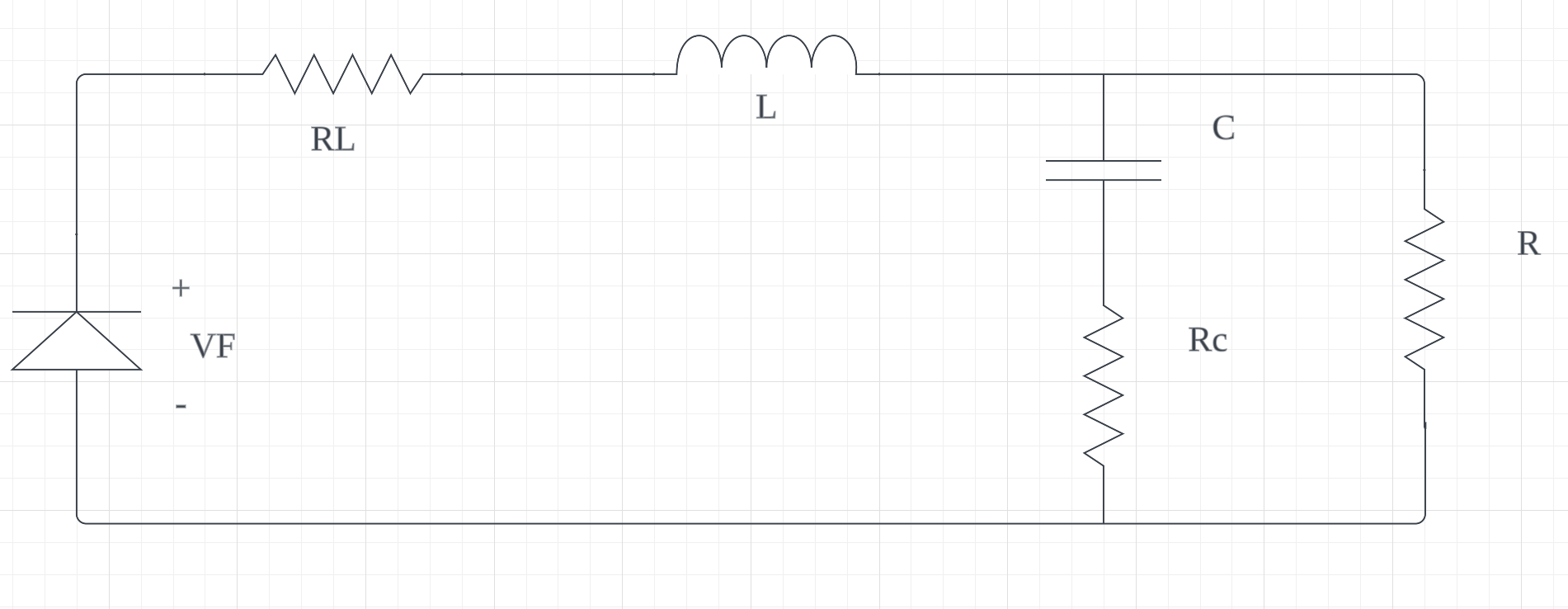


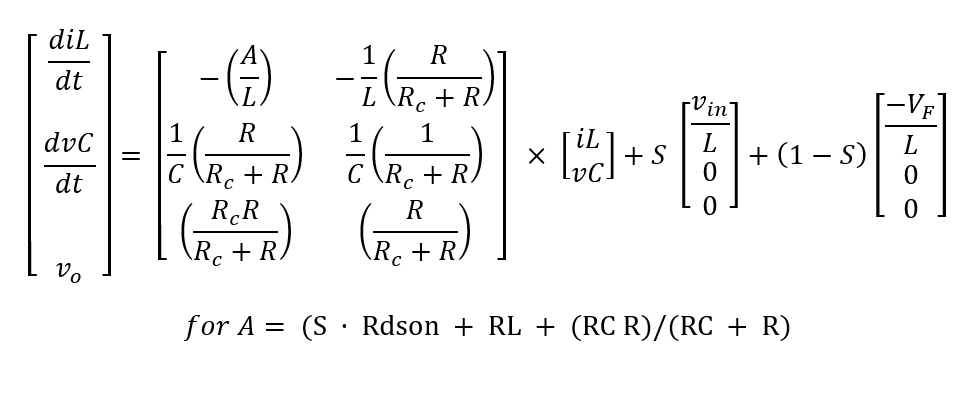
Fig. 3: Buck Converter “off” State

With an understanding of how the circuit operates, we noted key values of the current operation of the circuit such as , (switching frequncy), , and before exporting the data to take the next step of modeling an accurate digital twin. Relevant measurements for the circuit appear in Table 1.

Table 1: Physical Buck Converter Values

| Component |  |  |  |  |
| --- | --- | --- | --- | --- |
| Value | 24 V | 50 kHz | 0.5 | 11.4 V |

### 3.2 Virtual Twin

The goal of a virtual twin is to replicate the behavior of a physical system with a simulation. To predict circuit failure, we need a baseline for the ideal operation of the circuit to compare the sampled circuit data. For this reason, we need a reasonably accurate mathematical model of a buck converter using PWM voltage regulation. During the process of making our digital twin, we learned that it’s essential to model the PWM aspect of the circuit. Without the PWM switching frequency, the results would be an “averaged model” and the output ripple we want to analyze can not be seen. We used the state space representation from [4] to accurately model our buck converter. This work gives the equation below:



Due to the frequent need for matrix mathematical operation, we found it easiest to build a digital model in Matlab. It could then be transferred to other programming languages as needed. We have provided a link to our GitHub page with the created code which can also be found at the end of this report in the Appendix.

Link to our Project GitHub: <https://github.com/Epsilon391/High-Frequency-Sampling-for-Circuit-Analysis>

The parameter values for ideal operation conditions utilized in our virtual twin were selected based on the certain values we set in our physical circuit seen in Table 1 as well as datasheet information for components. The final variable values utilized in the simulation are listed below in Table 2.

Table 2: Digital Twin Buck Converter Variable Values

| Variable |  |  |  | L | C |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Value | 24 V | 0.1 Ω | 0.2 Ω | 0.001 H | 680 µF | 0.1366 Ω | 0.7 V | 10.9 Ω | 50 kHz | 0.5 |

The simulation developed is executed for 0.1 second and the rate of the simulated data is to be 10 ns, as this is the sampling rate of the MSO4034 oscilloscope we utilized to collect and store data from the physical circuit. An array representing the time values of each data point uses this runtime and time step. The values of this time array are utilized in the conditional statement in Equation 3 to create a logical array that models the switch state (1 for “on”, 0 for “off”) for each recorded moment in time given the switching period (TSW) and the duty cycle.

(t mod TSW) > (TSW \* Duty Cycle). (3)

Arrays on lines 30 and 31 of Fig. 4 are used to store the results of the simulation and a for loop on line 33 of Fig. 4 is used to calculate the values of the state variables at each time step. In each iteration of the loop, the established parameters and state of the switch in the current point of time in the simulation are entered into the state space equations to generate the change of inductor current, capacitor voltage, and output voltage across the load resistor. These values are used to generate the actual inductor current and capacitor voltage values at each time step and added to the previous iteration value to construct a simulation of the output voltage at each time. At the end of the loop on line 45 in Fig. 4, an array of the simulated output voltage values is created.

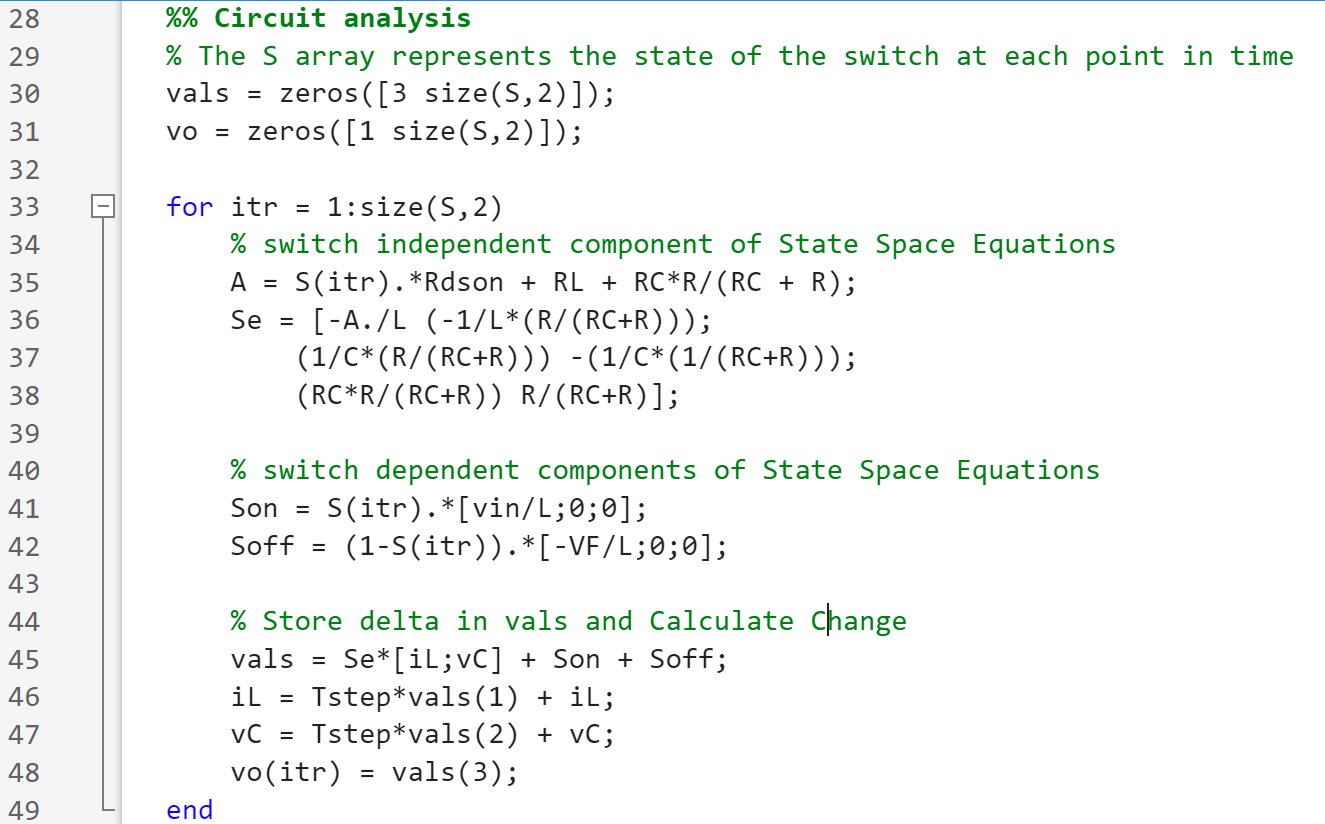


Fig. 4: MATLAB Code for State Space Equation Buck Converter Model

We selected this approach because it enabled us to create more accurate simulation results, unlike other approaches that model a wide variety of circuits in programs like LTSpice where we produced less accurate results. It is important to note that this process is still scalable for other power converters and is suggested for complex linear time-invariant systems. We discuss our approach to analyzing our real and simulated data in Section 5, Results.

### 3.3 Signal Processing Circuit

Fig 5 shows the results of the output signal of the buck converter that we plan to sample as measured by our MSO4034 oscilloscope. The peaks of the signal are noisy, even when measured with our relatively high-end oscilloscope. This is mainly due to the large DC offset in combination with the low voltage ripple amplitude of approximately 150 mV. To make the sampling process easier, we constructed a circuit containing a high-pass filter and amplifier (Fig 6) to process the data before sending it to an ADC.

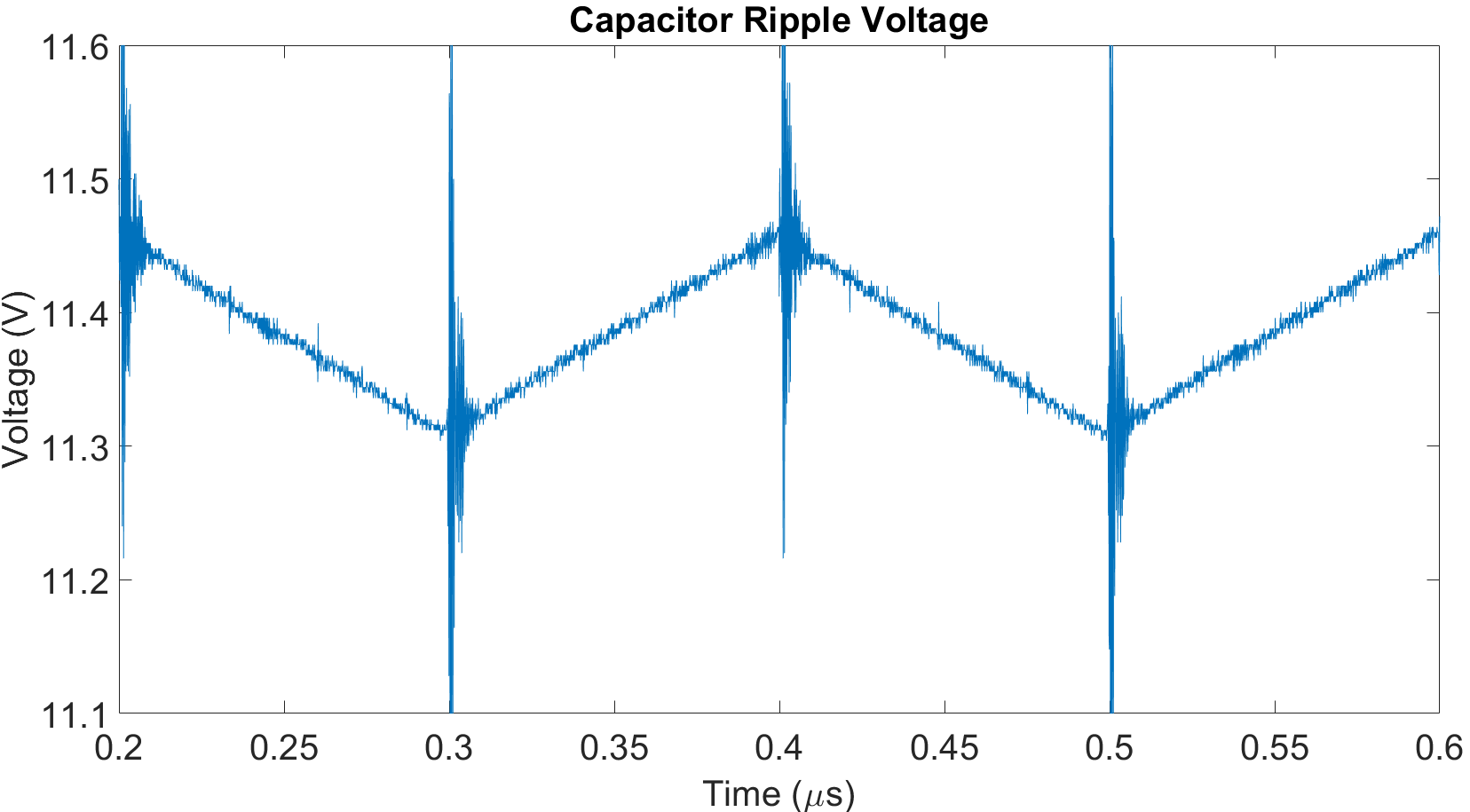


Fig. 5: MATLAB plot of the voltage across the buck converter output at steady state.

Our selected process of capacitor degradation identification, further discussed in the final results section of the report, is only reliant on the shape and magnitude of the voltage ripple, which means the DC offset can be eliminated using a high pass filter. This is done with 20 nF capacitor and a 10 kΩ resistor, yielding a cutoff frequency of 800 Hz. Now that the ripple has been separated, the signal ranges between ±75 mV. A 40 % increase in the ESR of the capacitor would cause the peaks to increase by about 50 mV. As changes on the order of a few millivolts are susceptible to noise, we concluded that the signal needed to first be amplified. Our amplifier of choice is the AD620 IA instrumentation amplifier [7]. It is built specifically for amplifying millivolts or microvolts AC inputs, and it has a 120 Hz bandwidth (a potential alternative for a 120 kHz+ system is the LTC6244). The successful circuit setup for our high pass amplifier circuit as well as the resulting amplified signal is shown in Fig 6.

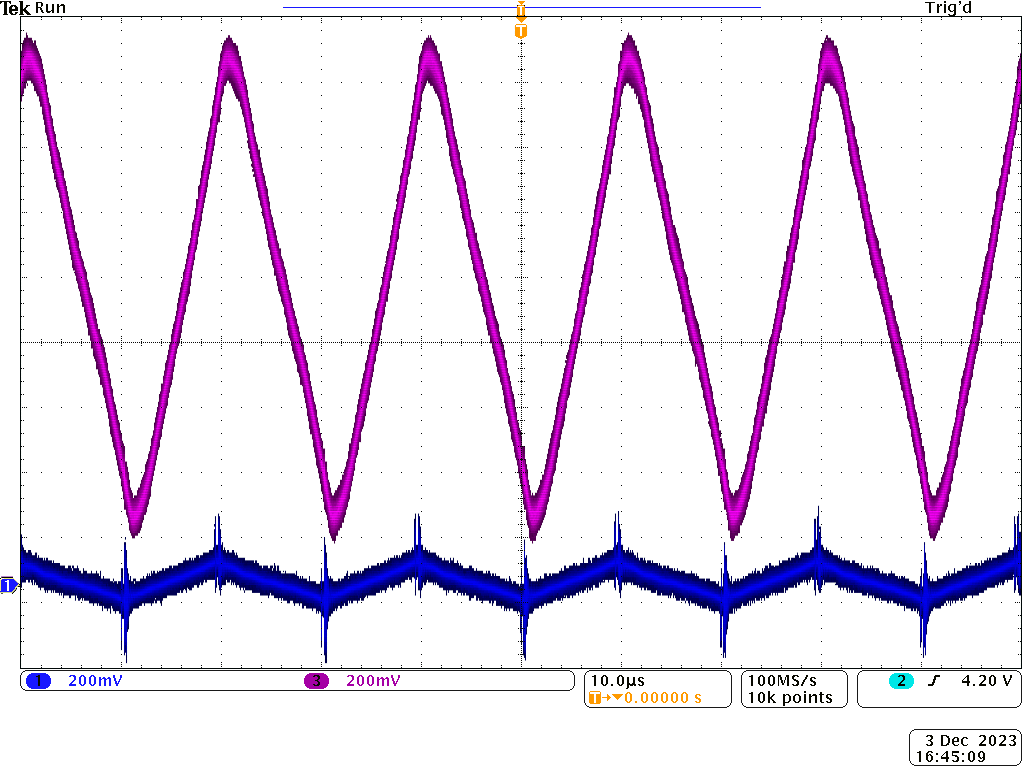


Fig. 6: Signal Processing Circuit (left) and the Corresponding Output Signal (right). The blue waveform is the output of the high pass filter, and the purple waveform is the output of the amplifier.

### 3.4 Assumptions

Environmental conditions can be critical factors in the performance of electrical components and circuits. Conditions that often decrease the reliability of a circuit include temperature, vibration, humidity, dust, pressure, and radiation. For this work, the previously defined buck converter was assumed to operate in normal environmental conditions. We assume that the converter is appropriately enclosed and shielded to mitigate damages from dust, humidity, and extreme vibrations.

The environmental condition whose impact we consider most in our experiment is temperature. We specifically selected this condition to study due to its critical impact of increased acceleration of electrolytic capacitor lifetime. Both ambient and internal temperatures of the capacitor can speed up the degradation process. As these temperatures increase in electrolytic capacitors such as the EEUFC2A681 [8] in our buck converter circuit, and other power converter applications the electrolyte evaporates through the seal, and leakage increases. This results in a higher ESR and decreased capacitance. Since the temperature heavily impacts these two properties, we plan to use them to predict failure by real-time comparisons between collected and simulated ideal data. The impacts stated can be seen by simulated data in our results section.

## 

## 4 Solution Process

### 4.1 Alternative Designs

As our group researched capacitor degradation our strategies took two specific directions. The first direction focused on measuring the decreasing capacitance. Decreased capacitance is indicated by a change in the shape of the waveform. Specifically, the rising edge of the waveform becomes more concave as capacitance decreases. The second direction we examined was to exclusively focus on the rising amplitude of our waveform due to an increased ESR when the capacitor degrades. Both of these approaches are practical for detecting a failing capacitor. This similarity is discussed further in the final results section. We are pursuing the more complicated of the two approaches: consider both shape and amplitude. We made this decision to allow for scalability and it is theoretically achievable in our time frame. In the process of deciding to measure shape, we experimented with alternative circuit sampling solutions. These potential solutions included a peak detection circuit, an ADC integrated with an FPGA, and a statistical peak detection program utilizing a Raspberry Pi.

#### 4.1.a Peak Detection Circuit

Peak detection circuits are utilized to find the average maximum output of an AC signal. The circuit processes the signal through a diode and capacitor which are connected in series. The ideal output of this circuit is a stable DC signal equal to the peak value of the AC signal. This solution can be used to detect if there is an increase in the amplitude of the waveform. Regarding capacitors, this would indicate an increase in internal resistance and decay. This situation would be beneficial because the output is a DC voltage and it can be measured by an ADC with a low sampling rate. Because of the simplicity behind this circuit, we would opt to use this solution if we did not have the goal of measuring shape.

#### 4.1.b FPGA ADC SPI

Creating an embedded system using an FPGA and then interfacing with an ADC would provide the most agility out of all of these solutions. This is due to the low-level language an FPGA is programmed with. This low-level language would also be the most complicated to build our simulation in. This assumption combined with the fact that we would need to build the SPI between the ADC and the FPGA was enough reason for our group to eliminate this solution based on time constraints.

#### 4.1.c Raspberry Pi

Our group came up with three potential solutions utilizing the GPIO pins on a Raspberry Pi. The first solution was to use the Raspberry Pi as our embedded system in conjunction with the peak detector circuit sampling process. This solution is, again, theoretically the most simple for detecting capacitor decay. However, this was not selected for the same reasons stated above. The second solution was also for measuring amplitude and not shape. This solution involved using the ADC on the Raspberry Pi which has a sampling rate that is too slow to sample the waveform precisely. The untested theory behind this solution was that the slow ADC could still be used to intermittently sample the circuit voltage. Then a simple statistical model in Python could be used to determine the peak voltage of the collection of the intermittent data points without registering noise. The third potential Raspberry Pi solution also involved the onboard ADC. The concept behind this solution was that if the period of the signal was known it could be used to calculate the waveform from the intermittent sampling. As the sampling program is running it would calculate the difference in time between the first sample and each following sample. Then after collecting several samples the period of the waveform and ∆t at each point could be utilized to reconstruct the signal. This idea would be beneficial because it would reduce the amount of physical components used to construct the virtual twin. We decided to avoid this solution after developing a simulation to test this theory. The simulation demonstrated that the period used for calculation needed to be very precise. Far more precise than we believed we would be able to achieve. The program indicated that the signal could be easily miscalculated if the period was off by a fraction. This problem is the reason we settled on the following solution.

### 4.2 Final Design

After constructing the signal processing circuit we needed to select an ADC to sample the 0-2V, 50kHz signal at a sampling rate high enough to capture the shape of the waveform. During discussions, we agreed that a minimum target sampling rate of 500 kHz would be sufficient, but 1 MHz+ was desired. Additionally, capacitor failure causes changes on the order of 5 millivolts. Since the gain is around 13x, our ADC needed to differentiate between 66 millivolt intervals. During research, we found a project that uses a blue pill board to create a simple oscilloscope capable of exporting waveform data as a CSV file. The board uses an STM32F103C8T6 microcontroller that has two built-in ADCs.

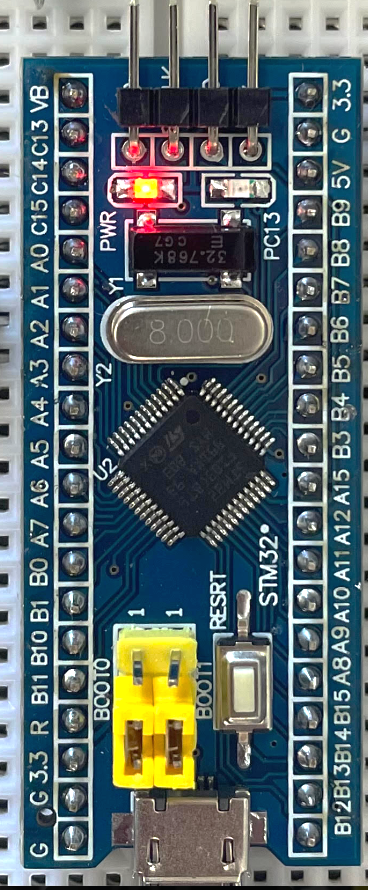
 

Fig. 7: STM32 Bluepill Development Board & STLink

The important parts of the chip are its ADC, DMA, and UART. The ADC can be clocked at a maximum of 14MHz, and it has a resolution of 12 bits with a voltage range of ±3.3V. This yields a resolution of 1.6 millivolts. Additionally, this board contained a 7-channel DMA controller capable of operating with peripherals such as the ADCs and UART. DMA or direct memory access is a separate controller from the CPU that handles data transfers without overwhelming the CPU with commands. We chose to set up this peripheral in our code to send data between our collected ADC values and UART transfer due to the high volume of data continuously being sent to the Raspberry Pi using UART.

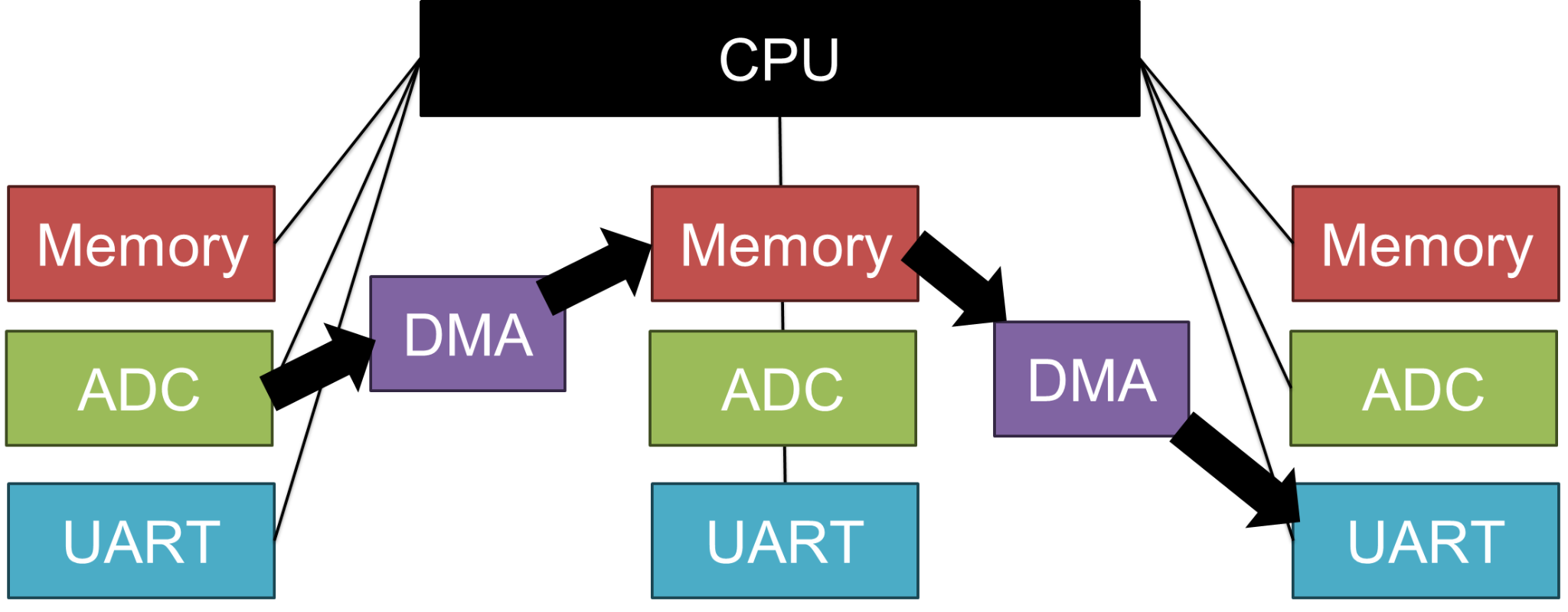


Fig. 8: ADC, DMA, UART System Diagram

To program the development board the STM32 Cube IDE can be downloaded from the STM32 website and utilized to upload C code to the board using an STLink connection shown in Fig. 7 to upload code from a USB port on a computer.

Overall, the STM32 is a good choice for a range of systems. We selected the blue pill board, as it is one of the cheaper implementations of the STM32 processor at around $8, additionally, it operates at 72MHz and can send data via UART. Exporting the data allows us to use a Raspberry Pi to compare the measured and ideal waveforms. Due to these factors, we selected this board as our final solution for our ADC and embedded system solution.

## 5 Results

### 5.1 Simulation vs Tektronix MSO 4034 Collected Data

Data for the capacitor ripple voltage was collected from measurements across the load resistor of the buck converter circuit for 10,000 data points and 5 switching periods using our oscilloscope. This was graphed in conjunction with simulated data to analyze the accuracy of the simulation data in modeling the buck converter circuit. As seen by the results in Fig 9 the simulated results closely model the results of the buck converter data.

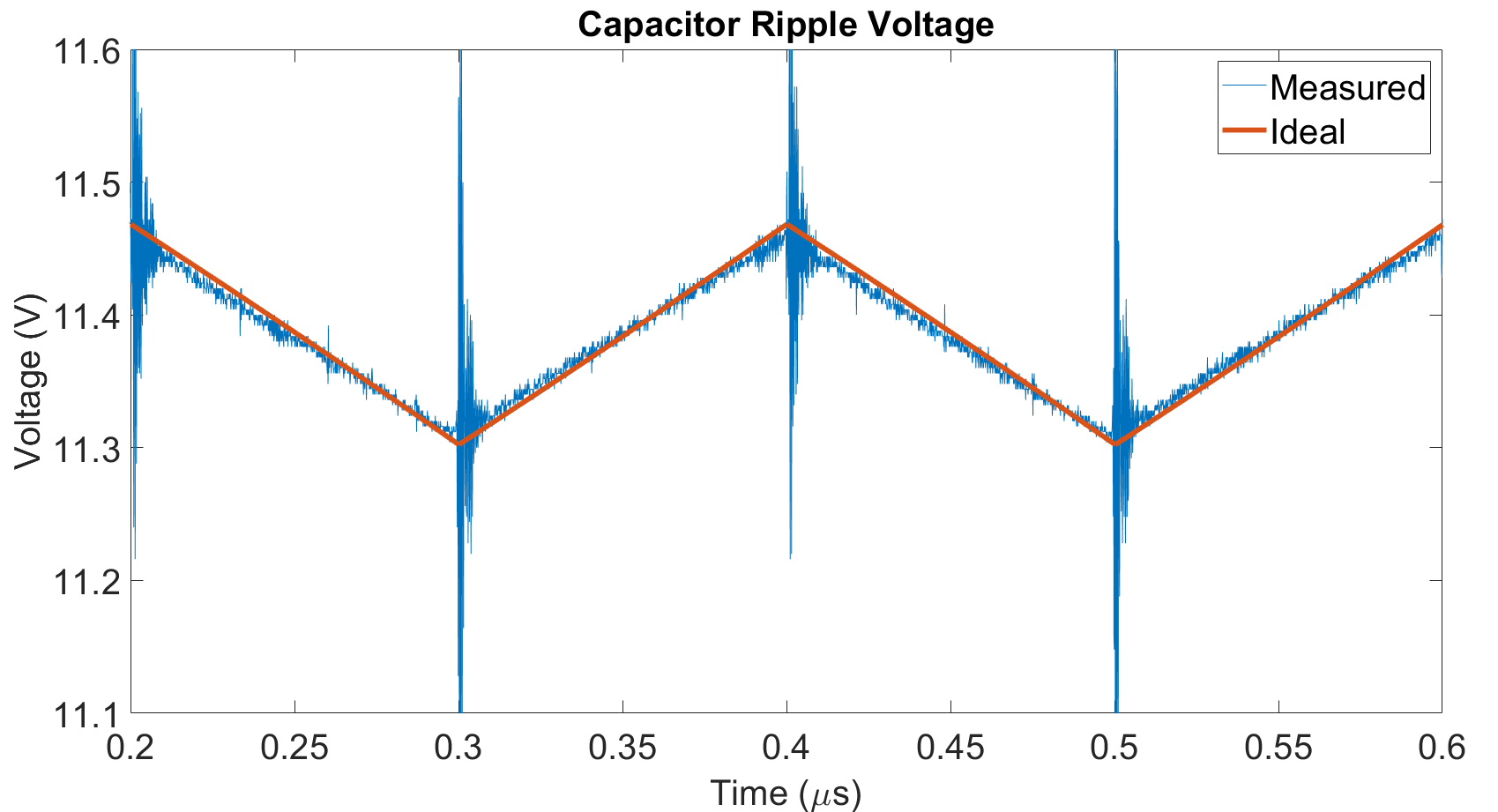


Fig. 9: Comparison of Simulated and Measured Buck Converter Data

In addition to modeling the ideal performance of the buck converter, we found that changes to capacitor properties RC and C correctly reflect the changes that would take place in real-world capacitor degradation. We tested the data at increases of ESR between 20 % and 40 % and decreases of capacitance between 5 % and 20 % based on the claim that these are reasonable percentages of failure [3].

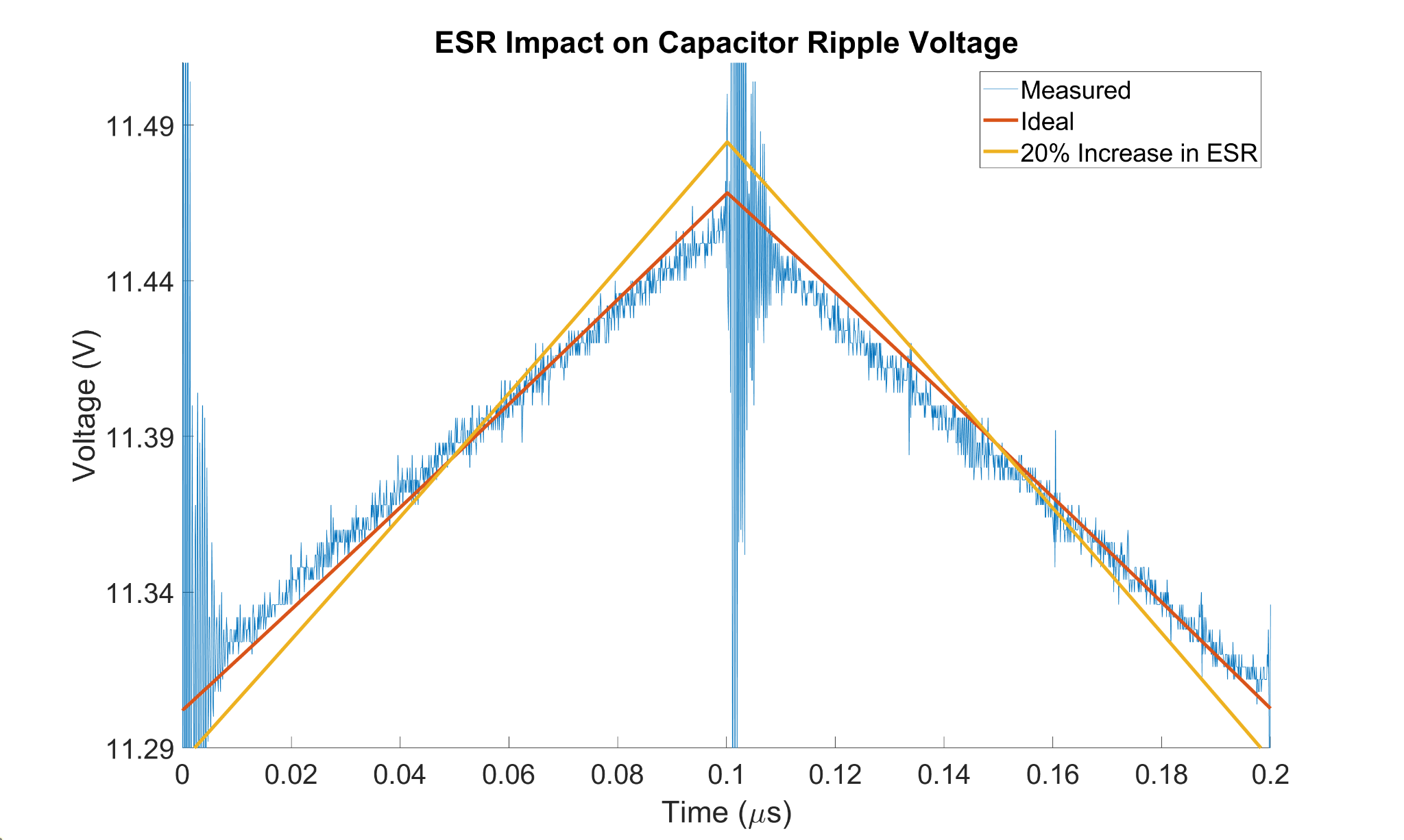
Figs 10 and 11 show the simulated results of the capacitor ripple response from increasing the ESR and decreasing the capacitance values of the capacitor. As the capacitor ripple was modeled from its ideal values to a 20% increase of ESR the peak capacitor ripple voltage increased and the ripple became very distinct from its ideal waveform. This change was clear using the lowest value of the ESR percentage increase range, however, the change in the waveform due to capacitance decreases was less noticeable graphically in the 5-15 % range which is why Fig 11 shows the results for a 90 % decrease in capacitance. At this degradation value, there is a noticeable change in the shape of the simulated data compared to the ideal simulation. 

Fig. 10: Impact of ESR on Capacitor Ripple Voltage

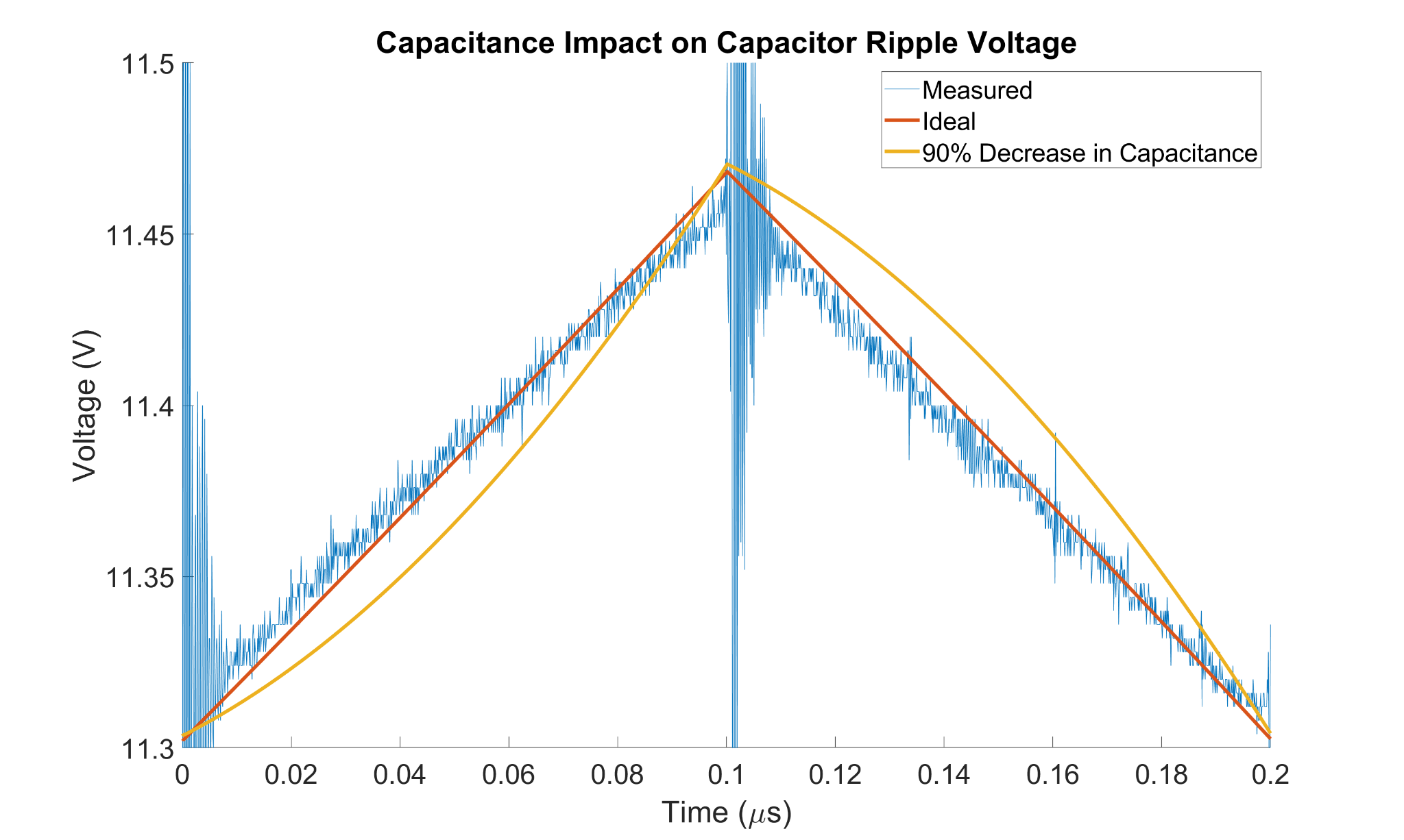


Fig. 11: Impact of Capacitance on Capacitor Ripple Voltage

These results indicate that our state space construction of a digital twin will be accurate enough to the real-world capacitor ripple voltage for our purposes of identifying capacitor degradation. As a capacitor degrades over time, changes in its ripple shape and more critically its peak value data can be collected with our selected ADC and embedded system and compared with the results of our digital twin to identify and predict failure.

### 5.2 Simulation vs STM32 Collected Data

Data for the capacitor ripple voltage was collected from measurements across the load resistor of the buck converter circuit for 20 total data points and 2 switching periods using our sampling circuit and the STM32 ADC. This ADC data was sent to the Raspberry Pi using UART and a Python script created a CSV file containing the received points. These points were graphed in conjunction with simulated data to analyze the accuracy of our collection method compared to the simulation data. As seen by the results in Fig 12 the collection method closely follows the peak values of the simulated data and the shape is similar to that of the simulated data.

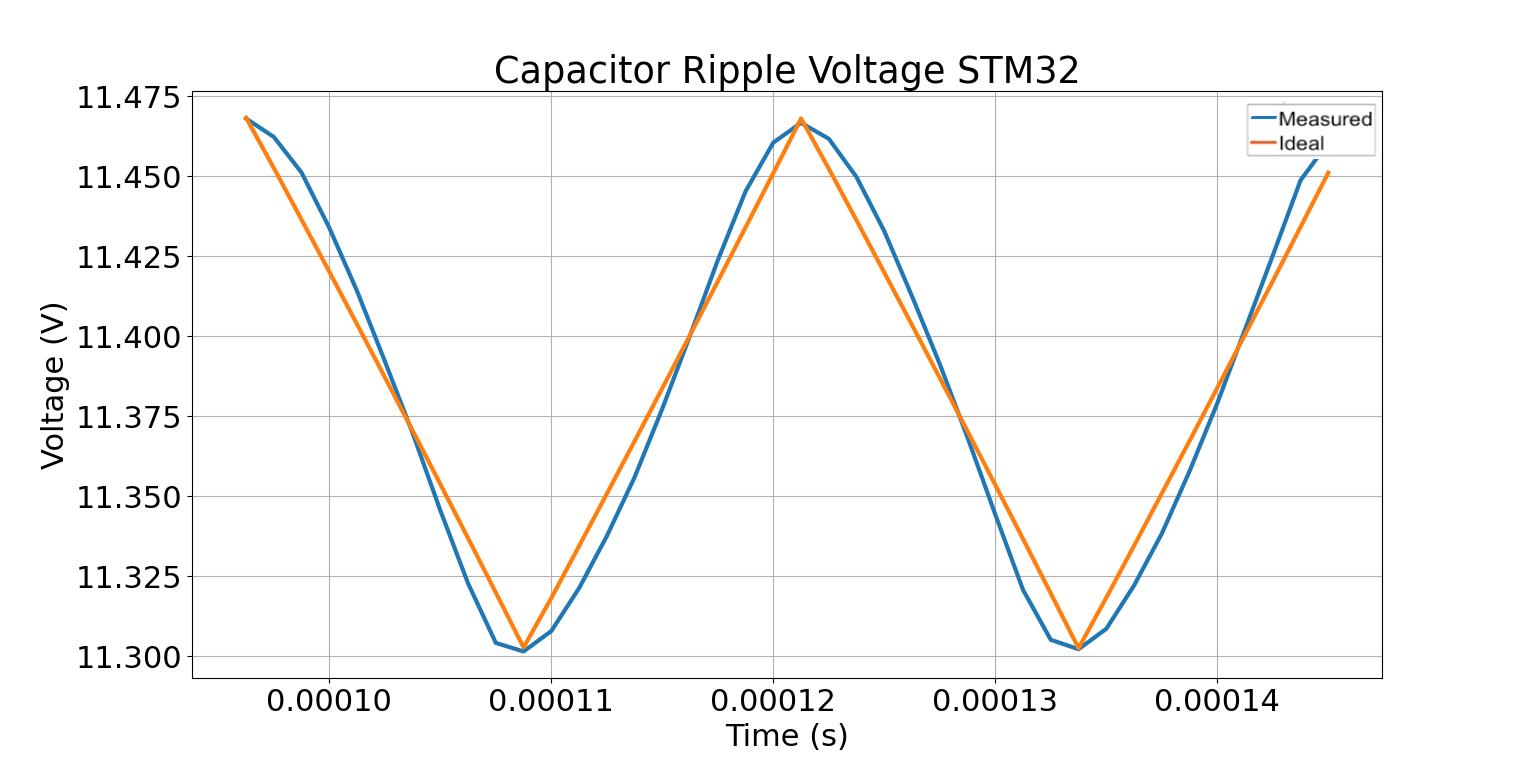


Fig. 12: Comparison of Simulated and Collected Buck Converter Data from the STM32

Additionally, tests were performed with different load values to ascertain the consistency of our design for separate load resistance values. As seen in Fig. 13, results show that our designed data collection method works for both a load of 5 ohms as well as 30 ohms.

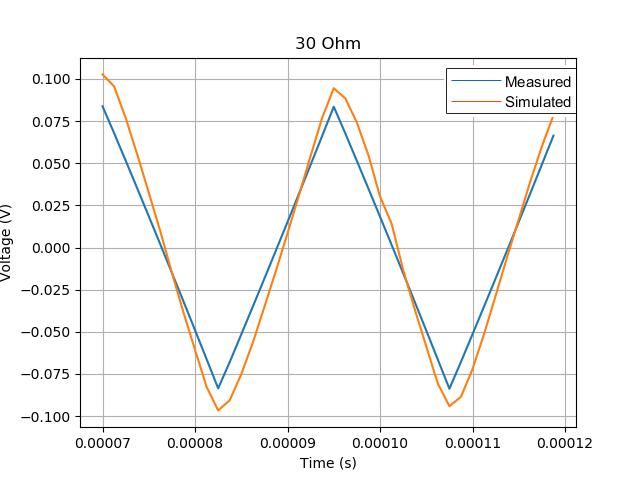
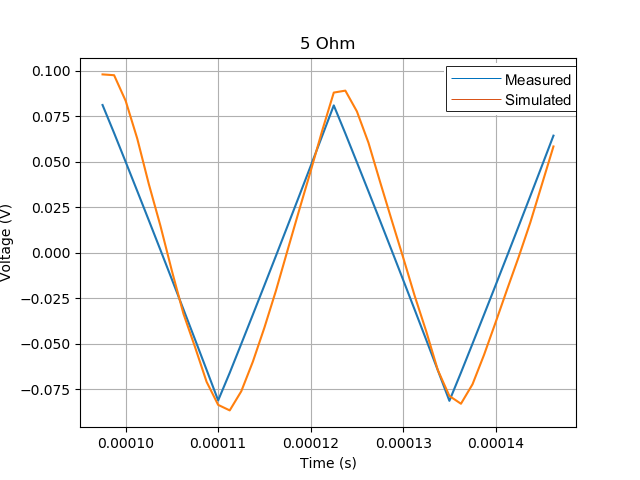


Fig. 13: Simulation vs Experimental Results at 5 Ohm and 30 Ohm Load

We believe that due to the similar nature of the peak failure due to increasing ESR could quantifiably be identified, however, the shape of the data would need to be slightly more accurate to be able to identify the failure due to decreasing capacitance. It is for this reason that future work should be completed to increase the accuracy of the collected data, though the data collection method of the STM32 blue pill does work and could be sufficient depending on the application with consideration of the cost vs accuracy tradeoffs.

## 6 Future Work

Our design of a sampling circuit that can collect data from high-frequency devices provides a lot of potential for future work in developing a method for identifying failure using this data. Based on the knowledge our team has gathered over a year, we believe the project could be bettered in three distinct ways: ADC optimization, statistical analysis of the waveforms, and cleaner design.

Currently, the code developed by our team uses a singular ADC operating at 14 Mhz clock speed. This allows us to send 10 data values per period for a 50 kHz signal (1 Msps). The resulting shape is similar to that of our simulated version, but we believe that by utilizing both ADCs on the STM32, code could be developed to use both ADCs with offsets from one another to double the data points collected. We believe that 20 data points could create more accuracy in the shape of the waveform and make analyzing the waveform for failure easier.

Secondly, due to difficulties programming our hardware during the semester, we were unable to compare the sampled waveform to its digital counterpart and quantifiably assign the possibility of failure for the capacitor based on the statistical similarity of the waveforms. A comparison method can begin development without needing to develop the circuit sampling portion of the problem. We believe the simulated and measured waveforms could be compared using a distance metric algorithm. Several distance metric algorithms exist, such as the Euclidean, Manhattan, and Minkowski distance metrics. Studying these and possibly other methods could help identify failure. A special focus should be placed on the relationship between the peak values of the capacitor ripple to identify failure due to increasing ESR being a very clear indicator with a relationship to the likelihood a capacitor will fail. Another approach is using machine learning to determine how the simulation parameters need to change in order to replicate the measured waveform. The new parameters should produce an accurate capacitance and ESR, which can be compared with the ideal to determine where the capacitor is in its lifetime.

Other tasks include bettering our signal processing design by transferring it to a PCB to increase the reliability of the circuit, as well as creating more permanent connections to the Blue Pill and Raspberry Pi to reduce the chances of failure due to poor connections.

## 7 Team Reflection

The research and implementation of our virtual twin project took us through multiple paths over the past year. It was evident that for an involved and complex project such as this and the many projects in our future, we must engage in lifelong learning. To assume that our current knowledge is sufficient introduces limitations and inhibits a project’s natural ability to progress. We must be mindful of this so that we don’t just create products that work, but rather that we design ones that efficiently utilize resources to better meet the diverse needs of the people in our world.

This is the benefit of our liberal education: to broaden our horizons to comprehend the diverse facets of our world so that we can design solutions that meet the changing needs of our world. While our engineering education was imperative to the progress accomplished, it could be argued that the skills we’ve gained in our other studies motivated us to see this project through, by understanding the universal benefits of finding a simple, scalable, and inexpensive solution to this problem that can benefit society and save lives.

## 8 Conclusion

In this report, we highlight the benefits of a virtual twin health monitoring approach to predict circuit failure by monitoring the performance of the output of a buck converter. We compiled significant findings about the literature surrounding this subject and built the foundation of our approach including our supporting research and assumptions made during the process. We then gave detailed explanations about the theorized ADC and embedded systems solutions to test our virtual twin and gave sufficient support as to why we settled on the black pill board as meeting our requirements. Additionally, results for the simulated digital twin were produced and utilized to support the conclusions that our digital twin successfully modeled the performance of a buck converter’s capacitor and that this model will be accurate enough to predict failure in the future. We concluded with descriptions of the future work to be performed for this project and reflected on the importance of this project to our present and future careers as engineers.

## 

## 9 Appendix

### 9.1 References

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### 9.2 Code

Link to our Project GitHub: https://github.com/Epsilon391/High-Frequency-Sampling-for-Circuit-Analysis