

Analog IC Design: Project - Part 2

Spring 2018

Contents

1	Objective	2
1.1	Primary Tasks	2
1.2	Circuit Requirements	2
1.3	Custom MOSFETS	2
1.3.1	Problems Encountered	3
2	Initial Circuit	3
3	Double ended Cascoded Amplifier	4
3.1	Gain Equation	4
3.2	Calculating Drain Current I_d	5
3.3	Finding Biasing Voltage	5
3.4	Calculating R_D	5
3.5	Current Source $\frac{W}{L}$	6
3.6	Circuit Design	6
4	Single-Ended Output	9
5	Conclusion	11

1 Objective

In part 1 of this project we designed a Operational-Amplifier from scratch. This was done by following a step by step incremental process. This allows for the understanding of each component of the circuit before moving forward to more complicated steps. In continuation of that theme we are going to take that previously constructed circuit and cascade it to increase its overall gain. After that is accomplished we will then attempt to cascade it again but with a single ended output.

1.1 Primary Tasks

The purpose of this project can be simplified into to primary tasks as given.

1. Determining the biasing circuit configuration
2. Designing/calculate all the MOSFETs parameters to achieve the desired amplifier specifications.

1.2 Circuit Requirements

The following are given circuit requirements that will be adhered to.

1. Do whatever modifications necessary to your circuit in the first part to cascode the differential stage, as shown in figure 9.13(a) in the textbook.
2. The new differential gain should be equal to 104 (with a tolerance of no more than 20%, but the gain should be at least 104)
3. Allowed 1 resistor (to be placed outside the IC), any number of n-type and p-type enhancement mode MOSFETS.
4. Allowed a maximum of 2 power supplies (excluding the test input signal source of course)
5. λ for all MOSFETS should be at least 0.02
6. W and L should be at least 1m (assuming a 1m technology).

1.3 Custom MOSFETS

We will be using the MOSFETs that were designated in part one of the project. They are as follows

- NMOS

```
.SUBCKT enmos001 1 2 3
```

```
M 1 2 3 3 enmos001
```

```
.MODEL enmos001 NMOS (KP = 500E-6 VTO = 1 LAMBDA = 0.02 W=2u L=1u)
```

```
.ENDS enmos001
```

- PMOS

```
.SUBCKT enmos002 1 2 3
```

```
M 1 2 3 3 enmos002
```

```
.MODEL enmos002 PMOS (KP = 500E-6 VTO = 1 LAMBDA = 0.02 W=2u L=1u)
```

```
.ENDS enmos002
```

Using Multisim's component wizard we can import this settings and create custom MOSFETs for use in our simulation.

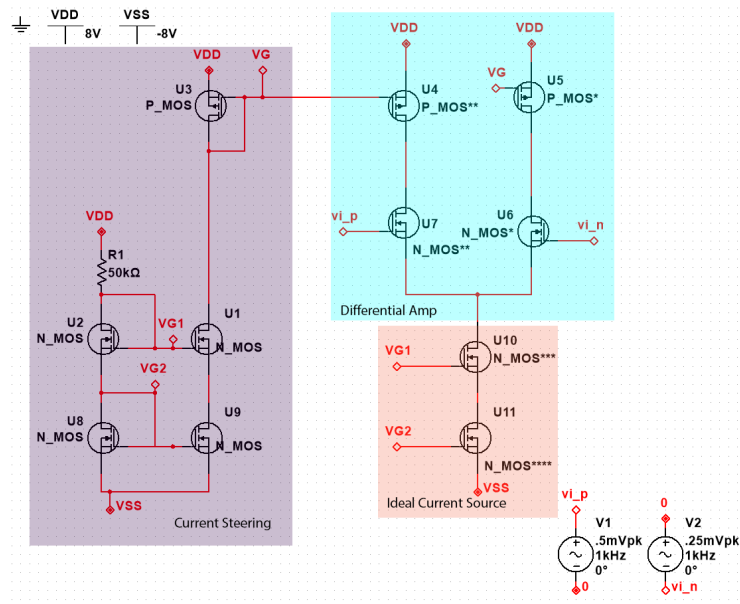
1.3.1 Problems Encountered

In part one of the project the above MOSFETs were causing wild variations in readings, switching to Multisim 14 helped to solve those problems. Multisim 14 was also used in part two of the project to prevent further issues.

2 Initial Circuit

The circuit designed in the previous project is as follows. The sections are colored to show the purpose of each area of the circuit. This is the circuit that will be cascoded for this project. In its current state the gain achieved is 100.

Figure 1: Project: Part 1



3 Double ended Cascoded Amplifier

To design an amplifier to work in a cascoded configuration we must calculate several values, including biasing voltages, drain current, and a new resistance value.

3.1 Gain Equation

Before we can start solving for other parts of the circuit we need to go ahead and find a equation for the gain of our circuit. From the book we can see that the gain can be obtained by the differential-half circuit of the cascoded amplifier, it is as follows

$$A_d \equiv \frac{V_{od}}{V_{id}} = g_{m1}(R_{on}||R_{op})$$

where

$$R_{on} = (g_{m3}r_{o3})r_{o1}$$

and

$$R_{op} = (g_{m5}r_{o5})r_{o7}$$

with those equations and our equation for transconductance

$$g_m = \sqrt{2k_n I_D}$$

we can begin to solve for A_D knowing that all mosfets have the same parameters.

$$R_{on} = \frac{1}{\lambda I_D} \frac{1}{\lambda I_D} g_m$$

$$R_{on} = \frac{1}{\lambda^2 I_D^2} g_m$$

$$R_{on} = \frac{1}{\lambda^2 I_D^2} \sqrt{2k_n I_D}$$

$$R_{on}||R_{op} = \frac{1}{2} \frac{1}{\lambda^2 I_D^2} \sqrt{2k_n I_D}$$

Now we take $R_{on}||R_{op}$ and plug it into our gain equation $A_d \equiv \frac{V_{od}}{V_{id}} = g_{m1}(R_{on}||R_{op})$

$$A_d = \frac{1}{2} \frac{1}{\lambda^2 I_D^2} \sqrt{2k_n I_D} \sqrt{2k_n I_D}$$

which simplifies to our gain equation,

$$A_d = \frac{k_n}{\lambda^2 I_D}$$

3.2 Calculating Drain Current I_d

With the given constants $k_n = k_p = .5m$ and $\lambda = .02$ we can effectively solve for I_D using the gain equation and $A_d = 10000$

$$A_d = \frac{k_n}{\lambda^2 I_D}$$

$$I_D = 250\mu A$$

3.3 Finding Biasing Voltage

In order to ensure that all MOSFETs are operating in saturation, we need to find the gate voltage that will cause saturation. Using the current equation

$$I_D = \frac{1}{2}k_n(V_G - V_S - V_t)^2(1 + \lambda V_{ds})$$

we can solve for V_G using constants and deriving constants. For V_{DS} we will use $V_g + 8$ and for V_S we will use $8v$

$$250\mu = \frac{1}{2}.001(V_G + 7)^2(1 + .02(V_G + 8))$$

Solving Through gives us

$$0 = .02V_G^3 + 1.44V_G^2 + 17.22V_G + 56.34$$

$$V_G = -58, -6.4, -7.7$$

The first value of $V_G - 58$ can be immediately disregarded from the extraneous solutions due to its extreme variation from the normal values. From simulation the value arrived at is

$$V_{Gn} = -6.3V$$

Since the all biasing MOSFETs are matched we can conclude that the drop across each will be roughly $1.7V$.

3.4 Calculating R_D

We can now find R_D using the values calculated and by finding the voltage drop across the resistor. V_{SS} drops from $-8V$ to $-6.3V$ and then drops another $1.7V$ to $-4.6V$. From $8V$ to $-4.6V$ will be the drop across our resistor.

$$R_D = \frac{8 + 4.6V}{.00025} \approx 50K\Omega$$

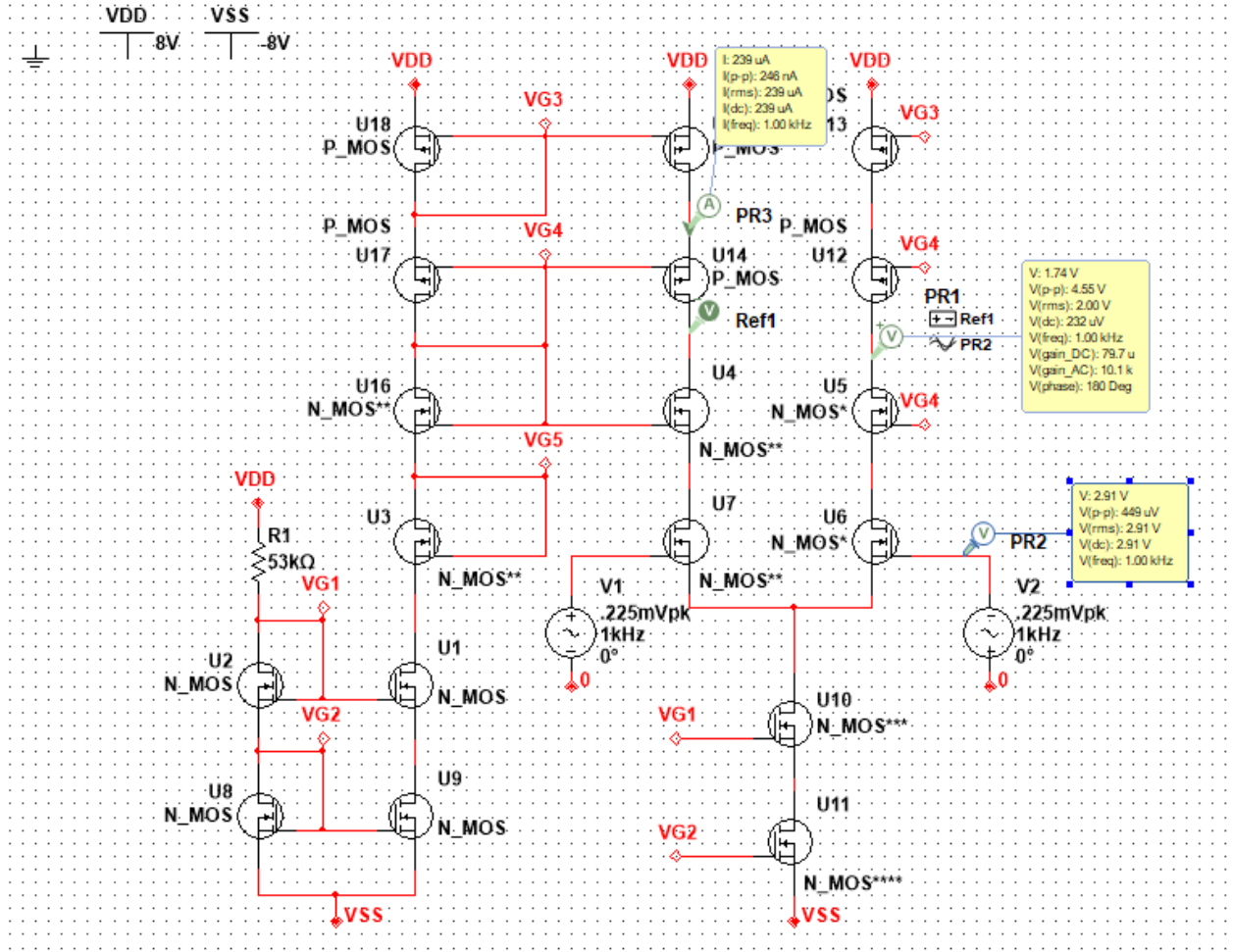
3.5 Current Source $\frac{W}{L}$

Knowing that our W/L for each of our branches results in a current of $250\mu A$ and that it is related directly to current we can double $\frac{W}{L}$ to obtain an I of $500\mu A$. This results in our current source NMOS to have a ratio of $\frac{4}{1}$.

3.6 Circuit Design

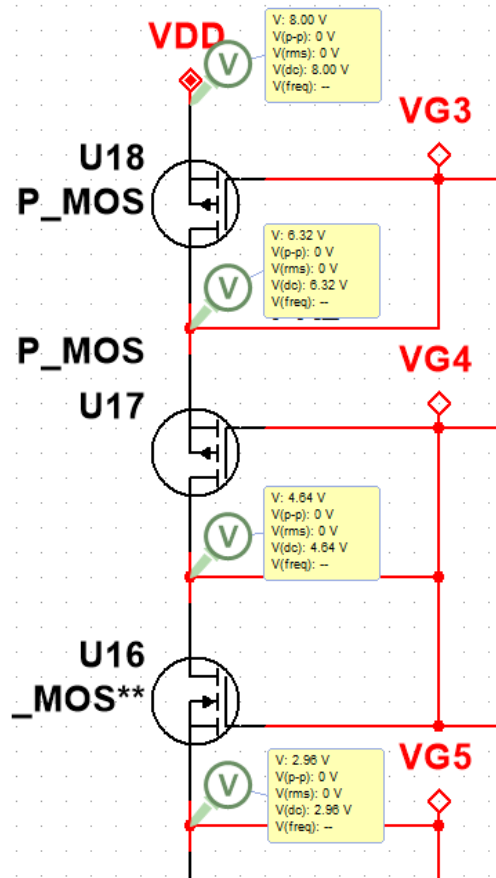
The final circuit design is as follows. A resistance value of $53k\Omega$ was used to obtain acceptable gain.

Figure 2: Project: Part 2 Circuit Design



Each NMOS and PMOS to the left of the cascoded amplifier acts to bias the corresponding MOSFETs on the right. This ensures that all MOSFETs operate in saturation to achieve a correct gain of $\approx 10,000$. These MOSFETs preform as predicted in section 3.3 with a drop of $1.7V$ after each subsequent MOSFET.

Figure 3: Biasing Mosfets



AC_VOLTAGE

Label Display Value Fault Pins

Voltage (Pk): .225m V

Voltage offset: 2.91 V

Frequency (F): 1k Hz

Time delay: 0 s

Damping factor (1/s): 0

Phase: 0 °

AC analysis magnitude: 1 V

AC analysis phase: 0 °

Distortion frequency 1 magnitude: 0 V

Distortion frequency 1 phase: 0 °

Distortion frequency 2 magnitude: 0 V

Distortion frequency 2 phase: 0 °

Tolerance: 0 %

Replace... OK Cancel Help

(a) Positive Offset

AC_VOLTAGE

Label Display Value Fault Pins

Voltage (Pk): .225m V

Voltage offset: -2.91 V

Frequency (F): 1k Hz

Time delay: 0 s

Damping factor (1/s): 0

Phase: 0 °

AC analysis magnitude: 1 V

AC analysis phase: 0 °

Distortion frequency 1 magnitude: 0 V

Distortion frequency 1 phase: 0 °

Distortion frequency 2 magnitude: 0 V

Distortion frequency 2 phase: 0 °

Tolerance: 0 %

Replace... OK Cancel Help

(b) Negative Offset

Figure 4: Offsetting input voltages

The NMOS U3 as seen in figure 3, when connected directly to the small-signal input causes convergence errors, its purpose is to create a biasing voltage for U7, the way that I solved this error is to apply the offset directly to the two input signal as seen in Figure 4.

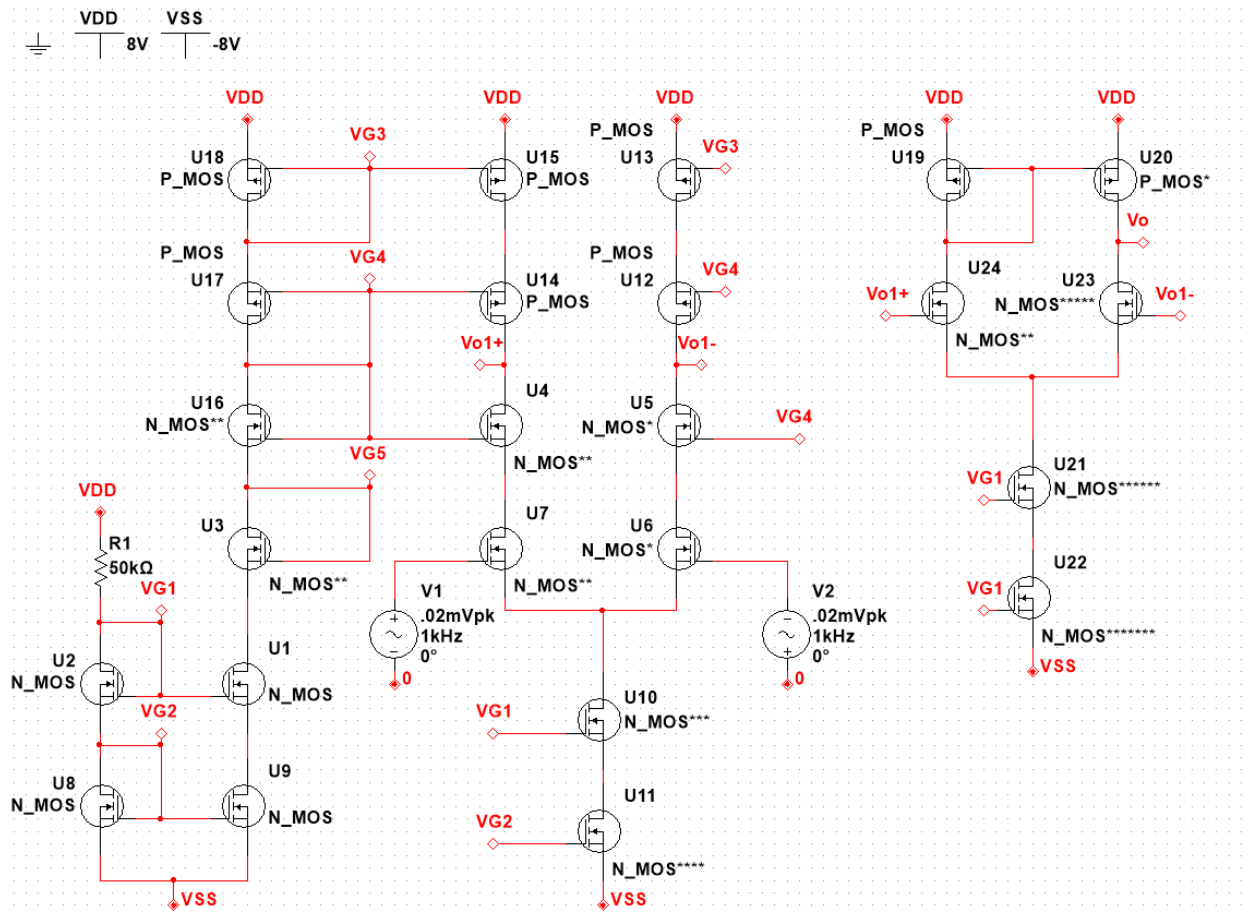
4 Single-Ended Output

Now that we have cascoded our amplifier successfully we can continue our design process to now add another amplifier with a gain of 10 to a single ended output.

We must also keep in mind that this amplifier because it is single-ended must produce a gain of 20 that will be reduced by half.

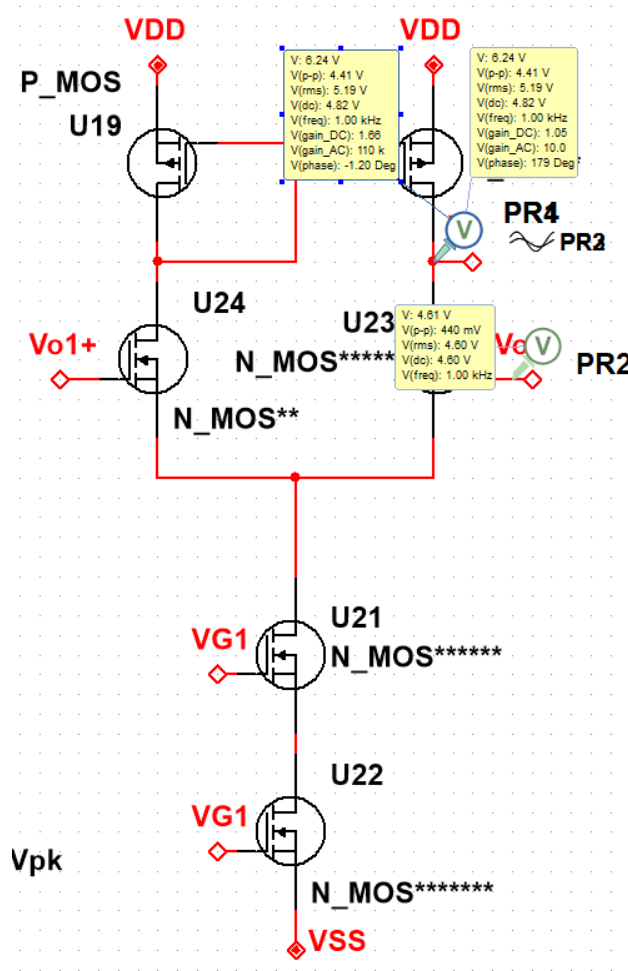
The following figure is the designed amplifier with the Single-ended Output.

Figure 5: Single-Ended Output Amplifier



The gain produced by this circuit can be seen in the following.

Figure 6: Single-Ended Output Amplifier



5 Conclusion

The project so far has been challenging but rewarding. By chopping the assignment into pieces and individual circuits it made tackling the final circuit significantly easier. Im am very proud that the final circuit that does in fact meets all requirements set forth. The tackling of this project help solidify my understanding of not only MOSFETs but also engineering design as a whole.