数字电子技术（双语）　核心知识点自测题

院(系)_____ 班级_____ 学号_____ 姓名_____

1．(15') Analyze the circuit in Figure1.

(1) Write the output expression for the circuit.

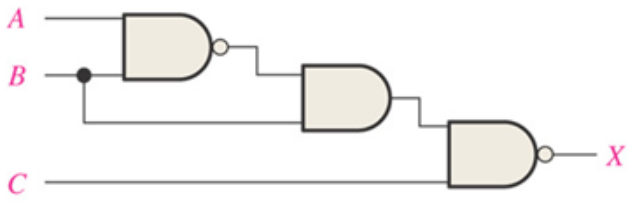


Figure 1

(2) Develop the truth table for the circuit.

(3) **Minimize** the gates required to implement the function.

2. (10')A D flip-flop is connected as shown in Figure2. Determine the Q output in relation to the clock and inputs.

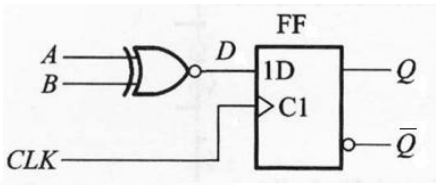
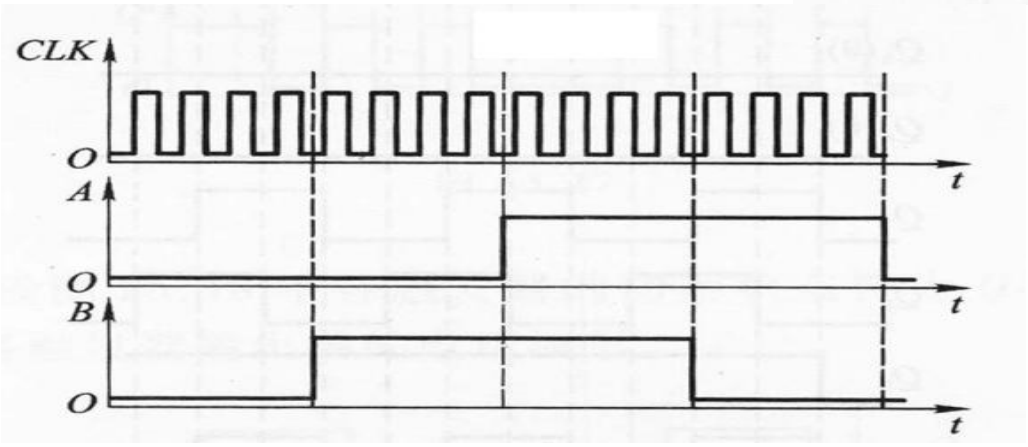


Figure2



自觉遵守考试规则，诚信考试，绝不作弊　装订线内不得答题

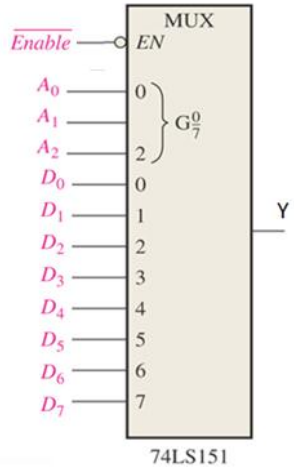
3. (20’) Implement a three inputs parity checker with odd parity. The output is “1” when the number of input “1” is odd.

（1）Using NAND Gates only

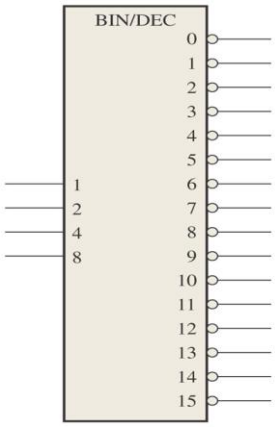
(2) Using a 74LS151 8-inputs data selector/multiplexer.

Function Table of 74LS151

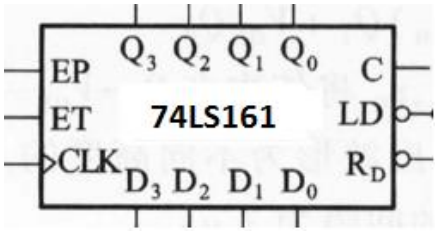
INPUTS			OUTPUT
A_2	A_1	A_0	Y
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

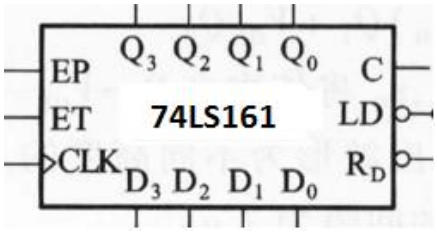


4. (10’)You wish to detect only the presence of the codes 1110, 1001, 0101 and 1011. An active-HIGH output is required to indicate their presence. Develop the logic circuit with a single output that will indicate when any one of these codes is on the inputs. For any other code, the output must be LOW. Please use a 4-line-to-16-line decoder with fewer gates as needed.



5. (15')Show how to connect two 74LS161s for a modulus-35 counter with sequence $(1,2,\ldots 35)_{10}$.





6. (15')Determine the sequence of the counter in Figure 3, showing the Q_1, Q_2 and Q_3 waveforms.

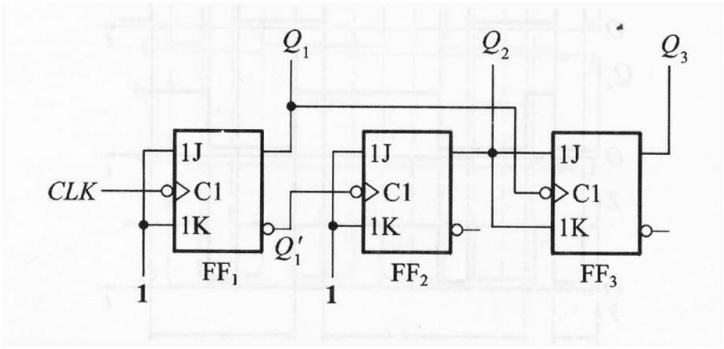
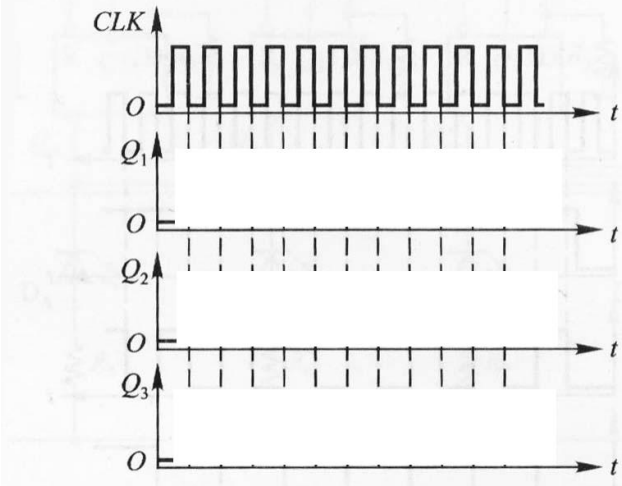


Figure 3



7. (15') Design a synchronous counter with sequence 00→01→11→10→00, use JK flip-flops.