第三章 逻辑代数

第四章 组合逻辑电路

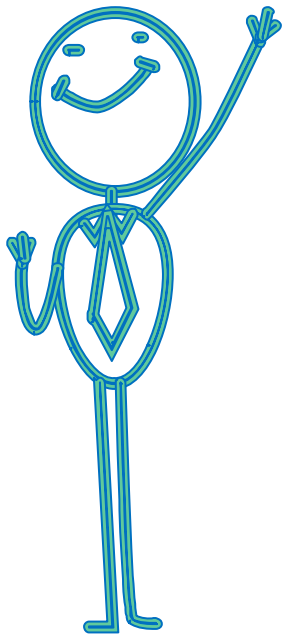
一、小规模组合逻辑电路初探（ 4.1 ）

二、 逻辑代数（3）

三、小规模组合逻辑电路分析和设计（ 4.1 ）

四、常用组合逻辑电路芯片（4.2）

四、常用组合逻辑电路芯片



4.2.1 加法器

4.2.2 数值比较器

4.2.3 编码器

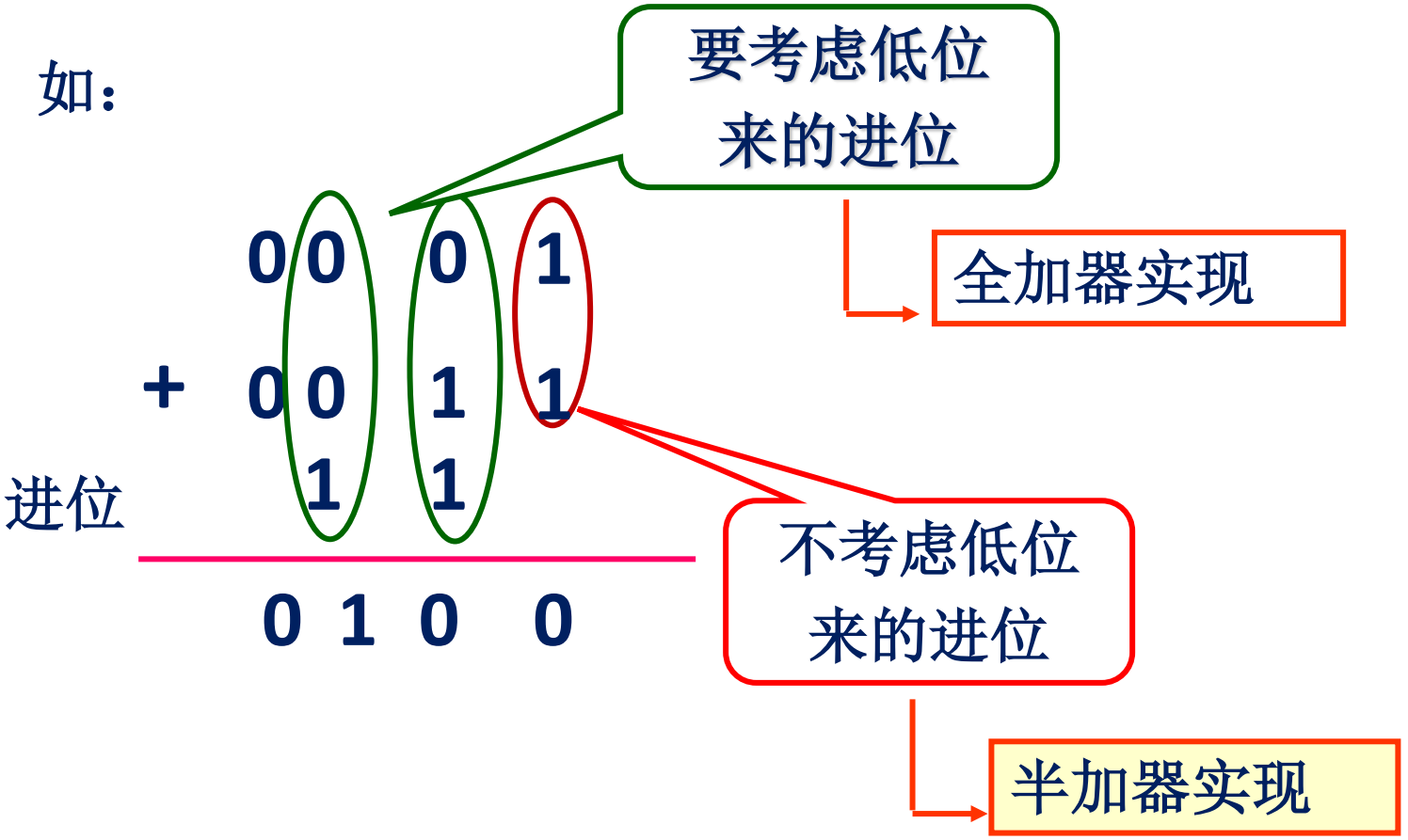
4.2.4 译码器

4.2.5 数据选择器和数据分配器

加法器(Adders)

实现二进制加法运算的电路

如：



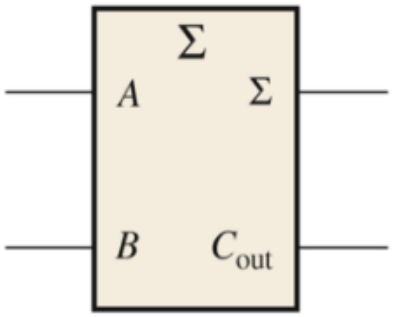
半加器(Half Adder)

实现两个一位二进制数相加，不考虑来自低位的进位。

两个输入：*A*，*B* 表示两个同位相加的数

两个输出：
- Σ —— 表示半加和
- *Cout* —— 表示向高位的进位

逻辑符号



真值表

A	*B*	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

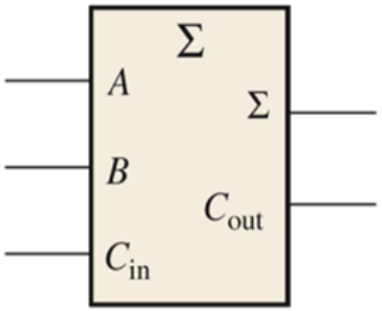
全加器 (Full Adder)

实现两个一位二进制数相加，且考虑来自低位的进位

输入
- A
- B 表示两个同位相加的数
- C_{in} 表示低位来的进位

输出
- $\sum$ 表示本位和
- C_{out} 表示向高位的进位

逻辑符号



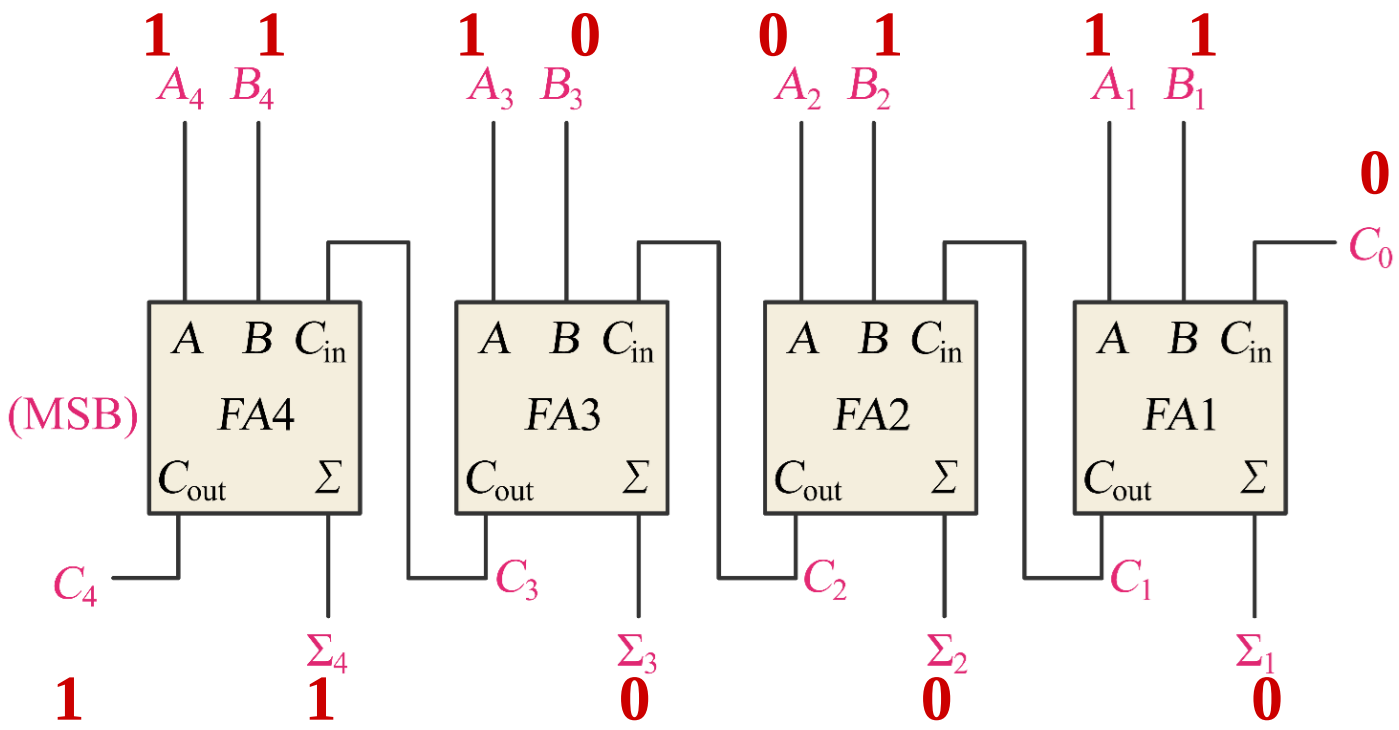
真值表

A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

用全加器实现四位二进制加法

$$A_4A_3A_2A_1 + B_4B_3B_2B_1$$

级联



如：

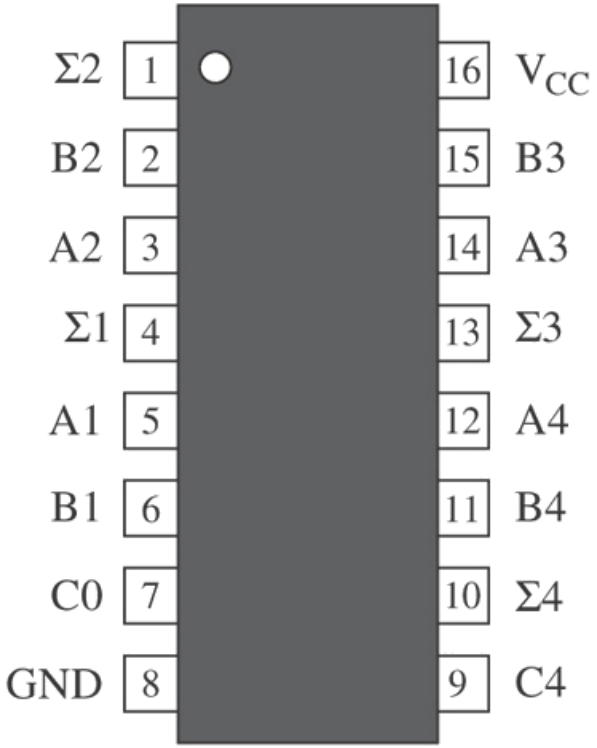
1 1 0 1

+ 1 0 1 1

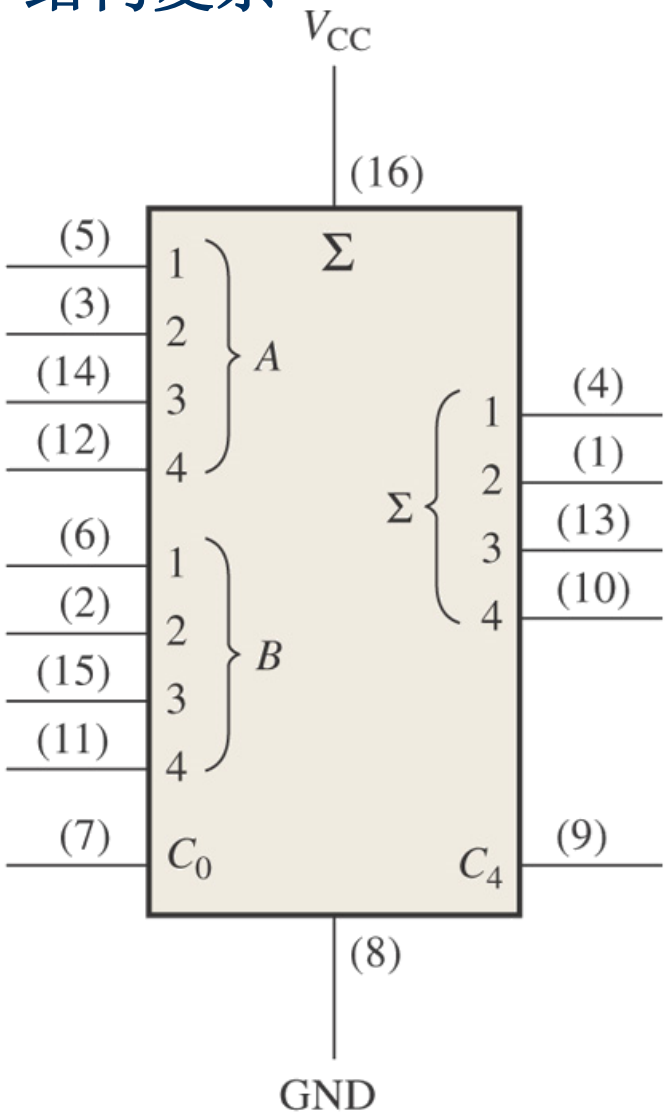
工作特点：任意一位的加法运算，都必须等到低位加法完成送来进位时才能进行

串行进位加法器

超前进位加法器——速度快，结构复杂

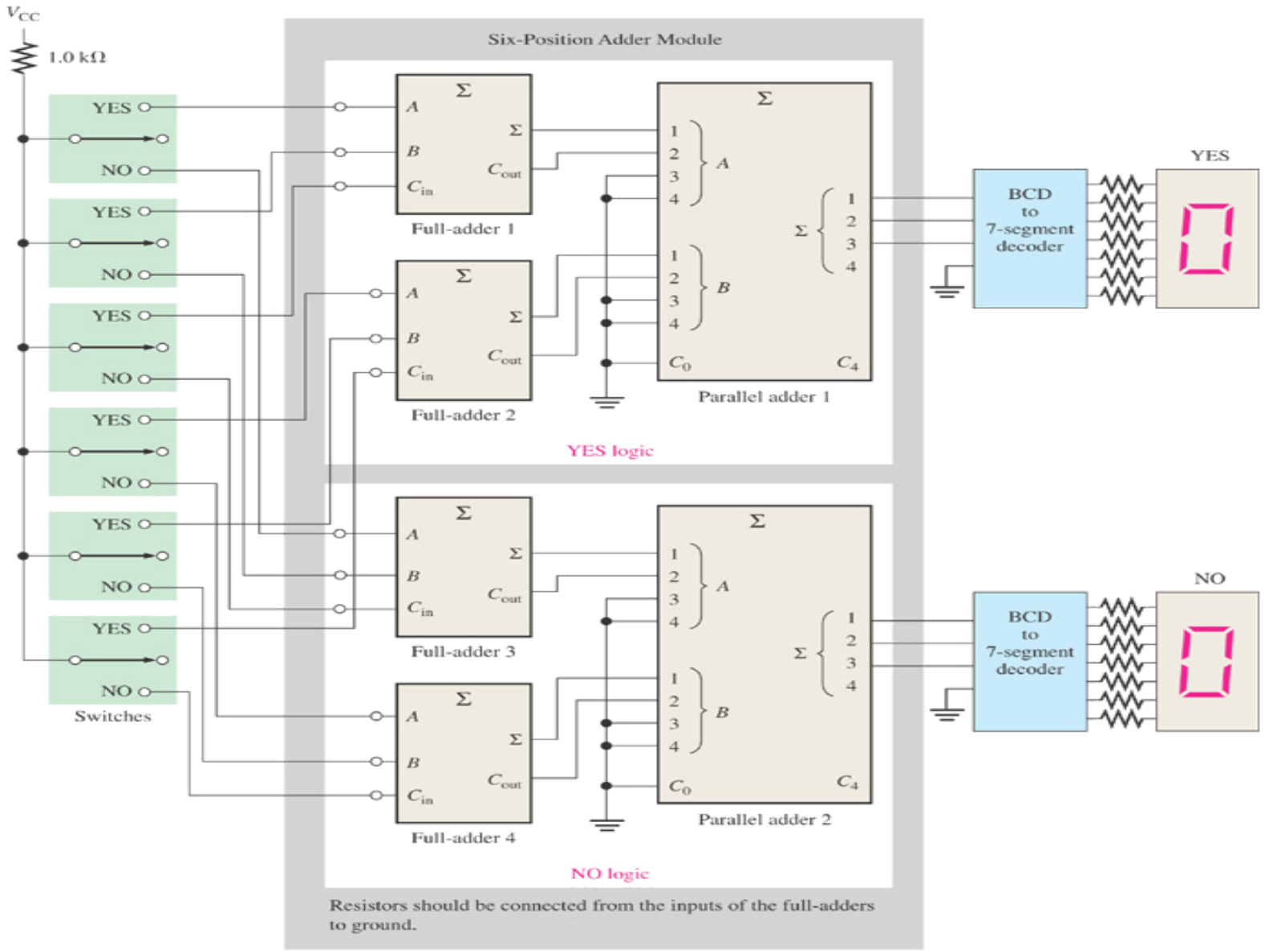


(a) Pin diagram of 74LS283

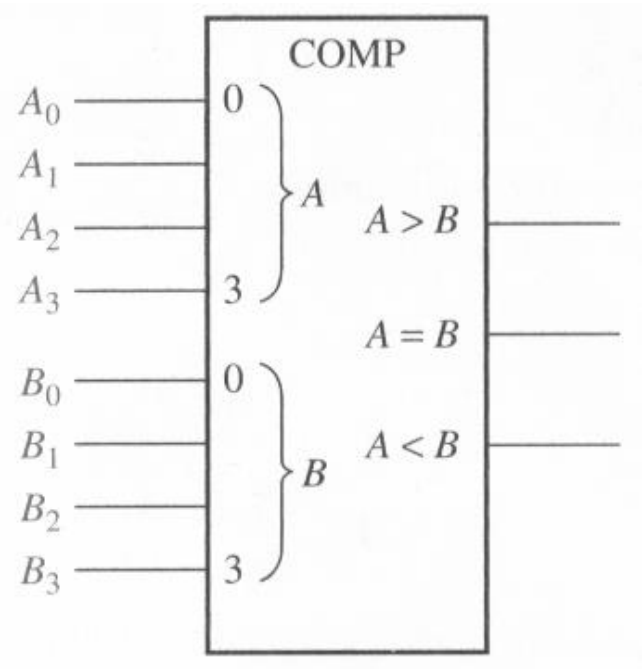


(b) 74LS283 logic symbol

Application of adder : A voting system



比较器(Comparators)



四位二进制比较器

- A 大于B时
  (A > B输出高电平)
- A 等于 B时
  (A = B输出高电平)
- A小于B时
  (A < B输出高电平)

more-Bit Comparator

Comparing principle：

1. 先从高位比起，高位大的数值一定大,不需要看低位。

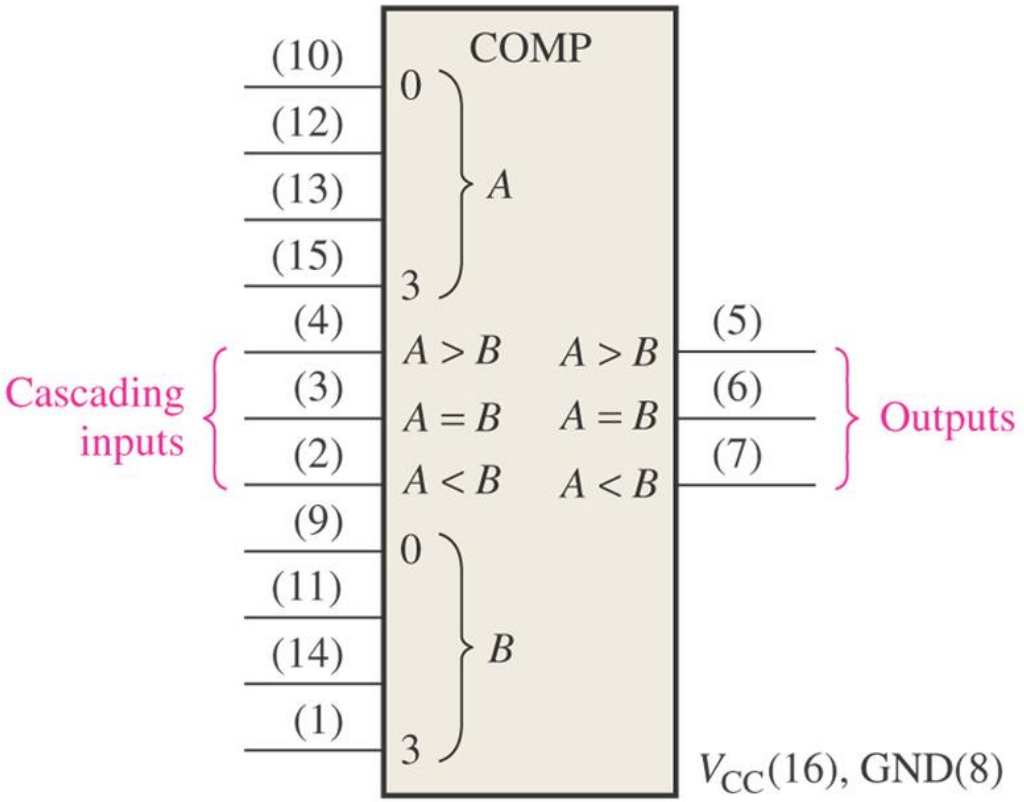
2. 若高位相等，则再比较低位数，最终结果由低位的比较结果决定。

3. 比较结果先看谁？低位or高位？

Truth table for four-bit comparator

input				output		
$a_3\ b_3$	$a_2\ b_2$	$a_1\ b_1$	$a_0\ b_0$	L (A>B)	E (A=B)	S (A<B)
$a_3 > b_3$	×	×	×	1	0	0
$a_3 < b_3$	×	×	×	0	0	1
$a_3 = b_3$	$a_2 > b_2$	×	×	1	0	0
$a_3 = b_3$	$a_2 < b_2$	×	×	0	0	1
$a_3 = b_3$	$a_2 = b_2$	$a_1 > b_1$	×	1	0	0
$a_3 = b_3$	$a_2 = b_2$	$a_1 < b_1$	×	0	0	1
$a_3 = b_3$	$a_2 = b_2$	$a_1 = b_1$	$a_0 > b_0$	1	0	0
$a_3 = b_3$	$a_2 = b_2$	$a_1 = b_1$	$a_0 < b_0$	0	0	1
$a_3 = b_3$	$a_2 = b_2$	$a_1 = b_1$	$a_0 = b_0$	0	1	0

芯片74HC85



AB不等时，比较器的输出可以不用看低位送过来的cascading inputs

AB相等时，比较器的输出需要看cascading inputs来给出最后判断

A=B:

$$\mathbf{E} = \overline{\mathbf{A} \oplus \mathbf{B}}$$

$$= \overline{(a_3 \oplus b_3)}\,\overline{(a_2 \oplus b_2)}\,\overline{(a_1 \oplus b_1)}\,\overline{(a_0 \oplus b_0)}\,I_{A=B}$$

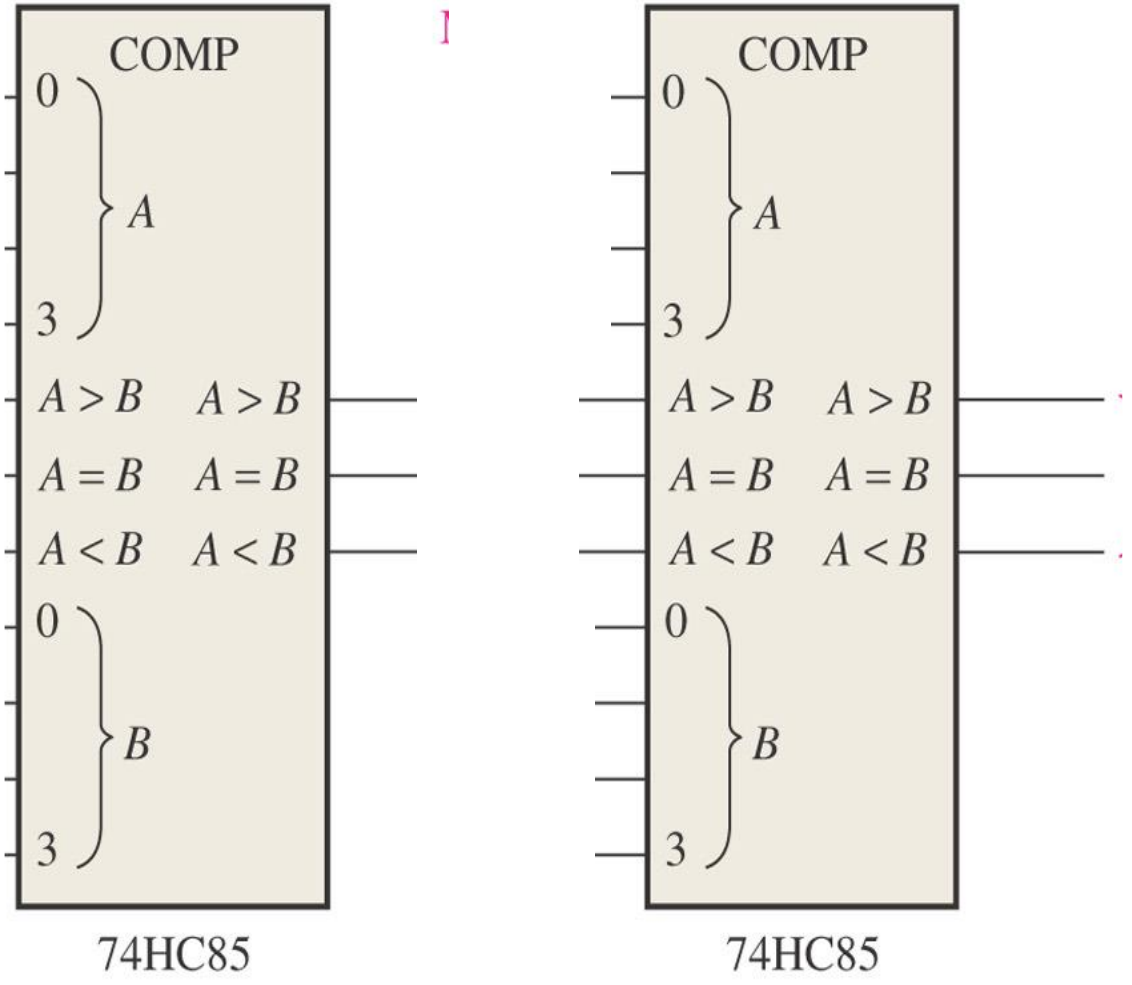
A<B:

$$\mathbf{S} = \overline{\mathbf{a}_3}\,\mathbf{b}_3 + \overline{(\mathbf{a}_3 \oplus \mathbf{b}_3)}\,\overline{\mathbf{a}_2}\,\mathbf{b}_2 + \overline{(\mathbf{a}_3 \oplus \mathbf{b}_3)}\,\overline{(\mathbf{a}_2 \oplus \mathbf{b}_2)}\,\overline{\mathbf{a}_1}\,\mathbf{b}_1$$
$$+ \overline{(a_3 \oplus b_3)}\,\overline{(a_2 \oplus b_2)}\,\overline{(a_1 \oplus b_1)}\,\overline{a_0}\,b_0$$
$$+ \overline{(a_3 \oplus b_3)}\,\overline{(a_2 \oplus b_2)}\,\overline{(a_1 \oplus b_1)}\,\overline{(a_0 \oplus b_0)}\,I_{A<B}$$

A>B:

$$\mathbf{L} = \overline{\mathbf{E} + \mathbf{S}}$$

芯片级联: 用两片74HC85实现两个八位二进制数的比较



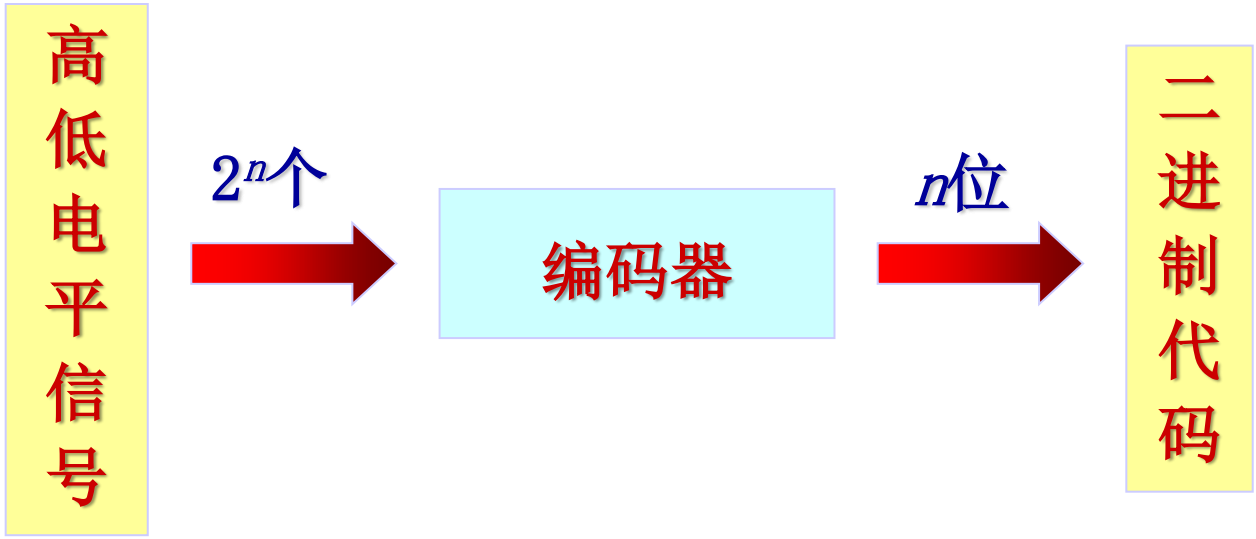
编码器 (Encoder）

编码:就用数字或某种文字符号来表示某一对象或信号的过程

如：电话号码、邮编、学号

二进制编码器

将一系列信号状态编制成二进制代码



一般编码器

每次只允许一个输入端有信号（只有一个有效信号 ）

8421BCD码编码

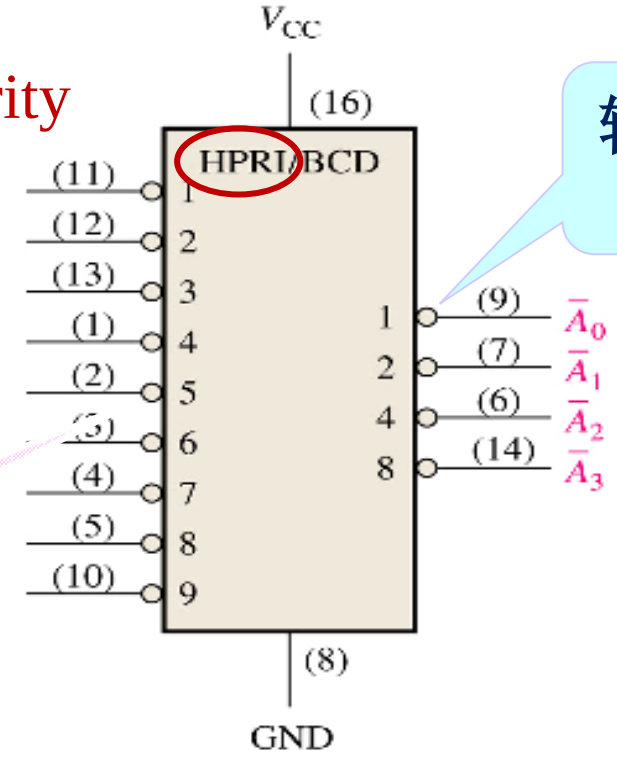
输 入	输 出			
	Y_3	Y_2	Y_1	Y_0
0 (I_0)	0	0	0	0
1 (I_1)	0	0	0	1
2 (I_2)	0	0	1	0
3 (I_3)	0	0	1	1
4 (I_4)	0	1	0	0
5 (I_5)	0	1	0	1
6 (I_6)	0	1	1	0
7 (I_7)	0	1	1	1
8 (I_8)	1	0	0	0
9 (I_9)	1	0	0	1

优先编码器

允许几个输入信号同时有效，但电路只对其中优先级别高的信号进行编码，对其它优先级别低的信号不予理睬。

74LS147集成优先编码器(10线–4线)

Highest has Priority



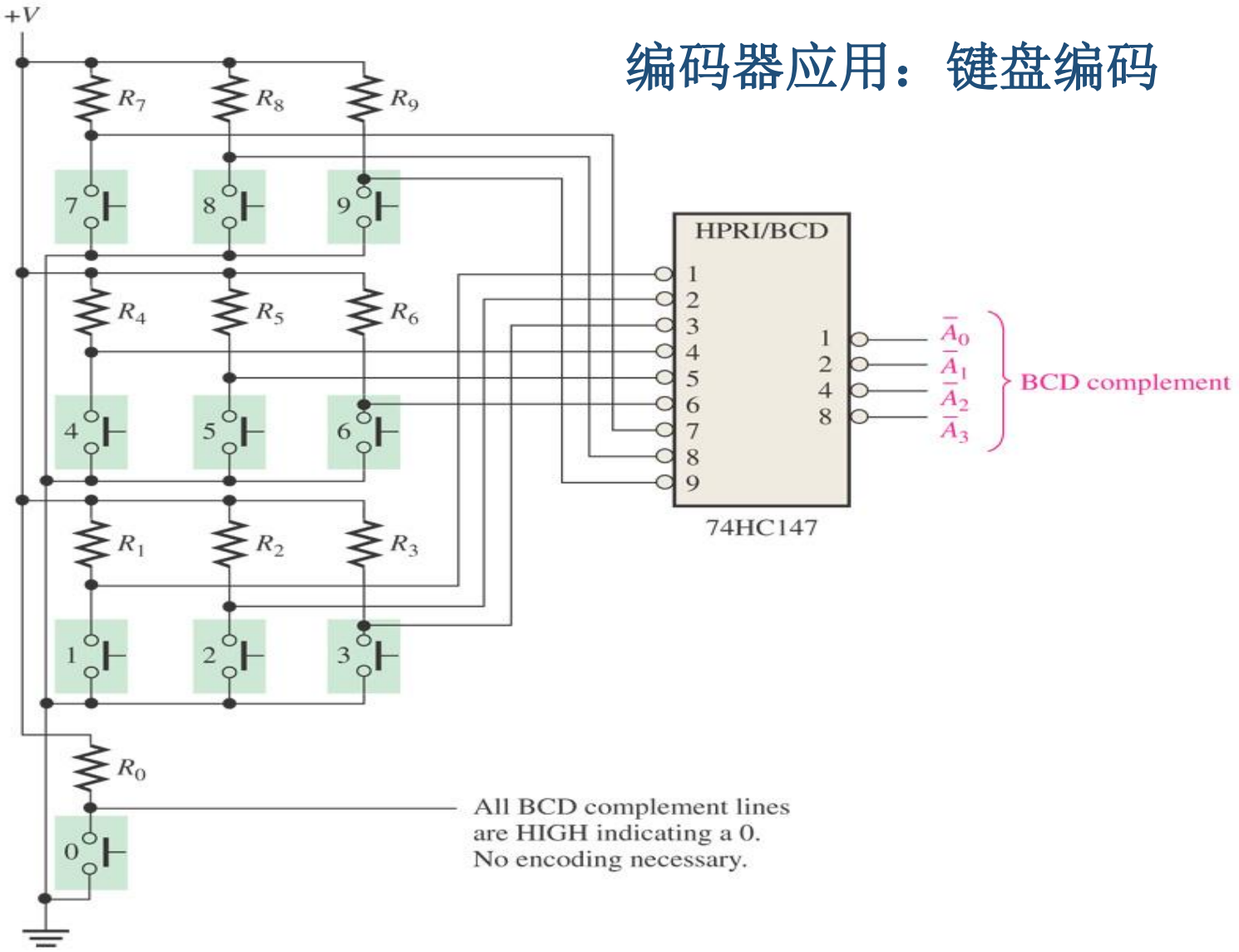
输出二进制反码

输入低电平有效

74LS147 优先编码器功能表——学会读

输入									输出			
$\overline{I_9}$	$\overline{I_8}$	$\overline{I_7}$	$\overline{I_6}$	$\overline{I_5}$	$\overline{I_4}$	$\overline{I_3}$	$\overline{I_2}$	$\overline{I_1}$	$\overline{A_3}$	$\overline{A_2}$	$\overline{A_1}$	$\overline{A_0}$
1	1	1	1	1	1	1	1	1	1	1	1	1
0	×	×	×	×	×	×	×	×	0	1	1	0
1	0	×	×	×	×	×	×	×	0	1	1	1
1	1	0	×	×	×	×	×	×	1	0	0	0
1	1	1	0	×	×	×	×	×	1	0	0	1
1	1	1	1	0	×	×	×	×	1	0	1	0
1	1	1	1	1	0	×	×	×	1	0	1	1
1	1	1	1	1	1	0	×	×	1	1	0	0
1	1	1	1	1	1	1	0	×	1	1	0	1
1	1	1	1	1	1	1	1	0	1	1	1	0

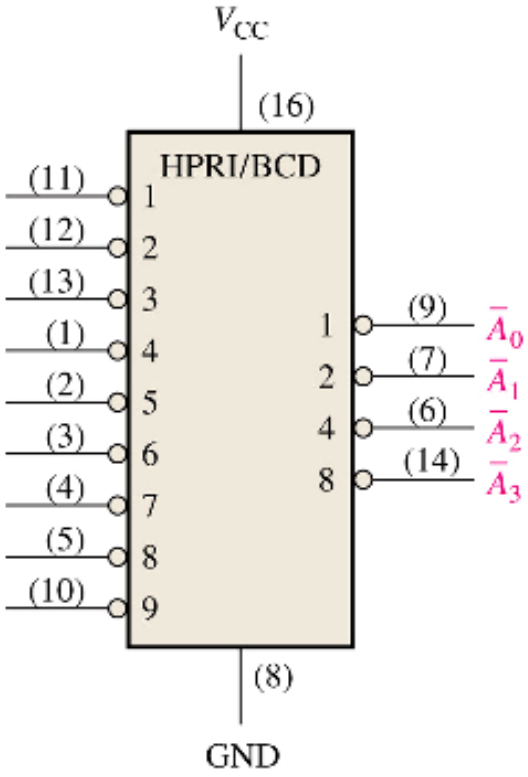
编码器应用：键盘编码


+V
R7
R8
R9
7
8
9
R4
R5
R6
4
5
6
R1
R2
R3
1
2
3
R0
0
HPRI/BCD
1
2
3
4
5
6
7
8
9
1
2
4
8
$\overline{A}_0$
$\overline{A}_1$
$\overline{A}_2$
$\overline{A}_3$
BCD complement
74HC147
All BCD complement lines
are HIGH indicating a 0.
No encoding necessary.

单选题 1分

设置

已知（ ）内数字为芯片管脚号，如果管脚1,4 和13为低电平, 其它输入端均为高电平， 请问四个输出端的状态应为___？（A_0为LSB）



A 0111

B 1000

C 1001

D 以上均不对

提交

单选题 1分

设置

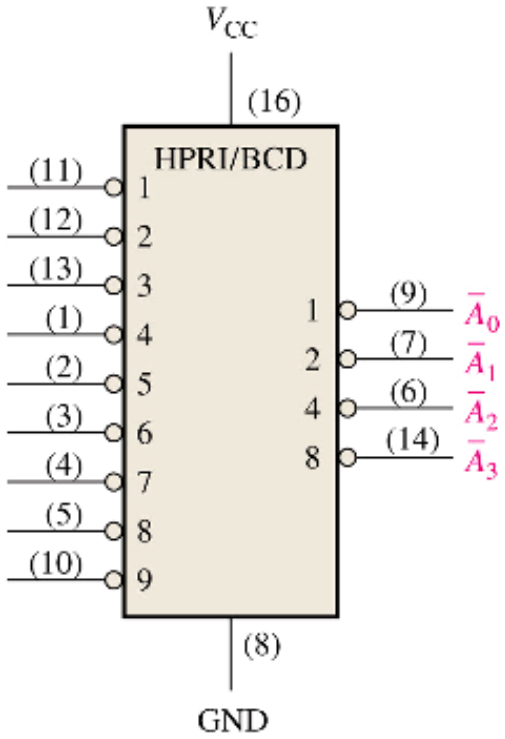
若所有输入均为低电平，四个输出端的状态应为____？（A_0为LSB）

A 0110

B 1000

C 1001

D 以上均不对



提交

单选题 1分

设置

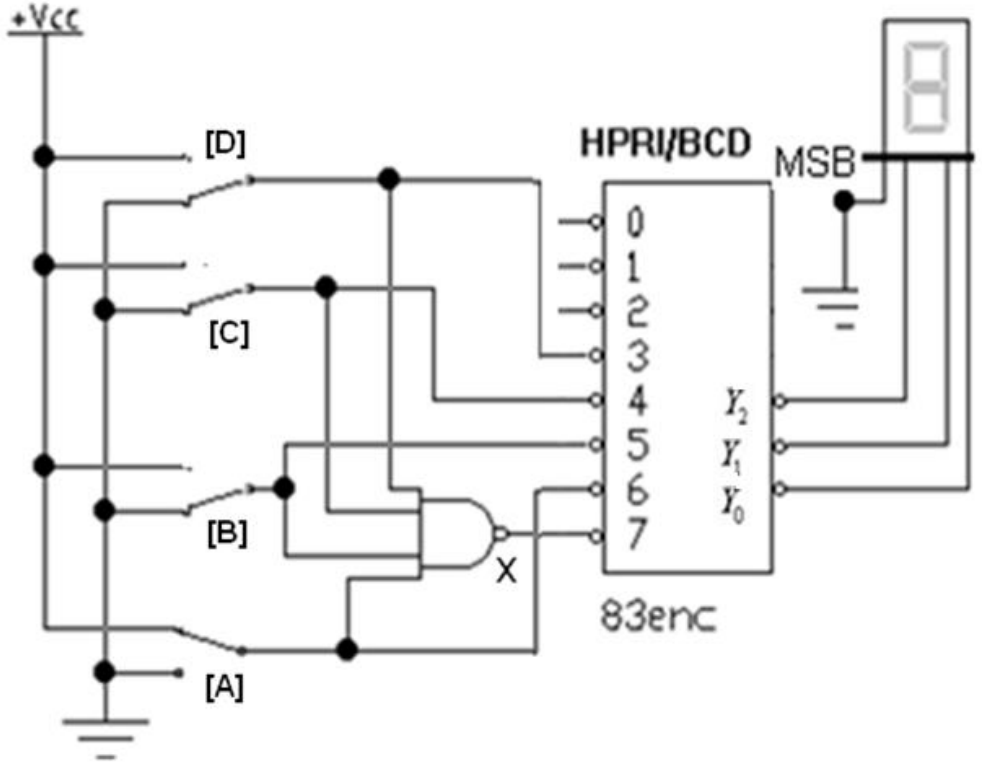
某病房呼叫显示系统中开关[A][B][C][D]分别用来模拟来自四个房间的呼叫信号，有呼叫信号时输入为低电平。当所有开关输入均位于高电平时，数码管显示数字为____

A 0

B 1

C 7

D 8

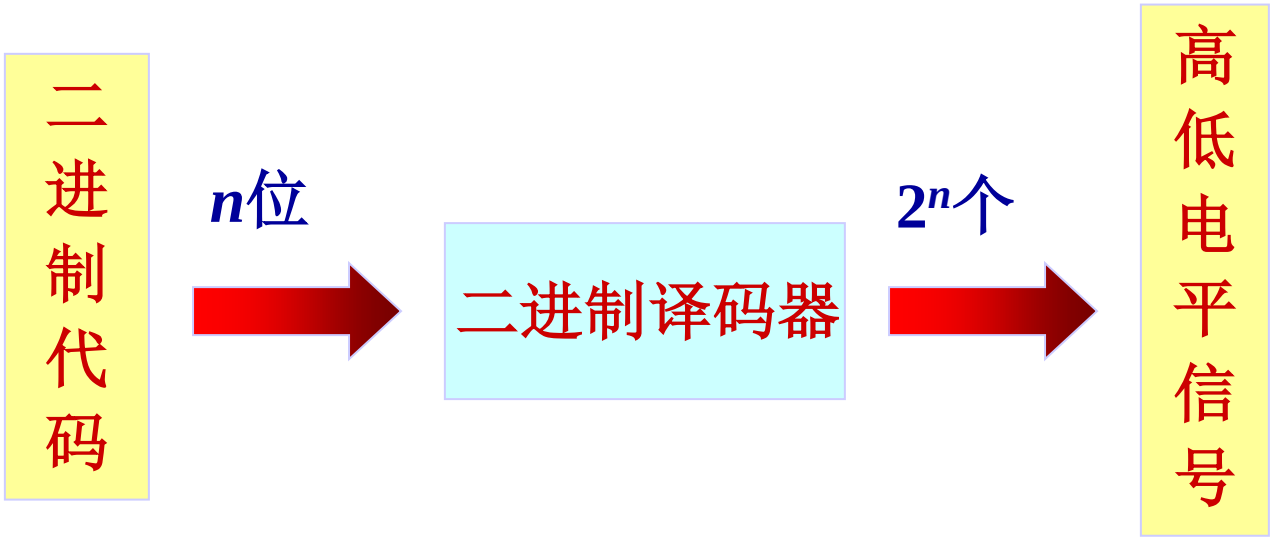


提交

译码器(Decoder)

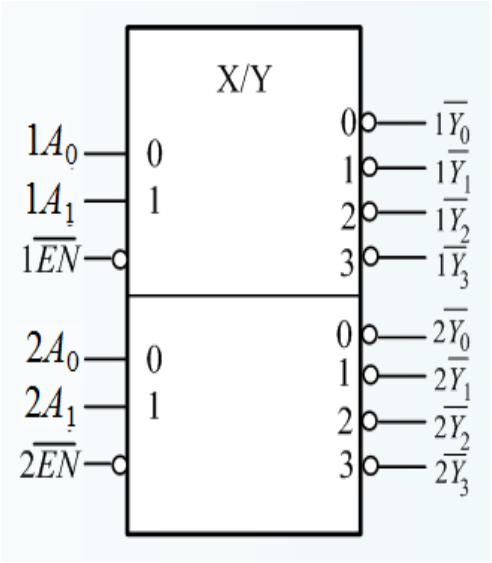
译码是编码的逆过程，即将某代码翻译成电路的某种状态

（二进制译码器， 显示译码器……）



74LS139 双2线/4线译码器

逻辑符号

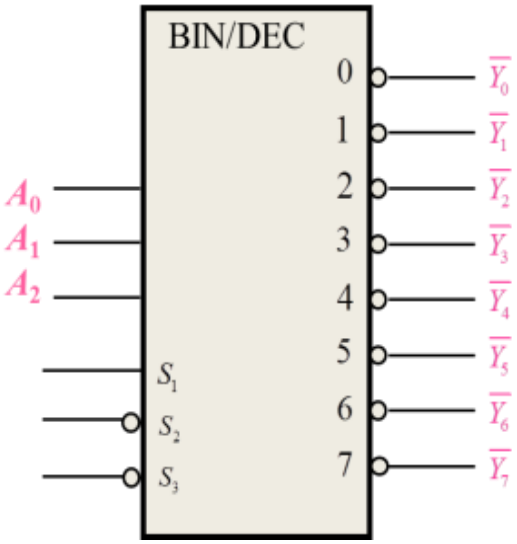


功能表

$\overline{EN}$	A_1	A_0	$\overline{Y}_3$	$\overline{Y}_2$	$\overline{Y}_1$	$\overline{Y}_0$
1	×	×	1	1	1	1
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1

74LS138 3线/8线译码器——会读功能表

逻辑符号

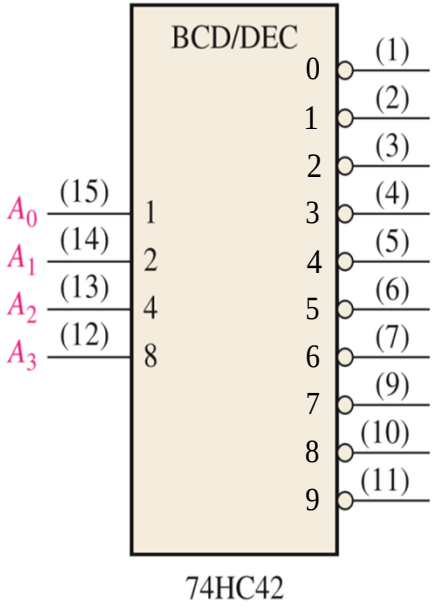


功能表

使能			输入			输出（低电平有效）							
S_1	$\overline{S}_2$	$\overline{S}_3$	A_2	A_1	A_0	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
0	×	×	×	×	×	1	1	1	1	1	1	1	1
×	1	×											
×	×	1											
1	0	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	0	0	1	1	1	1	0	1	1	1
1	0	0	1	0	1	1	1	1	1	1	0	1	1
1	0	0	1	1	0	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0

74HC42 BCD译码器

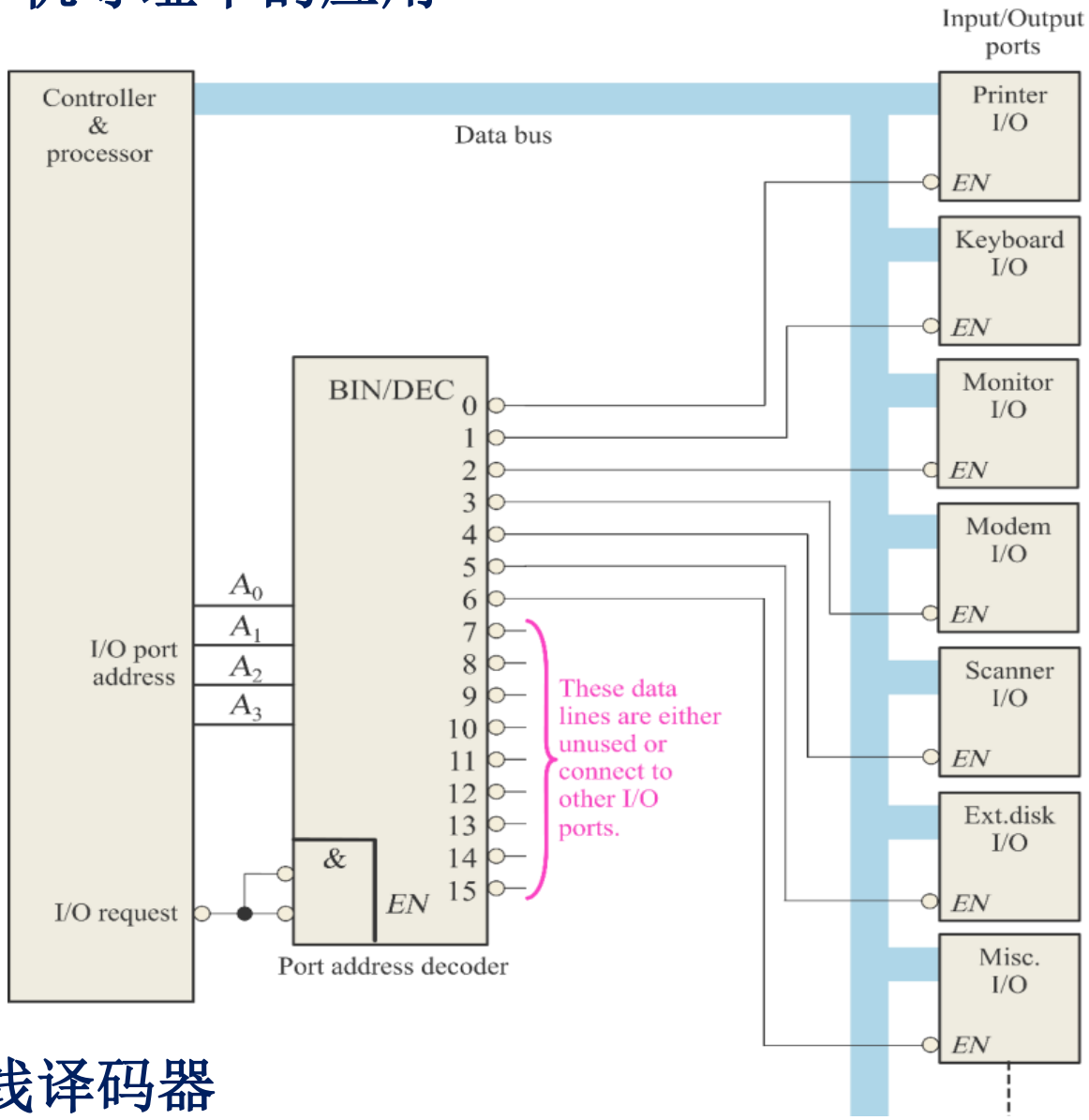
逻辑符号



功能表

十进制数	二进制输入				输出									
	A_3	A_2	A_1	A_0	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	1	0	1	1	1	1	1	1	1	1
2	0	0	1	0	1	1	0	1	1	1	1	1	1	1
3	0	0	1	1	1	1	1	0	1	1	1	1	1	1
4	0	1	0	0	1	1	1	1	0	1	1	1	1	1
5	0	1	0	1	1	1	1	1	1	0	1	1	1	1
6	0	1	1	0	1	1	1	1	1	1	0	1	1	1
7	0	1	1	1	1	1	1	1	1	1	1	0	1	1
8	1	0	0	0	1	1	1	1	1	1	1	1	0	1
9	1	0	0	1	1	1	1	1	1	1	1	1	1	0

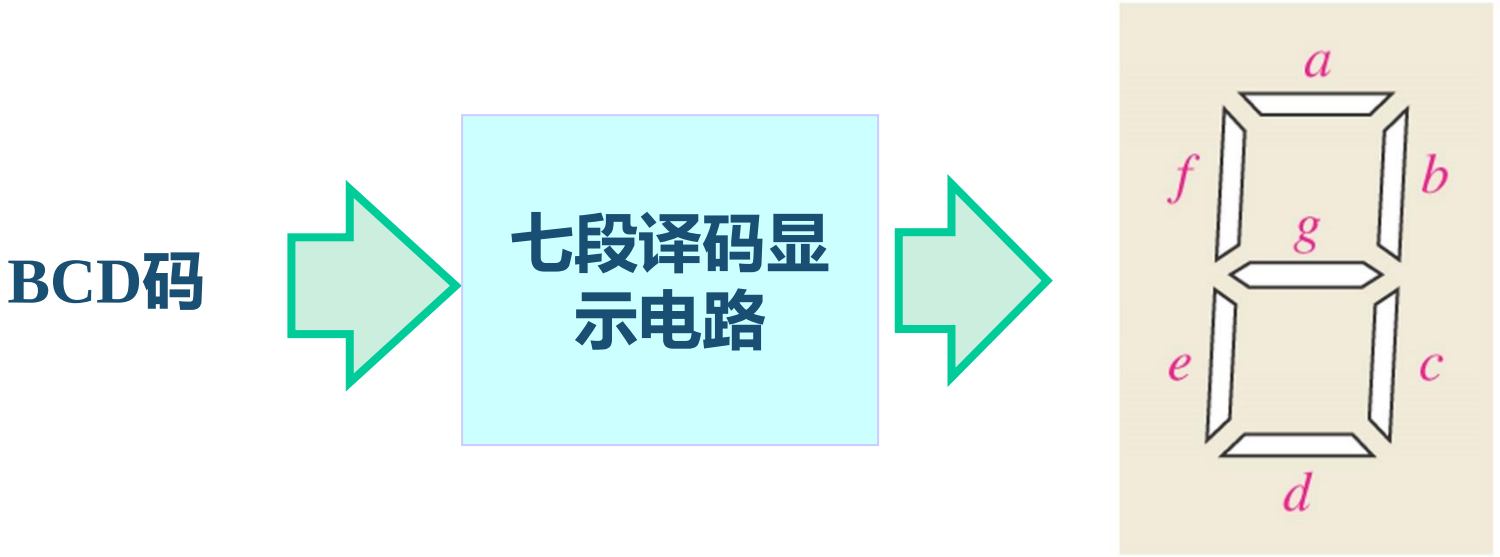
译码器在计算机寻址中的应用



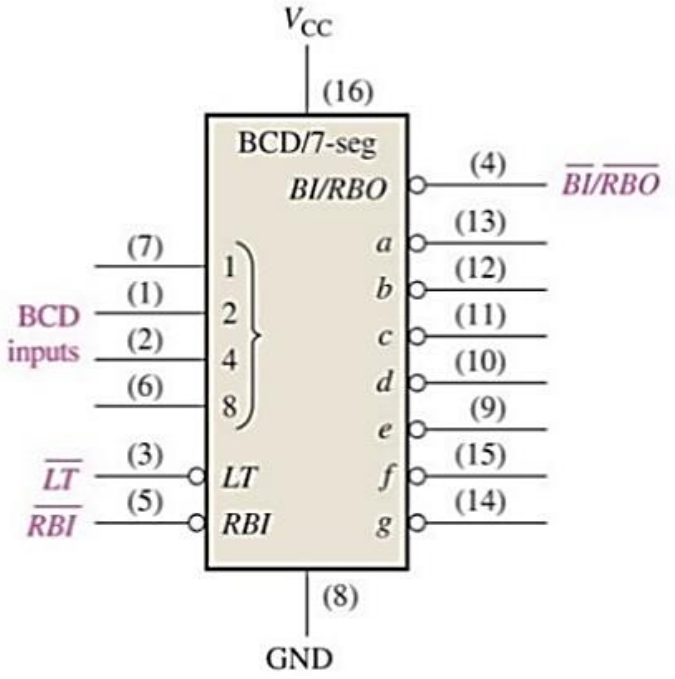
74HC154 4线16线译码器

七段数码管显示驱动电路的设计

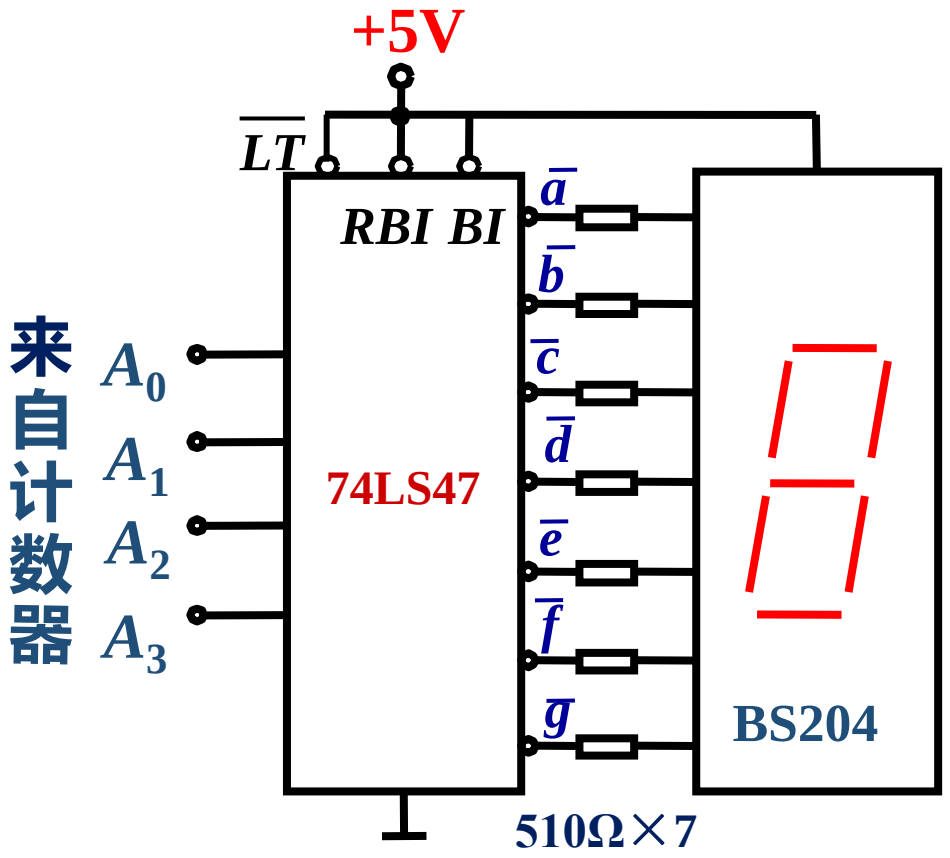
设计一个电路将用BCD码表示的数字通过七段数码管以十进制数值形式显示出来



显示译码器



74LS47



74LS47的功能表

	输入				输出	显示
	$\overline{LT}$	$\overline{RBI}$	$\overline{BI/RBO}$	$A_3A_2A_1A_0$	$\overline{a}\ \overline{b}\ \overline{c}\ \overline{d}\ \overline{e}\ \overline{f}\ \overline{g}$	
试灯	0	×	1	× × × ×	0 0 0 0 0 0 0	8
灭灯	×	×	0	× × × ×	1 1 1 1 1 1 1	全灭
灭零	1	0	1	0 0 0 0	1 1 1 1 1 1 1	全灭
	1	1	1	0 0 0 0	0 0 0 0 0 0 1	0
	1	×	1	BCD 码	译码	1~9

$\overline{BI/RBO}$（Blanking Input/Ripple Blanking Output）为复用端子

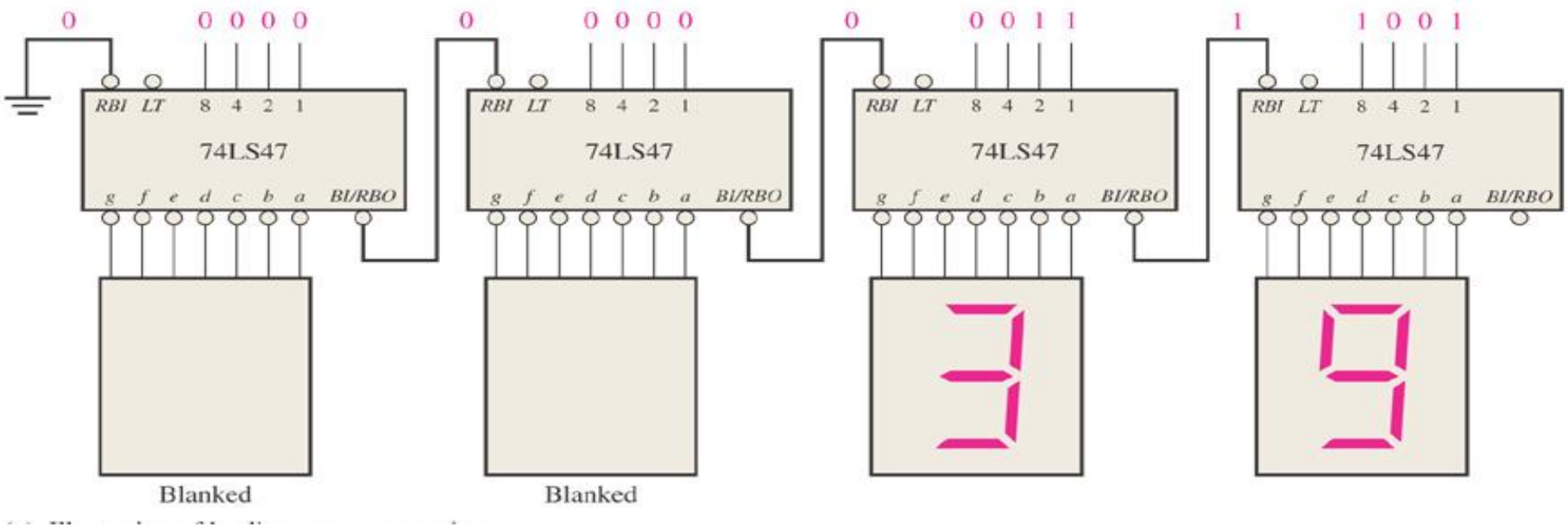
作为输入端子用时为$\overline{BI}$，是灭灯信号

作为输出端子用时为$\overline{RBO}$为，用来传递“灭零信号”

灭0应用举例

$\overline{RBI}$为灭零输入端子

$\overline{RBI}$为**0**和输入**0000**时，$\overline{RBO}$为零

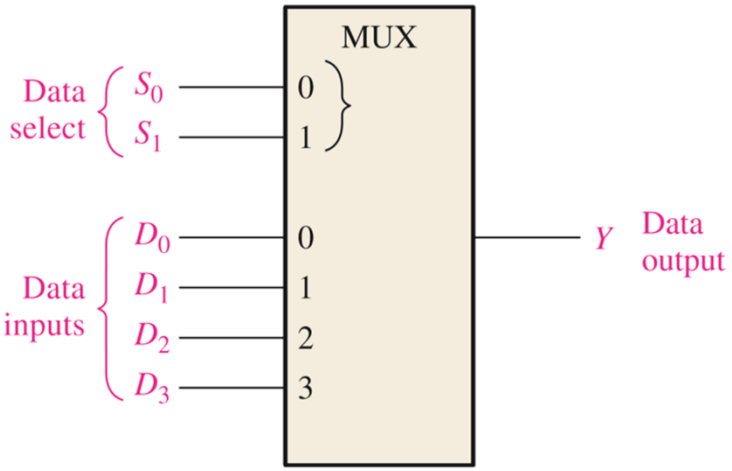


数据选择器(Multiplexer/Data Selector)

从多路数据中选择其中一路数据输出

四选一数据选择器

逻辑符号



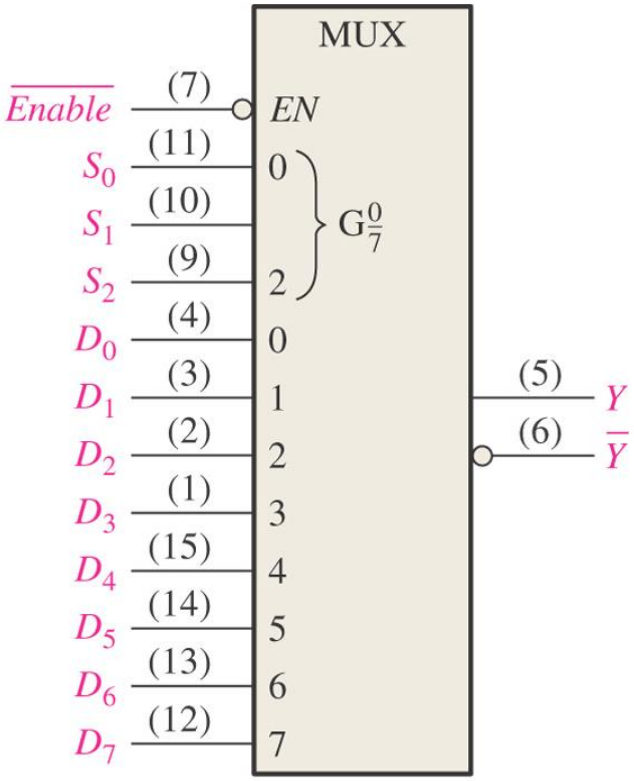
功能表

数据选择端		数据输出
S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

逻辑表达式 $Y = D_0\overline{S}_1\overline{S}_0 + D_1\overline{S}_1S_0 + D_2S_1\overline{S}_0 + D_3S_1S_0$

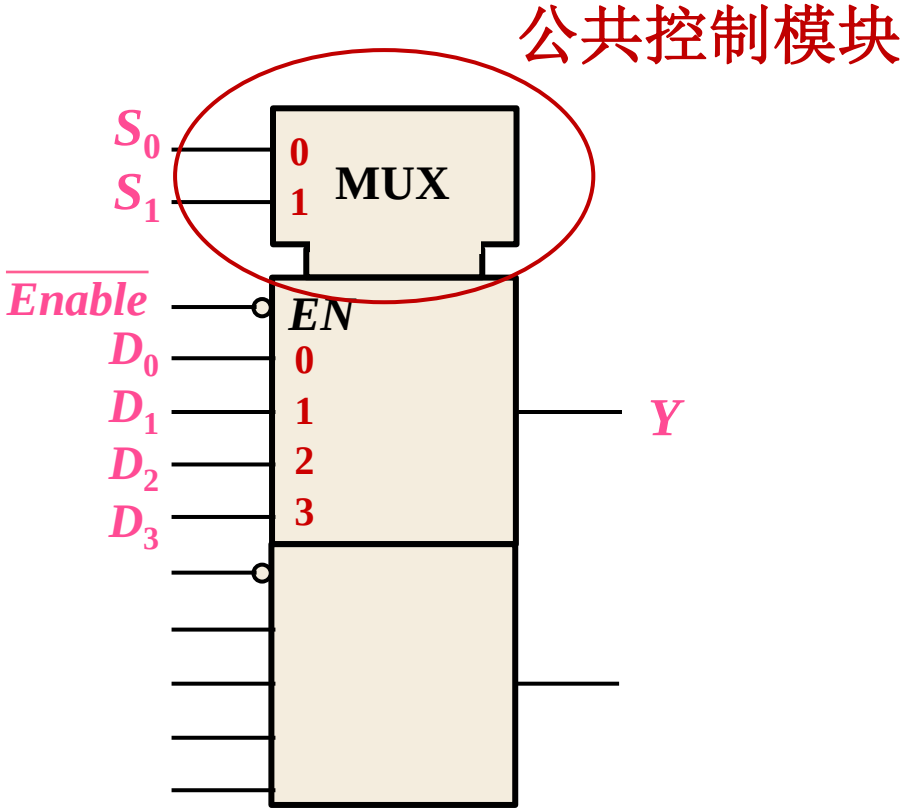
常用芯片

74LS151
8选1数据选择器



使能端	数据选择端			输出
$\overline{Enable}$	S_2	S_1	S_0	Y
1	×	×	×	0
0	0	0	0	D_0
0	0	0	1	D_1
0	0	1	0	D_2
0	0	1	1	D_3
0	1	0	0	D_4
0	1	0	1	D_5
0	1	1	0	D_6
0	1	1	1	D_7

74HC153
双四选一数据选择器

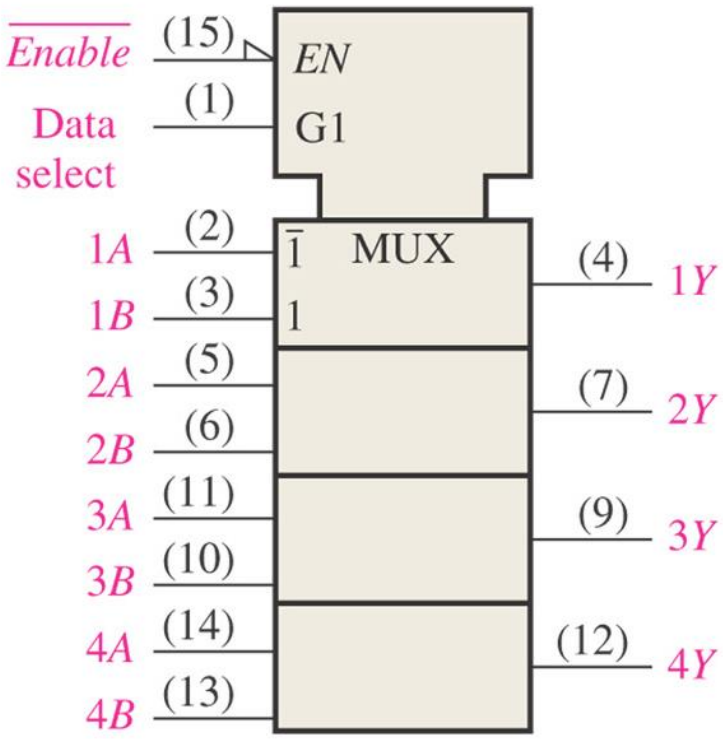


74HC157

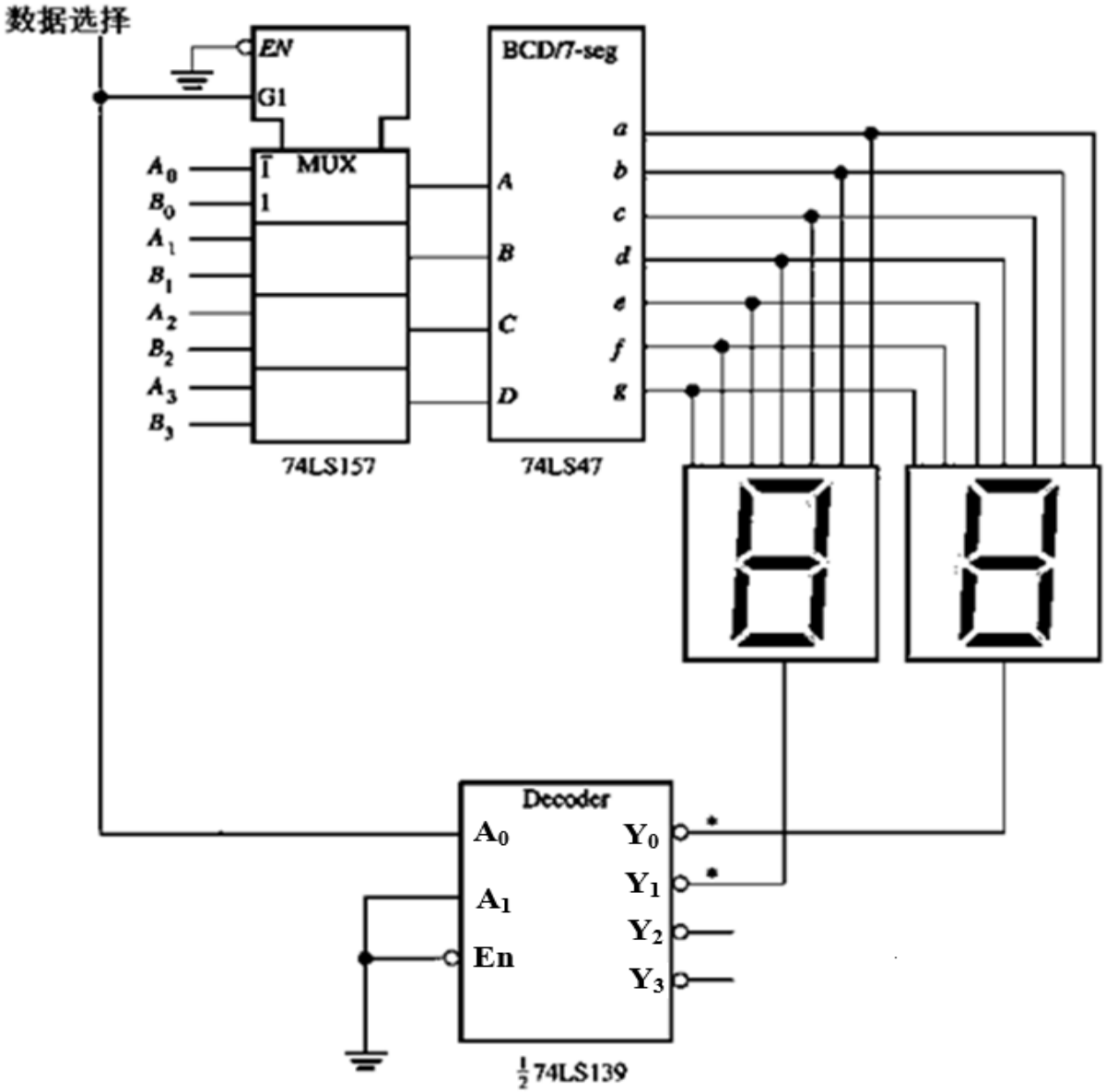
四二选一数据选择器

G1:数据选择输入端

高电平：选通数据B
低电平：选通数据A



应用举例：七段显示译码器复用电路



单选题 1分

设置

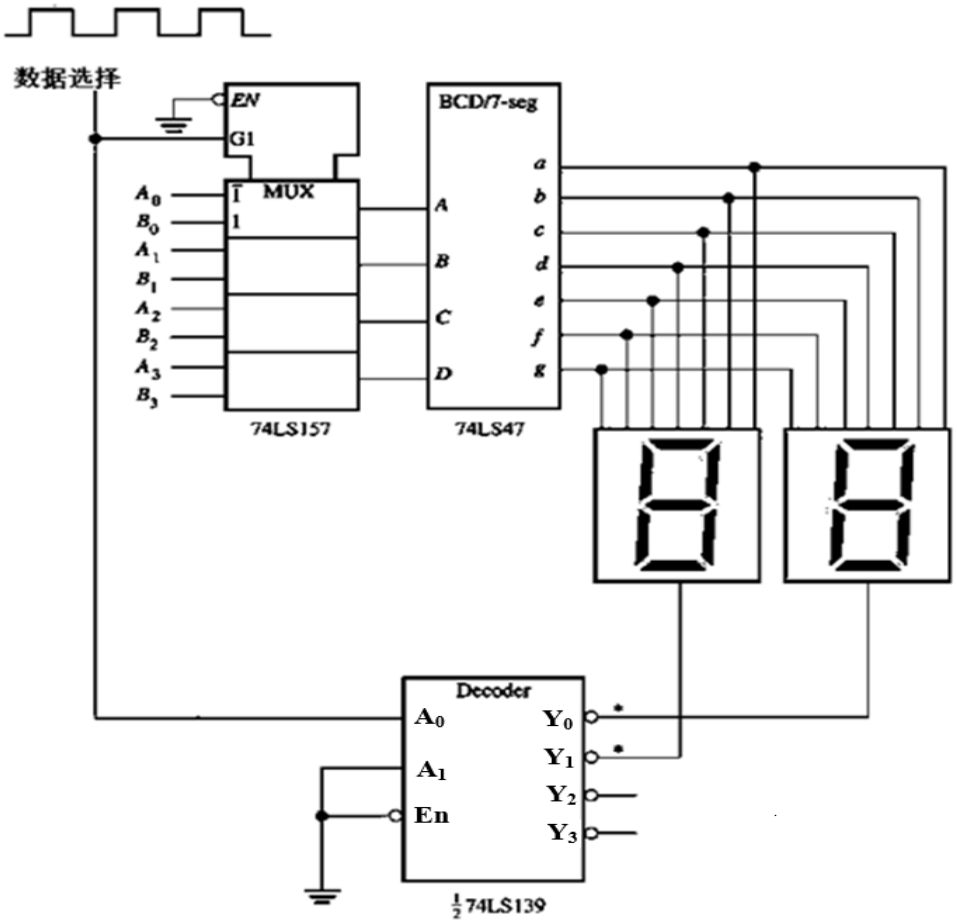
若$A_3A_2A_1A_0$=1001，$B_3B_2B_1B_0$=0001，数码管显示结果为____？

A 9

B 1

C 19

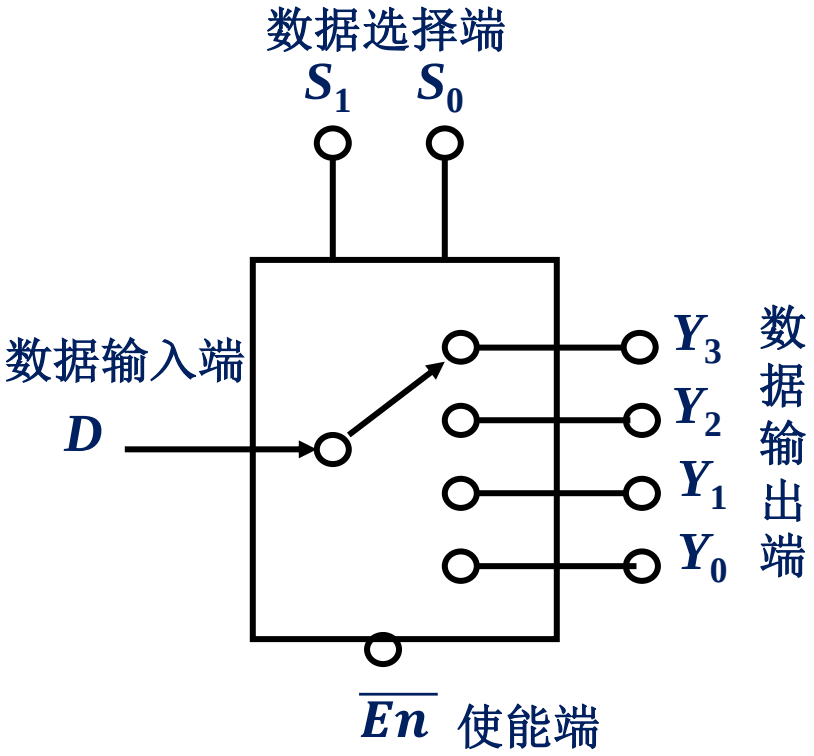
D 91



提交

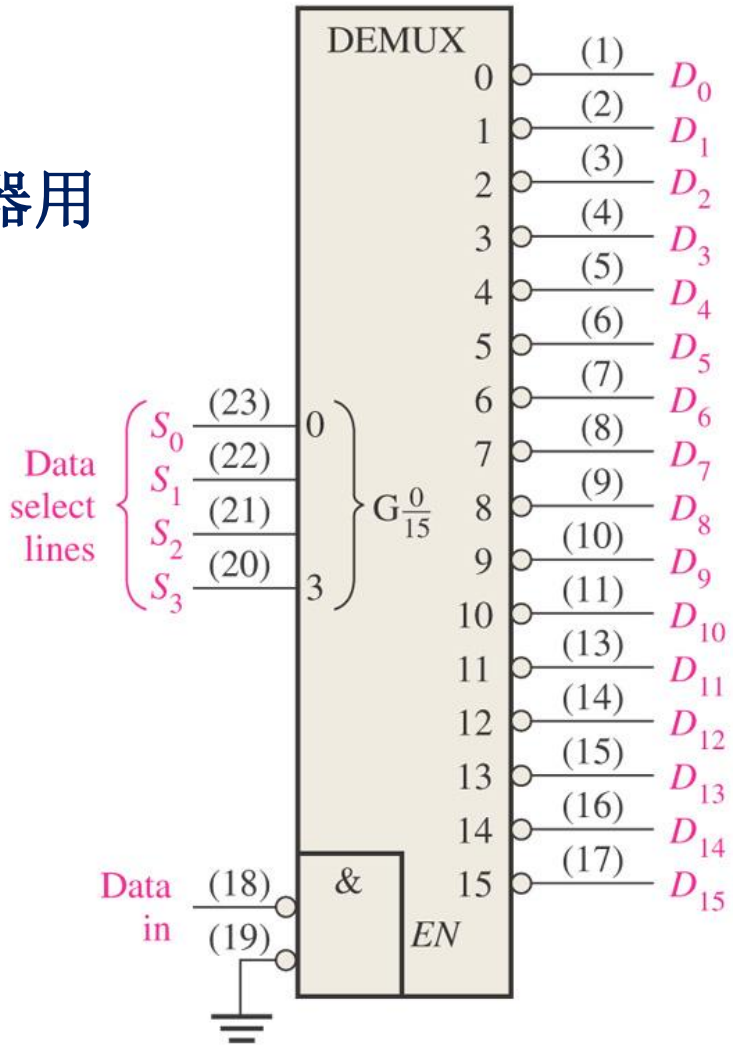
数据分配器(DeMultiplexer)

将数据分配到对应的输出端口



使能	选择端		输出端			
$\overline{EN}$	S_1	S_0	Y_3	Y_2	Y_1	Y_0
1	×	×	0	0	0	0
0	0	0	0	0	0	D
0	0	1	0	0	D	0
0	1	0	0	D	0	0
0	1	1	D	0	0	0

译码器做数据分配器用


DEMUX
Data select lines
S_0
S_1
S_2
S_3
(23)
(22)
(21)
(20)
0
3
$G\frac{0}{15}$
Data in
(18)
(19)
&
EN
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(10)
(11)
(13)
(14)
(15)
(16)
(17)
D_0
D_1
D_2
D_3
D_4
D_5
D_6
D_7
D_8
D_9
D_{10}
D_{11}
D_{12}
D_{13}
D_{14}
D_{15}

基于译码器的组合逻辑设计——重点

二进制译码器

每一项输出对应一个最小项
所有输出包含所有的最小项

输入			输出							
A	B	C	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

最小项译码器

$Y_0=\overline{A}\,\overline{B}\,\overline{C}$

$Y_1=\overline{A}\,\overline{B}C$

$Y_2=\overline{A}B\overline{C}$

⋮

$Y_7=ABC$

用来实现一般逻辑表达式！

译码器是低电平有效输出，

因此输出与最小项之间的关系为：

INPUTS			DECODING	OUTPUTS							
A_2	A_1	A_0	FUNCTION	0	1	2	3	4	5	6	7
0	0	0	$\bar{A}_2\bar{A}_1\bar{A}_0$	0	1	1	1	1	1	1	1
0	0	1	$\bar{A}_2\bar{A}_1A_0$	1	0	1	1	1	1	1	1
0	1	0	$\bar{A}_2A_1\bar{A}_0$	1	1	0	1	1	1	1	1
0	1	1	$\bar{A}_2A_1A_0$	1	1	1	0	1	1	1	1
1	0	0	$A_2\bar{A}_1\bar{A}_0$	1	1	1	1	0	1	1	1
1	0	1	$A_2\bar{A}_1A_0$	1	1	1	1	1	0	1	1
1	1	0	$A_2A_1\bar{A}_0$	1	1	1	1	1	1	0	1
1	1	1	$A_2A_1A_0$	1	1	1	1	1	1	1	0

$$\overline{Y}_i = \overline{m}_i$$

$$\overline{Y}_0 = \overline{\bar{A}_2\bar{A}_1\bar{A}_0} = \overline{m}_0$$

$$\overline{Y}_1 = \overline{\bar{A}_2\bar{A}_1A_0} = \overline{m}_1$$

$$\overline{Y}_2 = \overline{\bar{A}_2A_1\bar{A}_0} = \overline{m}_2$$

$$\overline{Y}_3 = \overline{\bar{A}_2A_1A_0} = \overline{m}_3$$

$$\overline{Y}_4 = \overline{A_2\bar{A}_1\bar{A}_0} = \overline{m}_4$$

$$\overline{Y}_5 = \overline{A_2\bar{A}_1A_0} = \overline{m}_5$$

$$\overline{Y}_6 = \overline{A_2A_1\bar{A}_0} = \overline{m}_6$$

$$\overline{Y}_7 = \overline{A_2A_1A_0} = \overline{m}_7$$

例：用译码器和门电路实现下面的组合逻辑函数

$$Z=AB+BC+CA$$

1) 选用芯片

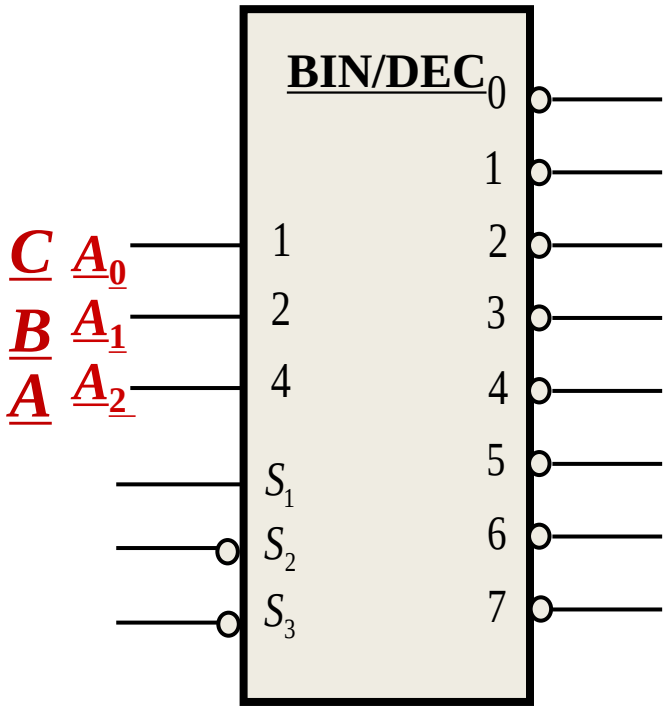
三变量函数用74LS138

2) 将表达式写成最小项形式

$$Z=\bar{A}BC+A\bar{B}C+AB\bar{C}+ABC$$

$$=m_3+m_5+m_6+m_7$$

$$=\overline{\bar{Y}_3\bar{Y}_5\bar{Y}_6\bar{Y}_7}$$



$$Z=\overline{\bar{Y}_3\bar{Y}_5\bar{Y}_6\bar{Y}_7}$$

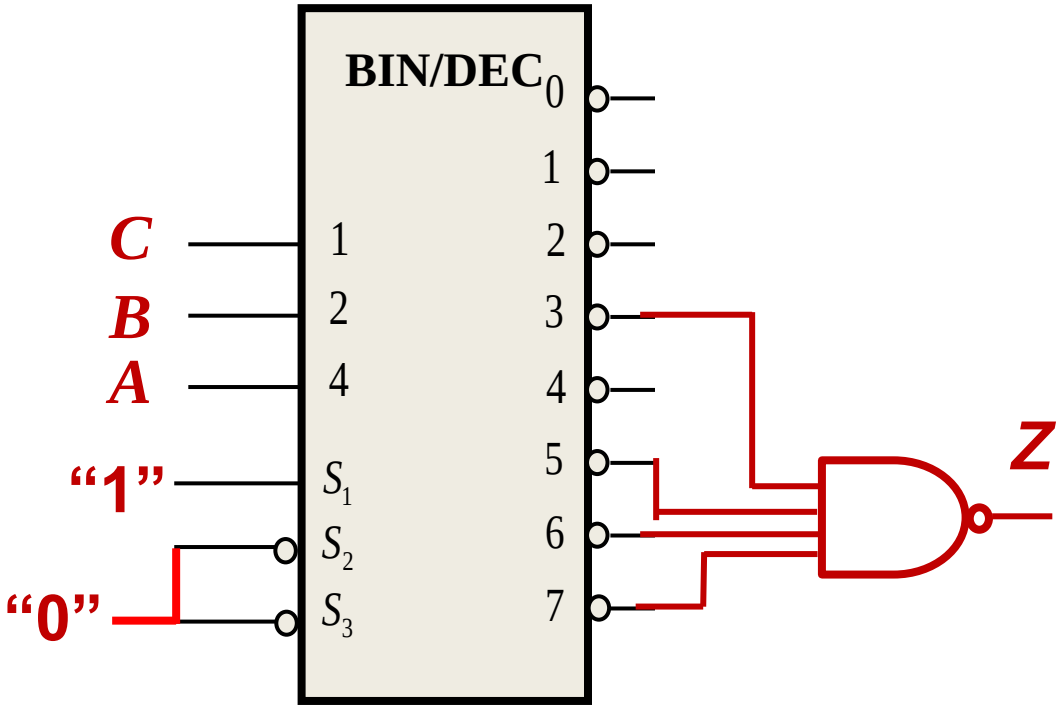
3) 画线路图

将输入变量*A,B,C*分别接到对应输入端

让使能端有效

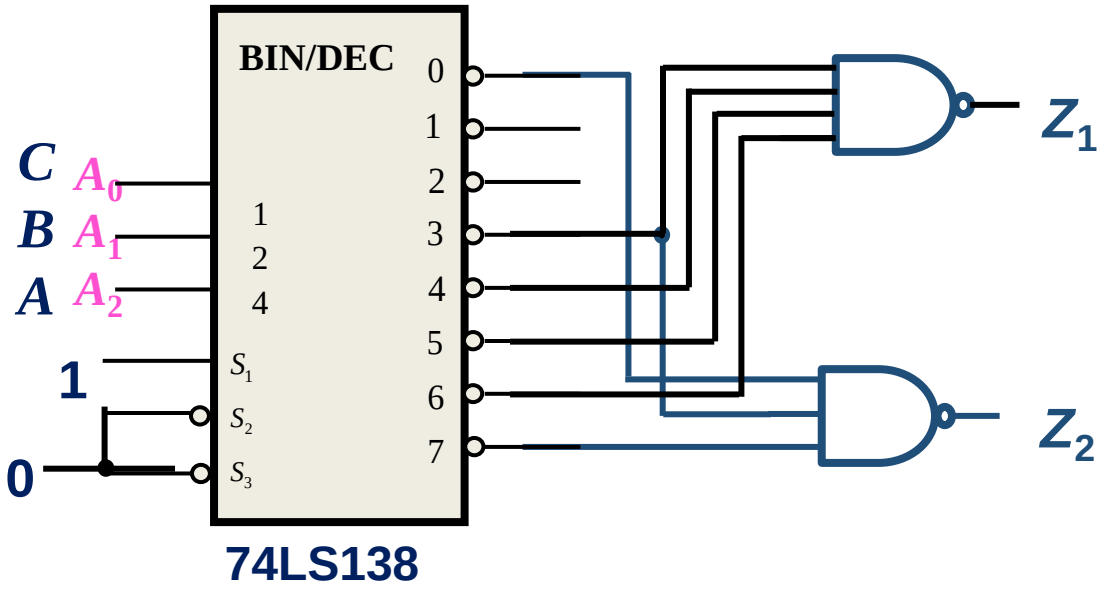
将 $\bar{Y}_3,\bar{Y}_5,\bar{Y}_6,\bar{Y}_7$

输出给与非门，与非门输出为Z，即可得到输出



注意ABC接入的高低位顺序！

练习：写出电路的逻辑关系



A \ BC	00	01	11	10
0	0	0	1	0
1	1	1	0	1

解：

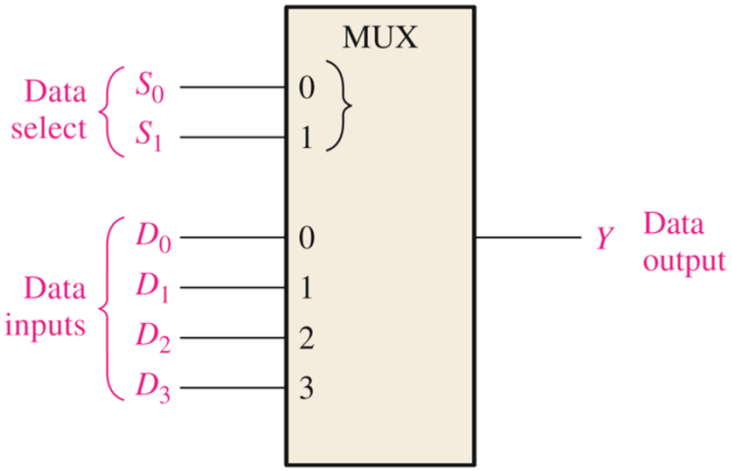
$$Z_1(A,B,C) = \overline{\bar{Y}_3\bar{Y}_4\bar{Y}_5\bar{Y}_6} = \bar{A}BC + A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C}$$

化简得 $= \bar{A}BC + A\bar{B} + A\bar{C}$

$$Z_2 = \bar{A}\bar{B}\bar{C} + \bar{A}BC + ABC = \bar{A}\bar{B}\bar{C} + BC$$

基于数据选择器的组合逻辑设计

逻辑符号



功能表

数据选择端 S_1	数据选择端 S_0	数据输出 Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

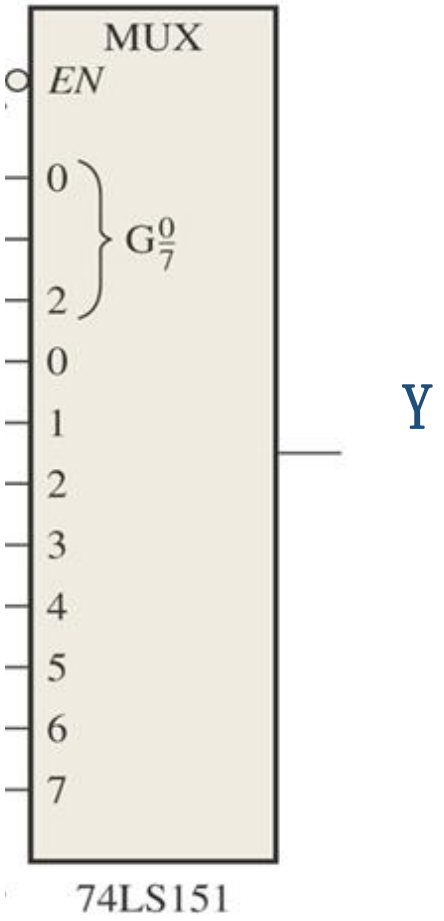
逻辑表达式 $$Y = D_0\overline{S}_1\overline{S}_0 + D_1\overline{S}_1S_0 + D_2S_1\overline{S}_0 + D_3S_1S_0$$

类似三变量函数的表达式！

举例说明基于数据选择器的组合逻辑设计

例：利用数据选择器151实现如下逻辑函数

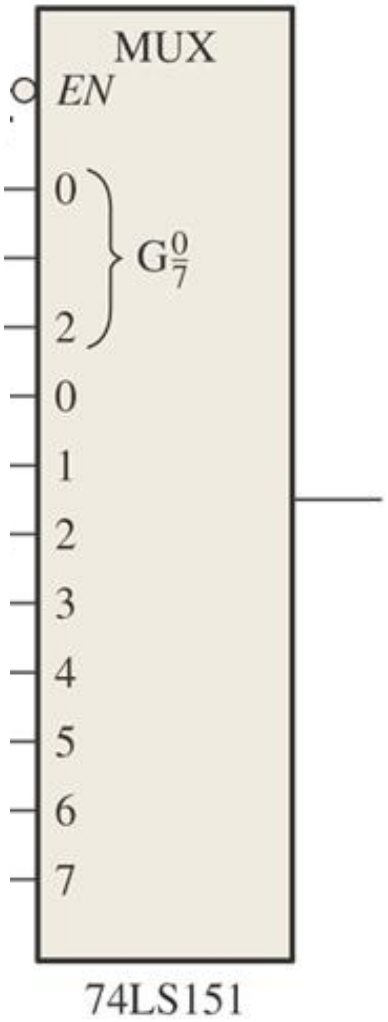
输入			输出
A_2	A_1	A_0	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0



$$Y = \bar{A}_2\bar{A}_1A_0 + \bar{A}_2A_1A_0 + A_2\bar{A}_1A_0 + A_2A_1\bar{A}_0$$

例：利用数据选择器151实现如下逻辑函数

DECIMAL DIGIT	INPUTS				OUTPUT	
	A_3	A_2	A_1	A_0	Y	
0	0	0	0	0	0	$Y=A_0$
1	0	0	0	1	1	
2	0	0	1	0	1	$Y=\overline{A}_0$
3	0	0	1	1	0	
4	0	1	0	0	0	$Y=A_0$
5	0	1	0	1	1	
6	0	1	1	0	1	$Y=1$
7	0	1	1	1	1	
8	1	0	0	0	1	$Y=\overline{A}_0$
9	1	0	0	1	0	
10	1	0	1	0	1	$Y=\overline{A}_0$
11	1	0	1	1	0	
12	1	1	0	0	1	$Y=1$
13	1	1	0	1	1	
14	1	1	1	0	0	$Y=A_0$
15	1	1	1	1	1	



$$Y=\overline{A}_3\overline{A}_2\overline{A}_1A_0+\overline{A}_3\overline{A}_2A_1\overline{A}_0+\overline{A}_3A_2\overline{A}_1A_0+\overline{A}_3A_2A_1\overline{A}_0+\overline{A}_3A_2A_1A_0+A_3\overline{A}_2\overline{A}_1\overline{A}_0+A_3\overline{A}_2A_1\overline{A}_0+A_3A_2\overline{A}_1\overline{A}_0+A_3A_2\overline{A}_1A_0+A_3A_2A_1A_0$$

第四章 作业

4.4 从波形进行组合电路设计

4.7 实际问题使用与非门组合电路设计

4.14 译码器设计

4.19 数选器设计实际问题

10月15日周五交作业