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Using Verilog and System Verilog Design and Verify the Communication Bridge between APB and I2C Protocol

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Abstract

SOC devices and circuits will consist of sub-circuits which will use different protocols, some will use serial data transmitting protocols and some will use parallel communication protocols so in this project we are presenting how to build communication between two different block which use different protocols. To build the communication bridge between these two protocols, first we designed each block separately then to make communication between these two protocols we developed bridge which consists of APB slave and I2C master blocks. Here we used Verilog Hardware description language to design the each blocks then used System Verilog to develop the Test Bench to verify the whole design, and used Model Sim tool for simulation and verifying it.

Keywords: APB, APB to I2C Bridge, FIFO, I2C, Parallel to serial communication protocols

I. INTRODUCTION

As we know the SOC system consist of different blocks operating with the different protocols so in this project one block operating using parallel communication protocol i.e. APB and serial communication protocol i.e. I2C and even their operating frequency are also different, APB is faster than the I2C protocol, so here we are building the communication bridge which supports the data transfer between APB Master and I2C slave.

APB to I2C Bridge will be a Device under Test (DUT) and APB Master Test bench (TB) will provide the stimulus to check the DUT so the signal flow will be controlled from the APB master. Here FIFO is used as the memory between the ABP slave and I2C Master Blocks. In our project we are using the System Verilog Test Bench to verify the design.

II. EXISTING METHOD

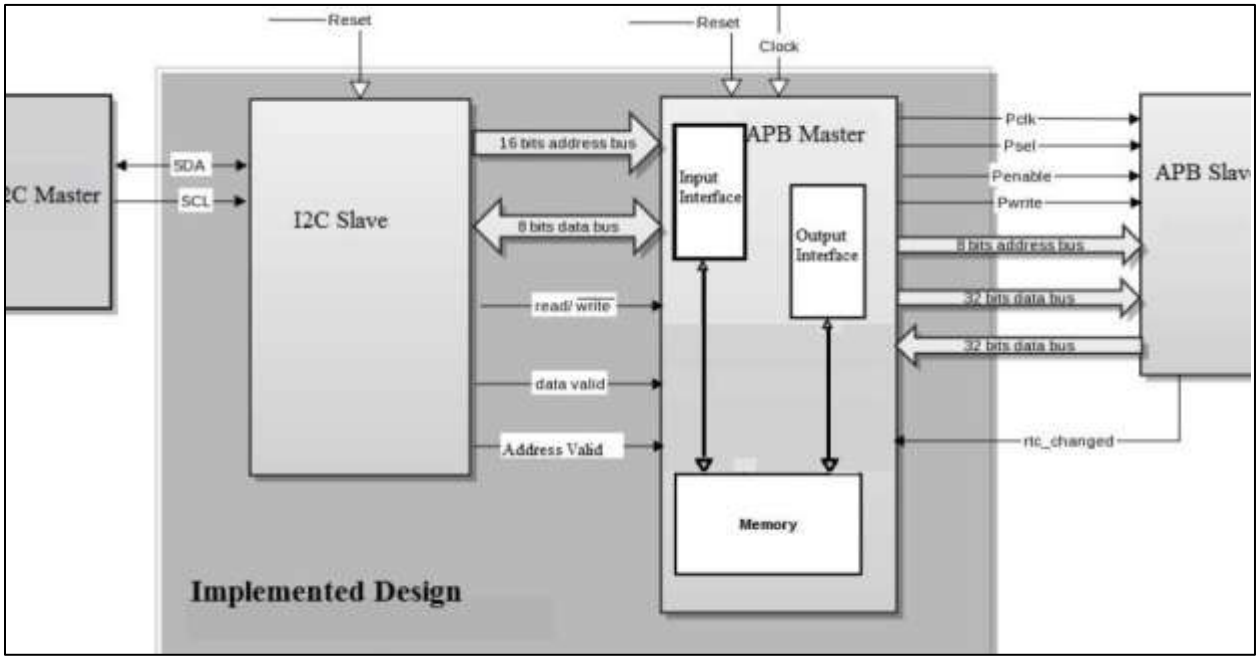

Fig. 1: Block Diagram existing method of bridge between I2C to APB protocol.

In existing method bridge consist of I2C slave and APB master so whole operation is controlled by the I2c master and they have used fifo for memory purpose but in this method they got limitation that over writing is happing while write operation so they failed to match the the speed of both protocols. So in following proposed method we have elimated this limit so speed of both protocols are matching perfectly.

III. PROPOSED METHOD

Here two main blocks which we have to concentrate are APB slave and I2C master those are the heart of project, APB Master is like Test Bench to the Design which will provide stimulus to the design. Here question is why we have to use the FIFO as we know I2C having low speed compared to APB protocol so FIFO will help to match the speed of both protocols.

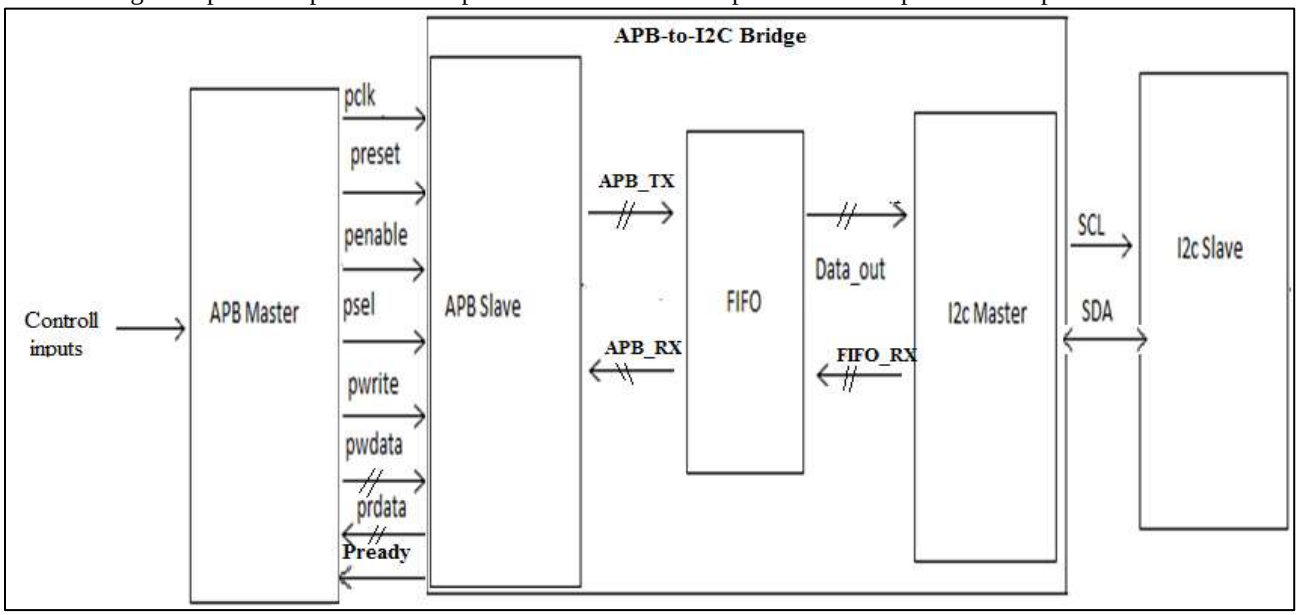

Fig. 2: Proposed method block diagram of bridge between APB to I2C

IV. OPERATION

A. Write Operation:

To write data from APB master to the I2C slave first make all enable signal of APB protocol like PENABLE, PSEL, PWRITE then the data is transferred from APB slave to FIFO. Then same data is send to the I2C master that the APB master want to write data and I2C master receive the data in parallel. Then I2C master will send the data serially to I2C slave over SDA line along with SCL clock with requested number of writes. During this phase APB and FIFO will be in idle condition.

B. Read Operation:

To read the data from the I2C slave the APB master will be made active by enabling the PENABLE, PSEL to high and PWRITE to the low so it means to APB is requesting to read data from I2C slave. Read request is sent to the I2C master, so I2C master will send the request to the I2C slave along with the address from which location data to be read, during this time APB and FIFO will be in idle mode, so now I2C master will communicate with slave to receive the data and once requested data from I2C slave is read then I2C master will send this data back to APB master through the I2C to APB bridge.

V. RESULT

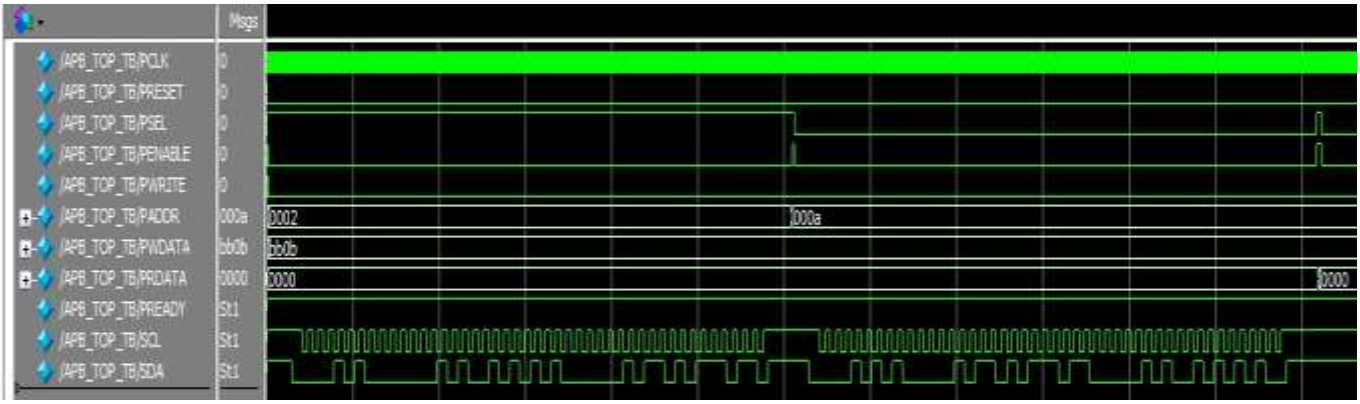

Fig. 3: Write and read operations of APB to I2C bridge

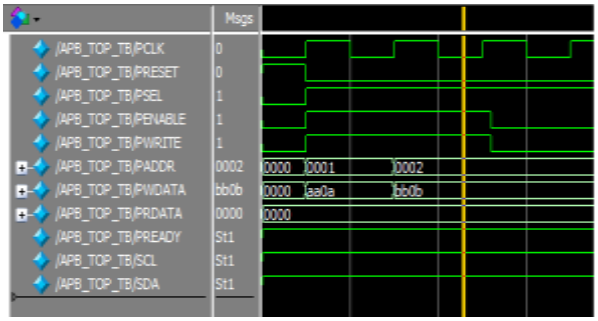

Figure 4: APB master write

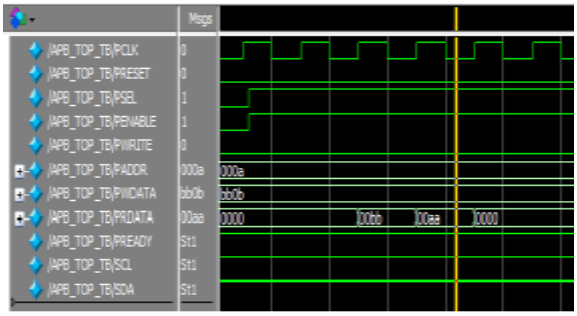

Figure 5: APB master read.

VI. CONCLUSION

By looking at the simulation result in above figures, we can conclude that the parallel pattern inputs which are given from APB master is sent on SDA line of I2C Slave, (figure 3) and again we received the serial data from I2C slave to APB master as parallel data (figure 5), that means the bridge which we built between APB-to-I2C and vice versa works good. And it is taking care of data loss and data over write from both protocols so that we are matching the speed of both the protocols.

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