Pins						Alternate functions[4]	
BGA100	LQFP64	LQFP100	Pin name	Type[1]	I / O Level[2]	Main function[3] (after reset)	Default	Remap
H2	15	24	PA1	I/O	-	PA1	USART2_RTS[7]/ ADC12_IN1/ TIM5_CH2 /TIM2_CH2[7]/ ETH_MII_RX_CLK/ ETH_RMII_REF_CLK	-
J2	16	25	PA2	I/O	-	PA2	USART2_TX[7]/ TIM5_CH3/ADC12_IN2/ TIM2_CH3[7]/ ETH_MII_MDIO/ ETH_RMII_MDIO	-
K2	17	26	PA3	I/O	-	PA3	USART2_RX[7]/ TIM5_CH4/ADC12_IN3 / TIM2_CH4[7]/ ETH_MII_COL	-
E4	18	27	V_{SS_4}	S	-	V_{SS_4}	-	-
F4	19	28	V_{DD_4}	S	-	V_{DD_4}	-	-
G3	20	29	PA4	I/O	-	PA4	SPI1_NSS[7]/DAC_OUT1 / USART2_CK[7] / ADC12_IN4	SPI3_NSS/I2S3_WS
H3	21	30	PA5	I/O	-	PA5	SPI1_SCK[7] / DAC_OUT2 / ADC12_IN5	-
J3	22	31	PA6	I/O	-	PA6	SPI1_MISO[7]/ADC12_IN6 / TIM3_CH1[7]	TIM1_BKIN
K3	23	32	PA7	I/O	-	PA7	SPI1_MOSI[7]/ADC12_IN7 / TIM3_CH2[7]/ ETH_MII_RX_DV[8]/ ETH_RMII_CRS_DV	TIM1_CH1N
G4	24	33	PC4	I/O	-	PC4	ADC12_IN14/ ETH_MII_RXD0[8]/ ETH_RMII_RXD0	-
H4	25	34	PC5	I/O	-	PC5	ADC12_IN15/ ETH_MII_RXD1[8]/ ETH_RMII_RXD1	-
J4	26	35	PB0	I/O	-	PB0	ADC12_IN8/TIM3_CH3/ ETH_MII_RXD2[8]	TIM1_CH2N
K4	27	36	PB1	I/O	-	PB1	ADC12_IN9/TIM3_CH4[7]/ ETH_MII_RXD3[8]	TIM1_CH3N
G5	28	37	PB2	I/O	FT	PB2/BOOT1	-	-
H5	-	38	PE7	I/O	FT	PE7	-	TIM1_ETR
J5	-	39	PE8	I/O	FT	PE8	-	TIM1_CH1N