Bilkent University

Department of Electrical and Electronical Engineering

EEE 313

Electronic Circuit Design

Analog Multiplier

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Section 2

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Introduction

This term project aimed to explore the practical applications of BJTs covered in lectures by creating, simulating, and executing an analog multiplier. Our approach involved proficiently utilizing LTSpice for simulations and implementing the hardware on a breadboard to bring our designs to life.

In line with the project assignment, we employed a Gilbert's Cell approach, specifying three overall differential pairs to achieve the desired circuitry. The design constraints were determined based on assumptions, ensuring that the differential pairs remained in the forward active region for efficient operation [1]. Additionally, various circuit components were selected to maintain this operational state.

Our research on analog multiplier principles and design led us to the conclusion that a Gilbert cell was essential for acquiring the desired circuitry outlined in the project assignment. The core of our circuit utilized a differential amplifier with a common emitter for its two BJTs. This configuration evenly split the voltage in the common emitter between both transistors, eliminating any voltage difference between their bases and resulting in matched collector voltages.

Introducing a small voltage difference between the emitter sides of the two transistors induced oscillations and subsequent voltage differences between the collector voltages. Building on this foundational understanding, we explored the gain in a differential amplifier, directly correlating with the collector current.

Moving from individual components to circuit construction, we connected another differential amplifier to the existing one. This combined circuit had the capability to sum the two inputs, with all four transistors matched, and the output taken from the collectors of the first and fourth transistors.

By adding a final differential pair, sharing a common base voltage, to the tails of the two sets of transistors, we achieved biasing and ensured all transistors remained in the forward active region. This addition shifted the dependence of the circuit's output voltage beyond the voltage difference between the bases of the transistors in each differential amplifier. The overall circuitry can be observed in Figure 1.

Simulation

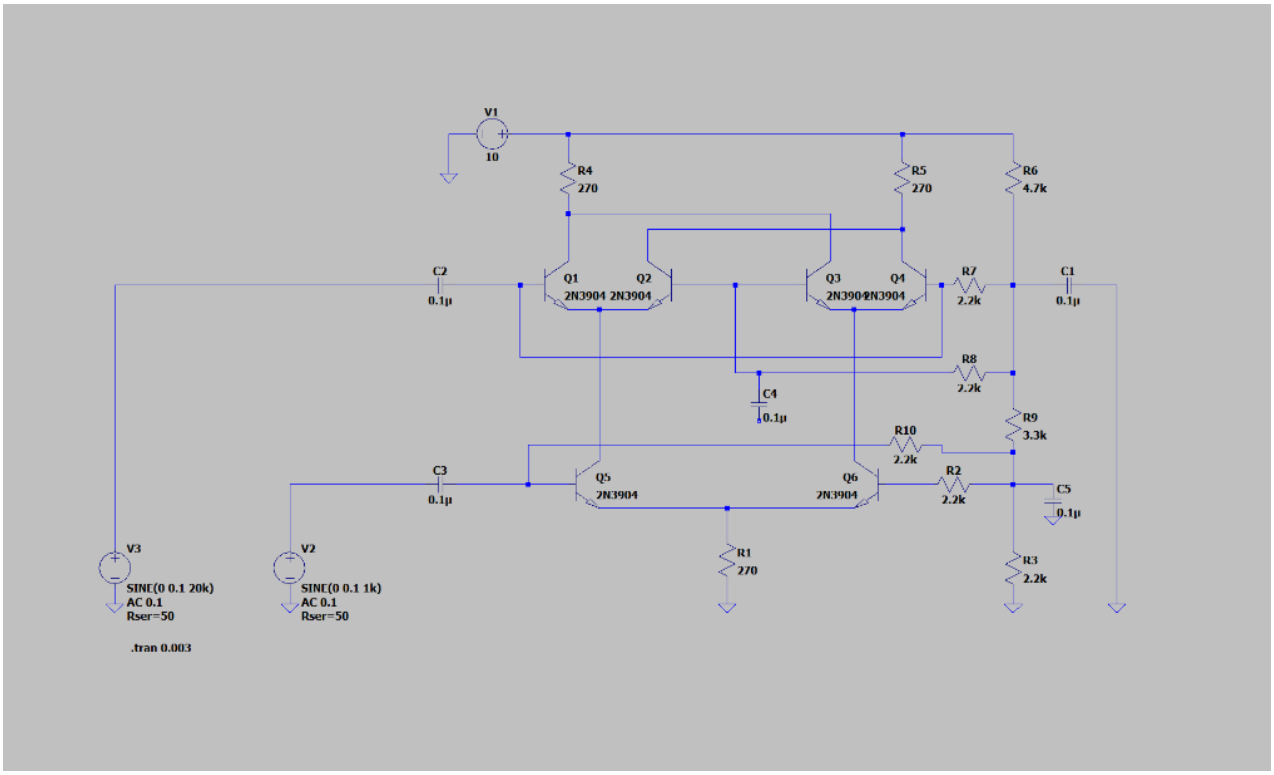

Figure 1 Software implementation of the circuit

The circuit is implemented as depicted in the introduction part by using 2N3904 transistors. From the following figure DC node voltages of the analog multiplier circuit can be observed. The aim is to observe DC operating points of the transistors and decide whether the values are satisfying the desired transistor states.

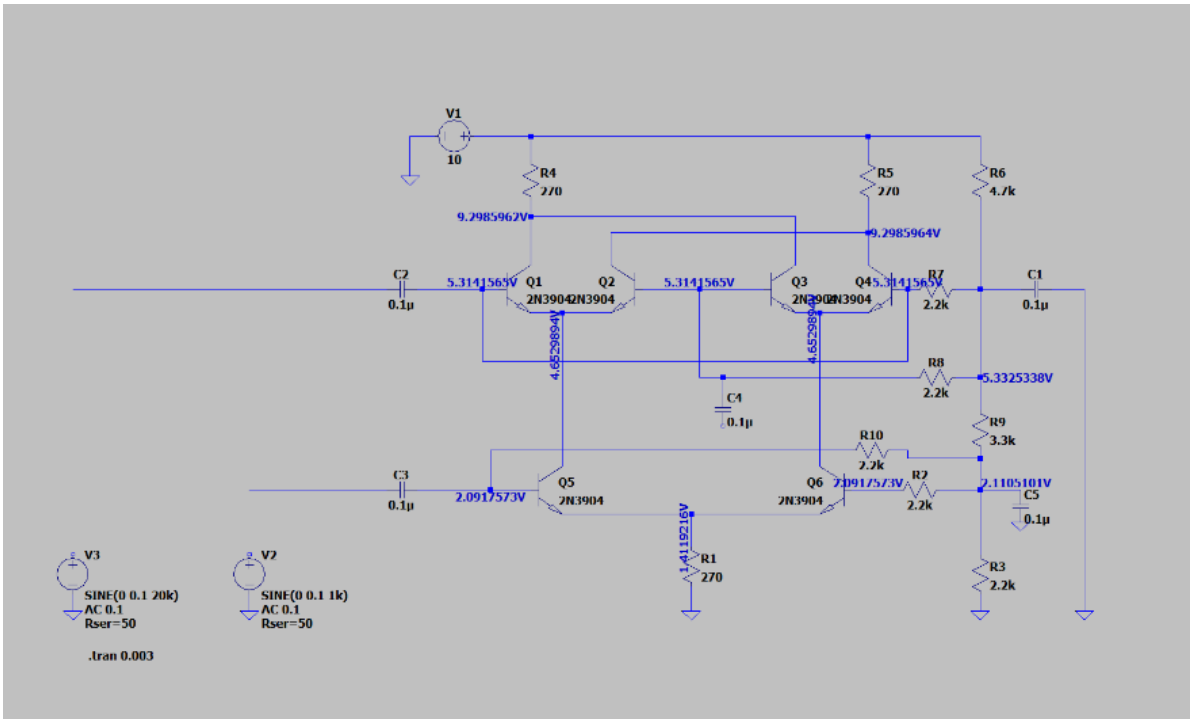

Figure 2 DC node voltages of the circuit

Regarding 2N3904 transistors, base to emitter and collecter to emitter potential differences are $V_{BE} = [0.6V, 0.7V]$ and $V_{CE} \geq 0.2V$. As it can be observed V_{CE} and V_{BE} values for all transistors satisfy the SAT condition for the transistors hence it can be concluded as DC biasing of the circuit is as desired. Now output of the analog multiplier will be tested using LTSpice simulation.

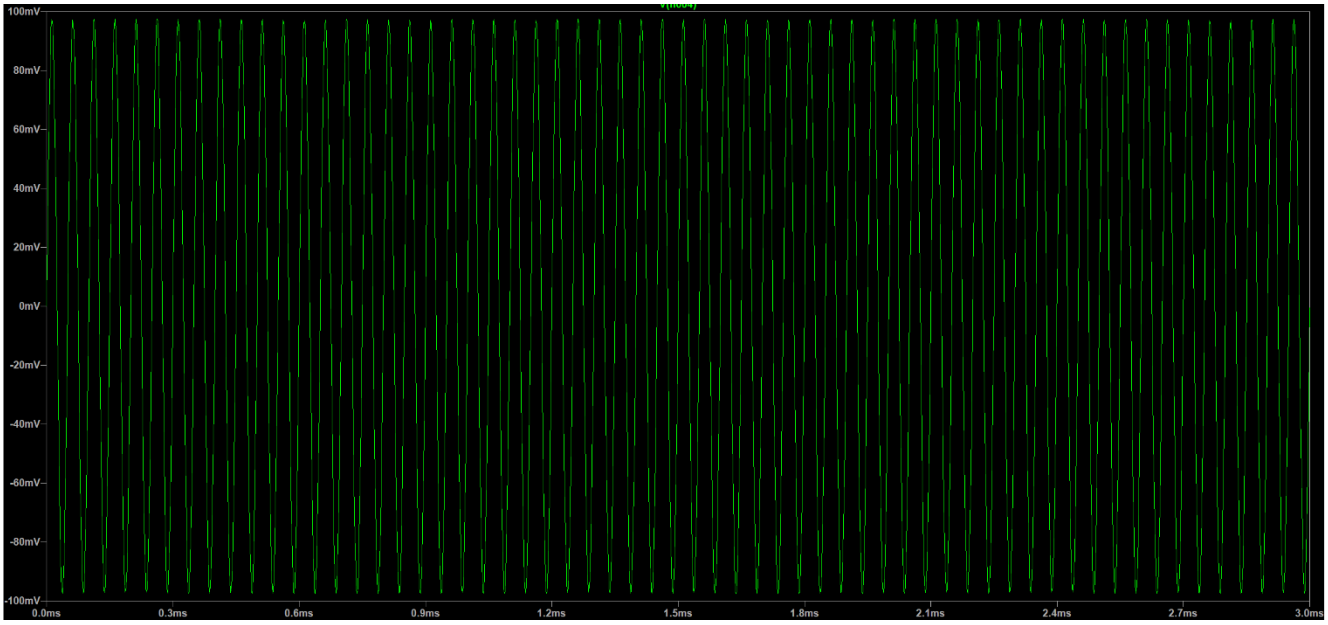

Figure 3 20kHz input

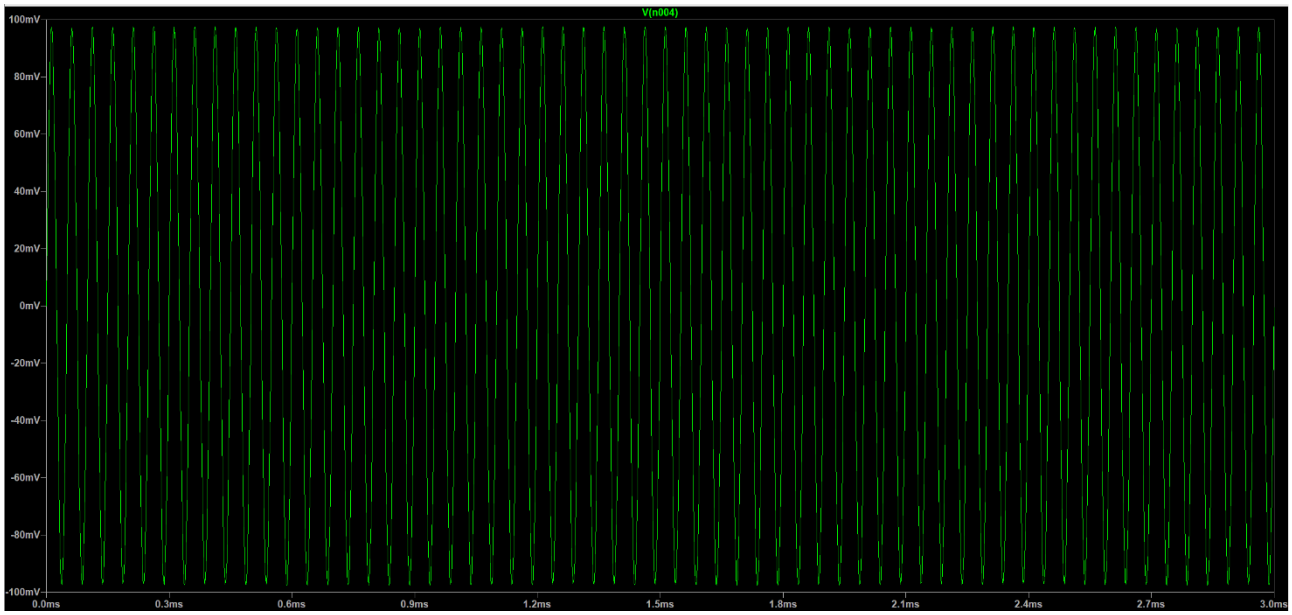

Figure 4 1kHz input

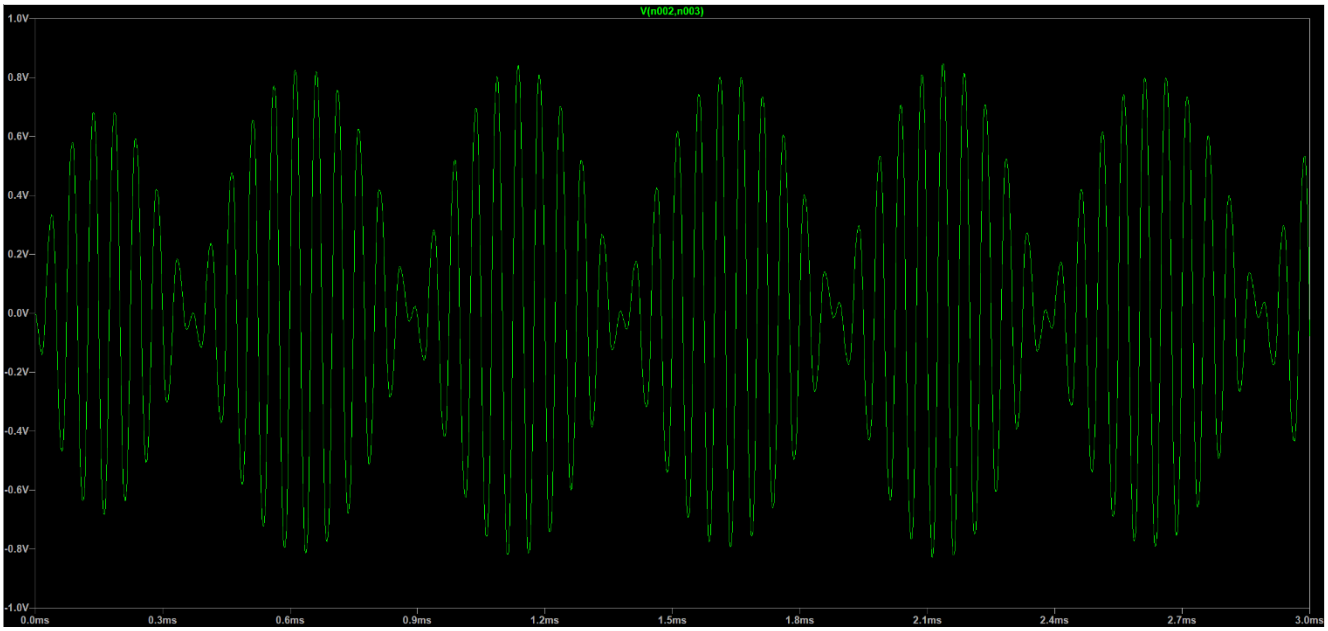

Figure 4 output of the circuit

It is important to highlight that output is the potential difference between the collectors of transistors which belong to one upper differential pair. Frequency of the output is determined by the higher frequency input(compare with Figure 12).

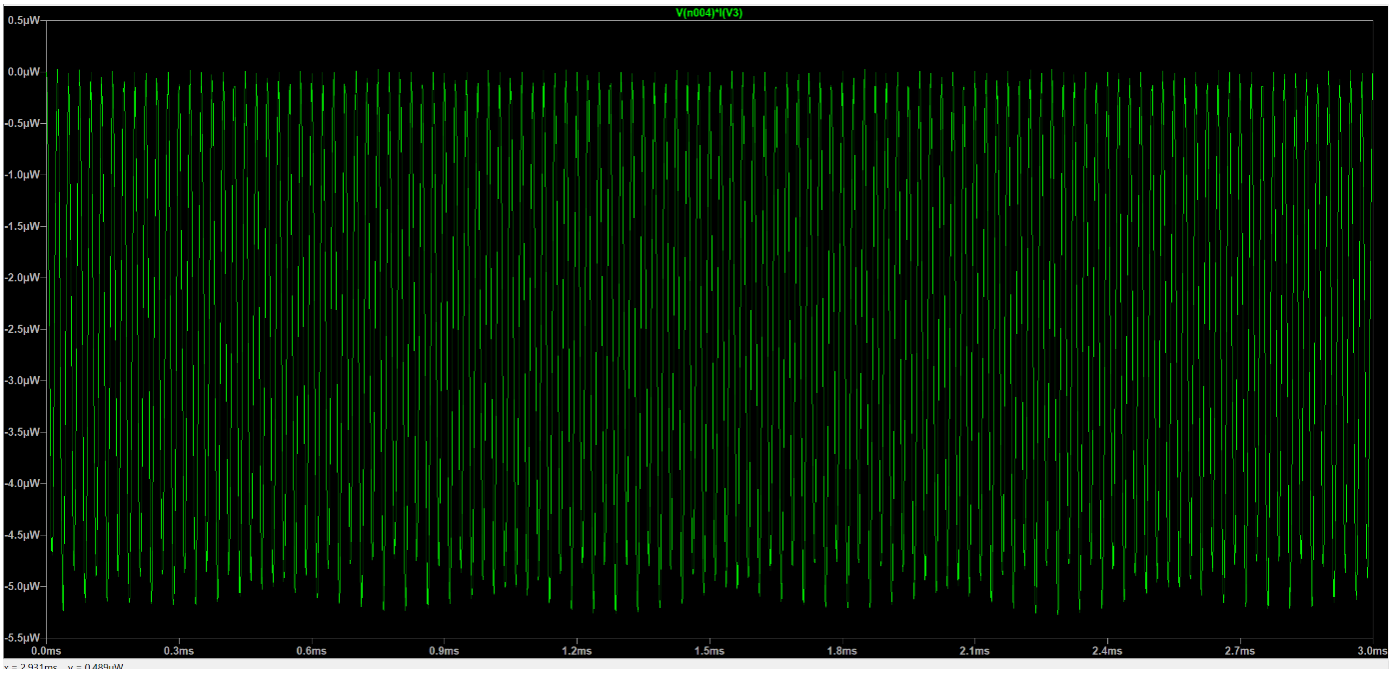

Figure 5 power consumption of 20Khz source

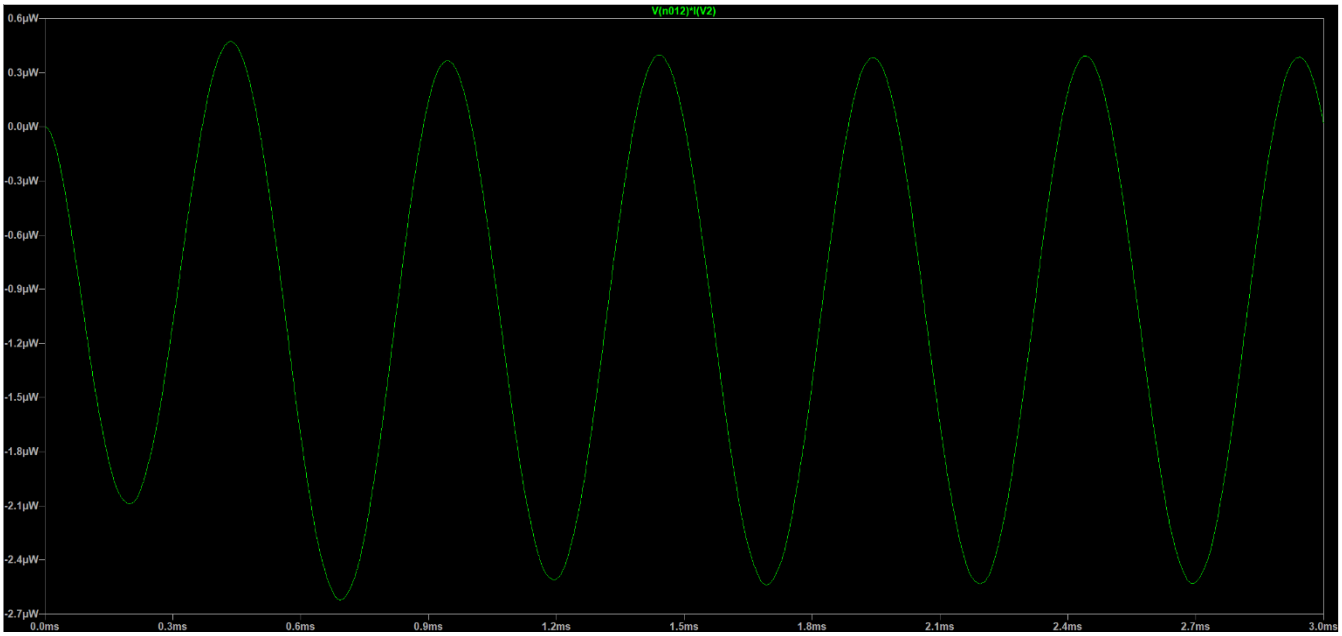

Figure 6 power consumption of 1kHz surce

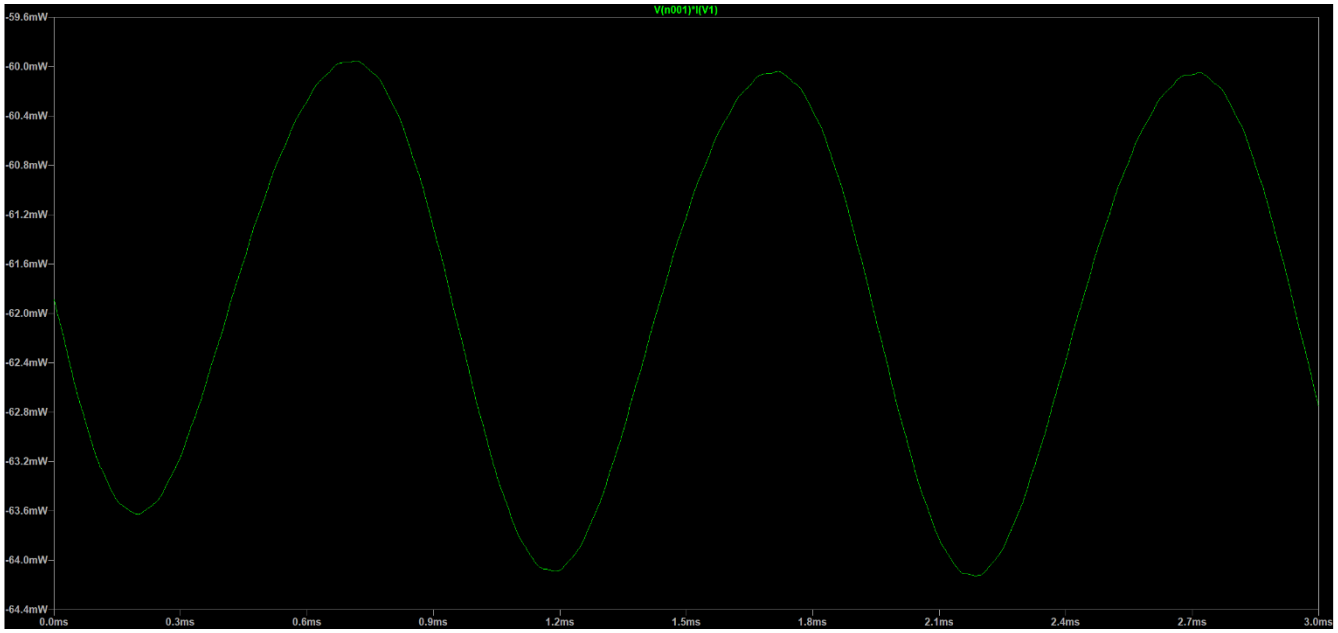

Figure 7 power consumption of 10V source

Power consumption of all 3 sources are less than the specified upper bound which is 200mW.

The software simulation and analysis indicate that the analog multiplier circuit meets with the requirements and the circuit will be implemented on breadboard and tested in hardware terms.

Hardware Implemetation and Analysis

The hardware implementation of the circuit is given in the Figure 3.

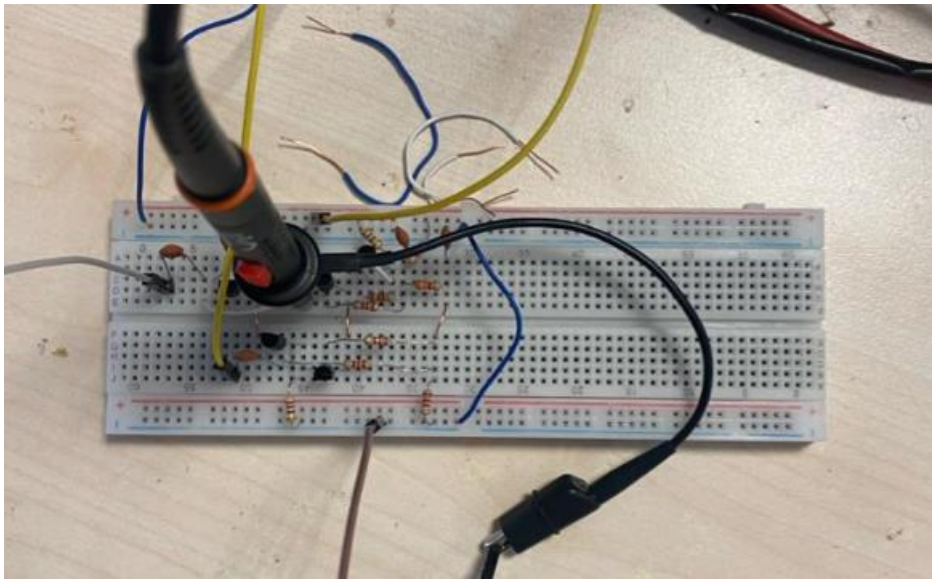

Figure 8 Breadboard Implementation

After the implementation with the chosen constraints that are found from the simulation, oscilloscope probe is connected to measure the exact output, which is taken from the first and forth transistors' collectors. Input signals are given as 0.1 Volts peak to peak for each input and the frequencies are chosen as 1kHz and 20kHz. The output waveform that aligns with simulation is given in Figure 4.

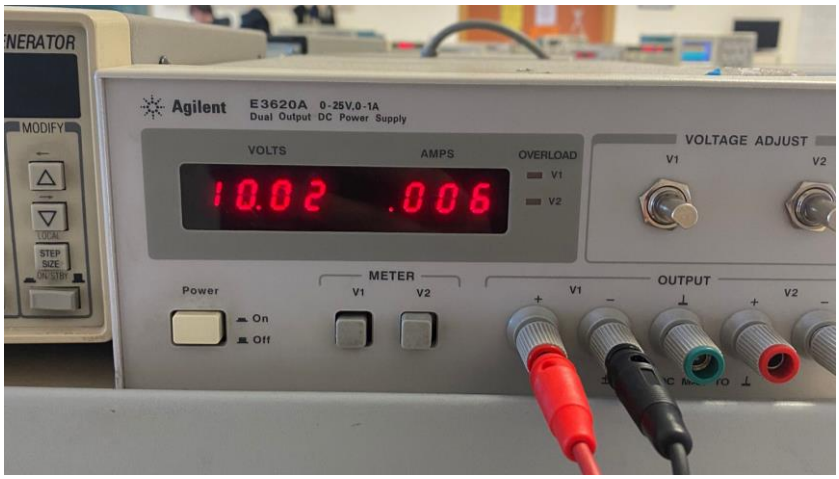

Figure 9 60 mW power consumption

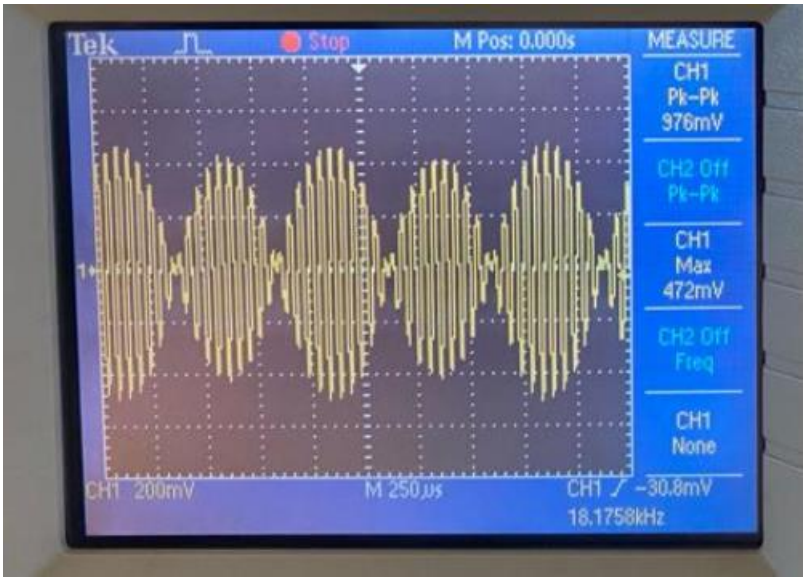

Figure 10 Output Waveform

As it can be observed from Figure 4, the output waveform is the multiplication of both signals, the main envelope is the 1kHz signal and the high frequency, (20kHz) signal oscillates between it. The peak to peak voltage is 976mV which closely aligns with the simulation.

The period and frequency of each input signal is observed trough setting time cursors in the oscilloscope and is conducted in Figures 5 and 6.

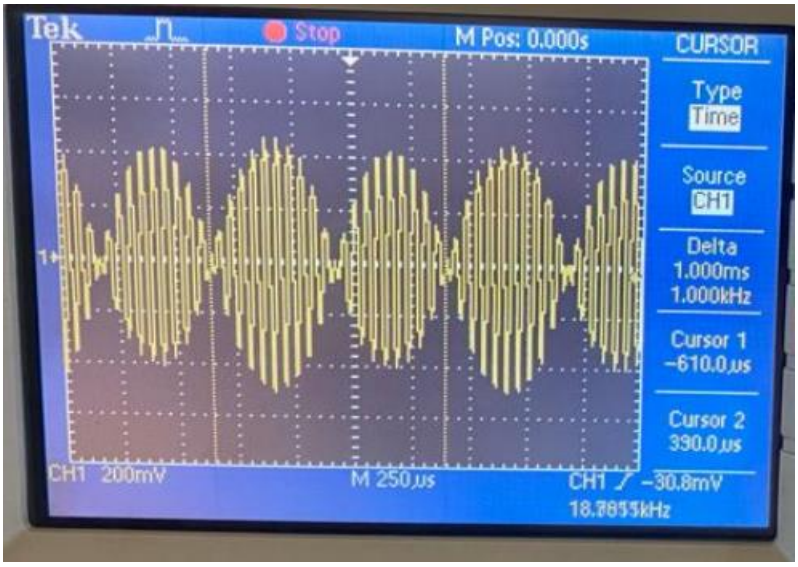

Figure 11 Frequency of the Envelope

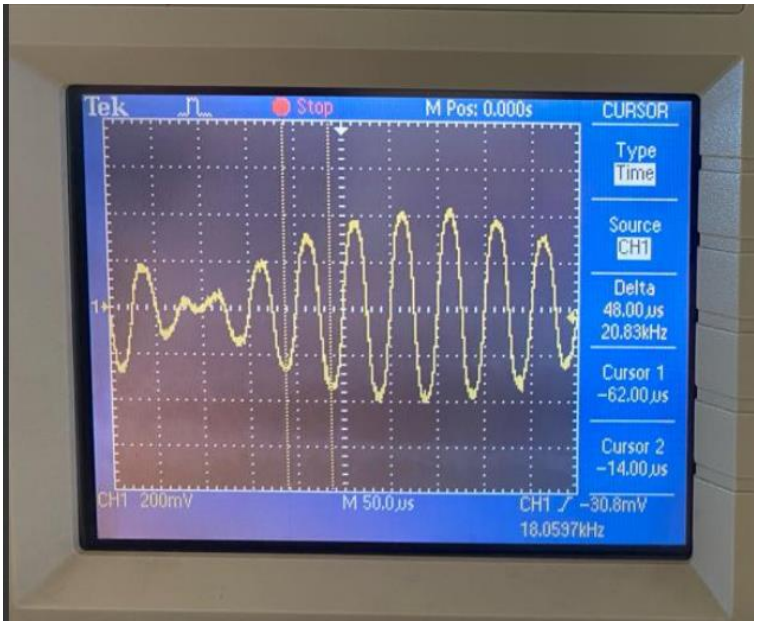

Figure 12 Frequency of the second input

After these observations, the FT of the signal is observed from the math menu to get an idea about the frequency analysis of the signal. It is given in Figure 7 such that in the frequency domain the frequencies 19kHz and 21kHz are more dominant than the 20kHz signal. This is because of the sifting property of the impulse when convolved in frequency domain.

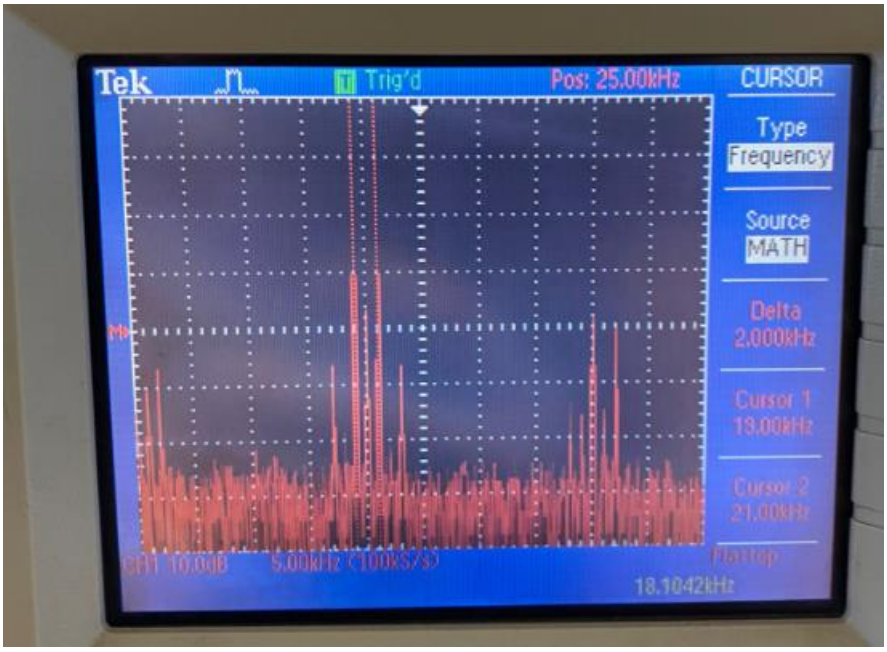

Figure 13 FFT of the output

As it can be observed from Figure 7, since our output signal is the multiplication of two sinusoids one at 1kHz frequency and the other at 20kHz frequency, they are the convolution of the Fourier transforms of these signals. It can be seen from Figure 8 that this is the expected magnitude, frequency graph of the output.

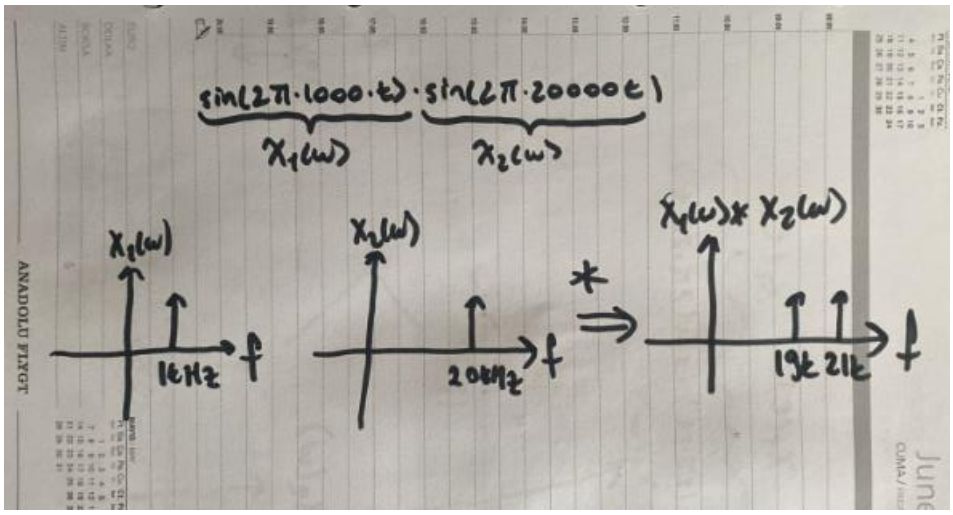

Figure 14 the idea behind 19kHz and 21kHz freq. components

Conclusion

In conclusion, our term project on designing and implementing an analog multiplier has been a comprehensive exploration of electronic circuit design, specifically focusing on the application of bipolar junction transistors (BJTs) and the utilization of a Gilbert cell approach. The project involved simulations using LTSpice, translating theoretical concepts into a practical breadboard implementation.

Our research and analysis led us to recognize the significance of a Gilbert cell in achieving the desired circuitry, with a central role played by the differential amplifier. This component, operating with a common emitter for its two BJTs, showcased the principles of equal voltage distribution, resulting in matched collector voltages when the two bases are connected to the same voltage.

The oscillations introduced by a small voltage difference between the emitter sides of the transistors illuminated the dynamic behavior of the circuit. Understanding the gain in the differential amplifier, which directly correlates with the collector current, was crucial in the transition from individual components to the construction of the overall circuit.

The implementation on a breadboard, depicted in Figure 3, validated our simulations. The observed output waveform, depicted in Figure 4, demonstrated the successful multiplication of signals, with a peak-to-peak voltage close to the simulation results. Frequency analysis, illustrated in Figures 5, 6, 7, and 8, provided insights into the characteristics of the signal in both time and frequency domains.

Despite the challenges we faced in breadboard implementation such as connectivity problems and finding components with exact values in the lab, our project achieved a meaningful and insightful exploration of analog multiplier design. The alignment between

simulation and hardware implementation serves as a testament to the accuracy of our chosen constraints and design decisions.

In essence, this project has not only deepened our understanding of analog multiplier circuits but also enhanced our practical skills in electronic circuit design. We appreciate the guidance of our course instructor, Erdinç Tatar, and look forward to applying the knowledge gained in future endeavors in the field of electrical and electronic engineering.