EEE415 Spring 2024/25 Homework 3

This report consists of two parts, in the first part the design proces of the amplifier is provided by focusing on theoratical background, schematic implmeentation and simulation. In the second part layout of the amplifier is designed and DRC, LVS simulations are performed.

Part 1

It is desired to implement an cascode amplifier with pmos loads. We are given a gain bandwidth spec, also it is desired to centert the output voltage around 0.9V Moreover, only one DC voltage souce is permittedd which is fixed to 750mV with the 50µA current flowing through the amplifier branch as provided in the intstructions. The design is initialized by aiming to center the voltrage at 0.9V.

Centering the output around 0.9V is achieved by building the amplifier branch from bottom to top. For if Figure 1 is taken as the reference, for the initial step a 0.45V test voltage is applied to drain of M0 and the width of the transistor is determined by sweeping width with respect to ids and the width that intersects witht the 50Ua is selected as the width of the related transistor. This porcess is carried out until vdd node is reached, in other words in the design the source of M1, M2, M3 are determined to be 0.45V, 0.9V, 1.35V respectively. The test biasing voltages are applied according to the SAT conditions of the transistors. The finalized values for biasing voltages can be observed accordingly.

$$V_{G_3} > 1.35V - |V_{tp}|$$

$$V_{G_2} > 0.9V - |V_{tp}|$$

$$0.9V + V_{th} > V_{G_1}$$

$$V_{S_1} + V_{th} > 0.75V$$

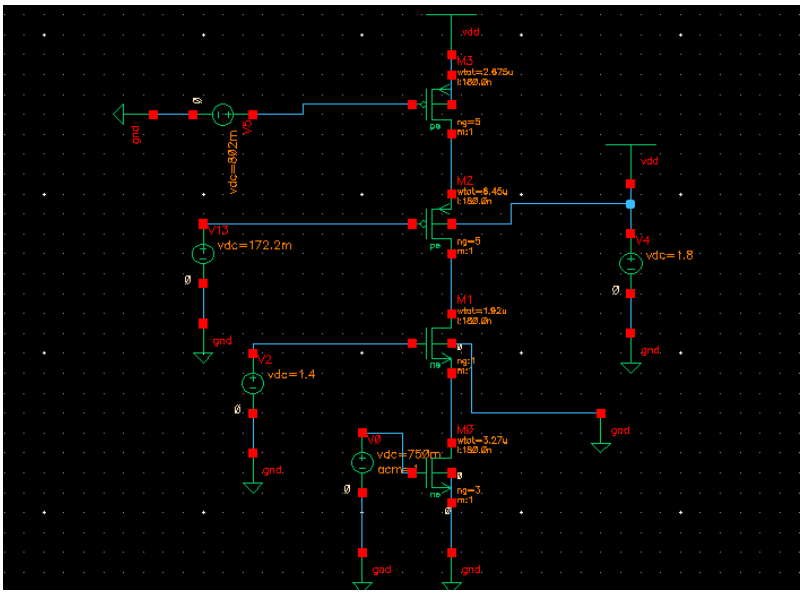

Figure 1 Test circuit schematic for biasing

In order to obtain the biasing voltages a biasing network should be created. For three bias voltages three different branch with the same reference current (10µA) is implemented. For the biasing branches different and appropriate biasing topologies are implemented (for instance low voltage cascode) and size of the transistors are determined by sweeping with respect to the voltage value. In Figure 2, it can be observed that the biasing voltages are successfuly obtained with centered output voltage of 825mV. DC operating points of the transistors are also provided in which ids and other transistor parameters can be observed.

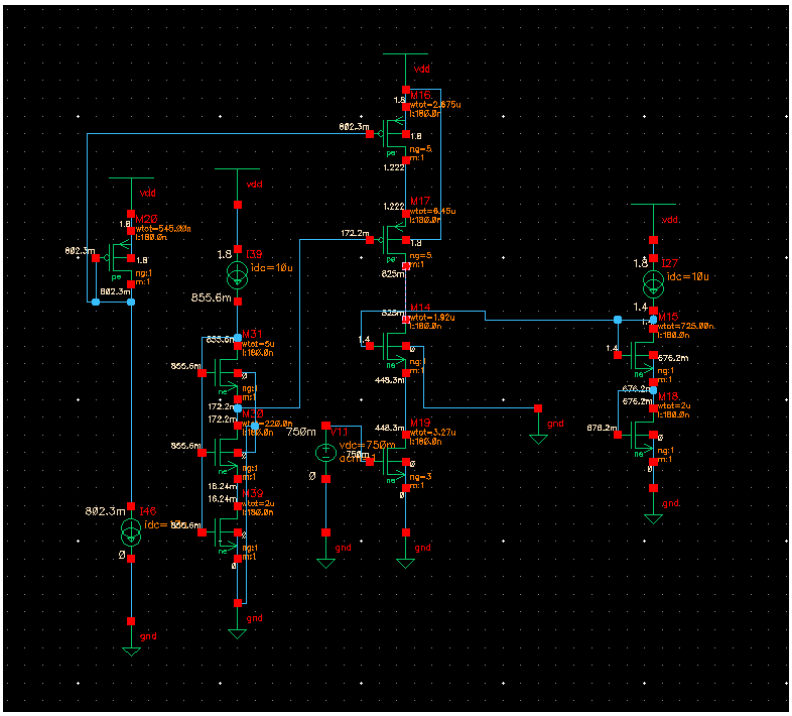

Figure 2 Complete schematic for the amplifier

string	OP("/M17" "??")
gds	12.14u
gm	394u
id	-46.57u
ids	-46.57u
isub	-1.748a
ron	8.526K
vbs	578m
vds	-397m
vdsat	-204.3m
vgs	-1.05
vth	-852.4m
signal	OP("M17.m1" "??")
beff	2.389m
betaeff	2.269m
cbb	14.04f
cbd	-5.24f
cbdbi	-2.087a
cbg	-1.582f
cbs	-7.22f
cbsbi	-1.462f
cdb	-5.254f
cdd	7.337f
cddbi	34.82a
cdg	-2.111f
cds	27.48a
cgb	-956.2a
cgbovl	0
cgd	-2.031f
cgdbi	32.61a
cgdovl	2.064f
cgg	11.98f
cggbi	7.85f

string	OP("/M16" "??")
gds	6.999u
gm	222.6u
id	-46.57u
ids	-46.57u
isub	-2.365a
ron	12.41K
vbs	0
vds	-578m
vdsat	-315.3m
vgs	-997.7m
vth	-617.3m
signal	OP("M16.m1" "??")
beff	643.4u
betaeff	765.9u
cbb	7.174f
cbd	-2.547f
cbdbi	-2.743a
cbg	-749a
cbs	-3.878f
cbsbi	-765.5a
cdb	-2.549f
cdd	3.412f
cddbi	11.8a
cdg	-868.2a
cds	5.221a
cgb	-409.5a
cgbovl	0
cgd	-853.4a
cgdbi	2.551a
cgdovl	856a
cgg	5.123f
cggbi	3.411f

Figure 3 DC operating points for pmos transistors

string	OP("/M14" "??")
gds	21.97u
gm	422.6u
id	46.57u
ids	46.57u
isub	467.1a
ron	8.09K
vbs	-448.3m
vds	376.7m
vdsat	138.1m
vgs	951.7m
vth	801.2m
signal	OP("M14.m1" "??")
beff	4.109m
betaeff	3.992m
cbb	5.306f
cbd	-2.094f
cbdbi	5.657a
cbg	-475.4a
cbs	-2.737f
cbsbi	-429.5a
cdb	-2.103f
cdd	2.741f
cddbi	7.137a
cdg	-645.2a
cds	7.713a
cgb	-410.3a
cgbovl	0
cgd	-601.4a
cgdbi	32.19a
cgdovl	633.6a
cgg	3.489f
cggbi	2.222f
cgs	2.478f

string	OP("/M19" "??")
gds	17.71u
gm	515.9u
id	46.57u
ids	46.57u
isub	559.4a
ron	9.627K
vbs	0
vds	448.3m
vdsat	113.7m
vgs	750m
vth	642.5m
signal	OP("M19.m1" "??")
beff	8.065m
betaeff	6.189m
cbb	9.053f
cbd	-3.351f
cbdbi	12.42a
cbg	-866.7a
cbs	-4.835f
cbsbi	-921.3a
cdb	-3.368f
cdd	4.447f
cddbi	4.341a
cdg	-1.09f
cds	9.957a
cgb	-755.8a
cgbovl	0
cgd	-1.036f
cgdbi	42.98a
cgdovl	1.079f
cgg	5.84f
cggbi	3.682f
cgs	4.048f

Figure 4 DC operating points for nmos transistors

The gain of this amplifier can be obtained as following. In the notation transistor numbers in Figure 2 should be considered.

$$A_v = -G_M R_{out}$$

$$A_v \approx -g_{m_{19}}(g_{m_{17}} r_{0_{17}} r_{0_{16}} || g_{m_{14}} r_{0_{14}} r_{0_{19}})$$

$$g_m = \sqrt{2 I_D \frac{W}{L} \mu C_{ox}}$$

Since minimum length transistors are used and current across the amplifier branch is constant gain is majorly dependent on the width of M17, M14, and M19. The cascode topolgy performs well in high level frequencies, however the design is implemented by being aware of the device capacitances, as width of the devices increase we obtain large gain as far as SAT conditions are satisfied, however this comes with the bandwith. Increase in device widths increase the device capacitance which results in the increase in time constant and decrease in the value of dominant pole in terms of frequency. This shrinks the BW of the amplifier. With the awarness of the gain-BW product the device widths are kept in a moderate range and the gain and BW can be observed in the following figures. The input voltage is 1V AC magnitude with 750mV DC magnitude. The maximum gain is found out to be 598.2282 which has a -3dB value of 423.24V. The gain of the designed amplifier is above 500 and the BW is 11.9645MHz which satisfies the gain-BW criteria.

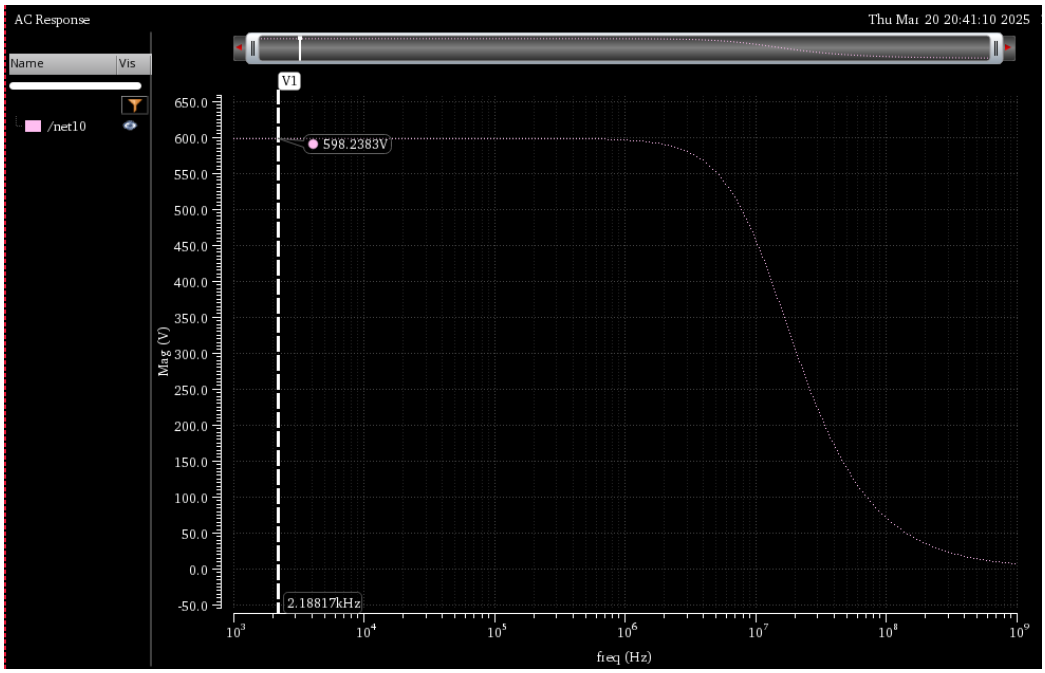

Figure 5 Gain of the amplifier with 1V AC magnitude input

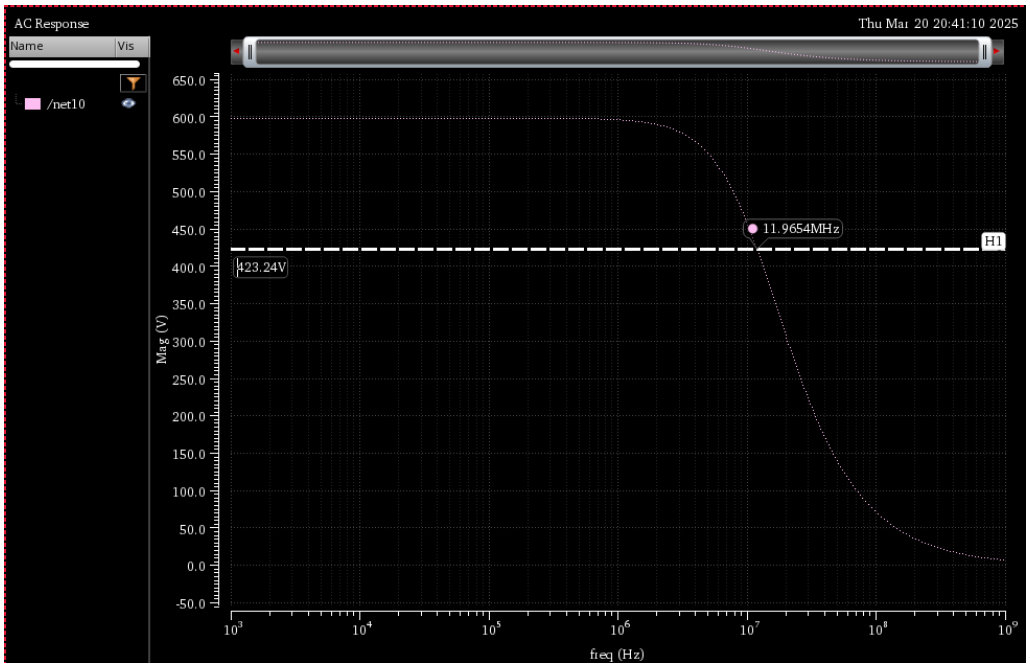

Figure 6 -3dB cutoff frequency

Also the transient analysis of the output node can be observed in the following figure. For the transient analysis input AC magnitude is 10mV with 10kHz frequency.

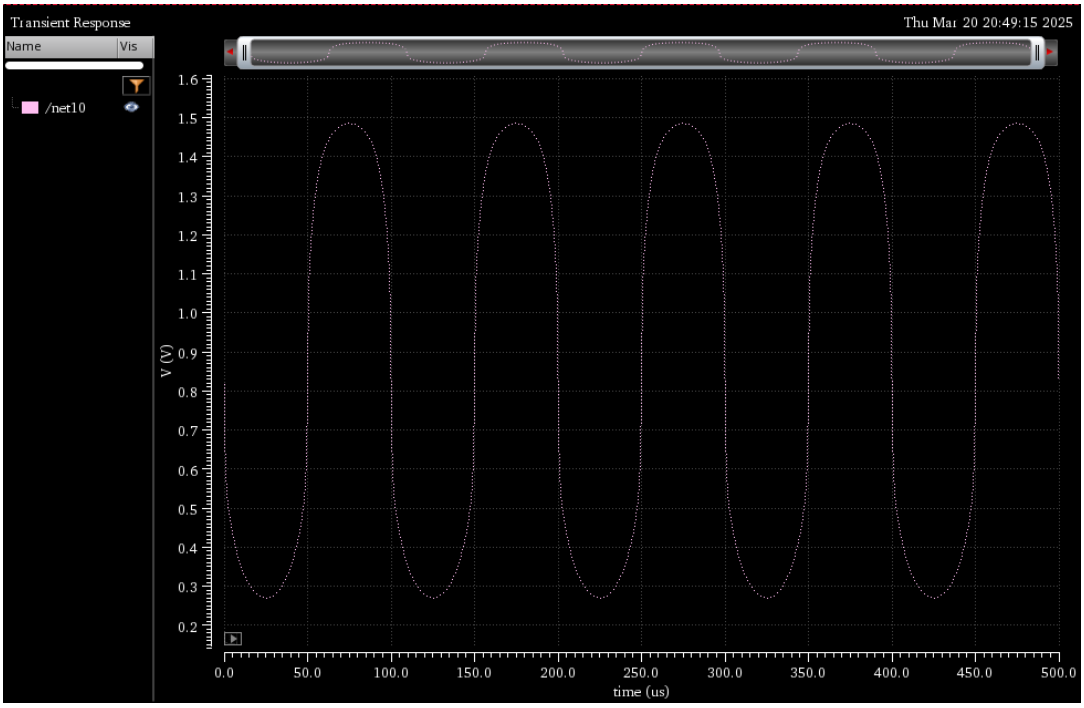

Figure 7 Transient analysis on output node

Previosly it is stated that in this design width determines an important role in defining the gain. However in a cascode amplifier width mismatches especially if a biasing network is utilized to bias transistors can lead to malfunctioning. Also the high gain circuits' gain expression consists of multiplication of gm values which makes them even more sensitive to small width variations.

In Figure 8 the plot for DC analysis between Vin vs Vout is provided to observe the rate of change between the variables. As it can be observed around 750mV the relation between Vin and Vout is almost linear which indicates the rate of change is constant around 750mV however increase in Vin significantly decreases Vout, in other words slope is very large.

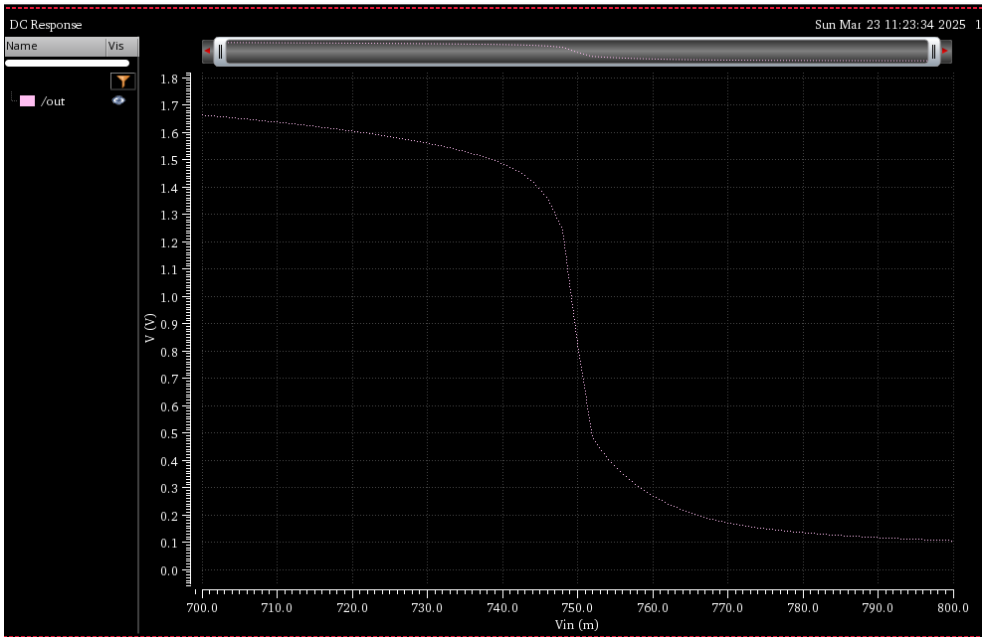

Figure 8 Vin vs Vout around 750mV

In this amplifier design the majority of noise is generated by M19 and M14 (top and bottom transistors). This is a result of the middle transistors being source degenerated hence noise is not amplified considerably. This conclusion can be verified form Figure 9. Moreover, in thermal noise analysis, as the final expression of input referred noise, in the denominator there is gm of the bottom nmos transistor. So by increasing gm of bottom transistor thermal nosie can be reduced. The 1/f noise is inversely proportional with the WL product meaning that by increasing the WL product 1/f noise can be reduced. Input referred nosie is plotted and provided as Figure 10 for the visualization.

Device	Param	Noise Contribution	% Of Total
/M19/m1	fn	3.67601e-08	68.53
/M16/m1	fn	2.47167e-09	4.61
/M14/m1	fn	3.24565e-11	0.06
/M19/m1	id	9.98634e-12	0.02

Spot Noise Summary (in V^2/Hz) at 10K Hz Sorted By Noise Contributors
Total Summarized Noise = 5.36442e-08
Total Input Referred Noise = 1.4931e-13
The above noise summary info is for noise data

Figure 9 Noise contributions of each transistor in amplifier branch

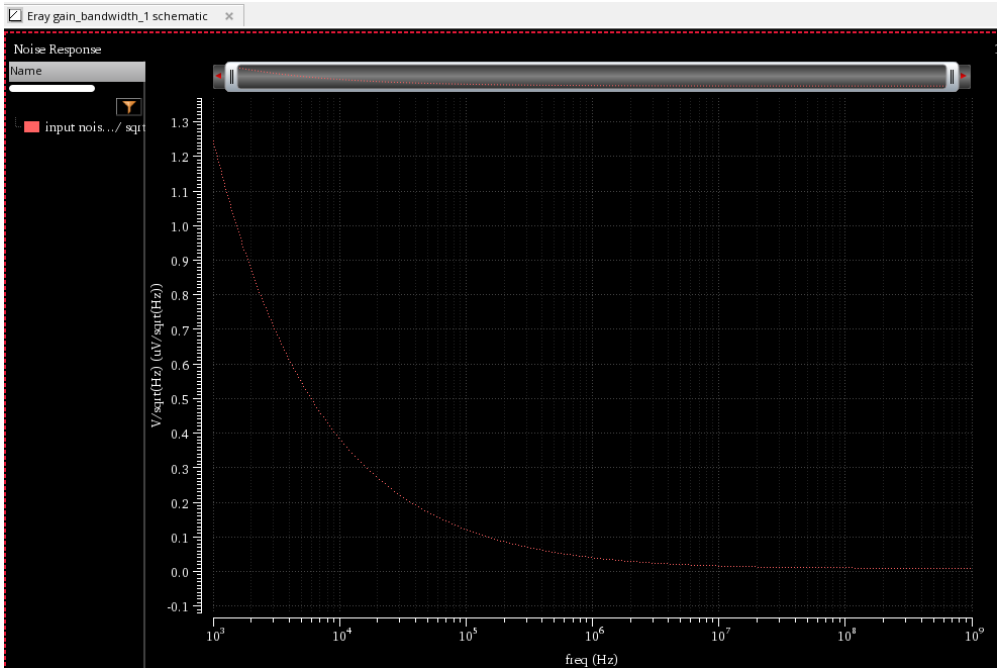

Figure 10 Input referred noise analysis

Part 2

In this part the purpose is to implement the layout of the designed amplifier and run DRC, LVS for the layout. It is desired to fit every component into a 20µm height with maximum 40µm width. In the schematic (Figure 2) only changes are made is to add input pin to replace the only voltage source and output pin to the output node. In Figure 11 it can be observed that there are 4 pins, Vdd and gnd pins are horizontal rails with 2µm height and there are additional two pins which represent input and output pins. First instances are generated from the source (schematic), no chaining or folding is used, 7 nmos transisttors are covered with p-guard and 3 pmos devices are covered with n-guard. The spacing for guards is determined to be 0.45 which is approximately %50 more compared default just for extra routing purposes. As th efinal step before routing pmos devices are covered with a single nwell to exclude violations. From Figure 11 it can be observed that layout is within the specified boundries. After appropriate routing with proper layers, DRC is run and initially some spacing erorrs are occured and they are solved by debugging and increasing the space to meet minimum spacing condition. The DRC analysis finalized with no errors as it can be observed from Figure 12. As the last step LVS analysis is performed and Figure 13 demonstrates the desired output for the LVS analysis.

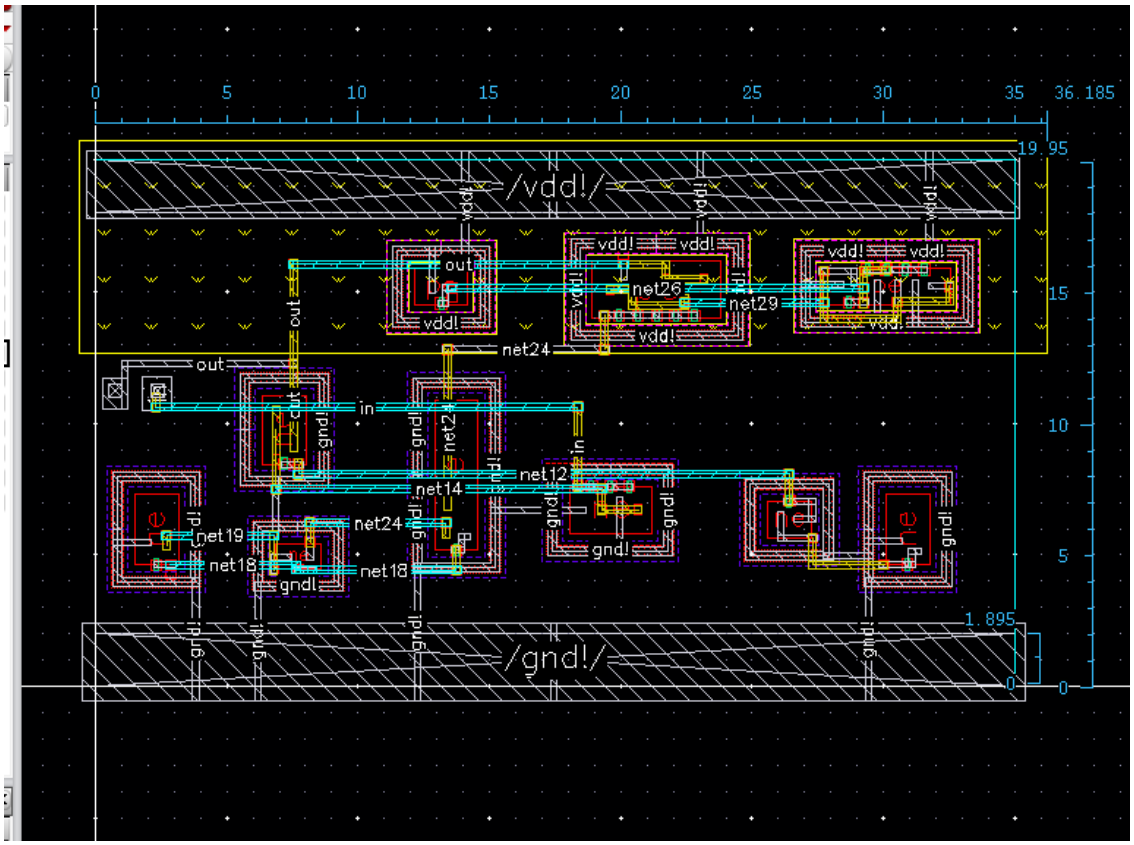

Figure 11 Layout of the amplifier

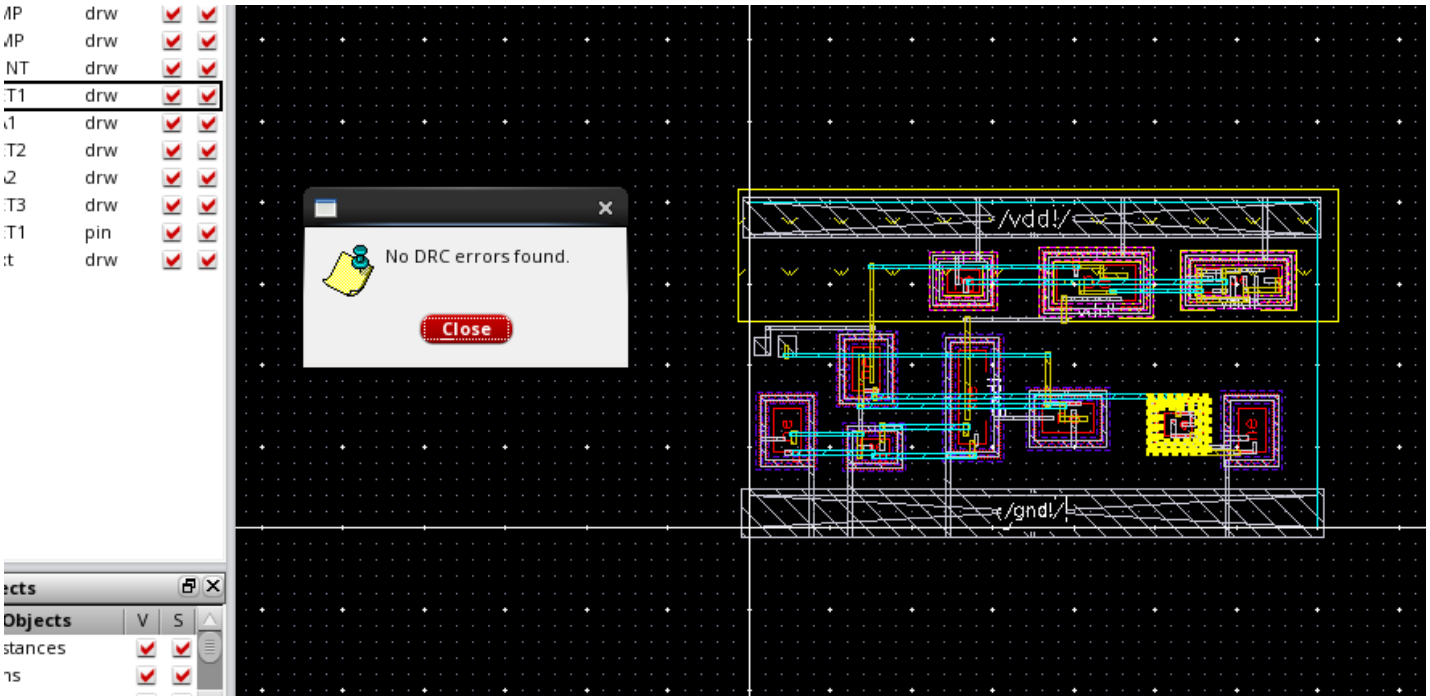

Figure 12 DRC analysis results

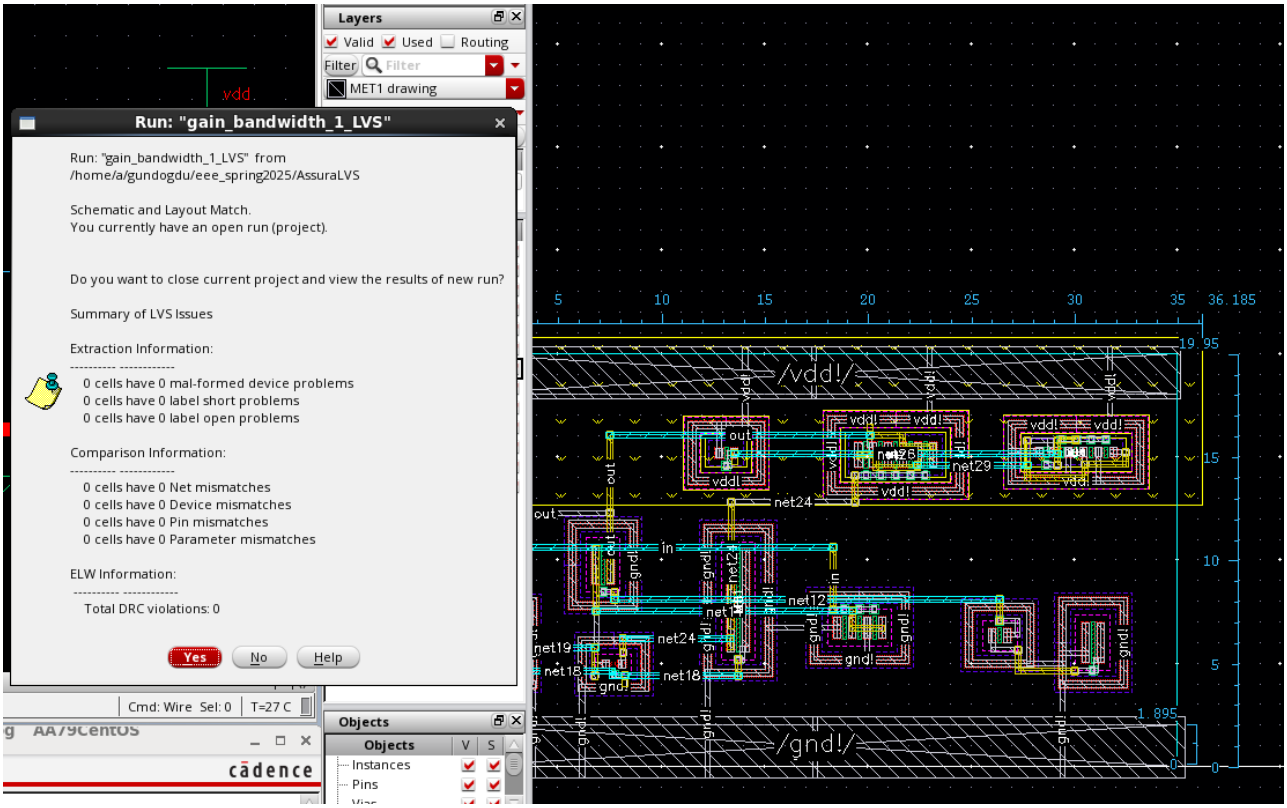

Figure 13 LVS analysis result