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# EEE313 Lab3 Report

## Introduction

Purpose of this lab is to familiarize students with nmos MOSFET and voltage amplifier circuits by designing a single staged common source amplifier. The nmos transistor that will be used in this lab is 2N7000. This lab consists of 3 parts. In part a by implementing a simple transistor curciut thresehold voltge for the transistor will be determined and a plot that demonstartes the relation between $I_D$ and $V_{DS}$ is given.

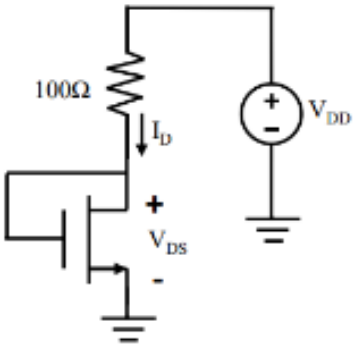



Fig 1.1 transistor circuit in part a

For part b 3 different $I_D$ vs $V_{DS}$ graphs will be plotted with three different $V_{GS}$ values then average value of $K_N$ and λ will be calculated.

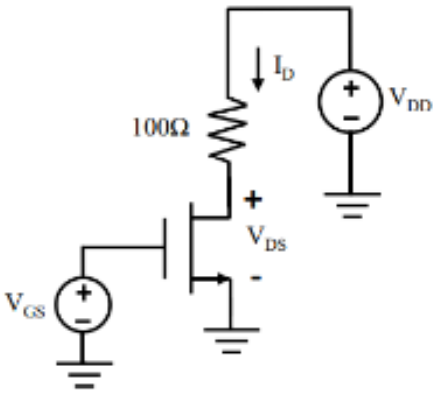
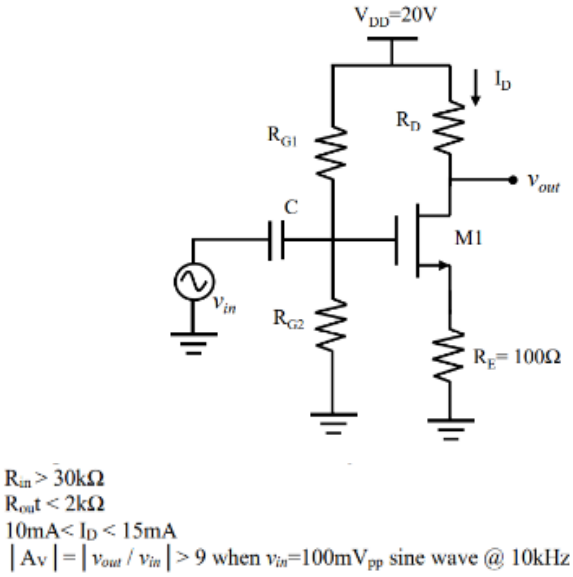



Fig1.2 test cuircuit in part b

In the last part after obtaining transistor values, small signal parameters, $g_m$ and $r_0$, will be determined and by using these values a single staged common source amplifier willl be desigend. The design specifications and the curciut can be observed as following.




$R_{in} > 30k\Omega$
$R_{out} < 2k\Omega$
$10mA < I_D < 15mA$
$|A_V| = |v_{out} / v_{in}| > 9$ when $v_{in}$=100mV$_{pp}$ sine wave @ 10kHz

Fig1.3 common source amplifier

**Hardware Implementation and Analysis**

Part a

The threshold voltage of the transistor can be determined by obtaining the $V_{DD}$ value at the turn on point of the transistor which is the $V_{DD}$ value when $1mA$ passes through the transistor. At this point $V_{GS} = V_{TH}$.In addition, $V_{GS} = V_{DS}$ for every i($I_D$) for this part.Therefore $V_{TH}$ can be obtained by using the following equation.

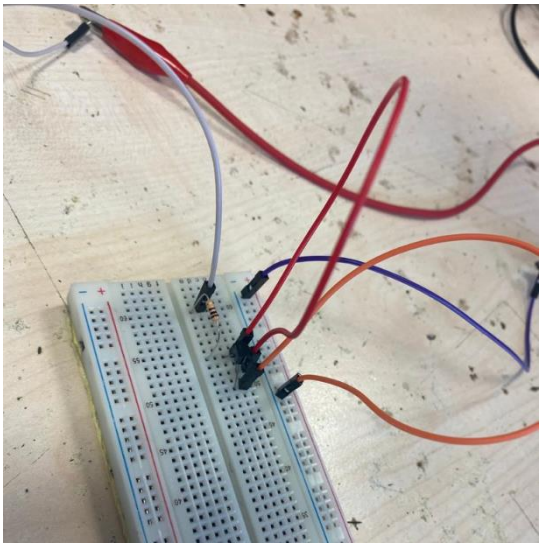


Fig2.1 hardware circuit for part a

$$V_{DD} - 0.1I_D = V_{TH}$$

$$V_{DD} = 1.61V, I_D = 1mA$$

$$V_{TN} = 1.51V$$

In order to plot the $V_{DS}$ vs $I_D$ graph 30 $V_{DD}$ values are captured for $I_D$ values from $1mA$ to $30mA$ with an arithmetic difference of 1. The relation for drain to source potential and transistor current is accordingly.

$$V_{DD} - 0.1I_D = V_{DS}$$

| $I_D(mA)$ | $V_{DD}(V)$ |
|---|---|
| 1 | 1.61 |
| 2 | 1.78 |
| 3 | 1.93 |
| 4 | 2.07 |
| 5 | 2.19 |
| 6 | 2.33 |
| 7 | 2.47 |

| | |
|---|---|
| 8 | 2.58 |
| 9 | 2.69 |
| 10 | 2.84 |
| 11 | 2.94 |
| 12 | 3.06 |
| 13 | 3.18 |
| 14 | 3.29 |
| 15 | 3.42 |
| 16 | 3.53 |
| 17 | 3.64 |
| 18 | 3.75 |
| 19 | 3.87 |
| 20 | 3.99 |
| 21 | 4.10 |
| 22 | 4.21 |
| 23 | 4.32 |
| 24 | 4.43 |
| 25 | 4.55 |
| 26 | 4.64 |
| 27 | 4.76 |
| 28 | 4.90 |
| 29 | 5.0 |
| 30 | 5.11 |

Table1.1 $I_D$ and corresponding $V_{DD}$ values

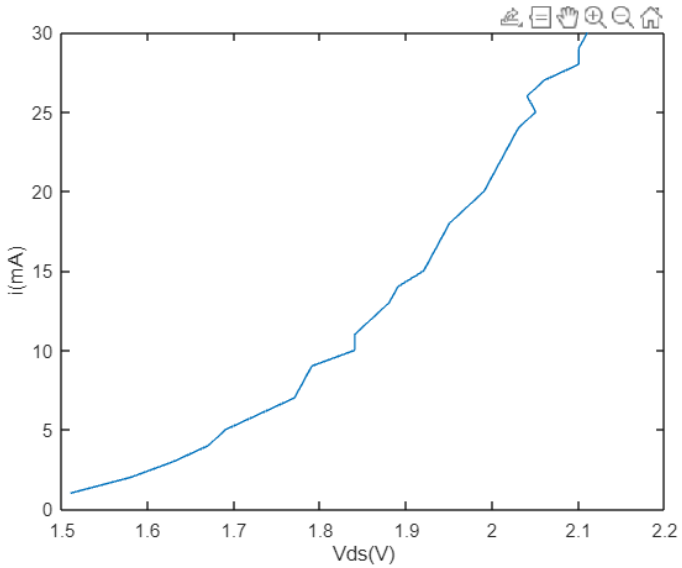



Fig2.2 $I_D$ vs $V_{DS}$

Part b

In this part 3 $I_D$ vs $V_{DS}$ graphs will be plotted with different $V_{GS}$ values $V_{TH}$+0.3, $V_{TH}$+0.4, $V_{TH}$+0.5. So, $V_{GS1} = 1.81V$, $V_{GS2} = 1.91V$, and $V_{GS3} = 2.01V$. It should be highlighted that due $V_{GS3}$ being large, it takes more to be saturated therefore for the last table 45 data is considered.

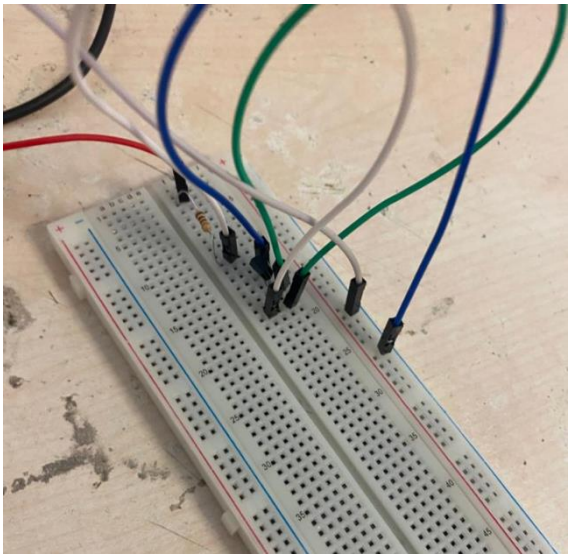


Fig3.1 hardware circuit for part b

| $I_D(mA)$ | $V_{DD}(V)$ |
|---|---|
| 1 | 0.11 |
| 2 | 0.23 |
| 3 | 0.34 |
| 4 | 0.47 |
| 5 | 0.59 |
| 6 | 0.71 |
| 7 | 0.84 |
| 8 | 0.97 |
| 9 | 1.11 |
| 10 | 1.28 |
| 11 | 1.44 |
| 12 | 1.88 |
| 13 | 2.20 |
| 14 | 3.92 |
| 15 | 4.19 |
| 16 | 4.40 |
| 17 | 4.61 |
| 18 | 4.91 |
| 19 | 5.16 |
| 20 | 5.42 |
| 21 | 5.73 |

| | |
|---|---|
| 22 | 6.0 |
| 23 | 6.32 |
| 24 | 6.60 |
| 25 | 6.89 |
| 26 | 7.24 |
| 27 | 7.60 |
| 28 | 7.82 |
| 29 | 8.15 |
| 30 | 8.43 |

Table2.1 $I_D$ and corresponding $V_{DD}$ values when $V_{GS1} = 1.81V$

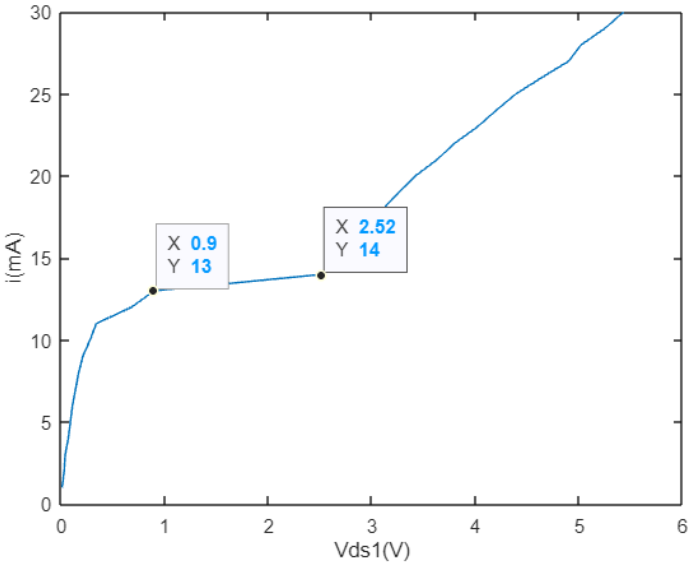



Fig3.2 $I_D$ vs $V_{DS1}$

Two points on the graph is given by using these points the x axis intersect can be found which is equal to $-\frac{1}{\lambda_1}$.

$$\frac{1}{2.52 - 0.9} = \frac{y - 13}{x - 0.9}$$

$$y = 0, x = -20.16$$

$$\lambda_1 \cong 0.0496V^{-1}$$

$$I_{DQ} = K_{N1}(V_{GS1} - V_{TH})^2(1 + \lambda_1 V_{DS1})$$
$$14mA = K_{N1}(0.3V)^2(1 + 0.05 * 2.52)$$

$$K_{N1} \cong 138.15 \frac{mA}{V^2}$$

| $I_D(mA)$ | $V_{DD}(V)$ |
|---|---|
| 1 | 0.11 |
| 2 | 0.23 |
| 3 | 0.34 |
| 4 | 0.45 |
| 5 | 0.56 |
| 6 | 0.68 |
| 7 | 0.79 |
| 8 | 0.92 |
| 9 | 1.01 |
| 10 | 1.15 |
| 11 | 1.24 |
| 12 | 1.35 |
| 13 | 1.49 |
| 14 | 1.61 |
| 15 | 1.72 |
| 16 | 1.85 |
| 17 | 1.97 |
| 18 | 2.13 |
| 19 | 2.28 |
| 20 | 2.44 |
| 21 | 2.71 |
| 22 | 3.88 |
| 23 | 5.10 |
| 24 | 5.51 |
| 25 | 5.85 |
| 26 | 6.10 |
| 27 | 6.41 |
| 28 | 6.74 |
| 29 | 7.09 |
| 30 | 7.34 |

Table2.2 $I_D$ and corresponding $V_{DD}$ values when $V_{GS2} = 1.91V$

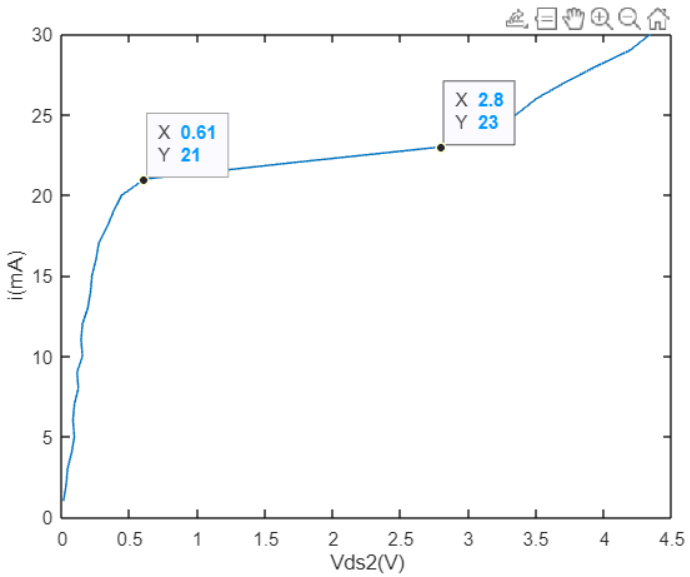



Fig3.3 $I_D$ vs $V_{DS2}$

$$\frac{2}{2.8-0.61}=\frac{y-23}{x-2.8}$$

$$y=0, x=-22.39$$

$$\lambda_2 \cong 0.0446V^{-1}$$

$$I_{DQ}=K_{N2}(V_{GS2}-V_{TH})^2(1+\lambda_2 V_{DS2})$$
$$23mA=K_{N1}(0.4V)^2(1+0.0446*2.8)$$

$$K_{N2} \cong 161.71\frac{mA}{V^2}$$

| $I_D(mA)$ | $V_{DD}(V)$ |
|---|---|
| 1 | 0.10 |
| 2 | 0.21 |
| 3 | 0.33 |
| 4 | 0.42 |
| 5 | 0.52 |
| 6 | 0.64 |
| 7 | 0.76 |
| 8 | 0.84 |
| 9 | 0.94 |
| 10 | 1.07 |
| 11 | 1.15 |
| 12 | 1.27 |
| 13 | 1.36 |
| 14 | 1.45 |
| 15 | 1.58 |
| 16 | 1.69 |
| 17 | 1.80 |
| 18 | 1.91 |
| 19 | 2.01 |
| 20 | 2.21 |
| 21 | 2.23 |
| 22 | 2.35 |
| 23 | 2.45 |
| 24 | 2.57 |
| 25 | 2.67 |
| 26 | 2.78 |
| 27 | 2.85 |
| 28 | 3.0 |
| 29 | 3.10 |
| 30 | 3.21 |
| 31 | 3.33 |
| 32 | 3.45 |
| 33 | 3.56 |
| 34 | 3.67 |
| 35 | 3.80 |
| 36 | 4.05 |

| | |
|---|---|
| 37 | 4.22 |
| 38 | 4.48 |
| 39 | 4.65 |
| 40 | 4.88 |
| 41 | 5.22 |
| 42 | 5.45 |
| 43 | 5.97 |
| 44 | 6.10 |
| 45 | 6.30 |

Table2.3 $I_D$ vs $V_{DS3}$

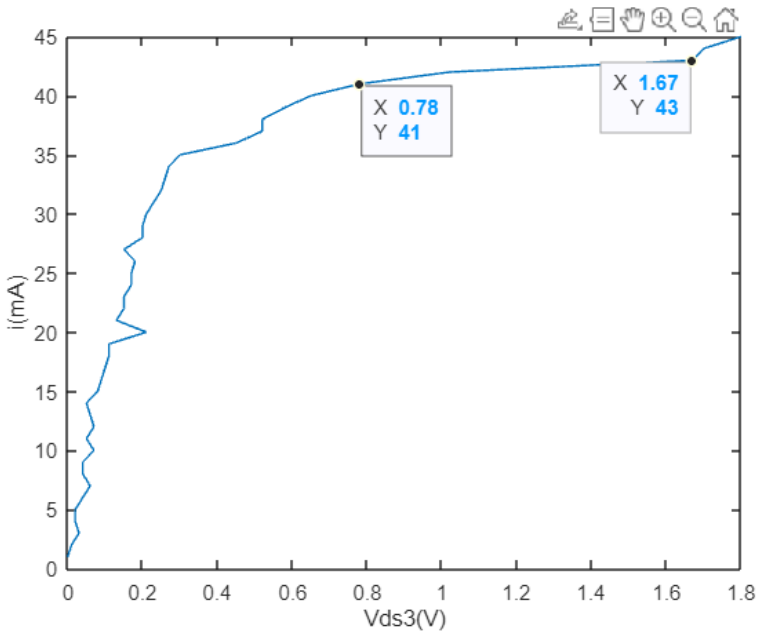



Fig3.4 $I_D$ vs $V_{DS3}$

$$\frac{2}{1.67-0.78}=\frac{y-43}{x-1.67}$$

$$y=0, x=-17.46$$

$$\lambda_2 \cong 0.0572V^{-1}$$

$$I_{DQ}=K_{N3}(V_{GS3}-V_{TH})^2(1+\lambda_3 V_{DS3})$$
$$43mA=K_{N3}(0.5V)^2(1+0.0572*1.67)$$

$$K_{N3} \cong 157.00\frac{mA}{V^2}$$

After obtaining 3 values for both $K_N$ and λ the avurage for them is calculated.

$$K_{Navg}=152.28\frac{mA}{V^2}$$

$$\lambda_{avg}=0.0504V^{-1}$$

Part c

In order to design a common source amplifier precise with the design specifications resistance values $R_{G1}$, $R_{G2}$, $R_D$, and small signal parameters $g_m$ , $r_0$ will be determined in this part. $I_{DQ}$ is selected as 12 $mA$

$$g_m = 2\sqrt{I_{DQ} * K_{Navg}}$$

$$g_m \cong 95.84\frac{mA}{V}$$

$$r_0 = \frac{1}{\lambda_{avg} * I_{DQ}}$$

$$r_0 \cong 1.65k\Omega$$

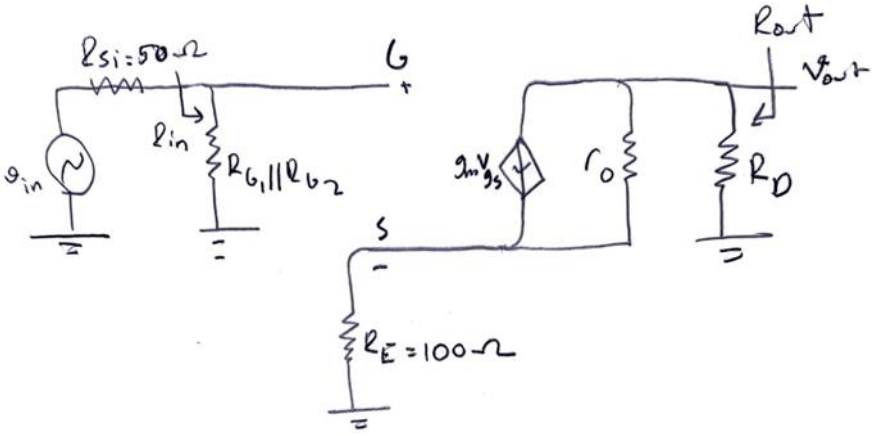



Fig4.1 small signal model of the common source amplifier

It is assumed that transistor is in SAT therefore,

$$V_{GS} > V_{TH}$$

$$V_G - 12 * 0.1 > 1.51$$

$$V_G > 2.71V$$

$V_G$ is taken as $3V$. It is also known that $R_{in} > 30k\Omega$. From voltage divider,

$$V_G = V_{DD}(\frac{R_{G2}}{R_{G2} + R_{G1}})$$

$$\frac{3}{17} = \frac{R_{G2}}{R_{G1}}$$

$$R_{in} = \frac{R_{G2} * R_{G1}}{R_{G2} + R_{G1}} > 30k\Omega$$

Combining the last two equations,

$$R_{G1} > 200k\Omega$$

$R_{G1}$ is selected as 300 $k\Omega$. According to this, value of $R_{G2}$ should be 52.9 $k\Omega$ however 50$k\Omega$ is chosen due not being present in lab. Now value of $R_D$ will be determined.

Using SAT condition,

$$V_{DS} > V_{GS} - V_{TH}$$

$$20V - 12 * R_D > 3V - 1.51V$$

$$1.54k\Omega > R_D$$

Using Rout condition from Fig4.1 KCL at drain with test source,

$$g_m V_{gs} + \frac{V_x - V_s}{r_0} + \frac{V_x}{R_D} = I_x$$

KCL at source,

$$\frac{V_s}{R_E} + \frac{V_s - V_x}{r_0} - g_m V_{gs} = 0$$

Combining two KCL,

$$\frac{V_x}{I_x} = R_{out} = \frac{(R_E + r_0(1 + R_E g_m))}{(R_E + r_0(1 + R_E g_m)) + R_D} R_D < 2k\Omega$$

$$R_D < 2.59k\Omega$$

Using the gain condition,

$$|A_v| = \left| -\frac{R_D * g_m * r_0}{R_D + R_E + (1 + g_m R_E) r_0} \right| > 9$$

$$R_D > 1.28k\Omega$$

Combining all $R_D$ inequalities,

$$1.54k\Omega > R_D > 1.28k\Omega$$

Chosen resistence values for implementation is as following.

$R_D = 1.50k\Omega$,

$R_{G1} = 300\ k\Omega$,

$R_{G2} = 50k\Omega$.

$C = 100\mu F$

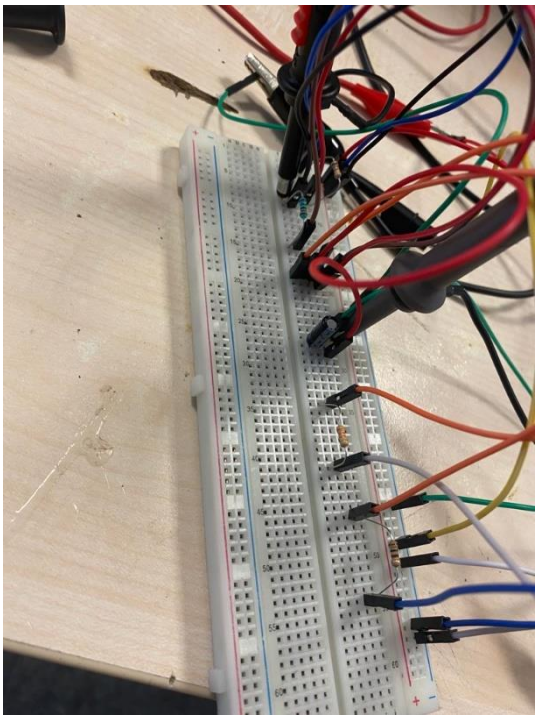


Fig4.2 hardware implementation of common source amplifier

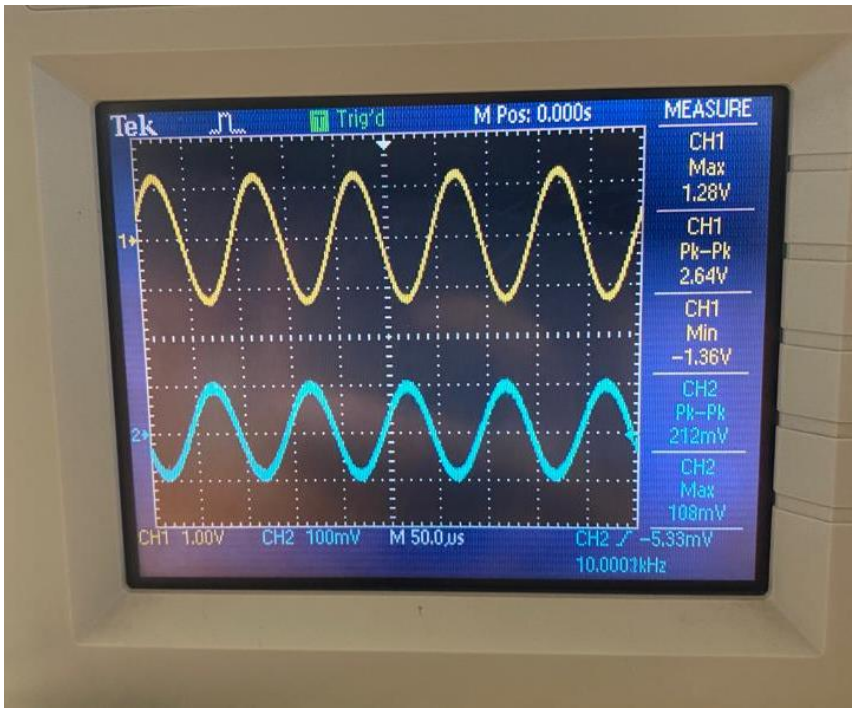



Fig4.3 demonstration of small signal gain

$|A_v| = \frac{1.28V}{108mV} = 11.85$. The gain is above 9 therefore the circuit operates as desired. After observing the gain it is desired to increase the small signal until distortions are noticed at the output. As small signal increases, at some point the the state of the transistor is changed from SAT to NONSAT hence,

voltage amplification is terminated until the transistor returns to SAT. As a result, it can be interpreted that maximum input voltage equals to the maximum voltage value that keeps the transistor in saturation. In this experiment when small signal increased to 0.7V distortions start which can be observed in the following figure. In order to prevent any confusion, unlike Fig4.3and Fig4.5, in Fig4.4 yellow traces represent the small signal.

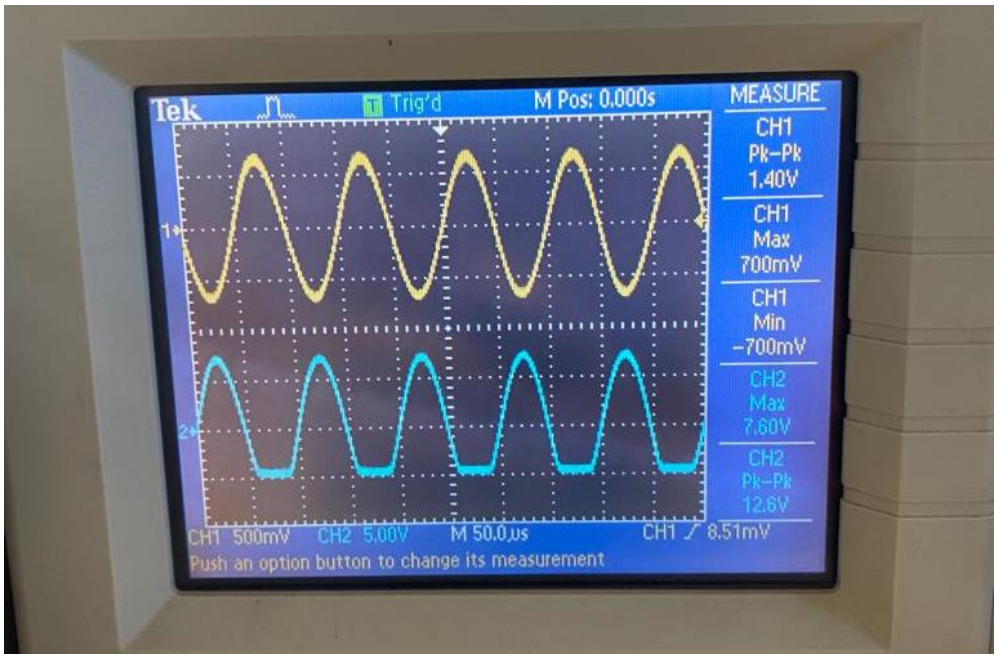



Fig4.4 demonstration of distortions.

After observing the distortions it is desired to observe the gain after connecting a $100\mu F$ capacitor parallel to $R_E$.

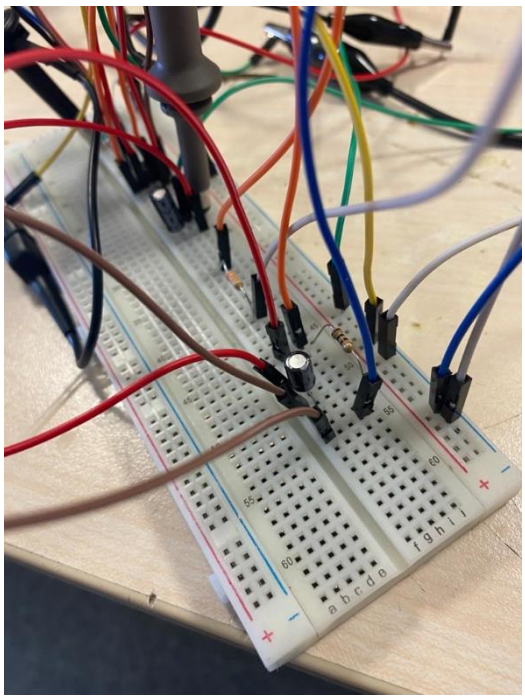


Fig4.5 implementation of the capacitor

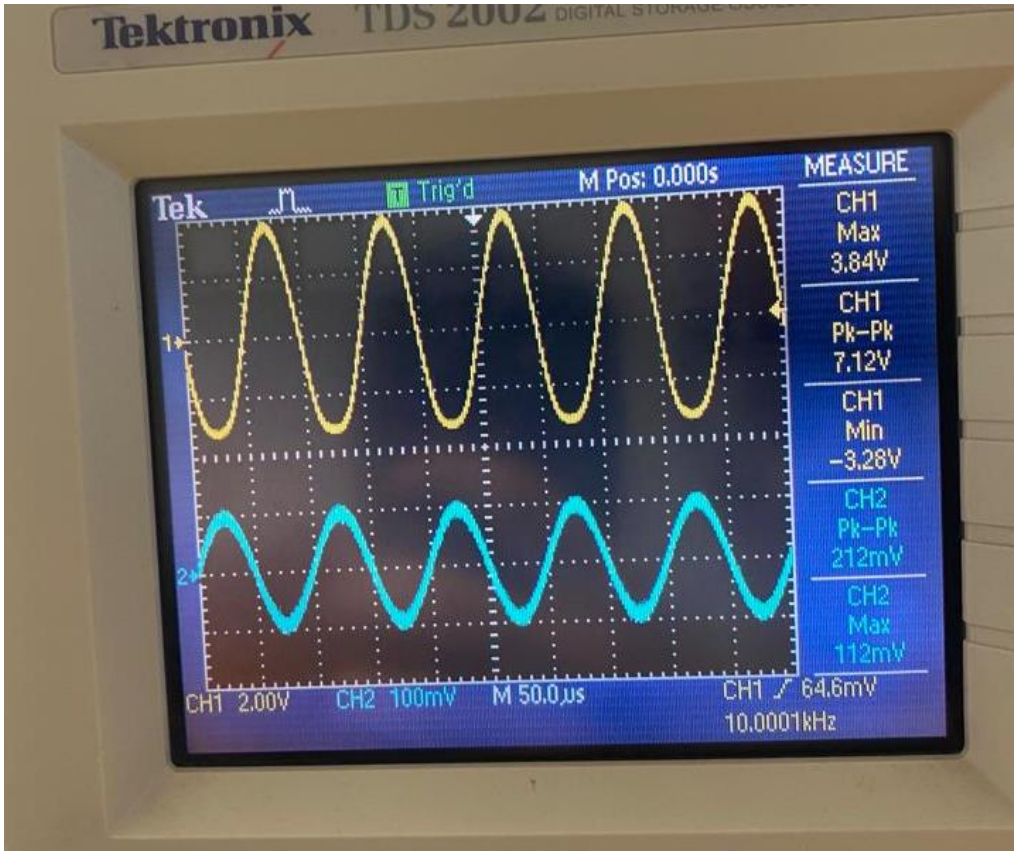



Fig4.5 demonstration of gain with parallel capacitor

$$|A_v| = \frac{3.84V}{112mV} = 34.28$$

Recalling the gain equation $A_v = -\frac{R_D * g_m * r_0}{R_D + R_E + (1 + g_m R_E) r_0}$, as a capacitor is connected parallel to $R_E$ the capacitor behaves like a short circuit therefore $R_E$ is not included to the gain equation. Removing a parameter from denominator increases the value hence gain increases.

**Conclusion**

This lab was useful to familiarize with transistors and voltage amplifier circuits. In this lab a common source amplifier is designed. Before implemeting the common source amplifier necessary transistor,small signal parameters and resistance values are calculated. After the implemetation gain is observed and two other apllications, determining max input voltage and parallel capacitor connection is done. These application gave even better insight of voltage amplifier circuits and transistors. The results were precise with the desired design specificacions meaning that the desigend common source amplifier is operating as desired. Even though the results may seem good enough there are always room for error that are caused by the uncertainity of the oscilloscobe and signal generater, excessive resistence of jumper cables.