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EEE313 Lab Report 4

Introduction

In this lab assignment it is desired to design a two stage BJT amplifier which is referred as common emitter stage cascaded with push-pull voltage buffer. Designing process of the amplifier circuit consists of two major steps which are software design and hardware implentation respectively. The desired common emitter stage cascaded with push-pull voltage buffer and specifications can be observed in the following figure.

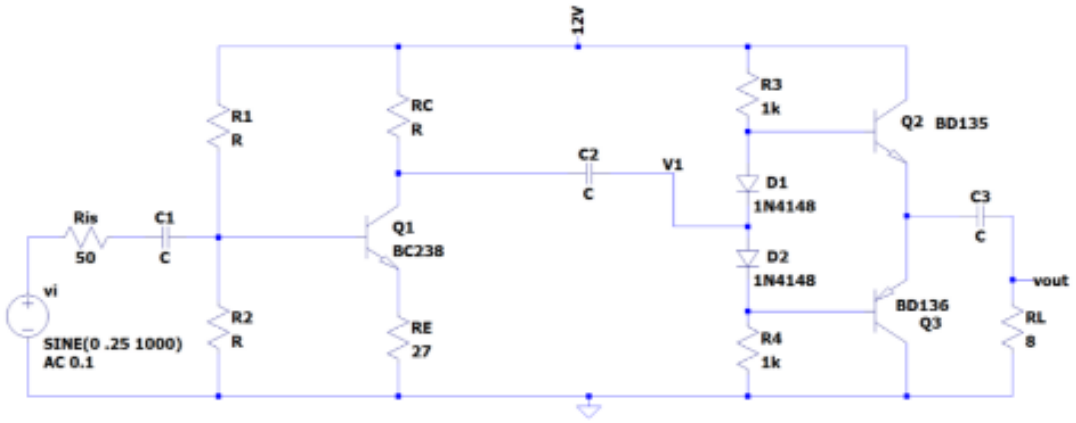

Fig1.1 Desired common emitter stage cascaded with push-pull voltage buffer

Specifications are listed as:

- Gain of the first stage should be equal to -10
- Overall gain should be -5
- The output should not get clipped up to an ac input of 0.5V peak.

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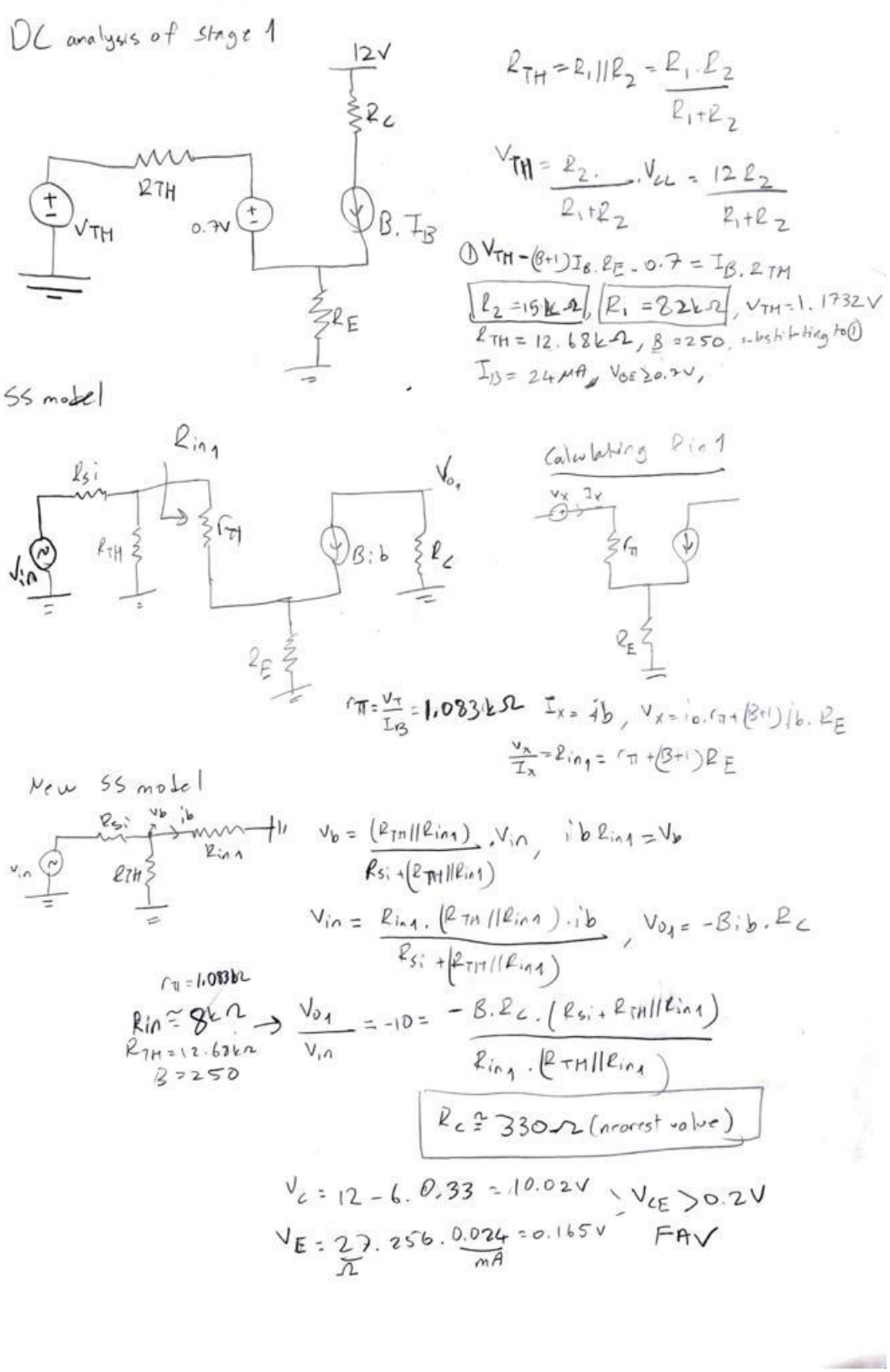
Software Design and Analysis

It is desired to determine values for R1, R2 and RC. These values are obtained by the following expressions. The values are selected according to the present values in the labratory.



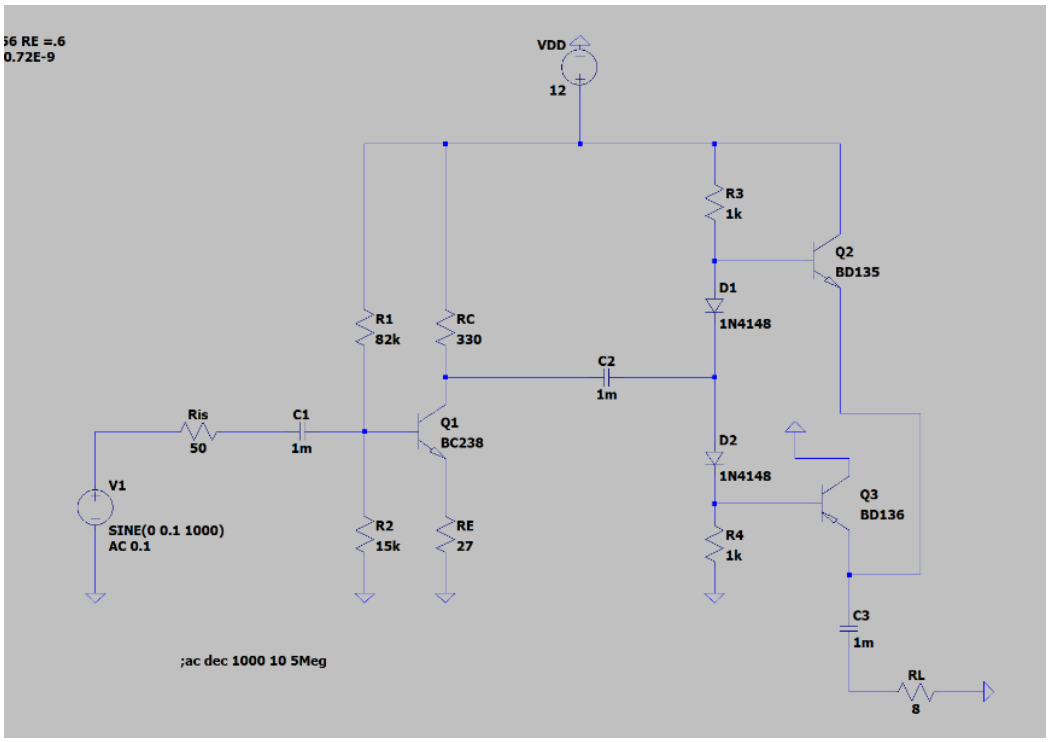


Fig2.1 Circuit implementation in LTSpice

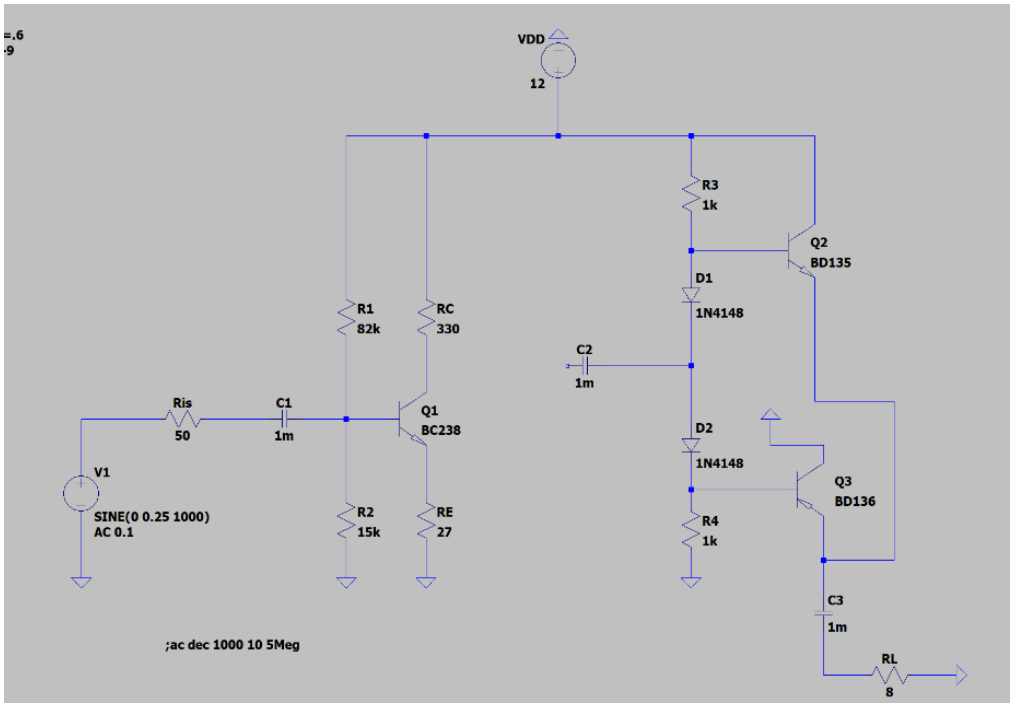


Fig 2.2 demonstration of disconnected stages

In the following steps gain of the first stage and overall gain, -3 dB cutoff frequencies, clipping are observed in software. Gains will be calculated seperately according to Fig2.2 and Fig2.1 respectively

afterwards capacitor values will be changed to C1=10µF, C2=100µF, C3=1000Mf. Cutoff frequencies and clipping will be observed after alternating the capacitor values.

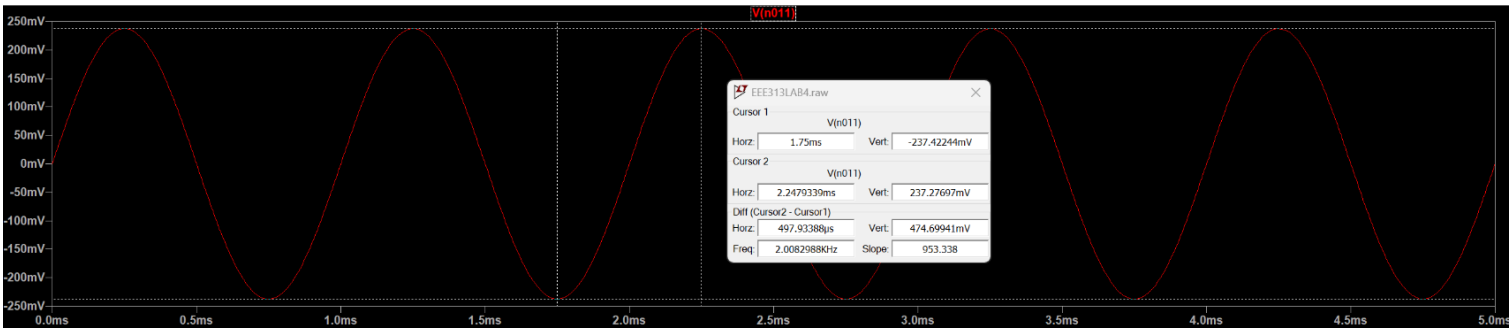


Fig2.3 input pk-pk voltage

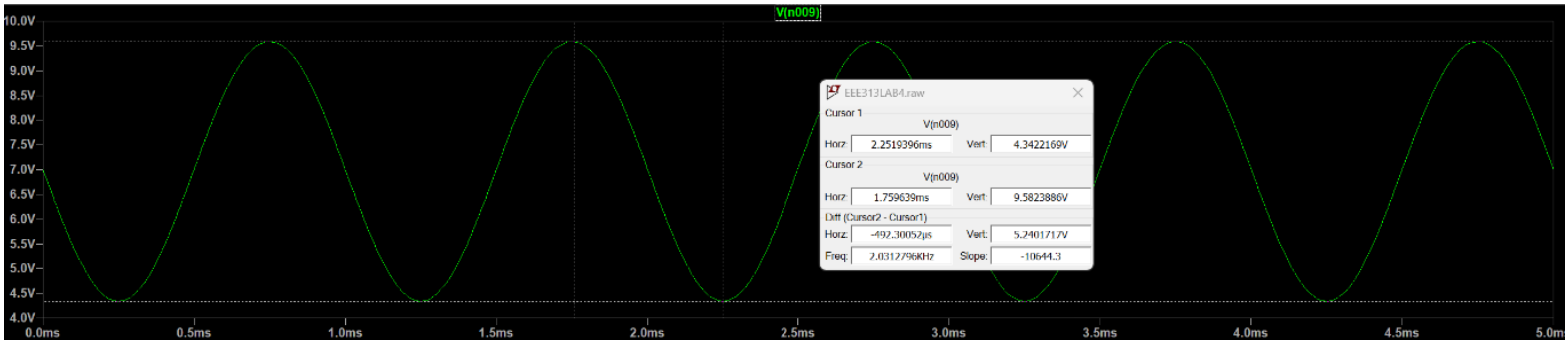


Fig2.4 Output pk-pk voltage of the first stage.

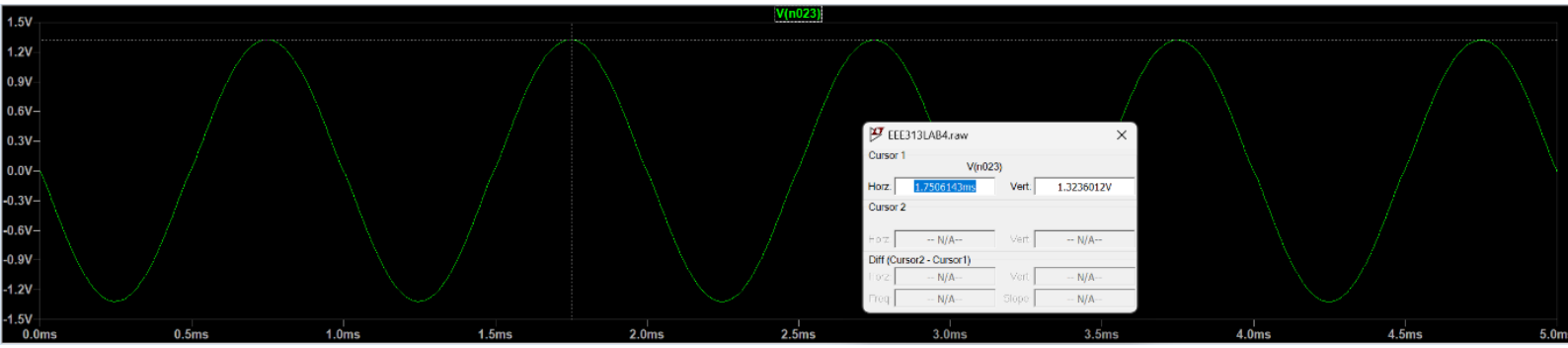


Fig2.4 Output peak voltage at the second stage

Gain can be expressed as

$$\frac{\nabla V_o}{\nabla V_{in}}$$

At the output of the first stage $\frac{\nabla V_o}{\nabla V_{in}} = \frac{-5240}{474.6} = -11.04$,

At the output of the stage two $\frac{\nabla V_o}{\nabla V_{in}} = \frac{-1323}{237.2} = -5.57$.

The gain values are higher than expected when compared to theoratical values. However this can be considered as optimal due to considerably higher energy loss in hardware circuits meaning that the hardware implementation will be even more accurate.

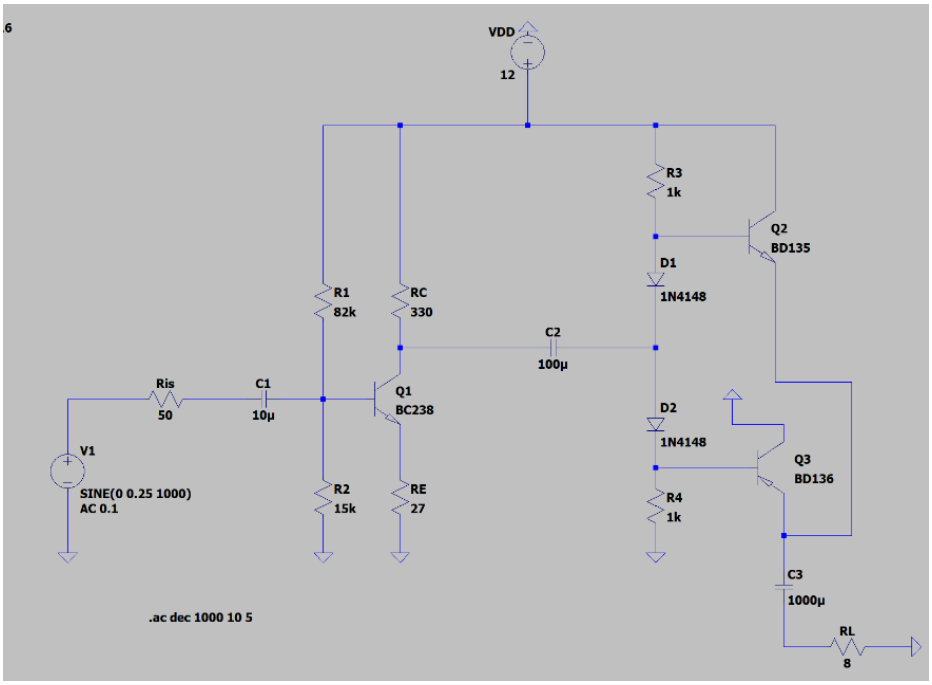


Fig2.5 circuit with alternated capacitors

Fig2.6 -3 dB low cutoff frequency

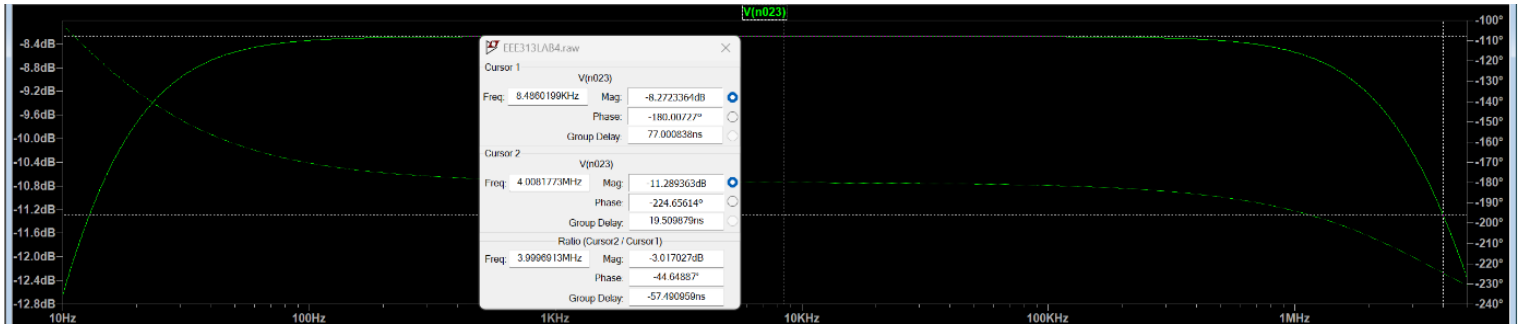


Fig2.6 -3 dB high cutoff frequency

fLow	fHigh
12.89Hz	4.00MHz

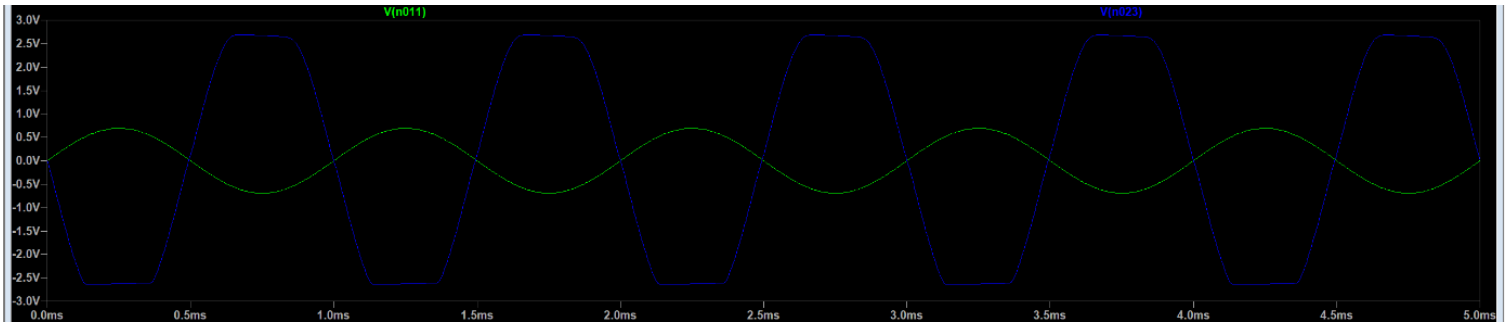


Fig2.7 demonstration of clipping when AC amp. is 0.7V

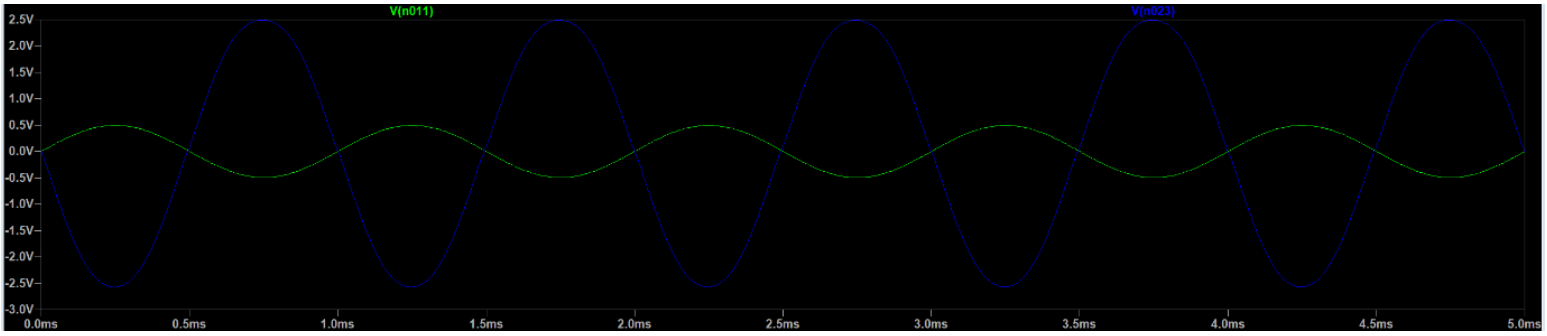


Fig2.8 input vs output when AC amp. is 0.5V

As it can be observed the output is not clipped when AC input has an amplitude of 0.5V. Now diodes will be short circuited and behavior of the circuit will be investigated.

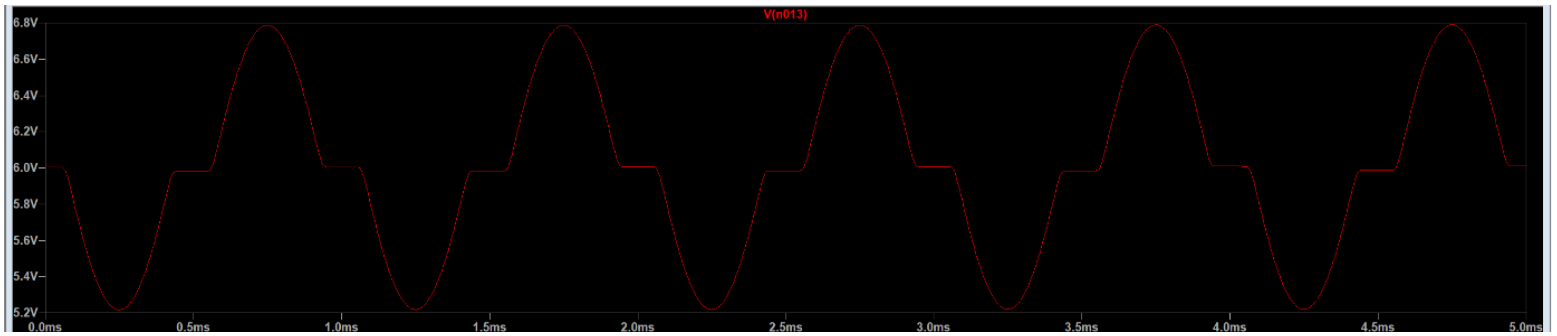


Fig2.9 Distorted output when diodes are short circuited

Diodes are responsible for maintaining the direction of the current meaning that when these diodes are short circuited base currents of BD235 and BD236 is alternated. In addition due to absenties of the diodes at some points base to emitter(emitter to base for pnp) becomes lower than the threshold voltage hence BD235 and BD236 moves to cutoff reigon. As a result of these magnitute and waveform of the output is alternated when diodes are short circuited.

Hardware Implementation

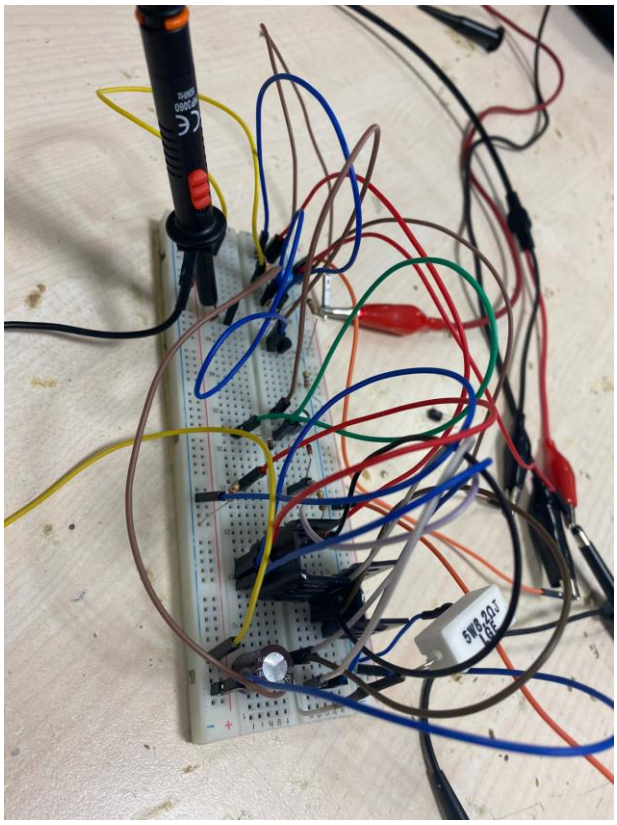


Fig3.1 Hardware implementation

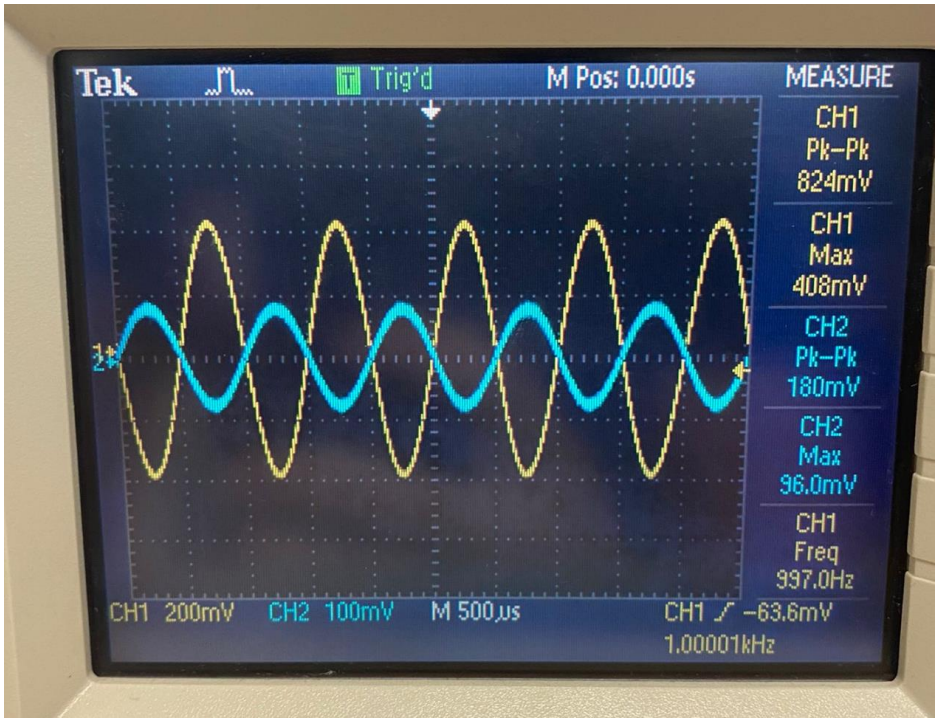


Fig3.2 input vs output when input is 0.1sinwt

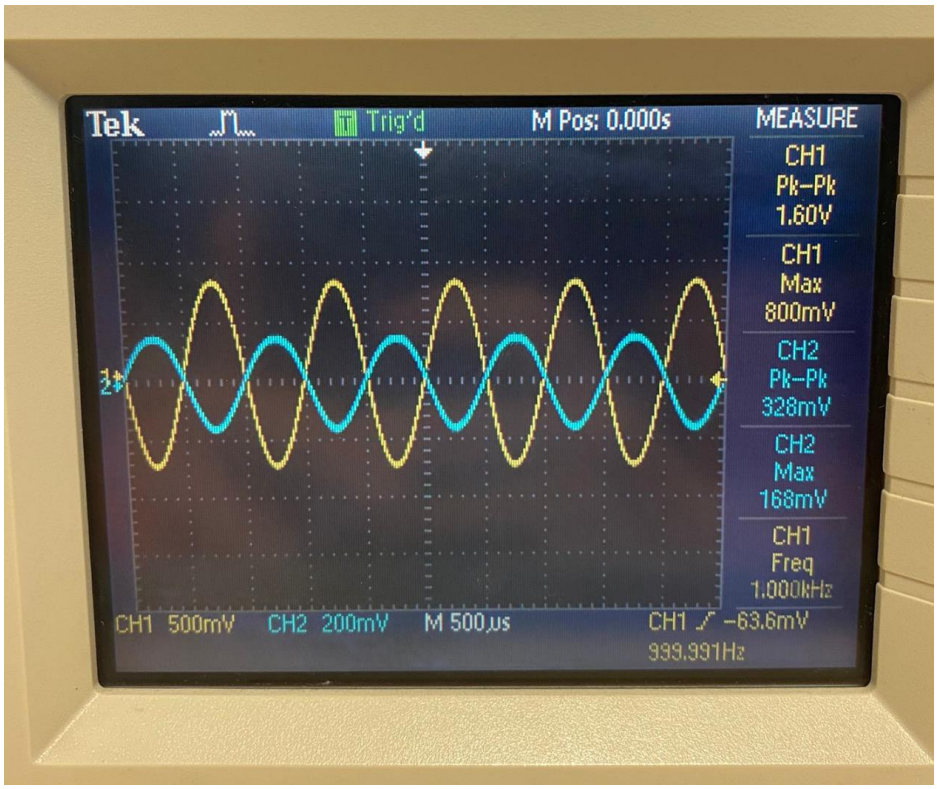


Fig3.3 input vs output when input is 0.2sinwt

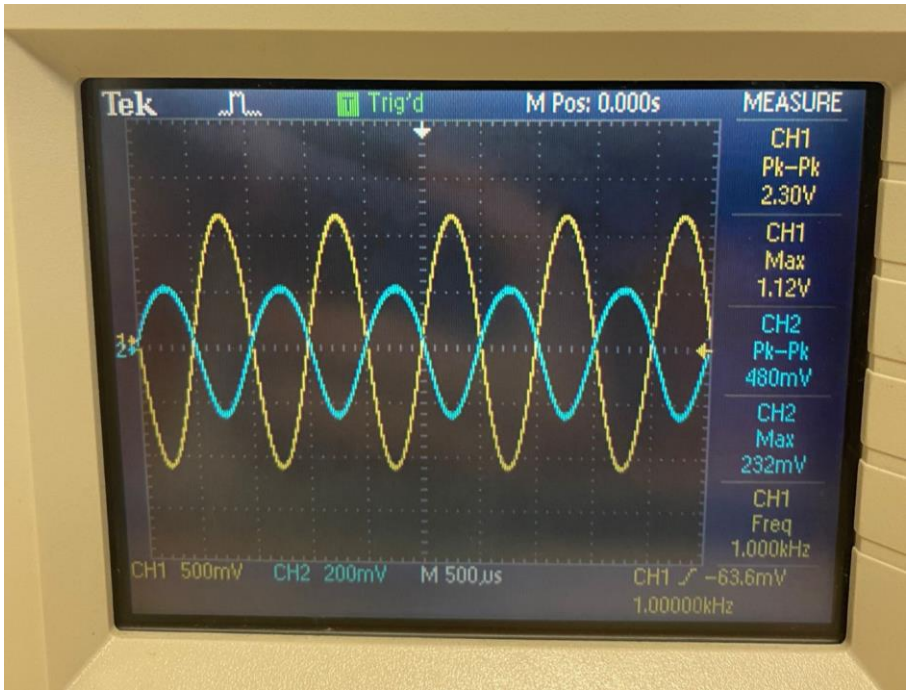


Fig3.4 input vs output when input is 0.3sinwt

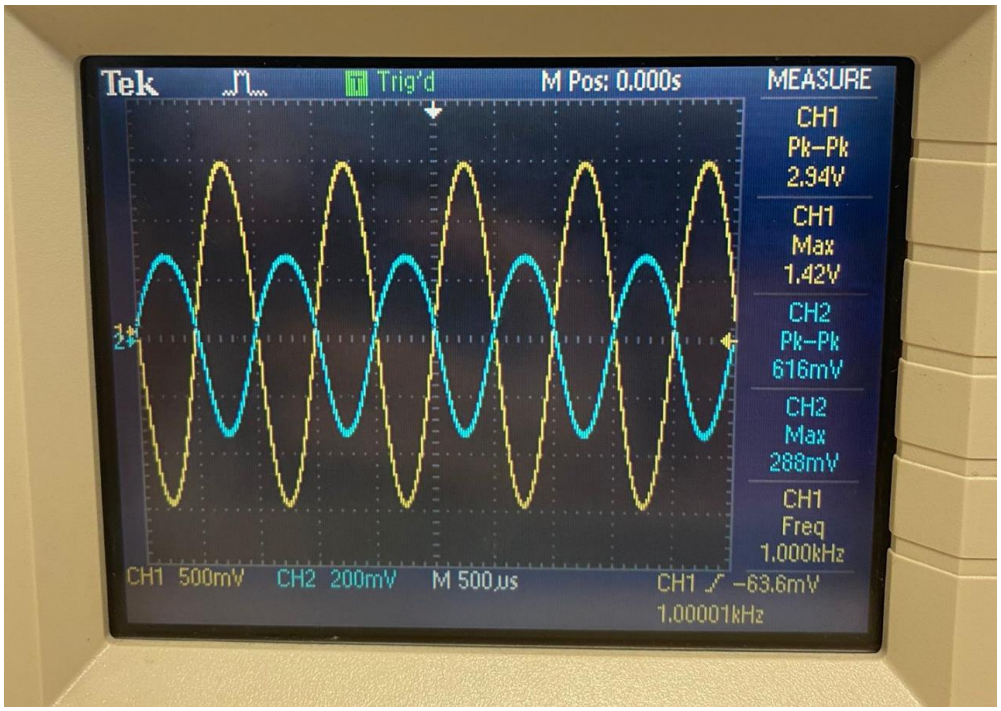


Fig3.5 input vs output when input is 0.4sinwt

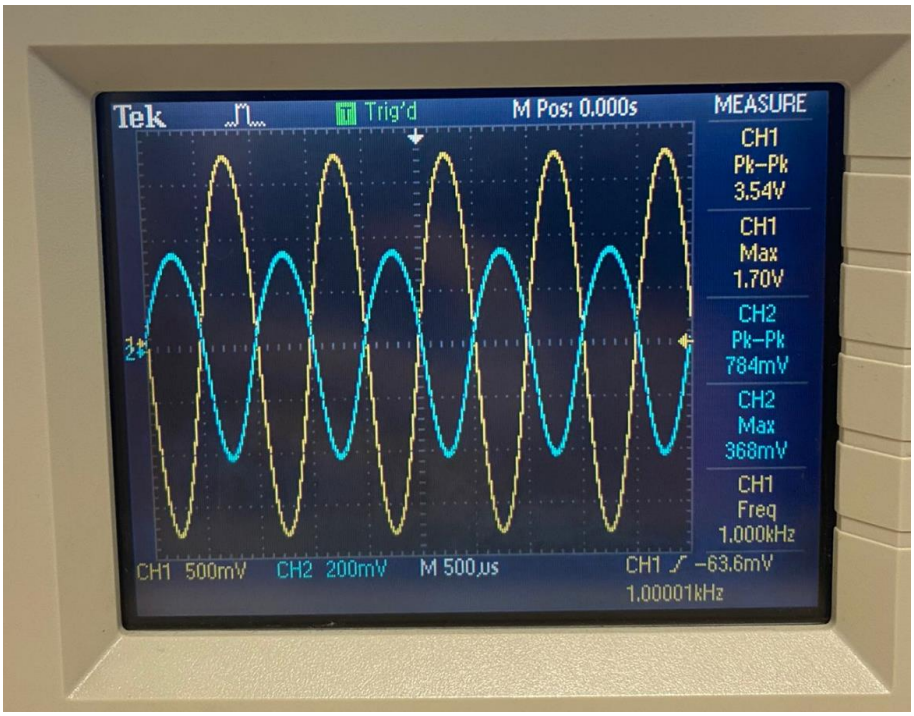


Fig3.6 input vs output when input is 0.5sinwt

Input	Gain
0.1sinwt	-4.57
0.2sinwt	-4.87
0.3sinwt	-4.79
0.4sinwt	-4.77
0.5sinwt	-4.51

Table3.1 Input vs Gain

No matter what the small signal input is gain should be constant theoratically. According to hardware results the gain is around -5 and can be considered as constant due to insignificant differences. Hence this step is as desired. Now harmonic content for every input will be observed.

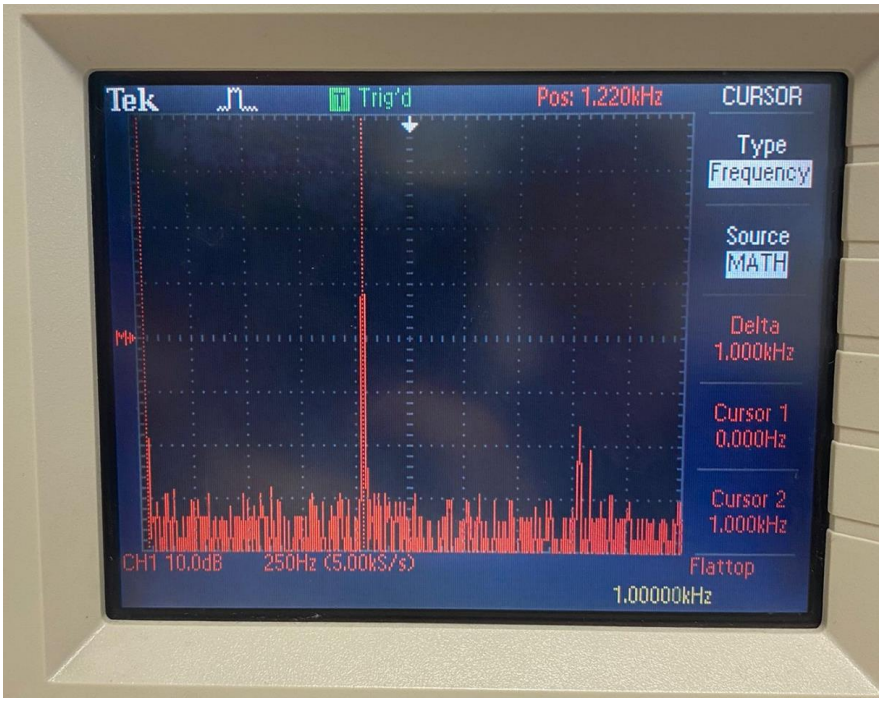


Fig3.7 harmonic content when input is 0.1sinwt

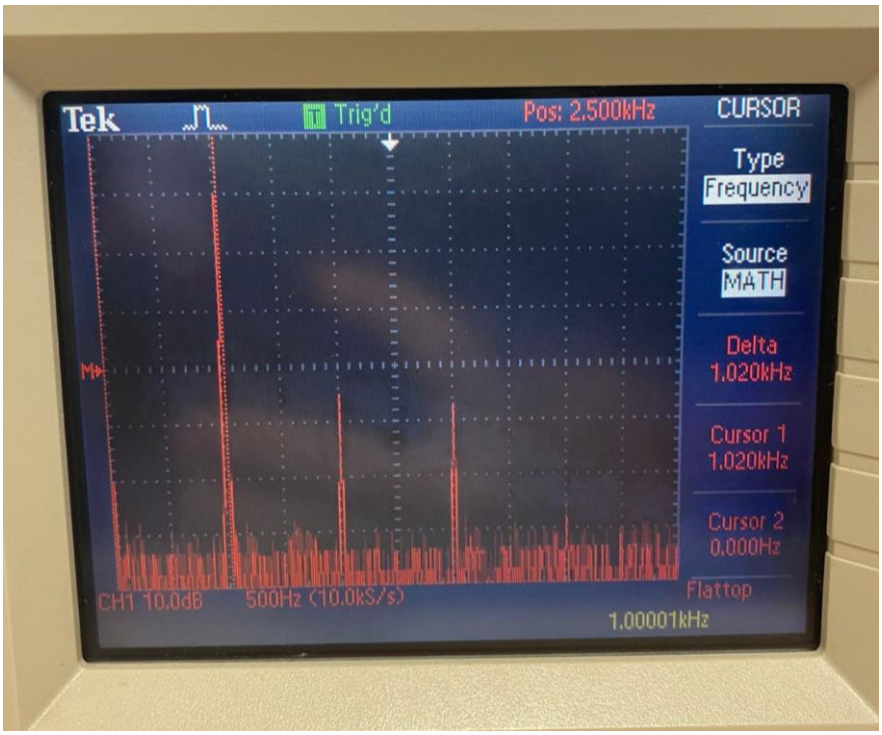


Fig3.8 harmonic content when input is 0.2sinwt

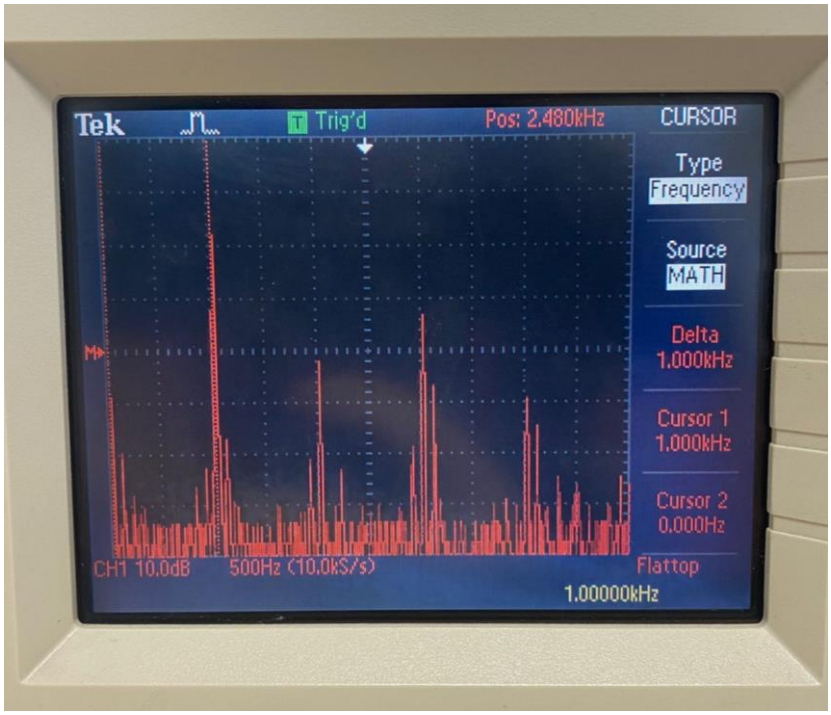


Fig3.9 harmonic content when input is 0.3sinwt

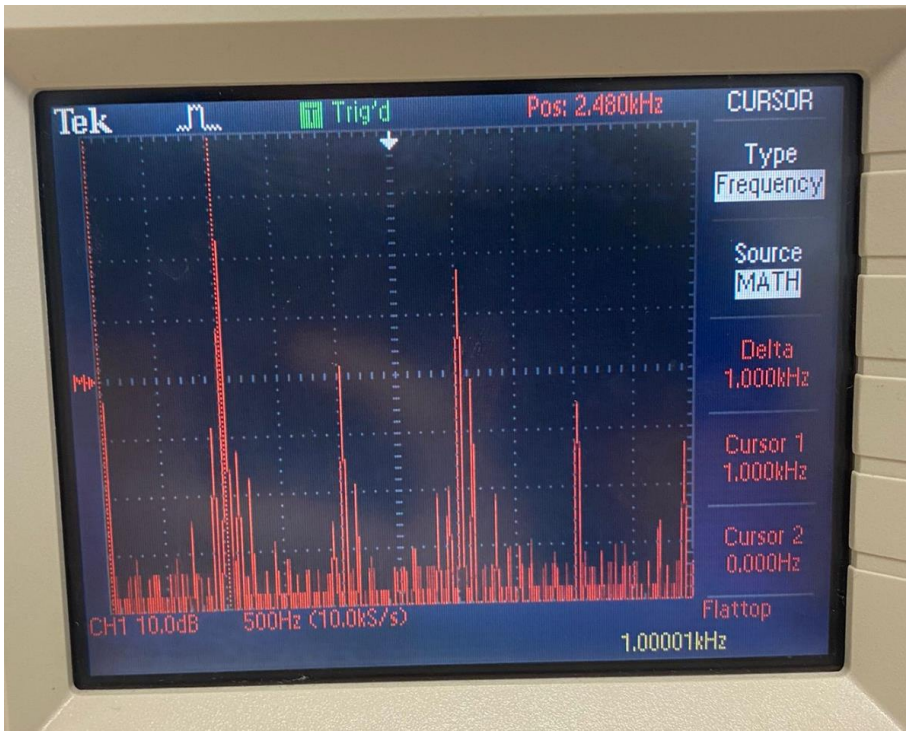


Fig3.10 harmonic content when input is 0.4sinwt

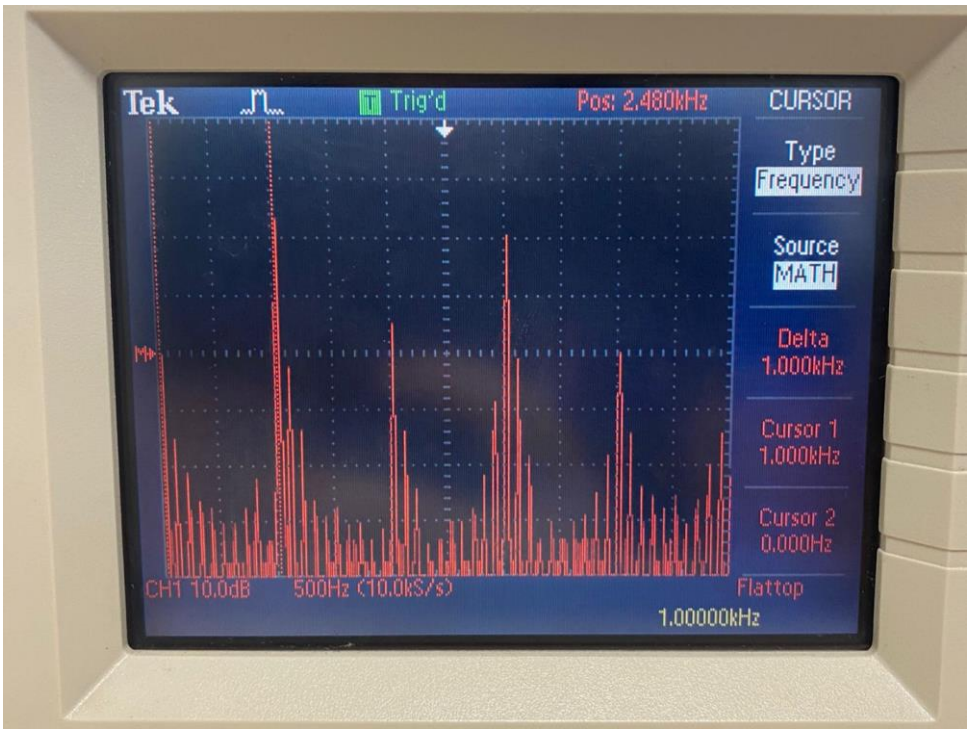


Fig3.11 harmonic content when input is 0.5sinwt

The important point while investigating the harmonic content is that the max value should be at 1kHz in all cases since the circuit is designed according to 1kHz input. Therefore it can be said that harmonic content observations also meets the requirements.

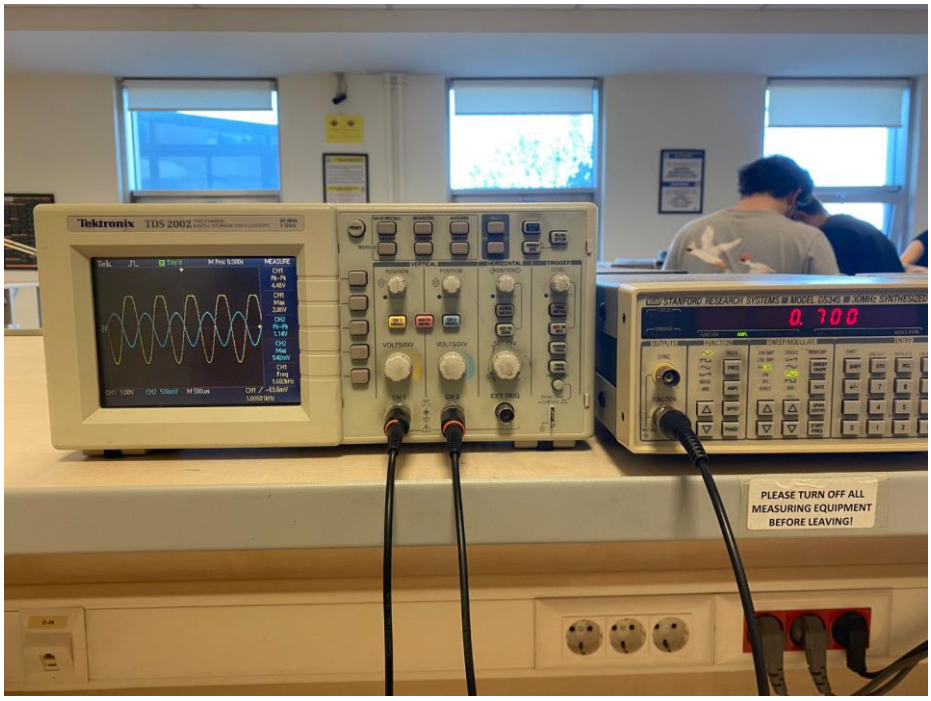


Fig3.12 Demontration of clipping

As it can be observed in the software results clipping occurs when ss input has an amplitude of 0.7V. The software and hardware designsgive the same result. Lastly the high and low -3 dB cutoff frequencies will be observed.

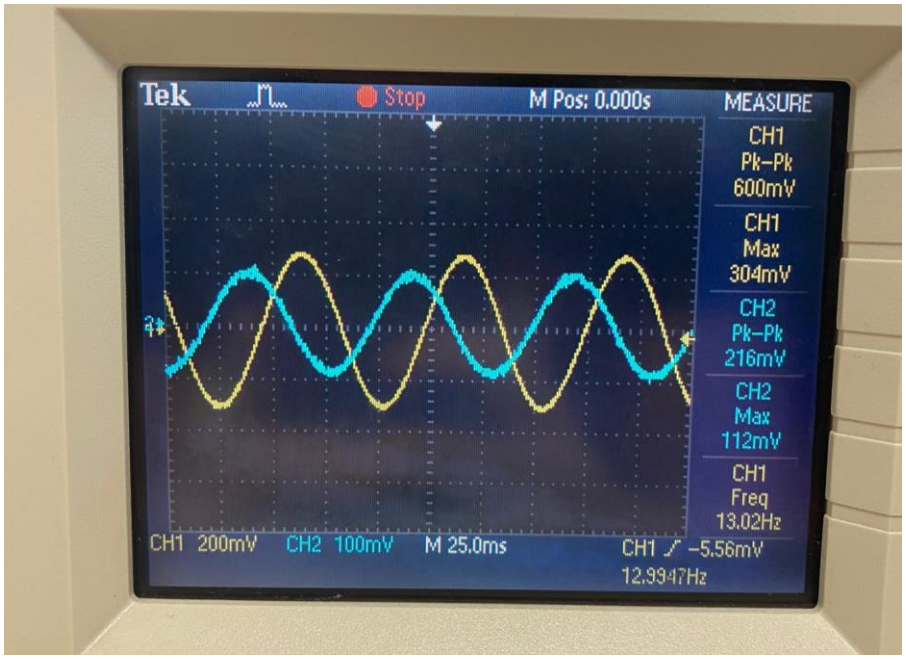


Fig3.13 low -3 dB cutoff frequency

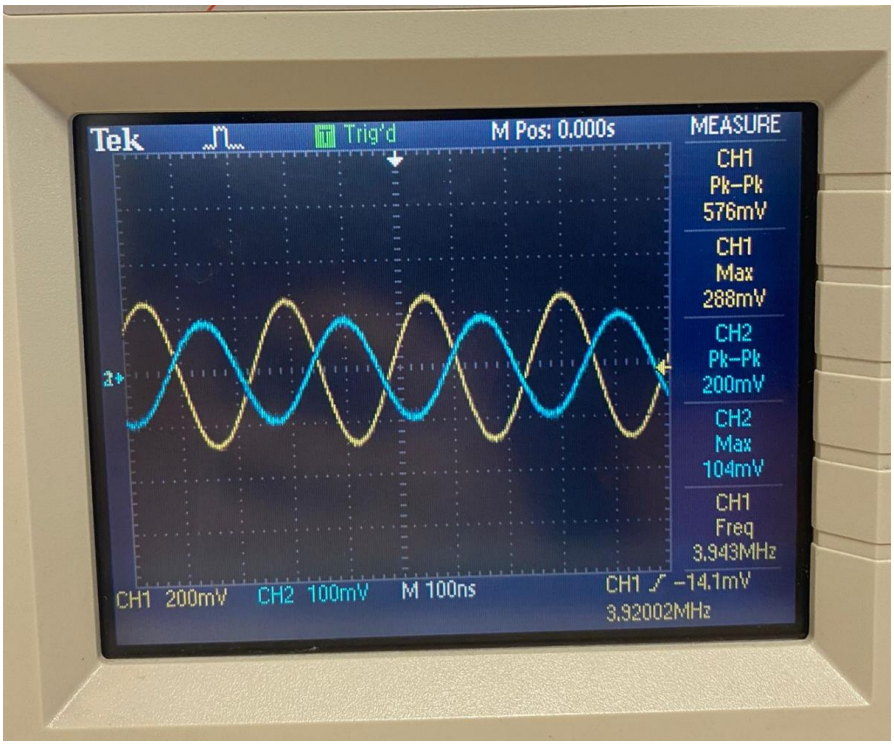


Fig3.14 high -3 dB cutoff frequency

According to Fig3.13 using -20log(600/216)=-8.87 dB. From Fig3.14 using -20log(576/200)=-9.18 dB which are approximately 3 dB lower than the gain.

	fLow	fHigh
Software	12.89Hz	4.00MHz
Hardware	12.99Hz	3.92MHz

Overall the results meet the desired specifications hence the circuit can be considered as successful.

Conclusion

In this labrotary work a common emitter stage cascaded with a voltage buffer is designed hence this lab assignment was useful to famialirize students with transistors, diodes, voltage amplifier circuits. Overall the software and hardware results are consistent with each other and precise with the desired specifications. The small differences are a result of excess resistence due to jumper cables, expansion due to heat, uncertainity of power supply and osciloscobe. The error in software may be a result of different software packages of the desired transistors. As it is highlighted, it can be concluded that the circuit operates as desired.