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Section-02

EEE202 CIRCUIT THEORY LAB1 REPORT

Time-Domain and Frequency-Domain Analyses

In this lab assignment, frequency-domain and time-domain analyses of RL circuit, inverting and integrating opamp circuits is done.Solving necessary mathematical equations and using LTSpice will give theoratical values of circuit components and results which will be further compared with hardware implementation.

Software Lab

First Part: Time-Domain Analysis

The software lab consists of three parts.In the first part it is desired to establish a circuit that has a voltage supply and two resistors.The circuit is investigated in time_domain.Voltage supply is set to 10 volts peak to peak and a frequency of 500 kHz.R1 is set to 4Ω and R2 is set to 16Ω.Value of node2 gives teh potential difference on R2 which is the output voltage.The circuit is demonstrated in

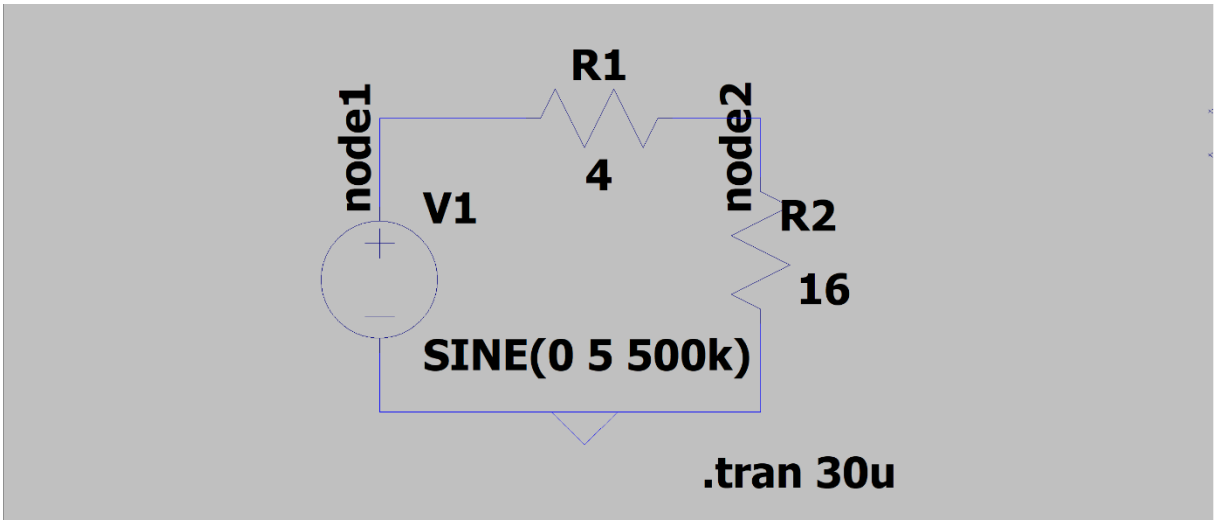

Fig1.1.

Fig1.1 demonstration of the circuit.

The output voltage can be calculated using the voltage divider formula which is:

$$V_0 = V1\frac{R2}{R1 + R2}$$

$$V_0 = 5\frac{16}{4 + 16}$$

$$V_0 = 4V$$

The simulation in time-domain of output voltage can be seen in Fig1.2

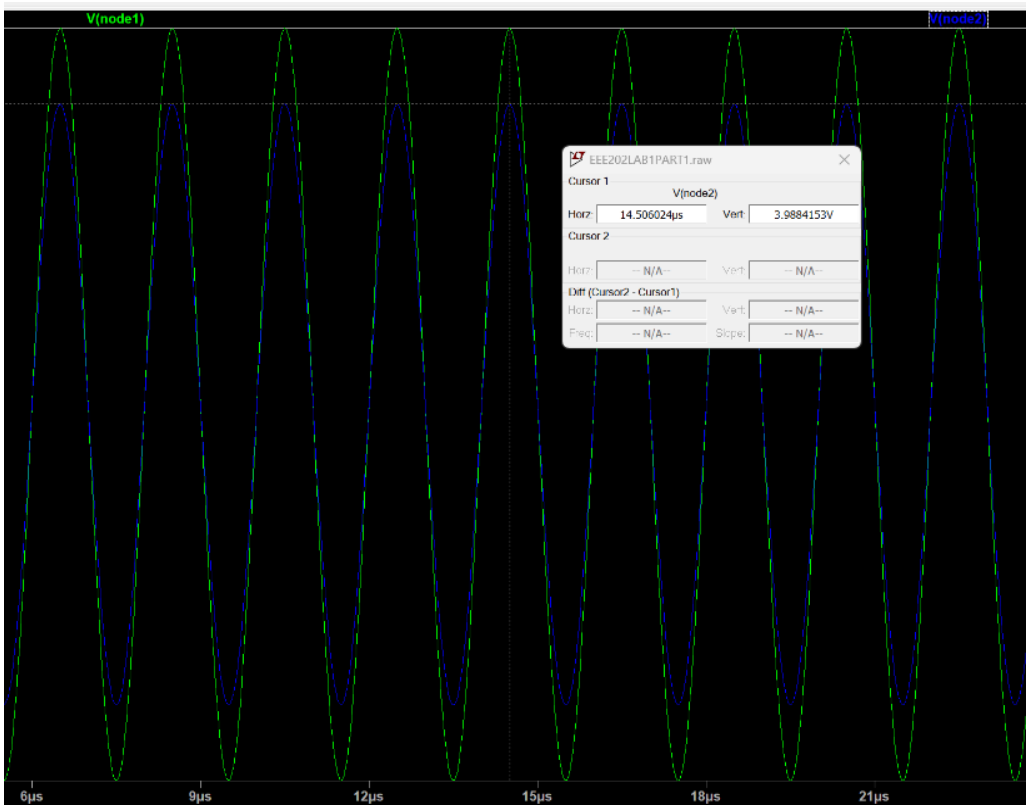

Fig1.2 demonstration of simulation result.Blue traces demonstrate the output voltage and green traces demonstrate the input voltage

Now R2 is replaced with a 100 µH inductor, R1 is replaced with a 25Ω resistor and frequency of voltage supply is switched to 100 kHz.The descripted circuit can be seen in Fig1.3.

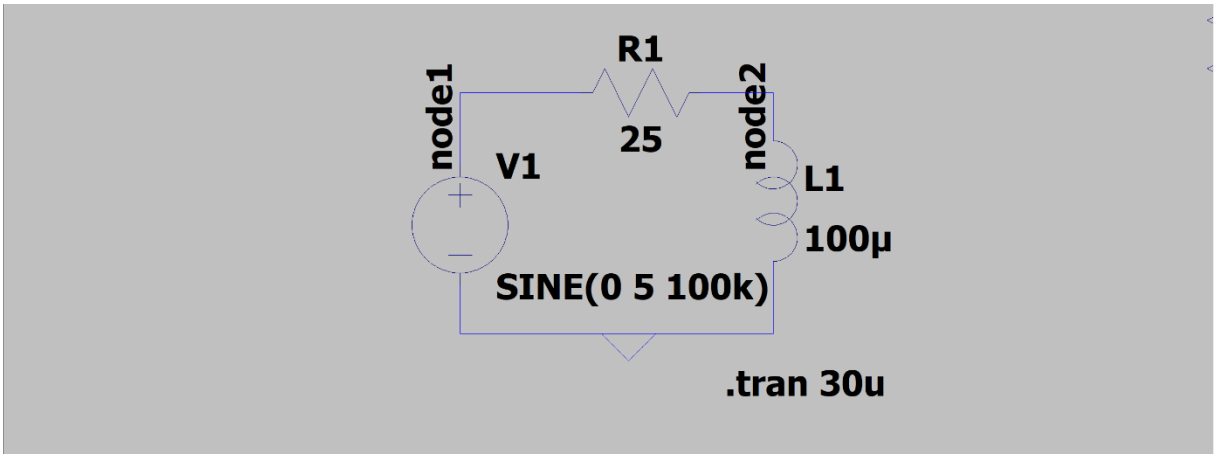

Fig1.3 desired RL circuit.

In this part it is desired to determine what kind of a filter is this RL circuit.By switching frequency to 10kHz and 500Khz it will be observed.

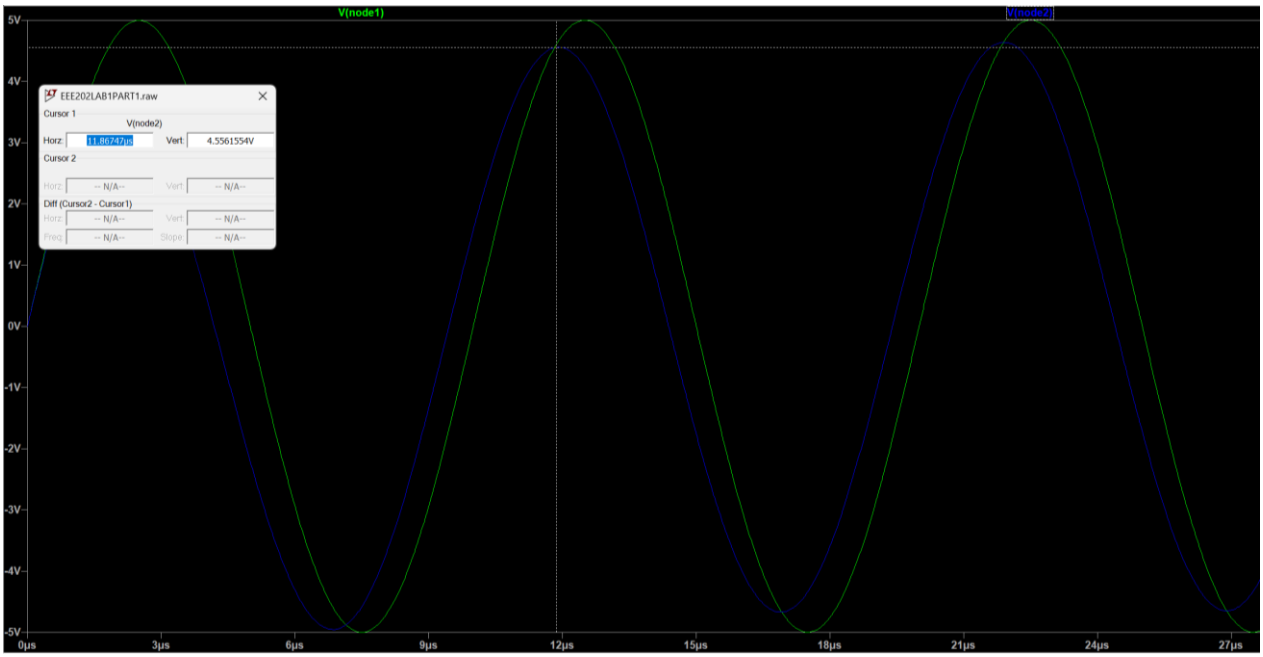

Fig1.4 output voltage observed in 100kHz

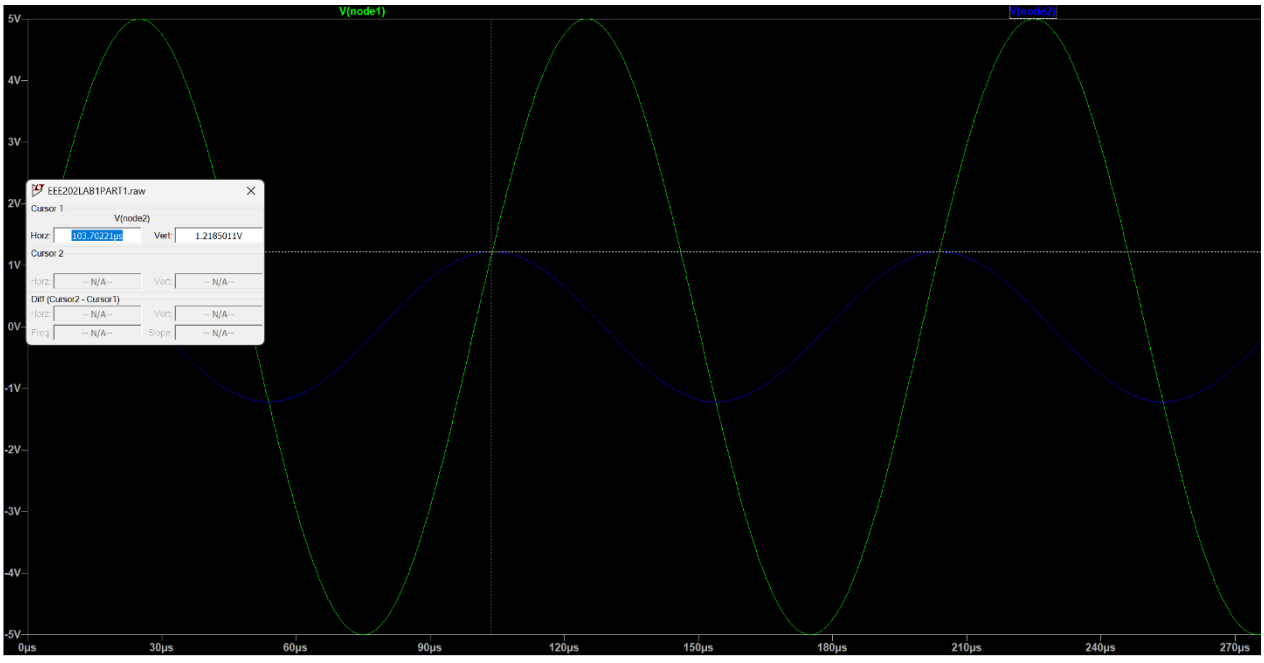

Fig1.5 output voltage observed in 10kHz

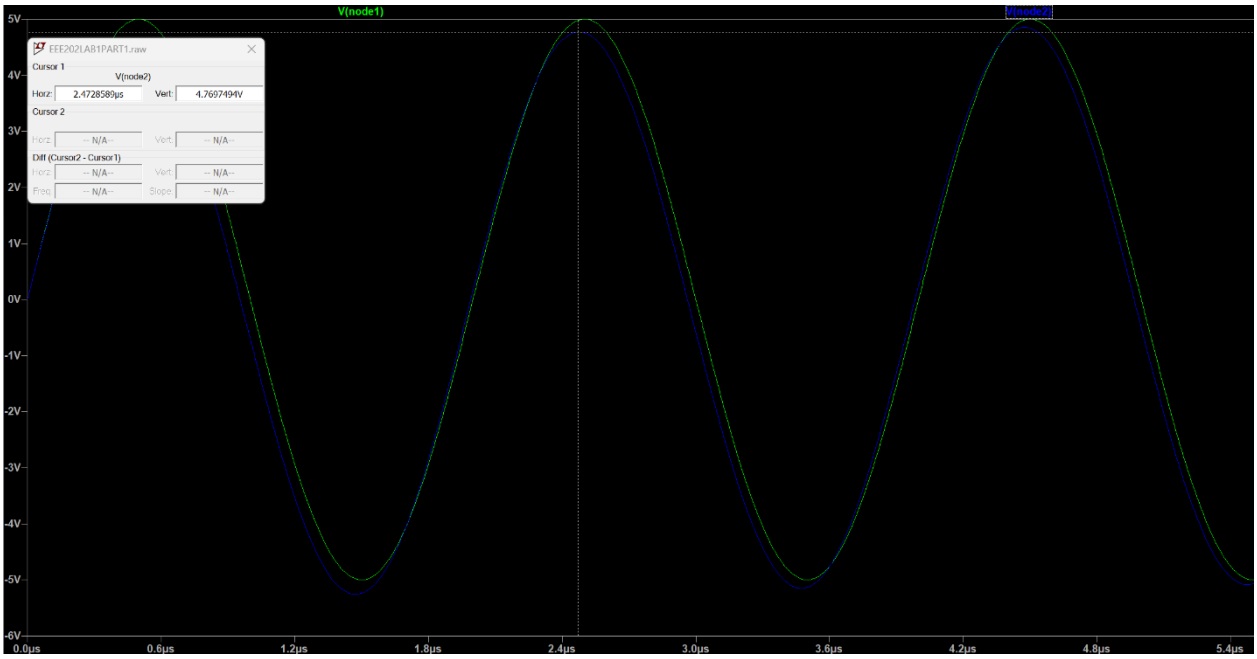

Fig1.6 output observed in 500kHz

As it can be seen, the output voltage decreases as the frequency of sine wave decreases and output voltage increases as the frequency of sine wave increases.This illustrates that established RL circuit is a high pass filter.

Second Part: Frequency-Domain Analysis

In this part, frequency-domain analysis is done on a RL circuit considering the serial resistance of the power supply in the labratory.A 50Ω resistance is connected series with the resistance of 33Ω and an inductor of 100 µH(Fig2.2).The gain of the circuit is investigated with respect to frequency.AC analyses setting is shown in Fig2.1.

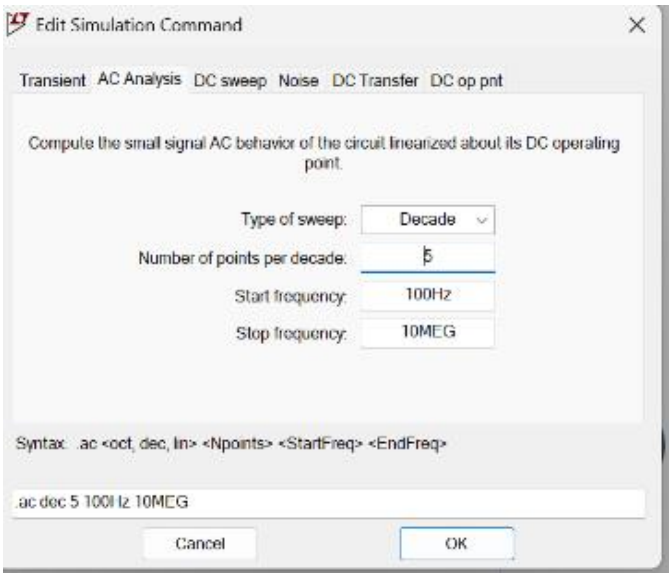

Fig2.1 setting of AC analysis

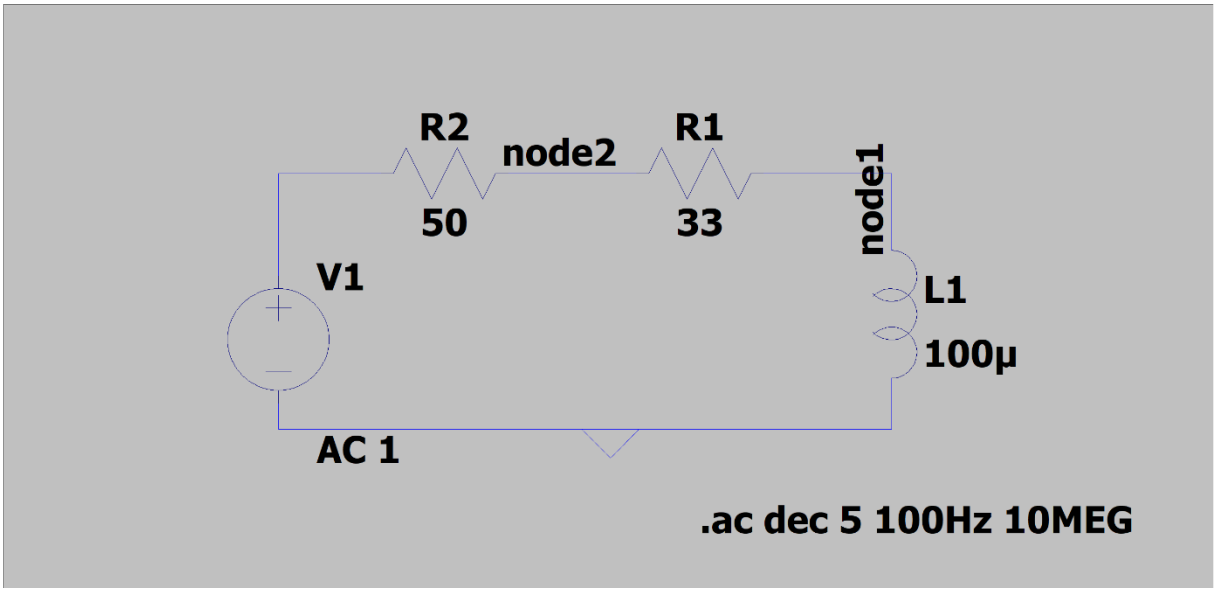

Fig2.2 demonstration of the RL circuit with internal resistance of voltage supply

In order to have a better understanding of serial internal resistance of the power supply frequency domain analysis is done by including and without including serial internal resistance.

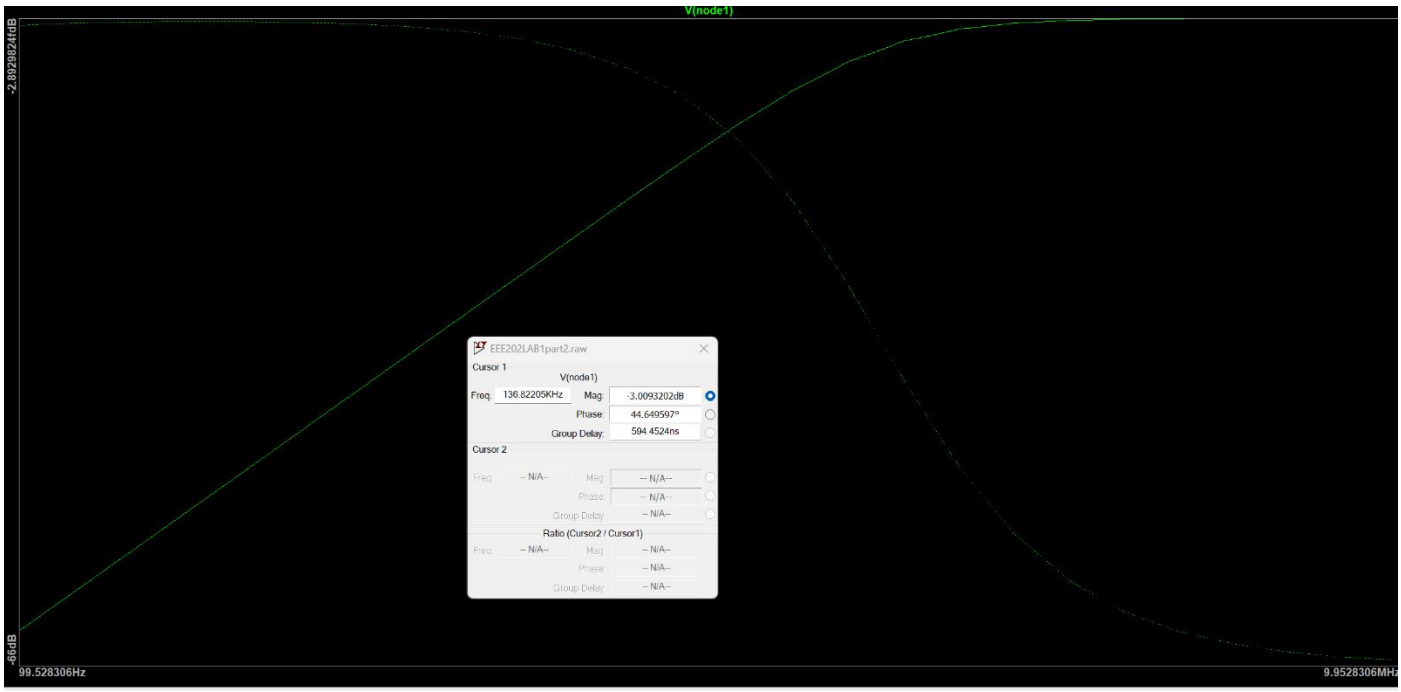

Fig2.3 simulation result including the internal resistance

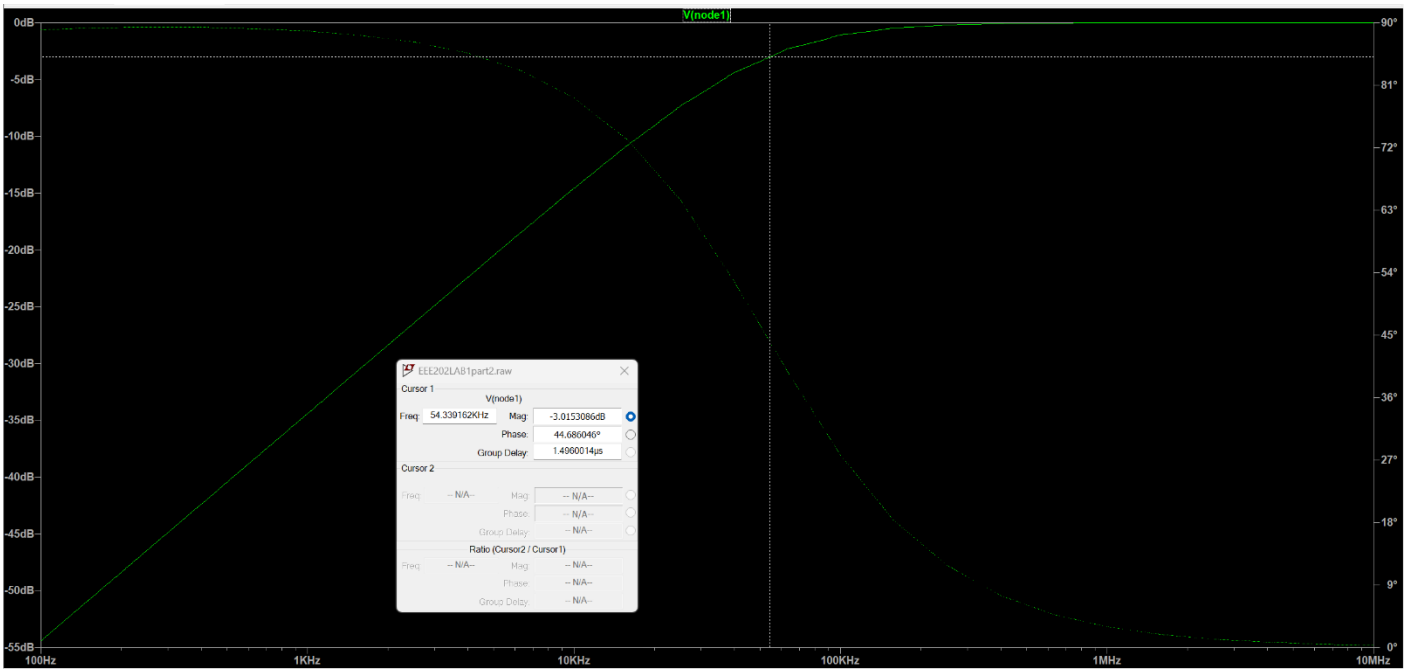

Fig2.4 simulation result without including internal resistance

	Gain	Cutoff frequency
Without resistance	-3.0dB	136.82kHz
Including resistance	-3.0dB	54.33kHz

Table1.1

Cutoff frequency of the high pass filter can be found as:

$$f_c = \frac{R_{eq}}{2\pi L}$$

By including 50Ω internal resistance R_{eq} increases therefore f_c increases and pass band area decreases.As a result it can be said that including internal resistance of the power supply increases the -3dB cutoff frequency and reduces pass band area of the high pass filter compared to the situation where serial internal resistance is not included.

Third Part: OPAMP Circuits

In this part of the lab, two opamp circuits are established.These circuits are inverting and integrating opamp circuits respectively.First inverting opamp circuit is observed.8V and -8V voltage sources are connected to LM324 opamp models for the saturation range.The aim of the inverting opamp circuit is to invert or reflect the input voltage with respect to horizontal axis and alernate the magnitude by the relation between resistors.The establishhed circuit can be seen in Fig3.1.

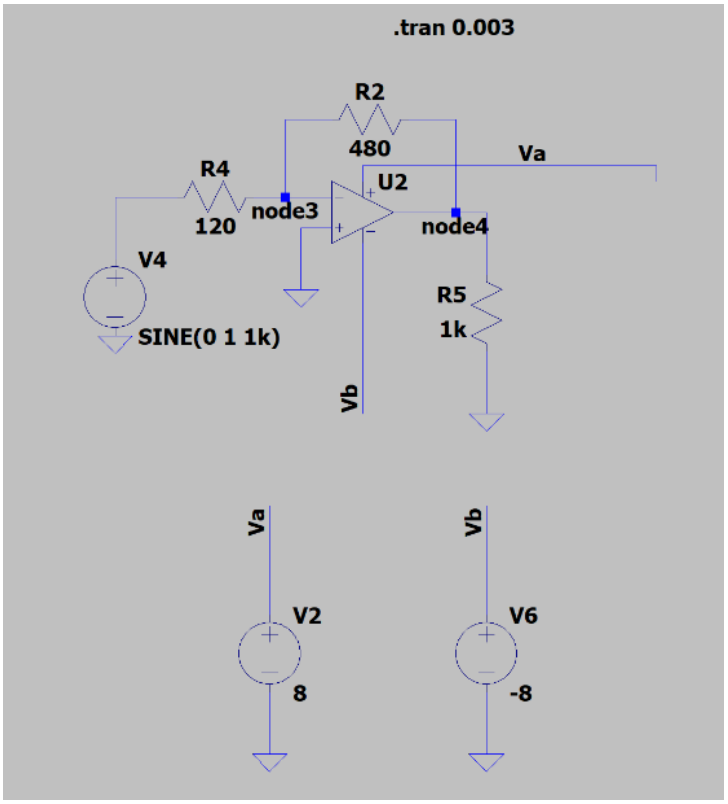

Fig3.1 demonstration of inverting opamp circuit

The output magnitude can be found by using nodal analysis.

$$(V_{node3} - V4)\frac{1}{R4} = (V_{node4} - V_{node3})\frac{1}{R2}$$

$$V_{node3} = 0$$

$$V_{node4} = -V4\frac{R2}{R4}$$

$$V4 = 1V, \qquad R2 = 480\Omega, \qquad R4 = 120\Omega$$

$$V_{node4} = -4V$$

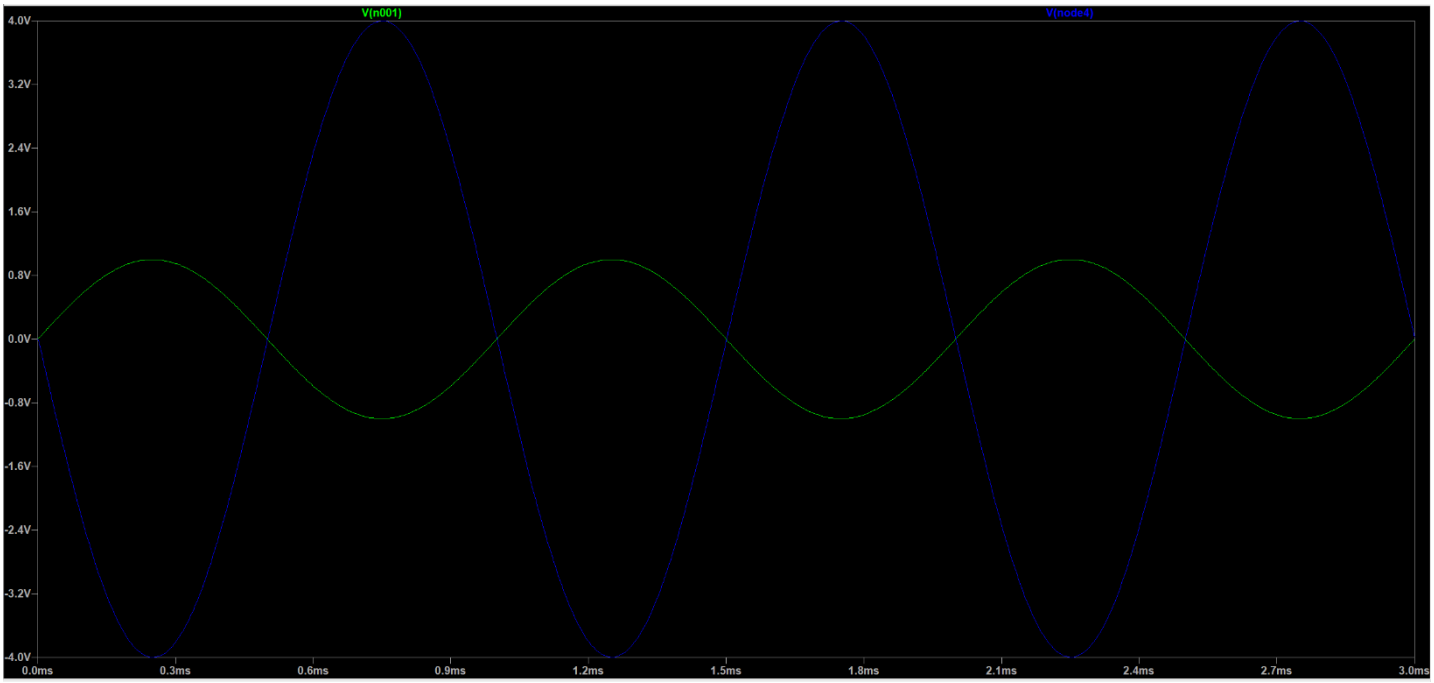

Fig3.2 simulation result of inverting opamp circuit

This circuit inverts the input signal and multiplies it by 4 due to the ratio between R4 and R2.The output voltage is 4V peak to peak.The saturation of opamp can be observed with higher ratios of R4 and R2.

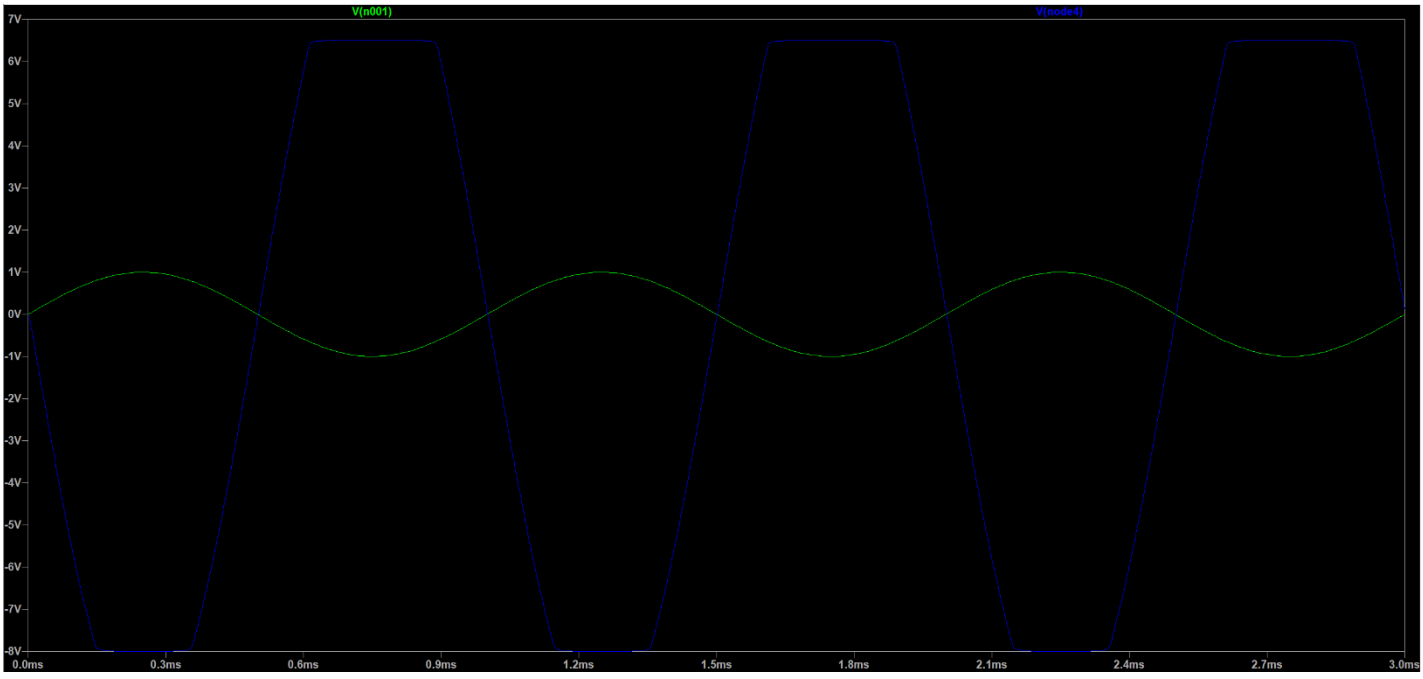

Fig3.3 saturation of opamp

Since the linear reigeon is between -8V and 8V when the ratio between R4 and R2 is 10 opamp is saturated as it can be seen in Fig3.3.

Now by replacing R2 with a 3 nF capacitor and replacing R4 with 8kΩ resistor an integrating opamp circuit is established.Purpose of the integrating opamp circuit is to get integral of the input signal and give it as the output signal .The integrating opamp circuit can be seen in Fig3.4.

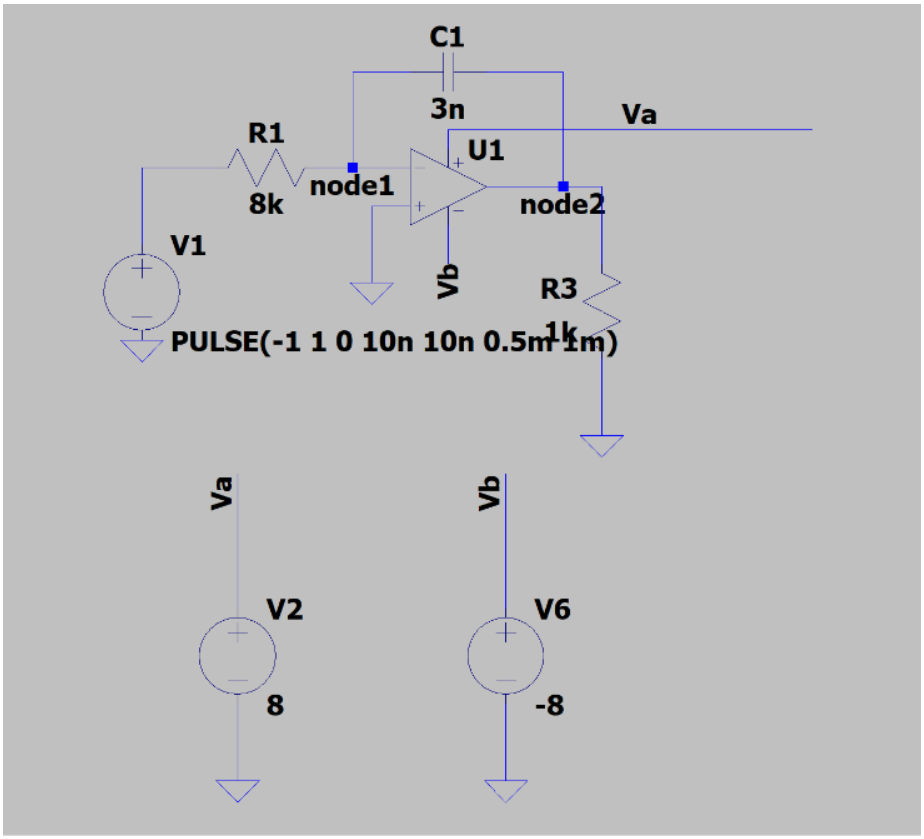

Fig3.4 demonstration of integrating opamp circuit.

The calculation for output voltage is as following:

$$(V1 - V_{node1})\frac{1}{R1} = i_C$$

$$V_{node1} = 0 \quad , \quad i_C = C1\frac{dV_{node2}}{dt}$$

$$V_{node2} = -\frac{1}{R1C1}\int_0^t V1dt$$

$$R1 = 8000\,, C1 = 3nF\,, height\ of\ square\ is\ 1V\ width\ of\ half\ wave\ is\ 0.5\ ms$$

$$V_{node2-min} = -20.83V$$

The expected theoratical value for output voltage is found as 20.83V.Since this value is out of linear reigeon the opamp will be saturated in the simulation.

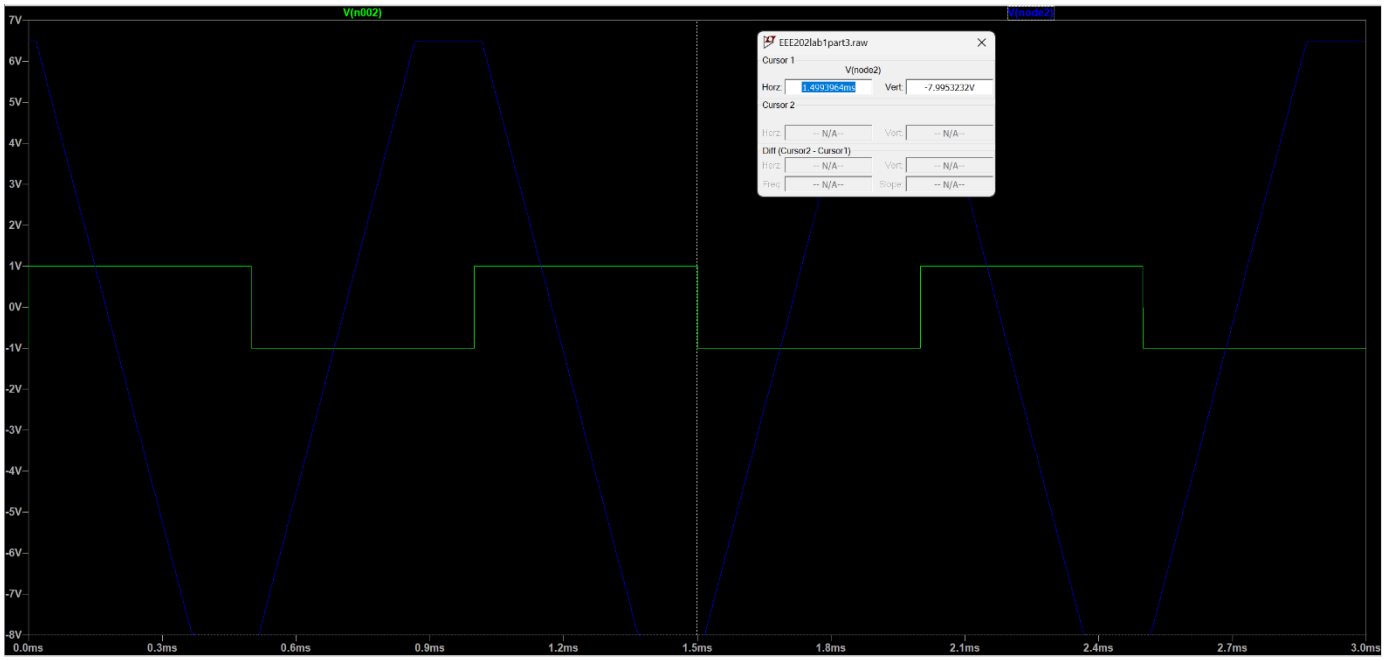

Fig3.5 simulation of integrating opamp circuit

As it can be seen output voltage waveforms are similar to waveforms in Fig3.3 which means opamp is saturated.For the integrator circuit since it integrates the input waveform, a triuangler waveform is expected as the output of a square wave input.However in this case min-max values of the expected triuangular waveform is out of linear reigeon therefore opamp becomes saturated and a truncated triangle waveform is observed.

Hardware Lab

In the hardware lab, experimental results are compared with previously calculated theoratical and observed simulation results.In the hardware part RL circuit and opamp circuits from software labs are observed.

First Part: RL High Pass Filter

In the first part high pass filter RL circuit is established on the breadboard with 5V amplitude voltage supply and 10kHz, 100kHz, 500kHz frequencies are applied and peak to peak voltages are observed.Observed peak to peak voltages are as following:

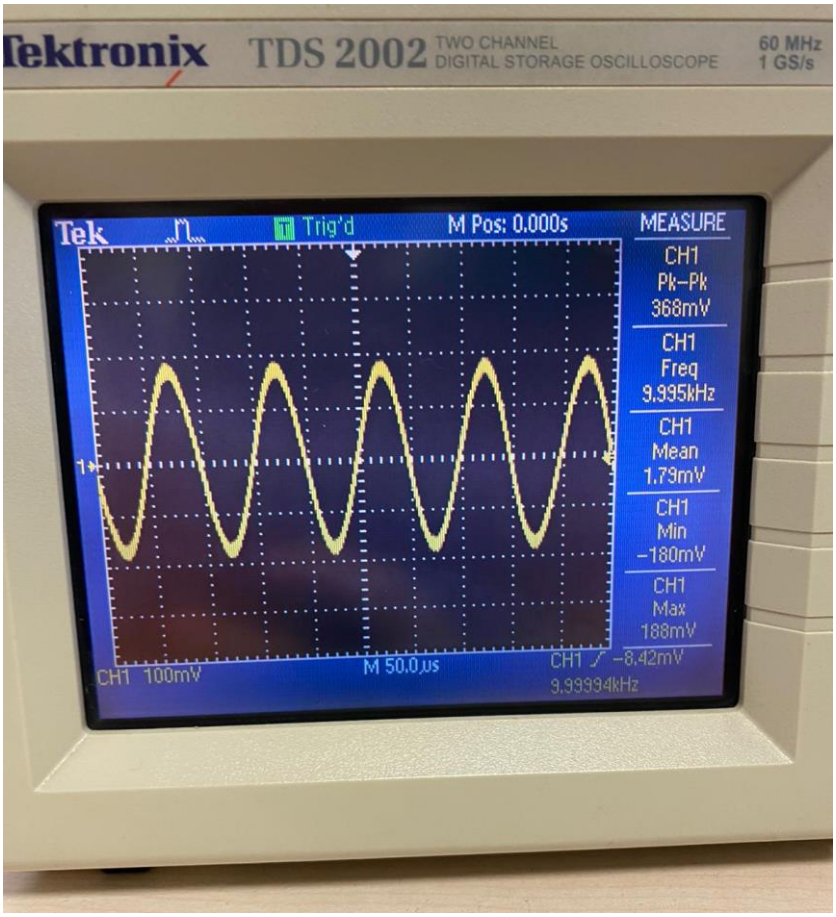

Fig4.1 applying 10kHz, observed peak to peak voltage is 368mV

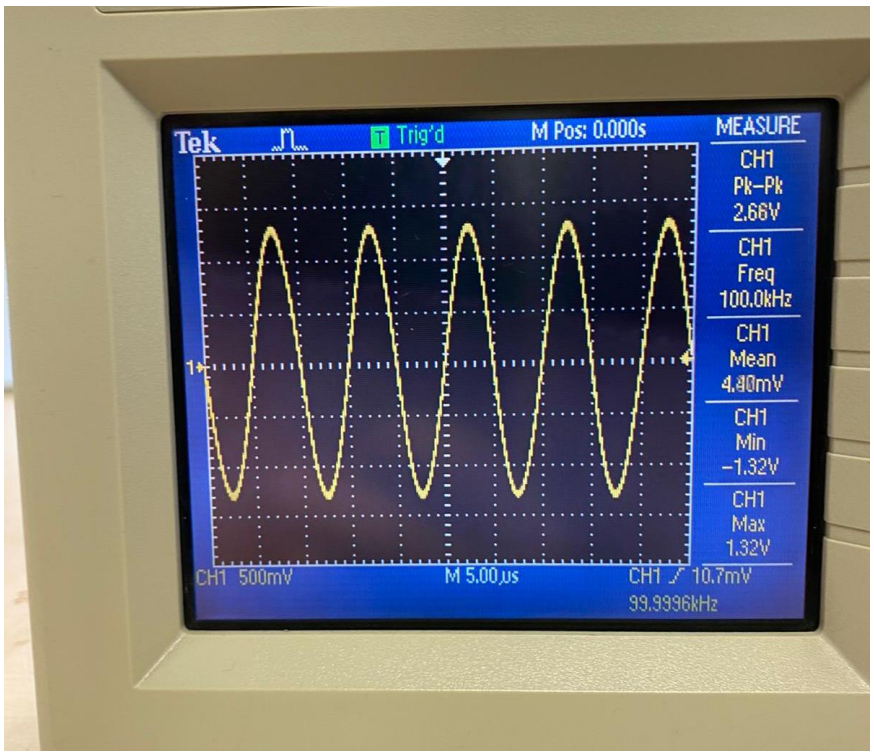

Fig4.2 applying 100kHz, observed peak to peak voltage value is 2.66V.

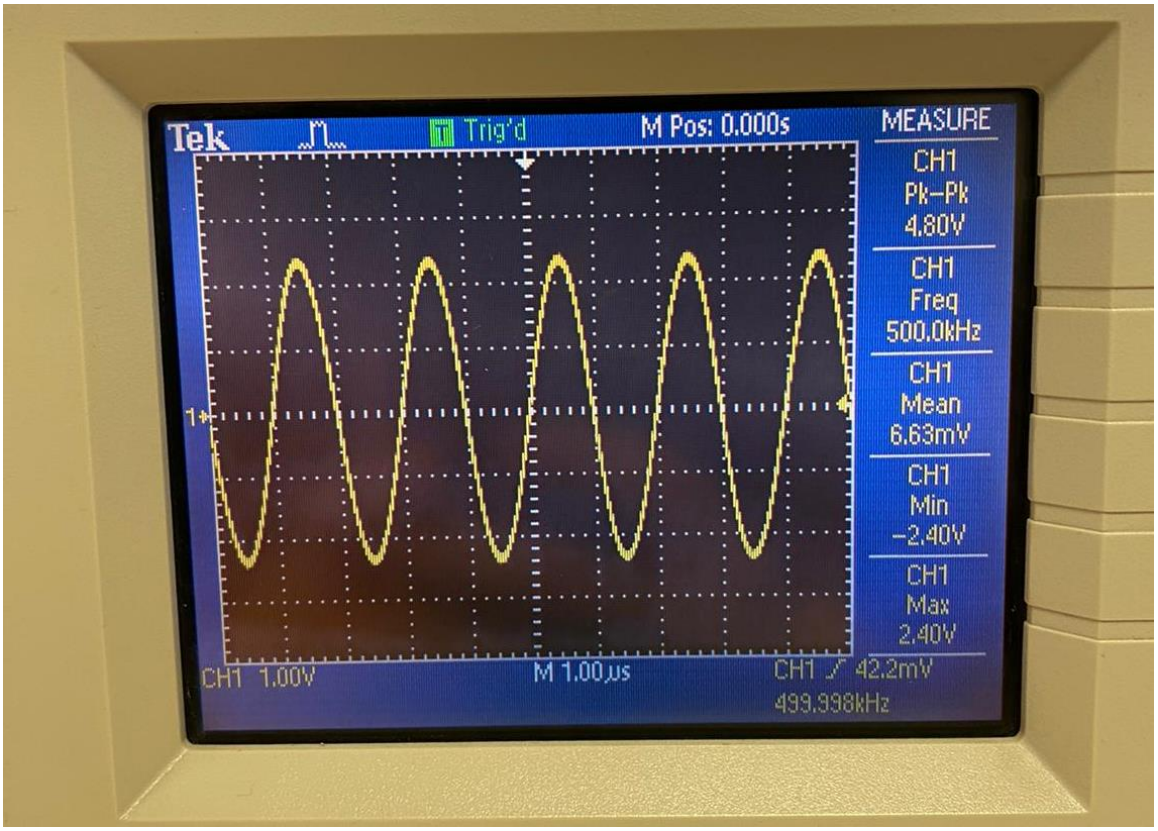

Fig4.3 applying 500kHz ,observed peak to peak value is 4.80V.

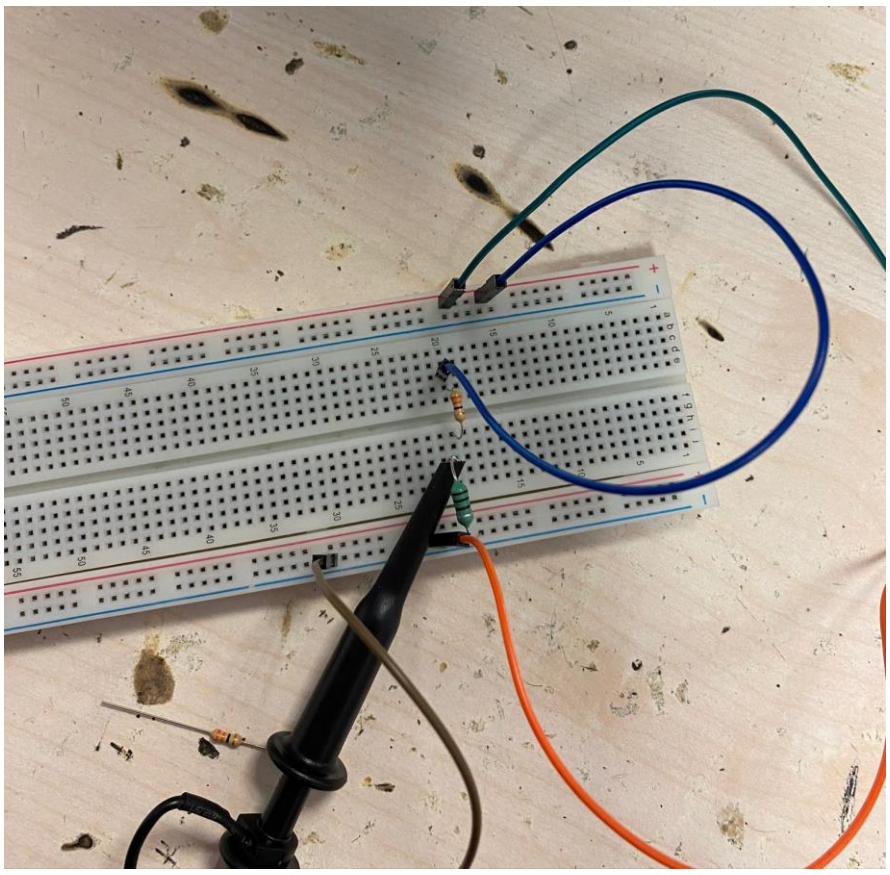

Fig4.4 implementation of high pass RL circuit on breadbord.

Frequency	Output voltage	Gain(decibel)
9.995kHz	368mV	-22.66
100kHz	2.66V	-5.48
500kHz	4.80V	-0.35

Table 1.2 table ofexperimental results

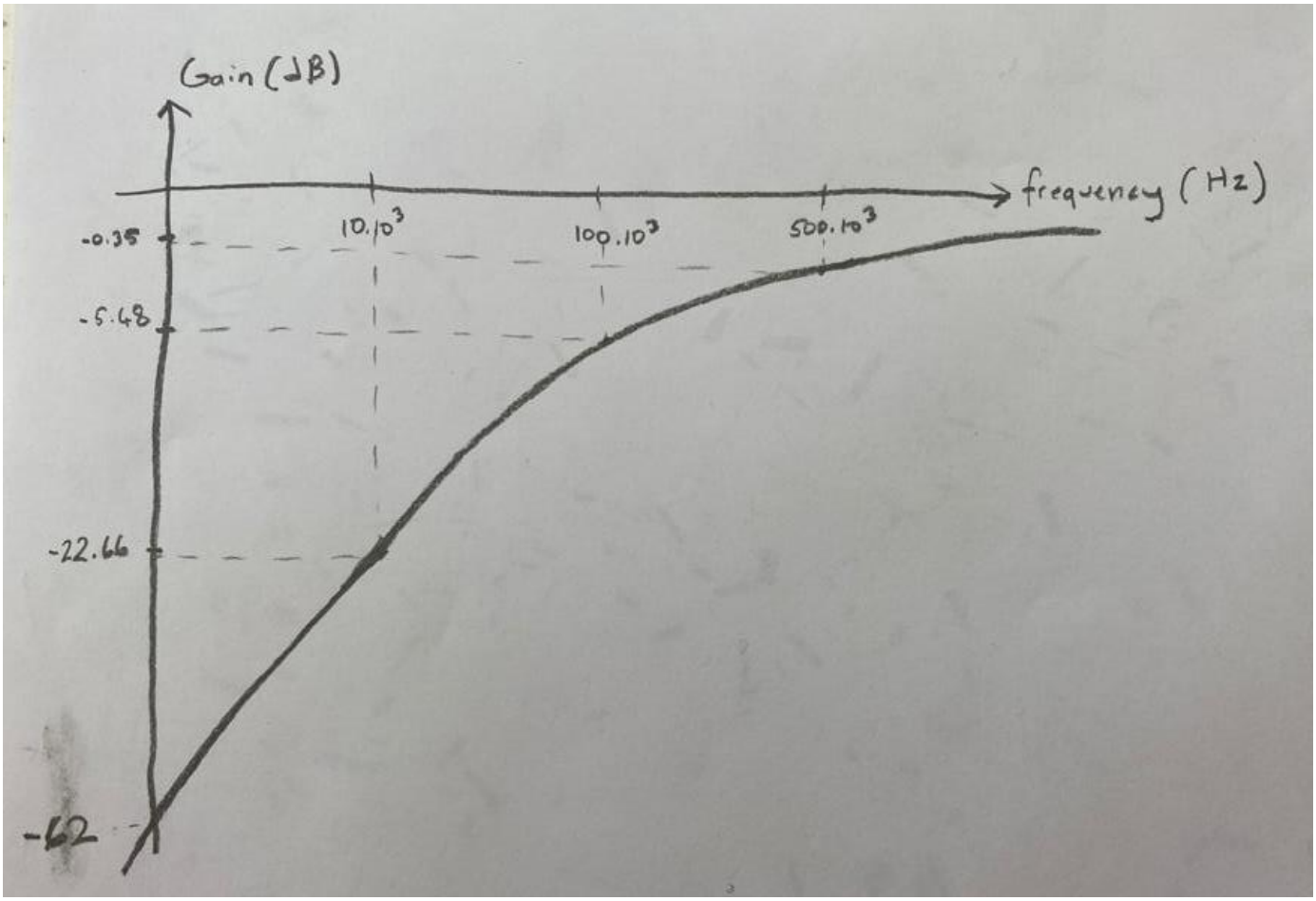

Fig4.5 plot of gain with respect to frequency using experimental results.

Frequency:	10kHz	100kHz	500kHz
Software gain(decibel)	-22.15	-4.30	-0.21
Hardware gain(decibel)	-22.66	-5.48	-0.35

Table1.3 comparison of gain between software and hardware labs

As the frequency increases peak to peak voltage value increases and gain approaches to 0db which means that ratio of input and output voltage approaches to 1.The hardware results confirms the software lab results since thje slight difference is between the error range.

Second Part: Opamp Circuits

In this part inverting and integrating opamp circuits are established on breadbord using LM32 4.First the inverting opamp circuit is observed.For the linear reigeon -8V and 8V are connected to the opamp.

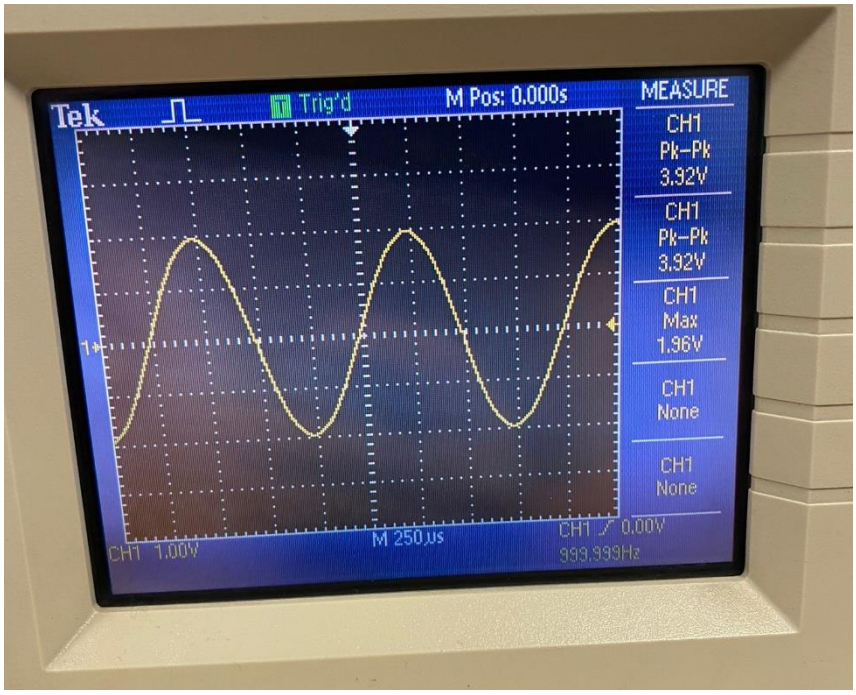

Fig4.5 output waveform of inverting opamp circuit.

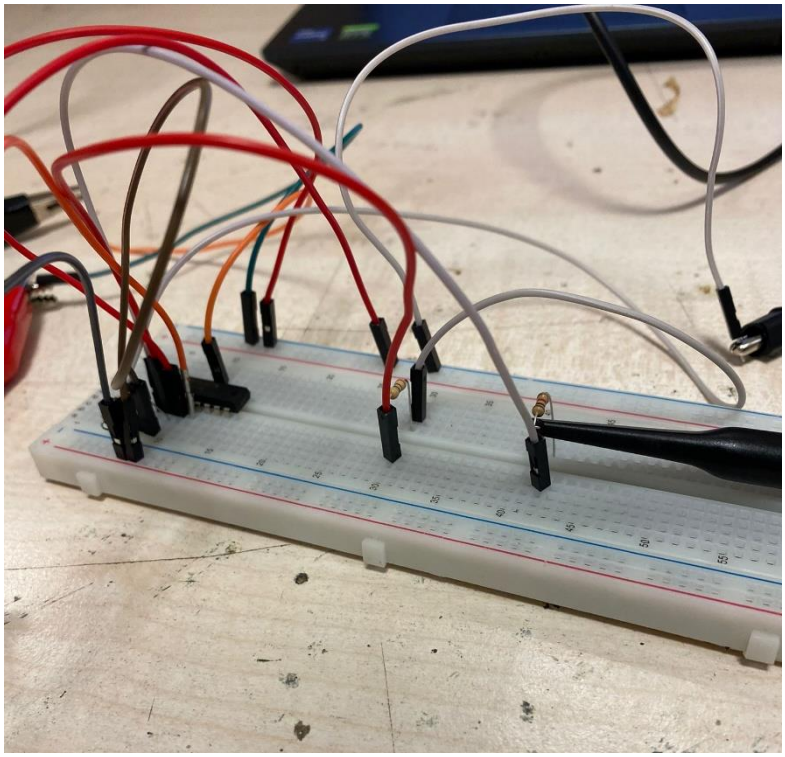

Fig4.6 implementation of inverting opamp circuit on breadboard

In order to invert and amplify the input signal by 4 the ratio of $\frac{R4}{R2}$ must be equal to 4 as mathematically given in the software part.By considering the serial internal resistance of the power supply 120Ω and 680Ω resistors are connected to obtain the desired ratio.Input signal is 1V peak to peak and obtained output waveform has 3.92V peak to peak and expected peak to peak voltage is 4V.The result 3.92V is valid since it does not exceed the error band.Moving onto integrator opmap circuit, again 1V peak to peak is given and following result is observed:

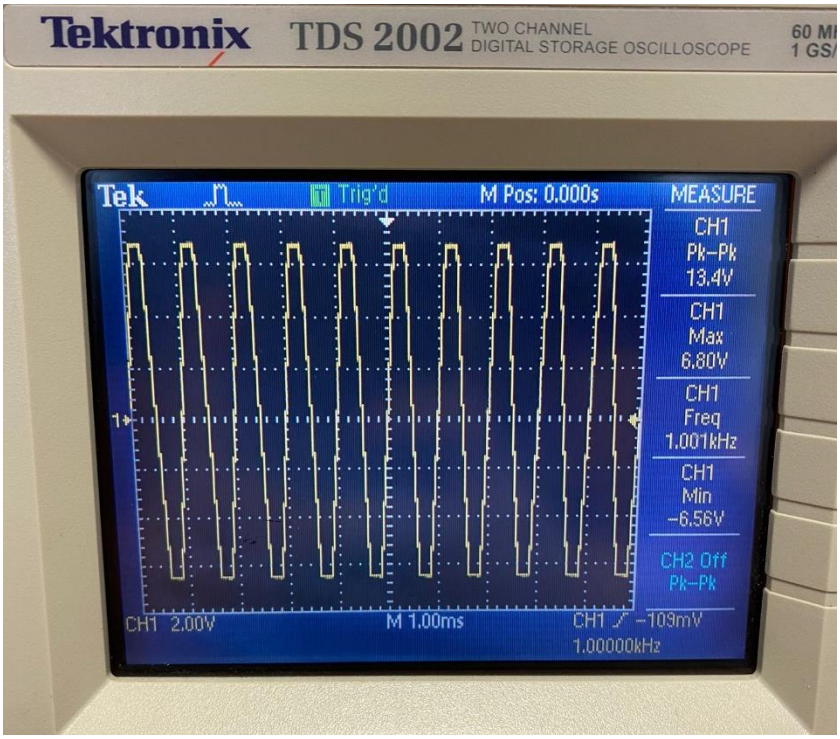

Fig4.7 output waveform of integrator opamp circuit.

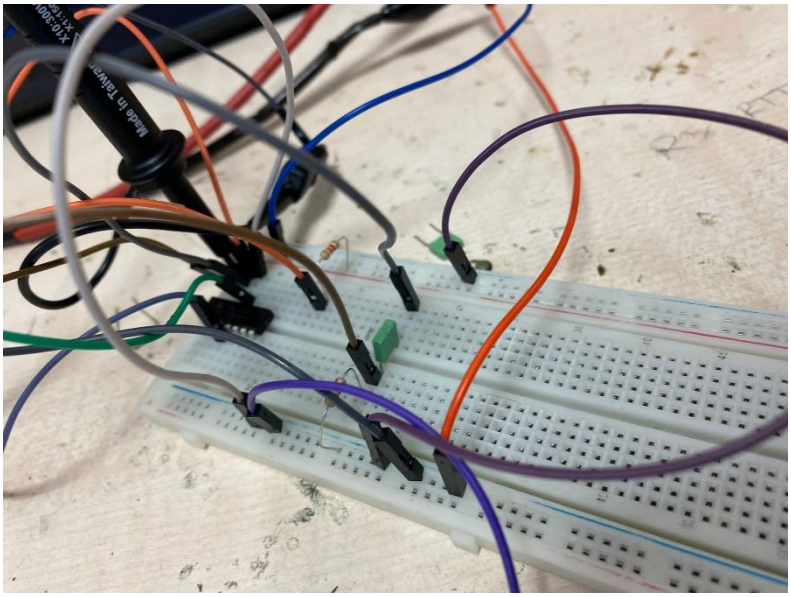

Fig4.8 integrating opamp circuit implementation on breadboard.

Similar to the software simulation result, opamp becomes saturated and a truncated triangle waveform is obtained with similar max-min or peak to peak values.14.1V peak to peak in software simulation and 13.4V peak to peak in experimental result.

Conclusion:

This assignments main purpose is to familiarize students with time-domain, frequency-domain circuits and providing better understanding of filters and opamp circuits.For the RL circuit three different frequencies are tested in order to determine the filter type of the circuit.It is observed that when the frequency is increase gain approaches to 0db which means the RL circuit is a high pass filter.It is also tested in hardware lab and confirmed.The lab work continues with opamp circuits which are inverting and integrating opamp circuits.The necessary mathematical equaitons are solved and theoratical values for output voltages are obtained and these values are compared with software simulation results.The experimental results are valid since they do not exceed the error band however there are slight error which may be results of uncertainity of power supply and oscilloscope, small resistance of jumper cables and human error.