EEE 415 Spring 2024/25 Project Report

Introduction

The aim of this proect is to design an IC OPAMP that meets the required specifications. Throughout the report the design methadology is explained which is followed with the layout design of the IC. Check Table 1 for project specifications. The used technology in the design is XFAB 180nm PDK with a supply voltage of 1.8V. In the design 10μA reference current is used.

Power Consumption	< 1mA
Open loop DC gain	>100dB with 5kΩ connected to the output
Unity Gain Bandwidth	>10MHz
Phase Margin	> 45 °
Output Voltage Swing	0.4V-1.4V
Output Referred Voltage Noise	$< 60\text{Nv}/\sqrt{Hz}$ at 10kHz
Driving Capacitance	Should be able to drive at least 5Pf capacitance

Table 1 Project specifications

Schematic and Results

The design is 3 stage OPAMP design in which the first two stages are responsable for high gain and the last stage is responsible for high output voltage swing. The first stage is selected as 5 transistor OTA to be able to convert differential input to single ended output. The biasing of the circuit is done with current mirroring and there are two current mirror branches where one of the current mirror branch is nmos current mirroring and the other one is for pmos current mirroring. The schematic can be observed in Figure 1. It is also benefitial to mention that Nested Miller Compensation is used for the frequency compensation meaning that there is a capacitor between outputs of second stage and third stage and, another capacitor between the outputs of first and third stage. The values of capacitors are 300Ff and 600Ff respectively. The DC biasing of the circuit can be observed in Figure 2 and all of the transistors are in reigon 2 which corresponds to SAT. The W/L ratios and current flowing through of 13 transistors can be observed in Table 2. In Table 2 the transistor numbers in Figure 2 is considered.

In the last stage minimum lenght transistors are used to minimize output resistance. In this circuit, output resistance is close to 5kΩ which is demonstrated by the GBW Figures in the following parts.

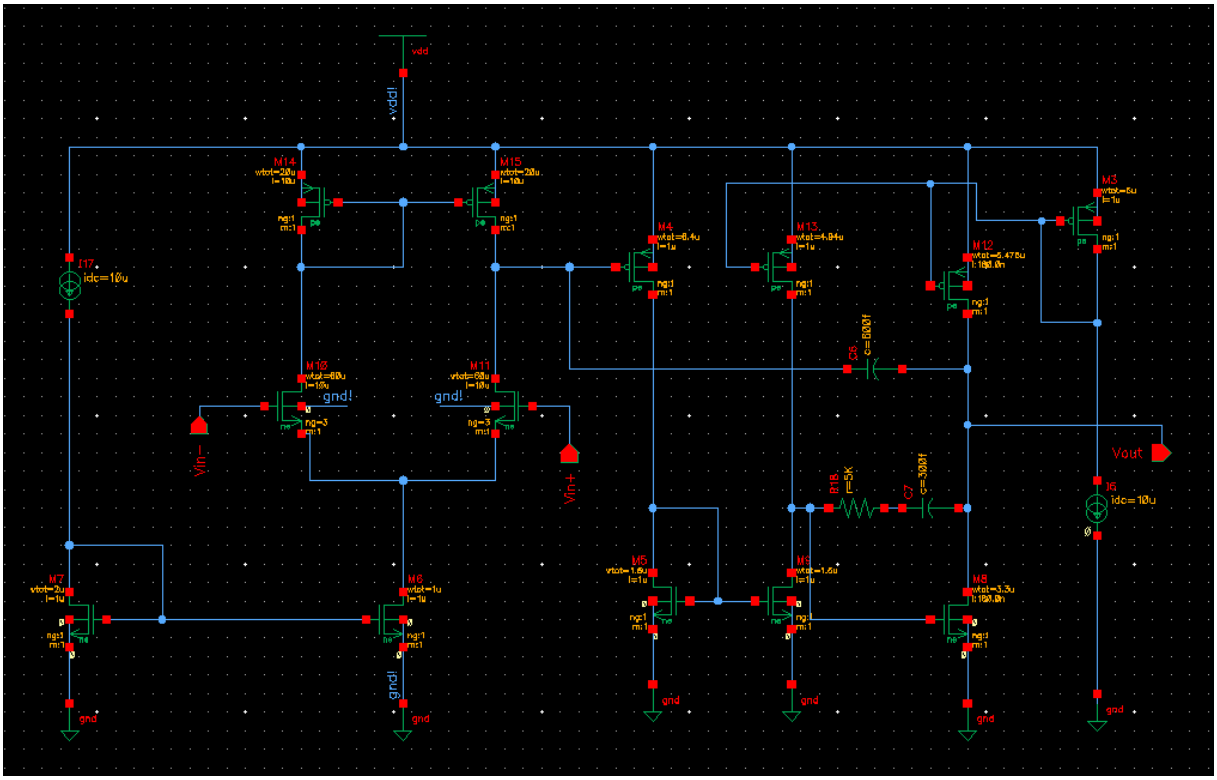

Figure 1 OPAMP design schematic

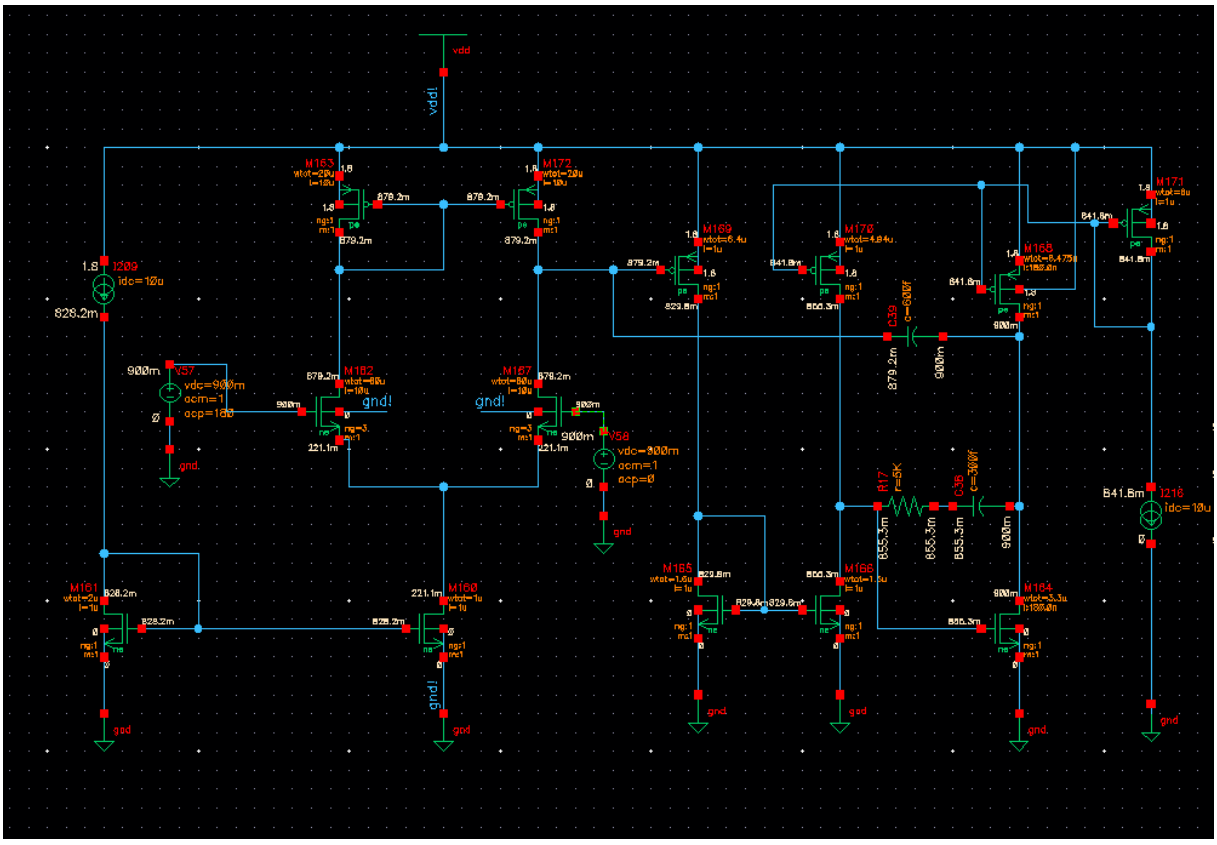

Figure 2 DC node voltages of the circuit

Transistor	W	L	W/L	Finger	Current (µA)
M161	2µm	1µm	2	1	10
M160	1µm	1µm	1	1	5.161
M162	20µm	10µm	6	3	2.581
M167	20µm	10µm	6	3	2.581
M163	20µm	10µm	2	1	2.581
M172	20µm	10µm	2	1	2.581
M169	6.4µm	1µm	6.4	1	8.241
M165	1.6µm	1µm	1.6	1	8.241
M166	1.6µm	1µm	1.6	1	8.243
M170	4.94 µm	1 µm	4.94	1	8.243
M168	6.475 µm	180 nm	35.972	1	119.5
M164	3.3 µm	180nm	18.3	1	119.5
M171	6 µm	1 µm	6	1	10

Table 2 Transistor sizes and currents

The sum of currents across all branches is 161.145 µA which is smaller than the power consumption specification in Table 1. As the next step gain of the circuit when 5kΩ resistence connected to output is observed. The test circuit configuration is given in Figure 3.

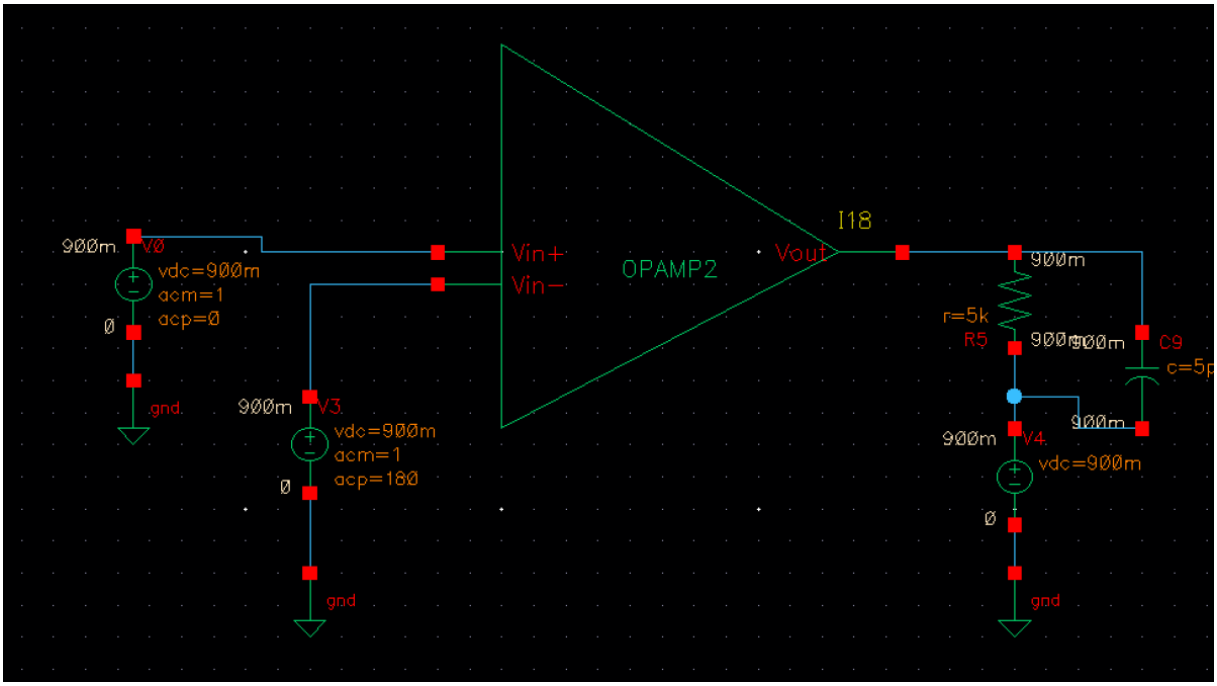

Figure 3 Test circuit for open loop DC gain

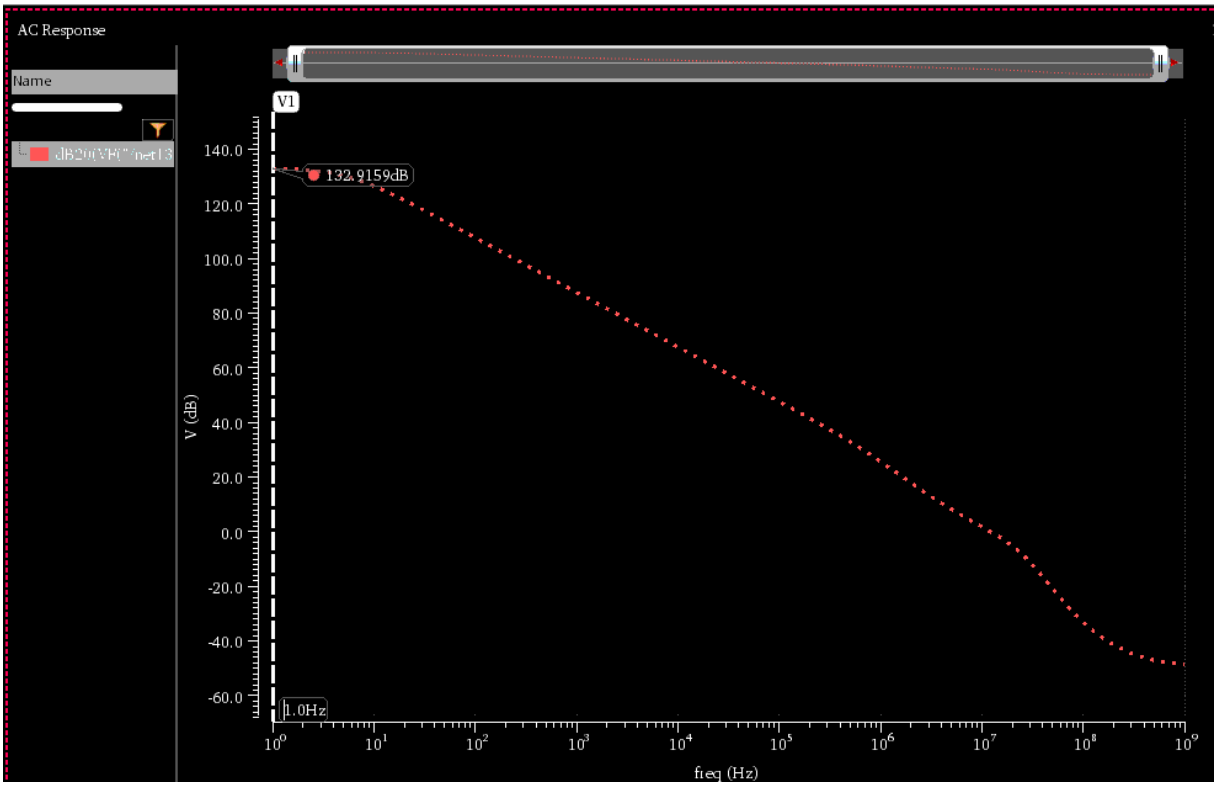

Figure 4 Open loop DC gain with load resistance

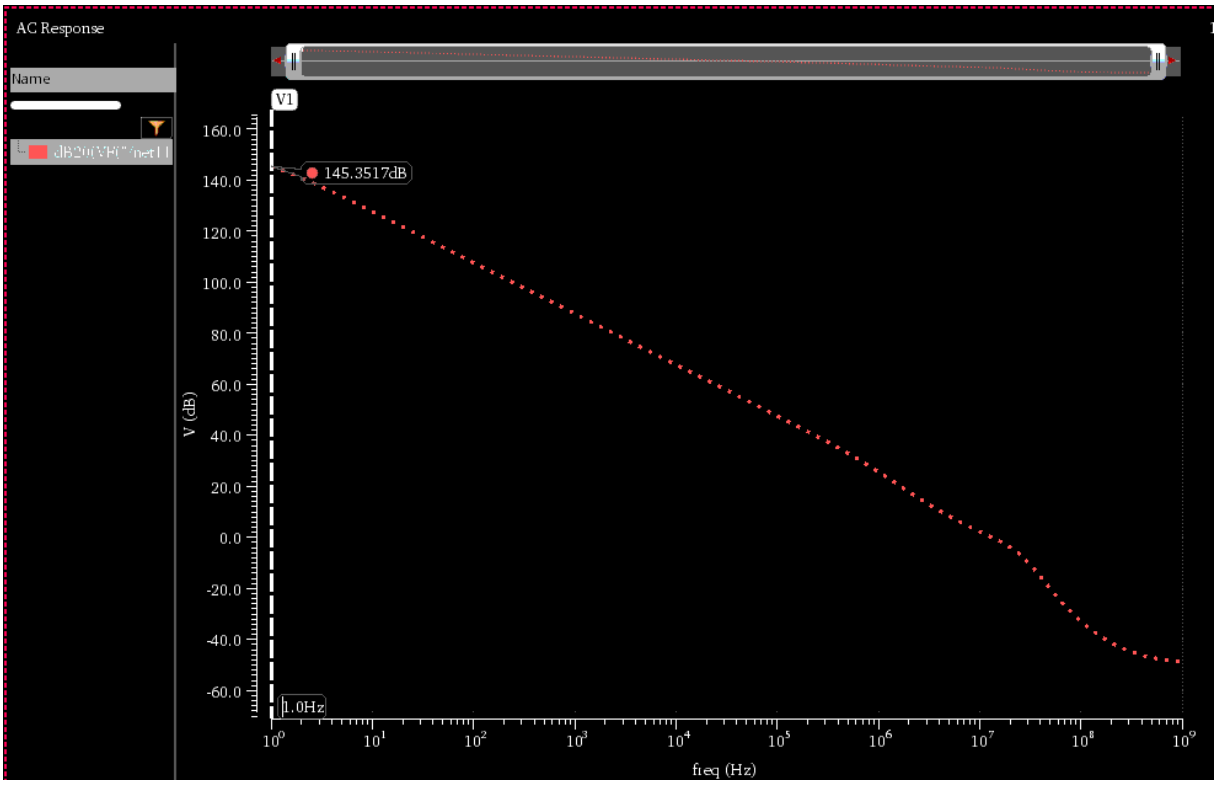

Figure 5 Open Loop DC gain without the load resistance

The open loop DC gain is above 100Db as it can be observed from Figure 4 and Figure 5. Also there is no drastic drop in gain when load resistance is connected. In the following section GBW product is observed. Figure 6 demonstrates the GBW with only driving capacitance connected to output. Figure 7 GBW is observed with load resistance besides the driving capacitor. As it can be observed the change

in output pole is minimal which indicates that RC value at the output does not differ significantly when load resistance is connected. As a result it can be concluded that output resistance is close to load resistance which is 5kΩ.

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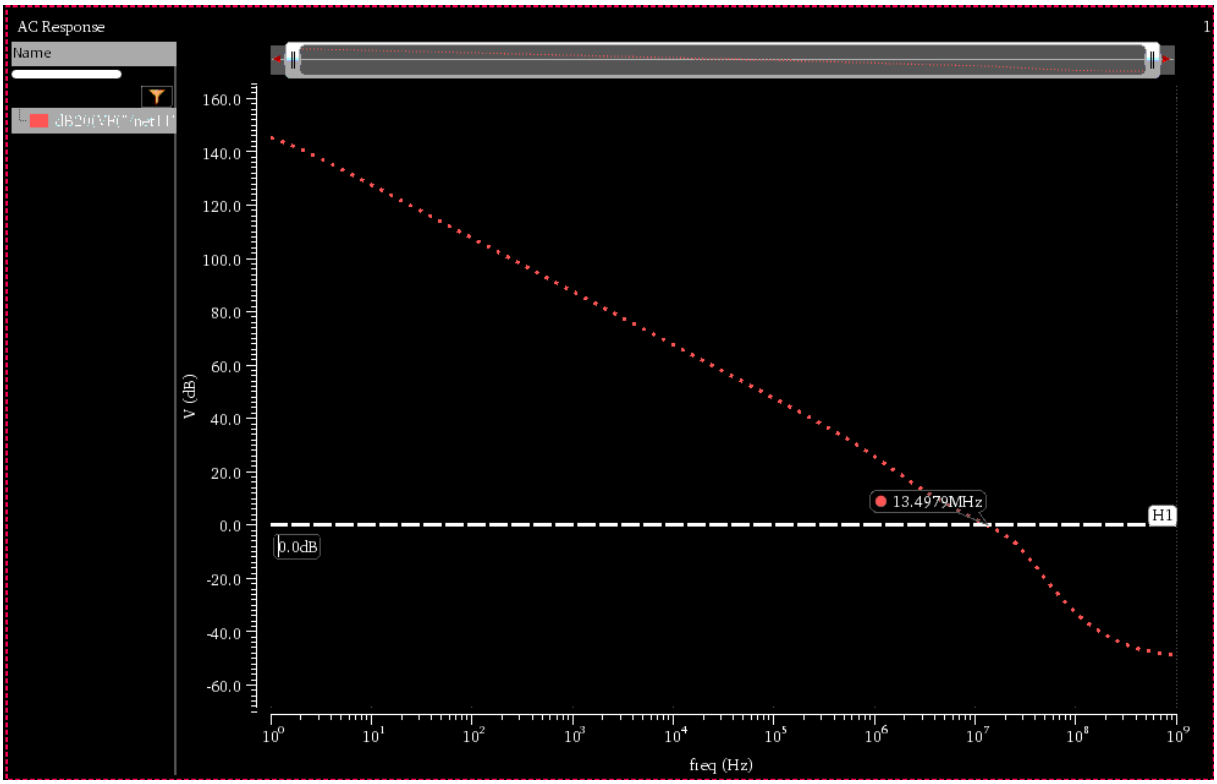

Figure 6 GBW product with only 5Pf

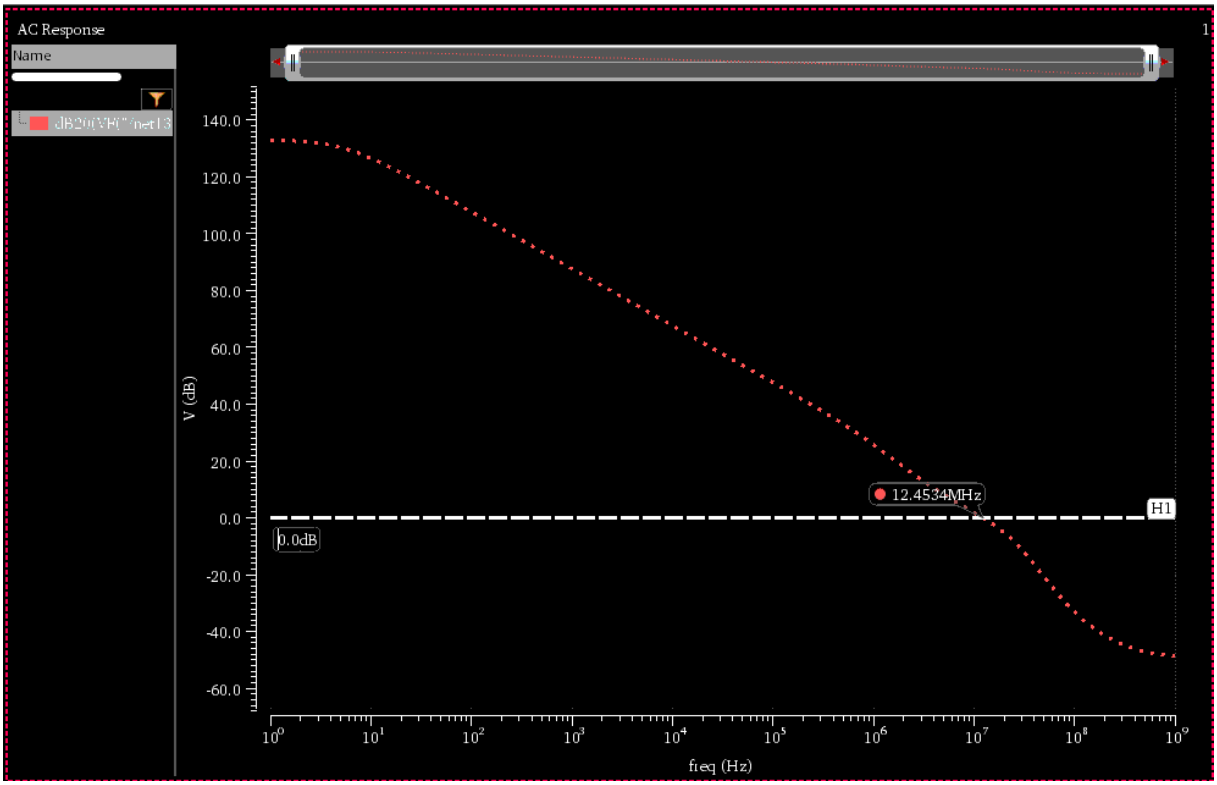

Figure 7 GBW product with load resistance and driving capacitor

As the frequency behavior is being investigated, for stability of the OPAMP Nested Miller Compensation is used as mentioned previously. In this project the necessary PM is above 45 degrees therefore values for C_1, C_2 and nulling resistor are experimentally found which satisfies minimum 45 degrees phase margin. The test configuration is the same with the test configuration of Figure 6 which is the circuit in Figure 3 with only 5Pf driving capacitor as the load. The results for PM and GM can be observed. The PM is given by the following expression. From the following Figures, $f_{gain\ crossover} = 13.4979MHz$ $f_{phase\ crossover} = 25.9785MHz$.

$$PM = -180 + \phi(f_{gain\ crossover})$$

$$GM = 0dB - 20log_{10}(|A(f_{phase\ crossover})|)$$

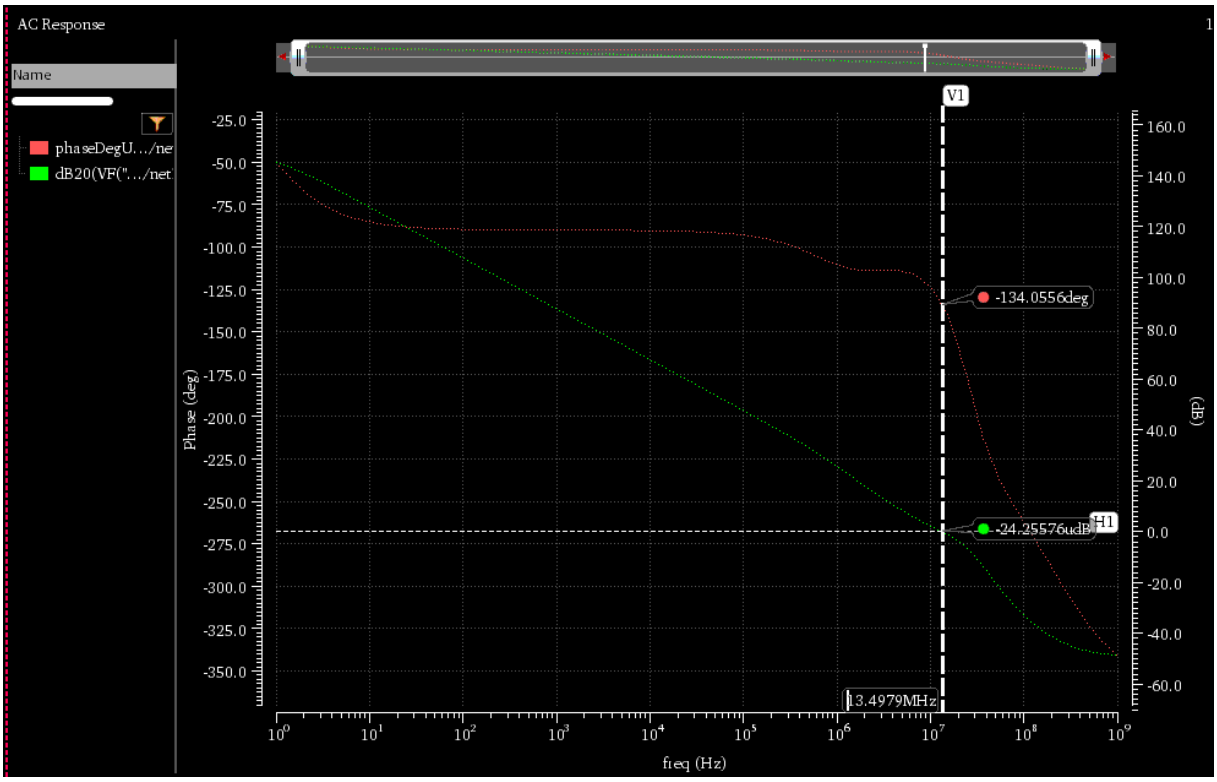

Figure 7 Phase at $f_{gain\ crossover}$

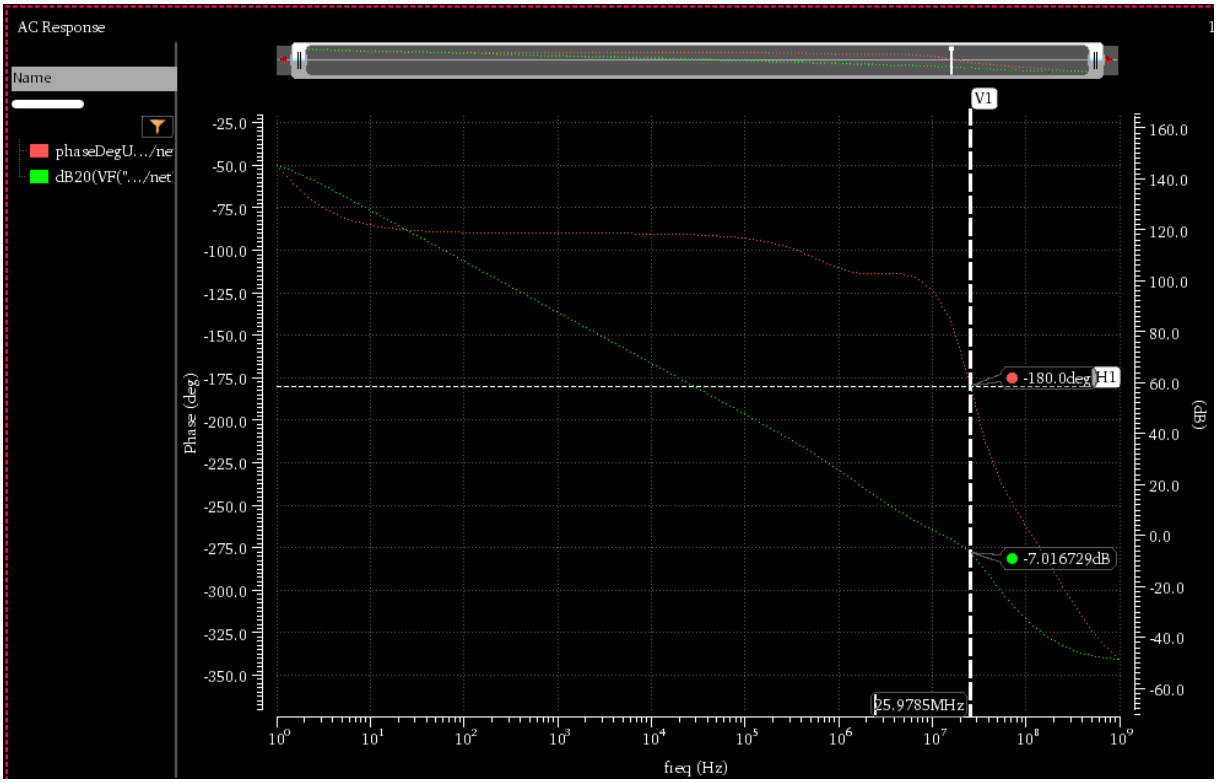

Figure 8 Gain at $f_{phase\ crossover}$

As it can be observed in Figure 7 and Figure 8 PM of the OPAMP is 45.945 degrees and a negative GM is obtained as -7.016729 which indicates OPAMP is stable.

For the voltage swing, unity gain buffer configuration is configured as the test circuit which can be observed in Figure 9. To Vin+ side, a sine wave with 900Mv DC level, 500Mv peak AC amplitude with 10kHz is applied. According to the operation logic of unity gain buffer circuit at the ouput 900Mv+500Mv, 900Mv-500Mv extremes is expected to be observed which can be verified from the 500µs transient analysis output provided in Figure 10.

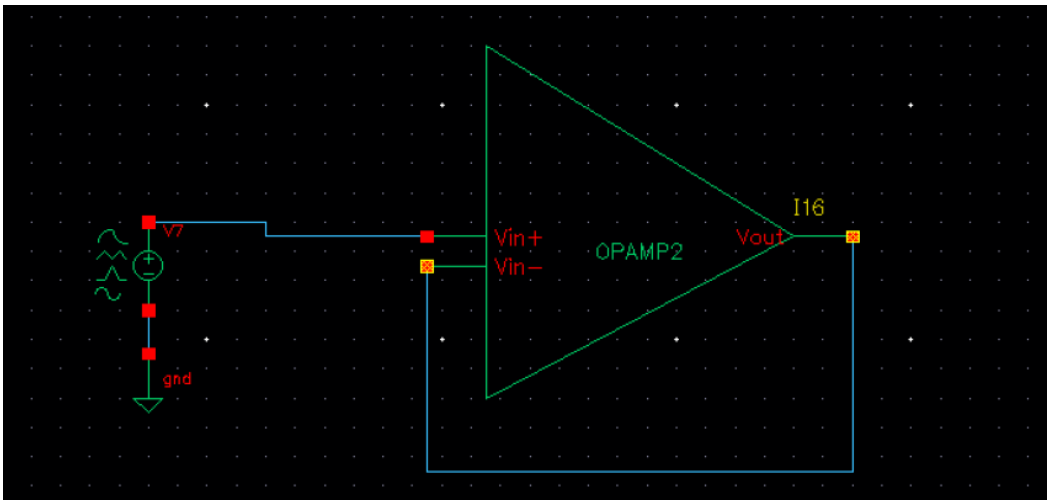

Figure 9 Unity gain buffer circuit configuration

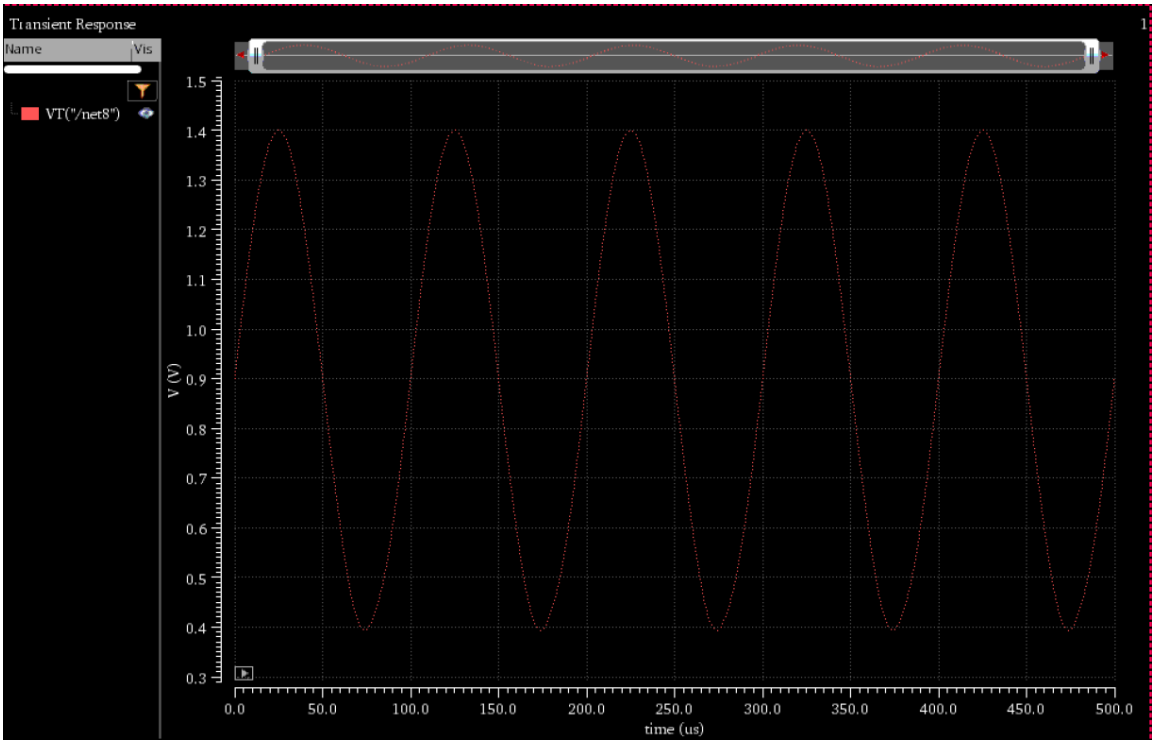

Figure 10 Transient response of unity gain buffer circuit

As it can be observed from Figure 10 the output is able to follow the voltage values from 0.4-1.4V which meets the output voltage swing specification. As the last section, noise analysis is performed with the following test circuit. The input output noise relation of this test circuit is as following.

$$v_{n,out}{}^2 = \left(\frac{5pF + C_{in}}{1pF}\right)^2 v_{n,in}{}^2$$

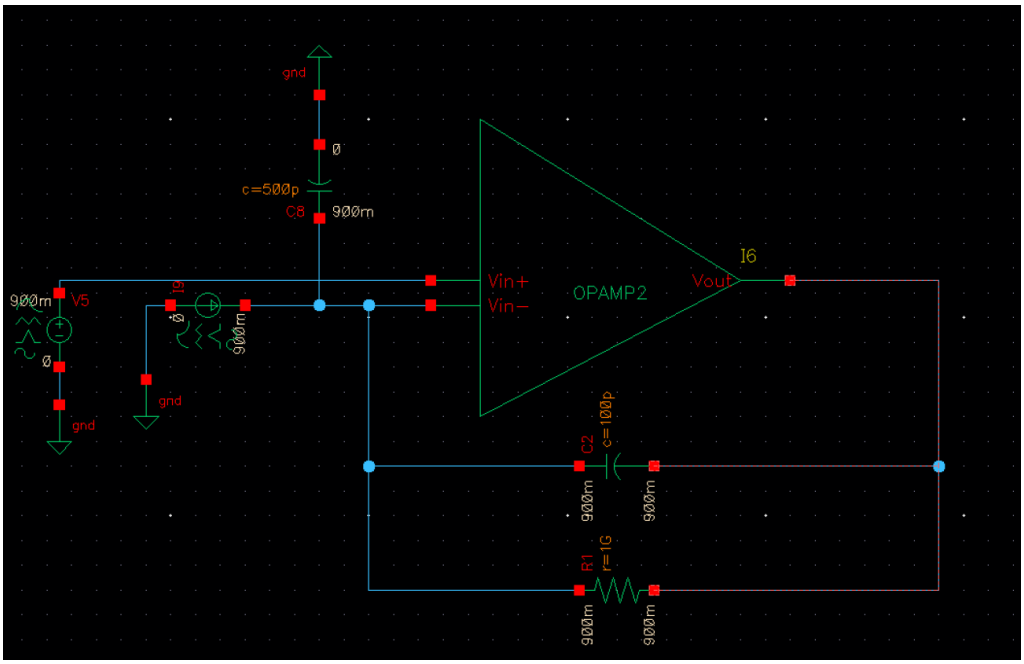

Figure 11 Noise Test Circuit

Initially investigate the transimpedance behavior of the amplifier. When 1Na 10kHz sine wave is applied 15.9Mv swing is obtained which can be observed from Figure 12. The saturation (distortion in the waveform/truncated sine wave) can be observed when 100Nv amplitude 10kHz sine wave is applied which can be observed from Figure 13.

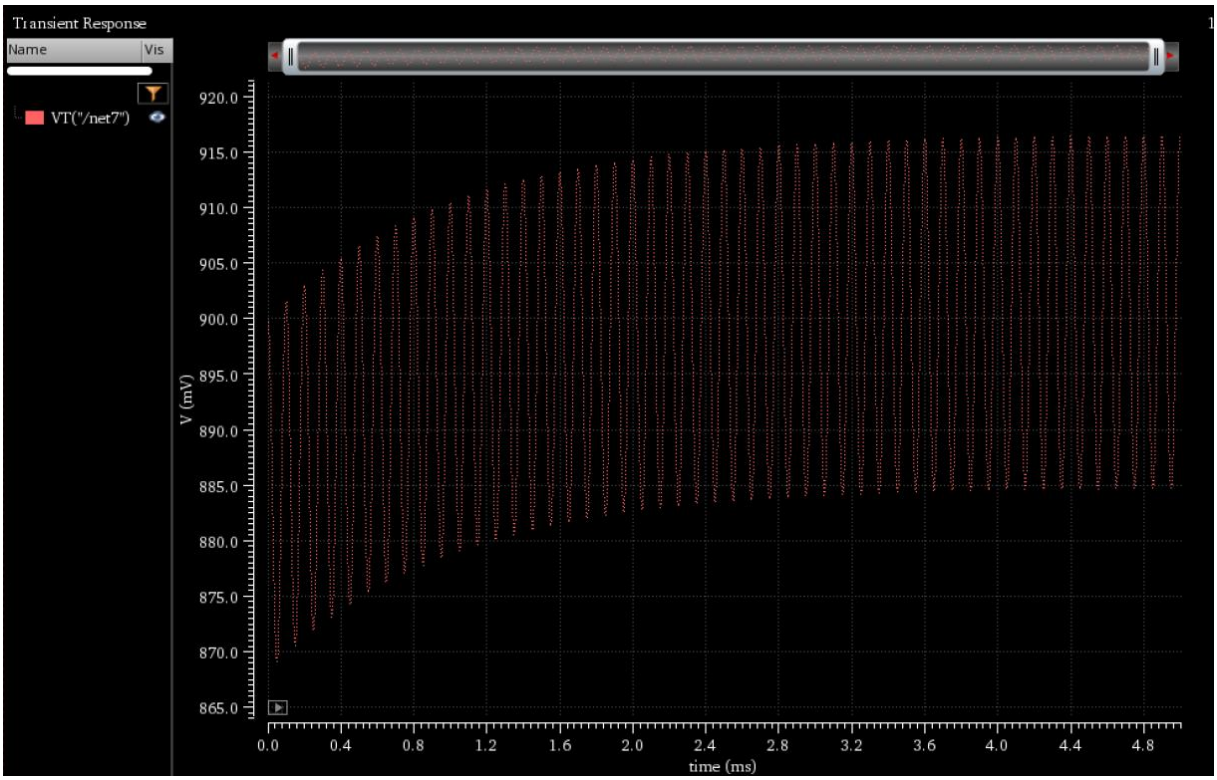

Figure 12 Transimpedance amplifier output with 1Na sine wave input

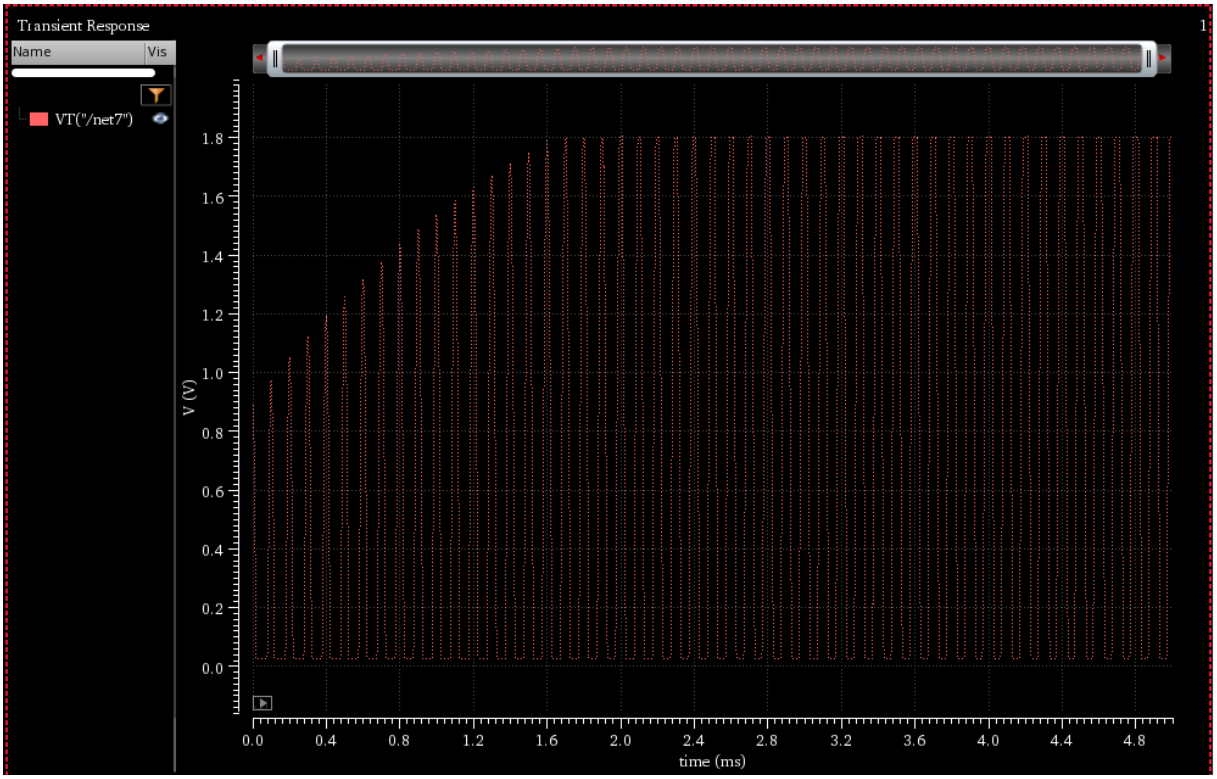

Figure 13 Transimpedance amplifier output with 1Na sine wave input

The output referred noise is dominated by the first stage of the amplifier which is the 5 transistor OTA. The input referred noise of 5 transistor OTA can be expressed as following.

$$v_{n,in,OTA}{}^2 = 8K\tau\gamma\left(\frac{1}{g_{m_{167}}} + \frac{g_{m_{172}}}{g_{m_{167}}{}^2}\right)$$

The input capacitance can be expressed as the following. Assume A is the gain of 5 transistor OTA.

$$C_{in} = C_{gs_{167}} + (1 - A)C_{gd_{167}}$$

As it can be observed from the expressions the noise is inversely proportional to the current flowing throught the 5 transistor OTA. However as current increases the gain decreases which can be inspected from the gain expression. Therefore there is a point for achieving the gain and a low noise operation.

When the current is increased (decreasing W/L of the bottom transistor of 5 transistor OTA) to satisfy the saturation transistor size of the input transistors should be increased which results in increase in input capacitance. Increasing the input transistor dimensions also reduce the input referred noise however the tradeoff is the capacitance size. Which can result in larger output referred noises even with smaller input reffered noise. Another situation is that the first stage is important for gain and high gain also results in larger input capacitance which also influences the noise gain tradeoff.

As a result, the most effective circuit is found to be the circuit in this report with $108.283\text{nV}/\sqrt{Hz}$ output reffered voltage noise.

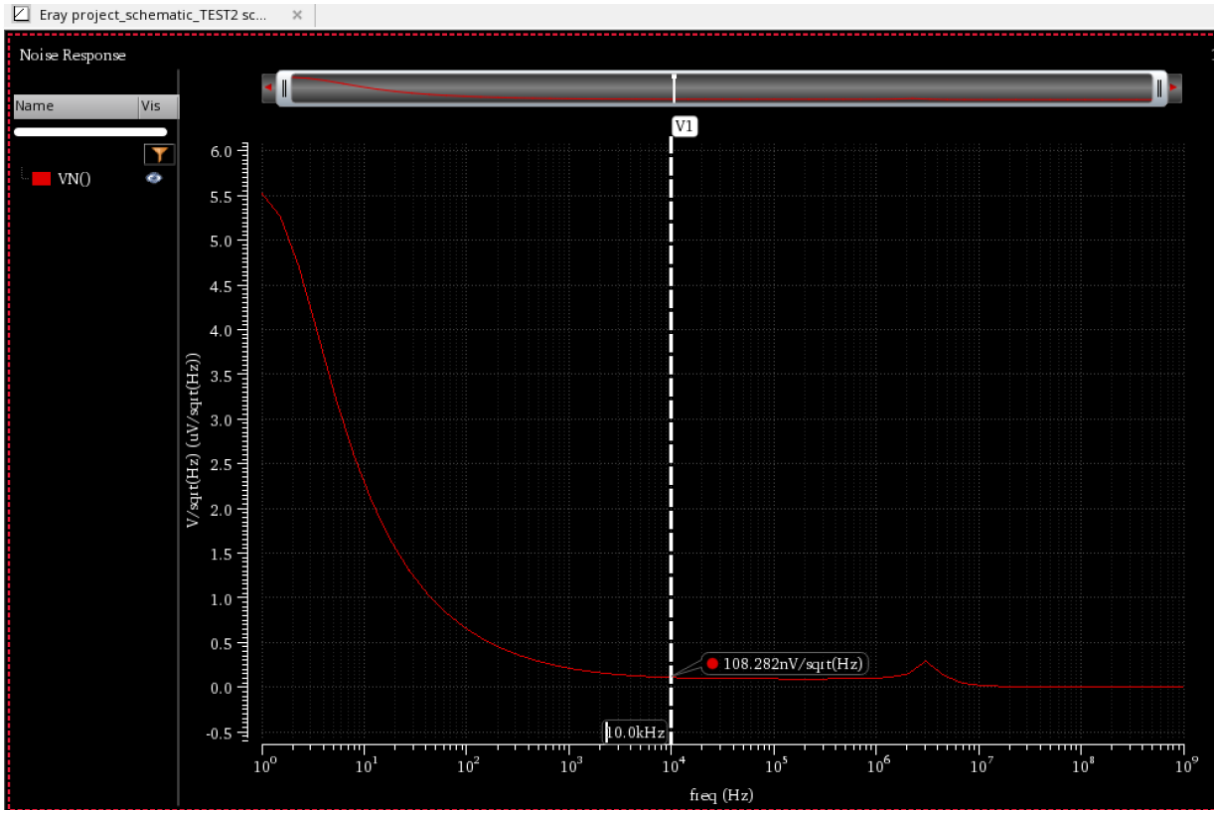

Figure 14 Output reffered voltage noise

Lastly an inverting amplifier with inverting amplification of 5 is configured with 5kΩ and 1kΩ resistances. Figure 15 is the inverting amplifier circuit. Figure 16 is the transient output when 100Mv sine wave with 10khz frequency is applied. The inverting amplifier operates as desired which is mostly as a result of output resistance being close to 5kΩ and lrge DC gain.

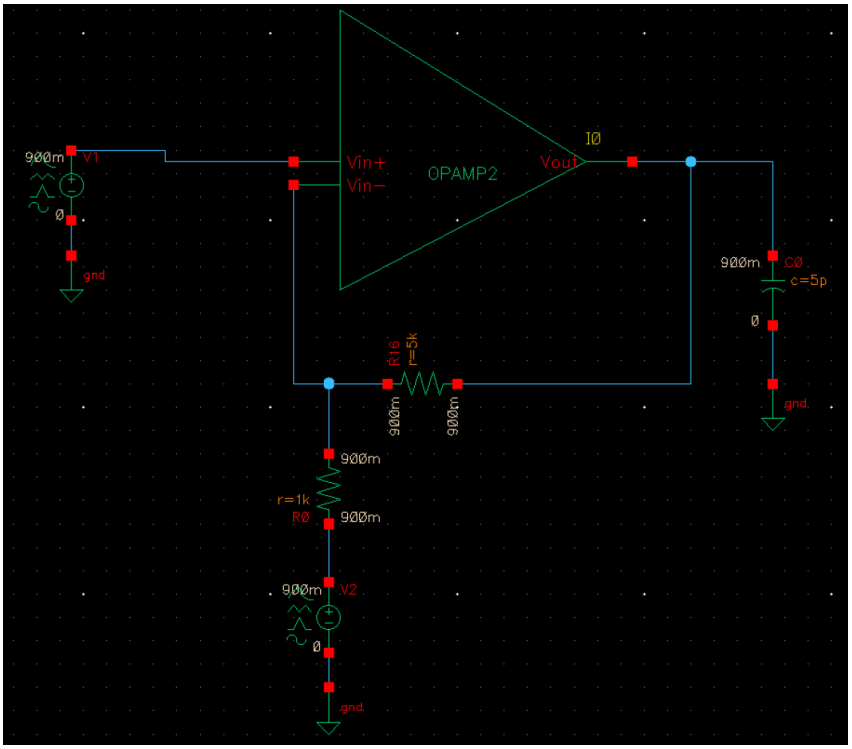

Figure 15 Inverting amplifier circuit

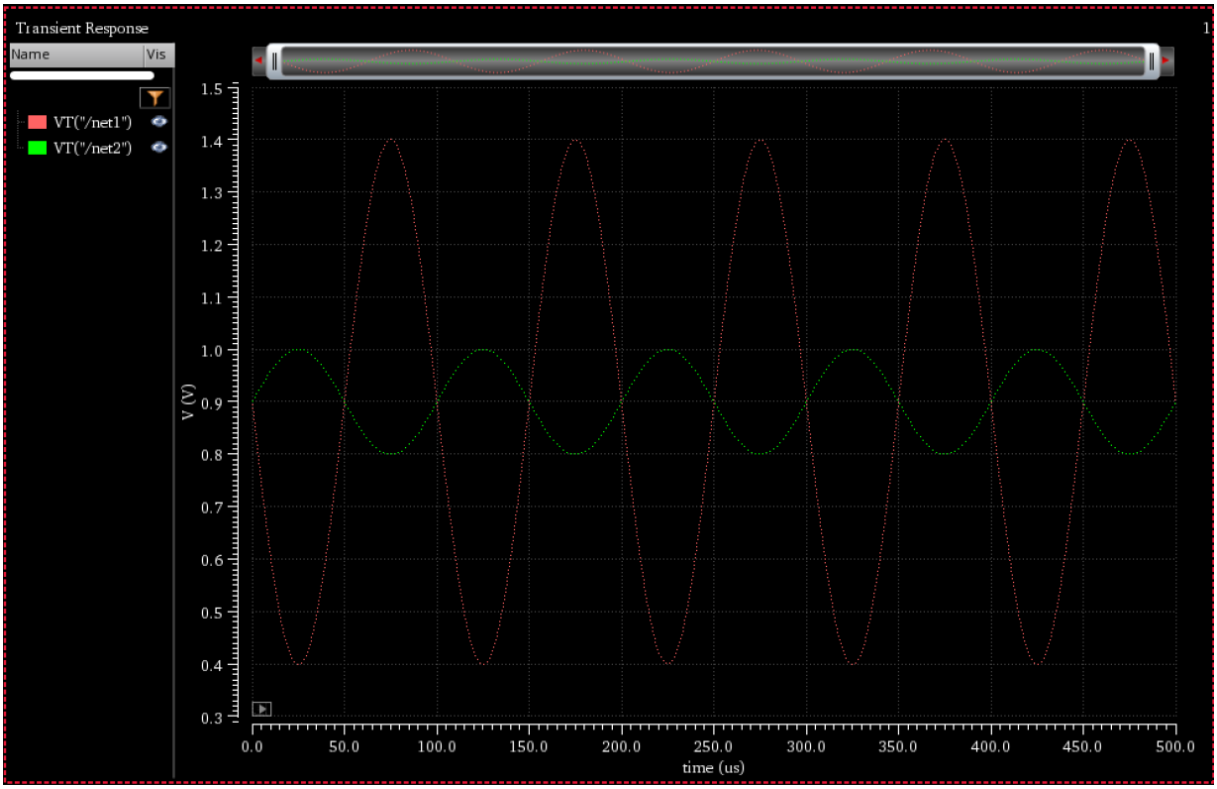

Figure 16 Output of transient analysis of the inverting amplifier

Layout

In order have schematic correspondance of the layout the schematic is alternated as provided in Figure 17. In total 6 pins are avaliable in which Vin- ,Vin+, gnd, vdd are as usual, additionally two pins in1 and in2 are defined to represent the reference current flowing through nmos and pmos current mirror branches respectively. As the layout correspondence of capacitors and resitor in frequency compensation configuration. As the capacitor cmm4 instance from PRIMLIB is used. As the resistor rnp instance from PRIMLIB is used since it has lower dimensions compared to other resistor alternatives. In a straightforward manner n-guard is applied to pmos devices and p-gueard is applied to nmos devices with 0.42 spacing. Also pmos devices are covered with n-well. As it can be observed from Figure 18 the layout is done such that devices are placed in a similar geometrical allignment when compared to schematic. Vdd and gnd pins are transformed into horizontal rails and the dimensions of the design clearly fits the restrictions. As the final results layout of the IC OPAMP design is DRC and LVS error free.

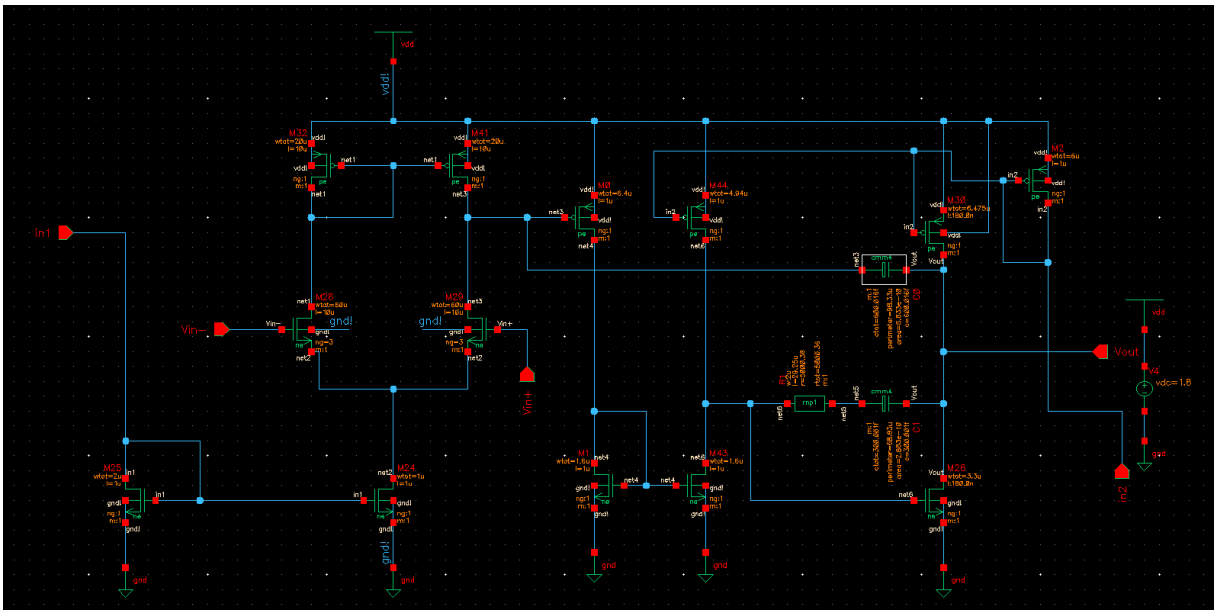

Figure 17 Schematic for the layout

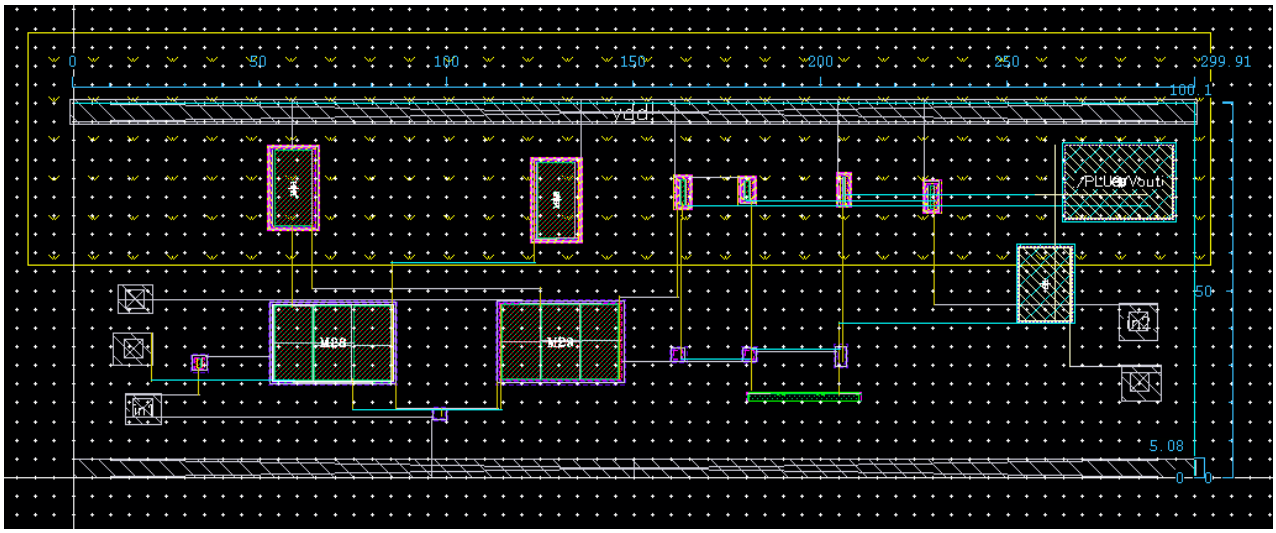

Figure 18 Overall layout and demonstration of dimensions

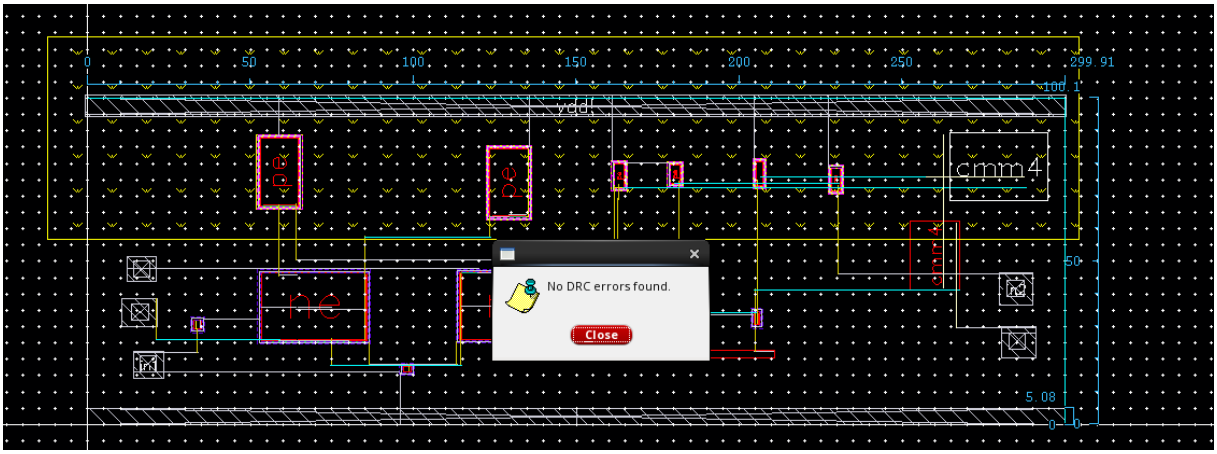

Figure 19 DRC simulation result

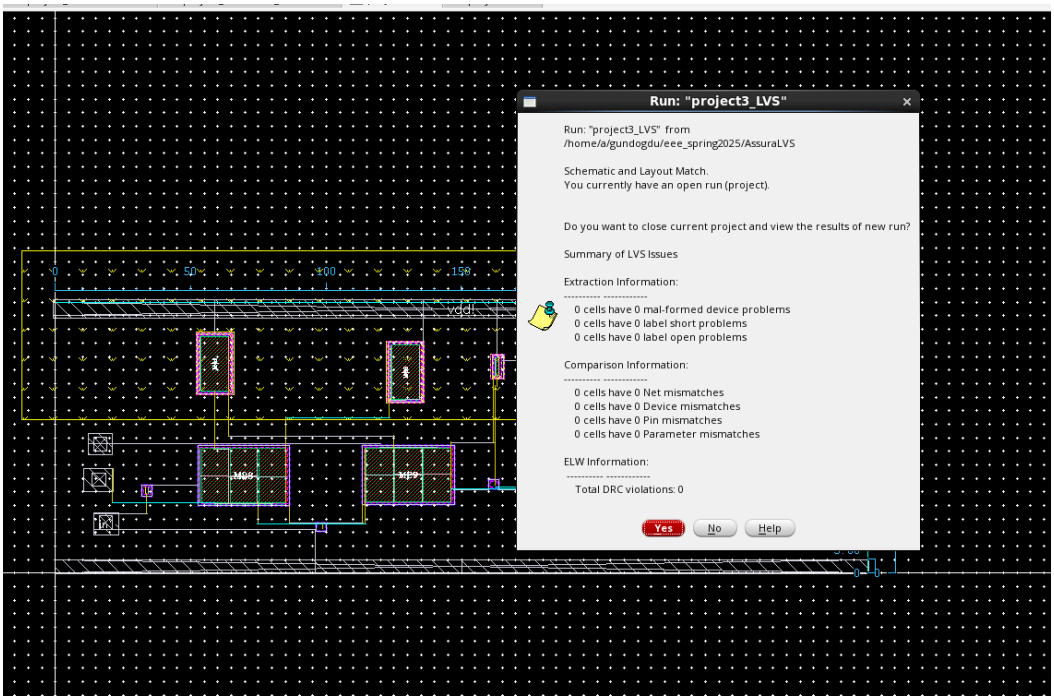

Figure 20 LVS simulation result