Eray Gündoğdu

Section-02

EEE202 CIRCUIT THEORY LAB4 REPORT

Purpose:

Aim of this labratory assignment is to generate a output signal that meets with the following requirements: .

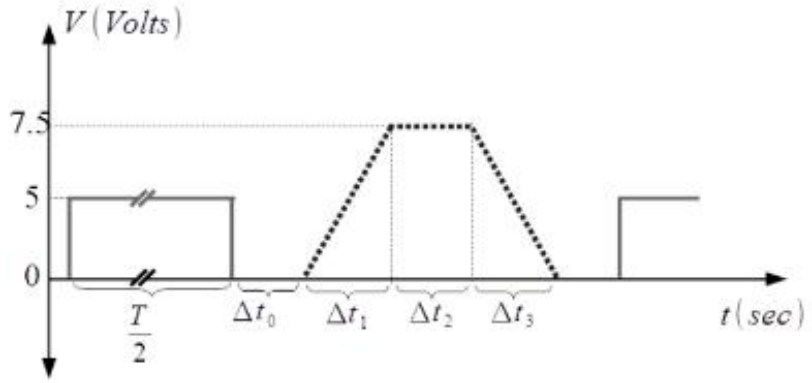

Fig1.1 Demonstration of output signal with input signal

$$\Delta t_0 = 3ms, \quad \Delta t_1 = 2ms, \quad \Delta t_2 = 3ms, \quad \Delta t_3 = 2ms$$

Input peak voltage: $5V$

Output peak voltage: $7.5V$

Input frequency: $f < 50Hz, \quad T = \frac{1}{f}$

Fig1.2 requirements for the output signal

Methadology:

In order to obtain the desired output signal, the input signal is shifted 3ms and 11ms, integrated for the skew-line shape and subtracted for the straight line. As it can be interpreted three processes are applied to the input signal. In addition, Vcc+=9.5V, Vcc-=0V, and Vcomp= 2.5V for the opamps.

First Process: Comparitor Opamp Circuit

In a comparitor opamp circuit, a reference voltage is connected to the V- termianl of opamp which is Vcomp= 2.5V in the designed circuit.By this way opamp will be negatively satured if Vcomp<V+ and positively saturated if Vcomp>V+.This property of comparitor circuit is suitable to

generate delays of 3ms and 10ms(3ms+2ms+3ms+2ms).Following calculations are necessary to find RC values and understand at what time opamp leaves the linear reigon:

$$\frac{dV_c}{dt} * C = \frac{V_{in} - V_c}{R}$$

$$\frac{dV_c}{dt} * C + \frac{V_c}{R} = \frac{V_{in}}{R}$$

Characteristic Equation of ODE:

$$\sigma * C + \frac{1}{R} = 0$$

$$\sigma = -\frac{1}{RC}$$

Natural Response:

$$V_{cnatural} = c_1 * e^{-\frac{t}{RC}}$$

Forced Response:

$$Let\ particular\ solution\ be\ K\ which\ is\ a\ constant$$

$$\frac{dK}{dt} * C + \frac{K}{R} = \frac{V_{in}}{R}$$

$$K = V_{in} = 5V$$

At t=0, $V_c = 0$:

$$V_c(0) = 5 + c_1 * e^{-\frac{0}{RC}}$$

$$c_1 = -5$$

Function for V_c is:

$$V_c = 5 - 5 * e^{-\frac{t}{RC}}$$

Moving to finding RC values, when t=3ms V_c= Vcomp=2.5V for a 3ms delay and when t=10ms V_c= Vcomp=2.5V for a 10ms delay.The RC values are selected according to values that are present in hardware lab.

Substituting t for 3ms delay:

$$2.5 = 5 - 5 * e^{-\frac{3}{RC}}$$

$$e^{-\frac{3}{RC}} = \frac{1}{2}$$

$$R_1 * C_1 = 0.043$$

$$R_1 = 8k\Omega\,, C = 430nF$$

Substituting t for 10ms delay:

$$2.5 = 5 - 5 * e^{-\frac{10}{RC}}$$

$$e^{-\frac{10}{RC}} = \frac{1}{2}$$

$$R_1 * C_1 = 0.0144$$

$$R_1 = 4.3k\Omega\,, C = 3.3\mu F$$

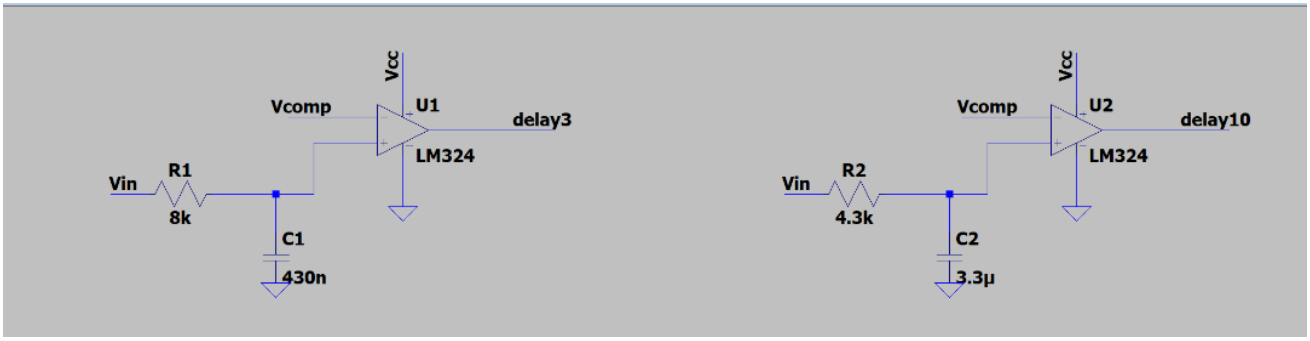

Fig2.1 designed comparitor circuits for 3ms delay and 10ms delay

Now 3ms and 10ms delayed waveforms with a peak voltage of saturation voltage are obtained and can be observed in the following figures:

Second Process: Integrating Opamp Circuit

After shifting input signals 3ms and 10ms in order to obtain a skew-line shape integrator opamp circuit is used because a constants integral equals to a linear function.RC values of integrator circuits can be found with following calculations:

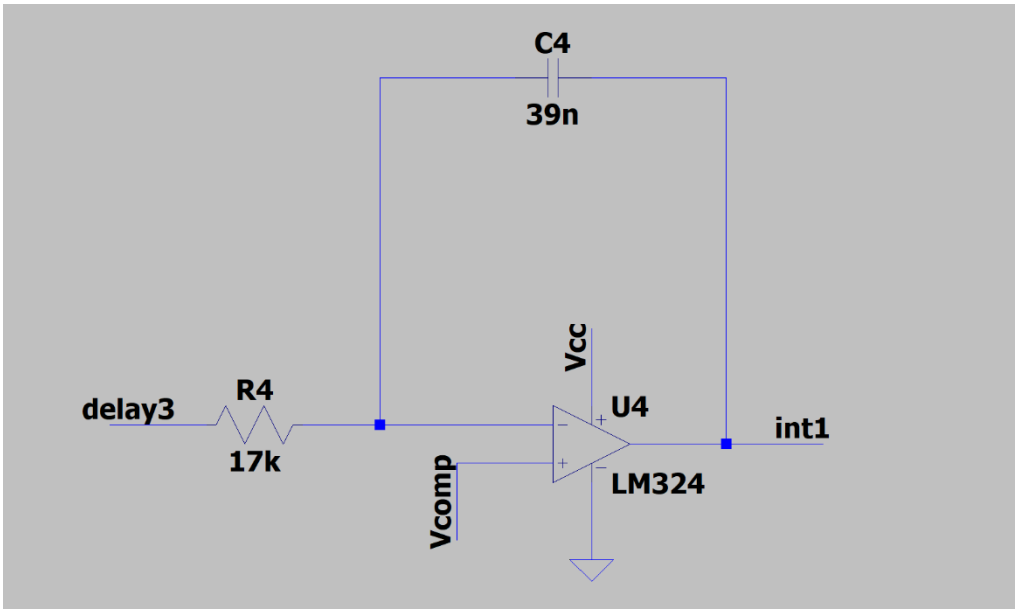

Fig3.1 integrator circuit

KCL at V^-:

$$\frac{dV_c}{dt} * C = \frac{V_{in} - V^-}{R}$$

$$dV_c = \frac{V_{in} - V^-}{RC} dt$$

$$\int \frac{V_{in} - V^-}{RC} dt = V_c$$

$$\frac{V_{in} - V^-}{RC} * t + c_2 = V_c$$

$$t = 0, V_c = 0 \; so \; c_2 = 0$$

$$\frac{2.5}{RC} * t = V_c$$

At t=3ms V_c should be 7.5V:

$$\frac{2.5}{RC} * 3ms = 7.5V$$

$$R_1 * C_1 = 1ms$$

$$R_1 = 17k\Omega\,, C = 39nF$$

A duplicate of the integrator circuit in fig3.1 is established for the 10ms delayed signal. The values of RC is selected appropriate for hardware lab and in the purpose of minimizing error in the final output.

Third Process: Subtractor Opamp Circuit

The current integrated and delayed waveforms should be substracted to obtain the final desired output signal.This is done by the subtractor circuit.

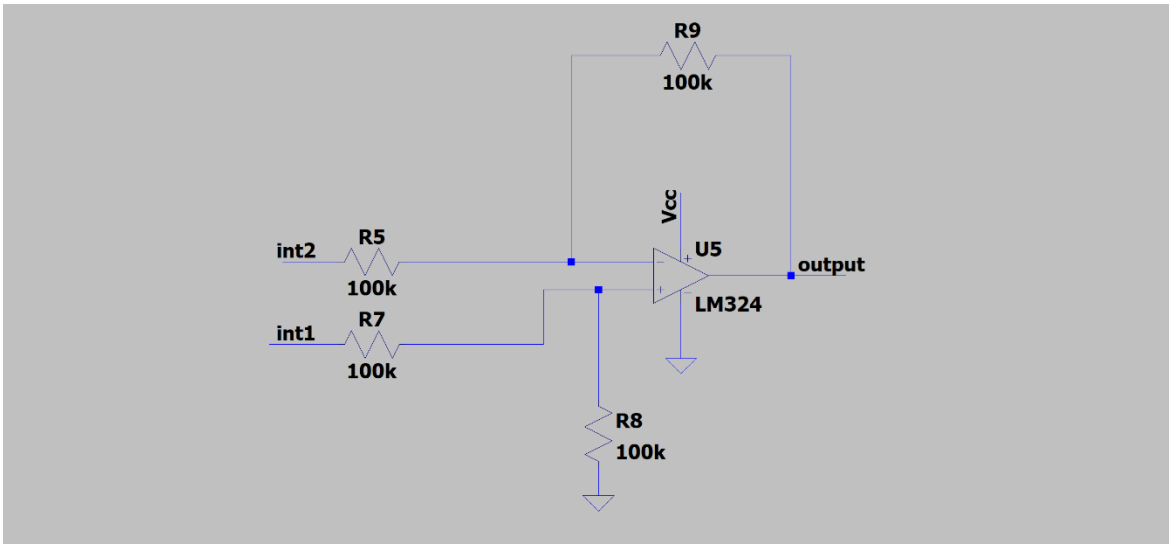

Fig4.1 subtractor circuit

Calculation for the resistance values are as following:

$$\frac{V_{int2} - V^-}{R5} = \frac{-V_{out} + V^-}{R9}$$

$$V^- = \left(\frac{V_{int2}}{R5} + \frac{V_{out}}{R9}\right) * \frac{1}{(\frac{1}{R5} + \frac{1}{R9})}$$

For V^+:

$$\frac{V_{int1} - V^+}{R7} = \frac{V^+}{R8}$$

$$V^+ = \frac{V_{int1}}{R7(\frac{1}{R7} + \frac{1}{R8})}$$

Since $V^+ = V^-$:

$$\frac{V_{int1}}{R7(\frac{1}{R7}+\frac{1}{R8})} = \left(\frac{V_{int2}}{R5}+\frac{V_{out}}{R9}\right) * \frac{1}{(\frac{1}{R5}+\frac{1}{R9})}$$

If all resistor values are equal the equation is satisfied as following:

$$R7 = R5 = R9 = R8 = 100k\Omega$$

$$V_{int1} - V_{int2} = V_{out}$$

Last equation is valid for all ideal opamps so when all resistors are equal the equation is satisified.

Software Results:

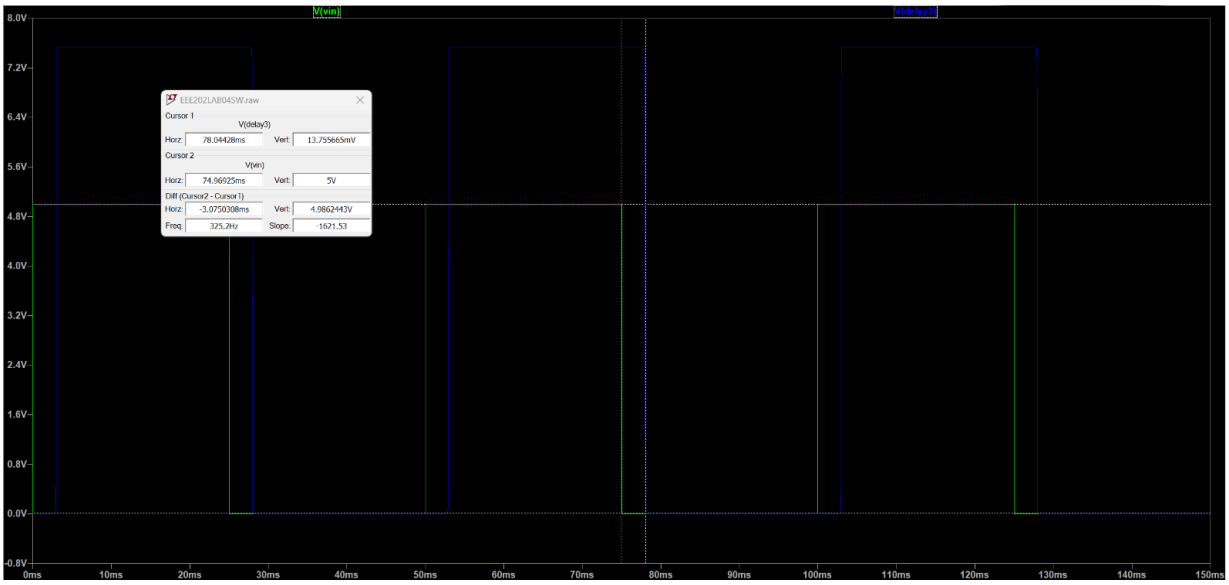

Fig5.1 demonstration of 3ms delay as 3.07ms comparitor circuit

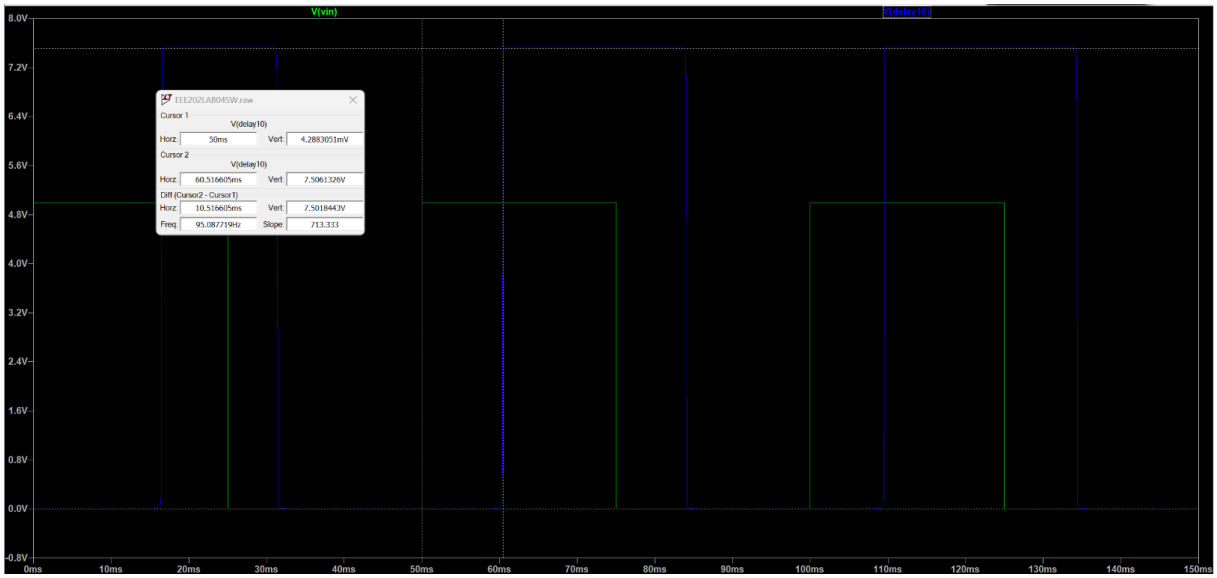

Fig5.2 demonstration of 10ms delay as 10.51ms comparitor circuit

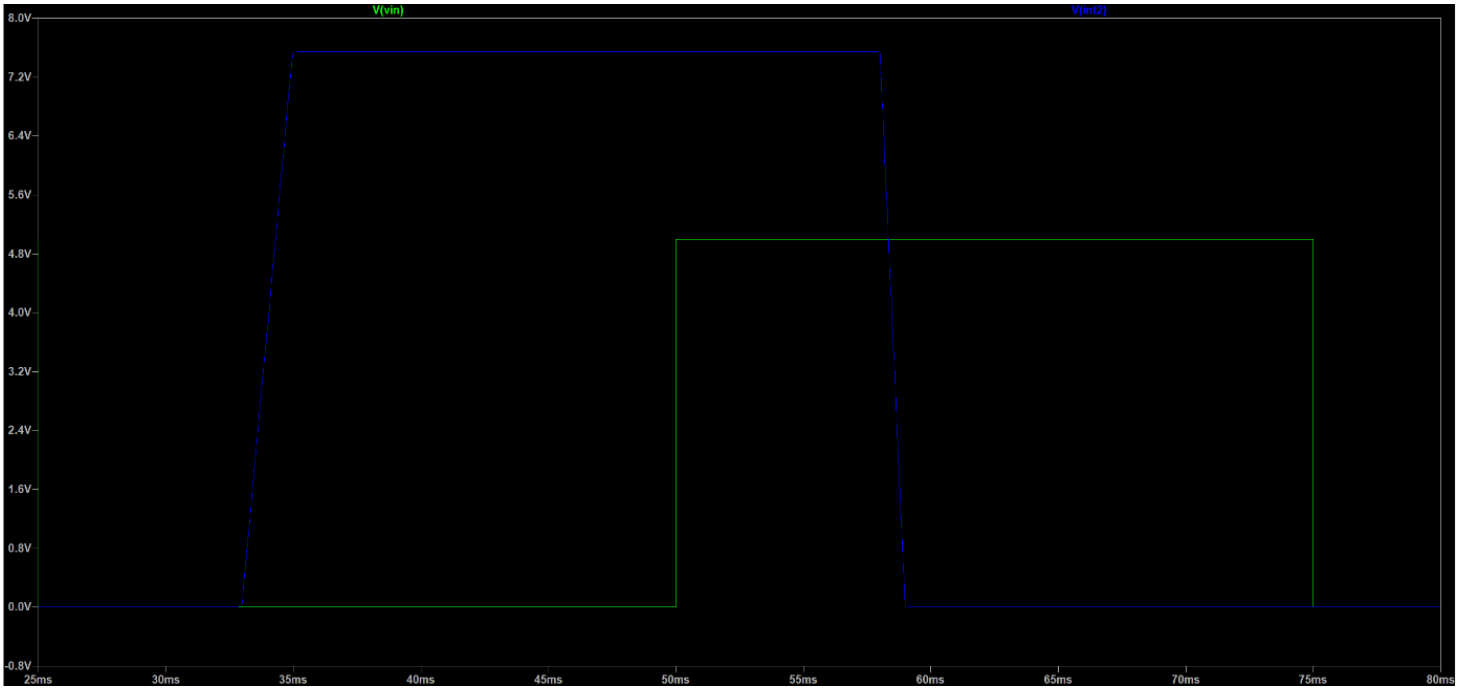

Fig5.3 output waveform after the shifted input signal is gone trough integrator circuit

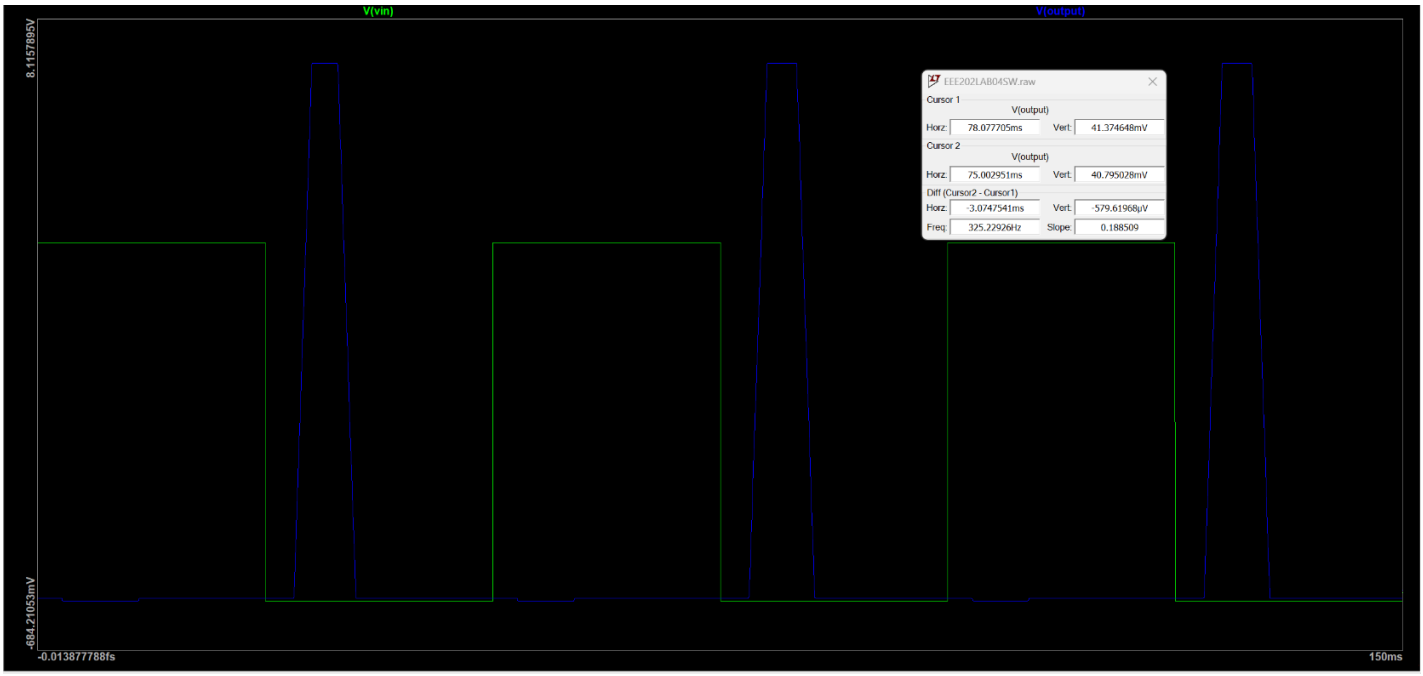

Fig5.4 Δt_1 =2.12ms final output signal

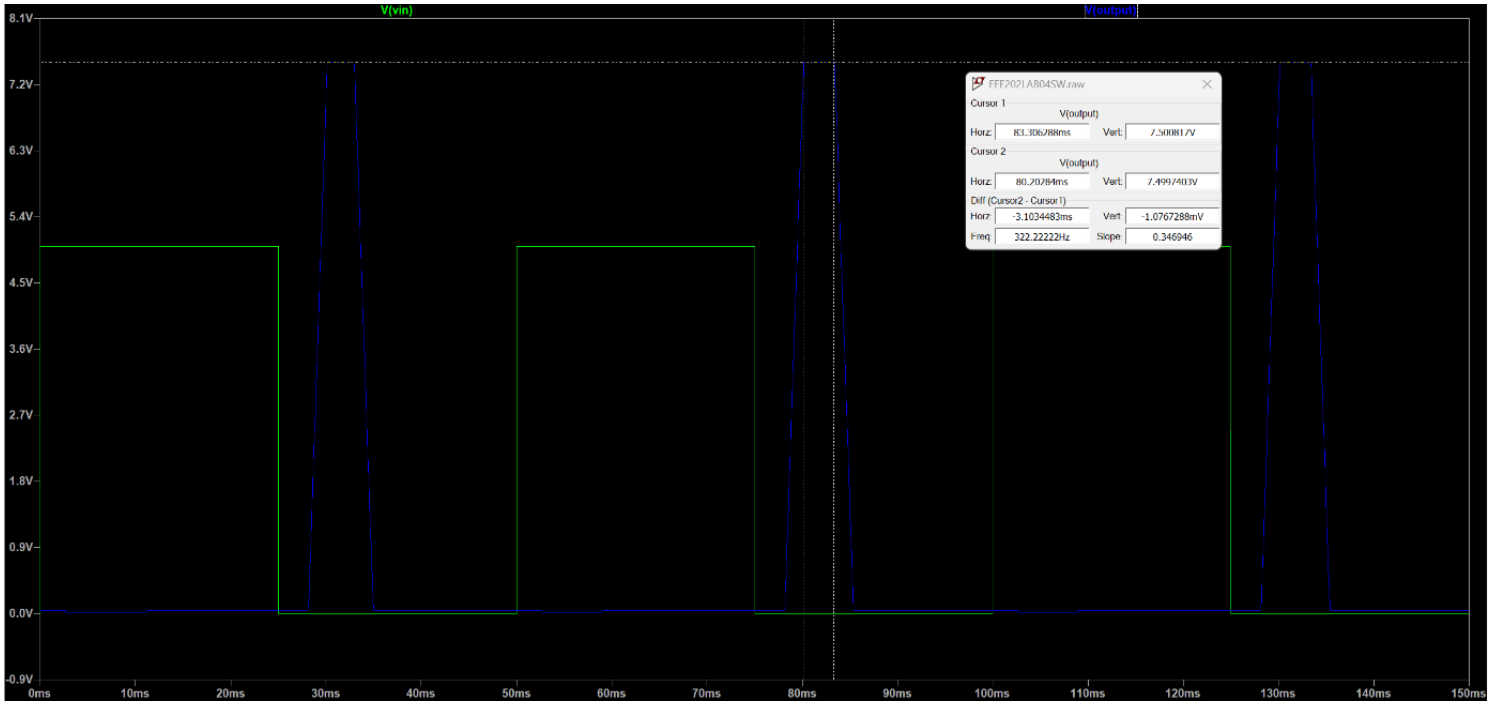

Fig5.5 Δt_2 =3.10ms final output signal

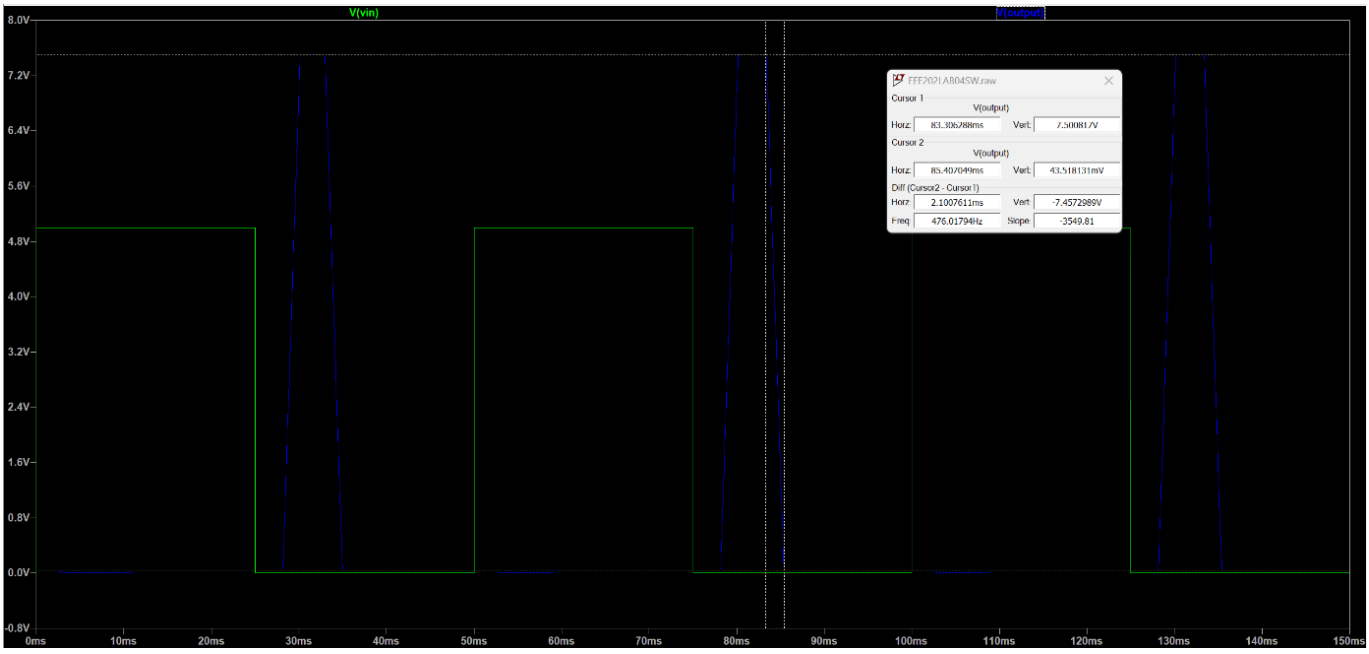

Fig5.6 Δt_3 =2.10ms final output signal

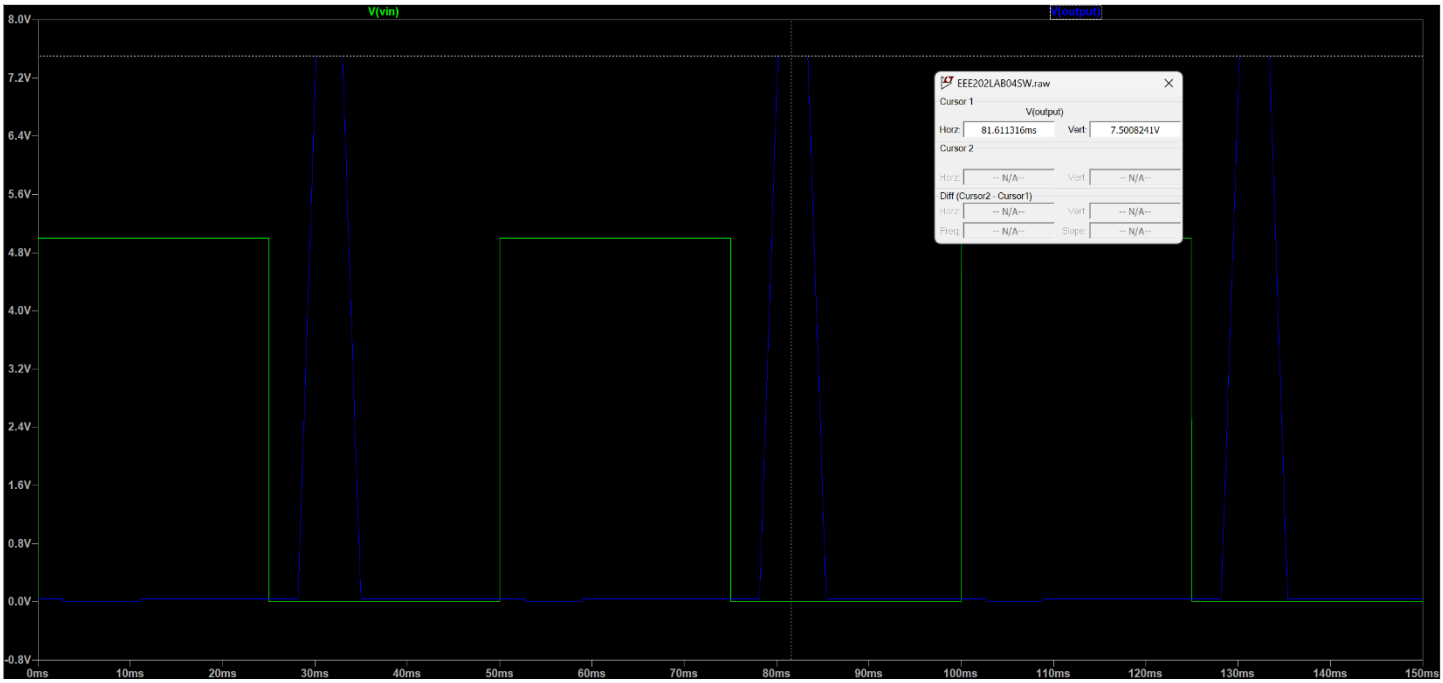

Fig5.3 final output signal(blue trace) with input signal and a peak voltage of 7.5V

	Δt_0	Δt_1	Δt_2	Δt_3
Expected Value	3ms	2ms	3ms	2ms
Software Result	3.07ms	2.12ms	3.10ms	2.10ms

Table 1 comparison of desired values and software results

	Peak Voltage
Expected Value	7.5V
Software Result	7.5V

Table 2 comparison of peak voltage values

The values are within %10 percent error band therefore the circuit works properly(%2.3,%6,%3.3 and %5 respectively for delays).The circuit will be implemented in the hardware part of the lab.

Hardware Part:

The designed circuit is implemented on breadboard by using LM324 with calculated RC values.

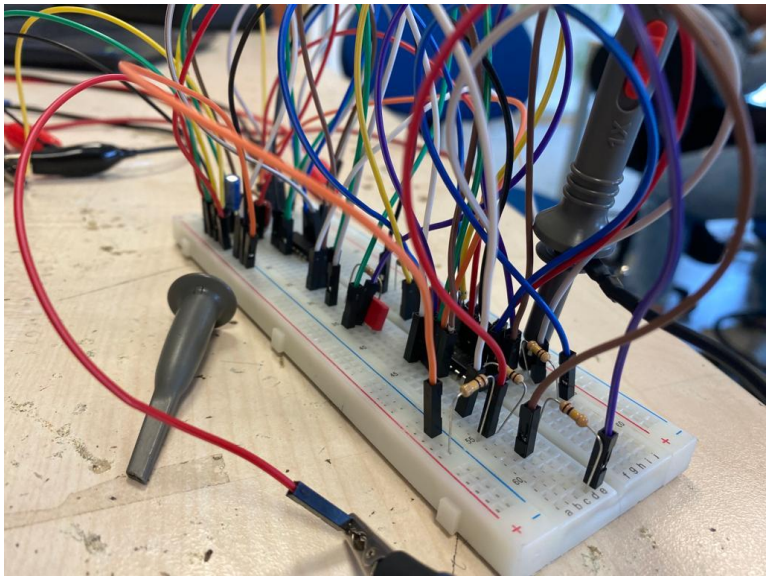

Fig6.1 hardware circuit

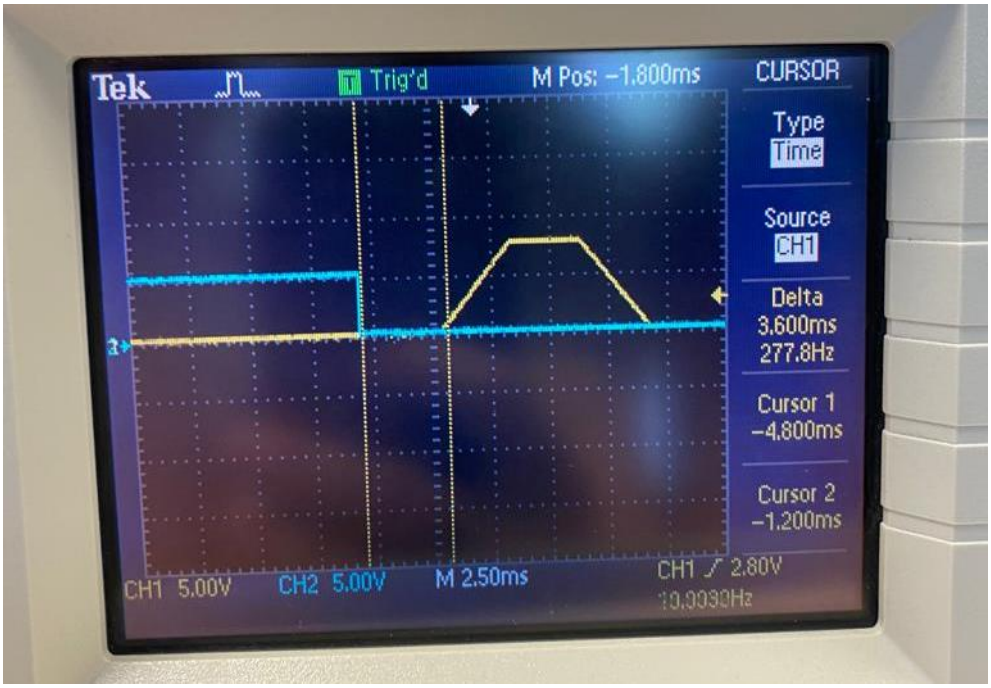

Fig6.2 hardware result of Δt_0

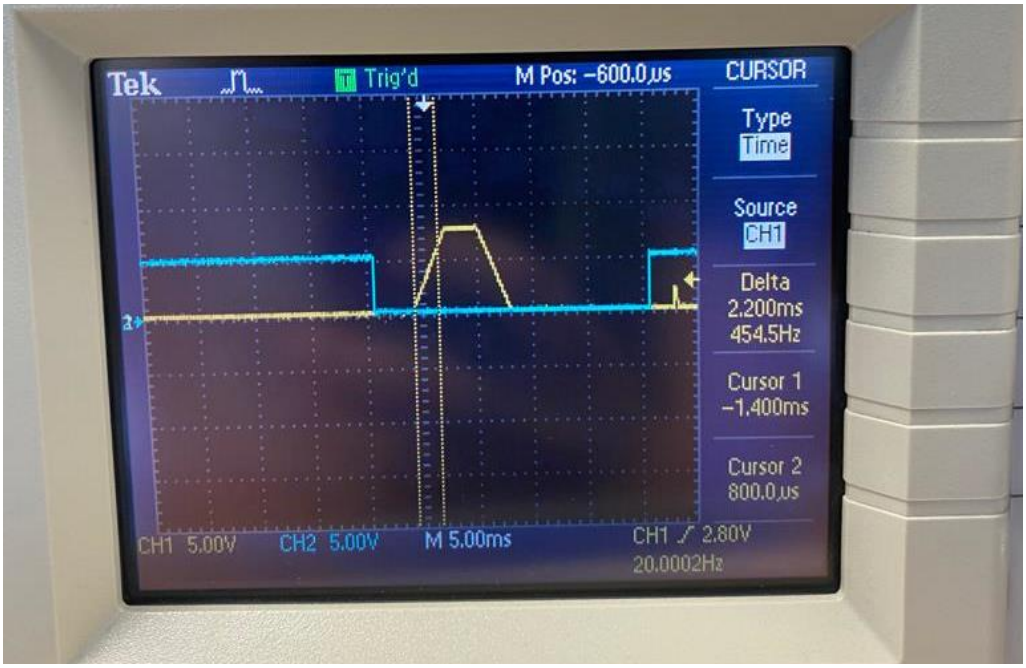

Fig6.3 hardware result of Δt_1

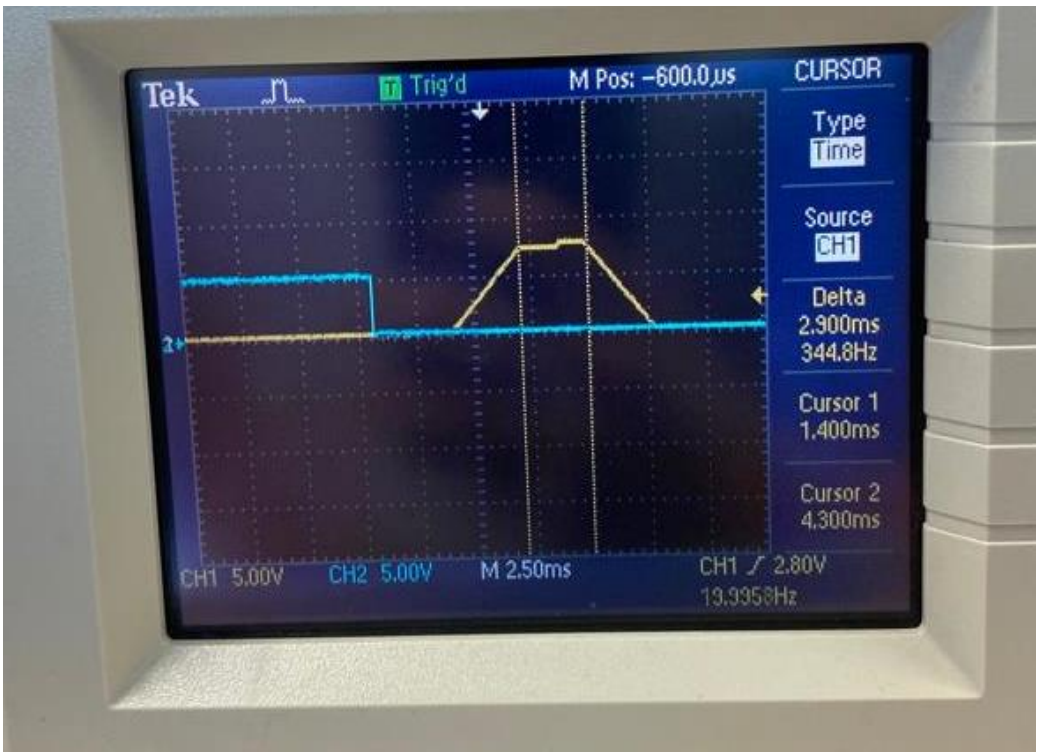

Fig6.4 hardware result of Δt_2

Fig6.5 hardware result of Δt_3

	Δt_0	Δt_1	Δt_2	Δt_3
Expected Value	3ms	2ms	3ms	2ms
Software Result	3.07ms	2.12ms	3.10ms	2.10ms
Hardware Result	3.60ms	2.20ms	2.90ms	2.20ms

Table1.3 comparison of delays

The tolarated error in hardware lab is %20 and all of the hardware delay results are within the error range(%20,%10,%3.3 and %10 respectively).So, hardware results are valid.

Fig6.6 demonstration of peak voltage of hardware output signal

	Peak Voltage
Expected Value	7.50V
Software Result	7.50V
Hardware Result	7.68V

Table 4 comparison of peak voltage values

Peak voltage result of hardware circuit is also within the %20 error range with an error percentage of %2.4 therefore result is valid.

Conclusion:

In this lab assignment desired waveform is obtained by using comparitor, integrator, and subtractor opmap circuits respecitvely. Comparitor is used for the delay, integrator is used for skew-line shape and finally subtractor is used to obtain the final waveform.The delay results and peak voltage results are precise since they are within the error band however they are slightly different from the expected values due to uncertainity of oscilloscope and signal generator, small resistance occured from jumper cables, LM324 not being an ideal opamp and human errors.