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EEE 415 Spring 2024/25 Homework 2

Question 1)

In the transistor test circuits it is desired to keep overdrive voltage around 100mV hence for the nmos transistor to observe DC operating points 745.1mV gate voltage is applied. In Figure 1 and Figure 2 the nmos test circuit schematic and its DC operating points can be observed respectively.

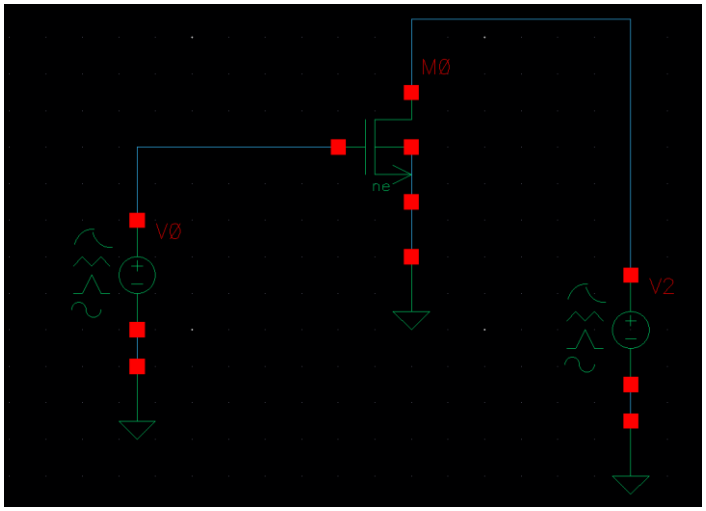

Figure 1 nmos test circuit schematic

string	OP("/M0" "??")
gds	8.263u
gm	362.2u
id	34.2u
ids	34.16u
isub	39.61n
ron	52.7K
vbs	0
vds	1.8
vdsat	115.8m
vgs	745.1m
vth	628.4m
signal	OP("M0.m1" "??")
beff	5.021m
betaeff	3.812m
cbb	5.775f

Figure 2 nmos test circuit DC operating points

Vth = 628.4mV and current passes among the transistor can be directly observed from Figure 2. To derive r_0 the following expression is used.

$$r_0 = \frac{1}{g_{ds}}$$

$$r_0 = 121.021k\Omega$$

Now the aim is to find $\mu_n C_{ox}$. The transistor operates in SAT mode (reigon 2 is observed from DC operating points). The current passes through the transistor can be expressed as following.

$$betaeff = \mu_n C_{ox}\left(\frac{W}{L}\right)$$

$$\mu_n C_{ox} = \frac{3.812m}{11.11} = 343.9\frac{\mu A}{V}$$

To comment on whether the analysis fit to the equations in class, it is determined to calculate the current and compare it with the simulation result.

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{th})^2 = 25.95\mu A$$

As it can be seen there is around 0.01mA deviation from the Cadence simulation which can be the result of influence of channel length modulation in Cadence and internal transistor characterisitcs. Also the I-D characteristics of the Nmos test circuit can be observed in the following figures.

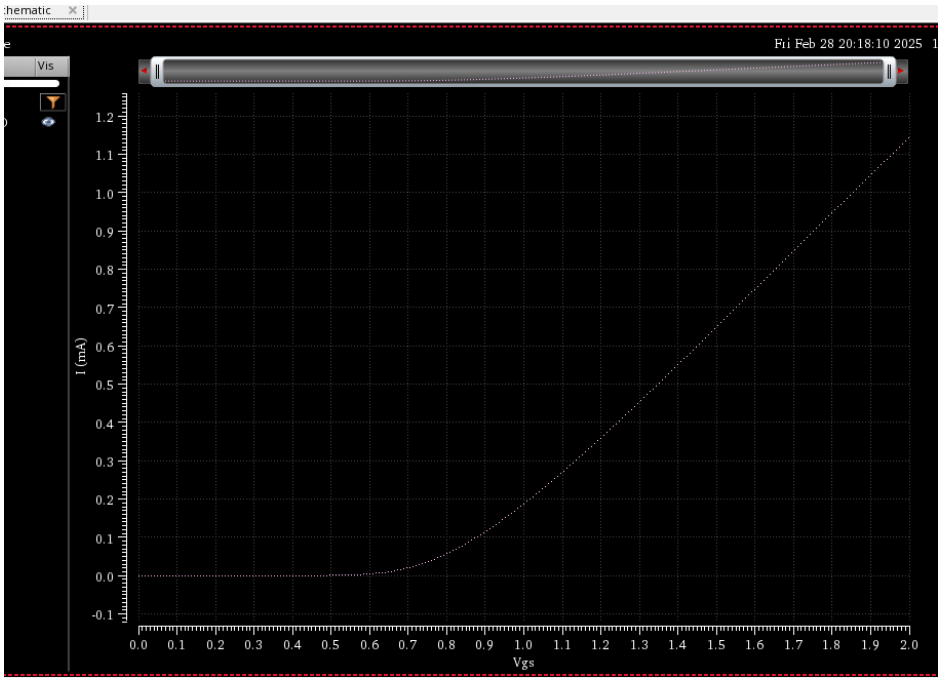

Figure 3 I_{DS} vs V_{GS} plot of nmos test circuit

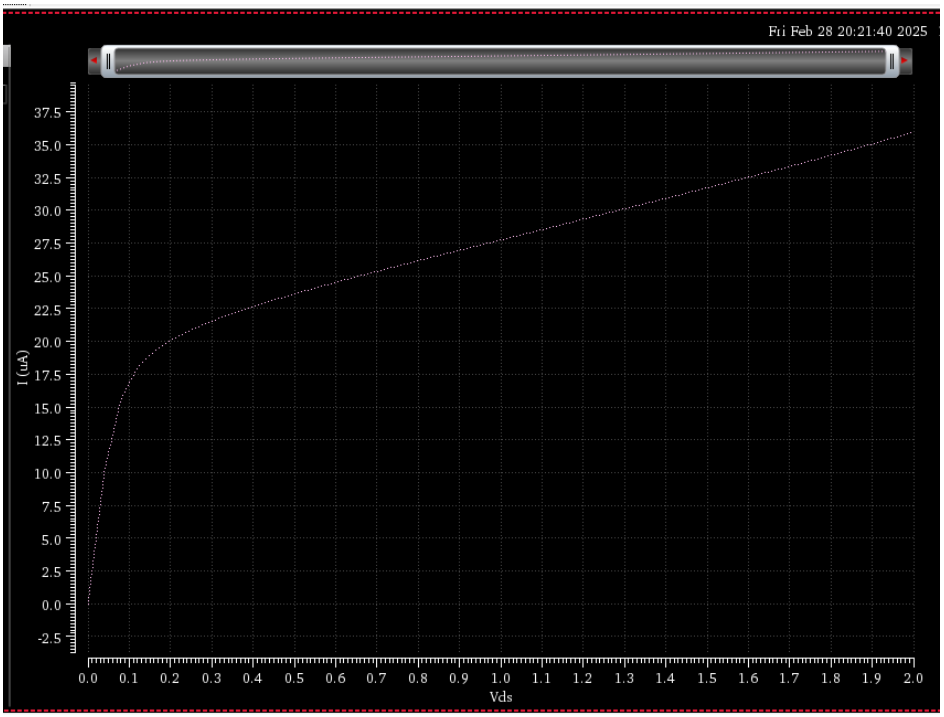

Figure 4 I_{DS} vs V_{DS} plot of nmos test circuit

In Figure 3 it can be observed that nmos is off until gate voltage is equal to the threshold which is 628.4mV. Moreover, in Figure 5 the nmos goes from TRIODE to SAT when V_{DS} = vdsat which is 115.8mV from Figure 2 and continues to increase with a slope which indicates channel length modulation is considered in the simulation. It can be concluded that the simulations are consistent with the logic of a nmos transistor.

Question 2)

In this question it is desired to perform the analysis again for a pmos transistor and comment on the currents of nmos and pmos transistors. Test circuit and DC operating points can be observed in the following figures respectively. Also it is benefitial to mention that $|V_{DS}|$ and $|V_{GS}|$ are kept approximately same with the nmos test circuit which can be observed by comparing Figure 2 and Figure 5.

string	OP("/M1" "??")
gds	754n
gm	86.46u
id	-7.177u
ids	-7.177u
isub	-104.2p
ron	250.8K
vbs	0
vds	-1.8
vdsat	-137.7m
vgs	-755m
vth	-633.9m
signal	OP("M1.m1" "??")
beff	979.2u
betaeff	724.3u
cbb	5.512f

Figure 5 pmos test circuit DC operating points

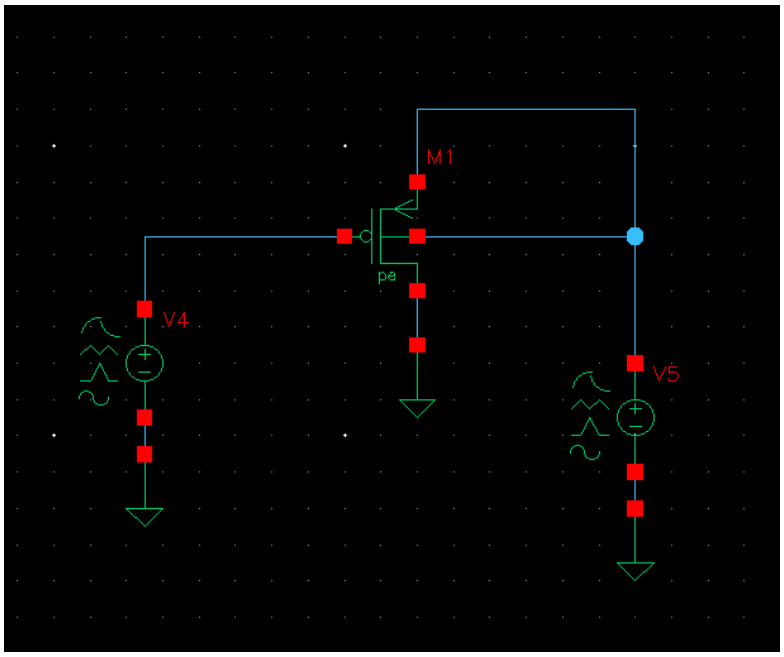

Figure 6 pmos test circuit schematic

The desired paramters for pmos are obtained by following the same methadolgy which is used to obtain parameters of nmos. From Figure 5 $|V_{tp}| = 633.9mV$.

$$r_0 = \frac{1}{g_{ds}}$$

$$r_0 = 1.326M\Omega$$

$$betaeff = \mu_p C_{ox}\left(\frac{W}{L}\right)$$

$$\mu_p C_{ox} = \frac{0.724m}{11.11} = 65.1\frac{\mu A}{V}$$

In the following figures I-V characteristics of the pmos test circuit can be observed. It is important to mention that in Figure 7 gate voltage is considered and in both plots the source node is selected as the y-axis which makes the current variable I_{SD}, current passes from source to drain. After observing the figures when gate voltage is less than Vdd - $|V_{tp}|$ the pmos is in SAT and turns off at Vdd - $|V_{tp}|$ which suits to the operating logic of pmos test circuit.

Moreover, the current flowing through nmos is larger than the current flowing through of pmos. If the calculated μC_{ox} values are compared $\mu_n C_{ox} > \mu_p C_{ox}$ which explains the current of pmos is larger than current of nmos under the same $|V_{DS}|$, $|V_{GS}|$ and $\left(\frac{W}{L}\right)$ ratios.

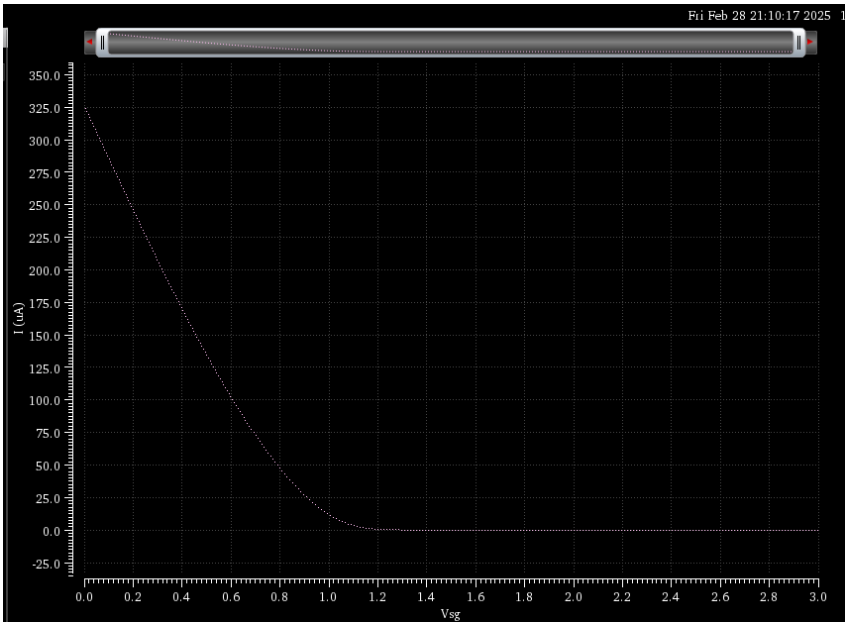

Figure 7 I_{SD} vs V_G plot of pmos test circuit

Question 3)

In this question the common source amplifier topology is selected to achieve the requirements by mimicing the intrinsic gain circuit of a common source amplifier to achieve largest gain possible. In the amplifier schematic the ideal current source is replaced with biased pmos load which is the best possible real design approach. As the very initial steps the transistors must be biased such that both of them operate in reigon 2 which can be observed in the following DC operating point figures.

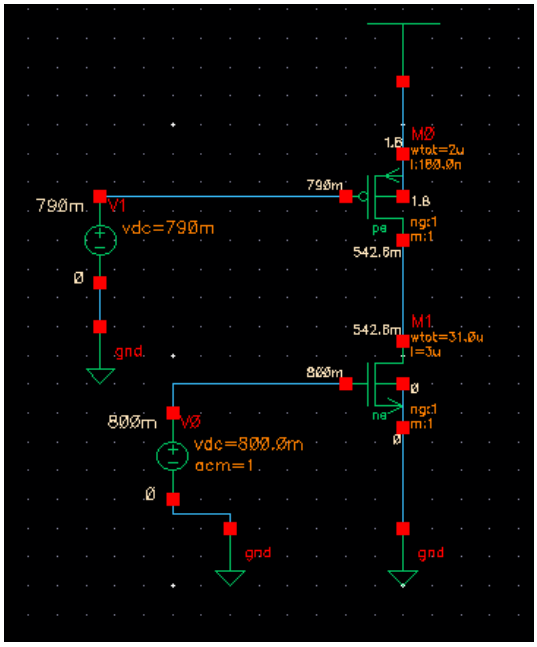

Figure 8 Amplifier Schematic

string	OP("/M1" "??")
gds	517.5n
gm	419.6u
id	47.93u
ids	47.93u
isub	377.3a
ron	11.32K
vbs	0
vds	542.6m
vdsat	175m
vgs	800m
vth	601.8m
ige	0
igidl	0
igisl	0
igs	0
is	-47.93u
isb	2.66a
ise	47.93u
isub	377.3a
pwr	26.01u
qb	-482.3f
qbd	-20.95f
qbi	-482.3f
qbs	-103z
qd	-2.873f
qdi	-239.5a
qg	581.8f
qgi	571f
qinv	457.4u
qsi	-88.49f
qsrco	-96.68f
region	2
reversed	0
ron	11.32K
rout	1.932M

string	OP("/M0" "??")
gds	3.59u
gm	229.2u
id	-47.93u
ids	-47.93u
isub	-122.3f
ron	26.24K
vbs	0
vds	-1.257
vdsat	-327.7m
vgs	-1.01
vth	-635.5m
is	47.93u
isb	42.35a
ise	-47.93u
isub	-122.3f
pwr	60.27u
qb	-2.917f
qbd	2.715f
qbi	2.917f
qbs	110.6z
qd	158a
qdi	340z
qg	4.125f
qgi	3.637f
qinv	271.6u
qsi	719.8a
qsrco	73.4a
region	2
reversed	0
ron	26.24K
rout	278.6K
self_gain	63.86
tk	NaN
trise	NaN
type	1

Figure 9 DC operating points of M1 and M0

As it can be observed the transistors operate in reigon 2 and the current flowing through them is 0.047mA. Since 0.047mA < 0.1mA the current condition is satisfied. To determine small signal cain AC small signal AC analysis is performed which can be observed from Figure 10.

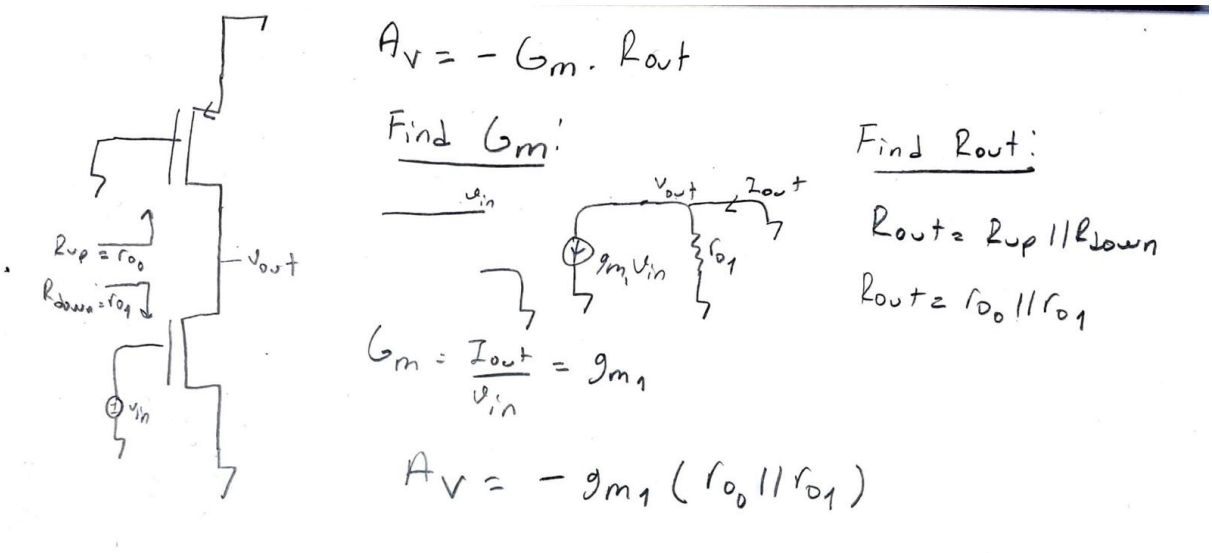

Figure 10 Small signal gain analysis

According to the found expressions by substituting the necessary values in Figure 9 the expected DC (0 frerquency) gain expression is calculated as following.

$$A_v \approx 0.5\,(278.6//1932) \approx 121.74$$

Figure 11 demonstrates magnitude of the output voltage vs frequency around 10kHz, which is a far point to DC level, when the input has 1V AC magnitude. The gain around 10kHz is 102.4 which indicates the DC gain is sufficiently above 100.

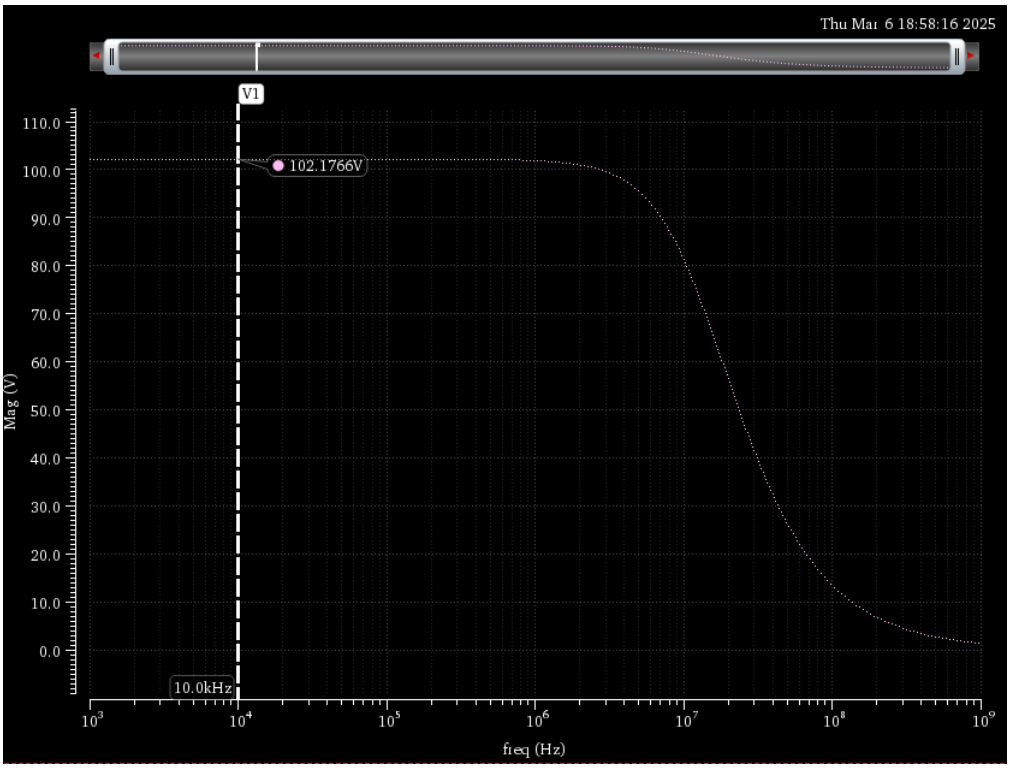

Figure 11 Gain of the amplifier

It is also important to mention that increasing the L increases the gain by $\sqrt{L}$ since λ is directly proportional with $\frac{1}{L}$ and $A_v = g_{m1}(r_{0_1}//r_{0_0}) = (\frac{1}{\lambda_0 I_D}//\frac{1}{\lambda_1 I_D})\sqrt{2\mu_n C_{ox}\frac{W}{L}_n I_D}$. In order to not distort the DC biasing $\frac{W}{L}_n$ is slightly lower than the default ratio, however the large increase in L was able to provide a large gain which is well above 100. The pmos size ratio is kept constant in order to preserve the DC biasing.

Voltage swing is the difference of maximum and minimum voltage difference of the output voltage. To keep the transistors in ON and SAT the following conditions must be satisifed.

$$V_1 + |V_{tp}| > V_{out} > V_{in} - V_{th}$$

To achieve a voltage swing greater than 1.2 V,

$$V_1 + |V_{tp}| - V_{in} + V_{th} > 1200mV$$

$$37.3mV > V_{in} - V_1$$

The obtained condition is already satisfied in the DC biasing hence a voltage swing greater than 1.2V is expected at the output. To the input 10kHz 10Mv amplitude sine wave is applied. Following figures demonstrate the minimum and maximum voltage at the output, and voltage swing can be calculated as,

$$V_{swing} = 1411mV - 205.8mV = 1205.2mV > 1200mV$$

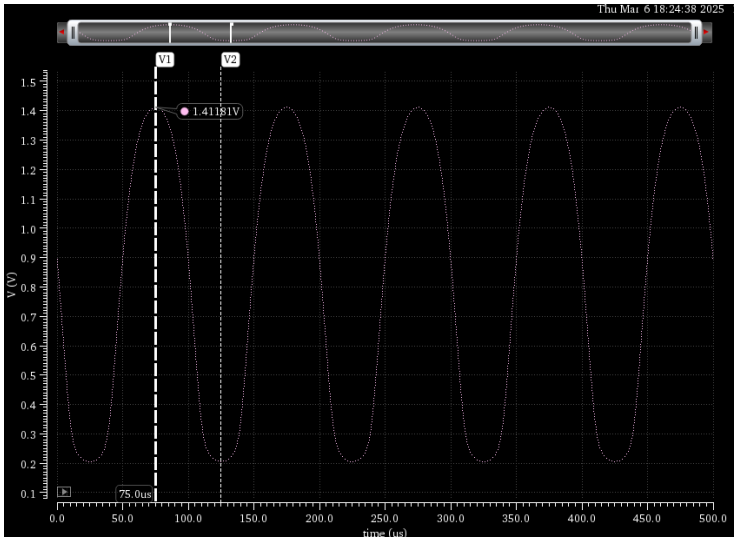

Figure 12 Maximum voltage at the output

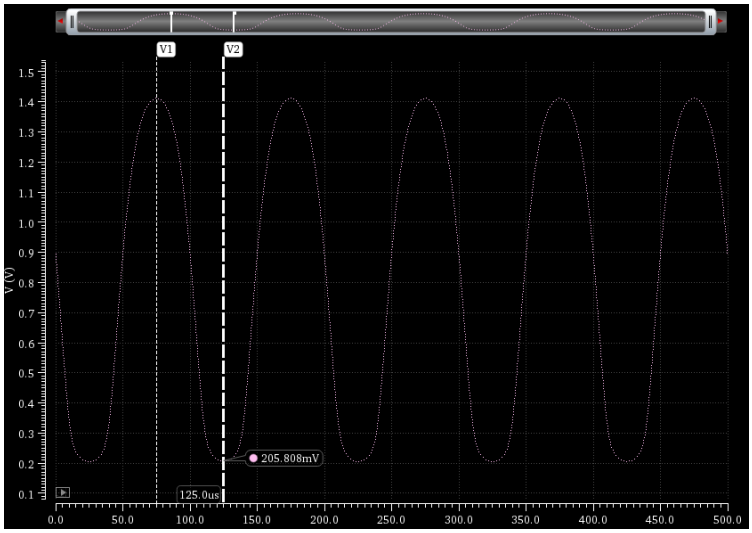

Figure 13 Minimum voltage at the output