Eray Gündoğdu Section-02 3.10.2022

EEE102 LAB2:

Introduction to VHDL

Research Questions:

How does one specify the inputs and outputs of a module in VHDL?

Inputs and outputs are defined in the module.Each ınputs and outputs must be named specificly in order to obtain a working design.In this lab we assigned inputs as in1 and in2,output as out1.

How does one use a module inside another code/module? What does PORT MAP do?

VHDL PORT MAP is used for providing interconnection between instances.In other words, PORT MAP process connects inputs and outputs to main module.A module can be used inside of another code or module with the help of PORT MAP.

What is a constraint file? How does it relate your code to the pins on your FPGA?

A constraint file is a file where crtain codes are written.By these codes, leds are arranged on the BASYS3 by assigning inputs to desired pins.

What is the purpose of writing a testbench?

The purpose of writing a testbench is to get a better understanding of the circuit designed as it displays the inputs and outputs as a waveform.

Purpose:

Aim of this experiment is to familiarize students with VİVADO and BASYS3 FPGA.

Design:

In this experiment,the design represents an analog circit with 2 switches and a light bulb.The design consists of two inputs and an output assigned as in1,in2 and out1 respectively.Inputs are connected to the output with an and gate.The inputs,in1 and in2 represents the two switches that are present in the analog circuit and inputs are assigned to switches V16 and V17(on BASYS3) respectively .The output is observed from the led U16 and represent the light bulb in the analog circuit.

Methadology:

This experiment consist of two steps.In the first step it is asked to create a design.The design is a simulation of indicated analog circuit which has two switches and a light bulb .This simulation is constructed by an and gate.And gate is constructed by using two inputs and an output.Inputs are assigned as in1 and in2.Output is assigned as out1.After assigning inputs and outputs,a specific code(out1 <= in1 and in2;) is added to “test5” file in order to obtain the and gate.By clicking “Open Eleborated Design” RTL shematic is obtained.Later on, a testbench file,named as “testbench1” is created .By adding specified codes to testbench1 file and cicking on “Run Synthsis” and “Run Behavioral Synthsis”, output waveform is displayed.

Second part of this experiment is to demonstrate the digital design on BASYS3 FPGA.This process is done by creating a constraint file named as “constraints1”.Specified codes in the lab assignment must be added to this file in order to obtain desired led-switch arrangment.After adding the codes to constraints1 file, design is demonstrated on BASYS3 FPGA by clicking “Program Device” and “Autoconnect”.By switching switches V16 and V17,and gate can be observed on BASYS3 FPGA.

Truth Table:

in1	in2	out1
0	0	0
1	0	0
0	1	0
1	1	1

Analog circuit example can be understood clearly from the truth table.If the two switches are open on the circuit the light bulb will not lit(0 0 0).If one of the switches are open again the light bulb will not lit.(1 0 0) or (0 1 0).If both of the switches are closed the light bulb will be lit.(1 1 1).

Part 1: RTL Schematic and Output Waveform

RTL schematic(Fig 1.1) and output waveform(Fig1.2) are generated as written in the methadology.

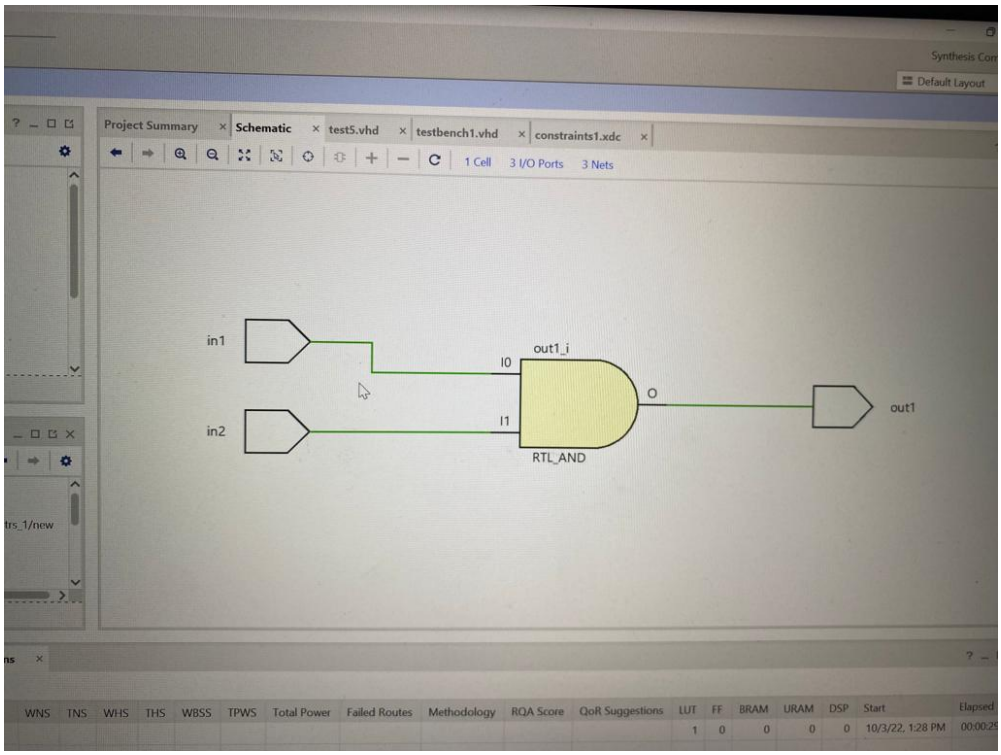


Fig 1.1

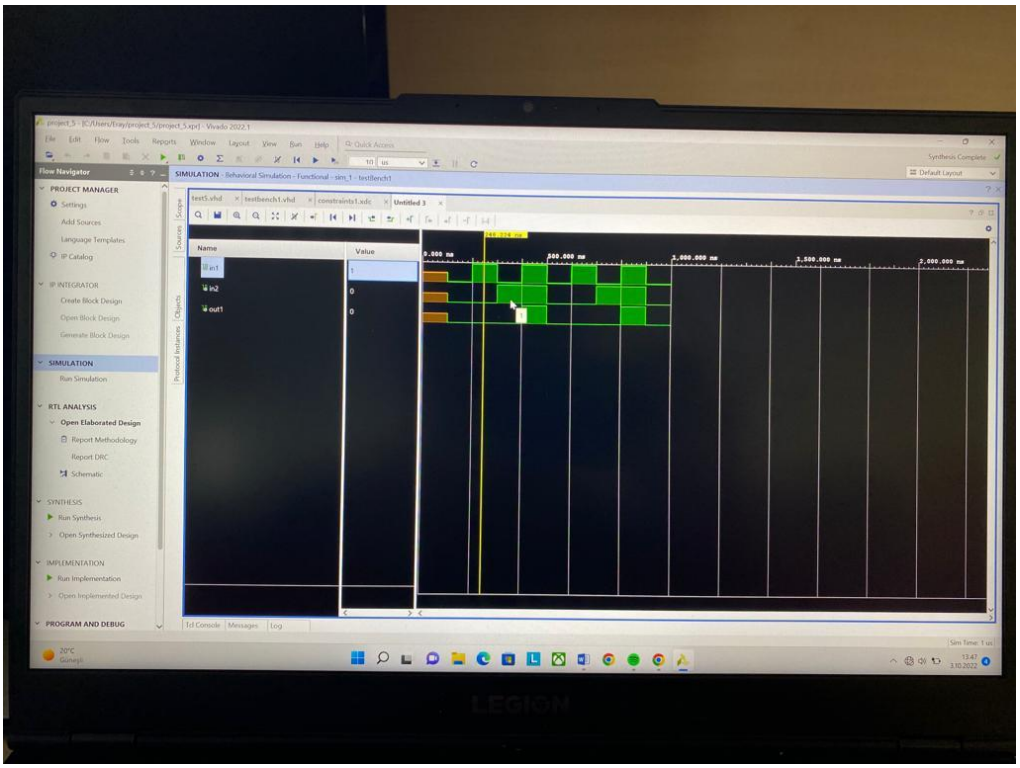
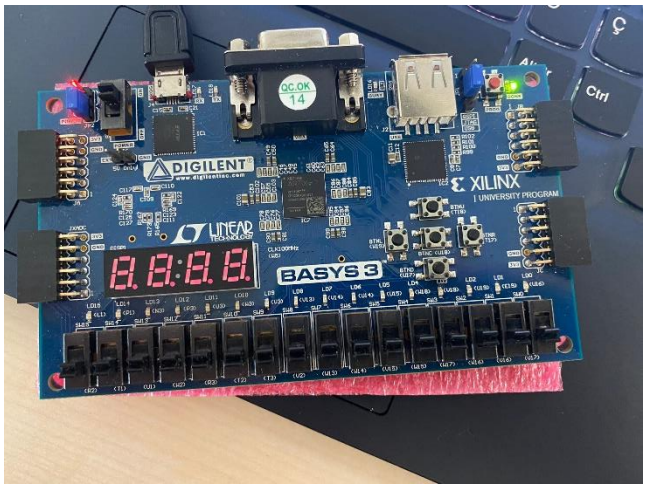


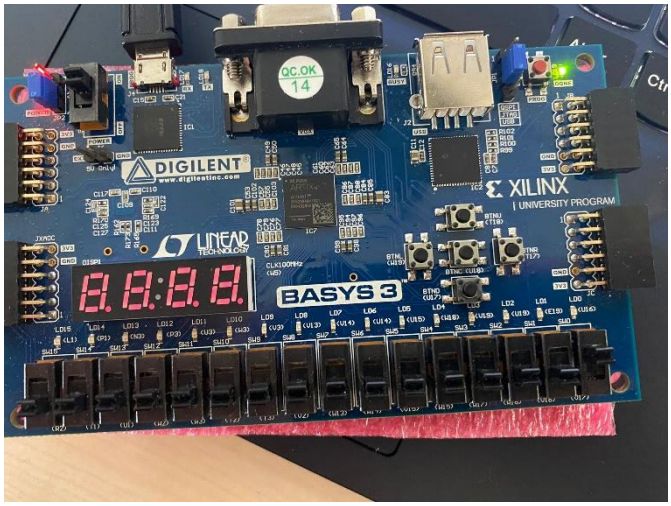
Fig 1.2

Part 2: Implementation on BASYS3

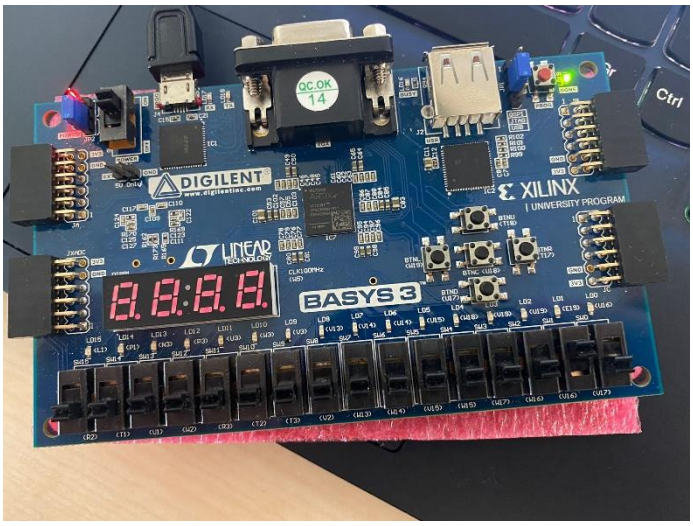
The designed circuit is implemented to BASYS3 as written in the methadology.After the implementation,by switching the switches V16 AND V17 on BASYS3 it is observed that the design operates successfuly.



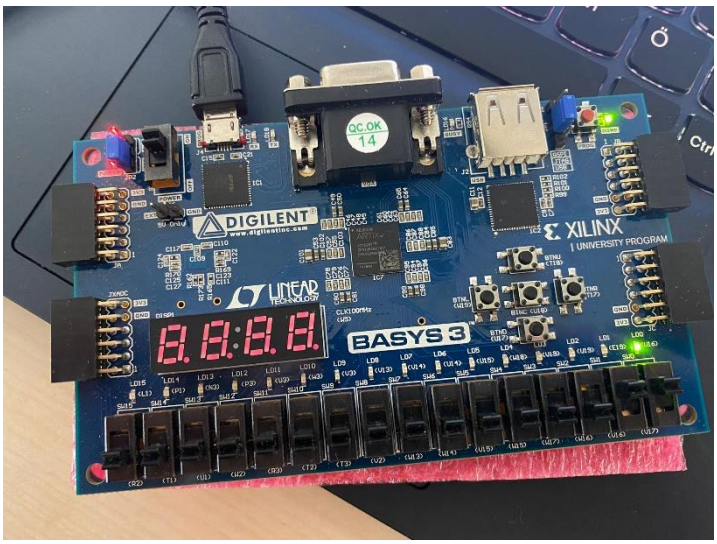
0 0 0 condition



0 1 0 condition



1 0 0 condition



1 1 1 condition

Codes:

test5 code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity test5 is
   Port ( in1 : in STD_LOGIC;
          in2 : in STD_LOGIC;
          out1 : out STD_LOGIC);
end test5;

architecture Behavioral of test5 is

begin
out1 <= in1 and in2;

end Behavioral;
```

testbench1 code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity testBench1 is
end testBench1;
architecture Behavioral of testBench1 is
COMPONENT test5
 PORT( in1 : IN STD_LOGIC;
 in2 : IN STD_LOGIC;
 out1 : OUT STD_LOGIC);
 END COMPONENT;
 SIGNAL in1 : STD_LOGIC;
 SIGNAL in2 : STD_LOGIC;
 SIGNAL out1 : STD_LOGIC;
BEGIN
 UUT: test5 PORT MAP(
in1 => in1,
in2 => in2,
out1 => out1
 );
 testBench1 : PROCESS
BEGIN
 wait for 100 ns;
 in1<='0';
```

```
in2<='0';

wait for 100 ns;
in1<='1';
in2<='0';

wait for 100 ns;
in1<='0';
in2<='1';

wait for 100 ns;
in1<='1';
in2<='1';
END PROCESS;
end Behavioral;
```

constraints1 code:

```
set_property PACKAGE_PIN V17 [get_ports {in1}]
set_property IOSTANDARD LVCMOS33 [get_ports {in1}]
set_property PACKAGE_PIN V16 [get_ports {in2}]
set_property IOSTANDARD LVCMOS33 [get_ports {in2}]
set_property PACKAGE_PIN U16 [get_ports {out1}]
set_property IOSTANDARD LVCMOS33 [get_ports {out1}]
```

Conclusion:

The experiment was successful since the code for the desired design worked successfuly and results are accurate.The experiment was a great experience for getting used to VHDL.