CS224
Fall 2020
QUIZ NO. 5

Solution comes later look below

December 23, 2020

PLEASE READ: 1. Only handwritten answers are accepted. 2. Convert your handwritten answers to pdf and upload one pdf file to Moodle. Make sure that you answer the questions in the order they are given. Provide a neat work and make sure that your answers are numbered and in the order of questions and distinguishable from each other. Do not miss the deadline.

1. **Cache Memory**

Consider a processor with an architecture similar to MIPS: byte addressable, words are 4 bytes, main memory size is 4 GB.

For the sections A and B below consider the following memory accesses with the given memory addresses. The table shows that for a word that contains a value represented with M1 is at memory location 0X10F and it is accessed for a lw instruction.

Memory Content	Used For instruction	Memory Address in Hex	Memory Address in Binary
M1	lw	10F	0001 0000 1111
M2	sw	0AF	0000 1010 1111
M3	lw	0F0	0000 1111 0000
M4	lw	05C	0000 0101 1100
M5	lw	10C	0001 0000 1100
M6	sw	0FC	0000 1111 1100
M7	sw	1FC	0001 1111 1100

A. Consider the following cache memory configuration for the above memory accesses. N= 1 (direct mapped cache), block size is 4 words, number of sets is 4.

a. Give the physical (main) memory address structure as it will be used to access the cache memory. Draw a simple figure and indicate the name and size of each subfield in terms of number of bits.

b. Draw the structure of a block in terms of its components: V (valid bit), D[1] (dirty bit), Tag, Data. Indicate the size of each field.
What is the total block size in bits?
What is the SRAM size in bits?
What is the cache memory total data field size in bytes?

c. Show the final contents of the cache memory in a figure in terms of its subfield after accessing memory locations in the order given above. Give the values of tag etc. in bits, show block data contents in terms of M1, M2 etc.

d. For each memory access indicate if it is a hit or miss. Give the miss type for each case. What is the hit rate?

[1] D bit indicates if the block content is modified during execution time and if it so when that block is emptied due to a conflict its content is written back to physical memory.

B. Consider the above memory access sequence with the following cache memory structure: N= 2 (2-way associative cache), block size is 2 words, number of sets is 4. For block replacement LRU is used. To support the LRU policy the U bit is used as illustrated in the textbook (slides). In your answer include the U bit when needed. Answer all sub questions of the question A given above, so in your answers you will have the sub questions B.a, ..., B.d.

2. Virtual Memory

A. Consider a virtual memory structure of size 4 GB. The physical (main) memory size is given as128 MB. The page size is 1 KB.

a. What is the virtual memory address structure in terms of its components and sizes (in bits)? Give a figure for the structure.

b. What is the structure of one row of the page table? Give it in terms of its subfield names and sizes in bits. Consider both D: dirty and V: bit. What is the size of one row in number of bits. Give a figure for the structure.

c. Now consider a 2-way (2-entry) TLB structure. Draw the structure of the TLB. Give it in terms of its subfield names and sizes in bits. Consider both D: dirty and V: bit. What is its total size? Assume that LRU is used for replacement. Use the minimum number of U bits.

d. Now consider a 4-way TLB structure. Draw the structure of the TLB. Give it in terms of its subfield names and sizes in bits. Consider both D: dirty and V: bit. What is the size of one row in number of bits. Draw it. Assume that LRU is used for replacement. Use two U bits for each entry of the TLB (we need 2 U bits since it is it is 4-way: we have to keep track of the utilization age of each of the 4 ways).

B. Consider a virtual memory environment of size 4KB with page size of 0.25 KB. Physical memory size is 2KB. (This part is independent of question 2.A.)

a. Consider the following memory accesses from left to right. Show the final content of the memory page table including the V bit and D bit after performing "all" memory accesses. For unknown entries assume 0 values.

Memory Access No.	1	2	3	4	5	6	7	8
Virtual Memory Address	0B4	0F0	2A0	2AC	4AC	0CC	244	B00
Physical Memory Address	2B4	2F0	4A0	4AC	0AC	2CC	444	700
Instruction Executed	sw	lw	lw	sw	lw	lw	sw	lw

b. Consider a TLB structure with two entries and with LRU replacement policy. Draw the TLB include D and U bits. Show the size of each component in number of bits. What is total size in terms of number of bits?

Show TLB contents in hexadecimal after "each" memory access. Indicate if a memory access produces a hit or miss for the TLB contents. State the type of each miss.

CS224
Fall 2020
Quiz No. 5
Dec. 26'20

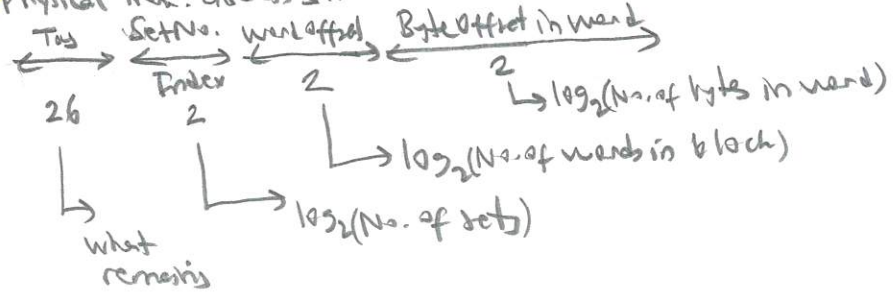
1. Cache Memory

MIPS: Byte addressable
Word: 4 bytes
Main Mem Size = 4GB → $2^2 \times 2^{30} = 2^{32}$

1.A. Cache Mem.

N = 1, Block Size: 4 words
No. of sets = 4

a. Physical mem. address structure



b. Cache Memory Block Structure

Block size = 1+1+26+128 = 156 bits ← (= set size)
SRAM size = 4 × 156 = 624 bits (Cache mem + overhead)
Cache Mem Total Data Field Size = No. of sets × N × Block Size (in byte)
4 × 1 × (4×4) = 64 bytes

c. Cache Mem Content (Set No)

M1: 0001 0000 1111 — Comp. Miss (Compulsory miss)
M2: 0000 10 11 1111 (sw) — Comp. Miss D=1
M3: 0000 1111 0000 — Comp. Miss
M4: 0000 0101 1100 — Comp. Miss
M5*: 0001 0000 1100 — Hit (Tag = Tag of M1)
M6: 0000 1111 1100 (sw) — Hit (Tag = Tag of M3)
M7: 0001 1111 1100 (sw) — Capacity Miss

Set No: underlined

Set

M2:

M3:

M4:

M7:

M6:

M5:

Cache Mem. Final Contents

V	D	Tag	Data	SetNo
1	1	0001	11 M7	11
1	1	0000	10 M2	10
1	0	0000	01 M4	01
1	0	0001	00 M1/M5	00

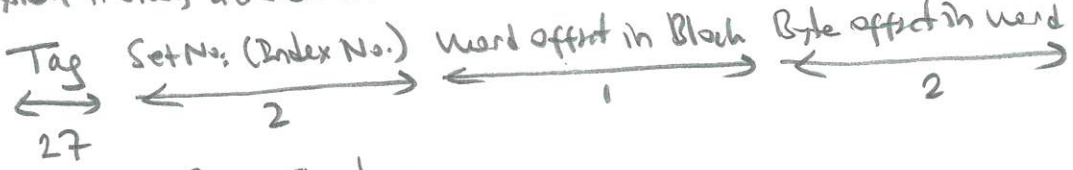
Tag is 32 bits, but only the relevant part is shown.

Hit/Miss Summary
First 4: Compulsory Miss
M5, M6: Hit
M7: Capacity Miss
Hit Rate: 2/7

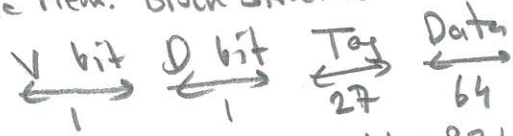
1-B Cache Mem. (cont.)

N=2, Block size: 2 words, No. of Sets: 4 Block Replacement: LRU

a. Physical memory address structure



b. Cache Mem. Block Structure



Block size: 1+1+27+64 = 93 bits

Set Size: 2 × Block size: 2×93 = 186 bits

SRAM Size: 4 × Set Size: 4×186 = 744 bits

↳ But we have one more detail: U bits for each set

4 sets × 1 U bit size = 4 bits

∴ Total SRAM size: 748 bits

Note: (No. of U bits for a set) = $\log_2 N$ ← General rule for U bits/set

c. Cache Memory Contents as we access memory

U bit: shows most recently accessed block in a set.

M1: 0001 0000 1111 Comp. Miss

M2: 0000 1010 1111 Comp. Miss

M3: 0000 1111 0000 Comp. Miss

M4: 0000 0101 1100 Comp. Miss

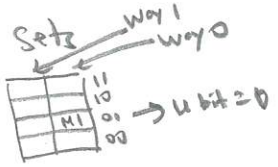
M5: 0001 0000 1100 Conflict Miss

M6: 0000 1111 1100 Comp. Miss

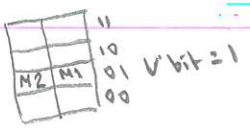
M7: 0001 1111 1100 Conflict Miss

Hit Rate = 0 All misses

M1:

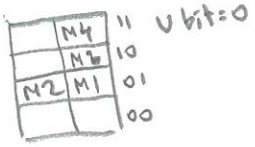


M2:



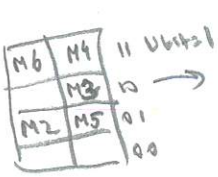
M3:

M4:

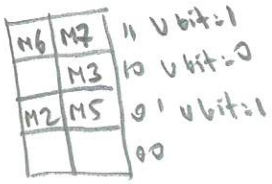


M5:

M6:



M7:

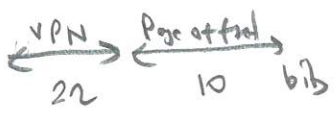


U bit: shows most recently accessed block

2. Virtual Memory

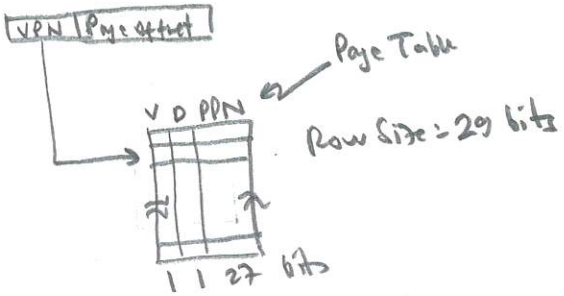
2.A. Virtual Mem Size = 4GB, 2^{32} Main Mem Size = 128 MB 2^{27} Page Size: 1K 2^{10}

a. VM add. structure

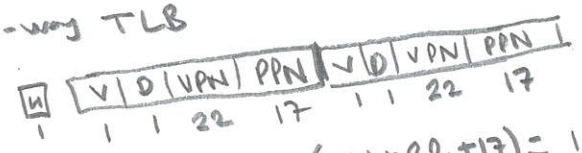


PM add. structure

b.



c. 2-way TLB



TLB Size = $1 + 2 \times (1+1+22+17) = 1 + 2 \times 41 = 83$ bits

d. 4-way TLB

U = 2 bits for each way

$4 \times (2+1+1+22+17) = 4 \times 43 = 172$ bits

We have to keep track of the life of each entry

Answer for this → Why U = 2 bits?

2.B VM Size = 4KB $\rightarrow 2^{12}$, PM Size = 2KB $\rightarrow 2^{11}$

Page Size = 0.25 KB $\rightarrow \frac{1}{4} \times 2^{10} = 2^8$

No. of VM pages $= \frac{2^{12}}{2^8} = 2^4$

No. of PM pages $= \frac{2^{11}}{2^8} = 2^3$

No	VM Address	PM Address	
1	0B4	2B4	SW
2	0F0	2F0	
3	2A0	4A0	
4	2AC	1AC	SW
5	1AC	0AC	
6	0CC	2CC	
7	244	144	SW
8	B00	700	

No. of VM pages $= 2^4 = 16$

	V	D	PPN
1111			
1110			
1101			
1100			
1011	1	0	111
1010			
1001			
1000			
0111			
0110			
0101			
0100	1	0	000
0011			
0010	1	1	100
0001			
0000	1	1	010

TLB Content Progress as we access memory

VPN & PPN are shown in decimal

①

No.	Way 1 V	D	VPN	PPN	Way 0 V	D	VPN	PPN	U	
					0	0	0	0	X	→ Initial condition
X	0	0	0	0	1	1	0	2	0	→ 1st compulsory miss, 2nd hit
1,2	0	0	0	0	1	1	0	2	1	→ 3rd compulsory miss, 4th hit
3,4	1	1	2	4	1	0	4	0	0	→ 5th conflict miss
5	1	1	2	4	1	0	4	0	1	→ 6th conflict miss
6	1	0	0	2	1	1	2	4	0	→ 7th compulsory miss
7	1	0	0	2	1	1	2	4	1	→ 8th compulsory miss
8	1	0	11/B	7						

* U: shows the last way/unit used.

Hit Rate = 2/8

CS224
FALL 2024
QUIZ NO. 4 Sec. 1 & 2

Student Name/Section:

Student Name/Section:

Solutions

Date: Dec 17, '24

PLEASE READ - Notes. 1. If you forget to sign below or forget to provide any of the above information 30 points will be taken off. 2. You have to give the answers in full detail you cannot leave them as expressions to be completed. 3. After reading these notes both students must sign here: _____

RULES: Two students work together. You can only use your notes, textbook, slides, and greencard.

1. A computer has a cache of 64KB with a block size of 64 Bytes. Assume that the main memory of size 256MB. Words are 32 bits and byte-addressable.

a. If the cache is direct mapped, what is the (physical) address format used to access this cache? Briefly explain.

Main memory 256 MB → 2^{28}

word 32 bits → 4 bytes

Block size 64 Bytes → No. of words/block = Block size/word size = 64/4 = 16 words/Block

No. of sets = (Cache size)/(N × Block size)

N = 1 direct mapped

No. of sets = 64KB/64 bytes = 2^{10}

Tag	Index (Set No)	word off. in Block/Byte	offset in word
12	10	4	2

⇒ 12/10/4/2

2, 4, 8, 16, 32, 64, 128, 256

b. If the cache is 4-way associative, what is the address format? Briefly explain.

4 way associative ⇒ No. of sets = (No of sets with N=1)/4

⇒ No. of sets = 8

Tag	Set	WOB	BOW
14	8	4	2

WOB: word offset in Block

BOW: Byte offset in word

c. If the cache is fully associative, what is the address format? Briefly explain. What is the SRAM size in number of bits?

No. of sets = 1 No need to indicate set no.

Tag	WOB	BOW
22	4	2

SRAM Size

No LRU is assumed (no u bit)

No D bit is assumed

Each block: V / Tag / Data ← each block 64 bytes

1 / 22 / 64×8 = 512

No. of block 2^{10} = 1024

$2^{10} \times (1 + 22 + 512)$

535 bits = 547,840 bits

1024 × 535 = 5120 + 30720 + 51200 = 547840

2. Consider the following address structure. ← BWO = 2

tag: 12 bits, set no. (index): 2 bit, word block offset: 2 bit. The words are 4 bytes in length.

a. What is the physical memory size in KB?

Tag / Set / WBO / BWO
12 2 2 2 → 18 bits

$\Rightarrow 2^8 \times 2^{10} = 256$ KB

b. What is the cache data area size in bytes (N= 2, 2-way associative)?

Cache data area size = No. of Sets × N × Block Size

$\Rightarrow 2^2 \times 2^1 \times (2^2 \times 2^2)$

$2^7 = 128$ bytes

↑ No. of words
WBO = 2
There are 4 words/block

3. For the memory structure given in question 2 assume that N= 1. Consider the following consecutive memory accesses

0x10, 0x18, 0x08, 0x0C0, x50, 0x5C

(0x10 means 0x0..10, the same applies to the other addresses). Show the change in the cache memory and indicate the type of miss (if any) for each memory access. Assume LRU for cache replacement, if needed. Calculate the hit rate.

N=1 Direct-access cache memory

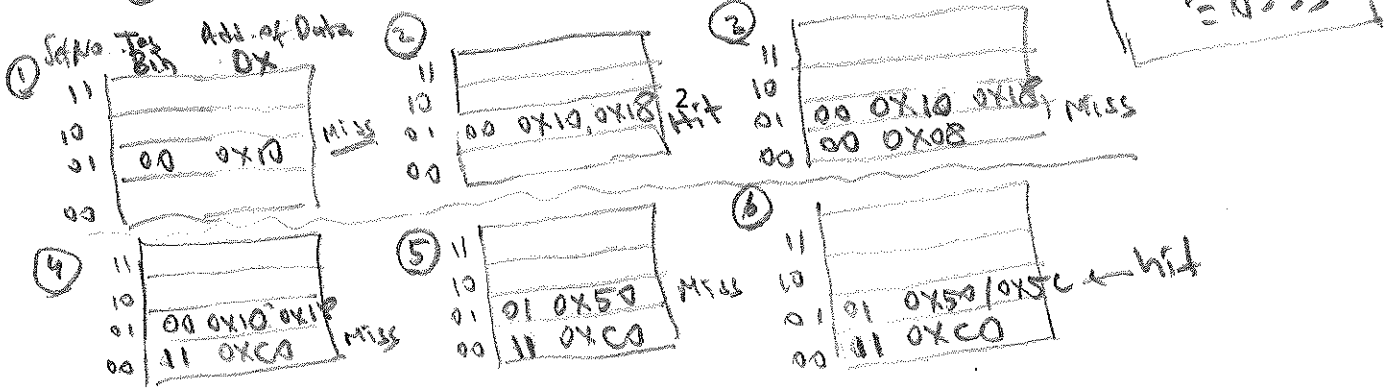
Tag / Set / WBO / BWO
12 2 2 2

No. of bits for set no: 2
There are 4 sets

With N=1 LRU is not needed!

		Tag	Set		
①	0X10 →	0001	0000	→ Tag=00	Set:01
②	0X18 →	0001	1000	→ Tag:00	Set:01
③	0X08 →	0001	1000	→ Tag:00	Set:10
④	0XC0 →	1100	0000	→ Tag:11	Set:00
⑤	0X50 →	0101	0000	→ Tag:01	Set:00
⑥	0X5C →	0101	1100	→ Tag:01	Set:11

Hit rate
2/6 = 1/3
≈ 0.33



CS224
SPRING 2024
QUIZ NO. 4

Student Name/Section: 5 & 6 Solutions

Student Name/Section:

Date: May 2, '24

PLEASE READ - Notes. 1. If you forget to sign below or forget to provide any of the above information 30 points will be taken off. 2. You have to give the answers in full detail you cannot leave them as expressions to be completed. 3. After reading these notes both students must sign here: _____

1. A computer has a cache of 32KB with a block size of 32 Bytes. Assume that the main memory of size 128MB. Words are 32 bits and byte-addressable.

a. If the cache is direct mapped, what is the (physical) address format used to access this cache? Briefly explain.

No. of blocks = Cache Size / Block Size = 32 KB / 32 bytes = $(2^5 \times 2^{10}) / 2^5 = 2^{10}$

128 MB = $2^7 \times 2^{20}$ → Phys. mem. addr size = 27 bits

Words 32 bits = 4 bytes → 2 bits byte offset

No. of words/block = Block Size / word size = 32 bytes / 4 bytes = $2^5/2^2 = 8$

Tag / Set No / word Block offset / Byte offset

12 10 3 2

Tag	Set No	WBO	BO
12	10	3	2

← No. of bits

↑ No. of blocks: 0, 2, 4, 8, 16, 32, 64, 128

↑ No. of sets

Word off.

b. If the cache is 4-way associative, what is the address format? Briefly explain.

4-way associative No. of sets $2^{10}/2^2 = 2^8$

Tag	Set No.	WBO	BO
14	8	3	2

← No. of bits

WBO: Word Block off.

BO: Byte off.

c. If the cache is fully associative, what is the address format? Briefly explain. What is the SRAM size?

Fully association: No need for set No. ⇒

Tag	WBO	BO
22	3	2

← No. of bits

Block Structure: V / Tag / Data

1 22 32×8 ← bits

279 bits

32 × 8 = 256, 23, 279

SRAM Size = No. of block × Block Size = $2^{10} \times 279$

If we include D bit Block Structure: D / V / Tag / Data

⇒ $2^{10} \times 280$ No. of V bits/block

LRU ⇒ (If we want to implement LRU each block must have [Tag (No. of Blocks)] no. of bits per block

LRU blocks V / V / Tag / Data ⇒ 10 / 1 / 22 / 32×8 ⇒ $2^{10} \times 289$ bits

each location we address contains a byte (8 bits)

2. Consider the following address structure (note that at each memory address one byte is stored, i.e. it is a byte addressable system).

(WBO) (BO)

tag: 12 bits, set no. (index): 1 bit, word block offset: 1 bit, byte offset: 2 bits.

a. What is the physical memory size in KB?

Tag / Set No / WBO / BO
12 1 1 2 → 16 bits $2^{16} = 2^6 \times 2^{10} = 64$ KB

77
x 4
308

64 KB

b. What is the cache memory size in bytes (N= 2, 2-way associative)?

N=2

Block structure
← Good enough as an answer

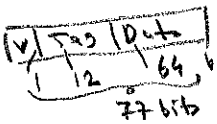
4 x 8 = 32 bytes

WBO = 1 bit ← 2 words/block
BO = 2 bits ← 4 bytes/word
→ Each block is 8 bytes

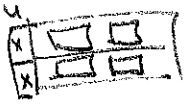
If we also consider SRAM size
Assume LRU

If we consider SRAM size

Tag / Set No / WBO / BO ⇒ Block Structure
12 1 1 2



SRAM Str.



SRAM Size

4
2 + 4 x 77 = 310 bits

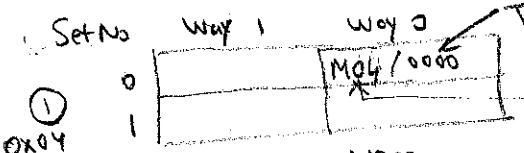
If random replacement
308 bits

c. For N= 2 consider the following consecutive memory accesses 4, 24, 60, 4, 44, 72 (all decimal numbers). Show the change in the cache memory and indicate the type of miss (if any) for each memory access. Assume LRU for cache replacement. Indicate conflict types.

In bin.

① 4 → 0X04 : 0000 0100
② 24 → 0X18 : 0001 1000
③ 60 → 0X3C : 0011 1100
④ 4 → 0X04 : 0000 0100
⑤ 44 → 0X2C : 0010 1100
⑥ 72 → 0X48 : 0100 1000

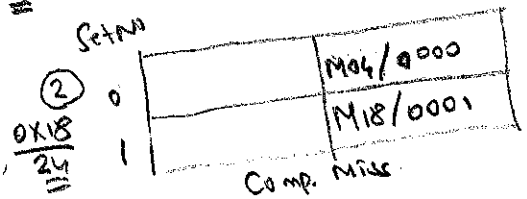
① 0X04 = 4



Mem. add. in hex.

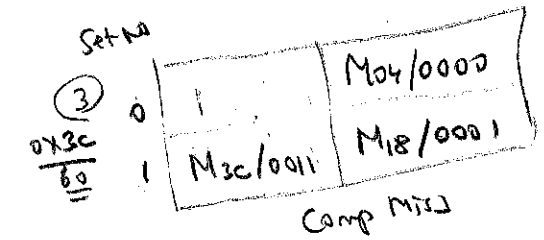
Comp. Miss

② 0X18 = 24



Comp. Miss

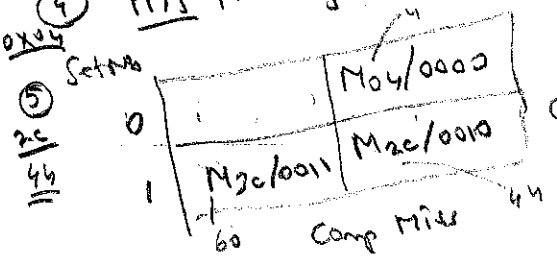
③ 0X3C = 60



Comp Miss

④ 0X04 Hit No change in cache mem.

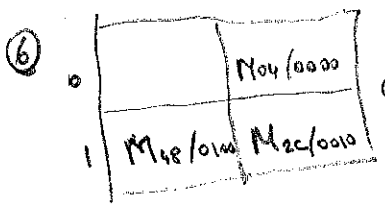
⑤ 2c = 44



Comp Miss

Comp Miss

⑥



Comp. Miss

Continued

2. Consider the following address structure:

tag: 20 bits, set no. (index): 1 bit, block offset: 1 bit, byte offset: 2 bits.

a. What is the physical memory size in MB?

Total no. of bits: $20+1+1+2 = 2^{24}$ ← No. of bits in phys. mem address

$2^{24} \rightarrow 2^4 \times 2^{20} \rightarrow$ 16 MB

b. What is the cache memory (SRAM) size in bits for (N= 4, (4-way associative)? Note that for eviction Random replacement is used.

no bit is needed

Block offset 1 bit → 2 words/block
Byte offset 2 bits → 4 bytes/word

Data: Each block is 2 words
each word is 4 bytes
⇒ $2 \times 4 \times 8 = 64$

set no { 1, 0 } ← In each set we have 4 blocks (N=4)

Block Structure

V	Tag	Block
1	20	64

SRAM Size = No. of sets × N × Block size
$= 2 \times 4 \times 85 =$ 680 bits ← corrected

c. Assume that for N> 1 we want to use FIFO (First In First Out) policy for cache memory replacement. How can you implement FIFO? Define a suitable data structure for its implementation. How many bits are required for its implementation for different values of N? Obhtain a general formula for the data structure size in number of bits.

FIFO : Queu

Pointer → 00, 01, 10, 11

First entry to point is: 0
After entering an entry pointer is updated
Pointer = mod (Pointer+1, 3) Entries are always
replaced in the same order Fill: 0,1,2,3, Evict: 0,1,2,3

No. of bits needed $\log_2 N$ assuming that N is multiple of 2.

d. Consider the following consecutive memory accesses for time t= 0, 1, 2 ns: 44, 74, 12, 54 (all decimal numbers). Show the change in the cache memory and indicate the type of miss (if any) for each memory access. Use FIFO if needed. Assume that N= 2.

Bin.
44 = 0x2C → 0010 1100 → Goes to set no.1
74 = 0x4A → 0100 1010 → set no.0
12 = 0x0C → 0000 1100 → set no.1
54 = 0x36 → 0011 0110 → set no.0
Tag ↑ Set No.

They all have different tags

M_{44} = contents of location at address 44 is

Set No	Initial cont.	t=0	t=1	t=2	t=3
1			M_{44}	M_{12}	M_{12}
0	All empty	M_{44}	M_{74}	M_{74}	M_{54}

All memory accesses cause compulsory miss.

⇒ 4 comp. misses

CS224
Fall 2020
QUIZ NO. 5

December 23, 2020

Solution comes later look below

PLEASE READ: 1. Only handwritten answers are accepted. 2. Convert your handwritten answers to pdf and upload one pdf file to Moodle. Make sure that you answer the questions in the order they are given. Provide a neat work and make sure that your answers are numbered and in the order of questions and distinguishable from each other. Do not miss the deadline.

1. Cache Memory

Consider a processor with an architecture similar to MIPS: byte addressable, words are 4 bytes, main memory size is 4 GB.

For the sections A and B below consider the following memory accesses with the given memory addresses. The table shows that for a word that contains a value represented with M1 is at memory location 0X10F and it is accessed for a lw instruction.

Memory Content	Used For instruction	Memory Address in Hex	Memory Address in Binary
M1	lw	10F	0001 0000 1111
M2	sw	0AF	0000 1010 1111
M3	lw	0F0	0000 1111 0000
M4	lw	05C	0000 0101 1100
M5	lw	10C	0001 0000 1100
M6	sw	0FC	0000 1111 1100
M7	sw	1FC	0001 1111 1100

A. Consider the following cache memory configuration for the above memory accesses. N= 1 (direct mapped cache), block size is 4 words, number of sets is 4.

a. Give the physical (main) memory address structure as it will be used to access the cache memory. Draw a simple figure and indicate the name and size of each subfield in terms of number of bits.

b. Draw the structure of a block in terms of its components: V (valid bit), D[1] (dirty bit), Tag, Data. Indicate the size of each field.
What is the total block size in bits?
What is the SRAM size in bits?
What is the cache memory total data field size in bytes?

c. Show the final contents of the cache memory in a figure in terms of its subfield after accessing memory locations in the order given above. Give the values of tag etc. in bits, show block data contents in terms of M1, M2 etc.

d. For each memory access indicate if it is a hit or miss. Give the miss type for each case. What is the hit rate?

[1] D bit indicates if the block content is modified during execution time and if it so when that block is emptied due to a conflict its content is written back to physical memory.

B. Consider the above memory access sequence with the following cache memory structure: N= 2 (2-way associative cache), block size is 2 words, number of sets is 4. For block replacement LRU is used. To support the LRU policy the U bit is used as illustrated in the textbook (slides). In your answer include the U bit when needed. Answer all sub questions of the question A given above, so in your answers you will have the sub questions B.a, ..., B.d.

2. Virtual Memory

A. Consider a virtual memory structure of size 4 GB. The physical (main) memory size is given as128 MB. The page size is 1 KB.

a. What is the virtual memory address structure in terms of its components and sizes (in bits)? Give a figure for the structure.

b. What is the structure of one row of the page table? Give it in terms of its subfield names and sizes in bits. Consider both D: dirty and V: bit. What is the size of one row in number of bits. Give a figure for the structure.

c. Now consider a 2-way (2-entry) TLB structure. Draw the structure of the TLB. Give it in terms of its subfield names and sizes in bits. Consider both D: dirty and V: bit. What is its total size? Assume that LRU is used for replacement. Use the minimum number of U bits.

d. Now consider a 4-way TLB structure. Draw the structure of the TLB. Give it in terms of its subfield names and sizes in bits. Consider both D: dirty and V: bit. What is the size of one row in number of bits. Draw it. Assume that LRU is used for replacement. Use two U bits for each entry of the TLB (we need 2 U bits since it is it is 4-way: we have to keep track of the utilization age of each of the 4 ways).

B. Consider a virtual memory environment of size 4KB with page size of 0.25 KB. Physical memory size is 2KB. (This part is independent of question 2.A.)

a. Consider the following memory accesses from left to right. Show the final content of the memory page table including the V bit and D bit after performing "all" memory accesses. For unknown entries assume 0 values.

Memory Access No.	1	2	3	4	5	6	7	8
Virtual Memory Address	0B4	0F0	2A0	2AC	4AC	0CC	244	B00
Physical Memory Address	2B4	2F0	4A0	4AC	0AC	2CC	444	700
Instruction Executed	sw	lw	lw	sw	lw	lw	sw	lw

b. Consider a TLB structure with two entries and with LRU replacement policy. Draw the TLB include D and U bits. Show the size of each component in number of bits. What is total size in terms of number of bits?

Show TLB contents in hexadecimal after "each" memory access. Indicate if a memory access produces a hit or miss for the TLB contents. State the type of each miss.

Some information about miss types:

Compulsory Miss: First access to data with a unique tag number.

Conflict Miss: Access to recently used data with the same tag; however, data is evicted and not in the cache anymore.

Capacity Miss: A special type of conflict miss, occurs when the data is recently used, but not in the cache anymore and all the cache is completely full. (not only the set for accessed block, when all the data on all the sets is full)

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Dec. 26'20

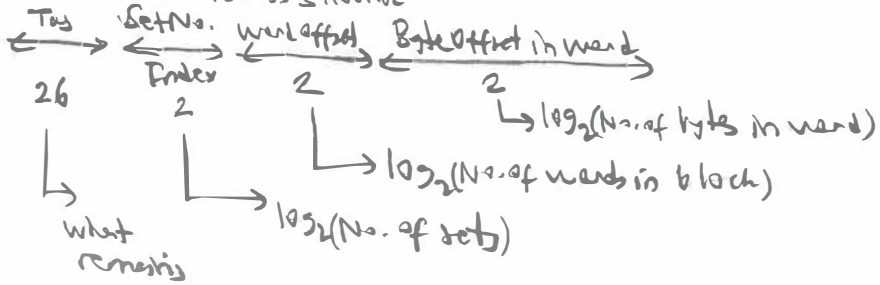
1. Cache Memory

MIPS: Byte addressable
Word = 4 bytes
Main Mem Size = 4GB $\rightarrow 2^2 \times 2^{30} = 2^{32}$

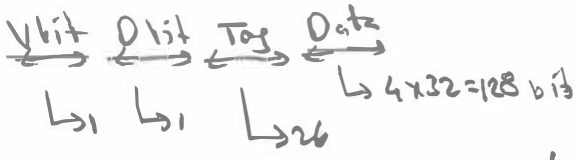
1.A. Cache Mem.

N=1, Block size = 4 words
No. of sets = 4

a. Physical mem. address structure



b. Cache Memory Block Structure



Block size = 1+1+26+128 = 156 bits ← (= set size)

SRAM size = 4 x 156 = 624 bits (Cache mem + overhead)

Cache Mem Total Data Field Size = No. of sets x N x Block Size (in byte)

4 x 1 x (4 x 4) = 64 bytes

c. Cache Mem Content (Set No)

M1: 0001 0000 1111 — Comp. Miss (Compulsory miss)
M2: 0000 1000 1111 (sw) — Comp. Miss D=1
M3: 0000 1111 0000 — Comp. Miss
M4: 0000 0101 1100 — Comp. Miss
M5*: 0001 0000 1100 — Hit (Tag = Tag of M1)
M6: 0000 1111 1100 (sw) — Hit (Tag = Tag of M3)
M7: 0001 1111 1100 (sw) — Comp. miss

Set No: underlined

M1: Set 11 / 10 / 01 / 00 → M1
M2: 11 → M2 / 10 → M1 / 01 / 00
M3: 11 → M3 / 10 → M2 / 01 → M1 / 00
M4: 11 → M3 / 10 → M2 / 01 → M4 / 00 → M1
M5: 11 → M3 / 10 → M2 / 01 → M4 / 00 → M1 M5
M6: 11 → M3 M6 / 10 → M2 / 01 → M4 / 00 → M1 M5
M7: 11 → M7 / 10 → M2 / 01 → M4 / 00 → M1 M5

Cache Mem. Final Content

V	D	Tag	Data	Set No
1	1	0001	11	M7 — 11
1	1	0000	10	M2 — 10
1	0	0000	01	M4 — 01
1	0	0001	00	M1/M5 — 00

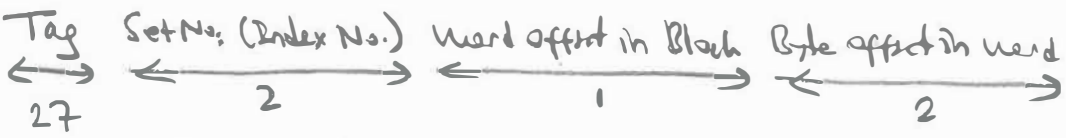
Tag is 32 bits, but only the relevant part is shown

Hit/Miss Summary
First 4: Compulsory Miss
M5, M6: Hit
M7: Comp. miss
Hit rate: 2/7

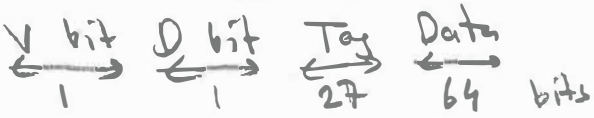
1-B Cache Mem. (cont.)

N=2, Block Size: 2 words, No. of Sets: 4 Block Replacement: LRU

a. Physical memory address structure



b. Cache Mem. Block Structure



Block size: 1+1+27+64 = 93 bits

Set Size: 2 x Block size: 2x93 = 186 bits

SRAM Size: 4 x Set Size: 4x186 = 744 bits

↳ But we have one more detail: U bits for each set

4 sets x 1 U bit size = 4 bits

∴ Total SRAM size: 748 bits

Note: (No. of U bits for a set) = $\log_2 N$ ← General rule for U bits/set

c. Cache Memory Contents as we access memory

M1: 0001 0000 1111 Comp. Miss

M2: 0000 1010 1111 Comp. Miss

M3: 0000 1111 0000 Comp. Miss

M4: 0000 0101 1100 Comp. Miss

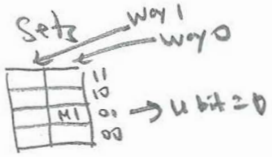
M5: 0001 0000 1100 Hit (same data with M1)

M6: 0000 1111 1100 Comp. Miss

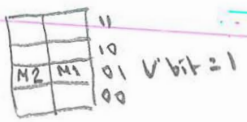
M7: 0001 1111 1100 Comp. miss

U bit: shows most recently accessed block in a set.

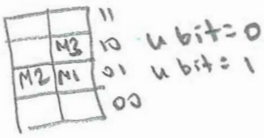
M1:



M2:



M3:

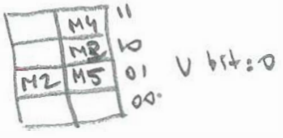


Hit rate = 1/7

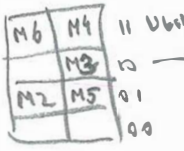
M4:

$M_1 = M_5$

M5:



M6:



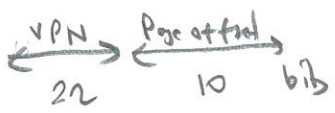
M7:

U bit: shows most recently accessed block

2. Virtual Memory

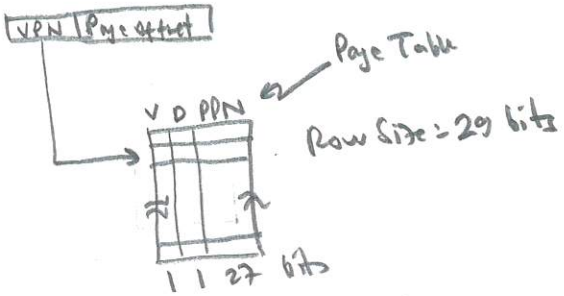
2.A. Virtual Mem Size = 4GB, 2^{32} Main Mem Size = 128 MB 2^{27} Page Size: 1K 2^{10}

a. VM add. structure

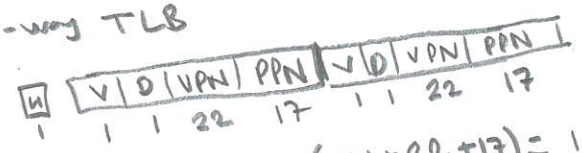


PM add. structure

b.



c. 2-way TLB



TLB Size = $1 + 2 \times (1+1+22+17) = 1 + 2 \times 41 = 83$ bits

d. 4-way TLB

U = 2 bits for each way

$4 \times (2+1+1+22+17) = 4 \times 43 = 172$ bits

We have to keep track of the life of each entry

Answer for this → Why U = 2 bits?

2.B VM Size = 4KB $\rightarrow 2^{12}$, PM Size = 2KB $\rightarrow 2^{11}$

Page Size = 0.25 KB $\rightarrow \frac{1}{4} \times 2^{10} = 2^8$

No. of VM pages $= \frac{2^{12}}{2^8} = 2^4$

No. of PM pages $= \frac{2^{11}}{2^8} = 2^3$

No	VM Address	PM Address	
1	0B4	2B4	SW
2	0F0	2F0	
3	2A0	4A0	
4	2AC	1AC	SW
5	1AC	0AC	
6	0CC	2CC	
7	244	144	SW
8	B00	700	

No. of VM pages $= 2^4 = 16$

	V	D	PPN
1111			
1110			
1101			
1100			
1011	1	0	111
1010			
1001			
1000			
0111			
0110			
0101			
0100	1	0	000
0011			
0010	1	1	100
0001			
0000	1	1	010

TLB Content Progress as we access memory

VPN & PPN are shown in decimal

①

No.	Way 1 V	D	VPN	PPN	Way 0 V	D	VPN	PPN	U	
					0	0	0	0	X	→ Initial condition
X	0	0	0	0	1	1	0	2	0	→ 1st compulsory miss, 2nd hit
1,2	0	0	0	0	1	1	0	2	1	→ 3rd compulsory miss, 4th hit
3,4	1	1	2	4	1	0	4	0	0	→ 5th conflict miss
5	1	1	2	4	1	0	4	0	1	→ 6th conflict miss
6	1	0	0	2	1	1	2	4	0	→ 7th compulsory miss
7	1	0	0	2	1	1	2	4	1	→ 8th compulsory miss
8	1	0	11/B	7						

* U: shows the last way/unit used.

Hit Rate = 2/8

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December 23, 2020

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1. **Cache Memory**

Consider a processor with an architecture similar to MIPS: byte addressable, words are 4 bytes, main memory size is 4 GB.

For the sections A and B below consider the following memory accesses with the given memory addresses. The table shows that for a word that contains a value represented with M1 is at memory location 0X10F and it is accessed for a lw instruction.

Memory Content	Used For instruction	Memory Address in Hex	Memory Address in Binary
M1	lw	10F	0001 0000 1111
M2	sw	0AF	0000 1010 1111
M3	lw	0F0	0000 1111 0000
M4	lw	05C	0000 0101 1100
M5	lw	10C	0001 0000 1100
M6	sw	0FC	0000 1111 1100
M7	sw	1FC	0001 1111 1100

A. Consider the following cache memory configuration for the above memory accesses. N= 1 (direct mapped cache), block size is 4 words, number of sets is 4.

a. Give the physical (main) memory address structure as it will be used to access the cache memory. Draw a simple figure and indicate the name and size of each subfield in terms of number of bits.

b. Draw the structure of a block in terms of its components: V (valid bit), D[1] (dirty bit), Tag, Data. Indicate the size of each field.
What is the total block size in bits?
What is the SRAM size in bits?
What is the cache memory total data field size in bytes?

c. Show the final contents of the cache memory in a figure in terms of its subfield after accessing memory locations in the order given above. Give the values of tag etc. in bits, show block data contents in terms of M1, M2 etc.

d. For each memory access indicate if it is a hit or miss. Give the miss type for each case. What is the hit rate?

[1] D bit indicates if the block content is modified during execution time and if it so when that block is emptied due to a conflict its content is written back to physical memory.

B. Consider the above memory access sequence with the following cache memory structure: N= 2 (2-way associative cache), block size is 2 words, number of sets is 4. For block replacement LRU is used. To support the LRU policy the U bit is used as illustrated in the textbook (slides). In your answer include the U bit when needed. Answer all sub questions of the question A given above, so in your answers you will have the sub questions B.a, ..., B.d.

2. Virtual Memory

A. Consider a virtual memory structure of size 4 GB. The physical (main) memory size is given as128 MB. The page size is 1 KB.

a. What is the virtual memory address structure in terms of its components and sizes (in bits)? Give a figure for the structure.

b. What is the structure of one row of the page table? Give it in terms of its subfield names and sizes in bits. Consider both D: dirty and V: bit. What is the size of one row in number of bits. Give a figure for the structure.

c. Now consider a 2-way (2-entry) TLB structure. Draw the structure of the TLB. Give it in terms of its subfield names and sizes in bits. Consider both D: dirty and V: bit. What is its total size? Assume that LRU is used for replacement. Use the minimum number of U bits.

d. Now consider a 4-way TLB structure. Draw the structure of the TLB. Give it in terms of its subfield names and sizes in bits. Consider both D: dirty and V: bit. What is the size of one row in number of bits. Draw it. Assume that LRU is used for replacement. Use two U bits for each entry of the TLB (we need 2 U bits since it is it is 4-way: we have to keep track of the utilization age of each of the 4 ways).

B. Consider a virtual memory environment of size 4KB with page size of 0.25 KB. Physical memory size is 2KB. (This part is independent of question 2.A.)

a. Consider the following memory accesses from left to right. Show the final content of the memory page table including the V bit and D bit after performing "all" memory accesses. For unknown entries assume 0 values.

Memory Access No.	1	2	3	4	5	6	7	8
Virtual Memory Address	0B4	0F0	2A0	2AC	4AC	0CC	244	B00
Physical Memory Address	2B4	2F0	4A0	4AC	0AC	2CC	444	700
Instruction Executed	sw	lw	lw	sw	lw	lw	sw	lw

b. Consider a TLB structure with two entries and with LRU replacement policy. Draw the TLB include D and U bits. Show the size of each component in number of bits. What is total size in terms of number of bits?

Show TLB contents in hexadecimal after "each" memory access. Indicate if a memory access produces a hit or miss for the TLB contents. State the type of each miss.

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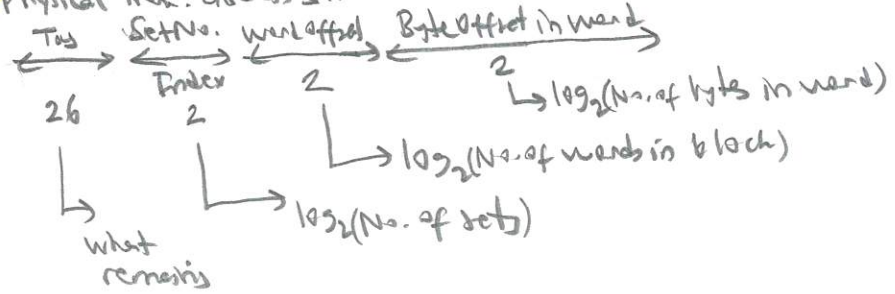
1. Cache Memory

MIPS: Byte addressable
Word: 4 bytes
Main Mem Size = 4GB → $2^2 \times 2^{30} = 2^{32}$

1.A. Cache Mem.

N = 1, Block Size: 4 words
No. of sets = 4

a. Physical mem. address structure



b. Cache Memory Block Structure

Block size = 1+1+26+128 = 156 bits ← (= set size)
SRAM size = 4 × 156 = 624 bits (Cache mem + overhead)
Cache Mem Total Data Field Size = No. of sets × N × Block Size (in byte)
4 × 1 × (4×4) = 64 bytes

c. Cache Mem Content (Set No)

M1: 0001 0000 1111 — Comp. Miss (Compulsory miss)
M2: 0000 10 11 1111 (sw) — Comp. Miss D=1
M3: 0000 1111 0000 — Comp. Miss
M4: 0000 0101 1100 — Comp. Miss
M5*: 0001 0000 1100 — Hit (Tag = Tag of M1)
M6: 0000 1111 1100 (sw) — Hit (Tag = Tag of M3)
M7: 0001 1111 1100 (sw) — Capacity Miss

Set No: underlined

Set

M2:

M3:

M4:

M7:

M6:

M5:

Cache Mem. Final Contents

V	D	Tag	Data	SetNo
1	1	0001	11 M7	11
1	1	0000	10 M2	10
1	0	0000	01 M4	01
1	0	0001	00 M1/M5	00

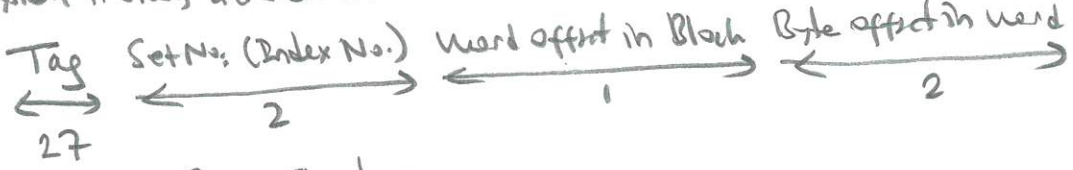
Tag is 32 bits, but only the relevant part is shown.

Hit/Miss Summary
First 4: Compulsory Miss
M5, M6: Hit
M7: Capacity Miss
Hit Rate: 2/7

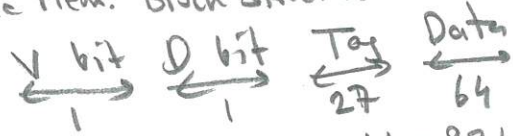
1-B Cache Mem. (cont.)

N=2, Block size: 2 words, No. of Sets: 4 Block Replacement: LRU

a. Physical memory address structure



b. Cache Mem. Block Structure



Block size: 1+1+27+64 = 93 bits

Set Size: 2 × Block size: 2×93 = 186 bits

SRAM Size: 4 × Set Size: 4×186 = 744 bits

↳ But we have one more detail: U bits for each set

4 sets × 1 U bit size = 4 bits

∴ Total SRAM size: 748 bits

Note: (No. of U bits for a set) = $\log_2 N$ ← General rule for U bits/set

c. Cache Memory Contents as we access memory

U bit: shows most recently accessed block in a set.

M1: 0001 0000 1111 Comp. Miss

M2: 0000 1010 1111 Comp. Miss

M3: 0000 1111 0000 Comp. Miss

M4: 0000 0101 1100 Comp. Miss

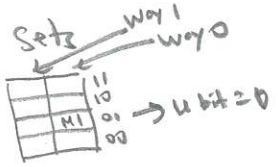
M5: 0001 0000 1100 Conflict Miss

M6: 0000 1111 1100 Comp. Miss

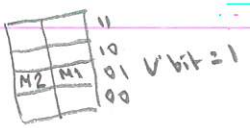
M7: 0001 1111 1100 Conflict Miss

Hit Rate = 0 All misses

M1:

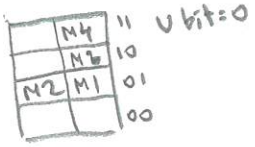


M2:



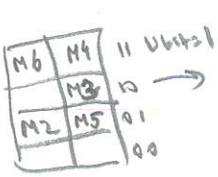
M3:

M4:

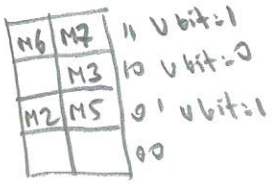


M5:

M6:



M7:

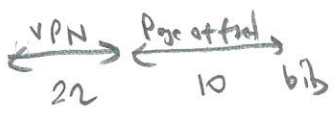


U bit: shows most recently accessed block

2. Virtual Memory

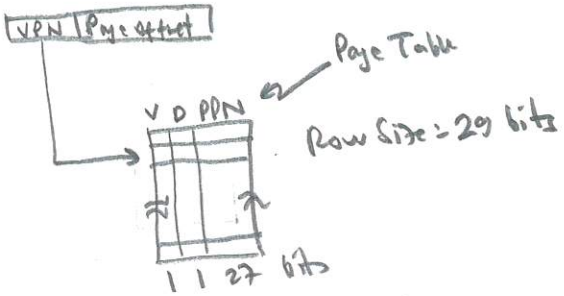
2.A. Virtual Mem Size = 4GB, 2^{32} Main Mem Size = 128 MB 2^{27} Page Size: 1K 2^{10}

a. VM add. structure

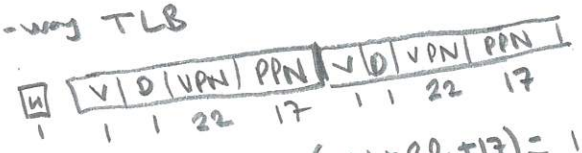


PM add. structure

b.



c. 2-way TLB



TLB Size = $1 + 2 \times (1+1+22+17) = 1 + 2 \times 41 = 83$ bits

d. 4-way TLB

U = 2 bits for each way

$4 \times (2+1+1+22+17) = 4 \times 43 = 172$ bits

We have to keep track of the life of each entry

Answer for this → Why U = 2 bits?

2.B VM Size = 4KB $\rightarrow 2^{12}$, PM Size = 2KB $\rightarrow 2^{11}$

Page Size = 0.25 KB $\rightarrow \frac{1}{4} \times 2^{10} = 2^8$

No. of VM pages $= \frac{2^{12}}{2^8} = 2^4$

No. of PM pages $= \frac{2^{11}}{2^8} = 2^3$

No	VM Address	PM Address	
1	0B4	2B4	SW
2	0F0	2F0	
3	2A0	4A0	
4	2AC	1AC	SW
5	1AC	0AC	
6	0CC	2CC	
7	244	144	SW
8	B00	700	

No. of VM pages $= 2^4 = 16$

	V	D	PPN
1111			
1110			
1101			
1100			
1011	1	0	111
1010			
1001			
1000			
0111			
0110			
0101			
0100	1	0	000
0011			
0010	1	1	100
0001			
0000	1	1	010

TLB Content Progress as we access memory

VPN & PPN are shown in decimal

①

No.	Way 1 V	D	VPN	PPN	Way 0 V	D	VPN	PPN	U	
					0	0	0	0	X	→ Initial condition
X	0	0	0	0	1	1	0	2	0	→ 1st compulsory miss, 2nd hit
1,2	0	0	0	0	1	1	0	2	1	→ 3rd compulsory miss, 4th hit
3,4	1	1	2	4	1	0	4	0	0	→ 5th conflict miss
5	1	1	2	4	1	0	4	0	1	→ 6th conflict miss
6	1	0	0	2	1	1	2	4	0	→ 7th compulsory miss
7	1	0	0	2	1	1	2	4	1	→ 8th compulsory miss
8	1	0	11/B	7						

* U: shows the last way/unit used.

Hit Rate = 2/8

CS224
FALL 2024
QUIZ NO. 4 Sec. 1 & 2

Student Name/Section:

Student Name/Section:

Solutions

Date: Dec 17, '24

PLEASE READ - Notes. 1. If you forget to sign below or forget to provide any of the above information 30 points will be taken off. 2. You have to give the answers in full detail you cannot leave them as expressions to be completed. 3. After reading these notes both students must sign here: _____

RULES: Two students work together. You can only use your notes, textbook, slides, and greencard.

1. A computer has a cache of 64KB with a block size of 64 Bytes. Assume that the main memory of size 256MB. Words are 32 bits and byte-addressable.

a. If the cache is direct mapped, what is the (physical) address format used to access this cache? Briefly explain.

Main memory 256 MB → 2^{28}

word 32 bits → 4 bytes

Block size 64 Bytes → No. of words/block = Block size/word size = 64/4 = 16 words/Block

No. of sets = (Cache size)/(N × Block size)

N = 1 direct mapped

No. of sets = 64KB/64 bytes = 2^{10}

Tag	Index (Set No)	word off. in Block/Byte	offset in word
12	10	4	2

⇒ 12/10/4/2

2, 4, 8, 16, 32, 64, 128, 256

b. If the cache is 4-way associative, what is the address format? Briefly explain.

4 way associative ⇒ No. of sets = (No of sets with N=1)/4

⇒ No. of sets = 8

Tag	Set	WOB	BOW
14	8	4	2

WOB: word offset in Block

BOW: Byte offset in word

c. If the cache is fully associative, what is the address format? Briefly explain. What is the SRAM size in number of bits?

No. of sets = 1 No need to indicate set no.

Tag	WOB	BOW
22	4	2

SRAM Size

No LRU is assumed (no u bit)

No D bit is assumed

Each block: V / Tag / Data ← each block 64 bytes

1 / 22 / 64×8 = 512

No. of block 2^{10} = 1024

$2^{10} \times (1 + 22 + 512)$

535 bits = 547,840 bits

1024 × 535 = 5120 + 30720 + 51200 = 547840

2. Consider the following address structure. ← BWO = 2

tag: 12 bits, set no. (index): 2 bit, word block offset: 2 bit. The words are 4 bytes in length.

a. What is the physical memory size in KB?

Tag / Set / WBO / BWO
12 2 2 2 → 18 bits

$\Rightarrow 2^8 \times 2^{10} = 256$ KB

b. What is the cache data area size in bytes (N= 2, 2-way associative)?

Cache data area size = No. of Sets × N × Block Size

$\Rightarrow 2^2 \times 2^1 \times (2^2 \times 2^2)$

$2^7 = 128$ bytes

↑ No. of words
WBO = 2
There are 4 words/block

3. For the memory structure given in question 2 assume that N= 1. Consider the following consecutive memory accesses

0x10, 0x18, 0x08, 0x0C0, x50, 0x5C

(0x10 means 0x0..10, the same applies to the other addresses). Show the change in the cache memory and indicate the type of miss (if any) for each memory access. Assume LRU for cache replacement, if needed. Calculate the hit rate.

N=1 Direct-access cache memory

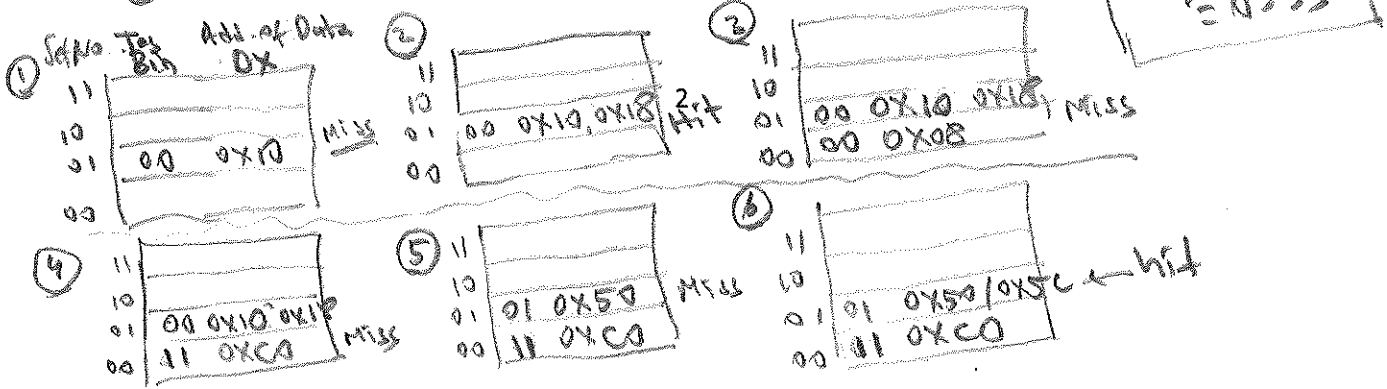
Tag / Set / WBO / BWO
12 2 2 2

No. of bits for set no: 2
There are 4 sets

With N=1 LRU is not needed!

		Tag	Set		
①	0X10 →	0001	0000	→ Tag=00	Set:01
②	0X18 →	0001	1000	→ Tag:00	Set:01
③	0X08 →	0001	1000	→ Tag:00	Set:10
④	0XC0 →	1100	0000	→ Tag:11	Set:00
⑤	0X50 →	0101	0000	→ Tag:01	Set:00
⑥	0X5C →	0101	1100	→ Tag:01	Set:11

Hit rate
2/6 = 1/3
≈ 0.33



CS224
SPRING 2024
QUIZ NO. 4

Student Name/Section: 5 & 6 Solutions

Student Name/Section:

Date: May 2, '24

PLEASE READ - Notes. 1. If you forget to sign below or forget to provide any of the above information 30 points will be taken off. 2. You have to give the answers in full detail you cannot leave them as expressions to be completed. 3. After reading these notes both students must sign here: _____

1. A computer has a cache of 32KB with a block size of 32 Bytes. Assume that the main memory of size 128MB. Words are 32 bits and byte-addressable.

a. If the cache is direct mapped, what is the (physical) address format used to access this cache? Briefly explain.

No. of blocks = Cache Size / Block Size = 32 KB / 32 bytes = $(2^5 \times 2^{10}) / 2^5 = 2^{10}$

128 MB = $2^7 \times 2^{20}$ → Phys. mem. addr size = 27 bits

Words 32 bits = 4 bytes → 2 bits byte offset

No. of words/block = Block Size / word size = 32 bytes / 4 bytes = $2^5/2^2 = 8$

Tag / Set No / word Block offset / Byte offset

12 10 3 2

Tag	Set No	WBO	BO
12	10	3	2

← No. of bits

↑ No. of blocks: 0, 2, 4, 8, 16, 32, 64, 128

↑ No. of sets

Word off.

b. If the cache is 4-way associative, what is the address format? Briefly explain.

4-way associative No. of sets $2^{10}/2^2 = 2^8$

Tag	Set No.	WBO	BO
14	8	3	2

← No. of bits

WBO: Word Block off.

BO: Byte off.

c. If the cache is fully associative, what is the address format? Briefly explain. What is the SRAM size?

Fully association: No need for set No. ⇒

Tag	WBO	BO
22	3	2

← No. of bits

Block Structure: V / Tag / Data

1 22 32×8 ← bits

279 bits

32 × 8 = 256, 23, 279

SRAM Size = No. of block × Block Size = $2^{10} \times 279$

If we include D bit Block Structure: D / V / Tag / Data

⇒ $2^{10} \times 280$ No. of V bits/block

LRU ⇒ (If we want to implement LRU each block must have [Tag (No. of Blocks)] no. of bits per block

LRU blocks V / V / Tag / Data ⇒ 10 / 1 / 22 / 32×8 ⇒ $2^{10} \times 289$ bits

each location we address contains a byte (8 bits)

2. Consider the following address structure (note that at each memory address one byte is stored, i.e. it is a byte addressable system).

(WBO) (BO)

tag: 12 bits, set no. (index): 1 bit, word block offset: 1 bit, byte offset: 2 bits.

a. What is the physical memory size in KB?

Tag / Set No / WBO / BO
12 1 1 2 → 16 bits $2^{16} = 2^6 \times 2^{10} = 64$ KB

77
x 4
308

64 KB

b. What is the cache memory size in bytes (N= 2, 2-way associative)?

N=2

Block structure
← Good enough as an answer

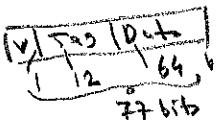
4 x 8 = 32 bytes

WBO = 1 bit ← 2 words/block
BO = 2 bits ← 4 bytes/word
→ Each block is 8 bytes

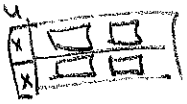
If we also consider SRAM size
Assume LRU

If we consider SRAM size

Tag / Set No / WBO / BO ⇒ Block Structure
12 1 1 2



SRAM Str.



SRAM Size

4
2 + 4 x 77 = 310 bits

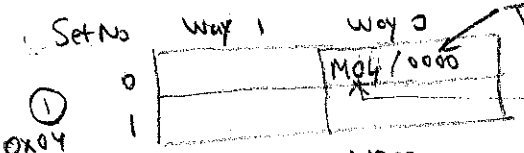
If random replacement
308 bits

c. For N= 2 consider the following consecutive memory accesses 4, 24, 60, 4, 44, 72 (all decimal numbers). Show the change in the cache memory and indicate the type of miss (if any) for each memory access. Assume LRU for cache replacement. Indicate conflict types.

In bin.

① 4 → 0X04 : 0000 0100
② 24 → 0X18 : 0001 1000
③ 60 → 0X3C : 0011 1100
④ 4 → 0X04 : 0000 0100
⑤ 44 → 0X2C : 0010 1100
⑥ 72 → 0X48 : 0100 1000

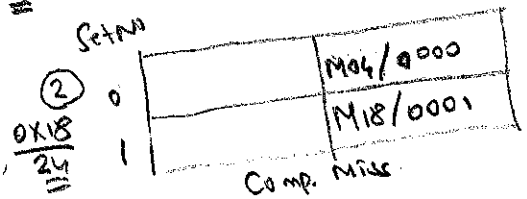
① 0X04 = 4



Mem. add. in hex.

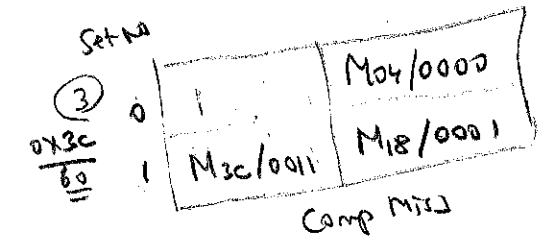
Comp. Miss

② 0X18 = 24



Comp. Miss

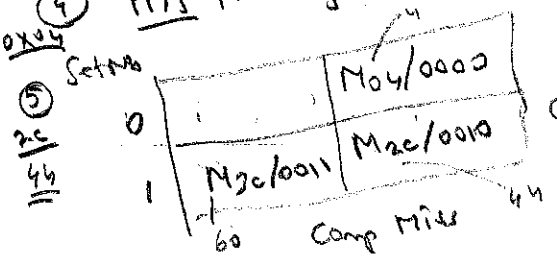
③ 0X3C = 60



Comp Miss

④ 0X04 Hit No change in cache mem.

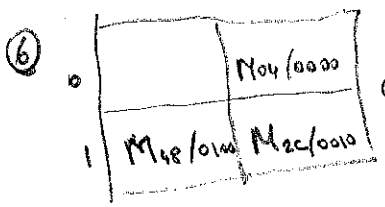
⑤ 2c = 44



Comp Miss

Comp Miss

⑥



Comp. Miss

Continued

2. Consider the following address structure:

tag: 20 bits, set no. (index): 1 bit, block offset: 1 bit, byte offset: 2 bits.

a. What is the physical memory size in MB?

Total no. of bits: $20+1+1+2 = 2^{24}$ ← No. of bits in phys. mem address

$2^{24} \rightarrow 2^4 \times 2^{20} \rightarrow$ 16 MB

b. What is the cache memory (SRAM) size in bits for (N= 4, (4-way associative)? Note that for eviction Random replacement is used.

no bit is needed

Block offset 1 bit → 2 words/block
Byte offset 2 bits → 4 bytes/word

Data: Each block is 2 words
each word is 4 bytes
⇒ $2 \times 4 \times 8 = 64$

set no { 1, 0 } ← In each set we have 4 blocks (N=4)

Block Structure

V	Tag	Block
1	20	64

SRAM Size = No. of sets × N × Block size
$= 2 \times 4 \times 85 =$ 680 bits ← corrected

c. Assume that for N> 1 we want to use FIFO (First In First Out) policy for cache memory replacement. How can you implement FIFO? Define a suitable data structure for its implementation. How many bits are required for its implementation for different values of N? Obhtain a general formula for the data structure size in number of bits.

FIFO : Queu

Pointer → 00, 01, 10, 11

First entry to point is: 0
After entering an entry pointer is updated
Pointer = mod (Pointer+1, 3) Entries are always
replaced in the same order Fill: 0,1,2,3, Evict: 0,1,2,3

No. of bits needed $\log_2 N$ assuming that N is multiple of 2.

d. Consider the following consecutive memory accesses for time t= 0, 1, 2 ns: 44, 74, 12, 54 (all decimal numbers). Show the change in the cache memory and indicate the type of miss (if any) for each memory access. Use FIFO if needed. Assume that N= 2.

Bin.
44 = 0x2C → 0010 1100 → Goes to set no.1
74 = 0x4A → 0100 1010 → set no.0
12 = 0x0C → 0000 1100 → set no.1
54 = 0x36 → 0011 0110 → set no.0
Tag ↑ Set No.

They all have different tags

M_{44} = contents of location at address 44 is

Set No	Initial cont.	t=0	t=1	t=2	t=3
1			M_{44}	M_{12}	M_{12}
0	All empty	M_{44}	M_{74}	M_{74}	M_{54}

All memory accesses cause compulsory miss.

⇒ 4 comp. misses

CS224
Fall 2020
QUIZ NO. 5

December 23, 2020

Solution comes later look below

PLEASE READ: 1. Only handwritten answers are accepted. 2. Convert your handwritten answers to pdf and upload one pdf file to Moodle. Make sure that you answer the questions in the order they are given. Provide a neat work and make sure that your answers are numbered and in the order of questions and distinguishable from each other. Do not miss the deadline.

1. Cache Memory

Consider a processor with an architecture similar to MIPS: byte addressable, words are 4 bytes, main memory size is 4 GB.

For the sections A and B below consider the following memory accesses with the given memory addresses. The table shows that for a word that contains a value represented with M1 is at memory location 0X10F and it is accessed for a lw instruction.

Memory Content	Used For instruction	Memory Address in Hex	Memory Address in Binary
M1	lw	10F	0001 0000 1111
M2	sw	0AF	0000 1010 1111
M3	lw	0F0	0000 1111 0000
M4	lw	05C	0000 0101 1100
M5	lw	10C	0001 0000 1100
M6	sw	0FC	0000 1111 1100
M7	sw	1FC	0001 1111 1100

A. Consider the following cache memory configuration for the above memory accesses. N= 1 (direct mapped cache), block size is 4 words, number of sets is 4.

a. Give the physical (main) memory address structure as it will be used to access the cache memory. Draw a simple figure and indicate the name and size of each subfield in terms of number of bits.

b. Draw the structure of a block in terms of its components: V (valid bit), D[1] (dirty bit), Tag, Data. Indicate the size of each field.
What is the total block size in bits?
What is the SRAM size in bits?
What is the cache memory total data field size in bytes?

c. Show the final contents of the cache memory in a figure in terms of its subfield after accessing memory locations in the order given above. Give the values of tag etc. in bits, show block data contents in terms of M1, M2 etc.

d. For each memory access indicate if it is a hit or miss. Give the miss type for each case. What is the hit rate?

[1] D bit indicates if the block content is modified during execution time and if it so when that block is emptied due to a conflict its content is written back to physical memory.

B. Consider the above memory access sequence with the following cache memory structure: N= 2 (2-way associative cache), block size is 2 words, number of sets is 4. For block replacement LRU is used. To support the LRU policy the U bit is used as illustrated in the textbook (slides). In your answer include the U bit when needed. Answer all sub questions of the question A given above, so in your answers you will have the sub questions B.a, ..., B.d.

2. Virtual Memory

A. Consider a virtual memory structure of size 4 GB. The physical (main) memory size is given as128 MB. The page size is 1 KB.

a. What is the virtual memory address structure in terms of its components and sizes (in bits)? Give a figure for the structure.

b. What is the structure of one row of the page table? Give it in terms of its subfield names and sizes in bits. Consider both D: dirty and V: bit. What is the size of one row in number of bits. Give a figure for the structure.

c. Now consider a 2-way (2-entry) TLB structure. Draw the structure of the TLB. Give it in terms of its subfield names and sizes in bits. Consider both D: dirty and V: bit. What is its total size? Assume that LRU is used for replacement. Use the minimum number of U bits.

d. Now consider a 4-way TLB structure. Draw the structure of the TLB. Give it in terms of its subfield names and sizes in bits. Consider both D: dirty and V: bit. What is the size of one row in number of bits. Draw it. Assume that LRU is used for replacement. Use two U bits for each entry of the TLB (we need 2 U bits since it is it is 4-way: we have to keep track of the utilization age of each of the 4 ways).

B. Consider a virtual memory environment of size 4KB with page size of 0.25 KB. Physical memory size is 2KB. (This part is independent of question 2.A.)

a. Consider the following memory accesses from left to right. Show the final content of the memory page table including the V bit and D bit after performing "all" memory accesses. For unknown entries assume 0 values.

Memory Access No.	1	2	3	4	5	6	7	8
Virtual Memory Address	0B4	0F0	2A0	2AC	4AC	0CC	244	B00
Physical Memory Address	2B4	2F0	4A0	4AC	0AC	2CC	444	700
Instruction Executed	sw	lw	lw	sw	lw	lw	sw	lw

b. Consider a TLB structure with two entries and with LRU replacement policy. Draw the TLB include D and U bits. Show the size of each component in number of bits. What is total size in terms of number of bits?

Show TLB contents in hexadecimal after "each" memory access. Indicate if a memory access produces a hit or miss for the TLB contents. State the type of each miss.

Some information about miss types:

Compulsory Miss: First access to data with a unique tag number.

Conflict Miss: Access to recently used data with the same tag; however, data is evicted and not in the cache anymore.

Capacity Miss: A special type of conflict miss, occurs when the data is recently used, but not in the cache anymore and all the cache is completely full. (not only the set for accessed block, when all the data on all the sets is full)

CS224
Fall 2020
Quiz No.5
Dec. 26'20

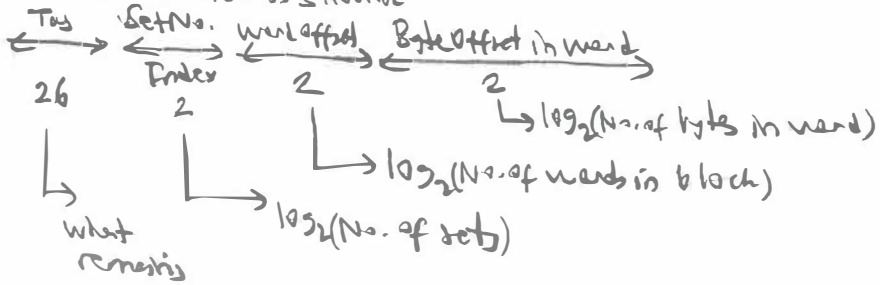
1. Cache Memory

MIPS: Byte addressable
Word = 4 bytes
Main Mem Size = 4GB $\rightarrow 2^2 \times 2^{30} = 2^{32}$

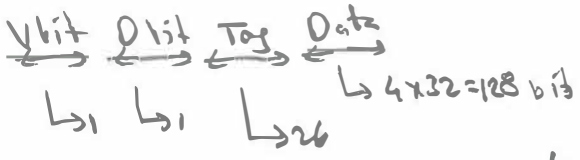
1.A. Cache Mem.

N=1, Block size = 4 words
No. of sets = 4

a. Physical mem. address structure



b. Cache Memory Block Structure



Block size = 1+1+26+128 = 156 bits ← (= set size)

SRAM size = 4 x 156 = 624 bits (Cache mem + overhead)

Cache Mem Total Data Field Size = No. of sets x N x Block Size (in byte)

4 x 1 x (4 x 4) = 64 bytes

c. Cache Mem Content (Set No)

M1: 0001 0000 1111 — Comp. Miss (Compulsory miss)
M2: 0000 1000 1111 (sw) — Comp. Miss D=1
M3: 0000 1111 0000 — Comp. Miss
M4: 0000 0101 1100 — Comp. Miss
M5*: 0001 0000 1100 — Hit (Tag = Tag of M1)
M6: 0000 1111 1100 (sw) — Hit (Tag = Tag of M3)
M7: 0001 1111 1100 (sw) — Comp. miss

Set No: underlined

M1: Set 11 / 10 / 01 / 00 → M1
M2: 11 → M2 / 10 → M1 / 01 / 00
M3: 11 → M3 / 10 → M2 / 01 → M1 / 00
M4: 11 → M3 / 10 → M2 / 01 → M4 / 00 → M1
M5: 11 → M3 / 10 → M2 / 01 → M4 / 00 → M1 M5
M6: 11 → M3 M6 / 10 → M2 / 01 → M4 / 00 → M1 M5
M7: 11 → M7 / 10 → M2 / 01 → M4 / 00 → M1 M5

Cache Mem. Final Content

V	D	Tag	Data	Set No
1	1	0001	11	M7 — 11
1	1	0000	10	M2 — 10
1	0	0000	01	M4 — 01
1	0	0001	00	M1/M5 — 00

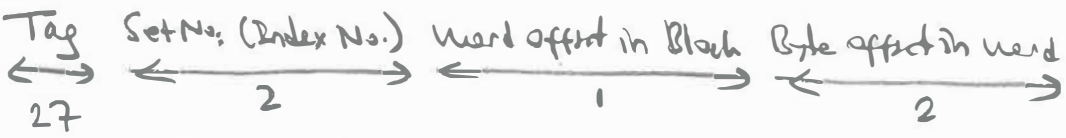
Tag is 32 bits, but only the relevant part is shown

Hit/Miss Summary
First 4: Compulsory Miss
M5, M6: Hit
M7: Comp. miss
Hit rate: 2/7

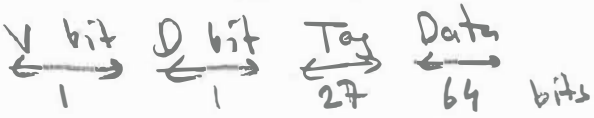
1-B Cache Mem. (cont.)

N=2, Block Size: 2 words, No. of Sets: 4 Block Replacement: LRU

a. Physical memory address structure



b. Cache Mem. Block Structure



Block size: 1+1+27+64 = 93 bits

Set Size: 2 x Block size: 2x93 = 186 bits

SRAM Size: 4 x Set Size: 4x186 = 744 bits

↳ But we have one more detail: U bits for each set

4 sets x 1 U bit size = 4 bits

∴ Total SRAM size: 748 bits

Note: (No. of U bits for a set) = $\log_2 N$ ← General rule for U bits/set

c. Cache Memory Contents as we access memory

M1: 0001 0000 1111 Comp. Miss

M2: 0000 1010 1111 Comp. Miss

M3: 0000 1111 0000 Comp. Miss

M4: 0000 0101 1100 Comp. Miss

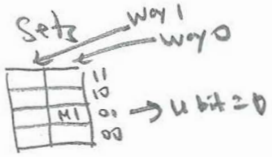
M5: 0001 0000 1100 Hit (same data with M1)

M6: 0000 1111 1100 Comp. Miss

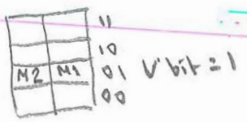
M7: 0001 1111 1100 Comp. miss

U bit: shows most recently accessed block in a set.

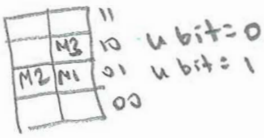
M1:



M2:



M3:

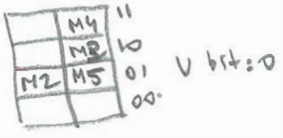


Hit rate = 1/7

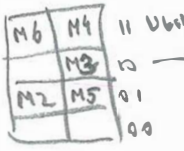
M4:

$M_1 = M_5$

M5:



M6:



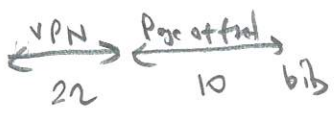
M7:

U bit: shows most recently accessed block

2. Virtual Memory

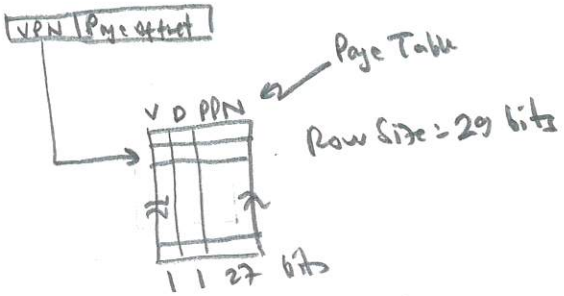
2.A. Virtual Mem Size = 4GB, 2^{32} Main Mem Size = 128 MB 2^{27} Page Size: 1K 2^{10}

a. VM add. structure

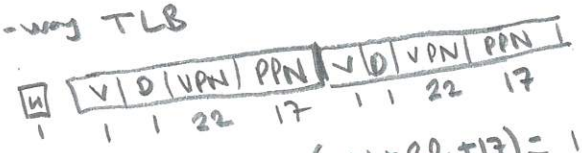


PM add. structure

b.



c. 2-way TLB



TLB Size = $1 + 2 \times (1+1+22+17) = 1 + 2 \times 41 = 83$ bits

d. 4-way TLB

U = 2 bits for each way

$4 \times (2+1+1+22+17) = 4 \times 43 = 172$ bits

We have to keep track of the life of each entry

Answer for this → Why U = 2 bits?

2.B VM Size = 4KB $\rightarrow 2^{12}$, PM Size = 2KB $\rightarrow 2^{11}$

Page Size = 0.25 KB $\rightarrow \frac{1}{4} \times 2^{10} = 2^8$

No. of VM pages $= \frac{2^{12}}{2^8} = 2^4$

No. of PM pages $= \frac{2^{11}}{2^8} = 2^3$

No	VM Address	PM Address	
1	0B4	2B4	SW
2	0F0	2F0	
3	2A0	4A0	
4	2AC	1AC	SW
5	1AC	0AC	
6	0CC	2CC	
7	244	144	SW
8	B00	700	

No. of VM pages $= 2^4 = 16$

	V	D	PPN
1111			
1110			
1101			
1100			
1011	1	0	111
1010			
1001			
1000			
0111			
0110			
0101			
0100	1	0	000
0011			
0010	1	1	100
0001			
0000	1	1	010

TLB Content Progress as we access memory

VPN & PPN are shown in decimal

①

No.	Way 1 V	D	VPN	PPN	Way 0 V	D	VPN	PPN	U	
					0	0	0	0	X	→ Initial condition
X	0	0	0	0	1	1	0	2	0	→ 1st compulsory miss, 2nd hit
1,2	0	0	0	0	1	1	0	2	1	→ 3rd compulsory miss, 4th hit
3,4	1	1	2	4	1	0	4	0	0	→ 5th conflict miss
5	1	1	2	4	1	0	4	0	1	→ 6th conflict miss
6	1	0	0	2	1	1	2	4	0	→ 7th compulsory miss
7	1	0	0	2	1	1	2	4	1	→ 8th compulsory miss
8	1	0	11/B	7						

* U: shows the last way/unit used.

Hit Rate = 2/8