Experiment 5 Arithmetic Processor

1. Sequence assignment

$Op_2\ Op_1$	Arithmetic Function
0 0	
0 1	
1 0	
1 1	

2. Processor Design

Construct the truth table for the input processor. (Use a_i, b_i, 0, 1)

$Op_2\ Op_1$	x_i	y_i	c_0
00			
01			
10			
11			

Experiment 5 Arithmetic Processor

1. Sequence assignment

$Op_2\ Op_1$	Arithmetic Function
0 0	2B + 1
0 1	A - B
1 0	A + B
1 1	A - 1

2. Processor Design

Construct the truth table for the input processor. (Use a_i, b_i, 0, 1)

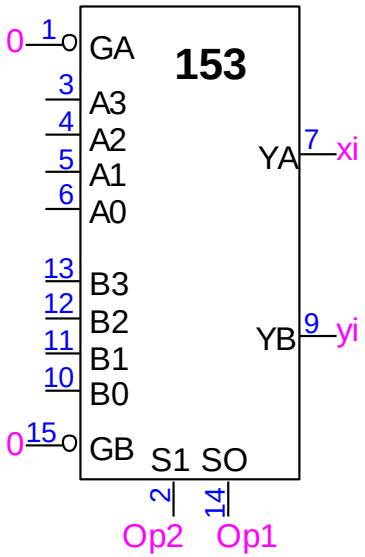
$Op_2\ Op_1$	x_i	y_i	c_0
00	b_i	b_i	1
01	a_i	b_i'	1
10	a_i	b_i	0
11	a_i	1	0

2. Processor Design

Construct the truth table for the input processor. (Use a_i, b_i, 0, 1)

Op_2 Op_1	x_i	y_i	c_0
00	b_i	b_i	1
01	a_i	b_i'	1
10	a_i	b_i	0
11	a_i	1	0

Label the data inputs of the two 4-to-1 multiplexers given below for the realization of x_i, y_i.



Express the initial carry c_0 as a function of Op_2 and Op_1.

c_0 =

2. Processor Design

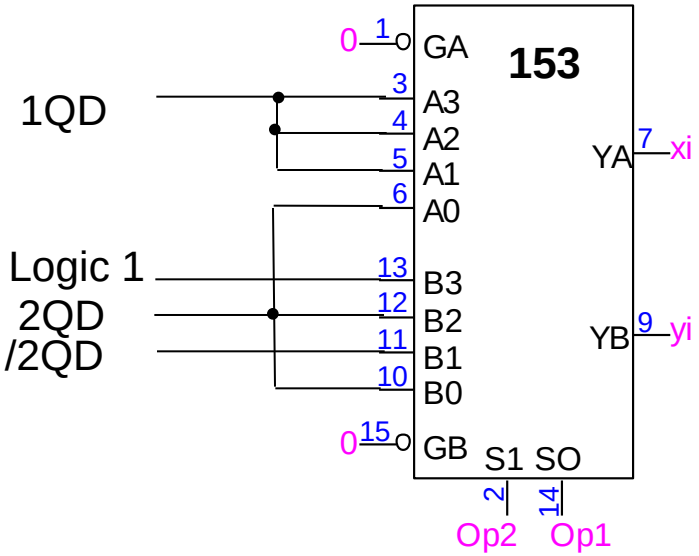
Construct the truth table for the input processor. (Use a_i, b_i, 0, 1)

Op_2 Op_1	x_i	y_i	c_0
00	b_i	b_i	1
01	a_i	b_i'	1
10	a_i	b_i	0
11	a_i	1	0

Label the data inputs of the two 4-to-1 multiplexers given below for the realization of x_i, y_i.

Use the following signal names for input processor 1QD for ai, 2QD for bi, Op2, Op1, xi, yi, zi

Use the following signal names for control signals 1s1, 1s0, 2s1, 2s0, c0, C2, C1



Express the initial carry c_0 as a function of Op_2 and Op_1.

$c_0 = Op_2'$

Construct the truth table for the control circuit.

State	START	$(s_1)_{R1}$	$(s_0)_{R1}$	$(s_1)_{R2}$	$(s_0)_{R2}$	C_2	C_1
T_0	0						
T_0	1						
T_1	d						
T_2	d						
T_3	d						
T_4	d						
T_5	d						

$(s_1)_{R1}$ =
$(s_0)_{R1}$ =
$(s_1)_{R2}$ =
$(s_0)_{R2}$ =
C_2 =
C_1 =

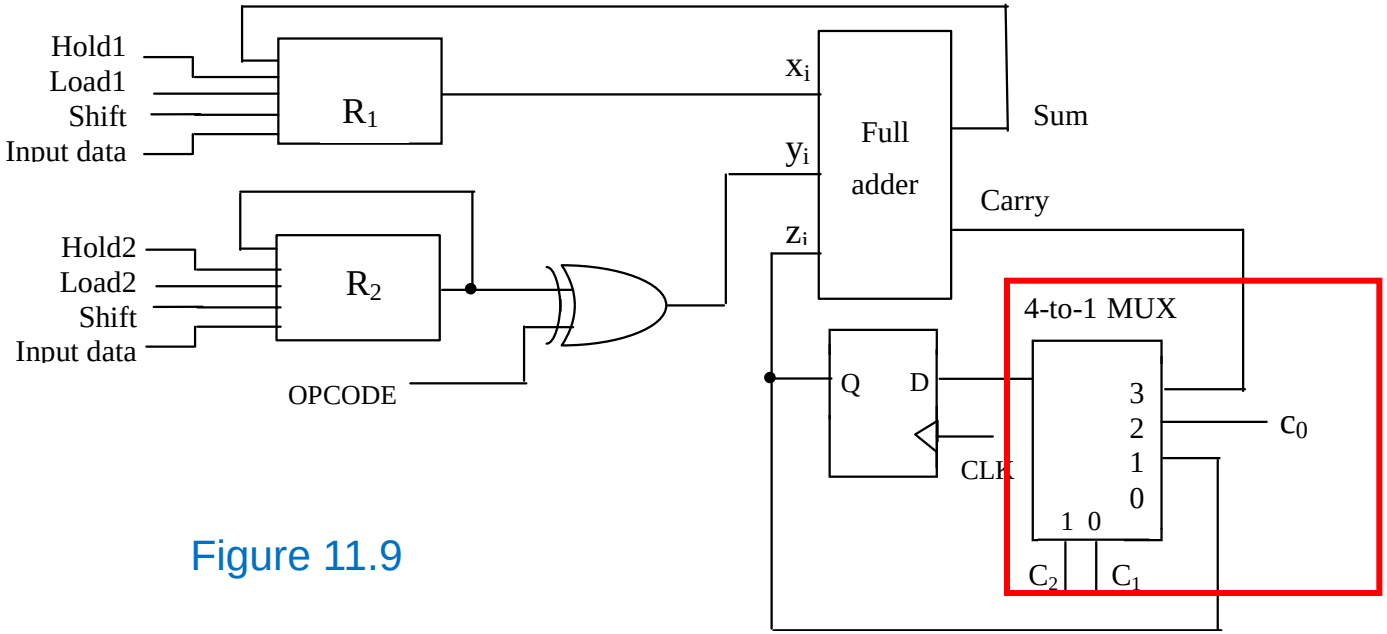
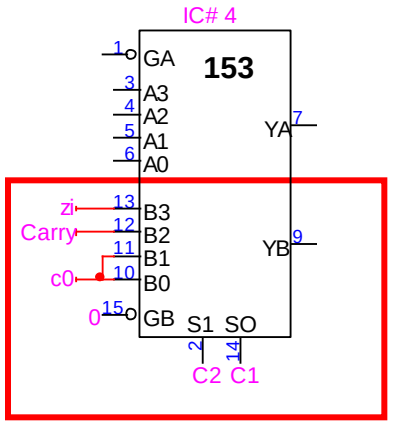


Figure 11.9

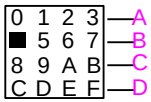
Note the difference in the data inputs of the two multiplexers.

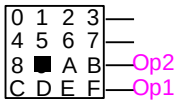
Lab 5 schematic diagram

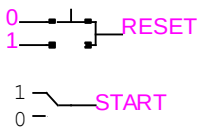


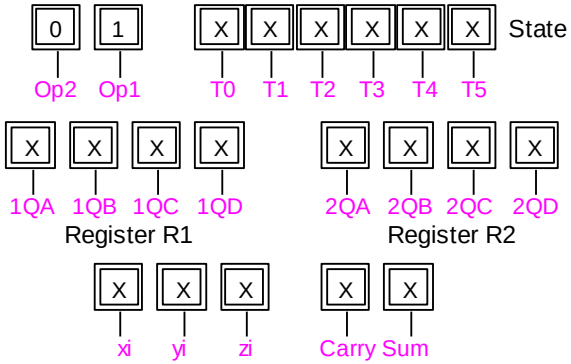
16.265 Logic Design
Experiment 5: Arithmetic Processor
Name:
Student Logic Number:
Function Set Number:

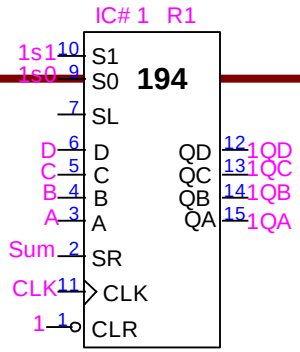
4-bit data
inpput
ABCD

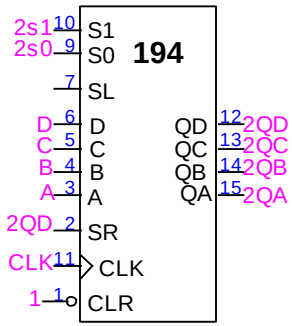


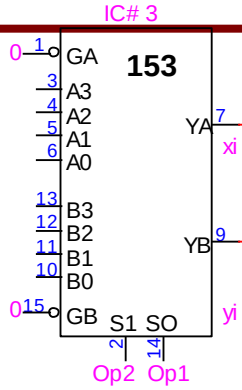


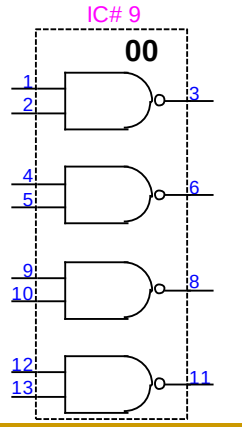


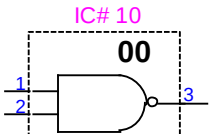


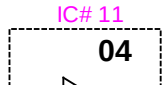


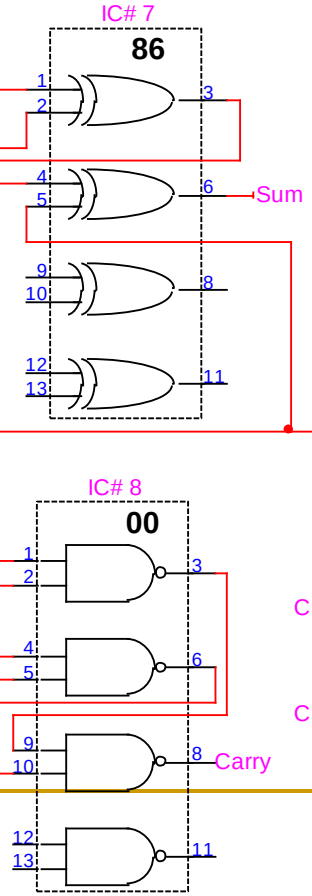


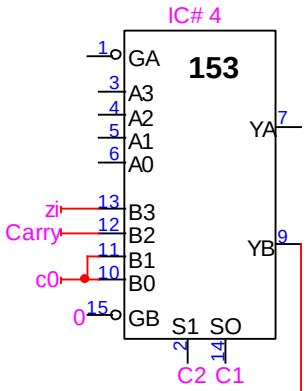


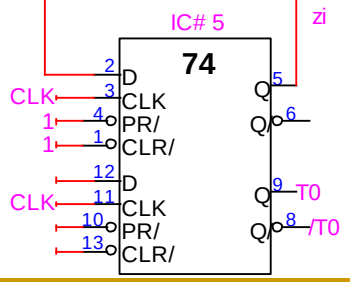








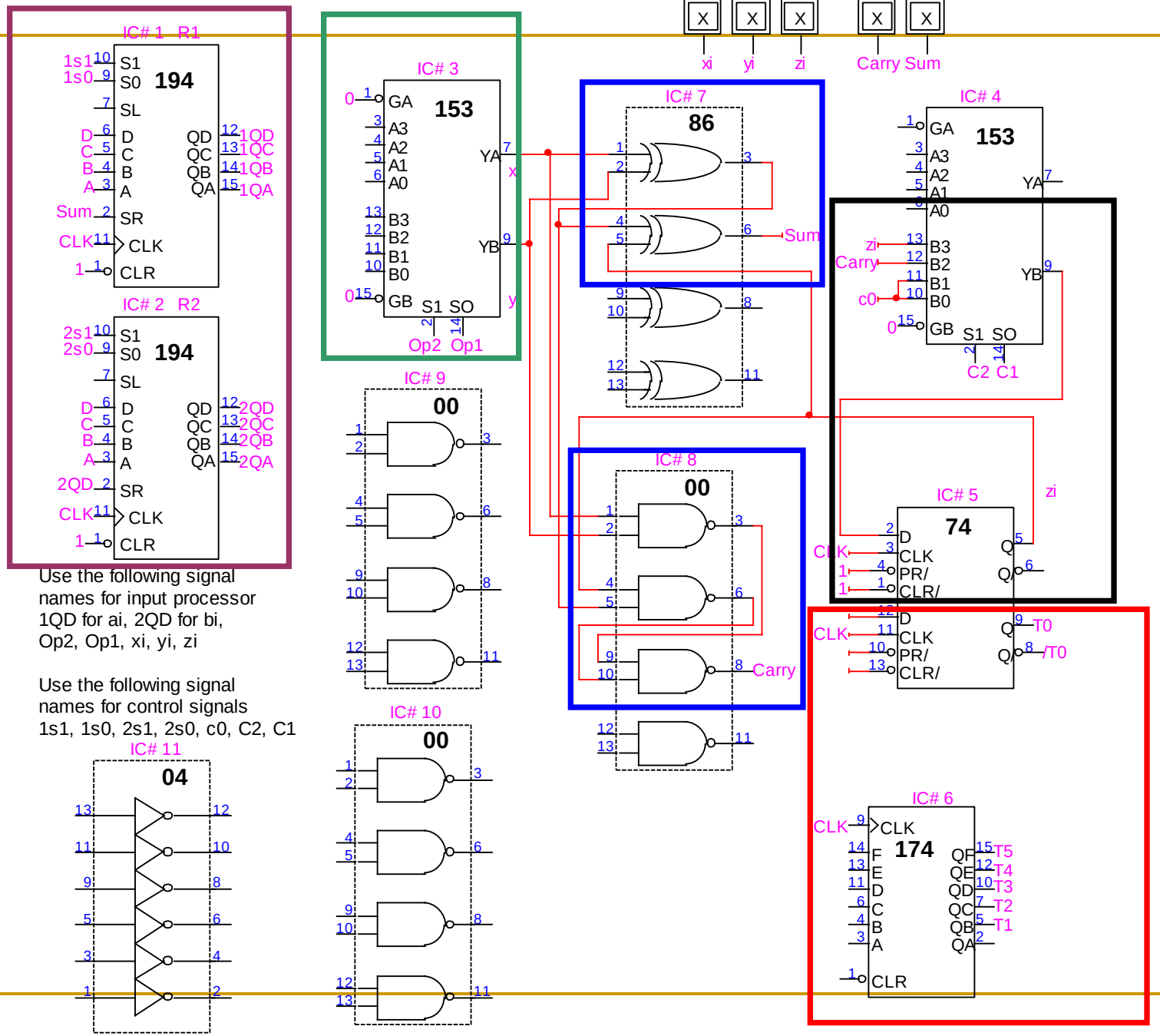




IC# 6

Use the following signal names for input processor 1QD for ai, 2QD for bi, Op2, Op1, xi, yi, zi

Use the following signal names for control signals 1s1, 1s0, 2s1, 2s0, c0, C2, C1


IC# 1 R1
194
1s1
1s0
Sum
CLK
1QD
1QC
1QB
1QA
IC# 2 R2
194
2s1
2s0
2QD
2QC
2QB
2QA
Use the following signal names for input processor 1QD for ai, 2QD for bi, Op2, Op1, xi, yi, zi
Use the following signal names for control signals 1s1, 1s0, 2s1, 2s0, c0, C2, C1
IC# 11
04
IC# 3
153
Op2
Op1
IC# 9
00
IC# 10
00
xi
yi
zi
Carry
Sum
IC# 7
86
IC# 8
00
IC# 4
153
C2
C1
IC# 5
74
IC# 6
174
T0
/T0
T1
T2
T3
T4
T5