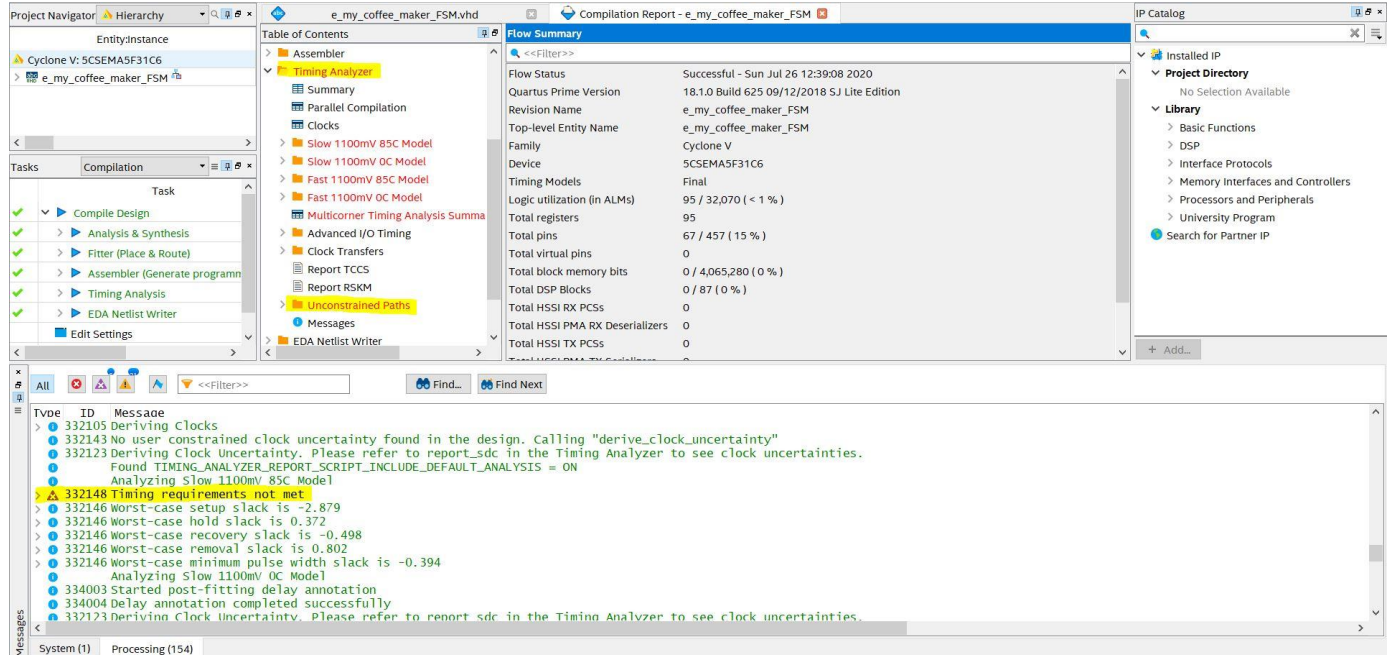
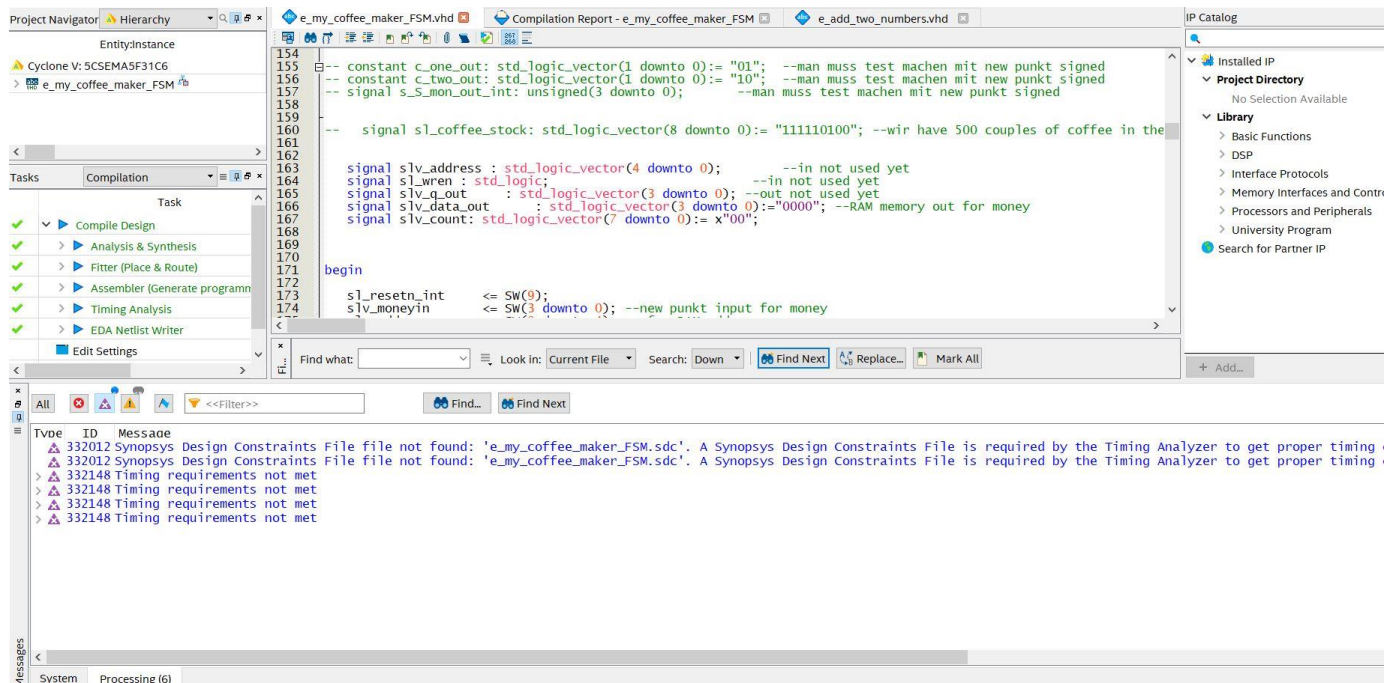


TimeQuest Analyzer Report

Time configuration parameters was created and saved as a file: *e_my_coffee_maker_FSM.sdc* (*C:\FPGA\Project\TimeQuest Analyzer Report\e_my_coffee_maker_FSM.sdc*). All steps were indicated in a screenshots bellow. In our case we have Maximum of negative slack is $-3,182\text{ ns}$. Worst case propagation delay could be found with a formula $\text{clock period} - \text{slack}$: $1\text{ ns} - (-3,182) = 4,182\text{ ns}$. From this we could find maximum frequency: $F_{\text{max}} = 1 / 4,182 = 239,12\text{ MHz}$.



Picture 1. Time requirements not met



Picture 2. Time requirements not met

Project Navigator: Entity/Instance
Cyclone V: 5CSEMA5F31C6
e_my_coffee_maker_FSM

Tasks: Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate program)
Timing Analysis
EDA Netlist Writer
Edit Settings

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Minimum Pulse Width Summary
Metastability Summary
Slow 1100mV OC Model
Fast 1100mV 85C Model
Fast 1100mV OC Model
Multicorner Timing Analysis Summa
Advanced I/O Timing
Clock Transfers

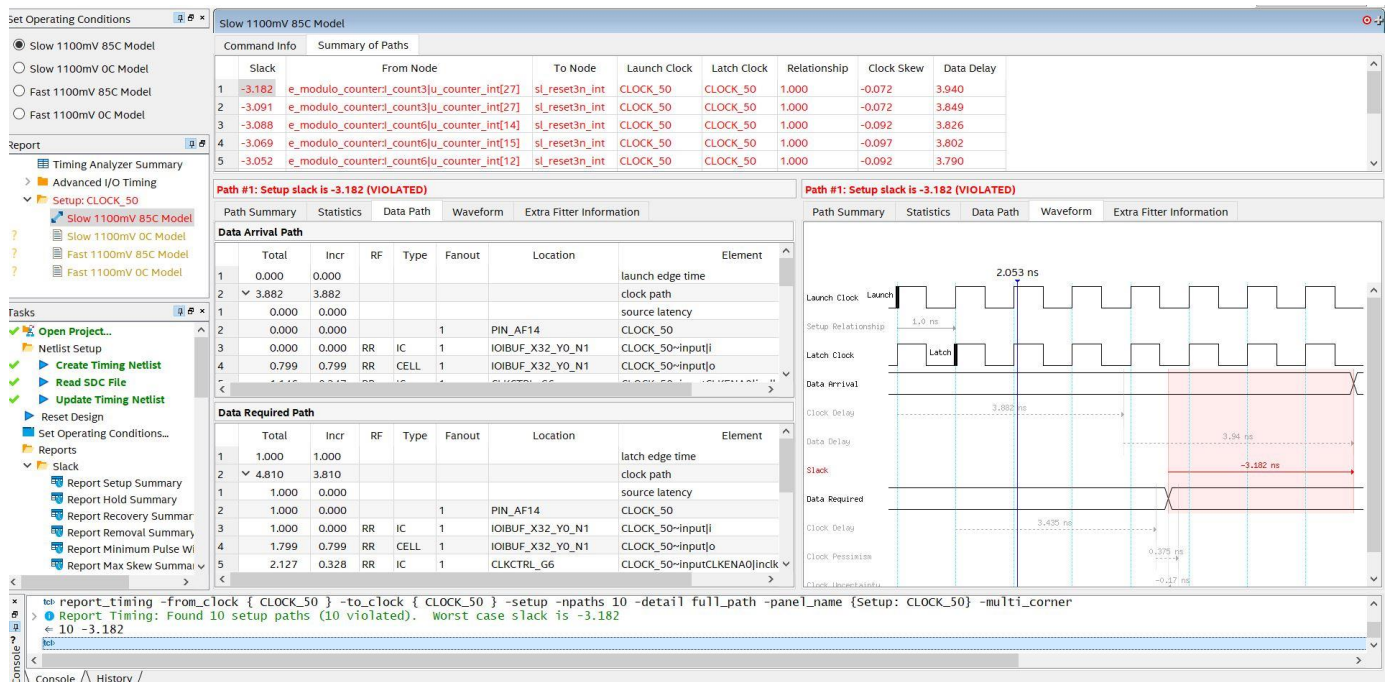
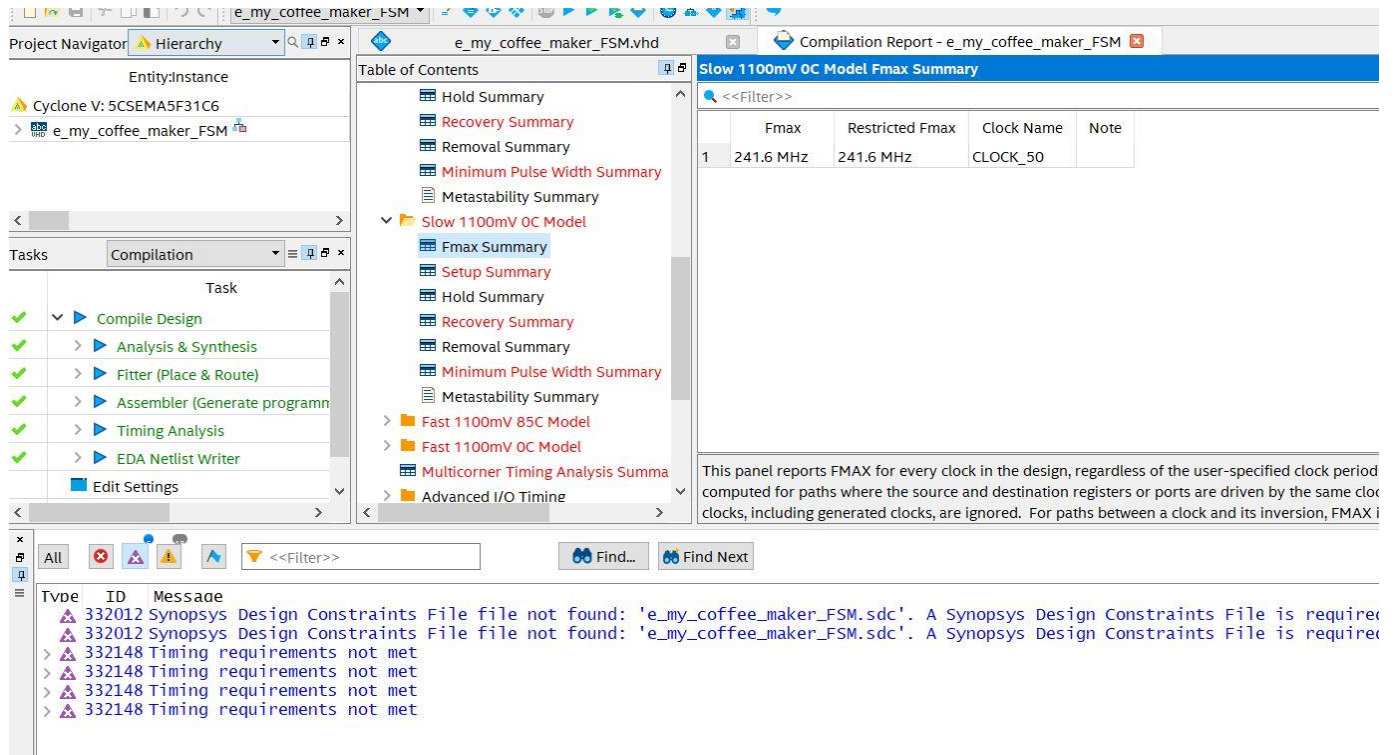
Slow 1100mV 85C Model Fmax Summary
Fmax Restricted Fmax Clock Name Note
1 239.12 MHz 239.12 MHz CLOCK_50

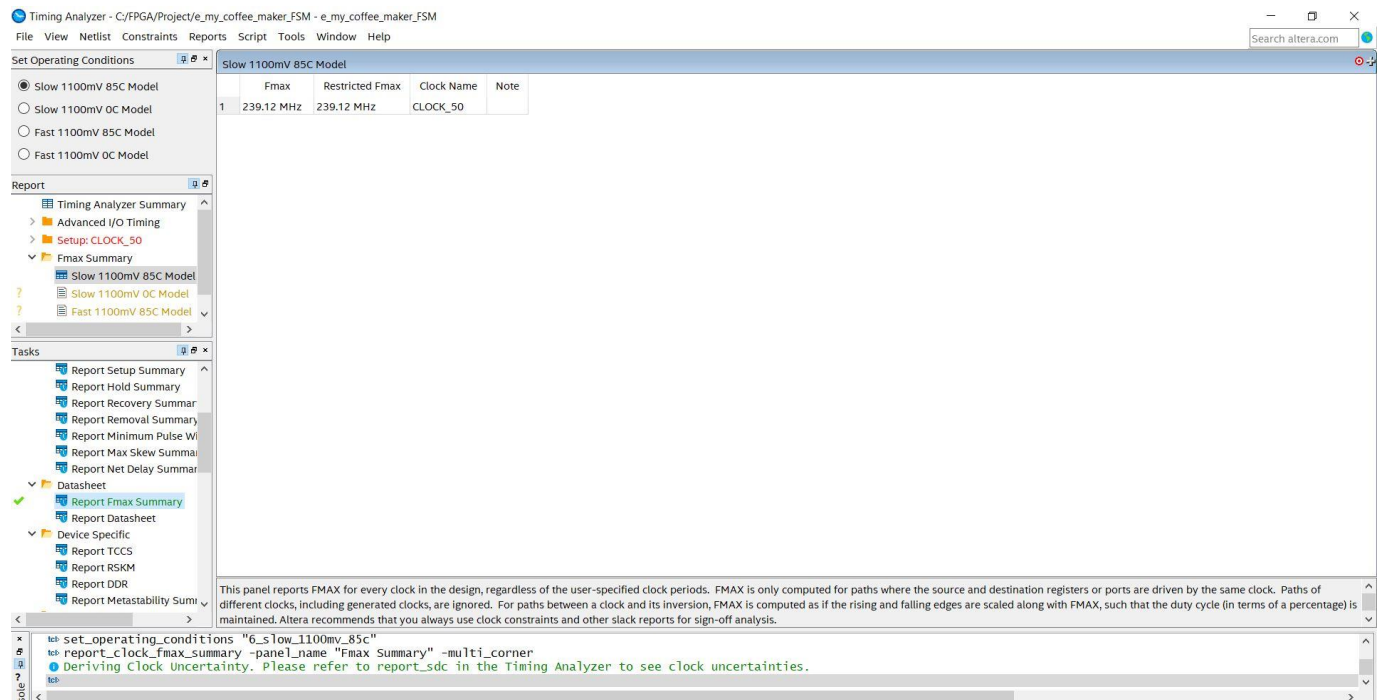
This panel reports FMAX for every clock in the design, regardless of the us computed for paths where the source and destination registers or ports ar clocks, including generated clocks, are ignored. For paths between a clock

All Find... Find Next

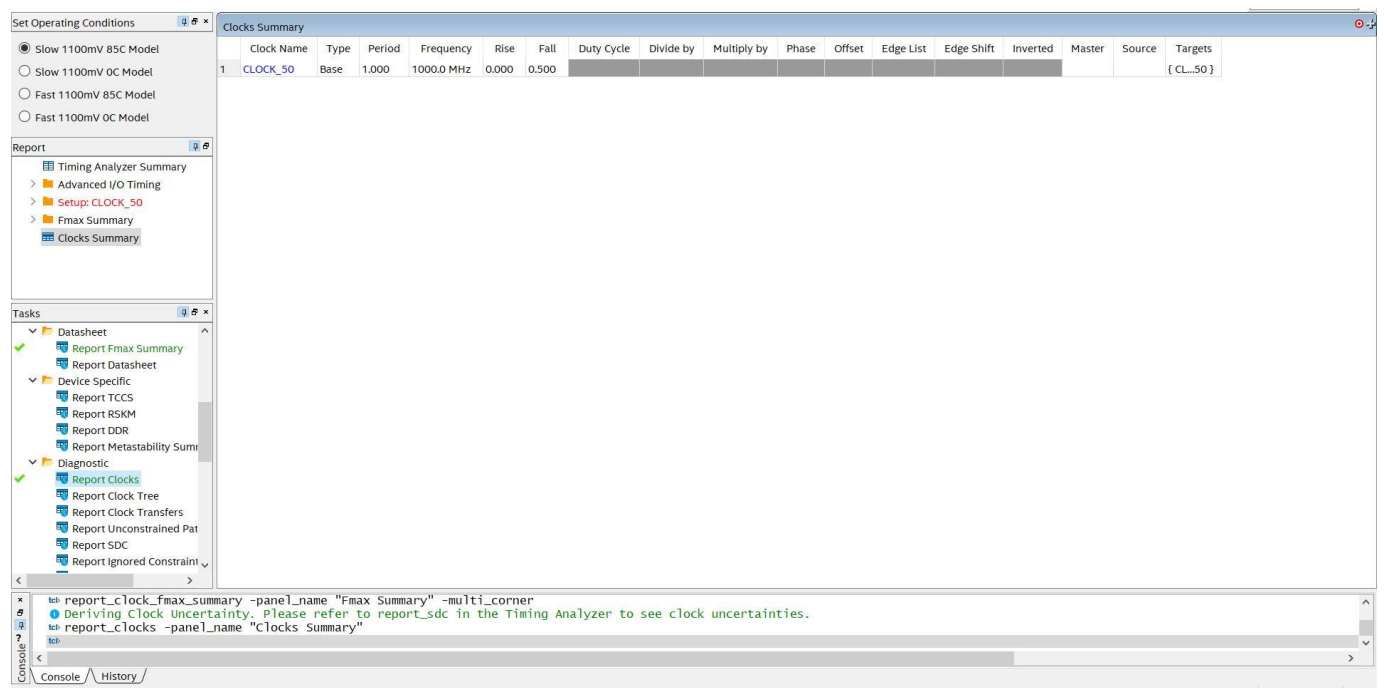
Type ID Message
332012 Synopsys Design Constraints File file not found: 'e_my_coffee_maker_FSM.sdc'. A Synopsys Design Constraint
332012 Synopsys Design Constraints File file not found: 'e_my_coffee_maker_FSM.sdc'. A Synopsys Design Constraint
> 332148 Timing requirements not met
> 332148 Timing requirements not met
> 332148 Timing requirements not met
> 332148 Timing requirements not met

Picture 3. Fmax Summary

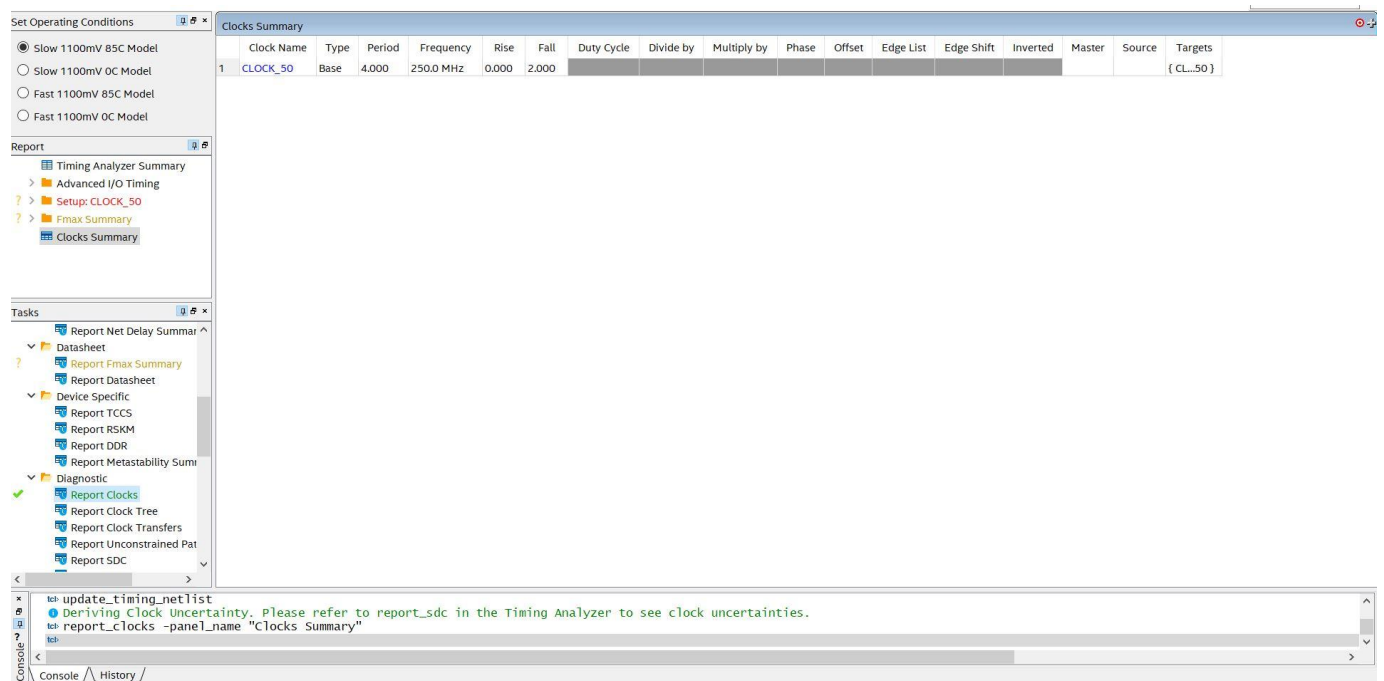




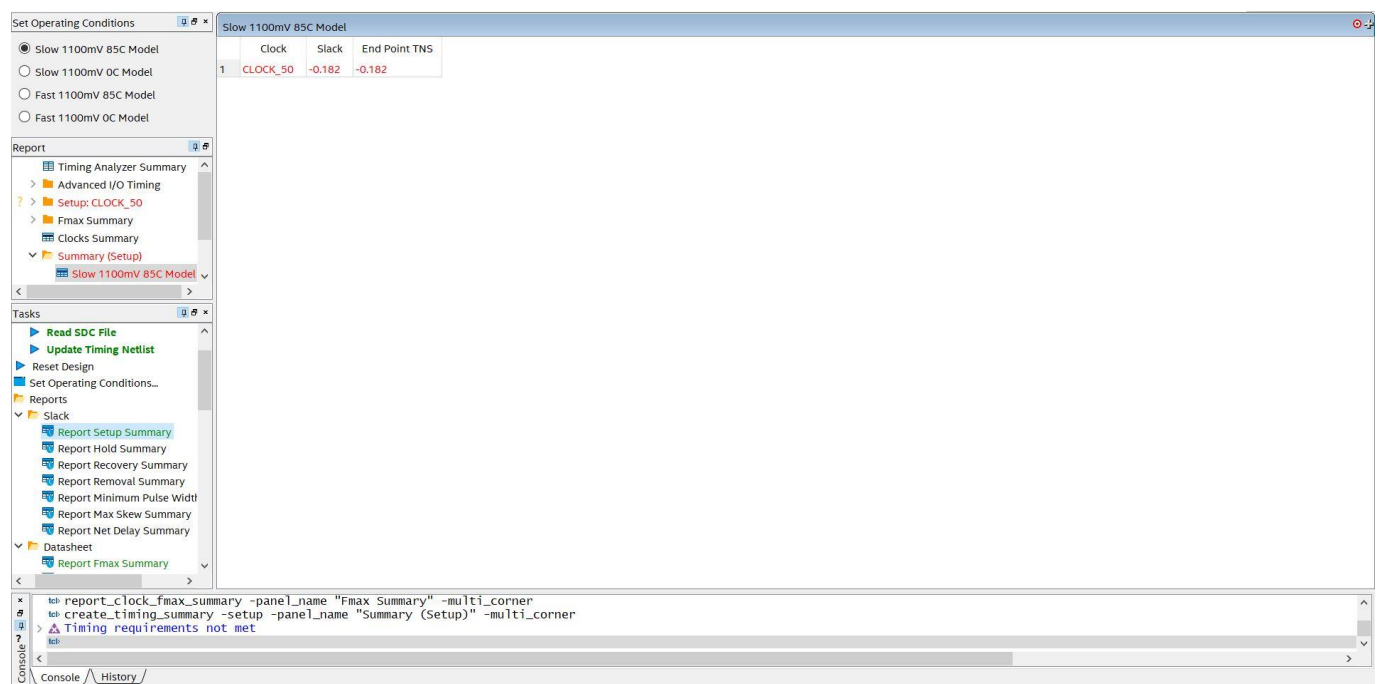
Picture 6. Before changes



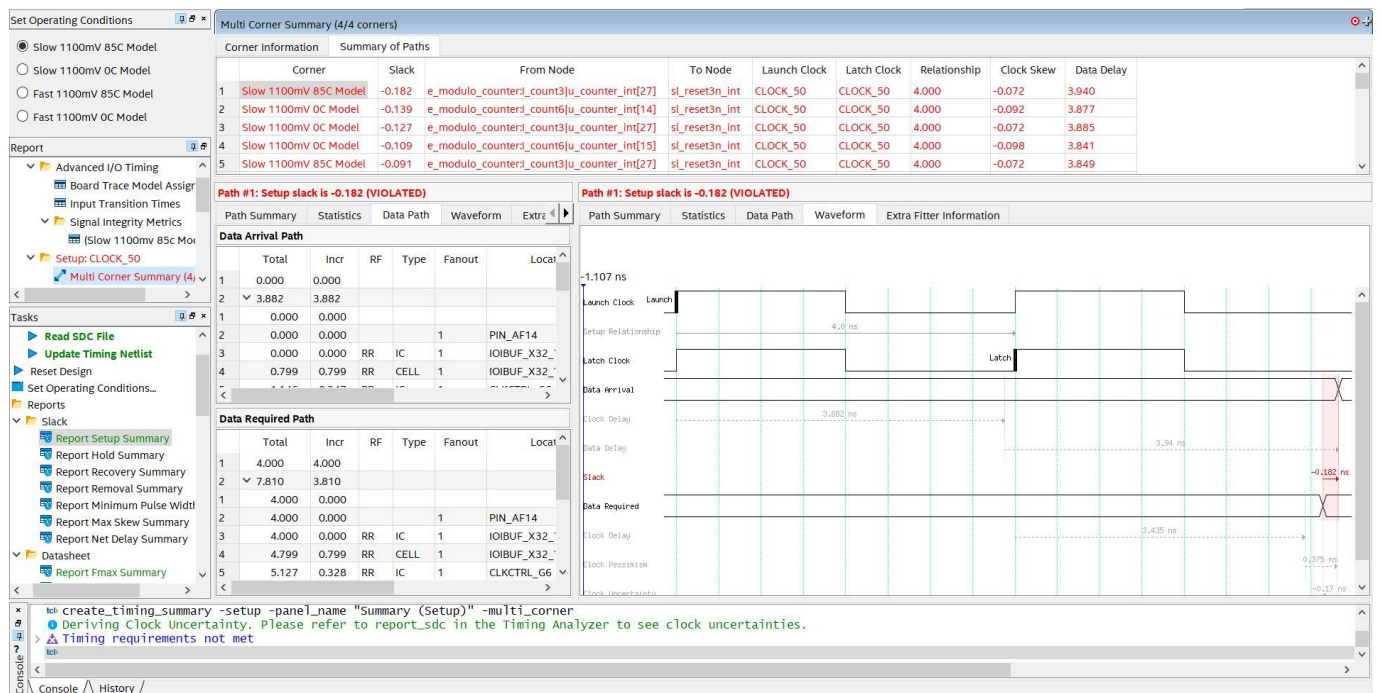
Picture 7. Per default a clock with a frequency of 1 GHz will be assumed



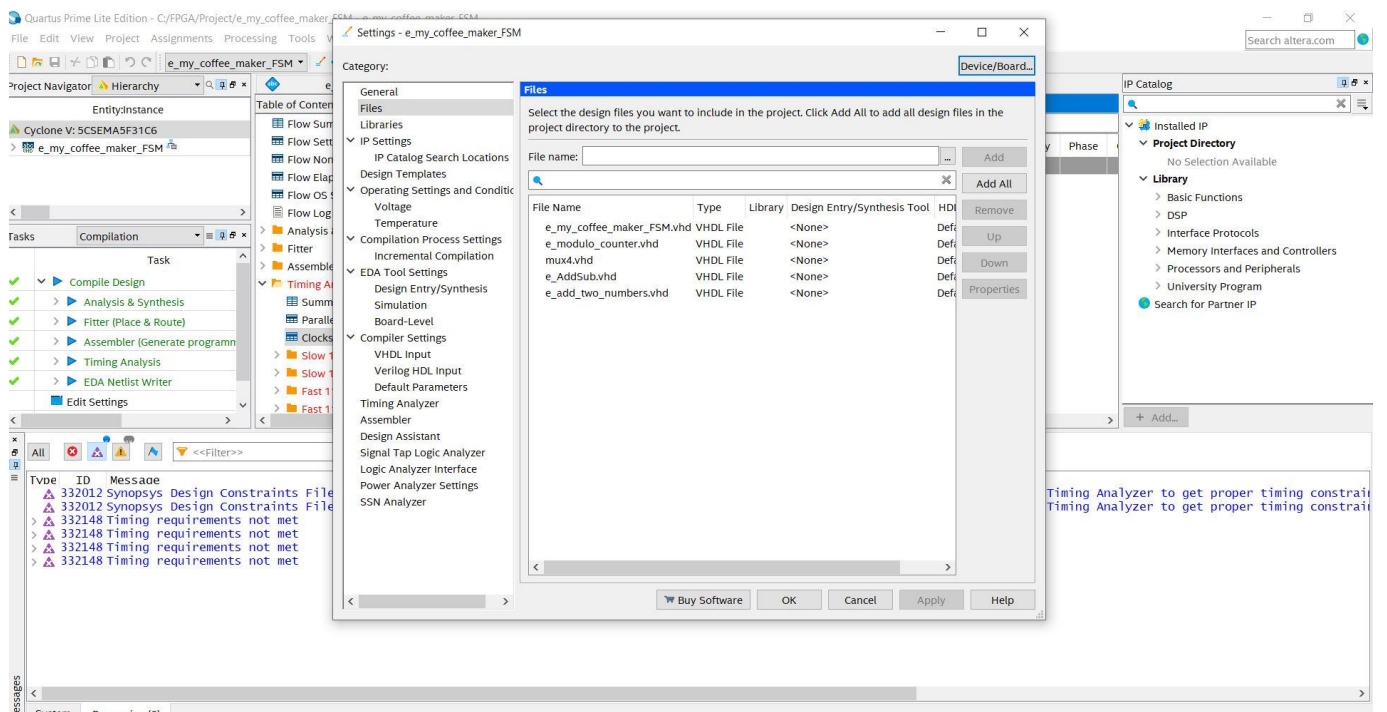
Picture 8. Was set 250 Mhz/4ns



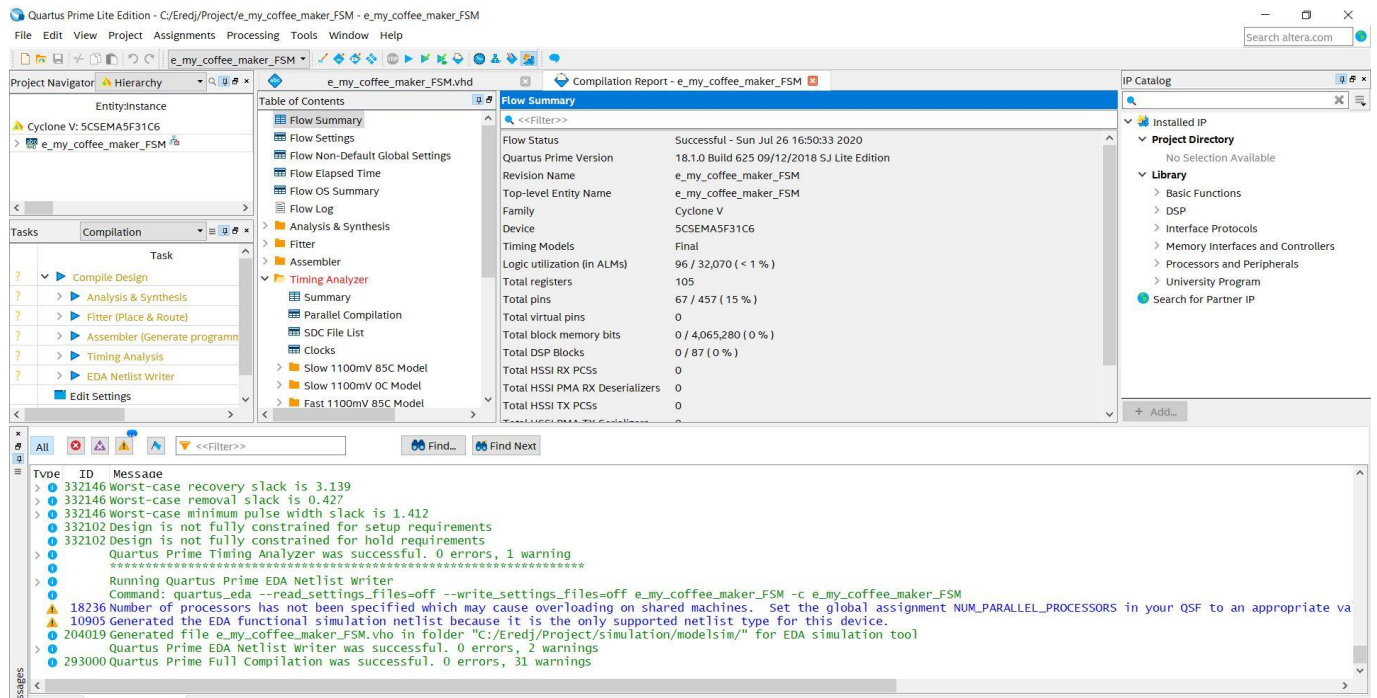
Picture 9. Clock revision



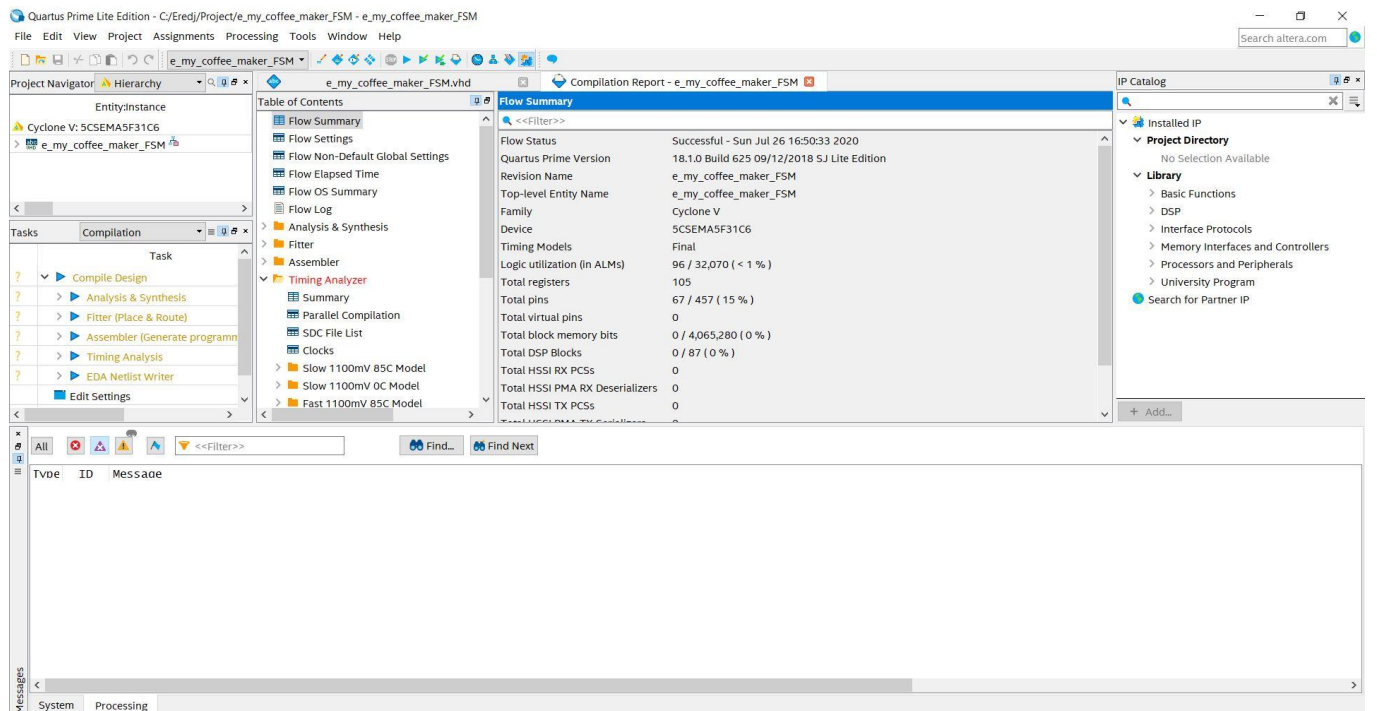
Picture 10. Saving new time constraints in a file e_my_coffee_maker_FSM.sdc



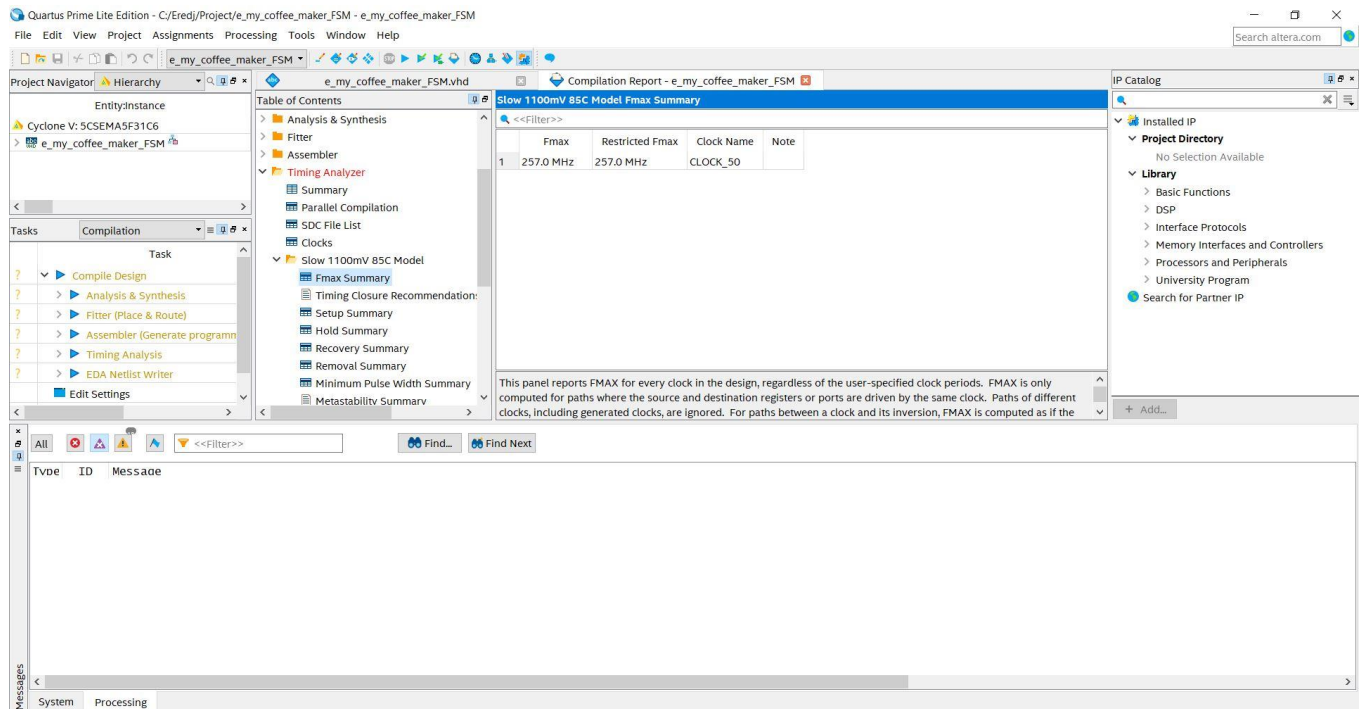
Picture 11. Import time constraints from e_my_coffee_maker_FSM.sdc



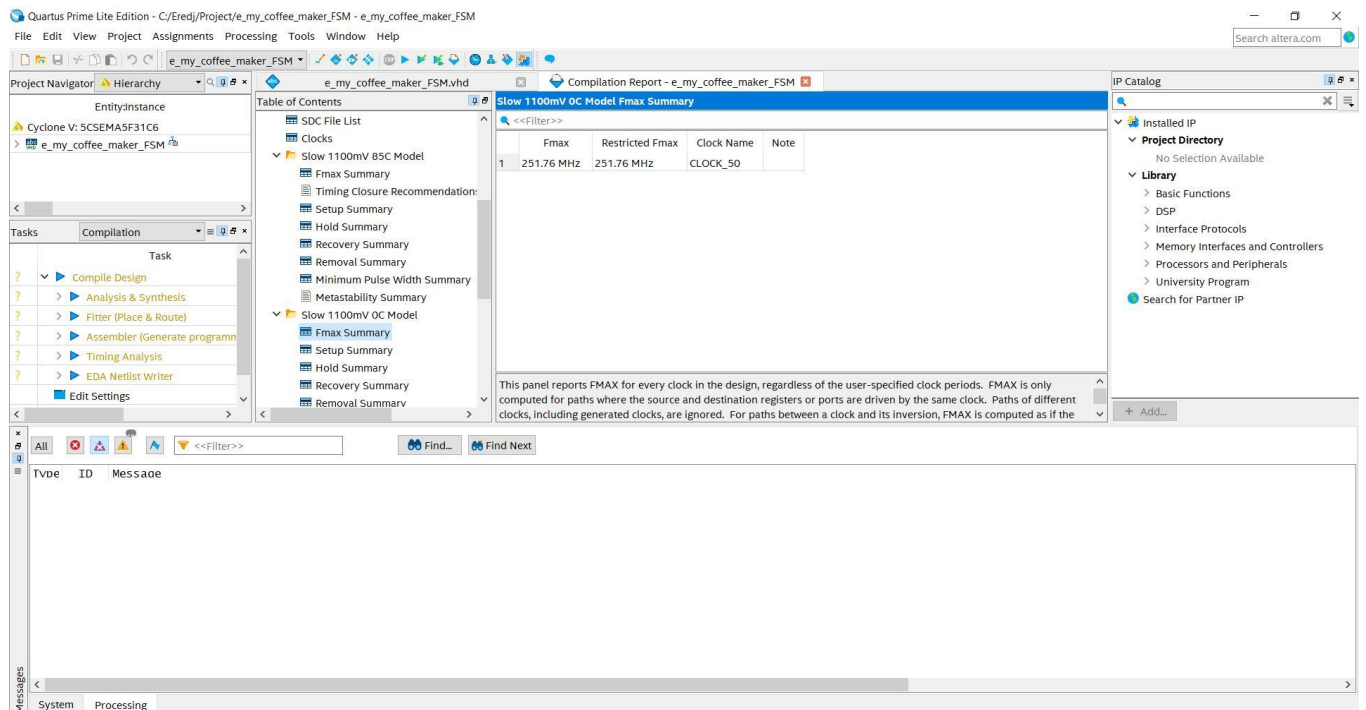
Picture 12. After updating Timing requirements are met



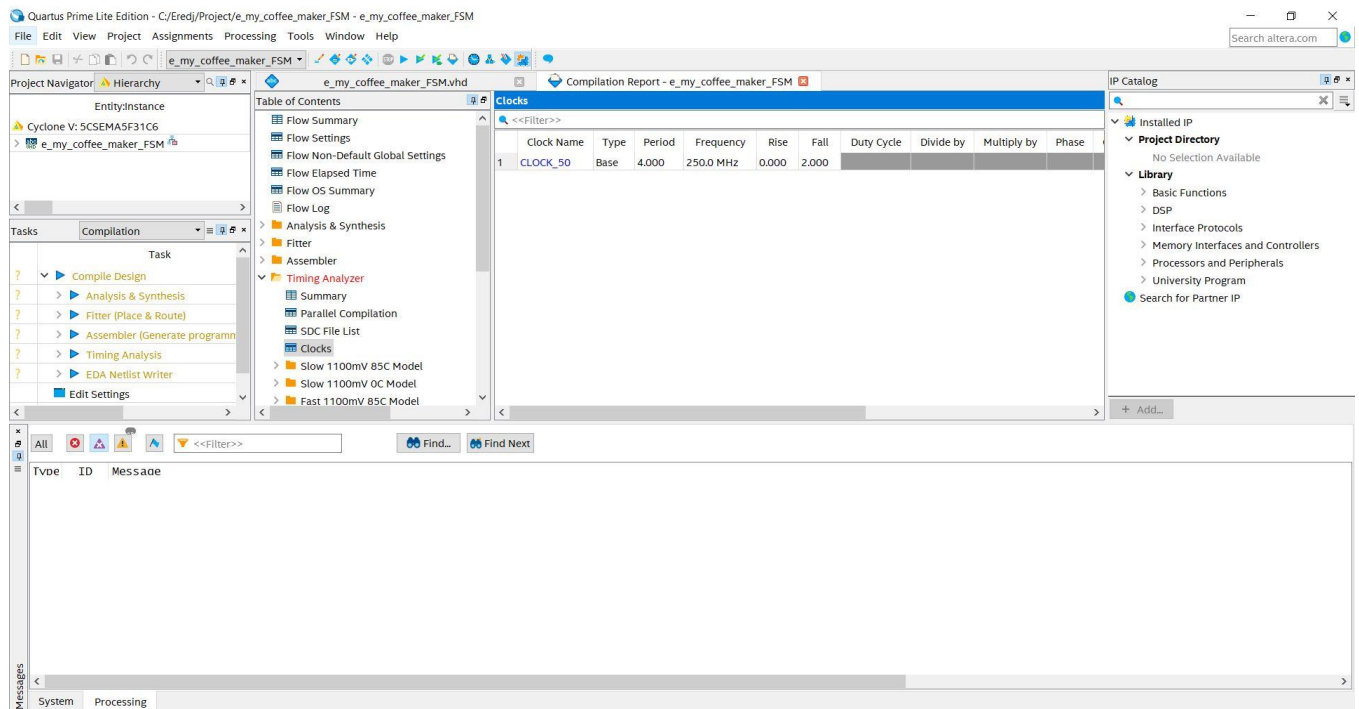
Picture 13. After updating Timing requirements are met



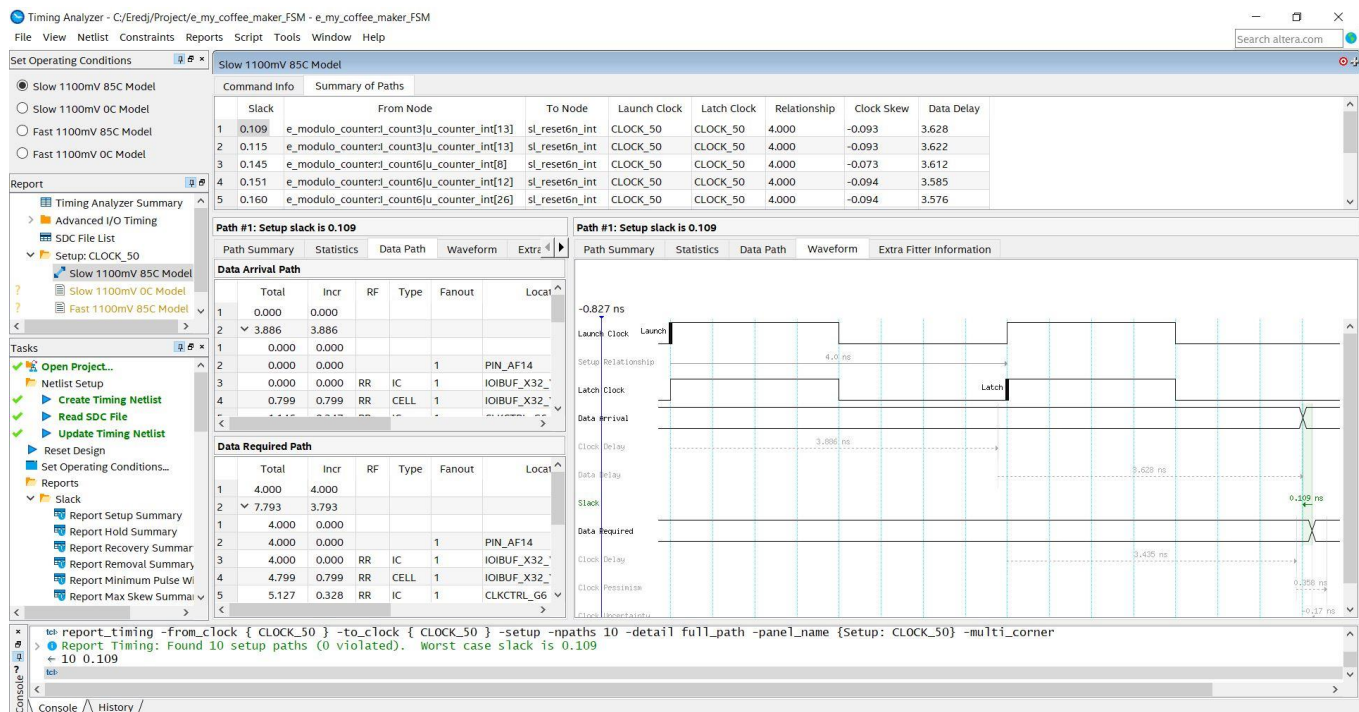
Picture 14. After updating Fmax Summary



Picture 15. After updating second Fmax Summary



Picture 16. Constraining input clock signal: 250 Mhz/ 4 ns



Picture 17. After updating timing netlist and regenerating report