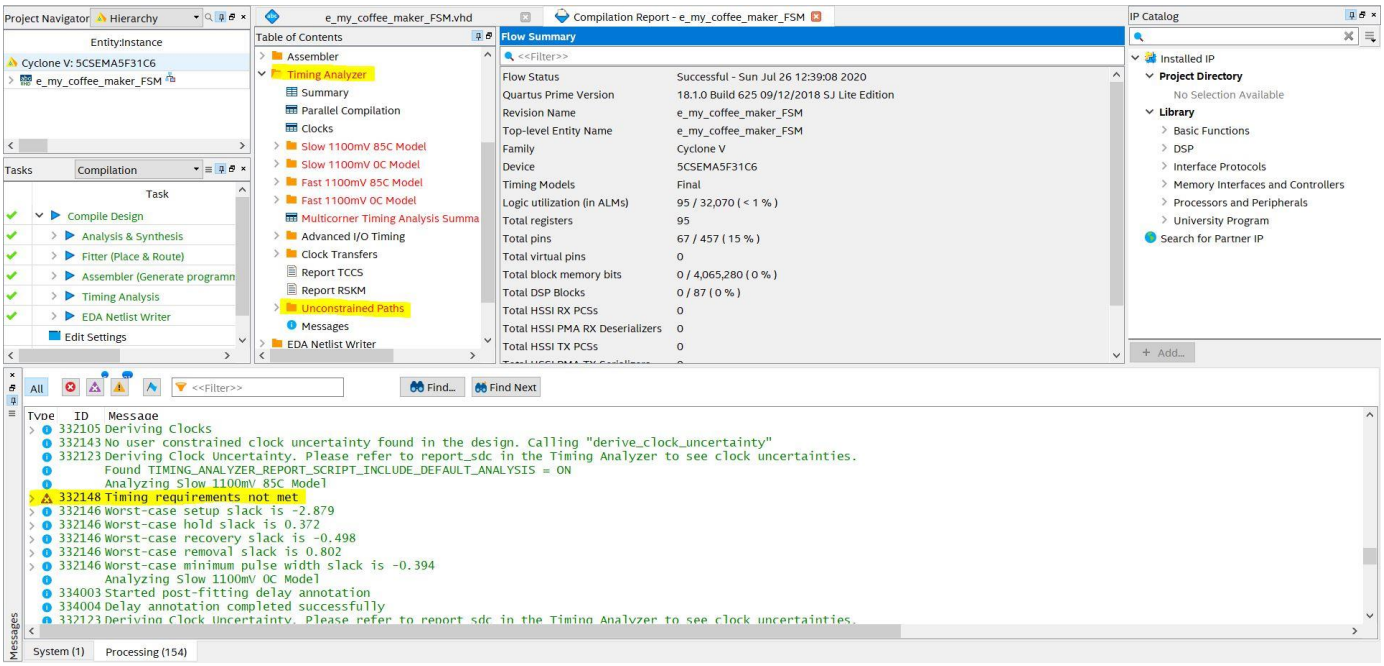
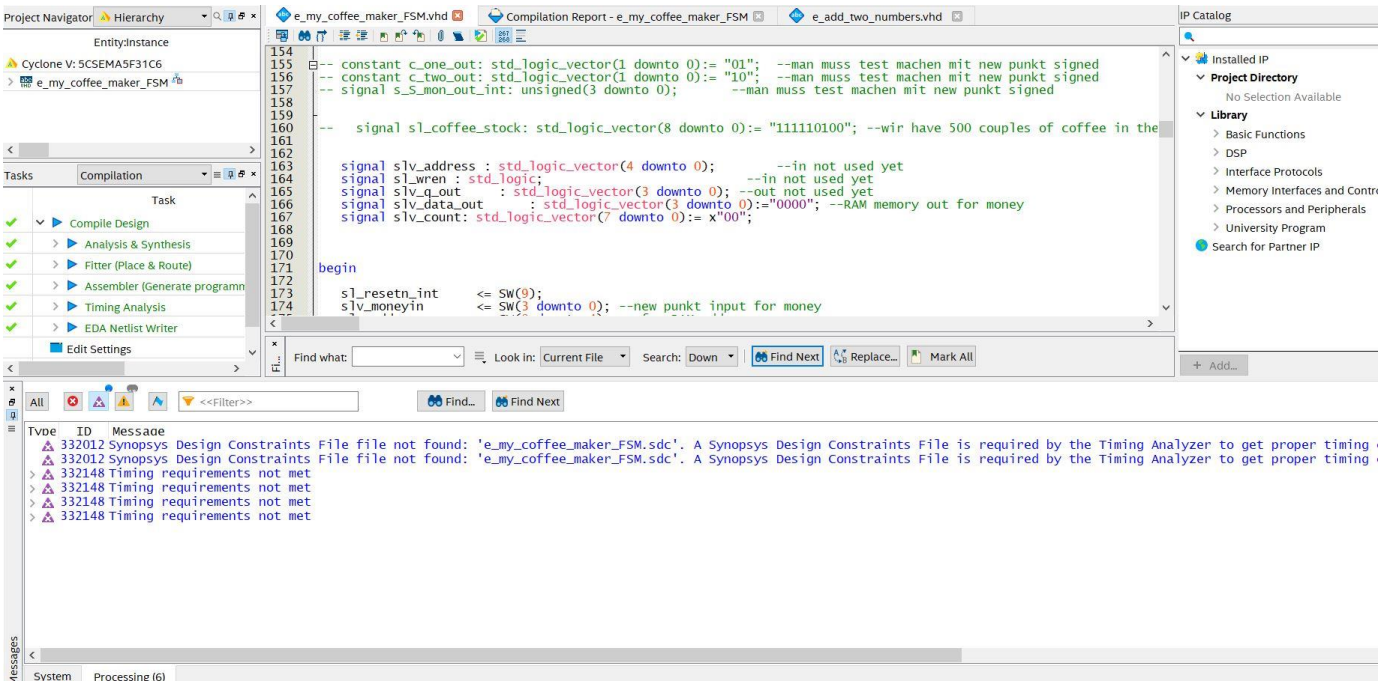
TimeQuest Analyzer Report

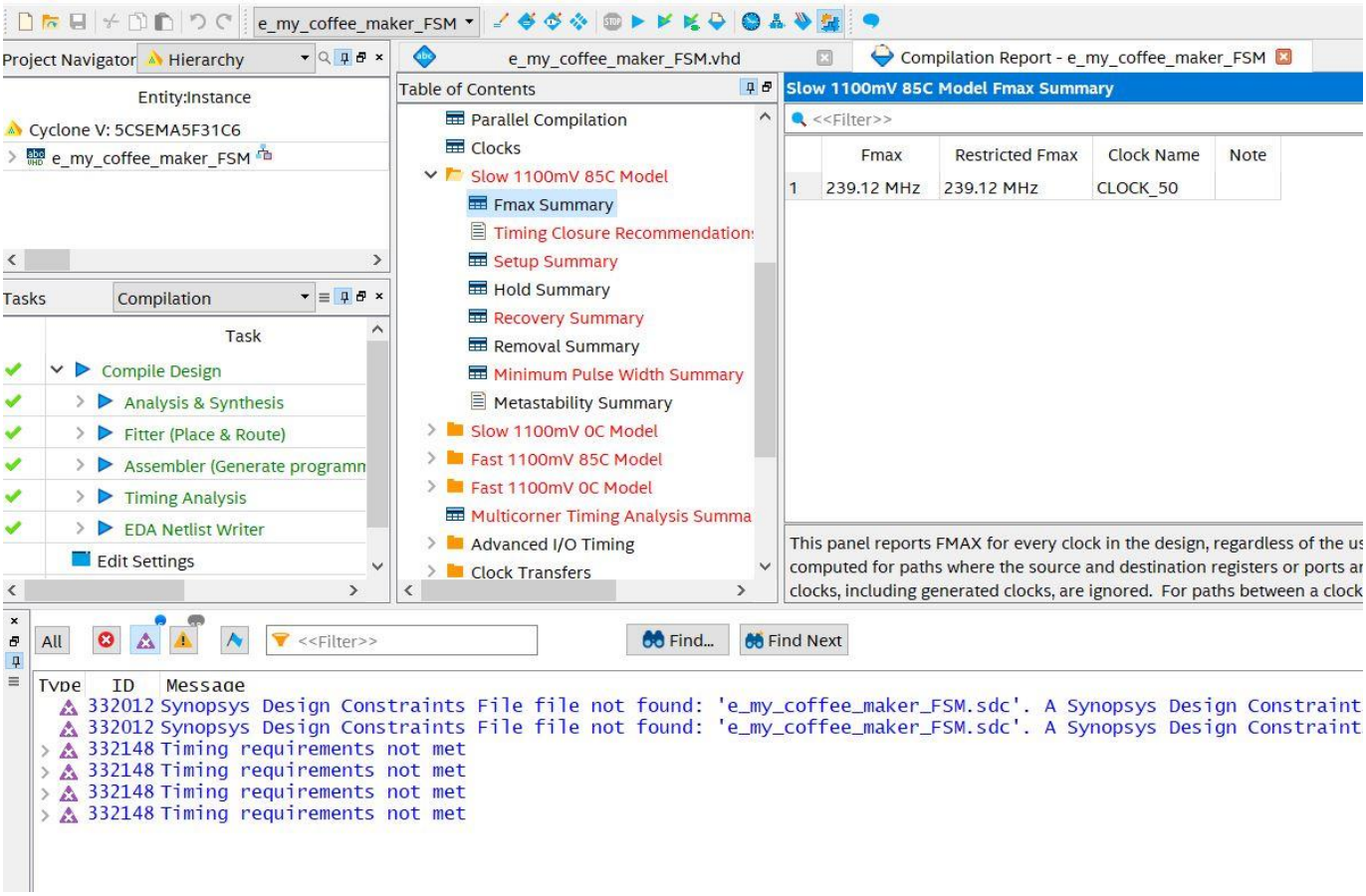
Time configuration parameters was created and saved as a file: *e_my_coffee_maker_FSM.sdc* (*C:\FPGA\Project\TimeQuest Analyzer Report\e_my_coffee_maker_FSM.sdc*). All steps were indicated in a screenshots bellow. In our case we have Maximum of negative slack is *-3,182 ns*. Worst case propagation delay could be found with a formula *clock period - slack*: *1 ns - (-3,182) = 4,182 ns*. From this we could find maximum frequency: *Fmax = 1 / 4,182= 239,12 MHz* .



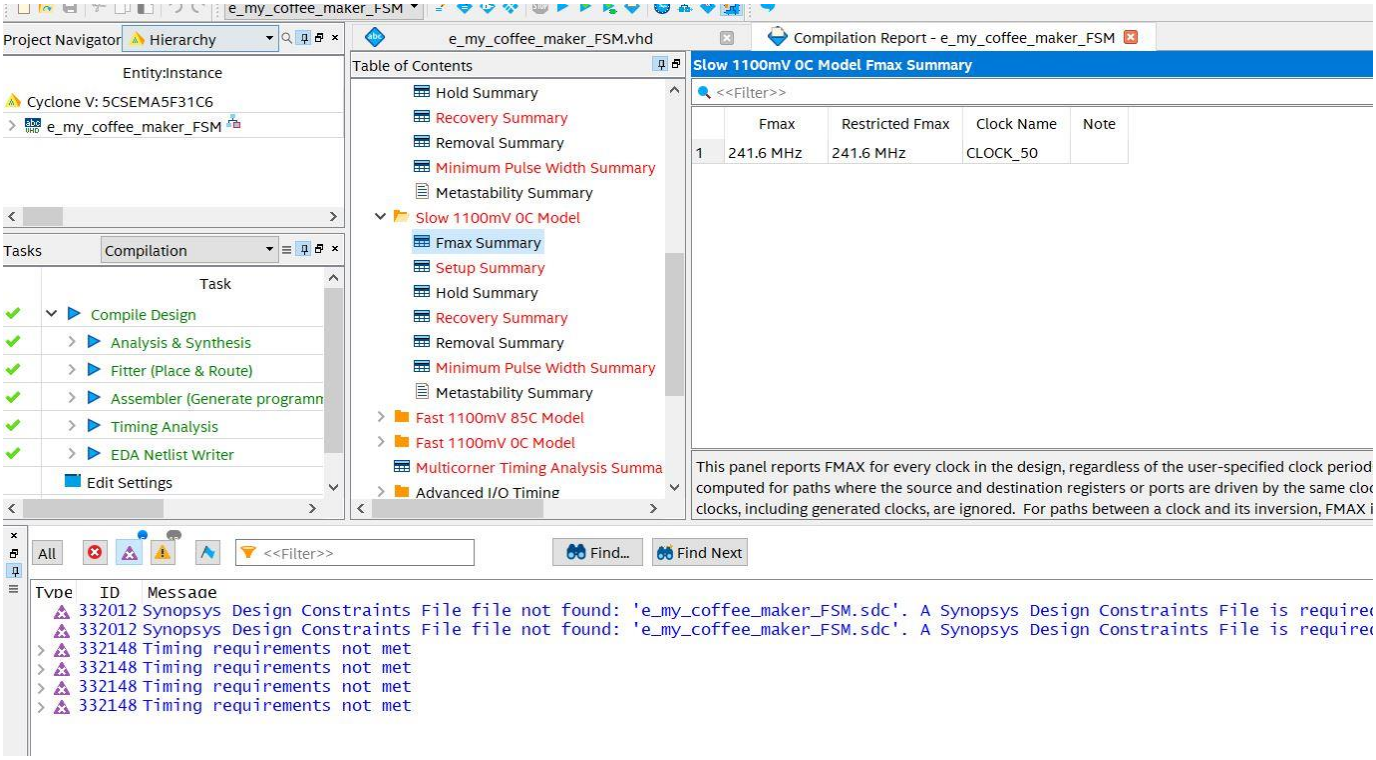
Picture 1. Time requirements not met



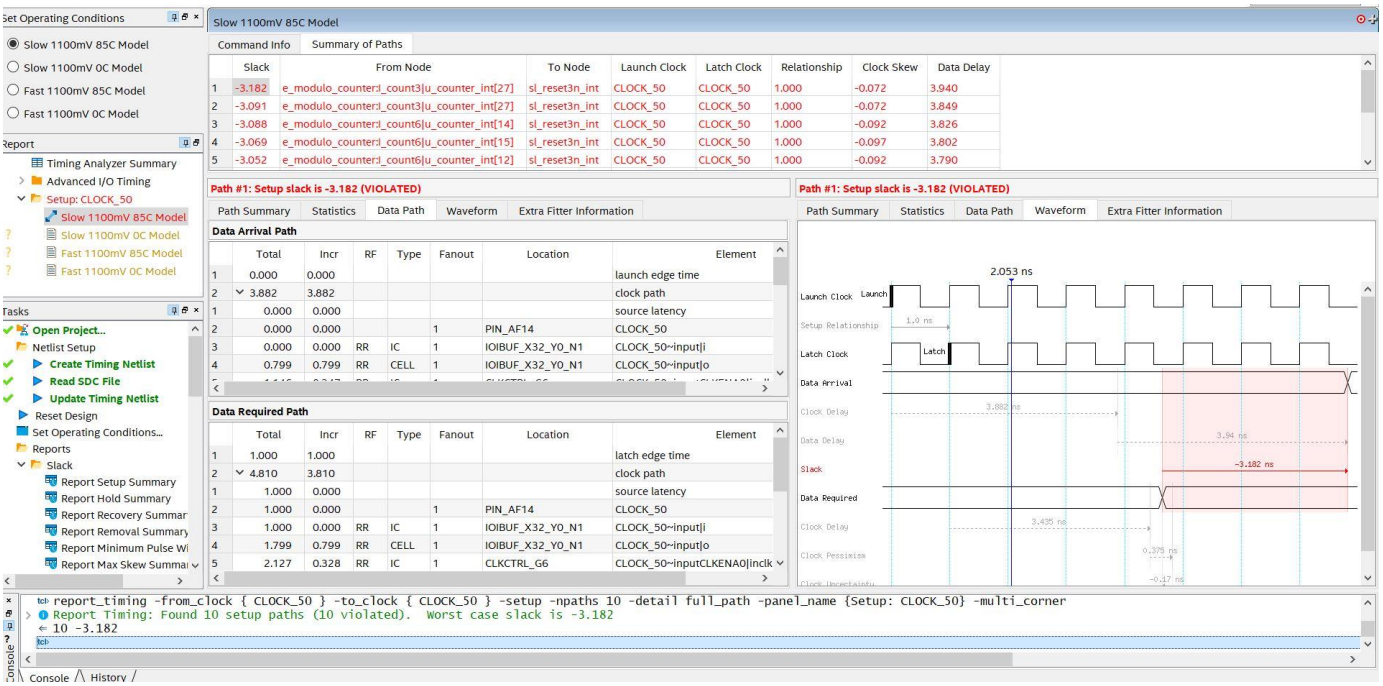
Picture 2. Time requirements not met



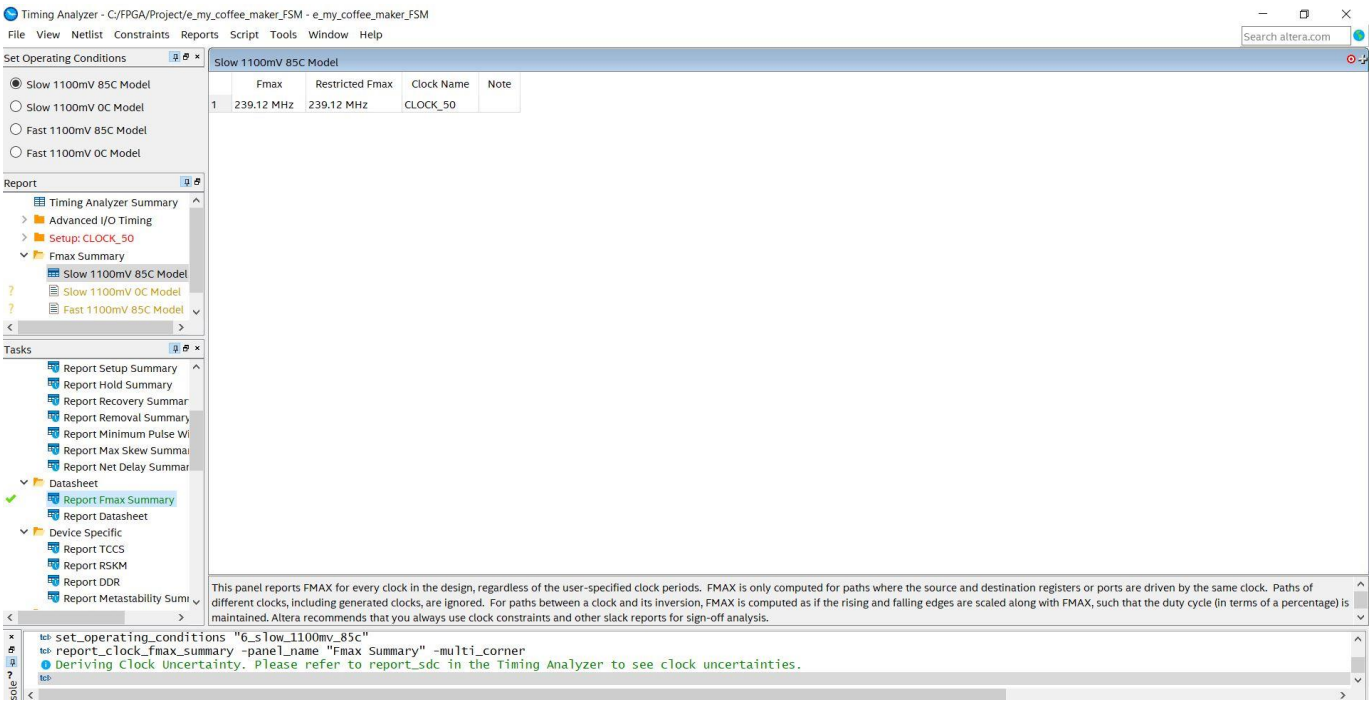
Picture 3. Fmax Summary



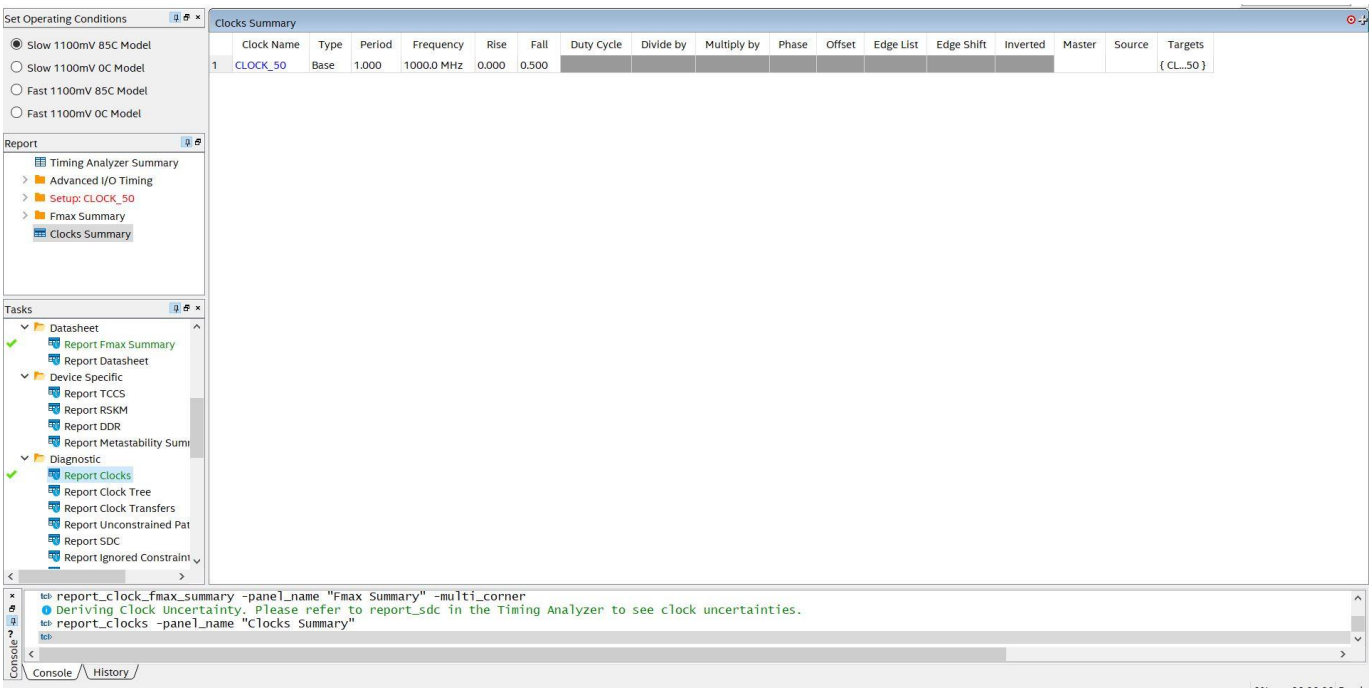
Picture 4. Second Fmax Summary



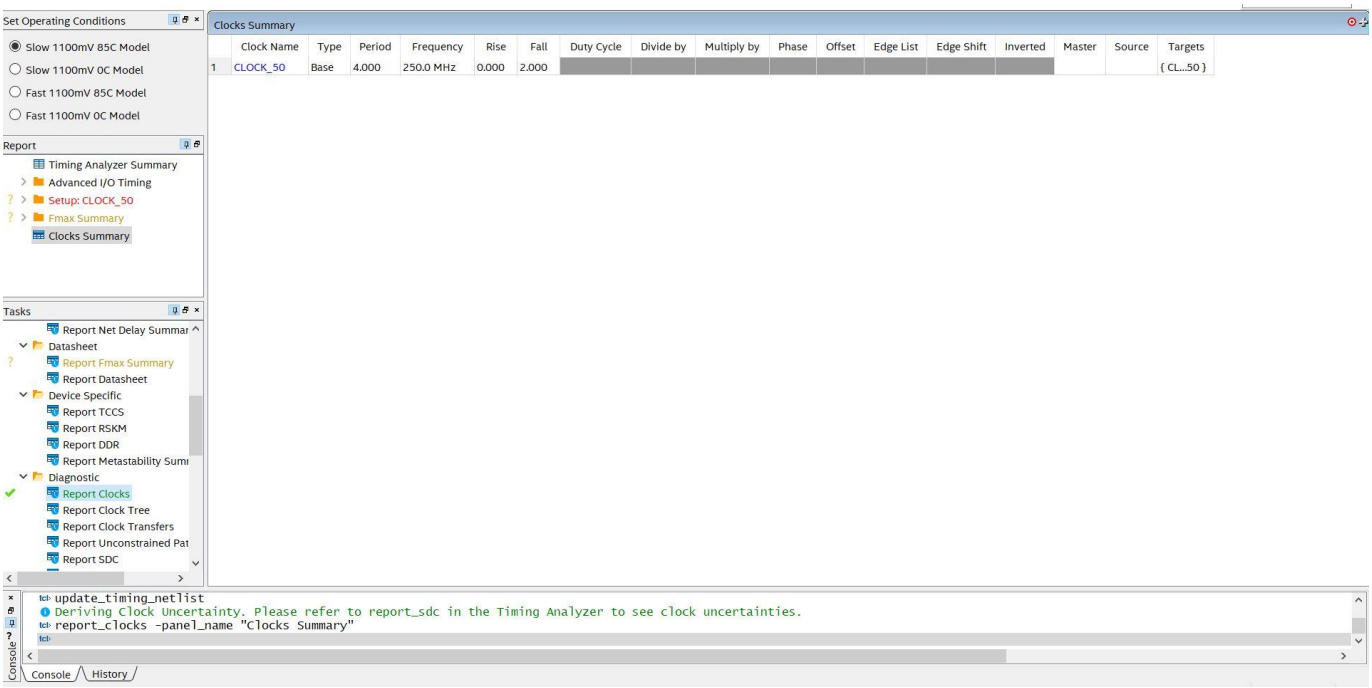
Picture 5. Negative slack violates timing. Maximum of negative slack is –3,182 ns



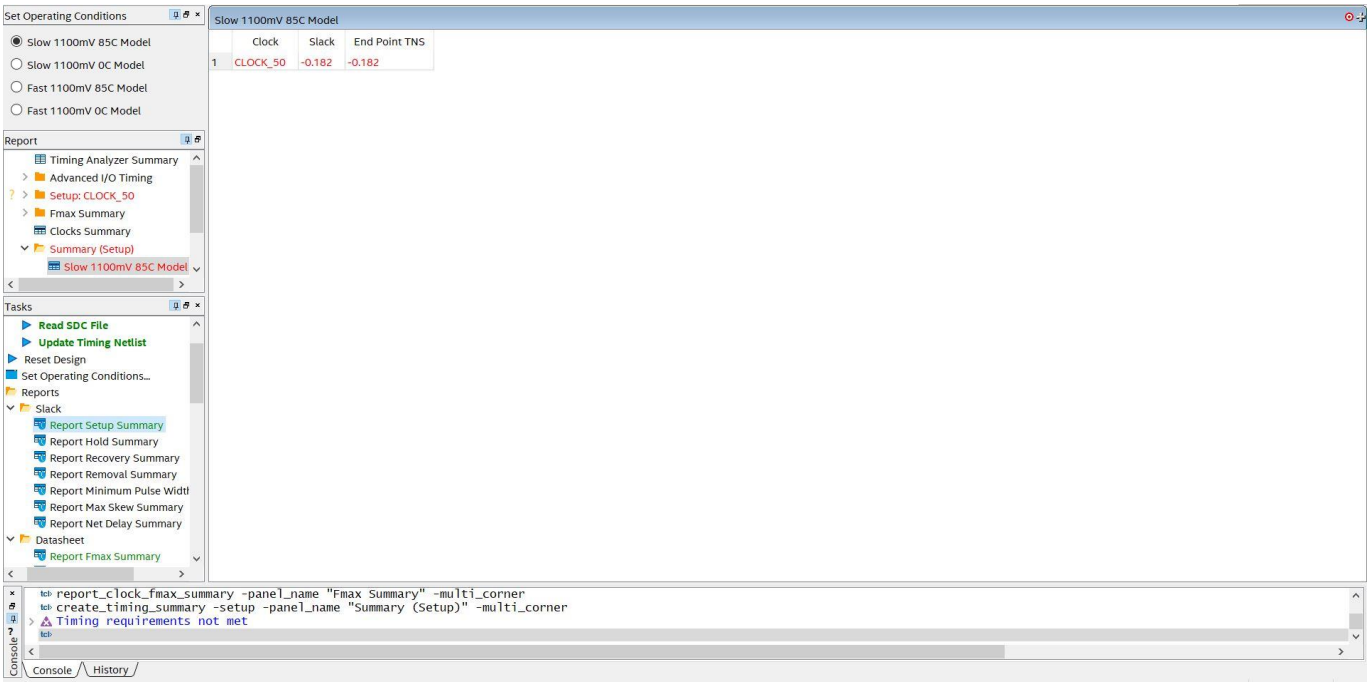
Picture 6. Before changes



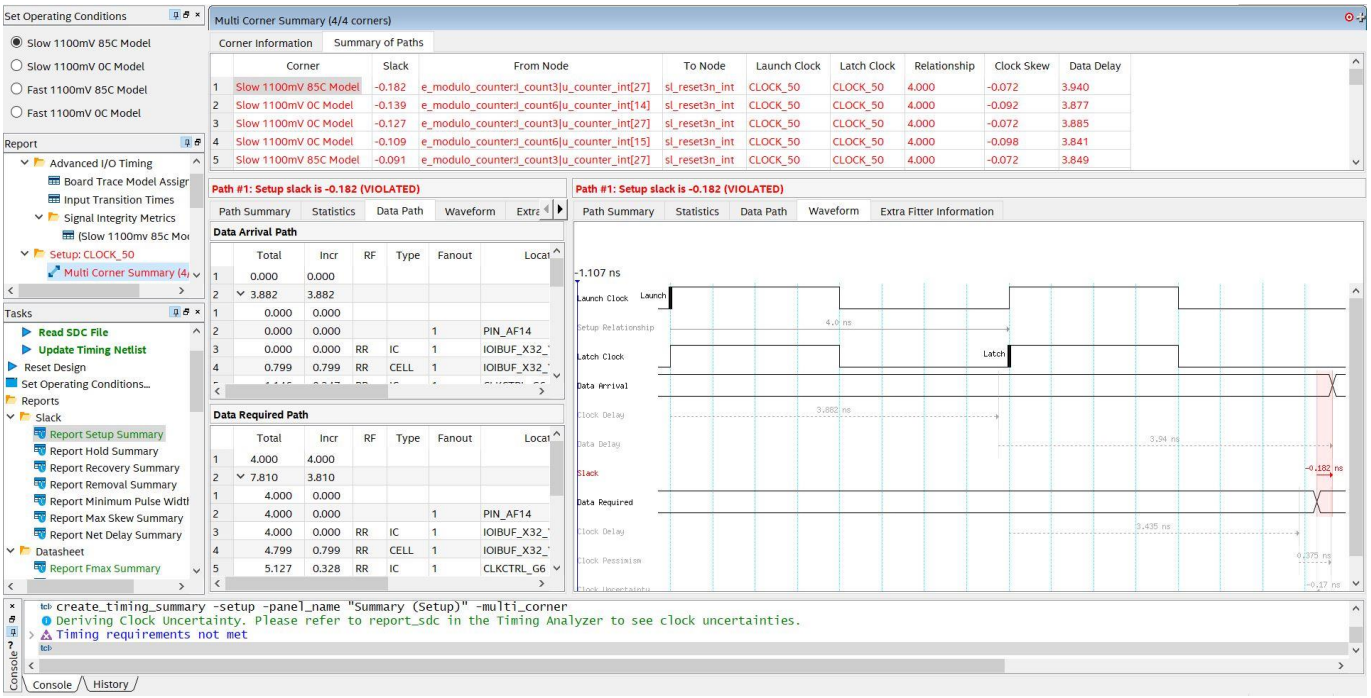
Picture 7. Per default a clock with a frequency of 1 GHz will be assumed



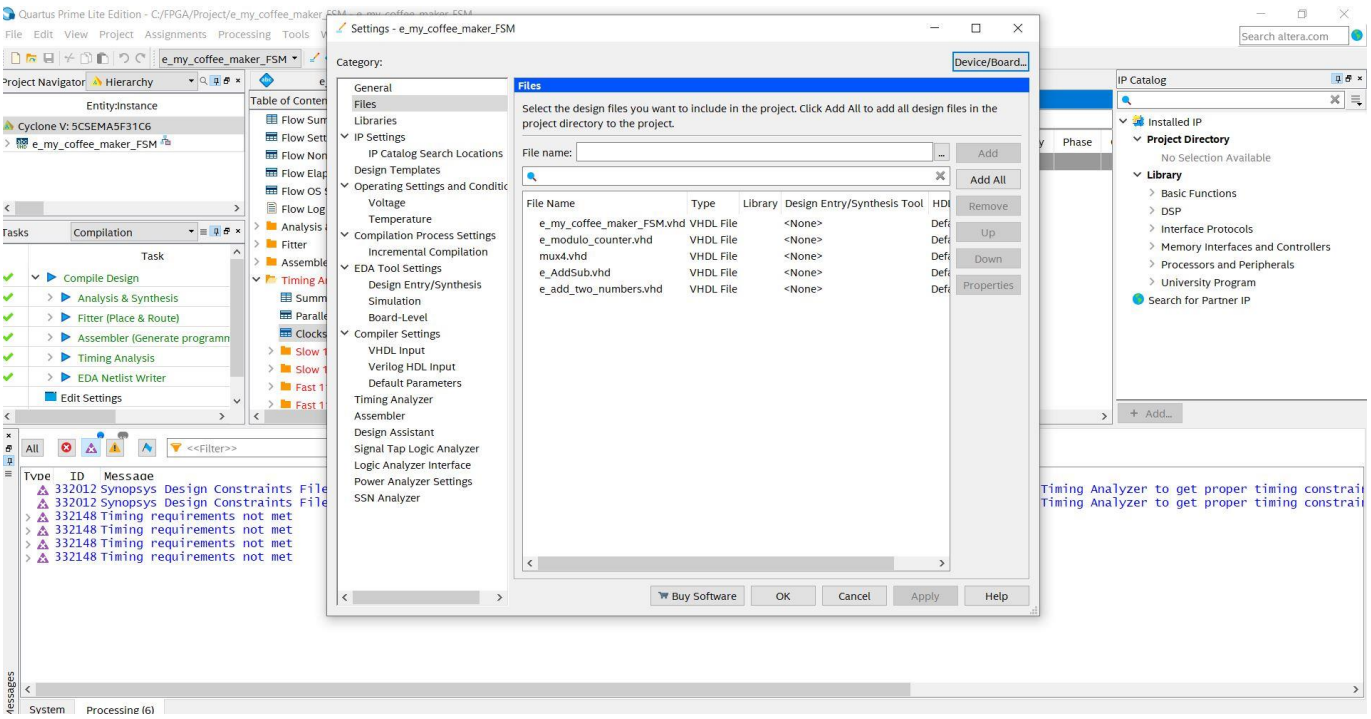
Picture 8. Was set 250 Mhz/4ns



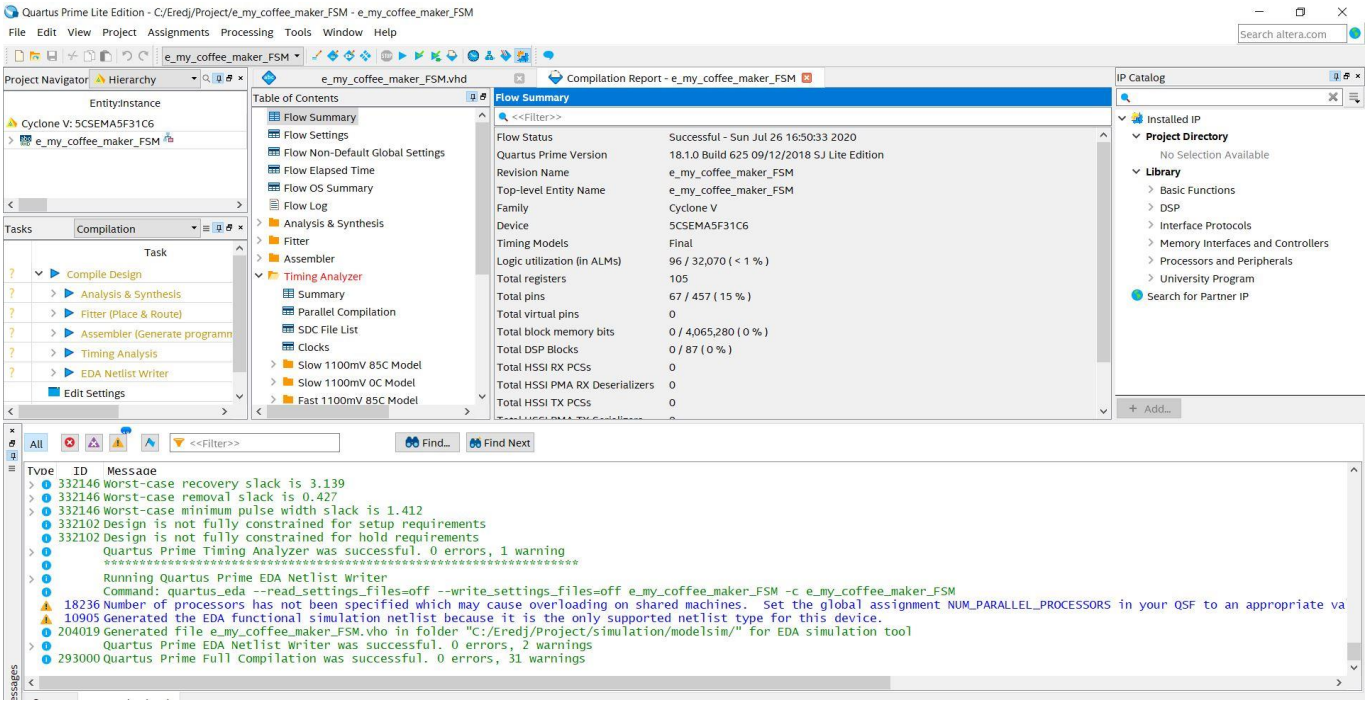
Picture 9. Clock revision



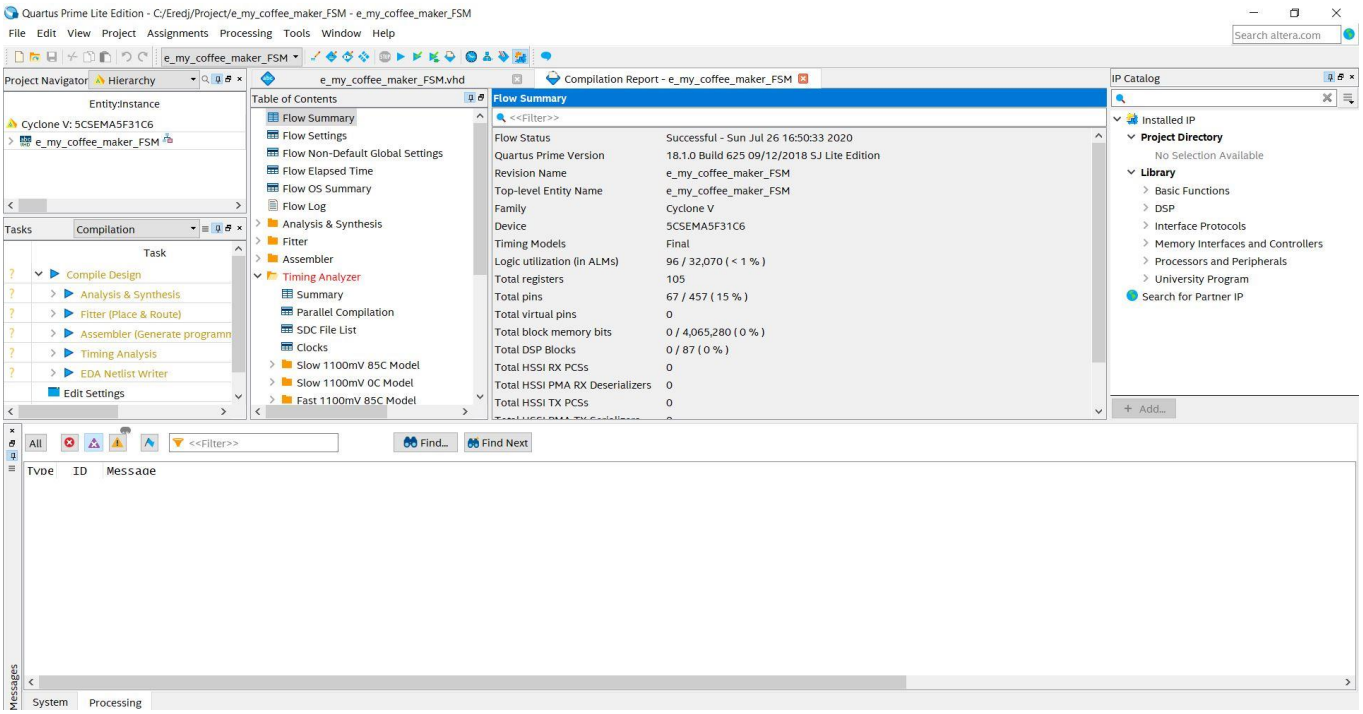
Picture 10. Saving new time constraints in a file e_my_coffee_maker_FSM.sdc



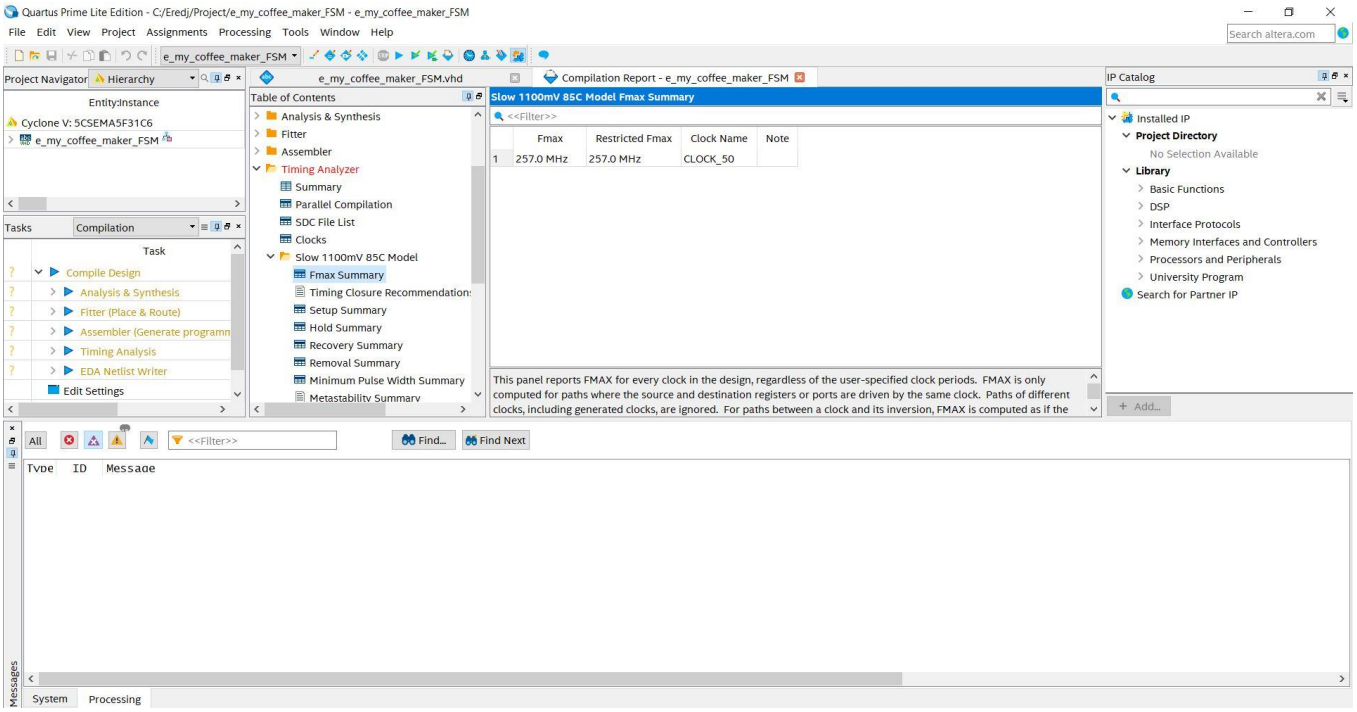
Picture 11. Import time constraints from e_my_coffee_maker_FSM.sdc



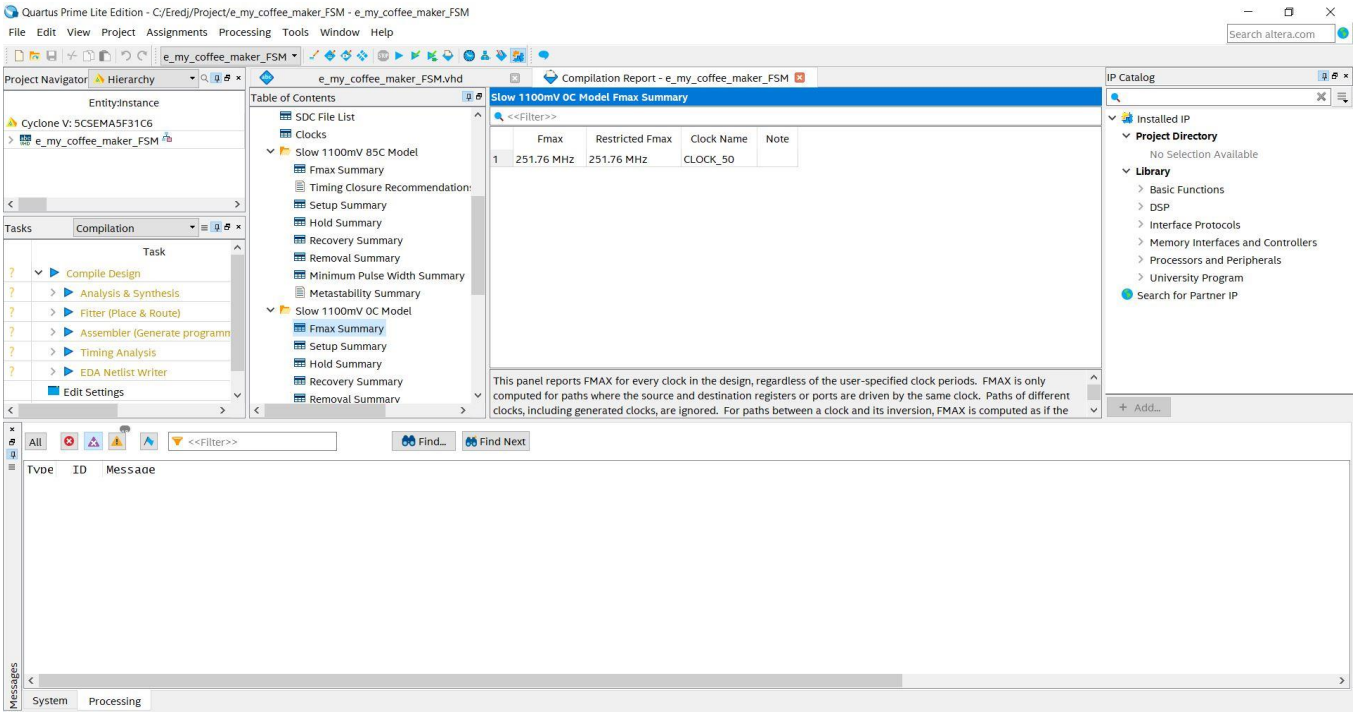
Picture 12. After updating Timing requirements are met



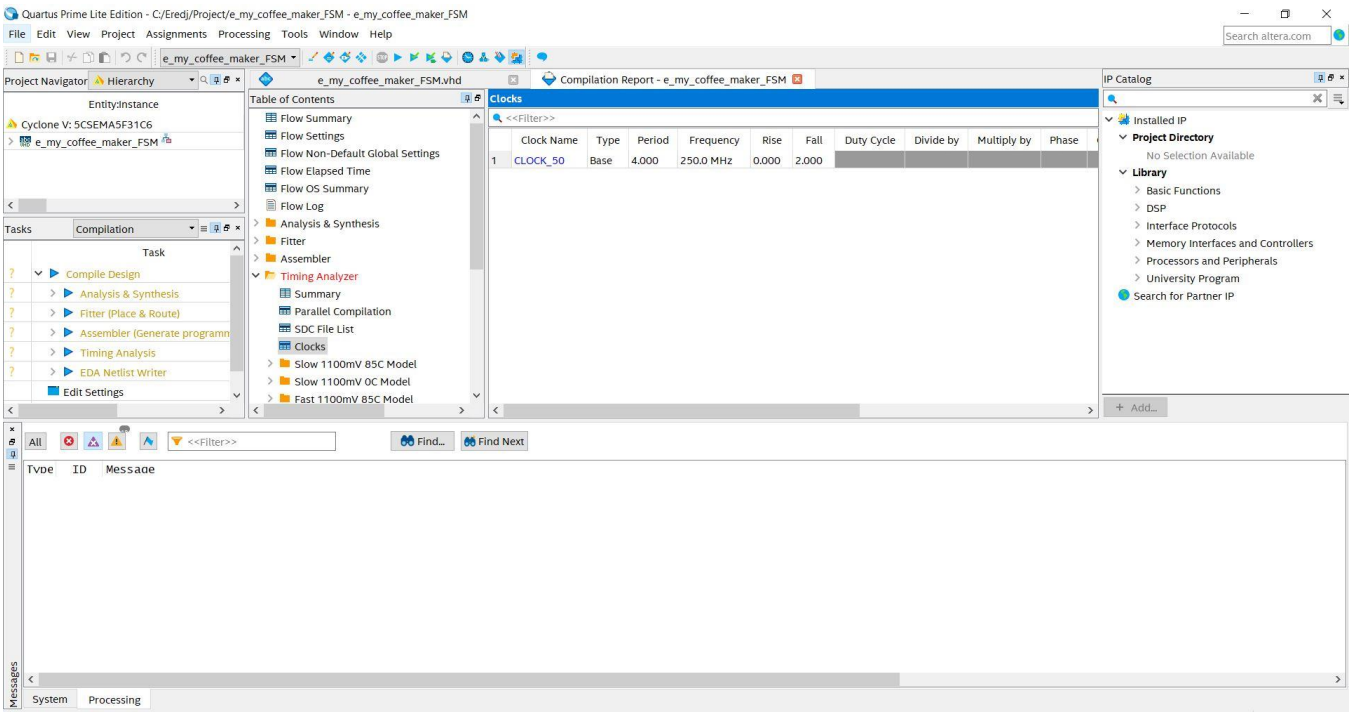
Picture 13. After updating Timing requirements are met



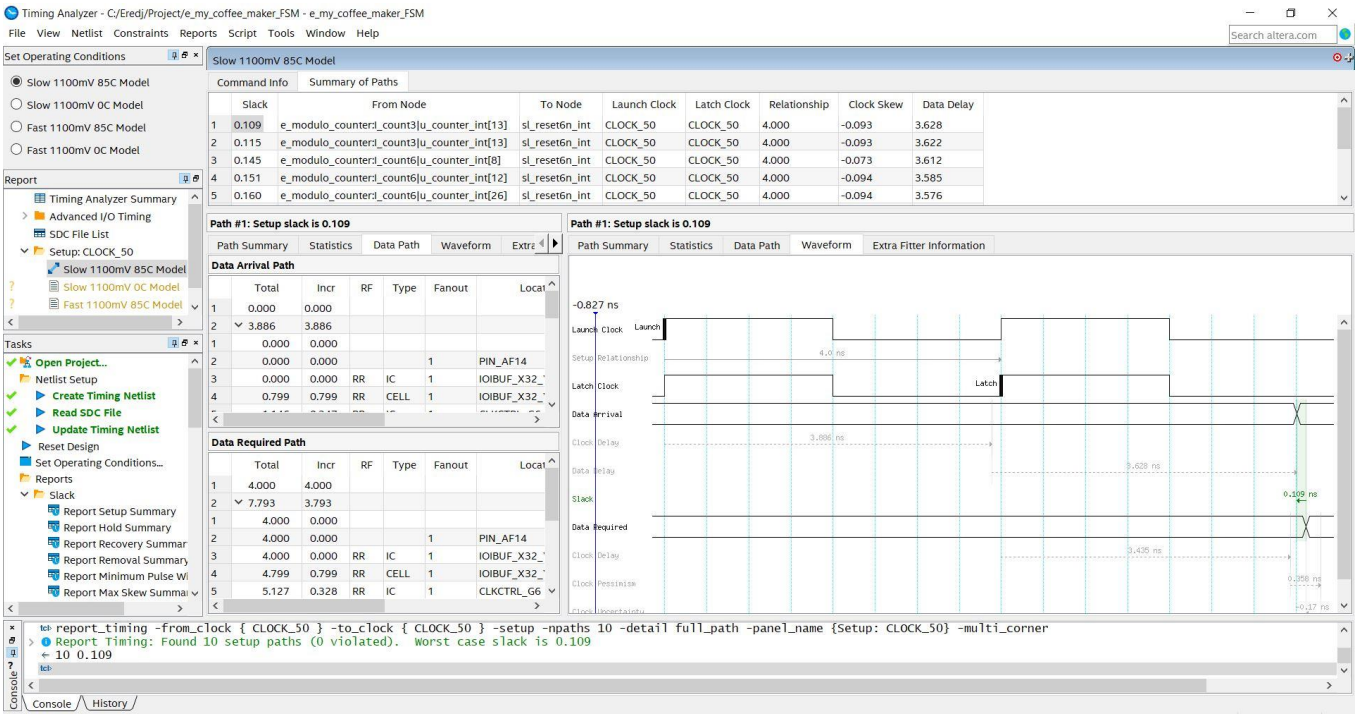
Picture 14. After updating Fmax Summary



Picture 15. After updating second Fmax Summary



Picture 16. Constraining input clock signal: 250 Mhz/ 4 ns



Picture 17. After updating timing netlist and regenerating report