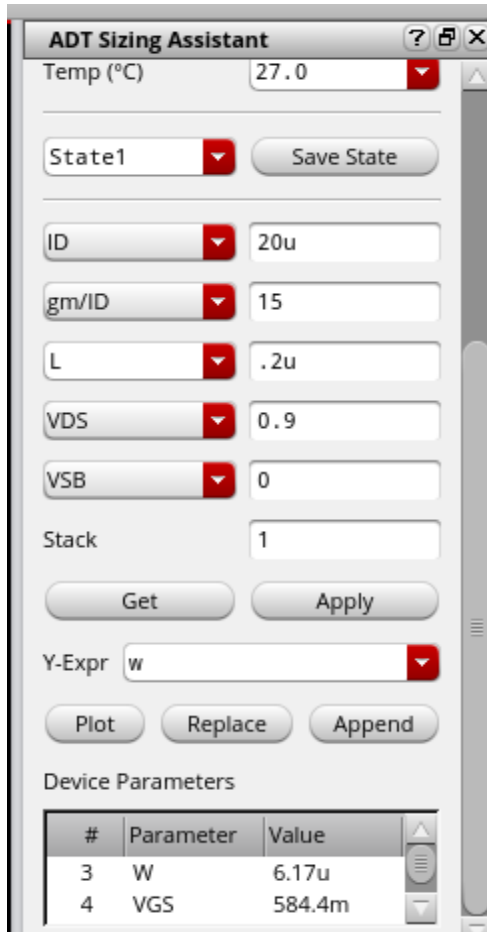


PART 2: OTA Design

For the input pair use short L and bias it in MI or WI, e.g., $L = 0.2\mu\text{m}$ and $gm/ID = 15$. This maximizes the GBW (good efficiency) and minimizes the input capacitive loading (avoid reducing the DC LG). You will have to tune your gm/ID to achieve the CL bandwidth spec.



The screenshot shows the 'ADT Sizing Assistant' dialog box with the following settings:

- Temp (°C): 27.0
- State1: [dropdown arrow] Save State
- ID: [dropdown arrow] 20u
- gm/ID: [dropdown arrow] 15
- L: [dropdown arrow] .2u
- VDS: [dropdown arrow] 0.9
- VSB: [dropdown arrow] 0
- Stack: 1
- Get: [button] Apply: [button]
- Y-Expr: w [dropdown arrow]
- Plot: [button] Replace: [button] Append: [button]
- Device Parameters table:

#	Parameter	Value
3	W	6.17u
4	VGS	584.4m

For the current source transistors use relatively long L and bias them in SI, e.g., $L = 1\mu\text{m}$ and $gm/ID = 10$. These transistors contribute significant offset and noise. A large gm will not help the gain but will increase the noise

ADT Sizing Assistant ? [icon] X

Temp (°C) 27.0 [dropdown]

State1 [dropdown] Save State

ID [dropdown] 40u

gm/ID [dropdown] 10

L [dropdown] 1u

VDS [dropdown] 0.45

VSB [dropdown] 0

Stack 1

Get Apply

Y-Expr w [dropdown]

Plot Replace Append

Device Parameters

#	Parameter	Value
3	W	8.59u
4	VGS	616m

ADT Sizing Assistant ? [icon] X

Temp (°C) 27.0 [dropdown]

State1 [dropdown] Save State

ID [dropdown] 20u

gm/ID [dropdown] 10

L [dropdown] 1u

VDS [dropdown] 0.45

VSB [dropdown] 0

Stack 1

Get Apply

Y-Expr w [dropdown]

Plot Replace Append

Device Parameters

#	Parameter	Value
3	W	17.47u
4	VGS	610.4m

For the cascode transistors use moderate L and bias them in MI or WI, e.g., $L = 0.5\mu\text{m}$ and $gm/ID = 15$. These transistors do not contribute significant offset and noise, so they don't need to be large. A large gm helps the gain and doesn't increase the noise.

The image displays two side-by-side screenshots of the 'ADT Sizing Assistant' window, showing the configuration of transistor parameters for a cascode transistor.

Left Screenshot:

- Temp (°C): 27.0
- State1: Save State
- ID: 20u
- gm/ID: 15
- L: .5u
- VDS: 0.45
- VSB: 0.45
- Stack: 1
- Get: Apply
- Y-Expr: w
- Plot: Replace: Append
- Device Parameters table:

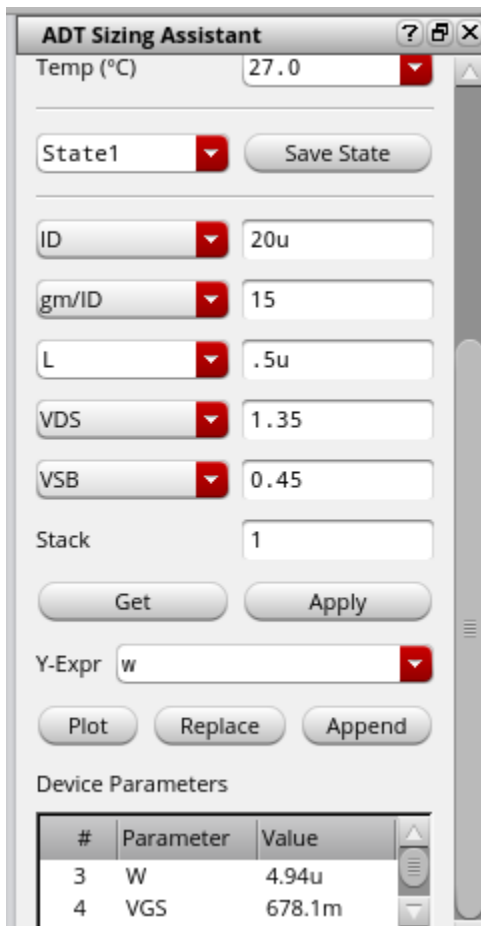
#	Parameter	Value
3	W	22.19u
4	VGS	674.4m

Right Screenshot:

- Temp (°C): 27.0
- State1: Save State
- ID: 20u
- gm/ID: 15
- L: .5u
- VDS: 0.45
- VSB: 0.45
- Stack: 1
- Get: Apply
- Y-Expr: w
- Plot: Replace: Append
- Device Parameters table:

#	Parameter	Value
3	W	4.96u
4	VGS	688.3m

-For the transistor under VBN



ADT Sizing Assistant

Temp (°C) 27.0

State1 Save State

ID 20u

gm/ID 15

L .5u

VDS 1.35

VSB 0.45

Stack 1

Get Apply

Y-Expr w

Plot Replace Append

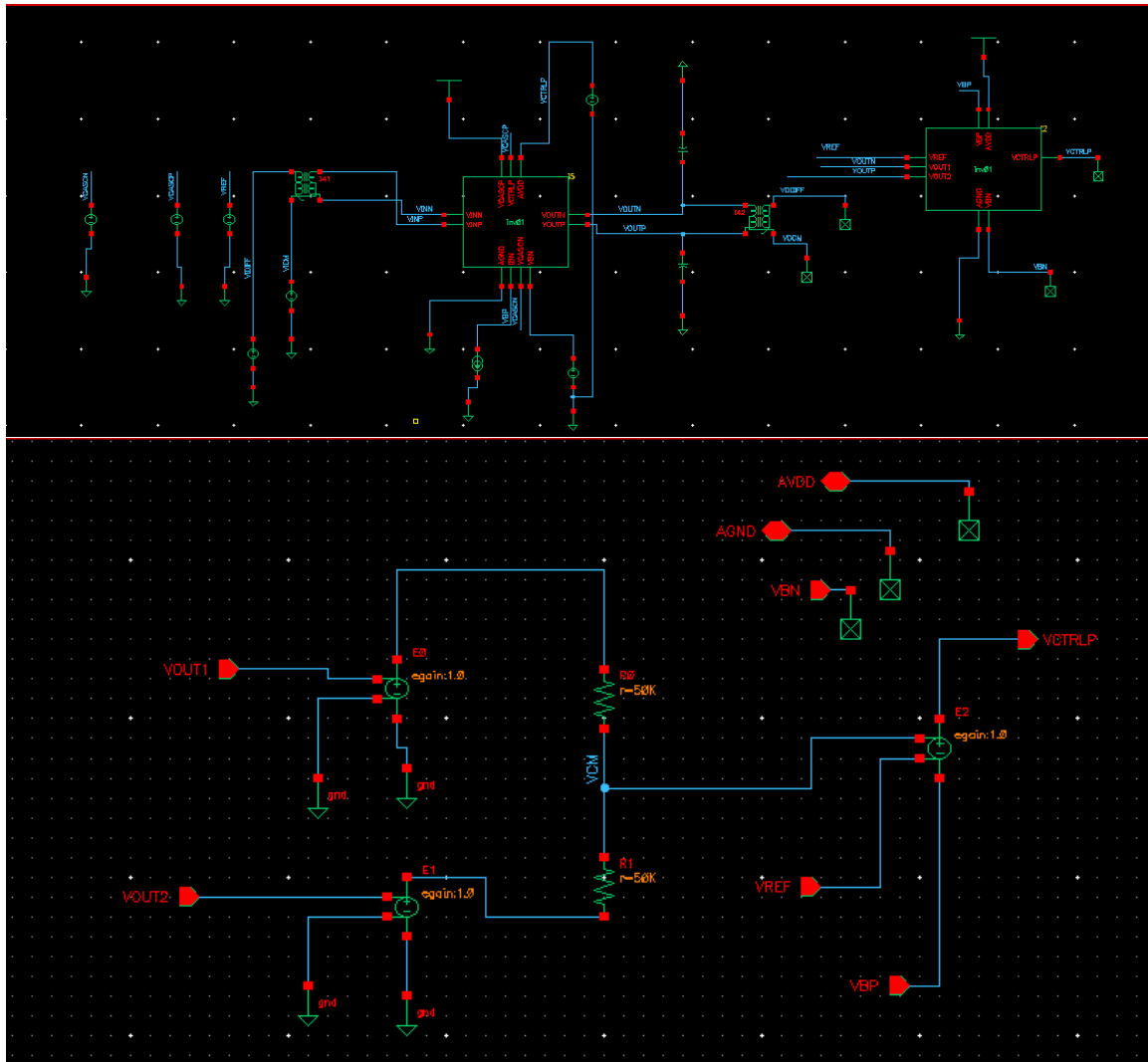
Device Parameters

#	Parameter	Value
3	W	4.94u
4	VGS	678.1m

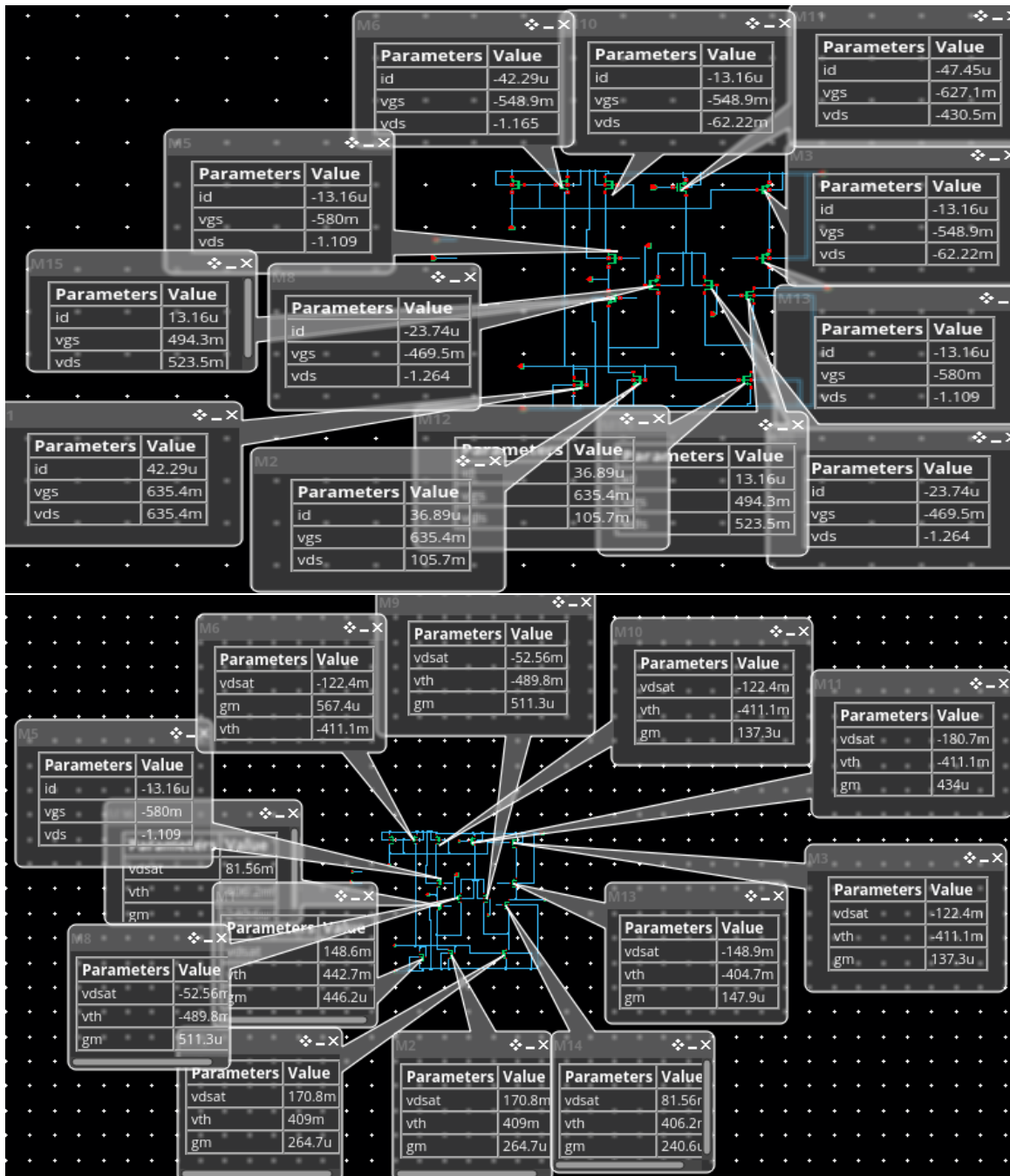
$$-VCASCN \approx VGSN + V^* = 688.3m + .1333 = .689$$

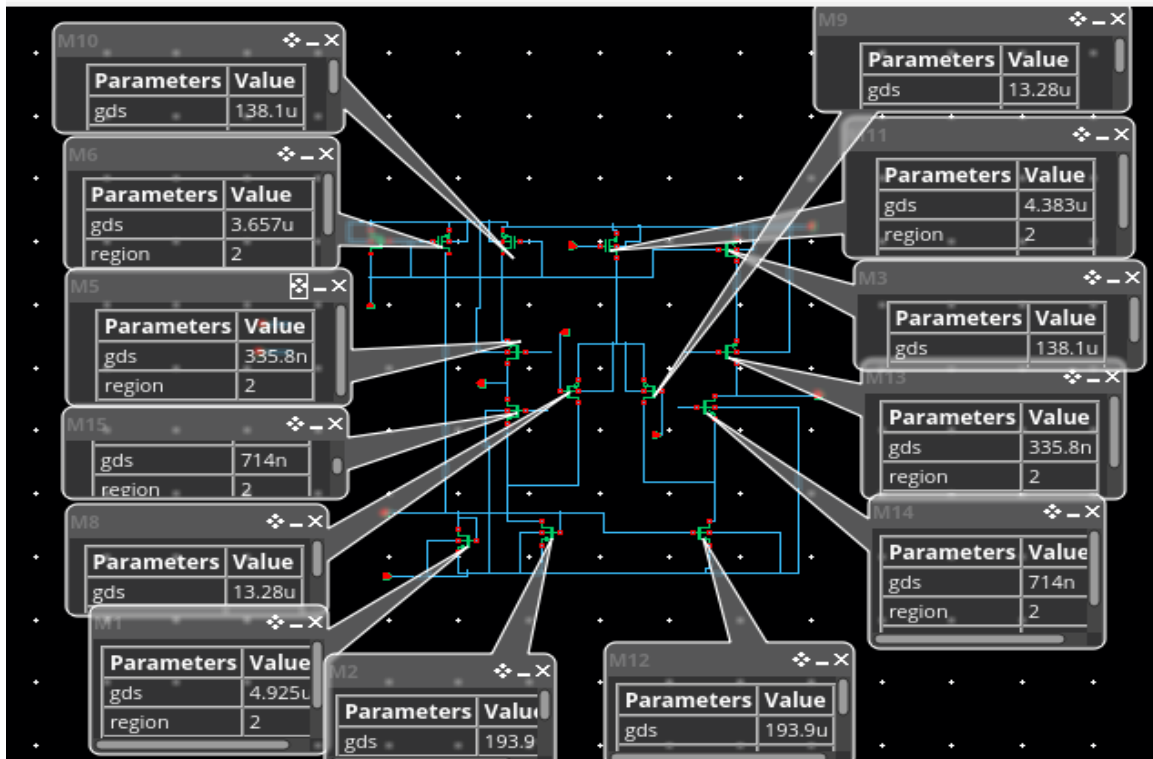
$$-VCASCP \approx VDD - |VGSP| - V^* = 1.8 - .6744 - .1333 = 1.157$$

PART 3: Open-Loop OTA Simulation (Behavioral CMFB)



1)



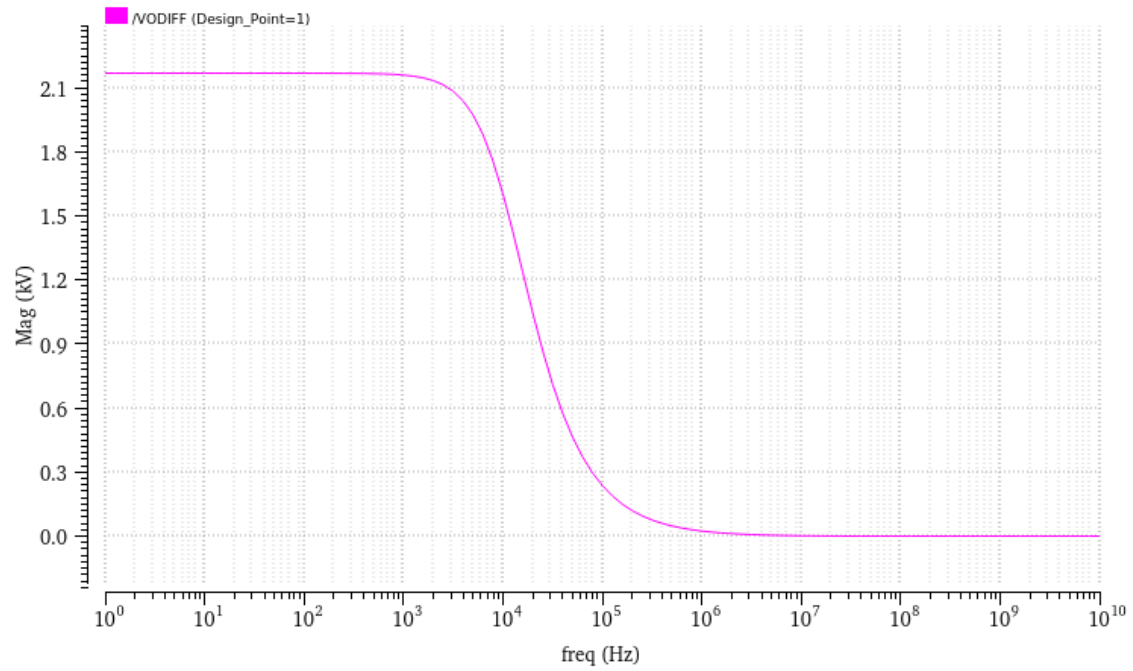


- $V_{OCM} = v_{dd} - |v_{ds1}| - |v_{ds2}| = 513\text{mv}$

2)

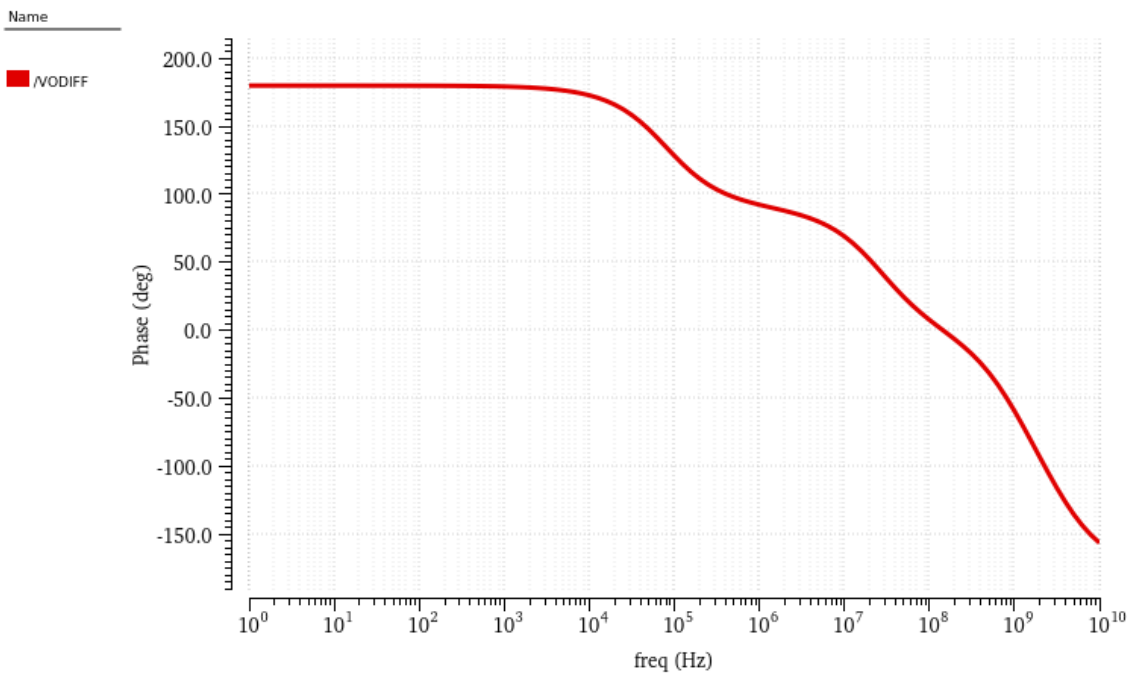
AC Response

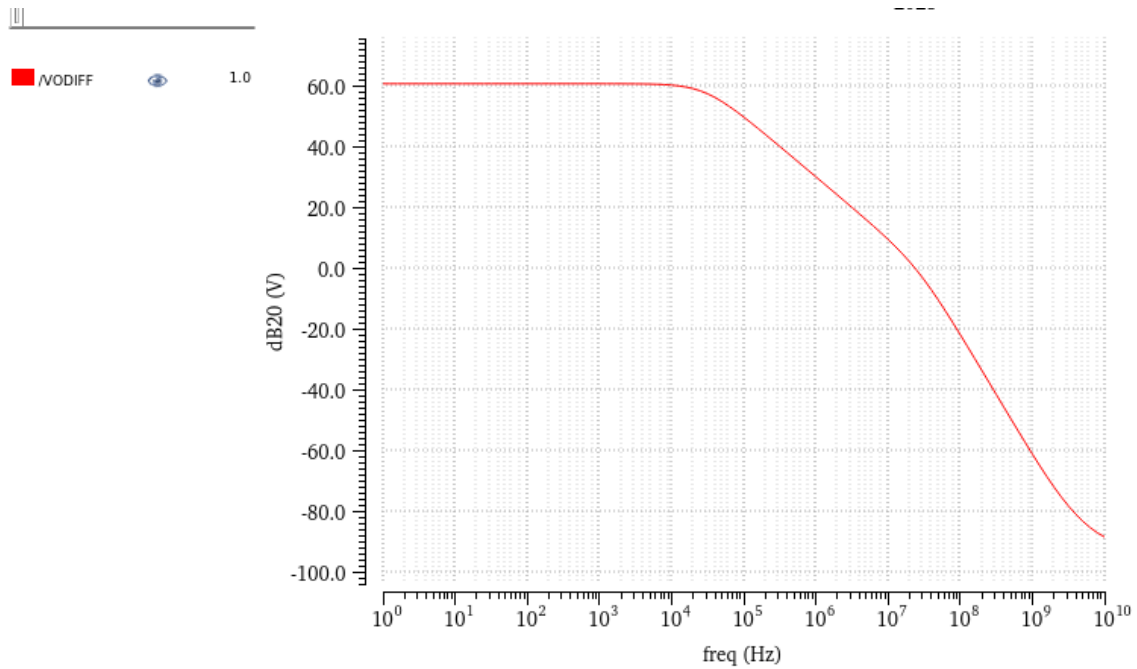
Thu Sep 21 09:57:49 2023 1



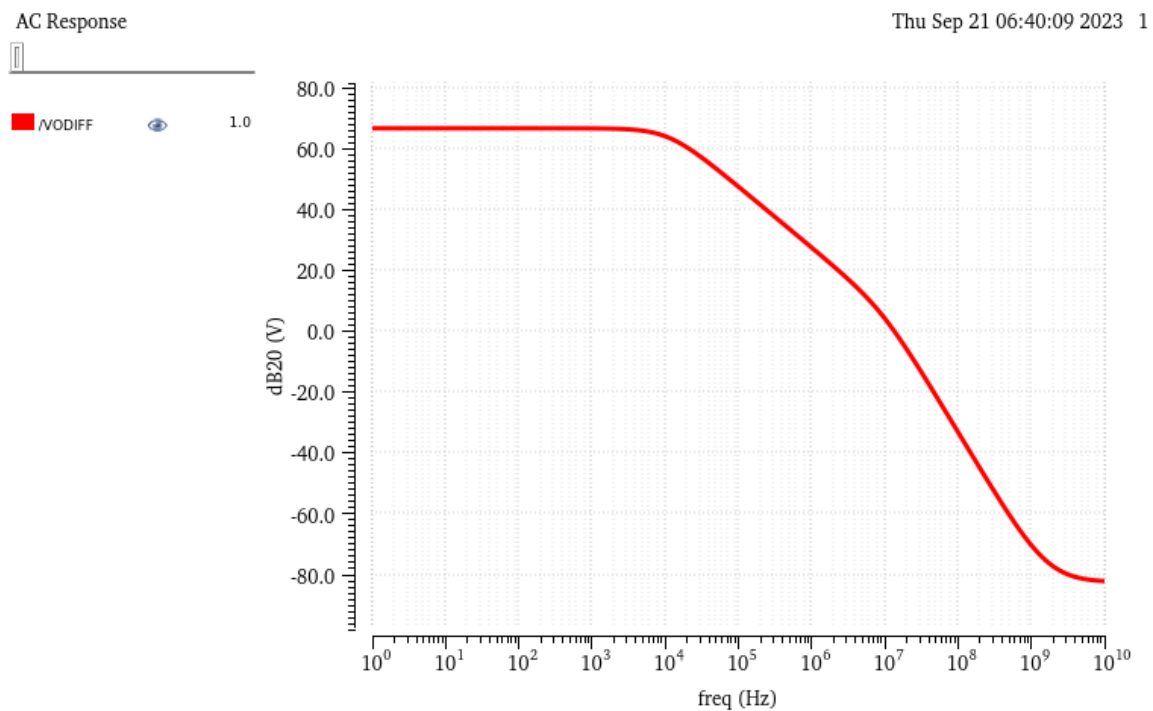
AC Response

Mon Sep 18 14:34:33 2023 1





And then to increase the gain we will raise the width of the cascade to meet the specs the new gain will be



GBW	23.92M
Fu	13.69M
BW	11.07K
Ao_dB	66.67

Gain = $-gm_0 * (gm_1 * ro^2) / 4 = 2942$,in db = 69.3 dB

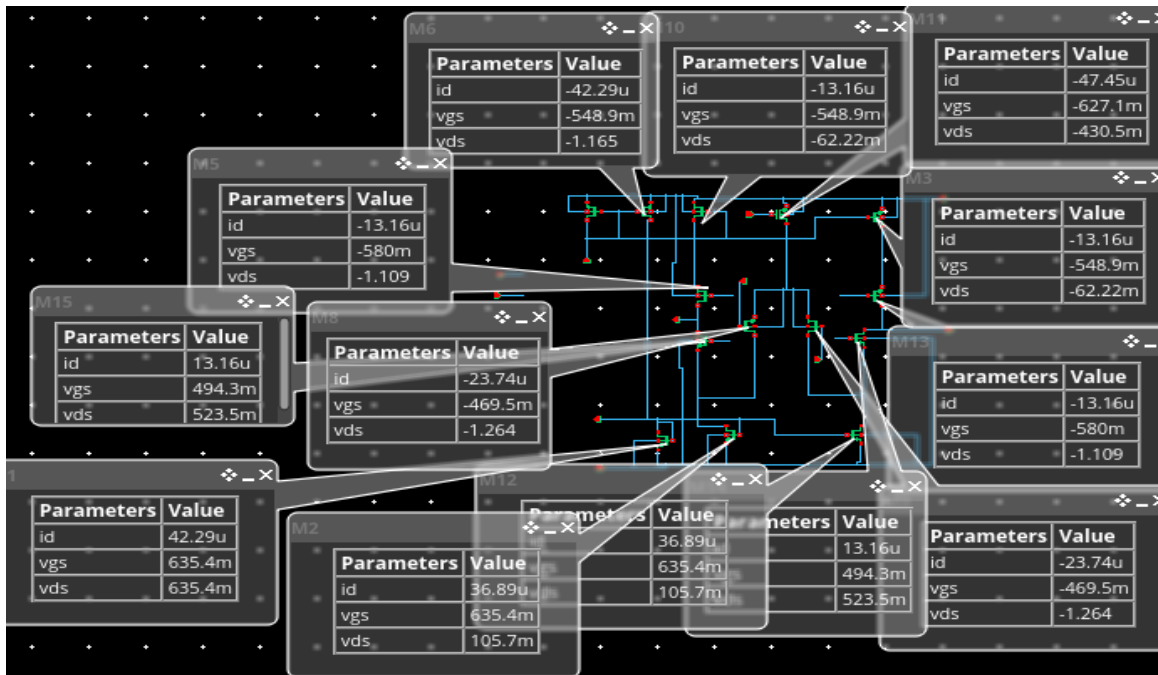
BW = $1 / Rout * C = 13$ k

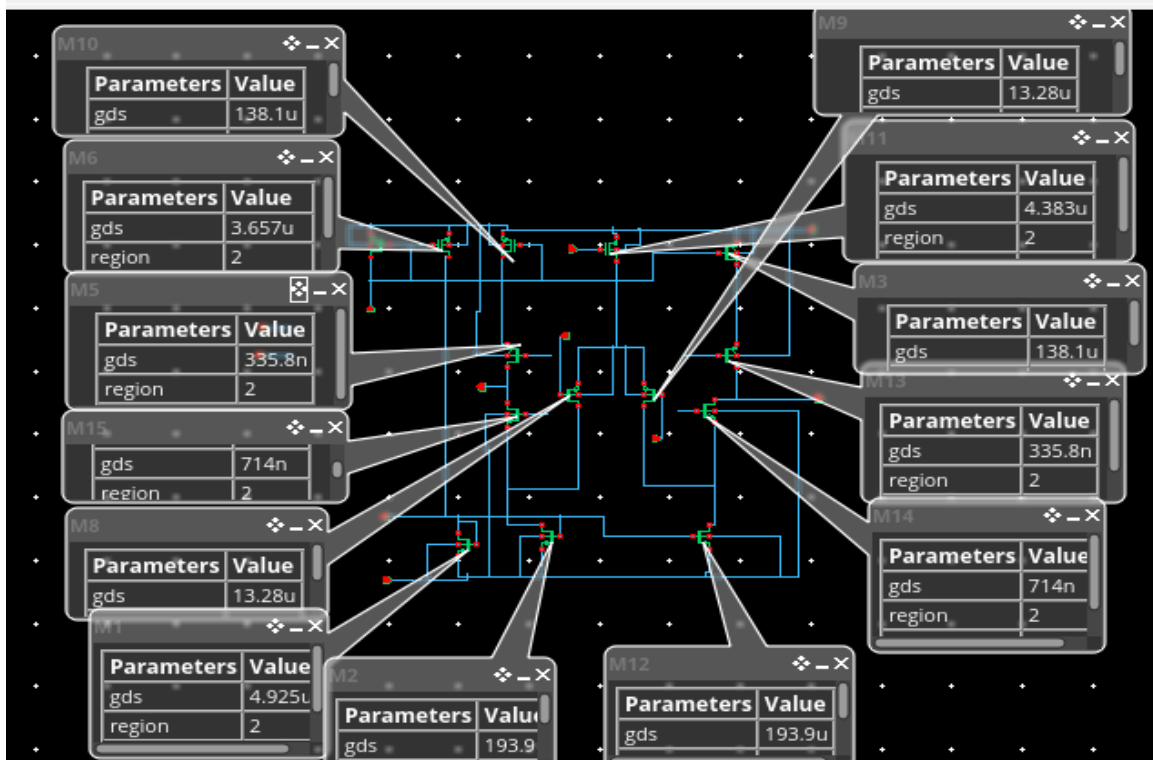
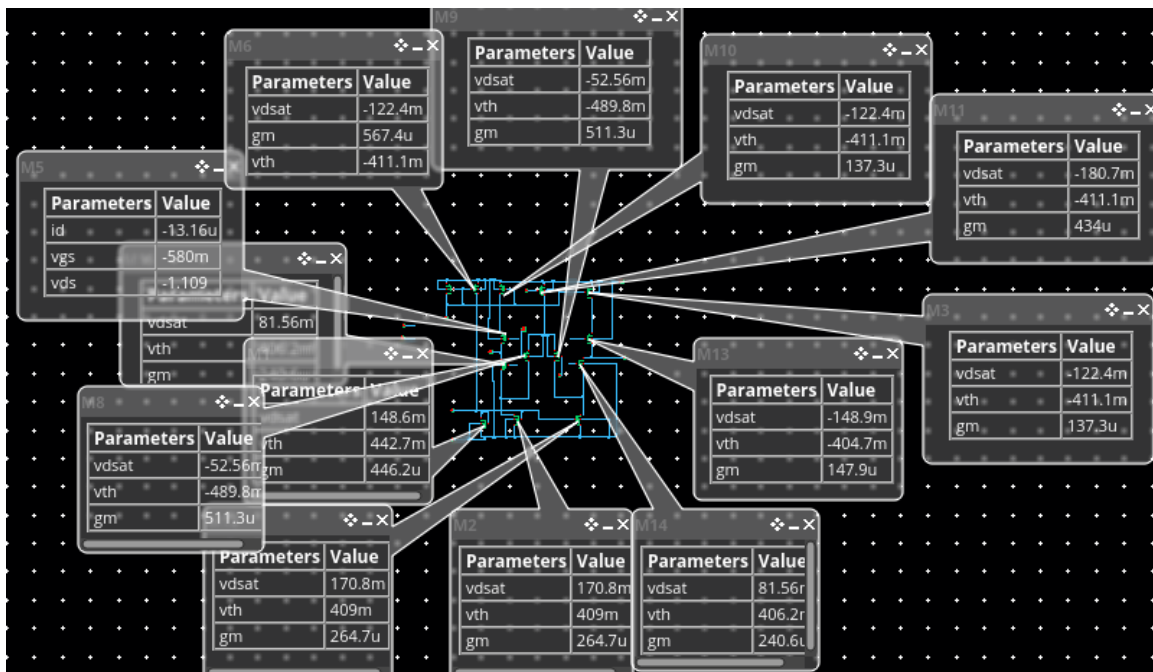
UGF=GBW = $gm_0 / Cl = 25.8$ MHz

	simulation	Hand analysis
GBW	23.92M	25.8M
Fu	13.69M	25.8M
BW	11.07K	13k
Ao_dB	66.67	69.3
A0	2450	2942

PART 4: Open-Loop OTA Simulation (Actual CMFB)

1)





-CM output = $1.8 + v_{ds1} + v_{ds2} = .628$

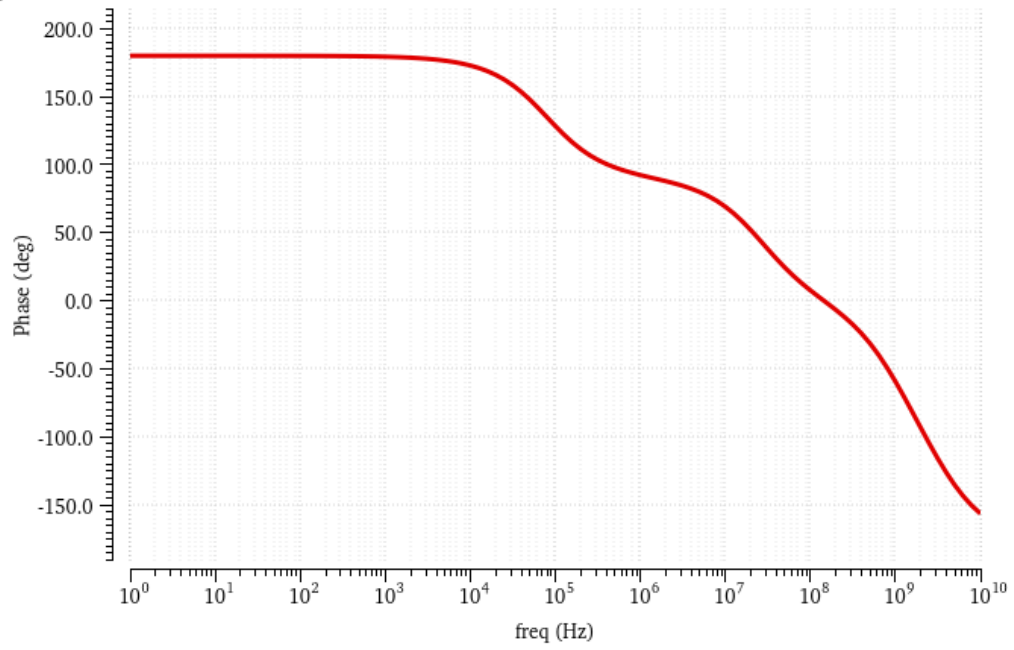
2)

AC Response

Mon Sep 18 14:34:33 2023 1

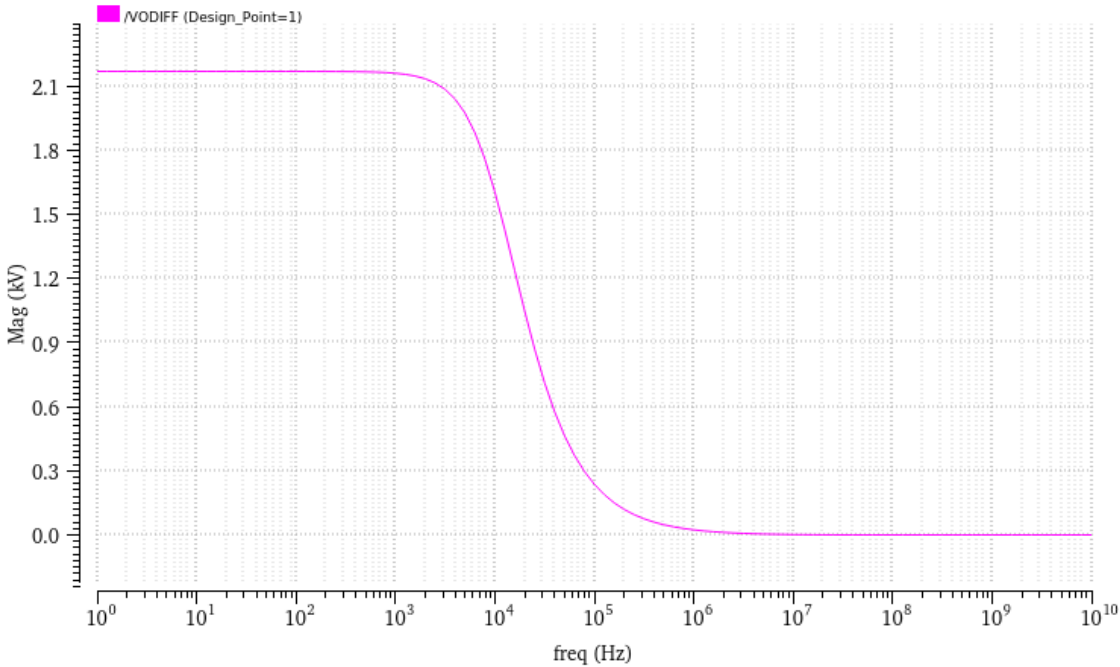
Name

■ /VODIFF



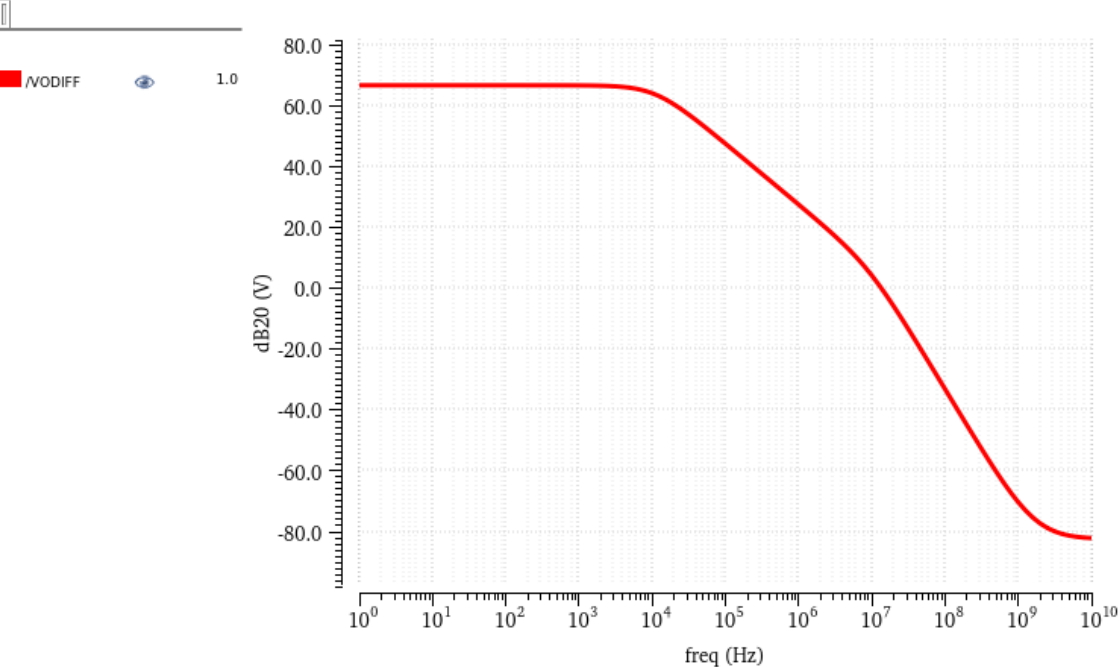
AC Response

Thu Sep 21 09:57:49 2023 1



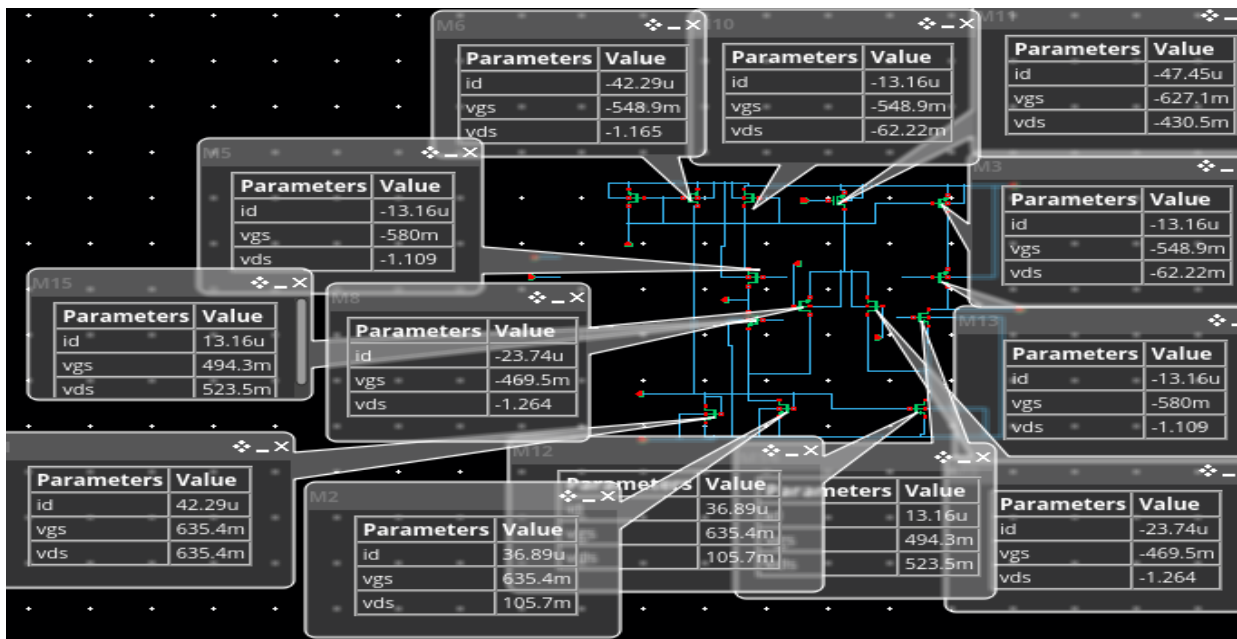
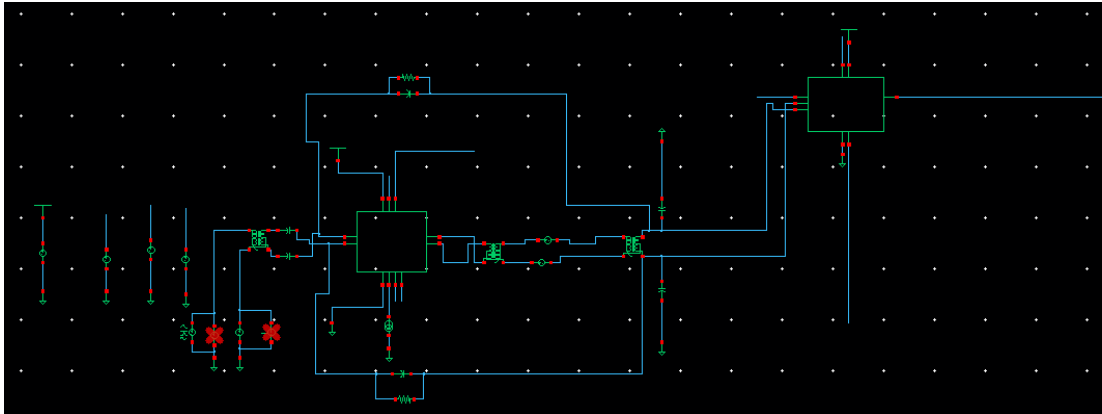
AC Response

Thu Sep 21 06:40:09 2023 1



GBW	23.92M
Fu	13.69M
BW	11.07K
PM	-146.1
Ao_dB	66.67

PART 5: Closed Loop Simulation (AC and STB Analysis)



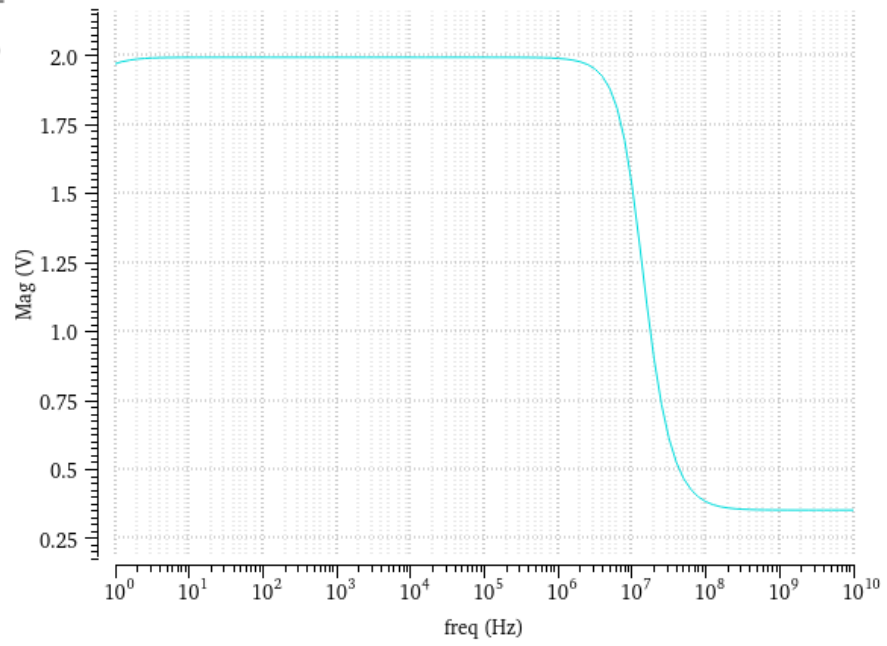
-CM level at the OTA output is 810 mV; $1.8 - V_{DS1} - V_{DS2} = 810$ m

-CM level at the OTA input is $1.8 - V_{GS} - V_{DS} = 607$ mV

2)

AC Response

Wed Sep 20 11:05:56 2023 1

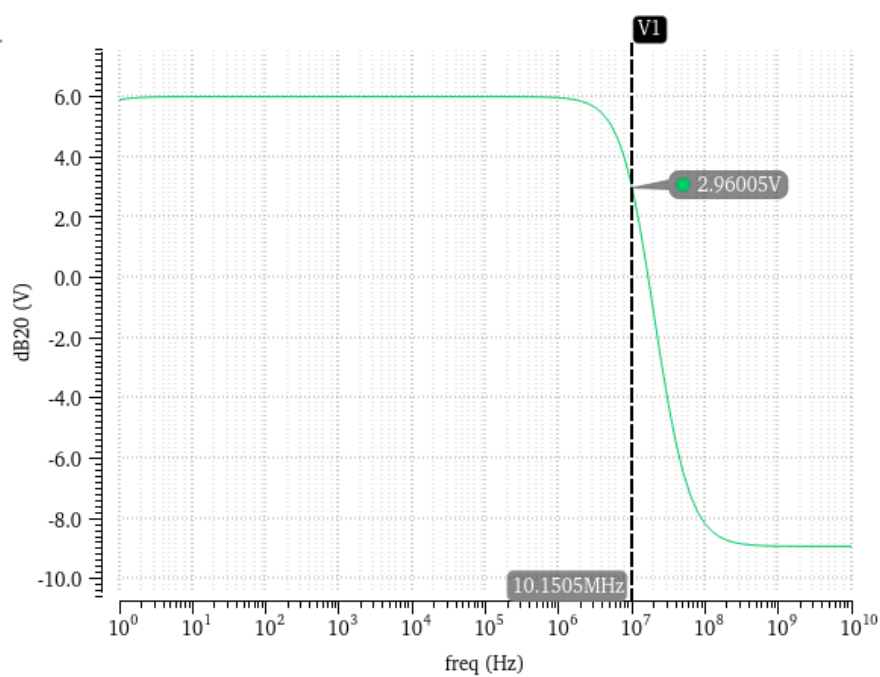


AC Response

Wed Sep 20 10:57:49 2023 1

V1

/VODIFF **...05V**

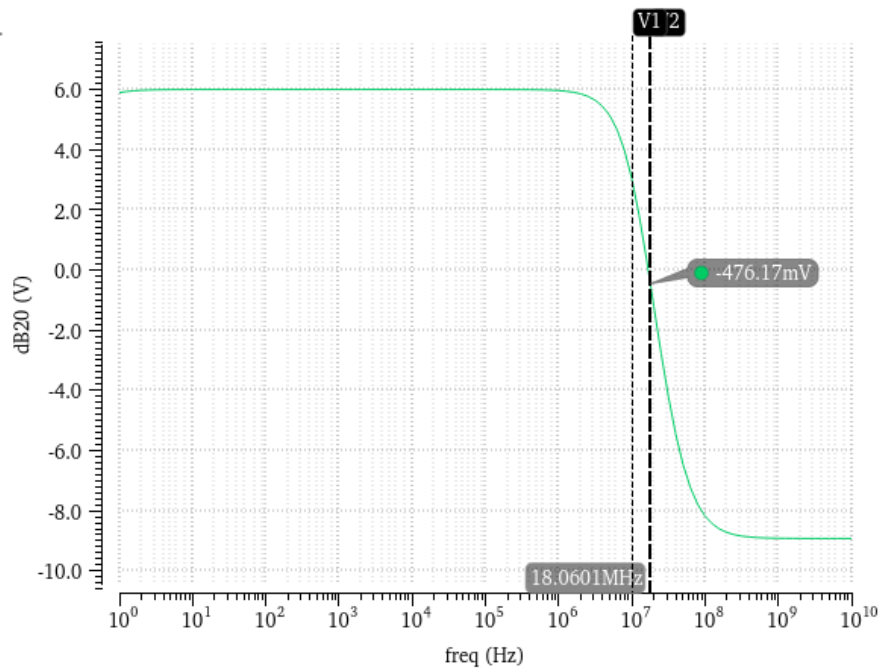


AC Response

Wed Sep 20 10:57:49 2023 1

V2

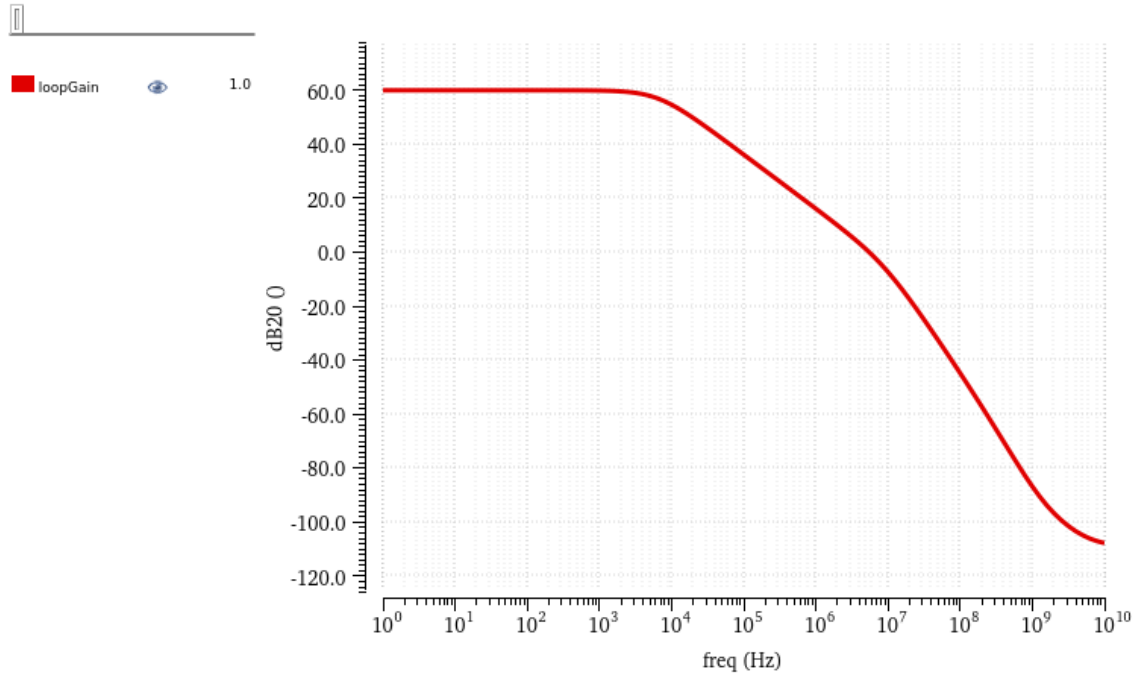
/VODIFF **...7mV**



3)

Stability Analysis `stb': freq = (1 Hz -> 10 GHz)

1

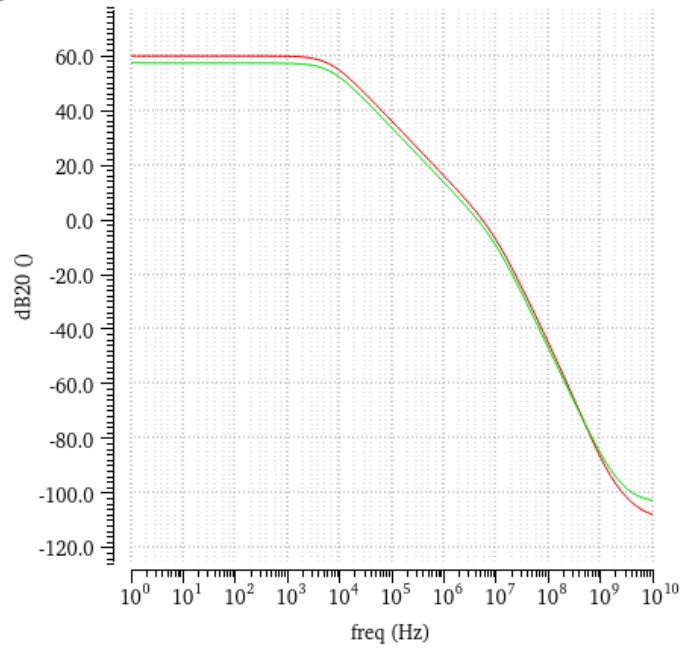


Stability Analysis `stb`: freq = (1 Hz -> 10 GHz)

1

Name	History	Design_Point
------	---------	--------------

loopGain		Interactive.40 1.0
loopGain		Interactive.43 1.0

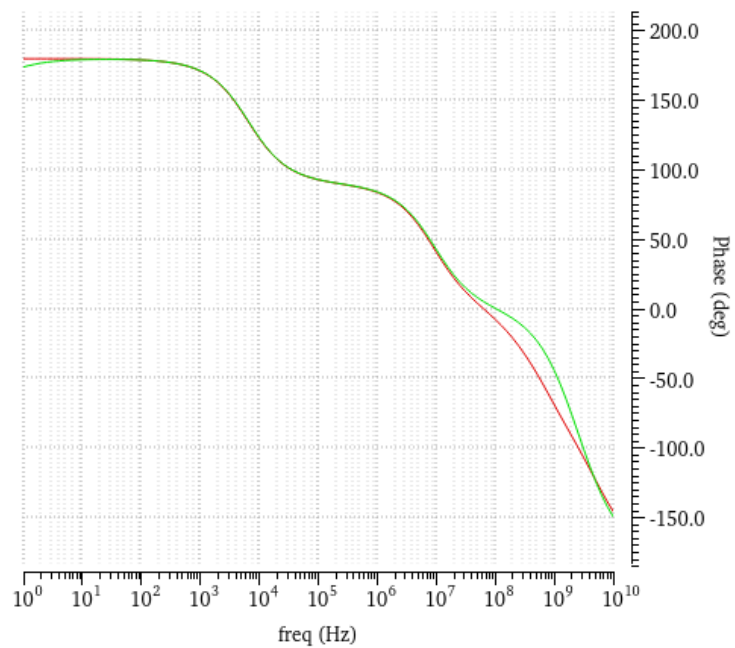


Stability Analysis `stb`: freq = (1 Hz -> 10 GHz)

1

Name	History	Design_Point
------	---------	--------------

loopGain		Interactive.40 1.0
loopGain		Interactive.43 1.0

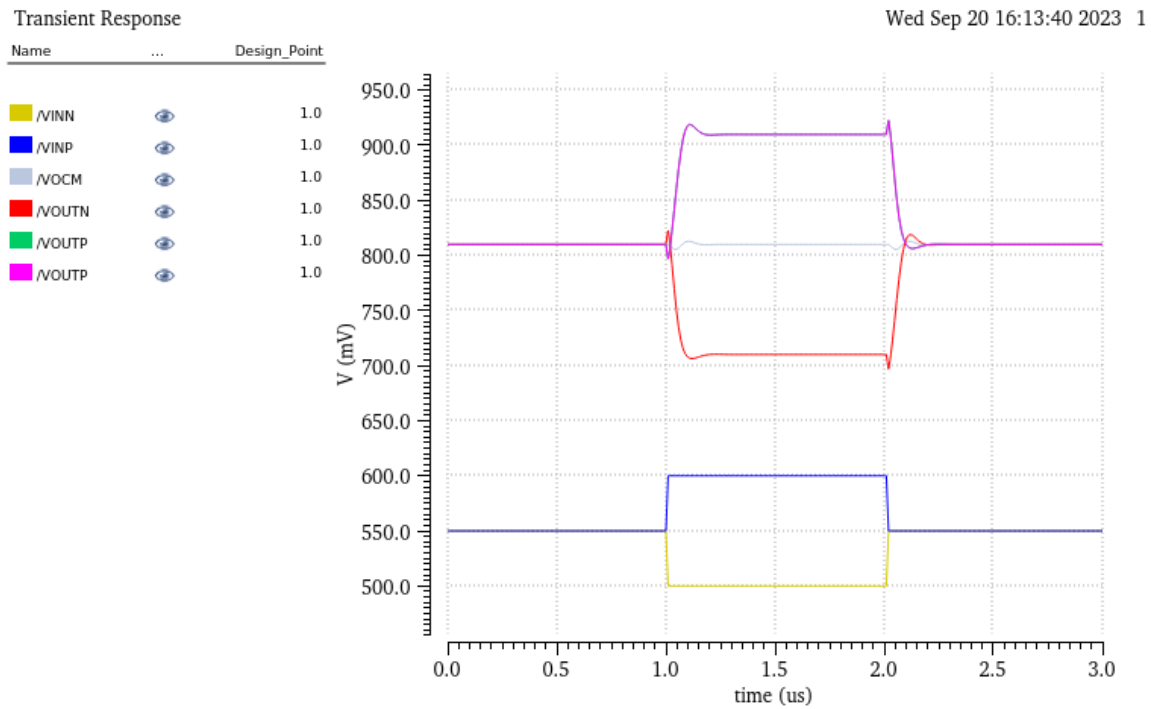


$$LG = B \cdot A_{oL} = 1/3 A_{oL}$$

$$B = Z_2 / (Z_1 + Z_2)$$

PART 6: Closed Loop Simulation (Transient Analysis)

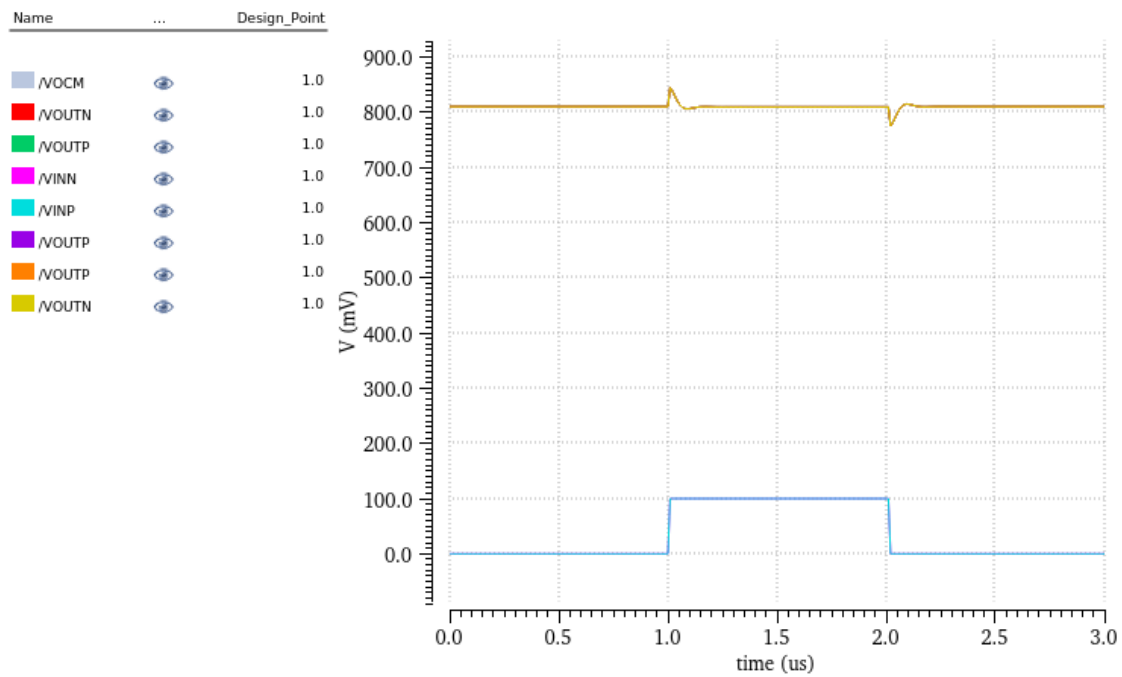
1)



There is a small ringing in the beginning and the loops are stable with adequate PM .

Transient Response

Wed Sep 20 16:24:07 2023 1

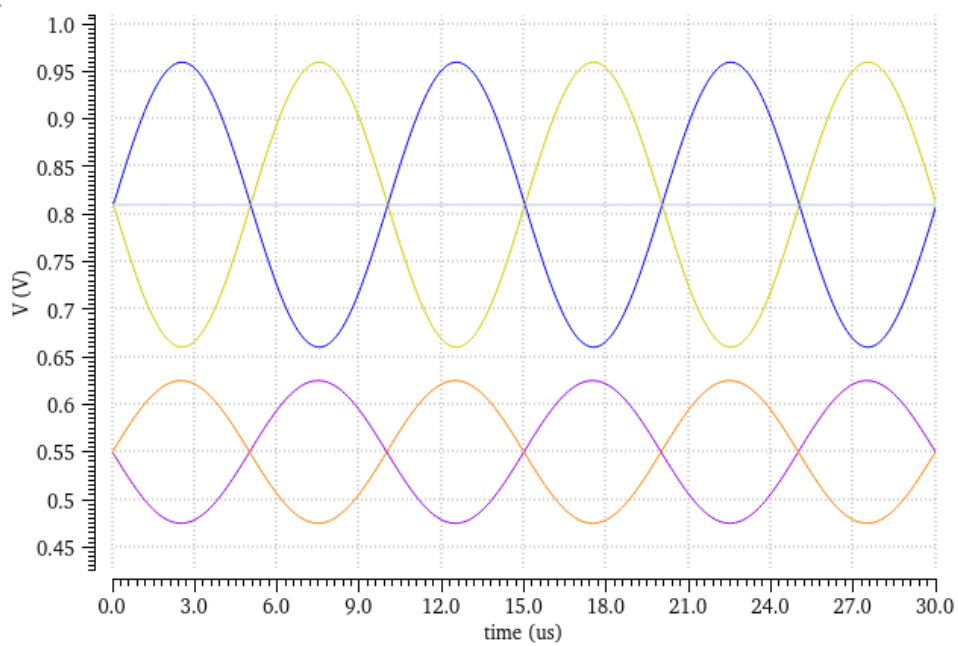


There is a small ringing in the beginning and the loops are stable with adequate PM.

2)

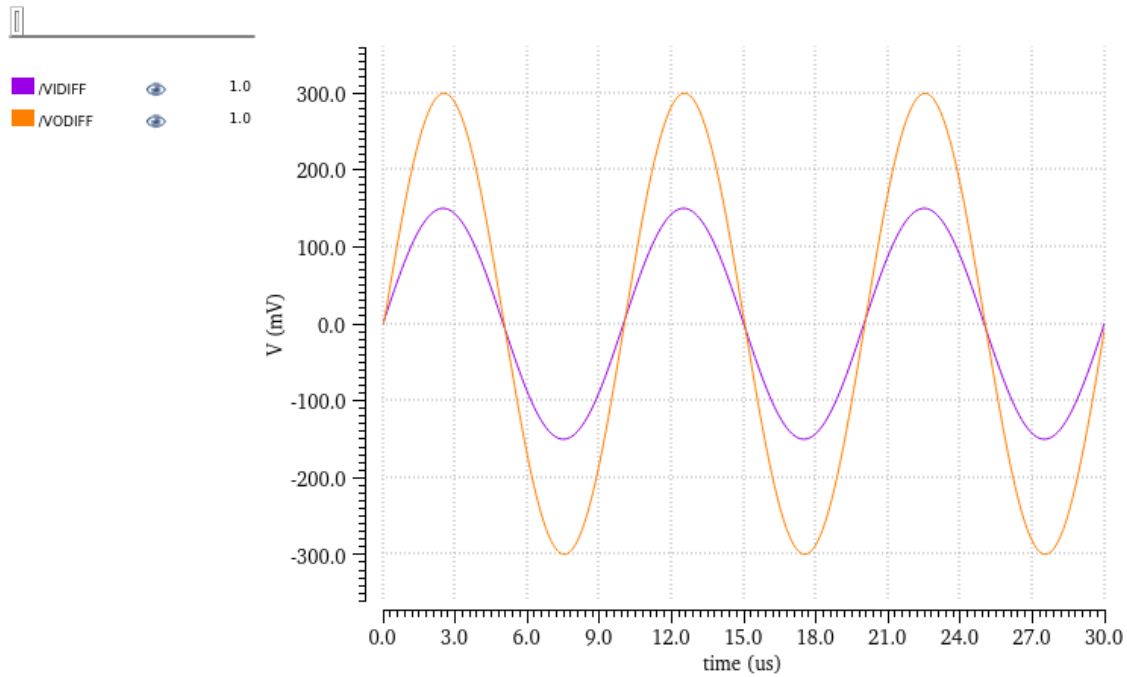


- /VINN
- /VINP
- /VOUTN
- /VOUTP
- /VOCM



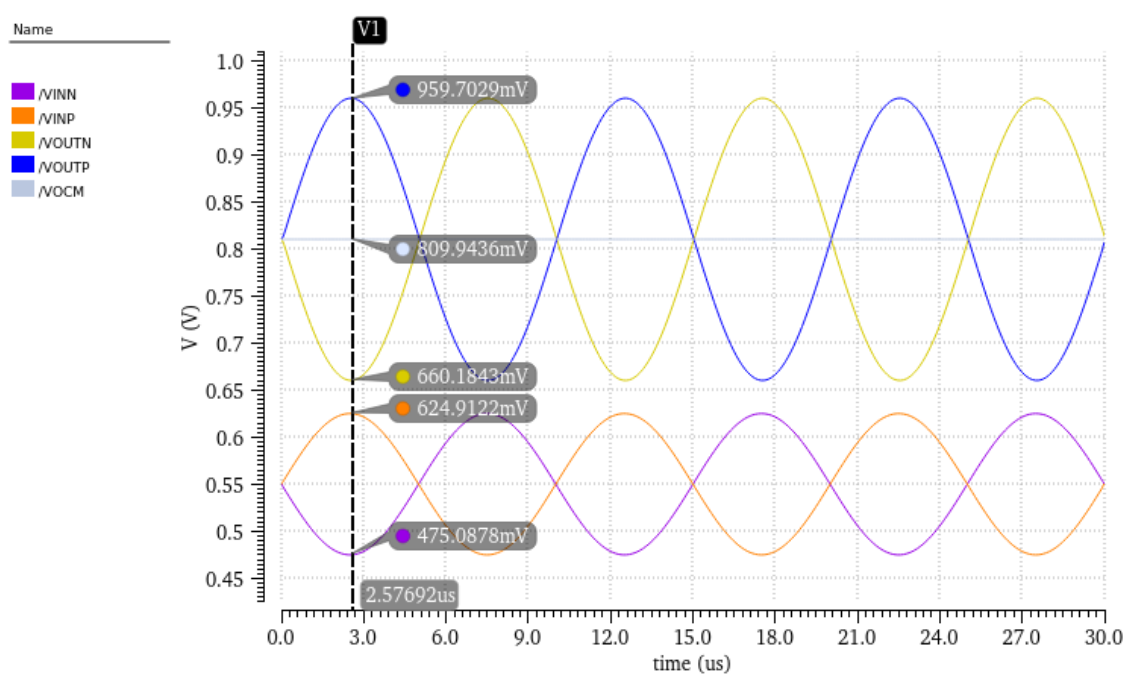
Transient Response

Wed Sep 20 16:46:31 2023 1



Transient Response

Thu Sep 21 08:30:11 2023 1



input peak to peak swing = $625\text{m} - 475\text{m} = 150\text{m}$ v

Output peak to peak swing = $(960\text{m} - 660\text{m}) = 300\text{mv}$

Closed loop gain = $(960\text{m} - 660\text{m}) / (625\text{m} - 475\text{m}) = 2$.

	Expression	Value	Expression	Value
1	gainBwProd(leaf...	4.800E6	phaseMargin(le...	180.0
	Expression	Value	Expression	Value
1	phaseMargin(le...	180.0	gainBwProd(leaf...	6.450E6