به نام خدا

UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department

Computer Assignment 2

Digital Systems I - ECE 894

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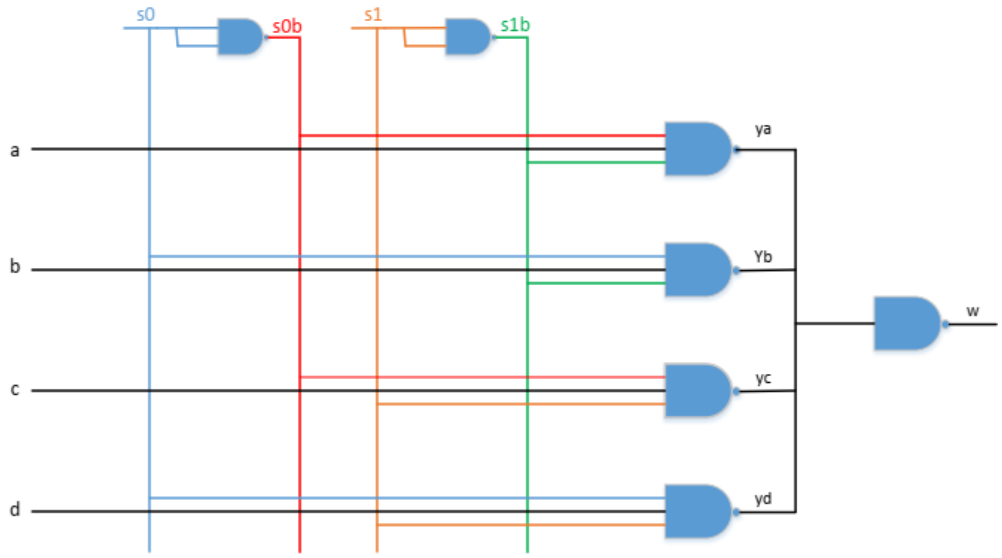
Spring 1400

List of Problems:.

Computer Assignment 2

Problem 1. File: MUX4to1.sv

A. **Circuit diagram:** According to Part 3 of CA1, We use this Circuit to write the description of 4-to-1 MUX. (Using 'assign')



B. **Worst-cases:** The worst cases in Part 3 of CA1 was:

Gate-Level: To1 = 42ns , To0=39ns

Transistor-Level: To1 = 32ns , To0=31ns

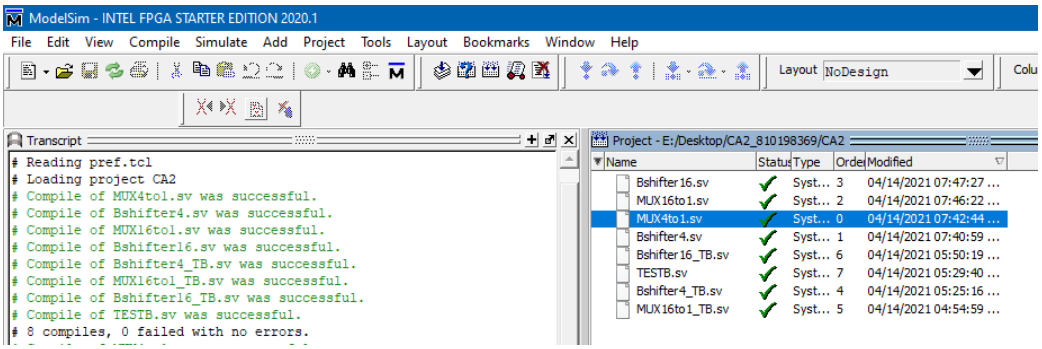
We use Gate-Level worst cases to write the 4-to-1 MUX module.

C. **System Verilog Descrioption:**

File: MUX4to1.sv

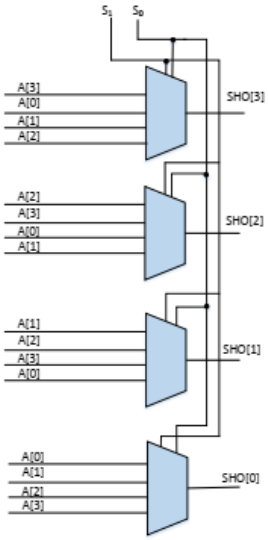
```
`timescale 1ns/1ns
module MUX4to1(input [3:0]A,[1:0]N,output w);
   assign #(42,39) w = ~ ( ~ ( A[0] & ~N[0] & ~N[1] )
                         & ~ ( A[1] & N[0] & ~N[1] )
                         & ~ ( A[2] & ~N[0] & N[1] )
                         & ~ ( A[3] & N[0] & N[1] ) );
Endmodule
```

D. Image of project and compiling:



Problem 2. Files: Bshifter4.sv – Bshifter4_TB.sv

A. Circuit diagram: The circuit for 4-bit barrel shifter is shown here:



B. Worst-cases:

All MUXs are parallel. So we can say that the worst case happens when worst case of a MUX happens. The greatest delay of a MUX is 42 (for output=1). So the worst case for the given circuit happens when one digit of input [0:3] input is 1. We expect the worst case delay would be 42ns.

$A = 0101\,, \qquad N = 00 \rightarrow N = 01$

$$\Longrightarrow Delay = \boldsymbol{To1\ (4-to-1\ MUX)} = 42ns\ (worst\ case)$$

C. System Verilog Descrioption:

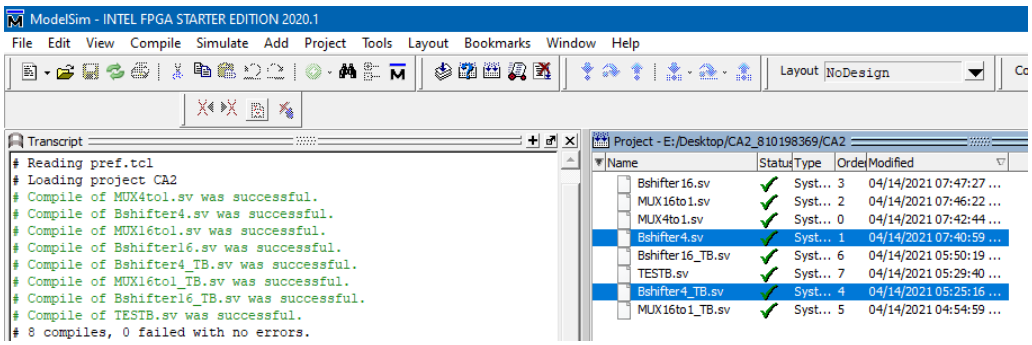
File: Bshifter4.sv

```
`timescale 1ns/1ns
module Bshifter4(input [3:0]A,[1:0]N,output [3:0]SHO);
	MUX4to1 G1({A[2],A[1],A[0],A[3]},N,SHO[3]);
	MUX4to1 G2({A[1],A[0],A[3],A[2]},N,SHO[2]);
	MUX4to1 G3({A[0],A[3],A[2],A[1]},N,SHO[1]);
	MUX4to1 G4({A[3],A[2],A[1],A[0]},N,SHO[0]);
endmodule
```

File: Bshifter4_TB.sv

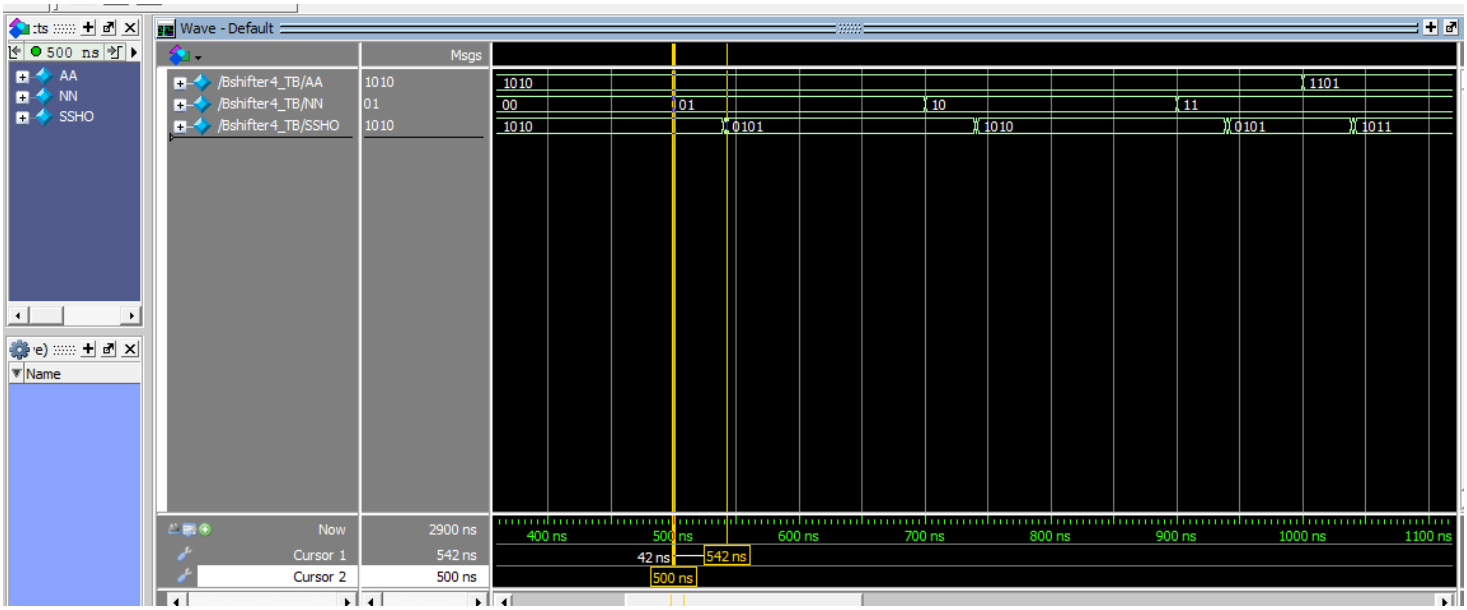
```
`timescale 1ns/1ns
module Bshifter4_TB();
	logic [3:0]AA;
	logic [1:0]NN;
	wire [3:0]SSHO;
	Bshifter4 R(AA,NN,SSHO);
	initial begin
		#100 AA=4'b1010;
		#200 NN=2'b00;
		#200 NN=2'b01;
		#200 NN=2'b10;
		#200 NN=2'b11;
		#200 AA=4'b1101;
		#200 NN=2'b11;
		#200 NN=2'b10;
		#200 NN=2'b01;
		#200 NN=2'b00;
		#200 AA=4'b0001;
		#200 NN=2'b00;
		#200 NN=2'b01;
		#200 NN=2'b10;
		#200 NN=2'b11;
		#200;
	end
endmodule
```

D. Image of project and compiling:



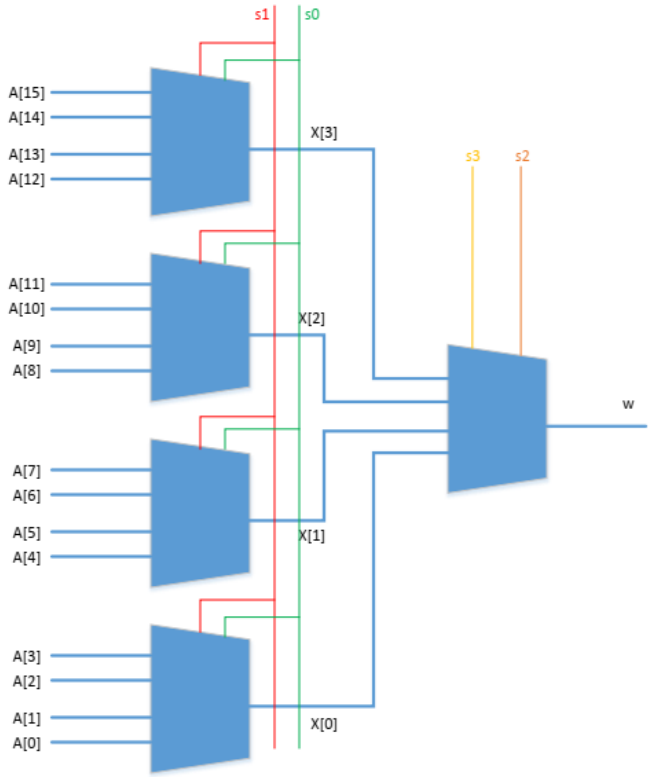
E. **Waveform:** worst case is shown on the waveform.

As expected worst case is 42ns on the waveform:



Problem 3. Files: MUX16to1.sv – MUX16to1_TB.sv

A. **Circuit diagram:** The circuit for 16-to-1 MUX is shown here:



B. Worst-cases:

a) Worst case to 1:

Worst case to 1 happens when both MUXs (drives to 0 and) after the change drives to 1. So we expect the worst case to 1 delay would be 84ns.

$A = 1011011110111011, \quad N = 1110 \rightarrow N = 1111$

$$\Longrightarrow Delay = \mathbf{2} \times \boldsymbol{To1} = 2 \times 42 = 84ns \ (worst\ case\ to\ 1)$$

b) Worst case to 0:

Worst case to 0 happens when after the change first MUX drives to 1 and the last MUX drives to 0. But actually the last MUX drives 0 sooner and delay of MUX that drives to 1 is not important. So we expect the worst case to 1 delay would be 78ns.

$A = 1011011110111011\,, \quad N = 1111 \rightarrow N = 1110$

$$\Longrightarrow Delay = \mathbf{2} \times \boldsymbol{To0} = 2 \times 39 = 78ns \ (worst\ case\ to\ 0)$$

C. System Verilog Descrioption:

File: MUX16to1.sv

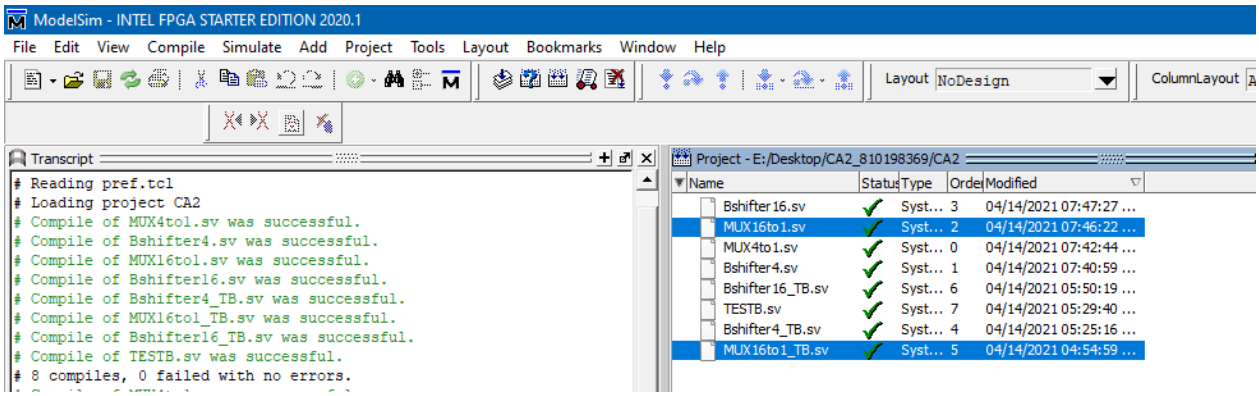
```
`timescale 1ns/1ns

module MUX16to1(input [15:0]A,[3:0]N,output w);
     wire [3:0]x;
     MUX4to1 g1({A[15],A[14],A[13],A[12]},{N[1],N[0]},x[3]);
     MUX4to1 g2({A[11],A[10],A[9],A[8]},{N[1],N[0]},x[2]);
     MUX4to1 g3({A[7],A[6],A[5],A[4]},{N[1],N[0]},x[1]);
     MUX4to1 g4({A[3],A[2],A[1],A[0]},{N[1],N[0]},x[0]);
     MUX4to1 g5(x,{N[3],N[2]},w);
endmodule
```

File: MUX16to1_TB.sv

```
`timescale 1ns/1ns
module MUX16to1_TB();
logic [15:0]AA;
logic [3:0]NN;
wire ww;
     MUX16to1 R(AA,NN,ww);
```

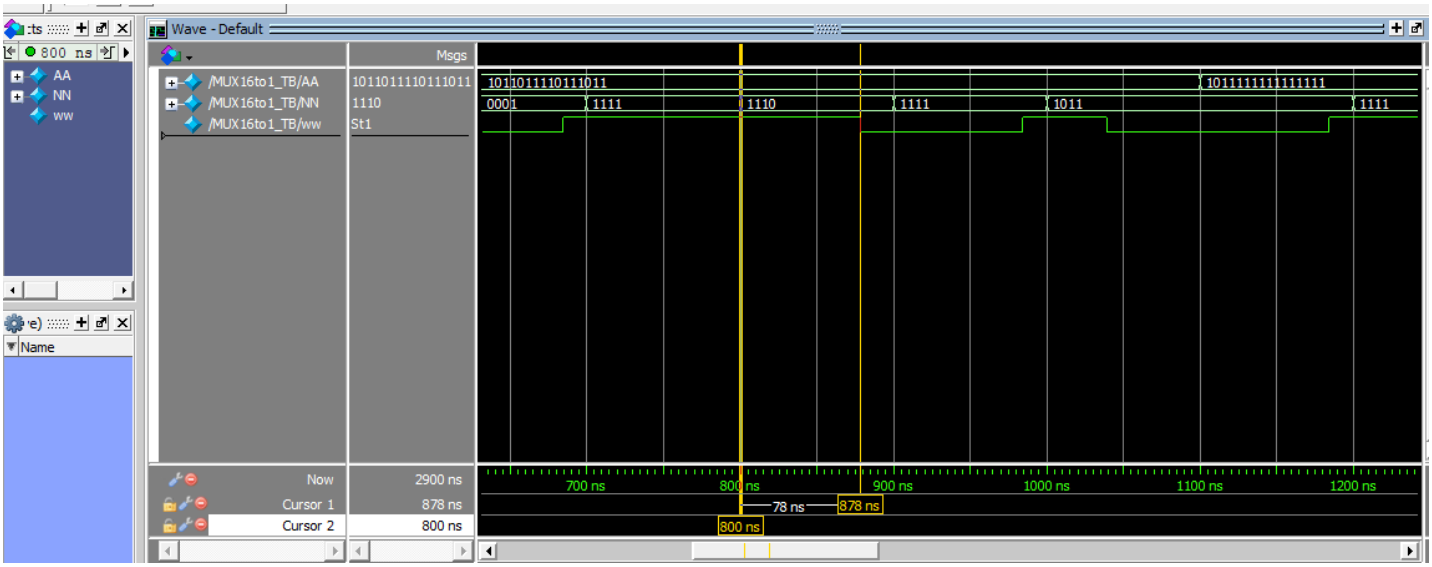
```
        initial begin
            #100 AA=16'b0101010101010101;
            #100 NN=4'd3;
            #100 NN=4'd2;
            #100 NN=4'd0;
            #100 NN=4'd1;
            #100 AA=16'b1011011110111011;
            #100 NN=4'b1111;
            #100 NN=4'b1110;
            #100 NN=4'b1111;
            #100 NN=4'b1011;
            #100 AA=16'b1011111111111111;
            #100 NN=4'b1111;
            #100 NN=4'b1110;
            #100 NN=4'b1100;
            #100 NN=4'b1110;
            #100 AA=16'd1038;
            #100 NN=4'b0000;
            #100 NN=4'b0001;
            #100 NN=4'b0011;
            #100 NN=4'b0111;
            #100 NN=4'b1111;
            #100 AA=16'd21;
            #100 NN=4'd0;
            #100 NN=4'd1;
            #100 NN=4'd2;
            #100 NN=4'd3;
            #100 NN=4'd4;
            #100 NN=4'd5;
            #100;
        end
    endmodule
```

D. Image of project and compiling:

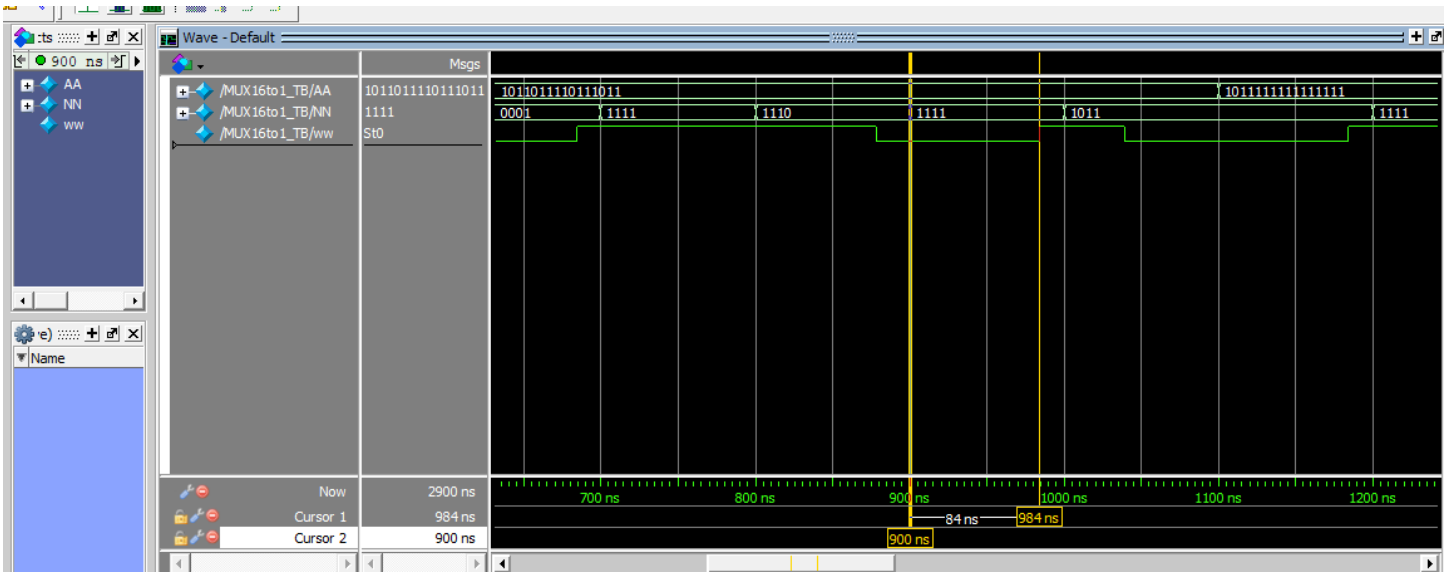


E. **Waveform:** worst case is shown on the waveform (next page).

a) As expected worst case to 0 is 78ns on the waveform:



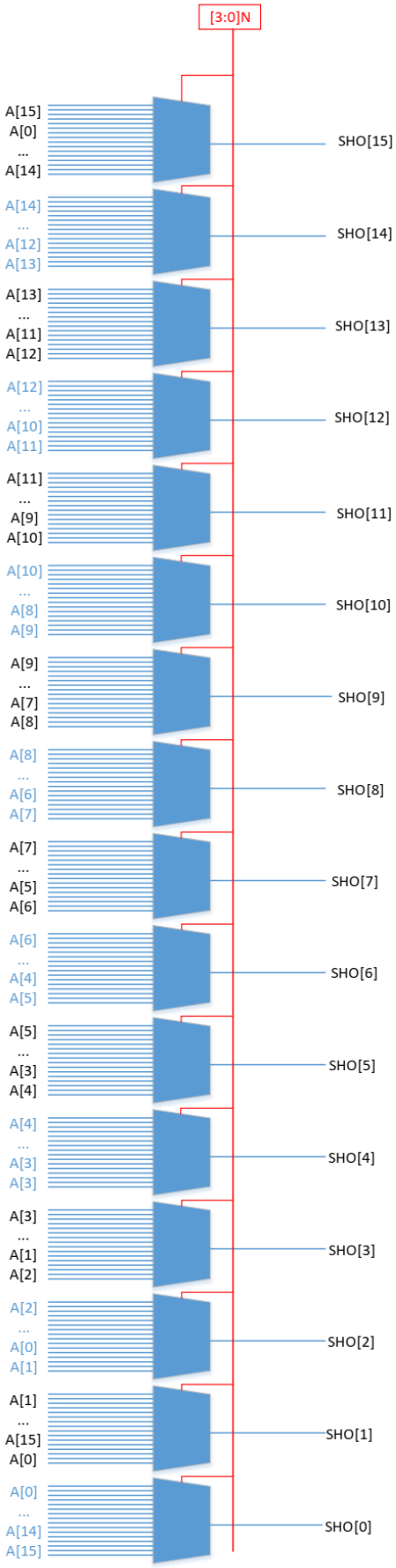
b) As expected worst case to 1 is 84ns on the waveform:



Problem 4. Files: Bshifter16.sv – Bshifter16_TB.sv

A. **Circuit diagram:** The circuit for 16-bit barrel shifter (Using 16-to-1 MUX) is shown in the next page:

(Blocks are 16-to-1 MUX)


[3:0]N
A[15]
A[0]
...
A[14]
SHO[15]
A[14]
...
A[12]
A[13]
SHO[14]
A[13]
...
A[11]
A[12]
SHO[13]
A[12]
...
A[10]
A[11]
SHO[12]
A[11]
...
A[9]
A[10]
SHO[11]
A[10]
...
A[8]
A[9]
SHO[10]
A[9]
...
A[7]
A[8]
SHO[9]
A[8]
...
A[6]
A[7]
SHO[8]
A[7]
...
A[5]
A[6]
SHO[7]
A[6]
...
A[4]
A[5]
SHO[6]
A[5]
...
A[3]
A[4]
SHO[5]
A[4]
...
A[3]
A[3]
SHO[4]
A[3]
...
A[1]
A[2]
SHO[3]
A[2]
...
A[0]
A[1]
SHO[2]
A[1]
...
A[15]
A[0]
SHO[1]
A[0]
...
A[14]
A[15]
SHO[0]

B. Worst-cases:

All MUXs are parallel. So we can say that the worst case happens when worst case of a MUX happens. The greatest delay of a MUX is 84 (worst case to 1 , according to Part3). So the worst case for the given circuit happens when one digit of input [0:3] input is 1. We expect the worst case delay would be 84ns.

$A = 0000\ 0000\ 0000\ 0001\ ,\qquad N = 0000 \rightarrow N = 0001$

$$\Longrightarrow Delay = \boldsymbol{To1\ (16 - to - 1\ MUX)} = 84ns\ (worst\ case)$$

C. System Verilog Descrioption:

File: Bshifter16.sv

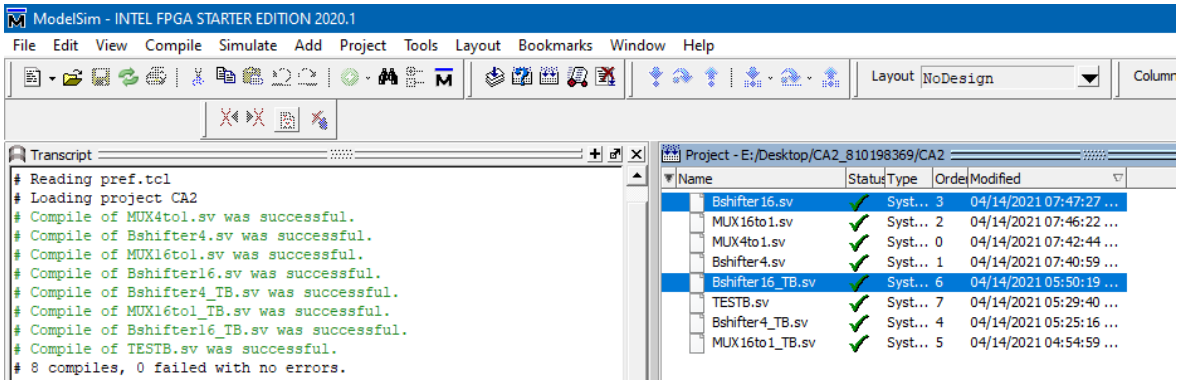
```
`timescale 1ns/1ns
module Bshifter16(input [15:0]A,[3:0]N,output [15:0]SHO);
MUX16to1 G1({A[14],A[13],A[12],A[11],A[10],A[9],A[8],A[7],A[6],A[5],A[4],A[3],A[2],A[1],A[0],A[15]},N,SHO[15]);
MUX16to1 G2({A[13],A[12],A[11],A[10],A[9],A[8],A[7],A[6],A[5],A[4],A[3],A[2],A[1],A[0],A[15],A[14]},N,SHO[14]);
MUX16to1 G3({A[12],A[11],A[10],A[9],A[8],A[7],A[6],A[5],A[4],A[3],A[2],A[1],A[0],A[15],A[14],A[13]},N,SHO[13]);
MUX16to1 G4({A[11],A[10],A[9],A[8],A[7],A[6],A[5],A[4],A[3],A[2],A[1],A[0],A[15],A[14],A[13],A[12]},N,SHO[12]);
MUX16to1 G5({A[10],A[9],A[8],A[7],A[6],A[5],A[4],A[3],A[2],A[1],A[0],A[15],A[14],A[13],A[12],A[11]},N,SHO[11]);
MUX16to1 G6({A[9],A[8],A[7],A[6],A[5],A[4],A[3],A[2],A[1],A[0],A[15],A[14],A[13],A[12],A[11],A[10]},N,SHO[10]);
MUX16to1 G7({A[8],A[7],A[6],A[5],A[4],A[3],A[2],A[1],A[0],A[15],A[14],A[13],A[12],A[11],A[10],A[9]},N,SHO[9]);
MUX16to1 G8({A[7],A[6],A[5],A[4],A[3],A[2],A[1],A[0],A[15],A[14],A[13],A[12],A[11],A[10],A[9],A[8]},N,SHO[8]);
MUX16to1 G9({A[6],A[5],A[4],A[3],A[2],A[1],A[0],A[15],A[14],A[13],A[12],A[11],A[10],A[9],A[8],A[7]},N,SHO[7]);
MUX16to1 G10({A[5],A[4],A[3],A[2],A[1],A[0],A[15],A[14],A[13],A[12],A[11],A[10],A[9],A[8],A[7],A[6]},N,SHO[6]);
MUX16to1 G11({A[4],A[3],A[2],A[1],A[0],A[15],A[14],A[13],A[12],A[11],A[10],A[9],A[8],A[7],A[6],A[5]},N,SHO[5]);
MUX16to1 G12({A[3],A[2],A[1],A[0],A[15],A[14],A[13],A[12],A[11],A[10],A[9],A[8],A[7],A[6],A[5],A[4]},N,SHO[4]);
MUX16to1 G13({A[2],A[1],A[0],A[15],A[14],A[13],A[12],A[11],A[10],A[9],A[8],A[7],A[6],A[5],A[4],A[3]},N,SHO[3]);
MUX16to1 G14({A[1],A[0],A[15],A[14],A[13],A[12],A[11],A[10],A[9],A[8],A[7],A[6],A[5],A[4],A[3],A[2]},N,SHO[2]);
MUX16to1 G15({A[0],A[15],A[14],A[13],A[12],A[11],A[10],A[9],A[8],A[7],A[6],A[5],A[4],A[3],A[2],A[1]},N,SHO[1]);
MUX16to1 G16({A[15],A[14],A[13],A[12],A[11],A[10],A[9],A[8],A[7],A[6],A[5],A[4],A[3],A[2],A[1],A[0]},N,SHO[0]);
endmodule
```

File: Bshifter16_TB.sv

```
`timescale 1ns/1ns
module Bshifter16_TB();
	logic [15:0]AA;
	logic [3:0]NN;
	wire [15:0]SSHO;
	Bshifter16 R(AA,NN,SSHO);
	initial begin
		AA=16'b0000000000000001;
		#100 NN=4'b0000;
		#100 NN=4'b0001;
		#100 NN=4'b0011;
		#100 NN=4'b0111;
		#100 NN=4'b1111;
		#100 AA=16'b0101010101010101;
		#100 NN=4'd3;
```

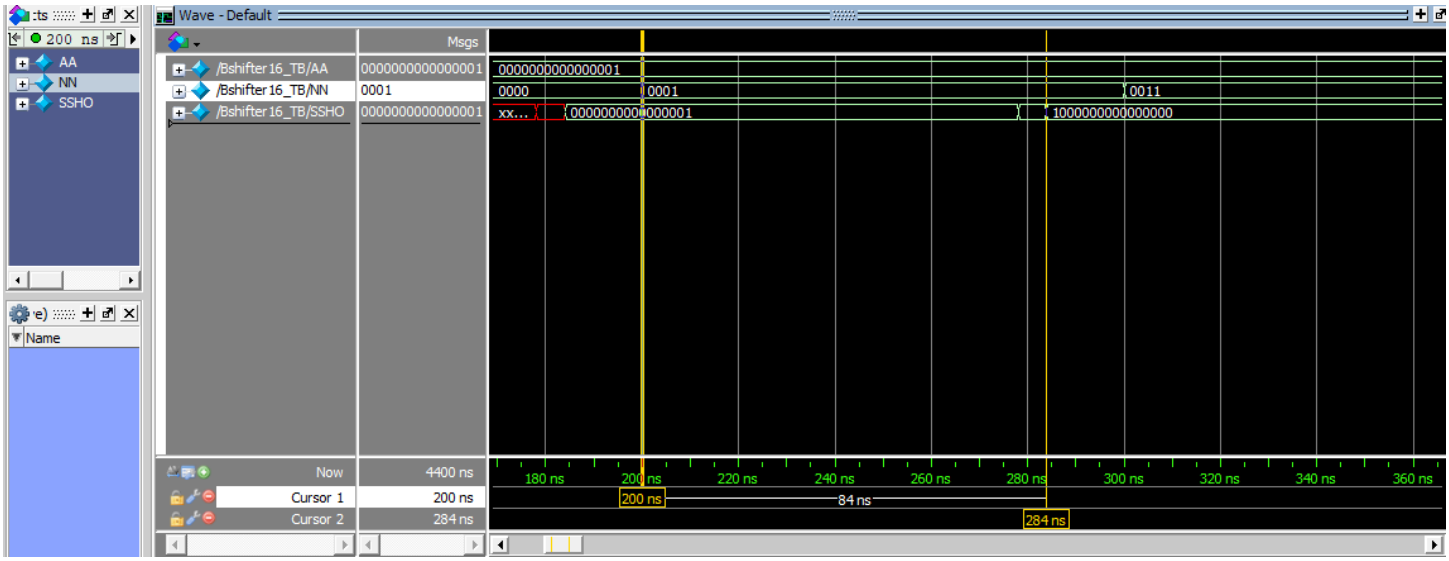
```
        #100 NN=4'd2;
        #100 NN=4'd0;
        #100 NN=4'd1;
        #100 AA=16'b1011011110111011;
        #100 NN=4'b1111;
        #100 NN=4'b1110;
        #100 NN=4'b1111;
        #100 NN=4'b1011;
        #100 AA=16'b1011111111111111;
        #100 NN=4'b1111;
        #100 NN=4'b1110;
        #100 NN=4'b1100;
        #100 NN=4'b1110;
        #100 AA=16'd1038;
        #100 NN=4'b0000;
        #100 NN=4'b0001;
        #100 NN=4'b0011;
        #100 NN=4'b0111;
        #100 NN=4'b1111;
        #100 AA=16'd21;
        #100 NN=4'd0;
        #100 NN=4'd1;
        #100 NN=4'd2;
        #100 NN=4'd3;
        #100 NN=4'd4;
        #100 NN=4'd5;
        #100;
        #1000;
    end
endmodule
```

D. Image of project and compiling:



A. Waveform: worst case is shown on the waveform (next page).

As expected worst case is 84ns on the waveform:


Wave - Default
Msgs
/Bshifter16_TB/AA
/Bshifter16_TB/NN
/Bshifter16_TB/SSHO
0000000000000001
0001
0000000000000001
0000
0001
0011
xx...
0000000000000001
1000000000000000
Now
4400 ns
Cursor 1
200 ns
Cursor 2
284 ns
180 ns
200 ns
220 ns
240 ns
260 ns
280 ns
300 ns
320 ns
340 ns
360 ns
84 ns
Name