

Experiment 1 - Clock and Periodic Signal Generation

Digital Logic Design Lab - Fall 2022

Erfan Panahi
ID: 810198369

Sogol Goodarzi
ID: 810198467

CLOCK GENERATION USING ICs AND ANALOG COMPONENTS

INTRODUCTION

The goal of this experiment is to introduce the concepts of static characteristics of digital logic gates, delay times, clock frequency generation and digital system using schematic diagram and Verilog HDL.

By the end of this experiment, you should have learned:

- Power supply, Function Generator, and Oscilloscope
- 74 Series Basic Logic Gates
- Different oscillator circuits (a LM555 timer IC, Schmitt trigger Oscillator)
- Sequential circuits using clocks and counters

I. RING OSCILLATOR

Question 1. Measure the propagation delay of the chain by measuring the period time of the output.

We calculate the period time of the output using the frequency that is shown in Fig.1 .

$$Frequency = 35.87\text{kHz} \quad (1)$$

$$F = 35.87\text{MHz} \rightarrow T = \frac{1}{F} = 0.0279 \times 10^{-6} = 27.9\text{ns}$$

$$T = 27.9\text{ns} \quad (2)$$

Question 2. Calculate the delay of a single inverter and report this time.

As we see in Fig. 2, a ring oscillator is composed of a chain of odd number of inverters, in which output of last inverter is connected to the input of first one. It can be easily seen that adding more inverters to the chain increases the total gate delay. The time at which a value feeds back to the same node is the time period of the ring oscillator which equals $2N \times t_d$, where N is the odd number and t_d is the delay of each inverter gate. The delay of each single inverter can be determined by measuring the total delay.

$$T = 2N \times t_d \rightarrow t_d = \frac{T}{2N} = \frac{27.9\text{ns}}{10} = 2.79\text{ns} \quad (3)$$

$$t_d = 2.79\text{ns} \quad (3)$$



Fig. 1. Ring-Oscillator waveform, as we see: $F = 35.87\text{kHz}$

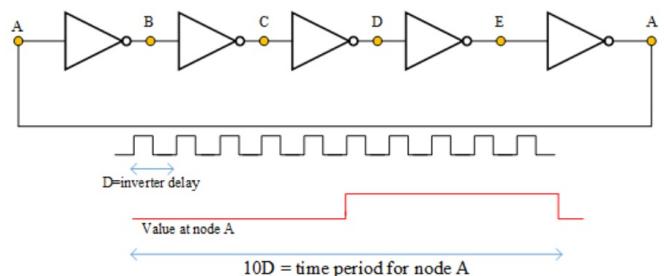


Fig. 2. Ring Oscillator

II. LM555 TIMER

Question 1. Implement the LM555 in astable mode using the wiring diagram from Fig. 3. and observe the output. Report the clock frequency and the duty cycle and include the waveform of the output in your report.

As we see in Fig. 4, for $R_2 = 50k\Omega$:

$$Frequency = 1.300\text{kHz} \quad (4)$$

$$Duty - Cycle = 49.5\% \quad (5)$$

Question 2. Change the value of R_2 resistors to produce different clock frequencies. To do so, R_2 should be $1k\Omega$,

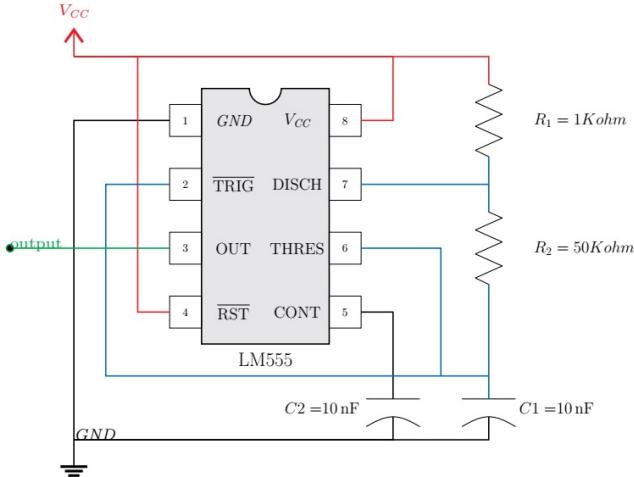


Fig. 3. LM555 in astable mode



Fig. 4. Output waveform of LM555 in astable mode with $R_2 = 50k\Omega$

10kΩ and 100kΩ. Calculate the frequency and duty cycle using above equations and compare them to the clock signal you see on the output.

As we read in the "Experiment1 Instruction", the external capacitor C_1 charges through $R_1 + R_2$ and discharges through R_2 . Thus, the duty cycle and frequency may be precisely set by selecting the right combination of resistances and capacitance. So the charge time (output high) is given by $T_1 = 0.693(R_1 + R_2)C_1$ and the discharge time (output low) by $T_2 = 0.693R_2C_1$. Thus, the total time period of square wave is $T = T_1 + T_2 = 0.693(R_1 + 2R_2)C_1$. Consequently, the frequency of oscillation is $f = 1/T$. The duty cycle also can be computed by $\frac{R_1+R_2}{R_1+2R_2}$.

$$f = \frac{1}{T} = \frac{1}{0.693(R_1 + 2R_2)C_1} \quad (6)$$

$$\text{Duty - Cycle} = \frac{R_1 + R_2}{R_1 + 2R_2} \quad (7)$$

Now, we calculate the frequency and duty-cycle for each value of resistors (R_1 , R_2) and capacitor (C_1). Then we compare them with the observation that we see on the output waveform.

- $R_2 = 1k\Omega$:

At first, we calculate the frequency and duty cycle like equation above.

$$f = \frac{1}{0.693(3 \times 10^3)10^{-8}} = 48.1kHz \quad (8)$$

$$\text{Duty - Cycle} = \frac{10^3 + 10^3}{10^3 + 2 \times 10^3} = 66.6\% \quad (9)$$

According to Fig. 5, the observed frequency and duty-cycle for this value of R_2 is:

$$f = 38.76kHz \quad (10)$$

$$\text{Duty - Cycle} = 65.9\% \quad (11)$$



Fig. 5. Output waveform of LM555 in astable mode with $R_2 = 1k\Omega$

- $R_2 = 10k\Omega$:

At first, we calculate the frequency and duty cycle like equation above.

$$f = \frac{1}{0.693(21 \times 10^3)10^{-8}} = 6.871kHz \quad (12)$$

$$\text{Duty - Cycle} = \frac{10^3 + 10 \times 10^3}{10^3 + 20 \times 10^3} = 52.38\% \quad (13)$$

According to Fig. 6, the observed frequency and duty-cycle for this value of R_2 is:

$$f = 6.088kHz \quad (14)$$

$$\text{Duty - Cycle} = 51.8\% \quad (15)$$

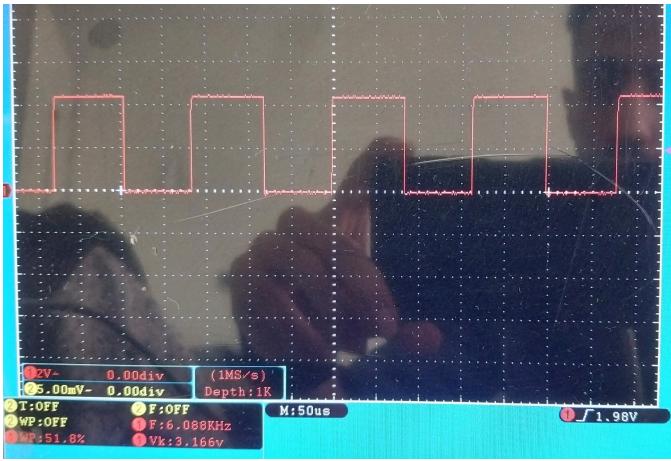


Fig. 6. Output waveform of LM555 in astable mode with $R_2 = 10k\Omega$

- $R_2 = 100k\Omega$: At first, we calculate the frequency and duty cycle like equation above.

$$\text{Frequency} = \frac{1}{0.693(201 \times 10^3)10^{-8}} = 48.1kHz \quad (16)$$

$$\text{Duty - Cycle} = \frac{10^3 + 100 \times 10^3}{10^3 + 200 \times 10^3} = 66.6\% \quad (17)$$

According to Fig. 7, the observed frequency and duty-cycle for this value of R_2 is:

$$\text{Frequency} = 669.3Hz \quad (18)$$

$$\text{Duty - Cycle} = 49.7\% \quad (19)$$



Fig. 7. Output waveform of LM555 in astable mode with $R_2 = 100k\Omega$

As it is shown in Table I and Table II the value of the observed and calculated frequencies and duty-cycles are almost the same.

TABLE I
THE OBSERVED FREQUENCY AND DUTY-CYCLE USING THE WAVEFORM

Value of R_2	Frquency	Duty-Cycle
$R = 1k\Omega$	38.76kHz	65.9%
$R = 10k\Omega$	6.088kHz	51.8%
$R = 100k\Omega$	669.3Hz	49.7%

TABLE II
THE CALCULATED FREQUENCY AND DUTY-CYCLE USING THE VALUE OF R_1 , R_2 AND C_1

Value of R_2	Frquency	Duty-Cycle
$R = 1k\Omega$	48.1kHz	66.6%
$R = 10k\Omega$	6.871kHz	52.38%
$R = 100k\Omega$	717.9Hz	49.75%

III. SCHMITT TRIGGER OSCILLATOR

Question 1. Considering the given equation, implement the circuit with different values for the resistor and observe the changes. Use 470Ω , 1000Ω and 2200Ω for the resistor and $10nF$ for the capacitor.

The frequency of the output waveform for each value of resistor R is shown below.

- $R = 1k\Omega$: The frequency for this value of R is observed in Fig. 8.

$$\text{Frequency} = 123.8kHz \quad (20)$$



Fig. 8. Output waveform of Schmitt Trigger Oscillator with $R = 1k\Omega$

- $R = 2.2k\Omega$: The frequency for this value of R is observed in Fig. 9.

$$\text{Frequency} = 55.87kHz \quad (21)$$



Fig. 9. Output waveform of Schmitt Trigger Oscillator with $R = 2.2k\Omega$

- $R = 470\Omega$: The frequency for this value of R is observed in Fig. 10.

$$\text{Frequency} = 246.3\text{kHz} \quad (22)$$



Fig. 10. Output waveform of Schmitt Trigger Oscillator with $R = 470\Omega$

Question 2. Find α parameter.

- $R = 1k\Omega$:

$$\text{Frequency} = 123.8\text{kHz} \rightarrow \alpha = fRC = 1.238 \quad (23)$$

- $R = 2.2k\Omega$:

$$\text{Frequency} = 55.87\text{kHz} \rightarrow \alpha = 1.22914 \quad (24)$$

- $R = 1k\Omega$:

$$\text{Frequency} = 246.3\text{kHz} \rightarrow \alpha = 1.15761 \quad (25)$$

The frequency and α parameter for each value resistor R are shown in Table III.

TABLE III
THE FREQUENCY AND α PARAMETER FOR EACH VALUE OF RESISTOR R

Value of R	Frequency	α parameter
$R = 1k\Omega$	123.8kHz	1.238
$R = 1k\Omega$	55.87kHz	1.22914
$R = 470\Omega$	246.3kHz	1.15761

IV. SYNCHRONOUS COUNTER AS A FREQUENCY DIVIDER

Question 1. Use the ring oscillator of part 1 to generate a clock signal. This will be the clock input of the LSB counter. According to part 1 (Ring Oscillator) and equation (1):

$$F_{\text{Ring-Oscillator}} = 35.87\text{kHz}$$

Question 2. A Presetting mechanism is necessary for initial loading of the counters of Fig. 11. The mechanism as you have learned in the logic design course can include an AND gate for anding a preset input signal with the load inputs of the counter. Perform this presetting by using 7408 AND gate as shown in figure Fig. 11.

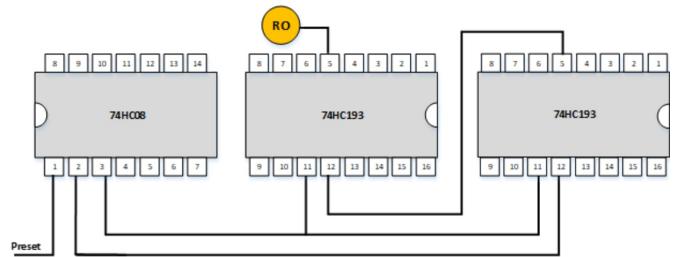


Fig. 11. Frequency divider using 74HC193

As we read in the "Experiment1 Instruction", When up counting is desired the initial value is obtained by:

$$\text{Initial Load} = \text{Maximum value} - \text{Modulus}$$

We want to construct a divide by 200 synchronous up-counter and we have two 74HC193. So the Maximum value is $2^8 - 1 = 255$. Thus we must set initial load of value 55.

$$\text{Initial Load} = 255 - 200 = 55 = (00110111)_{\text{binary}}$$

So we set the value of $P_3 - P_0$ of both IC as shown in Fig. 12.

Question 3. Record the results of carry out of the MSB counter and measure its frequency, compare the results with the frequency of the input clock.

As it is shown in Fig. 13. the frequency of carry out of the MSB counter is:

$$\text{Desired - Frequency} = 176.1\text{kHz} \quad (26)$$

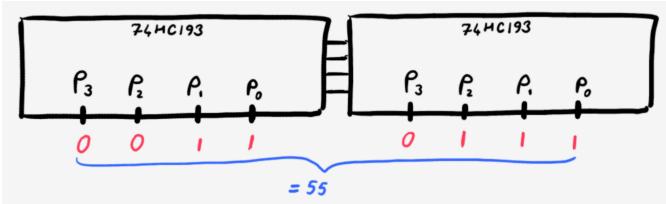


Fig. 12. Setting the value of $P_3 - P_0$ of ICs

As we want to construct a divide by 200 synchronous up-counter, we divide the Ring-Oscillator frequency by 200. After calculation the desired frequency can be achieved:

$$\text{Desired - Frequency}_{\text{calc}} = \frac{35.87\text{MHz}}{200} = 179.35\text{kHz} \quad (27)$$

As it is illustrated, the calculated value of the desired frequency and observed one are almost the same.

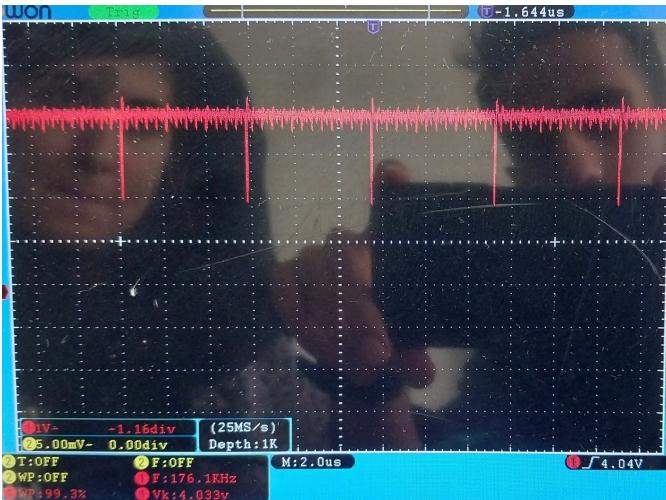


Fig. 13. Carry-Out of the MSB counter waveform and its frequency

V. T FLIP-FLOP

We use D Flip-Flop and convert it to a T Flip-Flop as the pin layout shown in Fig. 14. As we see in Fig. 15, the duty cycle is 50% and the frequency that is observed is

$$\text{Frequency} = 86.81\text{kHz} \quad (28)$$

which is almost half of the desired frequency.

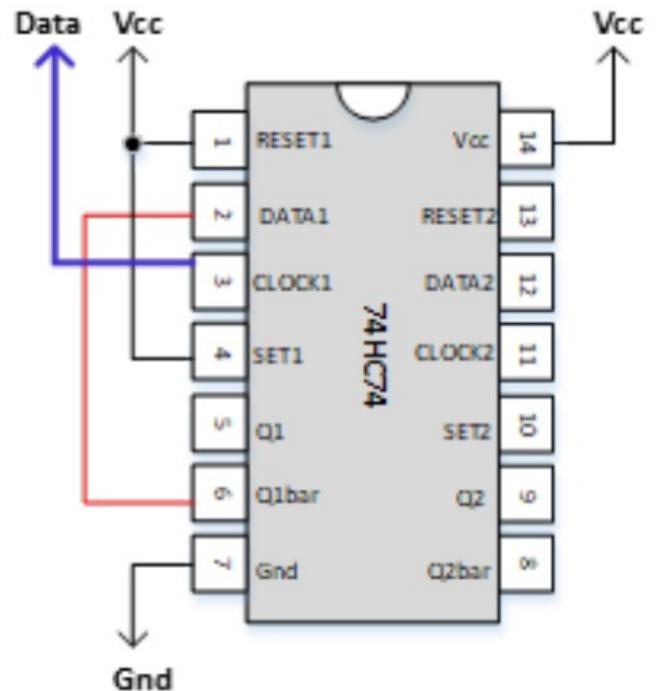


Fig. 14. Converting D Flip-Flop to T Flip-Flop

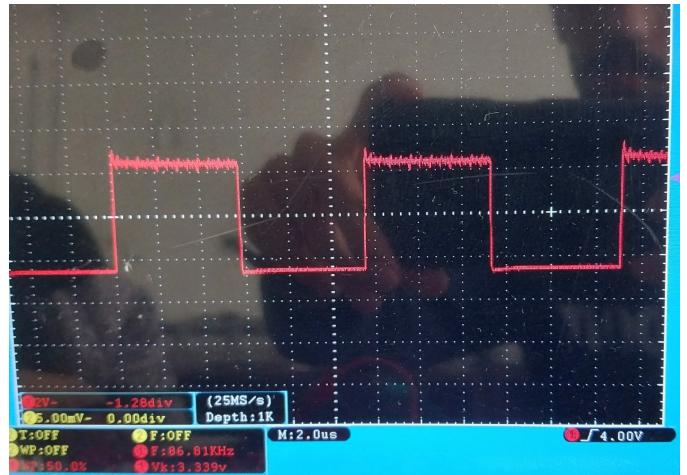


Fig. 15. Output waveform of the T Flip-Flop