

Computer Aided Design

Instructor: Dr.Beitollahi

Homework 4

Topic: Advanced VHDL & FPGA

Lectures: 7-8-9-10-11

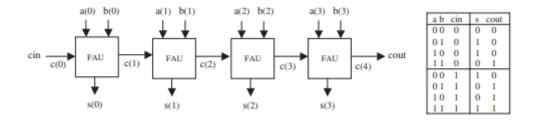
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Deadline: 1403/3/25

Implementation:

Q1) Consider the *Carry Ripple Adder* given below. Design a FAU (Full Adder Unit), to be used as a COMPONENT. Write a code for the complete *Carry Ripple Adder* containing instantiations of FAU. Compile and simulate the synthesized circuit. (15 points)



Implementation without component is not acceptable.

Q2) Write a <u>function</u> capable of converting an INTEGER to a STD_LOGIC_VECTOR value. Call it *conv_std_logic()*. Then write an application example, containing a call to your function, in order to test it. Construct a solution containing the function in the main code itself. (15 points)

Implementation without function is not acceptable.

Q3) Design a password system such that its inputs are 0, 1 and Reset. The system should recognize the input pattern 0110 as the correct password and, in this case, change the output state of the lock to 1 (Unlocked). If the input pattern is incorrect or the Reset button is pressed, the system should return to the initial state and change the output to 0 (Locked). The states and transitions between them should be clearly defined in the code. (20 points)

Theory:

Q4) Design a Finite State Machine (FSM) for a smart home lighting system that can turn the lights on/off, dim, and brighten. (10 points)

Q5) Implement these two functions on a <u>single PAL</u> with minimum number of resources. (10 points)

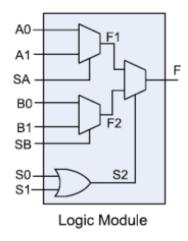
(hint: You can use S_0 to construct S_1)

$$S_0 = \overline{A_1} \, \overline{A_0} \, B_0 \, B_1 \, + \, \overline{A_1} \, \overline{A_0} \, B_0 \, \overline{B_1} \, + \, \overline{A_1} \, A_0 \, \overline{B_0} \, \overline{B_1} \, + \, \overline{A_1} \, A_0 \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, B_0 \, B_1 \, + \, A_1 \, \overline{A_0} \, B_0 \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, B_0 \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, B_0 \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, B_0 \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, B_0 \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, B_0 \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, B_0 \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, B_0 \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, B_0 \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, B_0 \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, B_0 \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \, \overline{B_1} \, + \, A_1 \, \overline{A_0} \, \overline{B_0} \,$$

$$S_1 = A_0 \overline{B_0} (A_1 + \overline{B_1}) + \overline{A_0} B_0 (\overline{B_1} + A_1) + \overline{A_1} B_1 (\overline{A_0} \overline{B_0} + A_0 B_0)$$

Q6) Implement the following function on the given logic module. (15 points)

$$F = (A.B) + (B'.C) + D$$



Q7) Using the programmable logic device shown below, implement a circuit in which input is a 3-bit number x and its output is x + 3. (15 points) Put a cross in the circles or fill up the circles where the connection should be made.

