



Digital System Design

Instructor: Dr.Beitollahi

Homework 1

Topic: Basic VHDL

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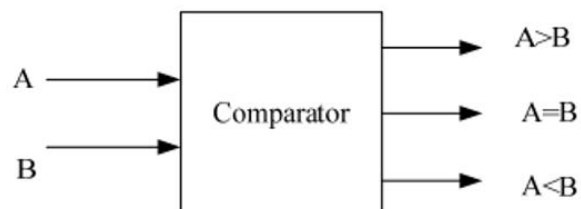
1) Answer the following questions. (10 points)

1. What are different modes of Ports? Explain each one and Compare them.
2. Write the number 478 in binary, octal and hexadecimal as a bit string.
3. What are the *Identifiers*? Write their properties in VHDL.
4. Explain five differences between *Variables* and *Signals*.
5. Name different usages of *Generics*.
6. In the following code, find all *Syntax Errors*.

```
entity Example is
Port (
input_signal : in STD_LOGIC;
output_signal : out STD_LOGIC
);

architecture Behavioral of Example is
signal internal_signal : STD_LOGIC;
begin
process
begin
if input_signal = '1' then
internal_signal <= '1';
else
internal_signal <= '0';
end process;
output_signal <= internal_signal
```

- 2) Design a Comparator for 4-bit numbers. The comparator should have 3 output signals, indicating whether the first number is greater than, smaller than or equal to the second number. (20 points)



Your implementation must contain test bench, including all possible cases.

- 3) A CPU with 8-bit registers needs a specific ALU with the following functionalities: (30 points)

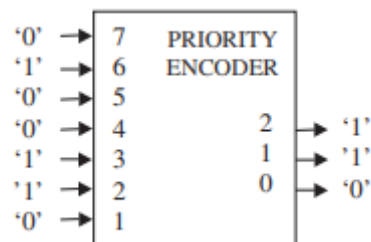
Selector	Function
000	Increment ($Y \leq a + 1$)
001	Unsigned Add ($Y \leq a + b$)
010	Signed Add ($Y \leq a + b$)
011	Add with carry ($Y \leq a + b + cin$)
100	Complement
101	2's Complement
110	NAND ($Y \leq a \text{ NAND } b$)
111	XOR ($Y \leq a \text{ XOR } b$)

First, draw the schematic of module, including *Datapath* and *Control Unit*.

Next, write a behavioral VHDL code for the ALU.

Your implementation must contain test bench, including all possible cases.

- 4) Imagine a *7-level Priority Encoder*, The circuit must encode the address of the input bit of highest order that is active. "000" should indicate that there is no request at the input (no bit active). (40 points)



Implement the Priority Encoder in VHDL using the following:

- Using WHEN/ELSE
- Using only Operators

Your implementation must contain test bench, including all possible cases.