بسمه تعالی

دانشگاه خوارزمی

Test and Testable Design (Fall 1402)

Assignment #2

Due date: 1402/09/05

No Late Submission Accepted!

In this exercise, we start practicing various aspects of fault simulation.

1- Use Netlist of *CKT.V* and do the followings:
   a. Write a testbench which can do serial fault simulation.
      i. To do so, you need to make a list of collapsed faults in "*CKT.flt"* using the PLI function *$faultCollapsing*
      ii. Your fault simulator must perform no fault dropping
      iii. Your fault simulator must report the type, test vector, and time for every detected fault in "CKT.det", for the given test set "CKT.tst"
      Fault: Tester.FUT.O1.in[0] S@1 was detected by TestVector=000 and time=50ns.

      Note: Your fault simulator must also report the fault coverage at the end of "CKT.tst"

   b. Write a testbench which makes a fault dictionary for the *CKT*.
      i. Your fault simulator must report the anticipated results for every fault for test vectors in the form of **fault syndromes** in "CKT.dct"
      ii. The format of the report **must** be like this:
      Tester.FUT.O1.in[0], Fault Type =S@1, Syndrom=0010101

2- Write a structural gate-level full-adder in verilog, then make a netlist using the NetlistGen application. To do so, please read the manual file of NetlistGen carefully.