Sets the Event Status Bit (ESB - bit No. 5) of the Service Request Enable Register (SRE) to 1 to enable ESB service request.

3. Send the overlapped command with `*OPC`
   Example: `INIT; *OPC`
4. Wait for an ESB service request.

   The service request indicates that the overlapped command has finished.

***OPC? with a service request**

1. Execute `*SRE 16`

   Sets the Message Available bit (MAV - bit No. 4) of the Service Request Enable Register (SRE) to 1 to enable MAV service request.
2. Send the overlapped command with `*OPC?`
   Example: `INIT; *OPC?`
3. Wait for an MAV service request.

   The service request indicates that the overlapped command has finished.

Event status enable register (ESE)

1. Execute `*ESE 1`

   Sets the OPC mask bit (bit No. 0) of the Standard Event Status Register (ESR) to 1
2. Send the overlapped command without `*OPC`, `*OPC?` or `*WAI`.
   Example: `INIT; *OPC?`
3. Poll the operation complete state periodically (with a timer) using the sequence: `*OPC; *ESR?`

   A return value (LSB) of 1 indicates that the overlapped command has finished.

5.5 Status reporting system

The status reporting system stores all information on the current operating state of the instrument, and on errors which have occurred. This information is stored in the status registers and in the error queue.

You can query both with the commands of the STATus subsystem.

5.5.1 Hierarchy of the status registers

The Figure 5-1 shows the hierarchical structure of information in the status registers (ascending from left to right).