- **Standard Event Status**, i.e. the Event status Register (ESR) and the Event Status Enable (ESE), see Chapter 5.5.4, "Event status register (ESR) and event status enable register (ESE)", on page 278.
- **Questionable Status** and **Operation Status**, the (SCPI status registers, see Chapter 5.5.2, "Structure of a SCPI status register", on page 275, Chapter 5.5.5, "Questionable status register (STATus:QUEStionable)", on page 278 and Chapter 5.5.6, "Operation status register (STATus:OPERation)", on page 279.
- **Output-Queue**
  The output queue contains the messages the instrument returns to the controller. It is not part of the status reporting system but determines the value of the `MAV` bit in the `STB` and thus is represented in the overview.
- **Error- /Event-Queue**
  The error-/event-queue contains all errors and events that have occurred in the past. When reading the queue, the instrument starts with the first occurred error/ event.

All status registers have the same internal structure.

SRE, ESE

The service request enable register `SRE` can be used as `ENABle` part of the `STB` if the `STB` is structured according to SCPI. By analogy, the `ESE` can be used as the `ENABle` part of the `ESR`.

5.5.2 Structure of a SCPI status register

Each SCPI status register consists of five parts. Each part has a width of 16 bits and has different functions. The individual bits are independent of each other, i.e. each hardware status is assigned a bit number, which is valid for all five parts. Bit 15 (the most significant bit) is set to zero for all parts. Thus, the contents of the register parts can be processed by the controller as positive integers.

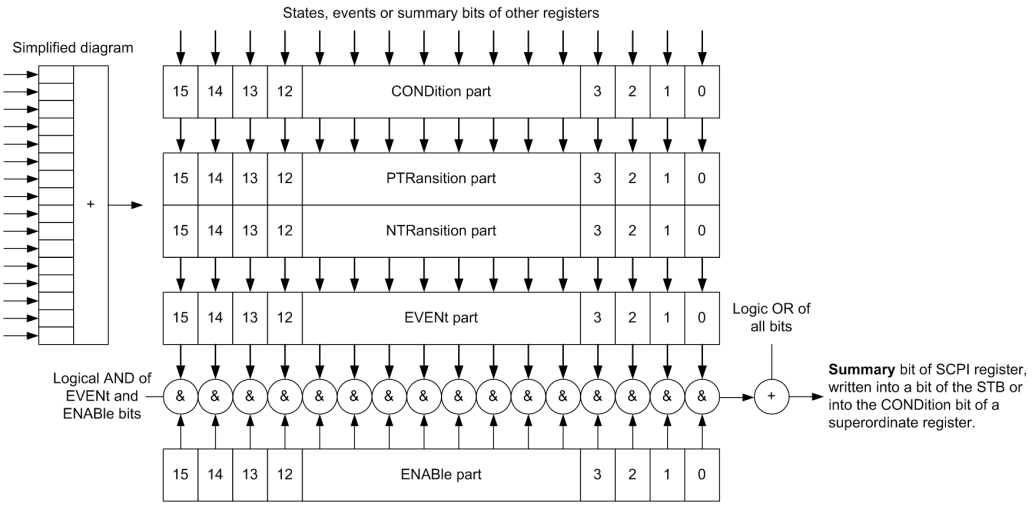

Figure 5-2: The status-register model

Description of the five status register parts

The five parts of a SCPI status register have different properties and functions:

- **CONDition**
  The CONDition part is written directly by the hardware or it mirrors the sum bit of the next lower register. Its contents reflect the current instrument status. This register part can only be read, but not written into or cleared. Its contents are not affected by reading.
- **PTRansition / NTRansition**
  The two transition register parts define which state transition of the CONDition part (none, 0 to 1, 1 to 0 or both) is stored in the EVENt part.
  The **Positive-TRansition** part acts as a transition filter. When a bit of the CONDition part is changed from 0 to 1, the associated PTR bit decides whether the EVENt bit is set to 1.
  – PTR bit =1: the EVENt bit is set.
  – PTR bit =0: the EVENt bit is not set.

  This part can be written into and read as required. Its contents are not affected by reading.
  The **Negative-TRansition** part also acts as a transition filter. When a bit of the CONDition part is changed from 1 to 0, the associated NTR bit decides whether the EVENt bit is set to 1.
  – NTR bit =1: the EVENt bit is set.
  – NTR bit =0: the EVENt bit is not set.

  This part can be written into and read as required. Its contents are not affected by reading.
- **EVENt**
  The EVENt part indicates whether an event has occurred since the last reading, it is the "memory" of the condition part. It only indicates events passed on by the transition filters. It is permanently updated by the instrument. This part can only be read by the user. Reading the register clears it. This part is often equated with the entire register.
- **ENABle**
  The ENABle part determines whether the associated EVENt bit contributes to the sum bit (see below). Each bit of the EVENt part is "ANDed" with the associated ENABle bit (symbol '&'). The results of all logical operations of this part are passed on to the sum bit via an "OR" function (symbol '+').
  ENABle bit = 0: the associated EVENt bit does not contribute to the sum bit
  ENABle bit = 1: if the associated EVENt bit is "1", the sum bit is set to "1" as well.
  This part can be written into and read by the user as required. Its contents are not affected by reading.

Sum bit

The sum bit is obtained from the EVENt and ENABle part for each register. The result is then entered into a bit of the CONDition part of the higher-order register.