## Program Classification Using the PMU

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#### Motivation

- Personal: Multidisciplinary project that exercises skills valuable for my career
  - Computer architecture PMU monitors microarchitectural events
  - Operating systems User space tools and performance event configurations
  - Machine learning Modeling outcomes based on PMU observations

#### Dataset generation

- Machine learning problem where the user gets to create the dataset instead of relying on existing datasets.
- Results in the need to tune data collection hyperparameters as well as model hyperparameters.

#### Unique Problem

- Underutilization of a potentially valuable methodology
  - sparse documentation of tools
  - Not a substantial area of research
- Dimensionality reduction when all features cannot be monitored simultaneously

## Performance Monitoring Unit (PMU)

#### What is the PMU?

Extra hardware that monitors microarchitectural "events" and increments performance monitoring counters (PMCs) when they occur.

#### What are events?

The set of occurrences that PMU architects have enabled PMCs to count.

#### **Event Examples**

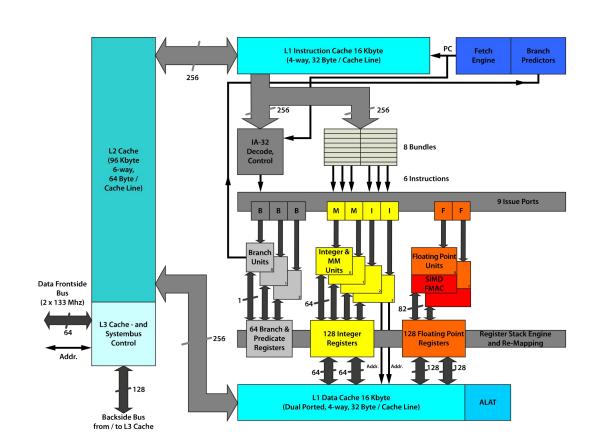
- Core clock cycles
- Instructions retired
- L1 Cache hits
- L2 Cache misses
- Branching instructions
- Branch mispredictions

#### PMU is Hardware

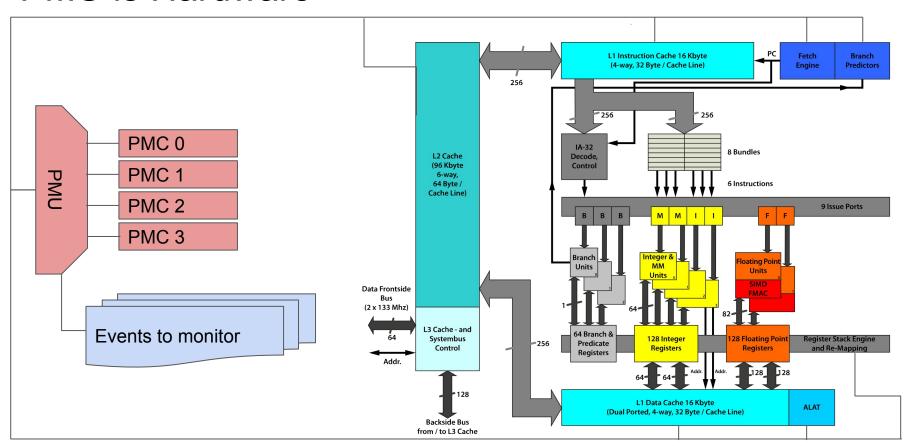
CPU diagrams have a lot of recognizable components

- Floating point units
- Caches
- Branch prediction
- Memory Busses
- etc...

You almost never see PMU hardware in a CPU diagram



#### PMU is Hardware



#### **PMU Interface**

The Intel IA-32 Software Developer's Manual is the end all be all for Intel CPU programming.

Referenced often when it comes to understanding Intel PMUs.



#### Intel® 64 and IA-32 Architectures Software Developer's Manual

Volume 3B: System Programming Guide, Part 2

NOTE: The Intel® 64 and IA-32 Architectures Software Developer's Manual consists of nine volumes. Basic Architecture, Order Number 253665; Instruction Set Reference A-M. Order Number 253666; Instruction Set Reference V-Z. Order Number 253667; Instruction Set Reference V-Z. Order Number 326018; Instruction Set Reference, Order Number 334569; System Programming Guide, Part 1, Order Number 253668; System Programming Guide, Part 2, Order Number 253669; System Programming Guide, Part 3, Order Number 326019; System Programming Guide, Part 4, Order Number 332831. Refer to all nine volumes when evaluating your design needs.

> Order Number: 253669-060US September 2016

#### PMU Chapters

## CHAPTER 18 PERFORMANCE MONITORING

Intel 64 and IA-32 architectures provide facilities for monitoring performance via a PMU (Performance Monitoring Unit).

## CHAPTER 19 PERFORMANCE-MONITORING EVENTS

This chapter lists the performance-monitoring events that can be monitored with the Intel 64 or IA-32 processors. The ability to monitor performance events and the events that can be monitored in these processors are mostly model-specific, except for architectural performance events, described in Section 19.1.

Non-architectural performance events (i.e. model-specific events) are listed for each generation of microarchitecture:

#### PMU Performance Event Select MSR

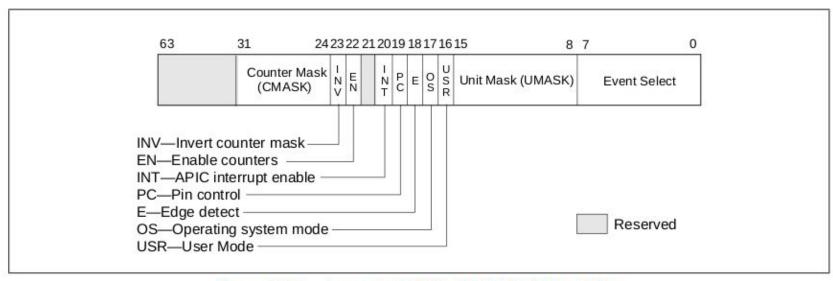


Figure 18-1. Layout of IA32\_PERFEVTSELx MSRs

## **Event and Mask Example**

Table 19-1. Architectural Performance Events

Event Num.	Event Mask Name	Umask Value	Description
3CH	UnHalted Core Cycles	00H	Counts core clock cycles whenever the logical processor is in CO state (not halted). The frequency of this event varies with state transitions in the core.
3CH	UnHalted Reference Cycles <sup>1</sup>	01H	Counts at a fixed frequency whenever the logical processor is in CO state (not halted).
СОН	Instructions Retired	00H	Counts when the last uop of an instruction retires.
2EH	LLC Reference	4FH	Accesses to the LLC, in which the data is present (hit) or not present (miss).
2EH	LLC Misses	41H	Accesses to the LLC in which the data is not present (miss).
C4H	Branch Instruction Retired	00H	Counts when the last uop of a branch instruction retires.
C5H	Branch Misses Retired	00H	Counts when the last uop of a branch instruction retires which corrected misprediction of the branch prediction hardware at execution time.

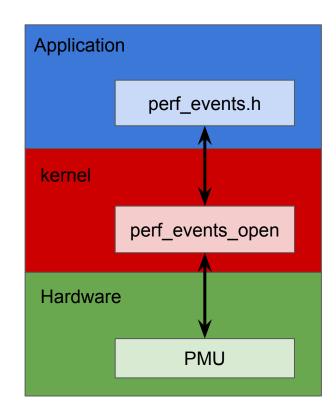
## Interacting With the PMU

The PMU is part of the microarchitecture

One option is to write x86 assembly to control the PMU directly (lots of work)

To avoid assembly the kernel must expose an API to interact with the PMU

Perf\_events is the Linux API and subsystem that allows for interaction with the PMU from C applications



#### perf\_event\_open

pid == 0 and cpu == -1	This measures the calling process/thread on any CPU.
pid == 0 and cpu >= 0	This measures the calling process/thread only when running on the specified CPU.
pid > 0 and cpu == -1	This measures the specified process/thread on any CPU.
pid > 0 and cpu >= 0	This measures the specified process/thread only when running on the specified CPU.
pid == -1 and cpu >= 0	This measures all processes/threads on the specified CPU. This requires CAP_SYS_ADMIN capability or a /proc/sys/kernel/perf_event_paranoid value of less than 1.

## perf\_events\_attr

- type Type of PMU event
- inherit If set, child processes
   events will be counted

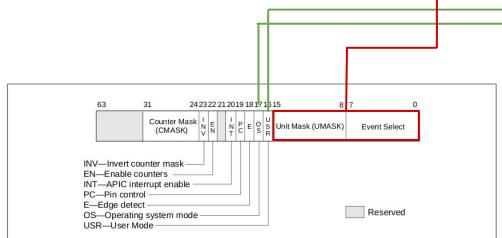


Figure 18-1. Layout of IA32\_PERFEVTSELx MSRs

```
struct perf event attr {
                   /* Type of event */
   u32 type;
    u32 size:
                   /* Size of attribute structure */
    u64 confia:
                    /* Type-specific configuration */
  union {
       u64 sample period; /* Period of sampling */
       u64 sample freq:
                            /* Frequency of sampling */
                          /* Specifies values included in sample */
  u64 sample type;
  u64 read format;
                          /* Specifies values returned in read */
    u64 disabled
                           : 1, /* off by default */
      inherit
                           : 1. /* children inherit it */
      pinned
                           : 1, /* must always be on PMU */
      exclusive
                           : 1, /* only group on PMU */
      exclude user
                           : 1. /* don't count user */
      exclude kernel
                          : 1. /* don't count kernel */
                           : 1, /* don't count hypervisor */
      exclude hv
                          : 1. /* don't count when idle */
      exclude idle
                           : 1. /* include mmap data */
      mmap
                           : 1. /* include comm data */
      comm
                           : 1, /* use freq, not period */
      frea
      inherit stat
                           : 1. /* per task counts */
                           : 1. /* next exec enables */
      enable on exec
                           : 1. /* trace fork/exit */
      task
      watermark
                           : 1, /* wakeup watermark */
                           : 2. /* skid constraint */
      precise ip
      mmap data
                           : 1, /* non-exec mmap data */
                           : 1, /* sample type all events */
      sample id all
                           : 1. /* don't count in host */
      exclude host
      exclude guest
                           : 1, /* don't count in guest */
                           : 1, /* include mmap with inode data */
      mmap2
                           : 1, /* flag comm events that are due to exec */
      comm exec
```

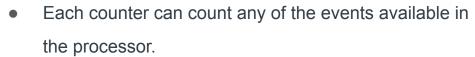
#### Implementation: Predict Raspberry Pi CPU Temp

- Last term
- More simple to understand before moving on to more complex task
- Subset of the main problem
  - PMU initialization
  - Forking and inherited monitoring
  - Python data collection manager

#### Hardware: Raspberry Pi 3b

- Quad Core 1.2GHz Broadcom BCM2837 64bit CPU
  - Implements the Arm Cortex A53 processor
  - Arm Cortex A53 implements the PMU

- ARM Cortex A53 PMU provides six counters
  - + dedicated cycle counter





#### Goal: Correlate microarchitectural events to temperature differential

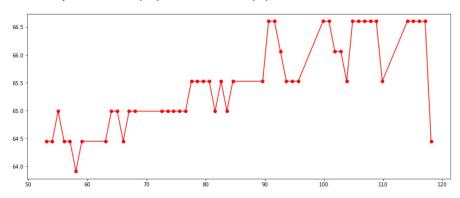
#### Methodology - Data collection

- Generate random workloads
- For each workload, monitor events
- Simultaneously monitor core temperature

#### Methodology - Regression

- Normalize event counts
- Ridge regression across normalized data

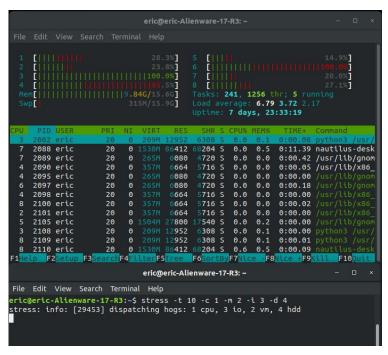




#### Workload generation: Linux stress

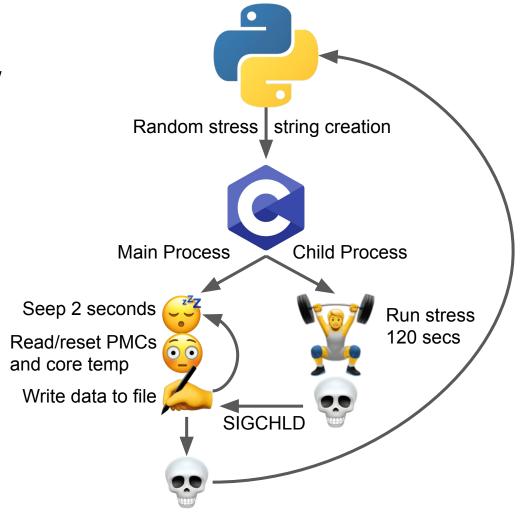
Linux stress is a tool that launches subprocesses of specific types for a specified period of time, generating a work load that can be used to test a system.

Opt	Meaning
-t N	Run for N seconds
-c N	Spawn N workers spinning on sqrt ()
-m N	spawn N workers spinning on malloc()/free()
-i N	Spawn N workers spinning on sync()
-d N	Spawn N workers spinning on write()/unlink()



#### Data collection workflow

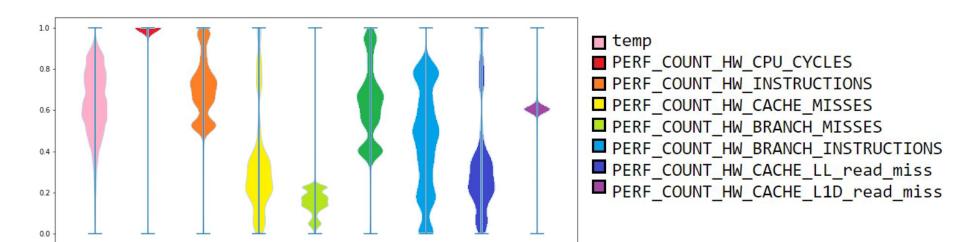
- Python generates stress executable strings with random set of workers
- 2. C program takes stress string as input
- 3. C sets up a SIGCHLD listener that will terminate the program
- 4. C program forks a child process
  - a. The child process runs the stress workload
  - The parent process sleeps for 1 second and then records and resets the PMCs
- 5. Exit of child processes results in the termination of program.
- 6. Python feeds the next stress call in



#### **Events Monitored**

Event Name	Description
PERF_COUNT_HW_CPU_CYCLES	Total cycles. Be wary of what happens during CPU frequency scaling.
PERF_COUNT_HW_INSTRUCTIONS	Retired instructions. Be careful, these can be affected by various issues, most notably hardware interrupt counts
PERF_COUNT_HW_CACHE_MISSES	Cache misses. Usually this indicates Last Level Cache misses
PERF_COUNT_HW_BRANCH_MISSES	Mispredicted branch instructions.
PERF_COUNT_HW_BRANCH_INSTRUCTIONS	Retired branch instructions.
PERF_COUNT_HW_CACHE_LL_read_miss	Measuring Last-Level Cache for read misses
PERF_COUNT_HW_CACHE_L1D_read_miss	Measuring Level 1 Data Cache for read misses

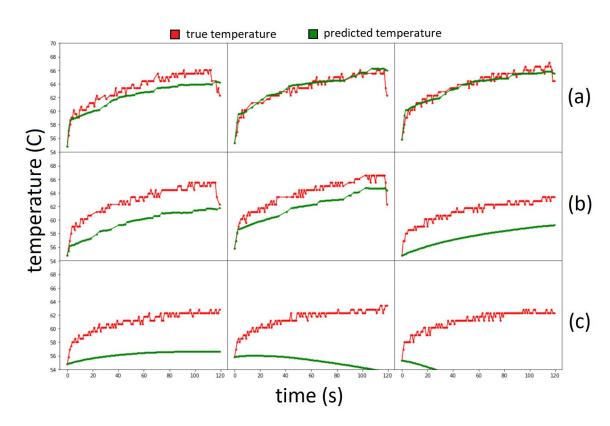
#### Normalized event count distributions



## Results: Ridge regression, $\alpha$ =1

coef

-0.281332 PERF COUNT HW CPU CYCLES -0.062500 PERF\_COUNT\_HW\_INSTRUCTIONS 0.161314 PERF COUNT HW CACHE MISSES 0.030964 PERF COUNT HW BRANCH MISSES 0.229393 PERF COUNT HW BRANCH INSTRUCTIONS PERF COUNT HW CACHE LL read miss 0.272127 PERF\_COUNT\_HW\_CACHE\_L1D\_read miss 0.030981



#### So there you have it

Using PMU events to predict a temperature

#### **But wait!**

- How were the event chosen? They seemed like a good idea...
- Can we be sure the selected events were the best for this task? No, not at all
- How do we find the best events to monitor for a specific task? Good question
- Why can't we monitor all events and perform dimensionality reduction?

# PMU Based Program Classification on the 6th Gen Intel Core i7 (Skylake)

The multiplexing problem

#### Intel Skylake Architecture Events

- Architecture code name: Skylake
- 4 physical cores / 8 logical cores
  - Hyperthreading
  - Can turn hyperthreading
- Complex PMU
  - 8 Skylake event PMCs per core if hyperthreading is diabled in the BIOS
  - 4 PMCs per core if hyperthreading is enabled (standard)
  - o Lots of events!

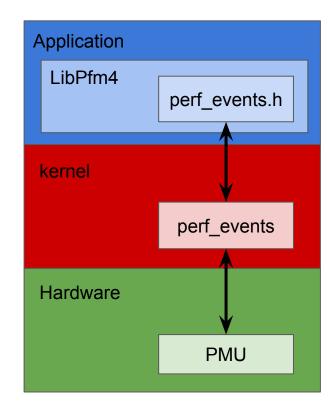


## LibPfm4: Configuring events

Wrapper around perf\_events that maintains list of available events and configurations for many architectures.

Given an "event string" input it will return a structure what contains the perf\_event\_attr structure.

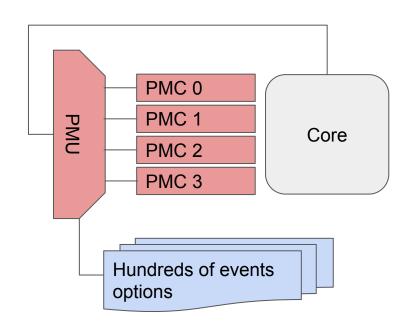
This structure can be fed directly into the perf\_event\_open system call.



#### The fundamental problem

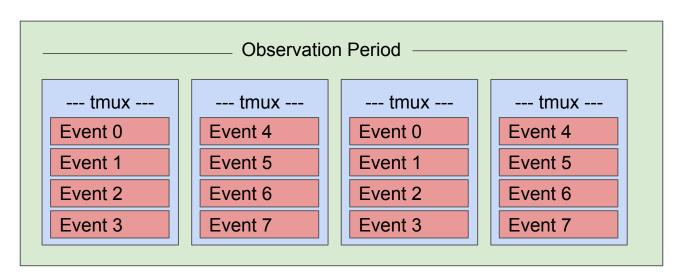
There are hundreds of events to monitor but only 4 counters per core.

This means that only up to 4 events can be monitored at any given time.



#### Temporal event multiplexing

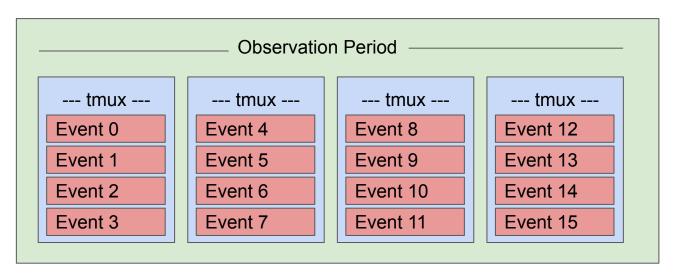
Swapping events on and off of the PMU in order to gather data on more events than there are performance counters. It is fundamentally a false view of reality since you miss all events that occur when that event is not programmed on the PMU. It is possible to normalize by capturing the amount of time an event was on the PMU during the observation period.



## Problems with temporal multiplexing

#### Low Resolution

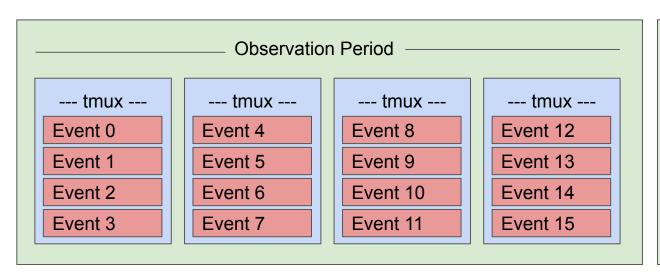
The fewer number of times events are scheduled on the PMU during an observation period the more exposed they are to temporal anomalies and the less accurately they reflect the reality of what is happening on the processor.

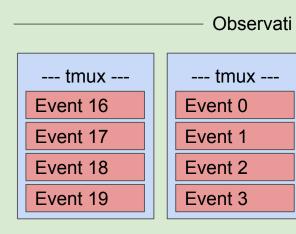


## Problems with temporal multiplexing

#### Missing data in observations

If there are more events to be monitored than there are multiplexing periods in the observation period then it is possible for events to never be scheduled on the PMU during an period.





## The Multiplexing Problem

- Multiplexing is useful in that it allows to gather, some level of statistical certainty, information on event occurrence about more events than there are available PMCs
- However, the more events there are the less precision we get.
- The observation window can be extended to allow for more event cycles, but then we begin aliasing on specific program functionality.
- If #events > PMCs/tmux then observations will be missing events entirely

## Program Classification

• Number of Events: 230

• PMC on Core: 4

• **Tmux**: 4 ms

Observation Period: 100 ms

How do we set up an experiment that determines the best combination of events to classify programs while avoiding the pitfalls of the multiplexing problem

#### What are the programs we are going to distinguish between?

- stress -t 100 -d 1
- stress -t 100 -i 1
- stress -t 100 -i 1 -d 1
- stress -t 100 -m 1
- stress -t 100 -m 1 -d 1
- stress -t 100 -m 1 -i 1
- stress -t 100 -m 1 -i 1 -d 1
- stress -t 100 -c 1
- stress -t 100 -c 1 -d 1
- stress -t 100 -c 1 -i 1
- stress -t 100 -c 1 -i 1 -d 1
- stress -t 100 -c 1 -m 1
- stress -t 100 -c 1 -m 1 -d 1
- stress -t 100 -c 1 -m 1 -i 1
- stress -t 100 -c 1 -m 1 -i 1 -d 1

- Each of the stress options either on or off
- Creates 15 programs to distinguish between
- Interesting because we know problems have a lot in common since they are different combinations of each other
- Each program runs for 100 seconds
- Since the observation period will be 100 ms, there will be 1,000 observations per program
- ► Total of ~15,000 observations

## Learning Method: Event Forest

#### **Data Collection Methodology**

Sample the available event list without replacement N times to create N decision trees.

#### **Data Collection Parameters**

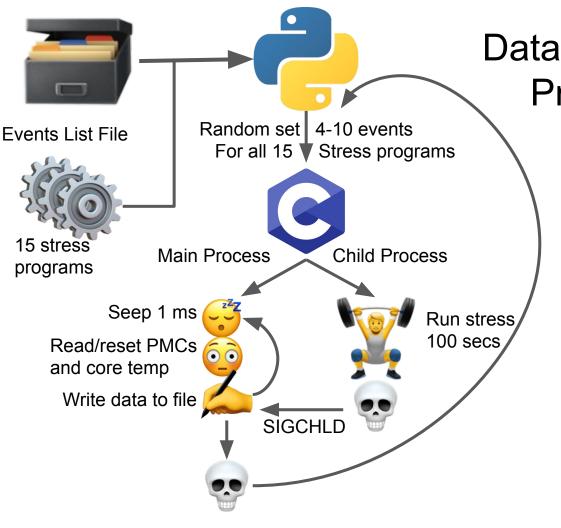
- Number of trees = 100
- Observation Period = 100 ms
- Min events = 4
- Max events = 10
  - $\circ$  .1/((10/4)\*.004 = 10 rounds on PMU/event

#### **Learning Methodology**

Apply standard decision tree algorighm to each tree and find get the best performing tree.

#### **Training Hyperparameters**

- Max depth = 8
- Min points = 64
- Impurity Metric = Gini



Data Collection:

Program classification

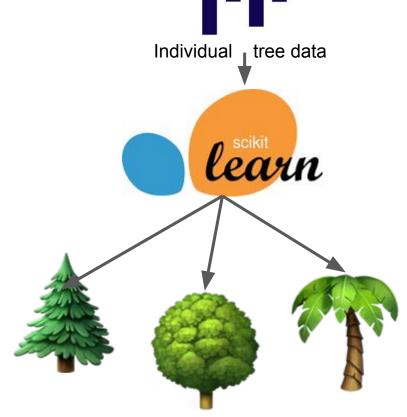
- 1. Python gathers all events from valid event list and creates 100 sets of 4 to 10 events.
- Python gathers the names of the different programs and manages the running of the programs against the specific event sets.
- 3. C program, using perf\_events and LibPfm4 generates the PMU configurations and loads the PMU.
- 4. C program monitors and records events just as last time, only associating events with a program instead of a temperature change.

## Classifier Training: Decision Tree Set

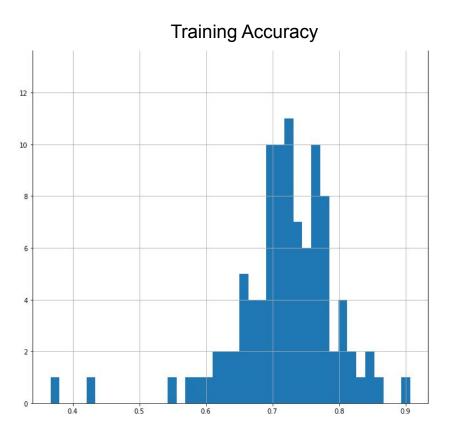


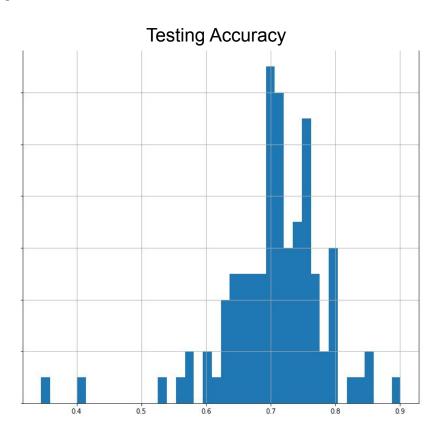


- Pandas is used to load and combine data files.
- ScikitLearn applies decision tree algorithm to data in training dataset generating trees.
- ScikitLearn runs test sets against built trees and outputs performance results.
- 4. The best tree is selected.



## Results: Tree 1 - 100 accuracy

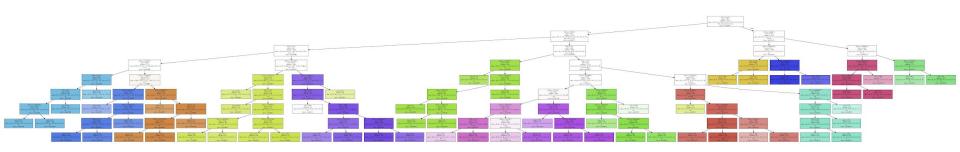




#### Best Tree: 66

Tree Index	Event Name	Description
0	DTLB_STORE_MISSES:WALK_ACTIVE	Counts cycles when at least one PMH (Page Miss Handler) is busy with a page walk for a store.
1	INST_RETIRED:PREC_DIST	A version of INST_RETIRED that allows for a more unbiased distribution of samples across instructions retired. It utilizes the Precise Distribution of Instructions Retired (PDIR) feature to mitigate some bias in how retired instructions get sampled.
2	MEM_LOAD_MISC_RETIRED:UC	Retired instructions with at least 1 uncacheable load or lock.
3	UOPS_EXECUTED:THREAD	Number of uops to be executed per-thread each cycle.
4	TX_EXEC:MISC2	Unfriendly TSX abort triggered by a vzeroupper instruction.
5	TX_MEM:ABORT_HLE_STORE_TO_ELIDED_LOCK	Number of times a TSX Abort was triggered due to a non-release/commit store to lock.

## Best Tree: 66



#### Recap

- Introduced the PMU
- Introduced tool to make working with the PMU easier
  - Perf events for interacting with the PMU with C
  - LibPfm4 for generating configurations to be fed to perf\_events
- Demonstrated PMU data can be used in data science application
  - Regression an pre selected events
  - Classification on all available events
- Identified a unique problem, uncommon in standard data science workflows
  - The multiplexing problem doesn't allow for all features in a dataset to be gathered simultaneously
- Proposed a simplistic form of dimensionality reduction to address the multiplexing problem

## Gratitude to the open source community

I do not possess the skill or the time to have been able to move this project forward without the wonderful tools that I was able to use.

It is a wonderful time to be a programmer and that is thanks to the open source community in a major way.

- Ubuntu Linux
- DebianStretch Linux
- Perf\_events
- LibPfm4
- Python3
- ScikitLearn
- Pandas
- Matplotlib
- Stress

