   For this lab, we were tasked with acquainting ourselves with the hardware and software that will be used over the course of the class. The software we used is a design tool made my Xilinx and the hardware was a FPGA digital logic board. The lab was broken into two parts. In the first, we were tasked with implementing a given 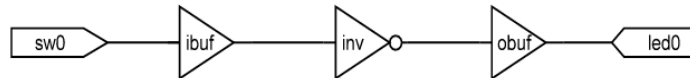circuit (image A) into Xilinx and upload it to the FPGA. This process was simple and took little time to do, but there was some difficulty as we were learning the ins and outs of the software

Image A: The circuit for the first task

simultaneously. The design was completed on Xilinx, but we were unable to upload the design to the FPGA since account we were working from was locked out. Unable to figure out the issue, we continued onto the second task since we had achieved the goal of the first task, which was to familiarize ourselves with Xilinx. The second task had us design a 3-bit full adder and a binary to hexadecimal converter in Xilinx and upload it to the FPGA where it would be displayed on the numeric display that the FPGA is connected to. I set out to design the logic for the adder and my lab partner, Nicholas, designed the binary to hexadecimal converter. The final adder design was implemented into Xilinx, but Nicholas had trouble implementing the converter design. What he did instead was route the outputs to LEDs 0-3 instead of the numeric display provided (image B). The issue that arose in the first part of the lab was prevalent in the second part, so we were also unable to test the design for this part.
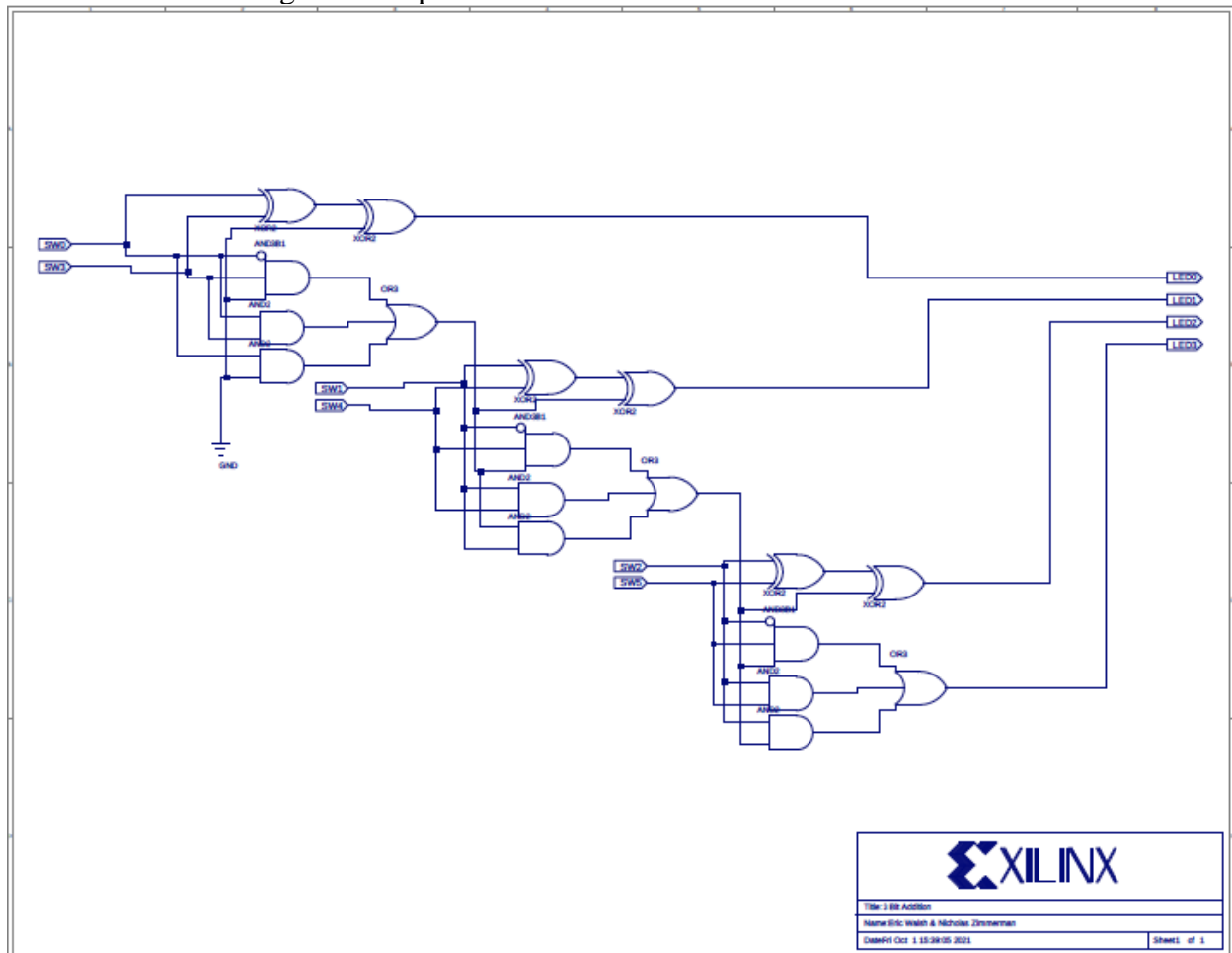

Image B: The Design for the second part