The objective of this lab was to create a finite state machine that measures the time between two button presses. The timer would only count up to 99 using binary coded decimals. Once the timer reached 99, it was to go into an error state. In the process of completing the lab, we ran into issues getting the lab to run on the FPGA. The issue was resolved by changing the output states from states C and D to states B and C (as seen on the attached schematic) which is seen in the logic from figure 1. With the issue resolved, the state machine ran as expected.

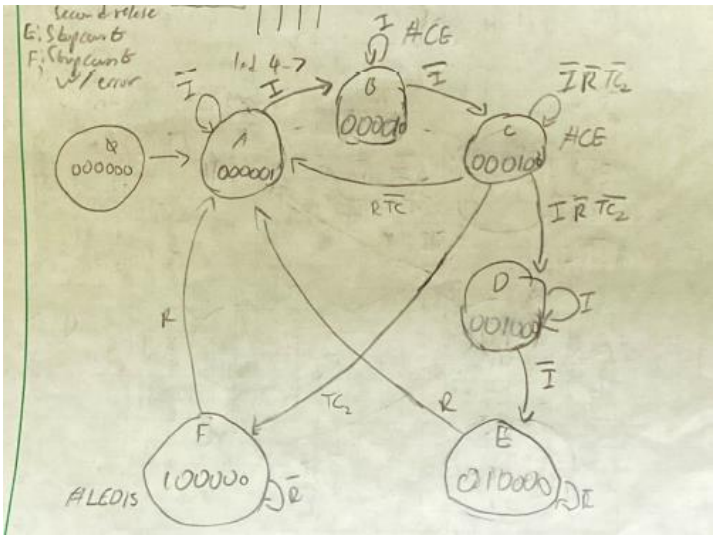


Figure 1: State diagram

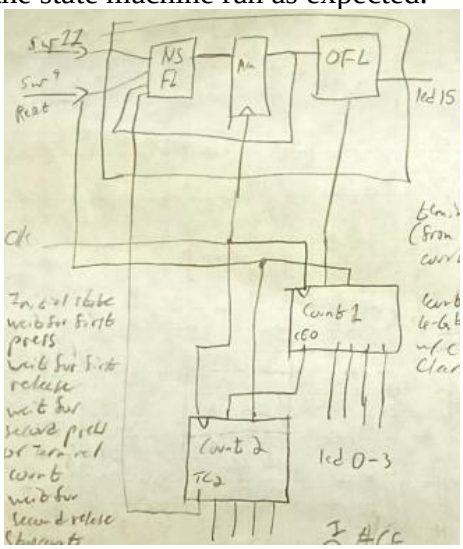
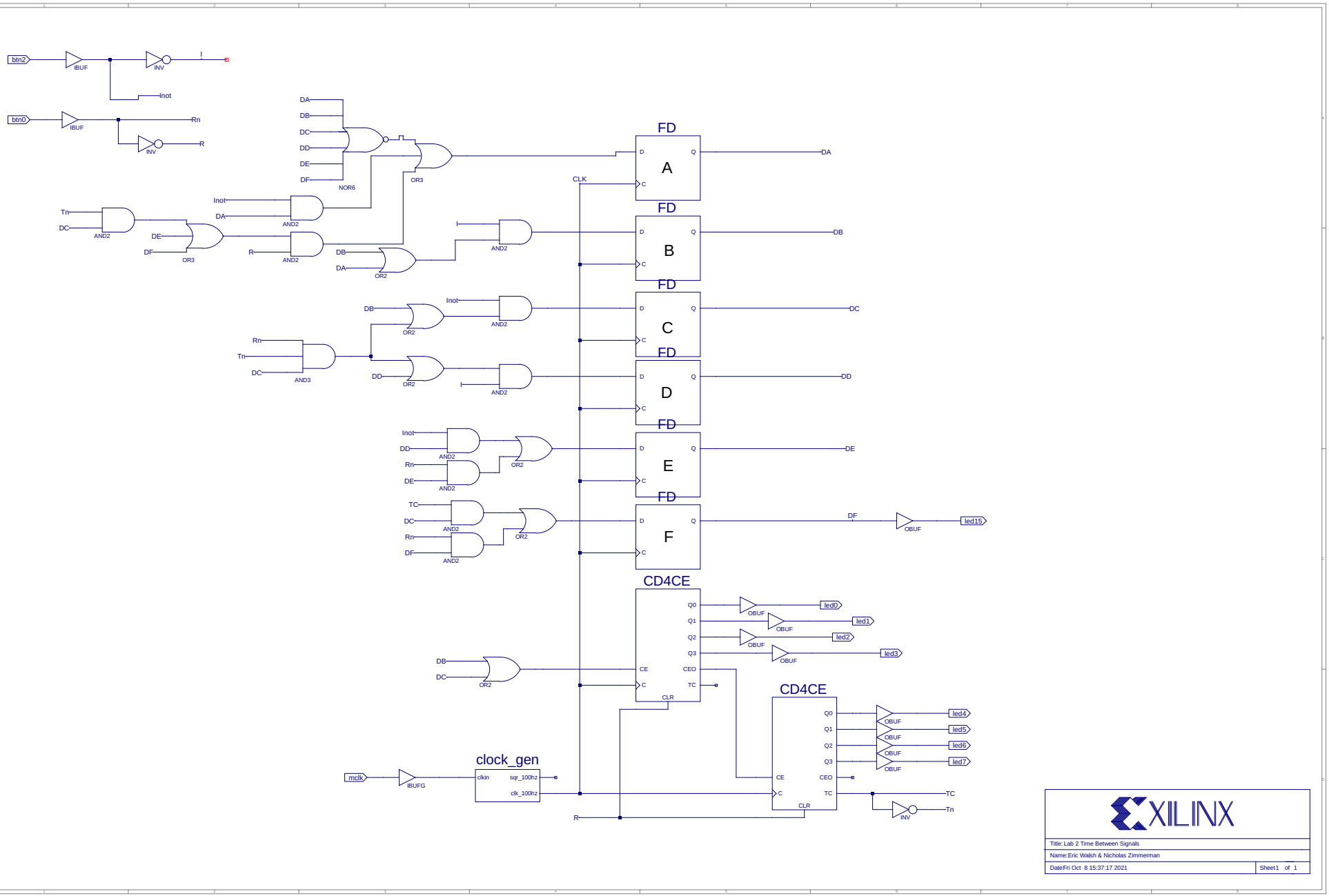


Figure 2: Block Diagram


btn2
IBUF
INV
I
Inot
btn0
IBUF
Rn
INV
R
DA
DB
DC
DD
DE
DF
NOR6
OR3
Tn
DC
AND2
DE
DF
OR3
Inot
DA
AND2
R
AND2
DB
DA
OR2
I
AND2
FD
A
D
Q
C
CLK
DA
FD
B
DB
FD
C
DC
FD
D
DD
FD
E
DE
FD
F
DF
OBUF
led15
DB
OR2
Inot
AND2
Rn
Tn
DC
AND3
DD
OR2
I
AND2
Inot
DD
AND2
Rn
DE
AND2
OR2
TC
DC
AND2
Rn
DF
AND2
OR2
CD4CE
Q0
Q1
Q2
Q3
CE
CEO
TC
C
CLR
OBUF
led0
led1
led2
led3
DB
DC
OR2
CD4CE
Q0
Q1
Q2
Q3
CE
CEO
TC
C
CLR
OBUF
led4
led5
led6
led7
TC
Tn
INV
R
clock_gen
mclk
IBUFG
clkin
sqr_100hz
clk_100hz
XILINX
Title: Lab 2 Time Between Signals
Name: Eric Walsh & Nicholas Zimmerman
Date Fri Oct 8 15:37:17 2021
Sheet 1 of 1