The objective of this lab was to create a finite state machine that measures the time between two button presses. The timer would only count up to 99 using binary coded decimals. Once the timer reached 99, it was to go into an error state. In the process of completing the lab, we ran into issues getting the lab to run on the FPGA. The issue was resolved by changing the output states from states C and D to states B and C (as seen on the attached schematic) which is seen in the logic from figure 1. With the issue resolved, the state machine ran as expected.

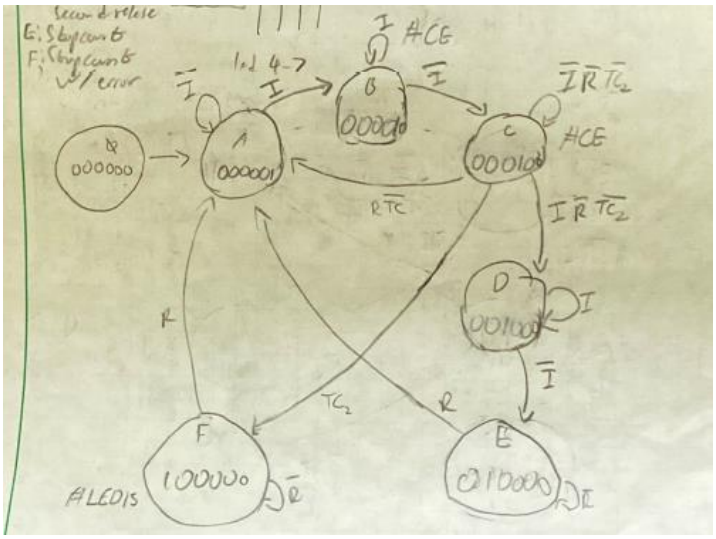

Figure 1: State diagram

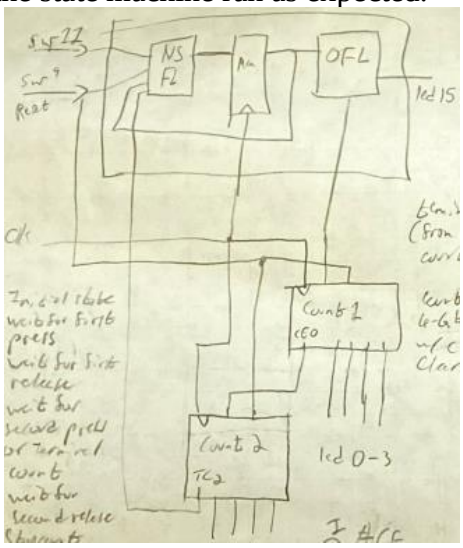

Figure 2: Block Diagram