

Abstract

The goal of this lab was to create a stopwatch using the provided FPGA and the ISE. The stopwatch was to have 4 digits the counts 0 to 99.99 seconds, and then goes into an error state. The device builds on the counter created from last week. The counter was changed in that it used the 7-segment display instead of the LEDs. The range of the counter was increased from 999 microseconds to 99 seconds. The error state and the input buttons remained the same. The primary task of the lab was to then apply these changes to the previously made device. This means that the state machine and input logic of the device did not need to be changed. The only changes made were to the output logic. These changes included increasing the number of counters from two to four, adding 8:1 multiplexers, adding a 16 bit RAM, and adding a BCD to 7-segment display converter (as seen in the attached schematic). The project ended with success, but not without issues.

The Issues and Credits

The first issue we came across after completing the design was an Maplib error. Specifically, errors 978 and 979. The errors complained that some input pins didn't have and inputs. We realized that the input bus on the RAM wasn't grounded. After adding a ground to each input on the bus, the error went away, and we were able to successfully upload the schematic to the FPGA. The next issue that arose was that the display was not functioning as intended. The first issue was that the far-right digit was increasing at the rate of the hundredths place (which is supposed to be on the far right), the far-right digit was increasing at the rate of the tenths place, the colon only had one of its dots lit, and the apostrophe was lit. To fix this, we went back to the hex and binary numbers we found for the RAM and made sure that they were correct and went back to the 8:1 multiplexers and made sure that those were outputting to the right input on the BCD to 7-segment display converter. We found the issue with the binary and re-uploaded the schematic. The final design worked as intended. The display would count from 0 to 99.99 seconds, go into an error state when it reaches 99.99, stop when sw11 is pressed and reset when sw9 was pressed.

The clock generator and the 7-segment decoder blocks and logic were proved to us by Dr. Larry Aamodt.

