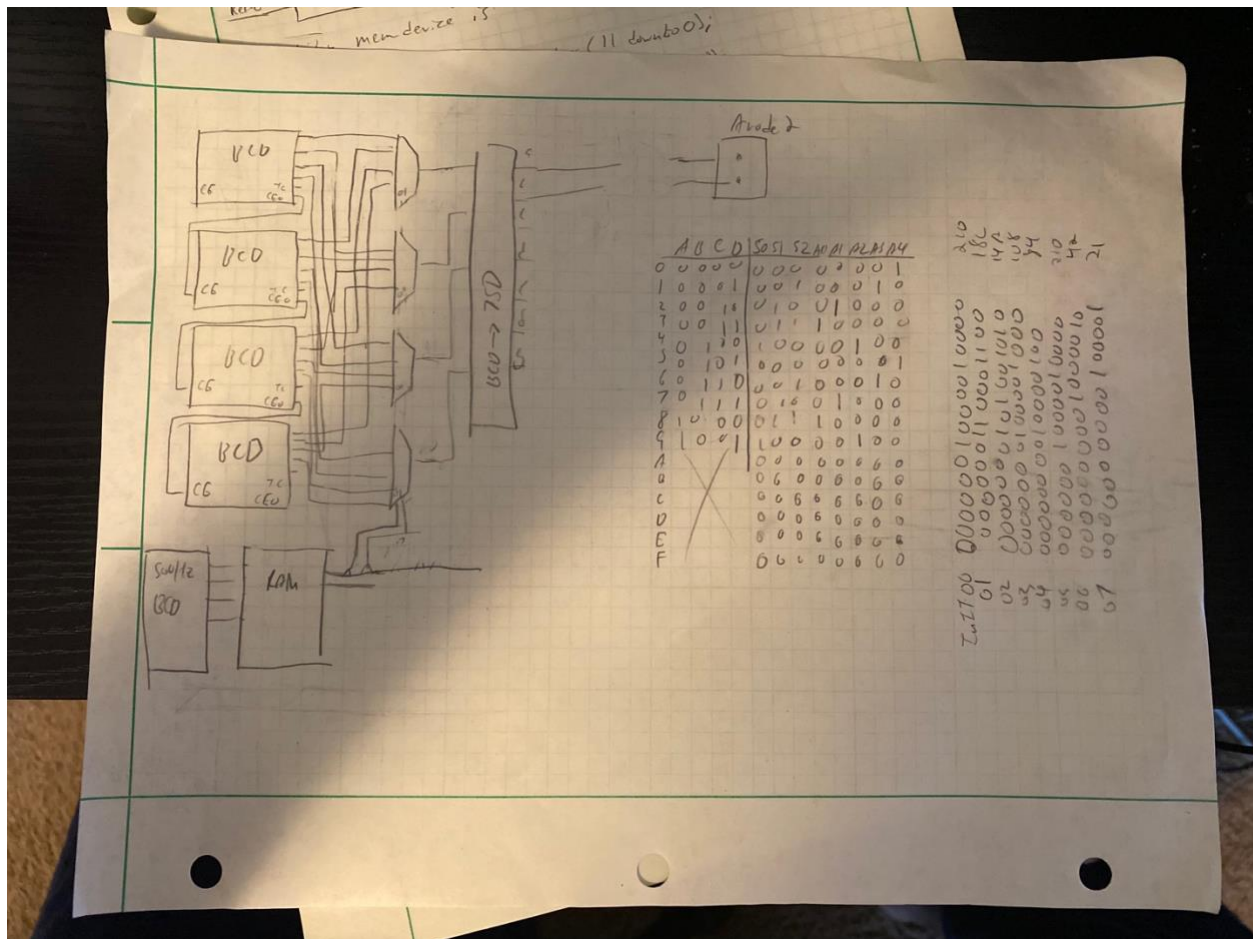## Abstract

        The goal of this lab was to create a stopwatch using the provided FPGA and the ISE. The stopwatch was to have 4 digits the counts 0 to 99.99 seconds, and then goes into an error state. The device builds on the counter created from last week. The counter was changed in that it used the 7-segmend display instead of the LEDs. The range of the counter was increased from 999 microseconds to 99 seconds. The error state and the input buttons remained the same. The primary task of the lab was to then apply these changes to the previously made device. This means that the state machine and input logic of the device did not need to be changed. The only changes made were to the output logic. These changes included increasing the number of counters from two to four, adding 8:1 multiplexers, adding a 16 bit RAM, and adding a BCD to 7-segment display converter (as seen in the attached schematic). The project ended with success, but not without issues.
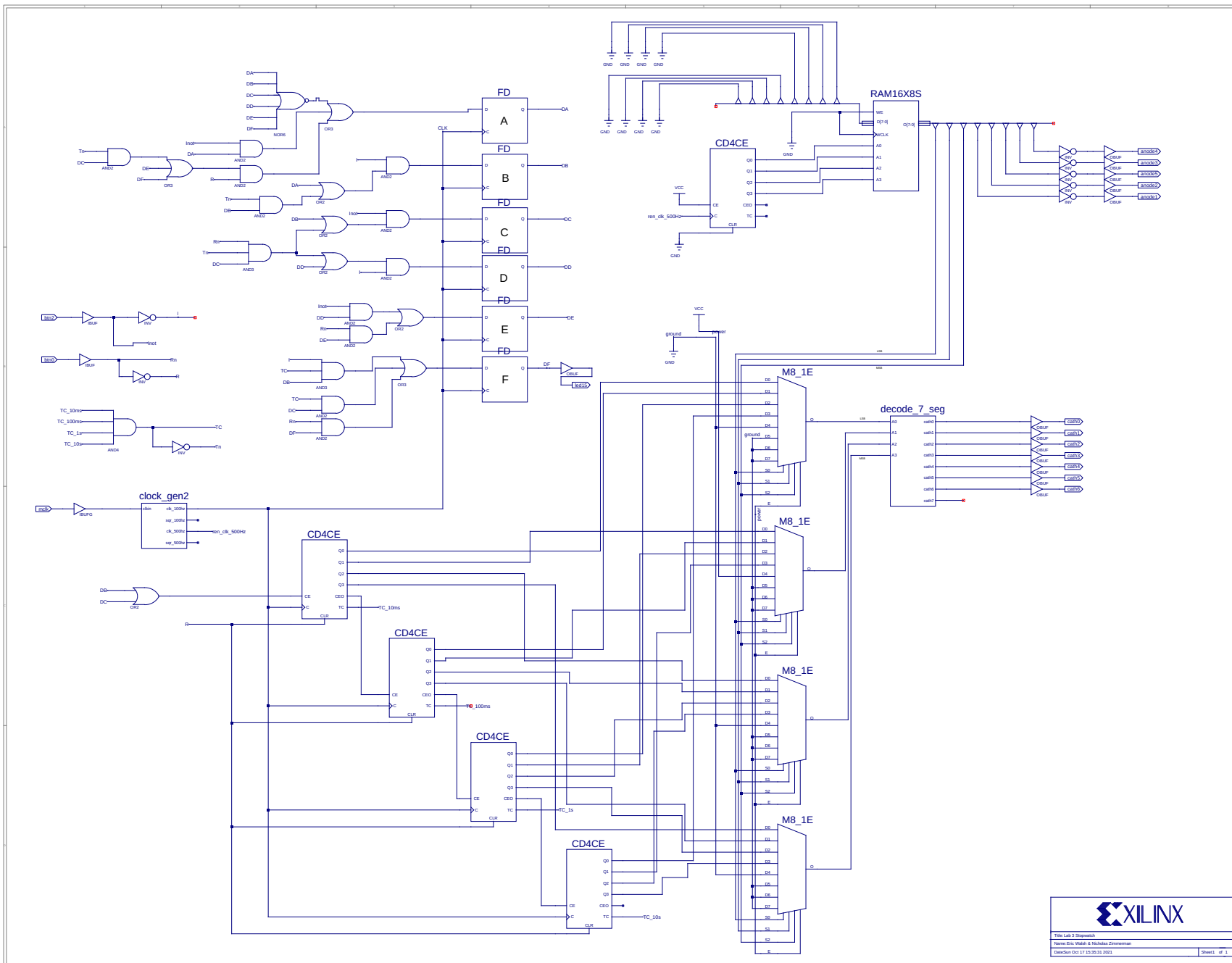
The Issues and Credits

        The first issue we came across after completing the design was an Maplib error. Specifically, errors 978 and 979. The errors complained that some input pins didn't have and inputs. We realized that the input bus on the RAM wasn't grounded. After adding a ground to each input on the bus, the error went away, and we were able to successfully upload the schematic to the FPGA. The next issue that arose was that the display was not functioning as intended. The first issue was that the far-right digit was increasing at the rate of the hundredths place (which is supposed to be on the far right), the far-right digit was increasing at the rate of the tenths place, the colon only had one of its dots lit, and the apostrophe was lit. To fix this, we went back to the hex and binary numbers we found for the RAM and made sure that they were correct and went back to the 8:1 multiplexers and made sure that those were outputting to the right input on the BCD to 7-segment display converter. We found the issue with the binary and re-uploaded the schematic. The final design worked as intended. The display would count from 0 to 99.99 seconds, go into an error state when it reaches 99.99, stop when sw11 is pressed and reset when sw9 was pressed.

        The clock generator and the 7-segment decoder blocks and logic were proved to us by Dr. Larry Aamodt.

The Block Diagram and scratch work

XILINX

FD

A

FD

B

FD

C

FD

D

FD

E

FD

F

DA
DB
DC
DD
DE
DF
NOR6
OR3

Tn
DC
AND2
Inot
DA
AND2
DE
DF
OR3
Rn
AND2

DA
OR2
Tn
DB
AND2
DB
OR2
Inot
AND2

Tn
DC
AND3
DD
OR2
AND2

Inot
DD
AND2
Rn
OR2
DE
AND2

TC
DB
AND3
TC
DC
AND2
Rn
DF
AND2
OR3

CLK

DA
DB
DC
DD
DE
DF

OBUF
led15

btn2
IBUF
INV

btn0
IBUF
Rn
INV
R
Inot

TC_10ms
TC_100ms
TC_1s
TC_10s
AND4
INV
TC
INV
Tn

clock_gen2
clkin
clk_100hz
sqr_100hz
clk_500hz
ren_clk_500Hz
sqr_500hz

mclk
IBUFG

CD4CE
Q0
Q1
Q2
Q3
CE
CEO
C
TC
CLR
TC_10ms

DB
DC
OR2

R

CD4CE
Q0
Q1
Q2
Q3
CE
CEO
C
TC
CLR
TC_100ms

CD4CE
Q0
Q1
Q2
Q3
CE
CEO
C
TC
CLR
TC_1s

CD4CE
Q0
Q1
Q2
Q3
CE
CEO
C
TC
CLR
TC_10s

GND GND GND GND

GND GND GND GND

RAM16X8S
WE
D[7:0]
WCLK
A0
A1
A2
A3
O[7:0]

CD4CE
Q0
Q1
Q2
Q3
CE
CEO
C
TC
CLR
VCC
ren_clk_500Hz

GND

VCC
ground
power
GND

M8_1E
D0
D1
D2
D3
D4
D5
D6
D7
S0
S1
S2
E
Q
ground

M8_1E
D0
D1
D2
D3
D4
D5
D6
D7
S0
S1
S2
E
Q
power

M8_1E
D0
D1
D2
D3
D4
D5
D6
D7
S0
S1
S2
E
Q

M8_1E
D0
D1
D2
D3
D4
D5
D6
D7
S0
S1
S2
E
Q

decode_7_seg
A0
A1
A2
A3
cath0
cath1
cath2
cath3
cath4
cath5
cath6
cath7

OBUF
OBUF
OBUF
OBUF
OBUF
OBUF
OBUF
OBUF
cath0
cath1
cath2
cath3
cath4
cath5
cath6
cath7

INV
INV
INV
INV
INV
OBUF
OBUF
OBUF
OBUF
OBUF
anode4
anode3
anode5
anode2
anode1

```
Release 14.7 Map P.20131013 (lin64)
Xilinx Mapping Report File for Design 'top_sch_pressTwice'

Design Information
------------------
Command Line   : map -intstyle ise -p xc7a100t-fgg676-1 -w -logic_opt off -ol
high -t 1 -xt 0 -register_duplication off -r 4 -mt off -ir off -pr off -lc off
-power off -o top_sch_pressTwice_map.ncd top_sch_pressTwice.ngd
top_sch_pressTwice.pcf
Target Device  : xc7a100t
Target Package : fgg676
Target Speed   : -1
Mapper Version : artix7 -- $Revision: 1.55 $
Mapped Date    : Thu Oct 14 12:07:46 2021


Design Summary
--------------
Number of errors   :  16
Number of warnings :   5


Section 1 - Errors
------------------
ERROR:MapLib:979 - LUT6 symbol "XLXI_591/Mmux_S2_D7_Mux_0_o_4" (output
   signal=XLXI_591/Mmux_S2_D7_Mux_0_o_4) has input signal "O<1>" which will be
   trimmed. See Section 5 of the Map Report File for details about why the input
   signal will become undriven.
ERROR:MapLib:979 - LUT6 symbol "XLXI_591/Mmux_S2_D7_Mux_0_o_4" (output
   signal=XLXI_591/Mmux_S2_D7_Mux_0_o_4) has input signal "O<0>" which will be
   trimmed. See Section 5 of the Map Report File for details about why the input
   signal will become undriven.
ERROR:MapLib:979 - LUT6 symbol "XLXI_592/Mmux_S2_D7_Mux_0_o_4" (output
   signal=XLXI_592/Mmux_S2_D7_Mux_0_o_4) has input signal "O<1>" which will be
   trimmed. See Section 5 of the Map Report File for details about why the input
   signal will become undriven.
ERROR:MapLib:979 - LUT6 symbol "XLXI_592/Mmux_S2_D7_Mux_0_o_4" (output
   signal=XLXI_592/Mmux_S2_D7_Mux_0_o_4) has input signal "O<0>" which will be
   trimmed. See Section 5 of the Map Report File for details about why the input
   signal will become undriven.
ERROR:MapLib:979 - LUT6 symbol "XLXI_593/Mmux_S2_D7_Mux_0_o_4" (output
   signal=XLXI_593/Mmux_S2_D7_Mux_0_o_4) has input signal "O<1>" which will be
   trimmed. See Section 5 of the Map Report File for details about why the input
   signal will become undriven.
ERROR:MapLib:979 - LUT6 symbol "XLXI_593/Mmux_S2_D7_Mux_0_o_4" (output
   signal=XLXI_593/Mmux_S2_D7_Mux_0_o_4) has input signal "O<0>" which will be
   trimmed. See Section 5 of the Map Report File for details about why the input
   signal will become undriven.
ERROR:MapLib:979 - LUT6 symbol "XLXI_594/Mmux_S2_D7_Mux_0_o_4" (output
   signal=XLXI_594/Mmux_S2_D7_Mux_0_o_4) has input signal "O<1>" which will be
   trimmed. See Section 5 of the Map Report File for details about why the input
   signal will become undriven.
ERROR:MapLib:979 - LUT6 symbol "XLXI_594/Mmux_S2_D7_Mux_0_o_4" (output
   signal=XLXI_594/Mmux_S2_D7_Mux_0_o_4) has input signal "O<0>" which will be
   trimmed. See Section 5 of the Map Report File for details about why the input
   signal will become undriven.
ERROR:MapLib:978 - LUT6 symbol "XLXI_591/Mmux_S2_D7_Mux_0_o_4" (output
   signal=XLXI_591/Mmux_S2_D7_Mux_0_o_4) has an equation that uses input pin I0,
   which no longer has a connected signal. Please ensure that all the pins used
   in the equation for this LUT have signals that are not trimmed (see Section 5
   of the Map Report File for details on which signals were trimmed).
ERROR:MapLib:978 - LUT6 symbol "XLXI_591/Mmux_S2_D7_Mux_0_o_4" (output
   signal=XLXI_591/Mmux_S2_D7_Mux_0_o_4) has an equation that uses input pin I1,
```

which no longer has a connected signal. Please ensure that all the pins used
in the equation for this LUT have signals that are not trimmed (see Section 5
of the Map Report File for details on which signals were trimmed).
ERROR:MapLib:978 - LUT6 symbol "XLXI_592/Mmux_S2_D7_Mux_0_o_4" (output
signal=XLXI_592/Mmux_S2_D7_Mux_0_o_4) has an equation that uses input pin I0,
which no longer has a connected signal. Please ensure that all the pins used
in the equation for this LUT have signals that are not trimmed (see Section 5
of the Map Report File for details on which signals were trimmed).
ERROR:MapLib:978 - LUT6 symbol "XLXI_592/Mmux_S2_D7_Mux_0_o_4" (output
signal=XLXI_592/Mmux_S2_D7_Mux_0_o_4) has an equation that uses input pin I1,
which no longer has a connected signal. Please ensure that all the pins used
in the equation for this LUT have signals that are not trimmed (see Section 5
of the Map Report File for details on which signals were trimmed).
ERROR:MapLib:978 - LUT6 symbol "XLXI_593/Mmux_S2_D7_Mux_0_o_4" (output
signal=XLXI_593/Mmux_S2_D7_Mux_0_o_4) has an equation that uses input pin I0,
which no longer has a connected signal. Please ensure that all the pins used
in the equation for this LUT have signals that are not trimmed (see Section 5
of the Map Report File for details on which signals were trimmed).
ERROR:MapLib:978 - LUT6 symbol "XLXI_593/Mmux_S2_D7_Mux_0_o_4" (output
signal=XLXI_593/Mmux_S2_D7_Mux_0_o_4) has an equation that uses input pin I1,
which no longer has a connected signal. Please ensure that all the pins used
in the equation for this LUT have signals that are not trimmed (see Section 5
of the Map Report File for details on which signals were trimmed).
ERROR:MapLib:978 - LUT6 symbol "XLXI_594/Mmux_S2_D7_Mux_0_o_4" (output
signal=XLXI_594/Mmux_S2_D7_Mux_0_o_4) has an equation that uses input pin I0,
which no longer has a connected signal. Please ensure that all the pins used
in the equation for this LUT have signals that are not trimmed (see Section 5
of the Map Report File for details on which signals were trimmed).
ERROR:MapLib:978 - LUT6 symbol "XLXI_594/Mmux_S2_D7_Mux_0_o_4" (output
signal=XLXI_594/Mmux_S2_D7_Mux_0_o_4) has an equation that uses input pin I1,
which no longer has a connected signal. Please ensure that all the pins used
in the equation for this LUT have signals that are not trimmed (see Section 5
of the Map Report File for details on which signals were trimmed).

Section 2 - Warnings

WARNING:MapLib:701 - Signal anode2 connected to top level port anode2 has been
removed.
WARNING:MapLib:701 - Signal anode3 connected to top level port anode3 has been
removed.
WARNING:MapLib:701 - Signal anode5 connected to top level port anode5 has been
removed.
WARNING:MapLib:701 - Signal anode4 connected to top level port anode4 has been
removed.
WARNING:MapLib:701 - Signal anode1 connected to top level port anode1 has been
removed.

Section 3 - Informational

Section 4 - Removed Logic Summary
----
  37 block(s) removed
   5 block(s) optimized away
  39 signal(s) removed

Section 5 - Removed Logic

The trimmed logic report below shows the logic removed from your design due to
sourceless or loadless signals, and VCC or ground connections. If the removal