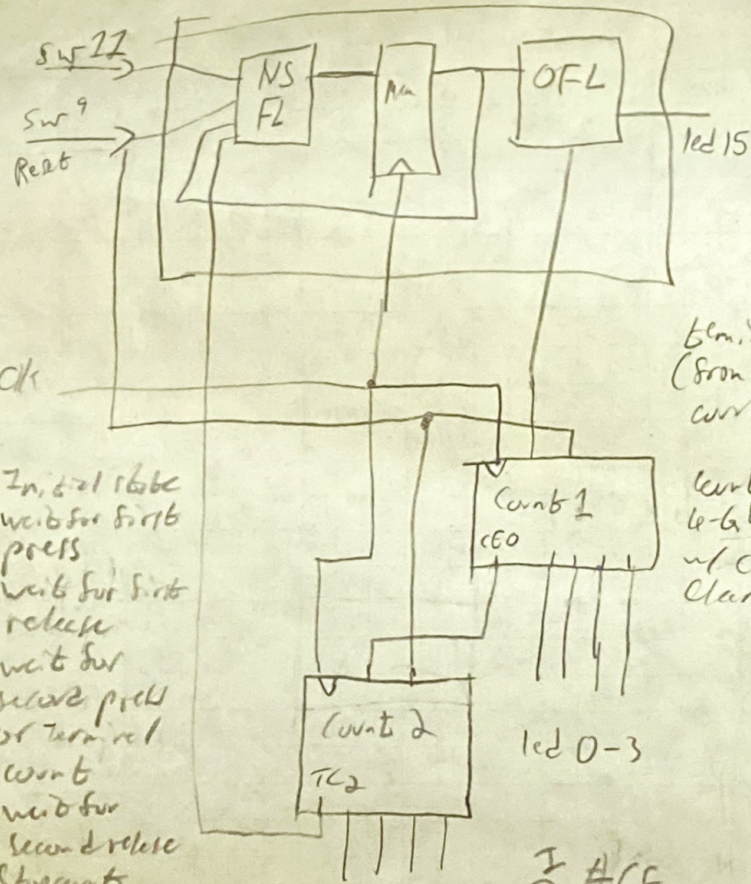


# Design

clk @ 10kHz

CD4CE

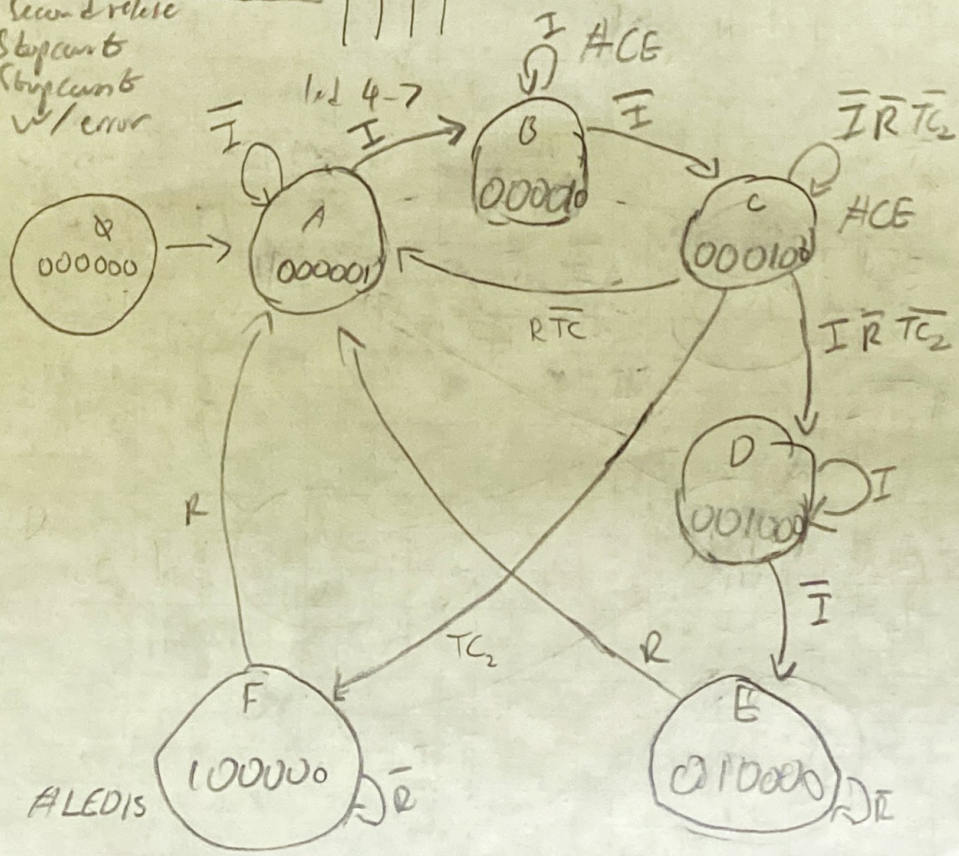


States  
 wait for first press  
 wait for second press  
 reset  
 stop counter no error  
 stop counter w/ error

SW 11 = I (input)  
 SW 9 = K (reset)  
 Terminating count = TC<sub>2</sub>  
 (from second counter)

- A: Initial state
- A: wait for first press
- B: wait for first release
- C: wait for second press or terminal count
- D: wait for second release
- E: Stop counter
- F: Stop counter w/ error

counter 1: CD4CE  
 4-bit asynchronous BCD counter  
 w/ clock enable & asynchronous clear.





$I RT_C$	Prime Side F E D C B A	Next Side A Q <sub>1</sub> Q <sub>2</sub> Q <sub>3</sub> Q <sub>4</sub>
0 0 0	0 0 0 0 0 0	0 0 0 0 0 1
0 0 1	0 0 0 0 0 1	0 0 0 0 0 1
1 0 0	0 0 0 0 0 1	0 0 0 0 1 0
1 0 1	0 0 0 0 1 0	0 0 0 0 1 0
0 0 0	0 0 0 0 1 0	0 0 0 1 0 0
0 0 0	0 0 0 1 0 0	0 0 0 1 0 0
0 1 0	0 0 0 1 0 0	0 0 0 0 0 1
0 0 1	0 0 0 1 0 0	1 0 0 0 0 0
1 0 0	0 0 0 1 0 0	0 0 1 0 0 0
1 0 0	0 0 1 0 0 0	0 0 1 0 0 0
0 0 0	0 0 1 0 0 0	0 1 0 0 0 0
0 0 0	0 1 0 0 0 0	0 1 0 0 0 0
0 0 0	0 1 0 0 0 0	0 0 0 0 0 1
0 0 0	1 0 0 0 0 0	1 0 0 0 0 0
0 1 0	1 0 0 0 0 0	0 0 0 0 0 1

$$D_A = \overline{F} \overline{E} \overline{D} \overline{C} \overline{B} \overline{A} + \overline{I} A + R \overline{T}_C C$$

$$+ R E + R F$$

$$D_B = I A + I B$$

$$Q_1 = \overline{I} B + \overline{I} R \overline{T}_C C$$

$$D_D = I R \overline{T}_C C + I D$$

$$D_E = \overline{I} D + R E$$

$$D_F = \overline{T}_C C + R F$$

$$C E = C + D$$

$$L E D 15 = F$$

$$D_A = \overline{F} \overline{E} \overline{D} \overline{C} \overline{B} \overline{A} + \overline{I} A + R (\overline{T}_C C + E + F)$$

$$D_B = I (C + D)$$

$$D_C = \overline{I} (B + R \overline{T}_C C)$$

$$D_D = I (R \overline{T}_C C + D)$$

$$D_E = \overline{T}_C C + R F$$

- 0 P23
- 1 P24
- 2 N21
- 3 N22
- 4 M24
- 5 M25
- 6 R26
- 7 P26